EMC-Optimized converter using Power GaN devices

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EMC-Optimized converter using Power GaN devices

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Abstract

The thesis investigates the possibility of EMI mitigation for power electronic converters with GaN transistors in three key areas: control strategy, layout design, and integrated magnetic filter. Based on a Buck converter, the contribution of hard and soft switching to the generated conducted noise (Common Mode (CM) and Differential Mode (DM)) has been investigated. The positive effect of soft switching on EMI reduction in a specific frequency range was demonstrated. The impact of layout design attributes was also observed and the need to optimize it was highlighted. Next, a detailed study of the identification of parasitic elements in a single inverter leg is presented. Specific areas of concern were detailed and considered later in the thesis. The developed simulation workflow in Digital Twin used to study the impact of individual layout elements on EMC is presented. The laboratory test bench used for EMC measurements is also presented, together with a description of the necessary experimental precautions. Furthermore, the two key concepts implemented in the layout - shielding and Power-Chip-on-Chip (PCoC) - are presented. Their effectiveness in reducing EMI by almost 20 dB was confirmed by simulation and experiment. Finally, the Integrated Inductor concept is presented, which can be implemented together with the previous solutions. The effectiveness of a planar Integrated Inductor connected to the middle point of the bridge was demonstrated by simulation studies. The author's method for identifying the impedance of the Integrated Inductor and the key parasitic elements (in terms of EMC) has also been developed and presented in details. In conclusion, the work presents a series of solutions that significantly reduce EMI in GaN-based converters, which have been validated by simulation and experiment and can be applied to all types of power electronic converters.

Résumé

Cette thèse étudie les possibilités de réduction des interférences électromagnétiques pour les convertisseurs d'électroniques de puissance utilisant des transistors GaN dans trois domaines principaux: la stratégie de contrôle, la conception des circuits imprimés ainsi que l'agencement des composants de puissance et les éléments magnétiques à haute fréquence. Sur la base d'un convertisseur Buck, l'impact de la contribution de la commutation dure et douce sur le bruit conduit généré (mode commun (CM) et mode différentiel (DM)) a été étudiée. L'effet positif de la commutation douce sur la réduction des perturbations CEM dans une gamme de fréquence spécifique a été démontré. L'impact des attributs de la conception de l'agencement a également été observé et la nécessité de l'optimiser a été soulignée. Ensuite, une étude détaillée de l'identification des éléments parasites dans un seul bras d'onduleur est présentée. Des domaines spécifiques de préoccupation ont été détaillés et examinés plus loin dans la thèse. Le flux de travail de simulation développé dans Digital Twin utilisé pour étudier l'impact des éléments de disposition individuels sur la CEM est présenté. Le banc d'essai de laboratoire utilisé pour les mesures CEM est également présenté, ainsi qu'une description des précautions nécessaires. En outre, les deux concepts clés mis en œuvre dans l'agencement - le blindage et le Power-Chip-on-Chip (PCoC) - sont présentés. Leur efficacité dans la réduction des interférences électromagnétiques de près de 20 dB a été confirmée par la simulation et l'expérimentation. Enfin, le concept d'inducteur intégré est présenté, qui peut être mis en œuvre en même temps que les solutions précédentes. L'efficacité d'un inducteur intégré planaire connecté au point central du pont a été démontrée par des études de simulation. La méthode de l'auteur pour identifier l'impédance de l'inducteur intégré et les principaux éléments parasites (en termes de CEM) a également été développée et présentée en détail. En conclusion, ce travail présente une série de solutions qui réduisent de manière significative l'EMI dans les convertisseurs à base de GaN, qui ont été validées par simulation et expérience et qui peuvent être appliquées à tous les types de convertisseurs électroniques de puissance.

Streszczenie

W niniejszej rozprawie zbadano możliwości ograniczania zakłóceń elektromagnetycznych w przekształtnikach energoelektronicznych z tranzystorami GaN w trzech kluczowych obszarach: strategii sterowania, projektowaniu geometrii układu ścieżek obwodów drukowanych i elementów magnetycznych wysokiej częstotliwości. W oparciu o przekształtnik Buck zbadano wpływ twardego i miękkiego przełączania na generowane zaburzenia przewodzone (tryb wspólny (CM) i tryb różnicowy (DM)). Wykazano pozytywny wpływ miękkiego przełączania na redukcję EMI w określonym zakresie częstotliwości. Zaobserwowano również wpływ negatywny geometrii ścieżek na przebiegi elektryczne i podkreślono potrzebę jej optymalizacji. Następnie przedstawiono szczegółowe badanie identyfikacji elementów pasożytniczych w pojedynczej gałęzi falownika. Poszczególne obszary wymagające szczególnej uwagi zostały wyszczególnione i rozważane w dalszej części pracy. Przedstawiono opracowany szablon wieloplatformowej symulacji (Digital Twin), który został wykorzystany do badania wpływu poszczególnych elementów układu na EMC. Przedstawiono również stanowisko laboratoryjne wykorzystywane do pomiarów EMC wraz z opisem zastosowanych niezbędnych wymagań metrologicznych. Ponadto zaprezentowano dwie kluczowe koncepcje zastosowane w układzie - ekranowanie i Power-Chip-on-Chip (PCoC). Ich skuteczność w redukcji EMI o prawie 20 dB została potwierdzona symulacyjnie i eksperymentalnie. Na koniec przedstawiono ideę zintegrowanej cewki, którą można wdrożyć razem z poprzednimi rozwiązaniami. Skuteczność zintegrowanej cewki planarnej podłączonej do punktu środkowego mostka została wykazana w badaniach symulacyjnych. Opracowano i szczegółowo omówiono autorską metodę identyfikacji impedancji zintegrowanej cewki wraz z wyznaczeniem wartości kluczowych (pod względem EMC) elementów pasożytniczych. Podsumowując, w pracy przedstawiono szereg rozwiązań, które znacznie zmniejszają zakłócenia elektromagnetyczne w przekształtnikach opartych na tranzystorach GaN, które zostały zweryfikowane symulacyjnie i eksperymentalnie oraz mogą być stosowane we wszystkich typach przekształtników energoelektronicznych.

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Abbreviations

2D	Two-Dimensional
2DEG	Two-Dimensional Electron Gas
3D	Three-Dimensional
AC	Alternating Current
AlAs	Aluminum Arsenide
AlN	Aluminum Nitride
BEV	Battery Electric Vehicle
CAD	Computer Aided Design
CAM	Computer Aided Manufacturing
CISPR	Comité International Spécifique pour les Radiofréquences
CM	Common-Mode
CMC	Common-Mode Choke
D-Mode GaN	Depletion-Mode GaN Transistor
DC	Direct Current
DCM	Discontinuous Current Mode
DM	Differential-Mode
E-Mode GaN	Enhancement-Mode GaN Transistor
EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interferences
E&RM	Electrostatic & Resonant frequency Method
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
EUT	Equipment Under Test
EV	Electric Vehicle
FCC	Federal Communications Commission
FCEV	Fuel Cell Electric Vehicle

FET	Field-Effect Transistor
FFT	Fast Fourier Transform
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GHG	Greenhouse Gases
GIT	Gate Injection Transistor
HEMT	High Electron Mobility Transistor
HF	High Frequency
HFET	Heterojunction Field Effect Transistor
HVDC	High Voltage Direct Current
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IGBT	Insulated-Gate Bipolar Transistor
IMS	Insulated Metal Substrate
JFET	Junction Field-Effect Transistor
LF	Low Frequency
LISN	Line Impedance Stabilizing Network
MEA	More Electric Aircraft
MID	Middle Point
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PCoC	Power-Chip-on-Chip
PE	Power Electronics
PEEC	Partial Elements Equivalent Circuit
PHEV	Plug-in Hybrid Electric Vehicle
PV	Photovoltaic
RM	Resonant frequency Method
Si	Silicone
SiC	Silicone Carbide
SMD	Surface-Mount Device
SST	Solid State Transformer
TCM	Triangular Current Mode
UPS	Uninterruptible Power Supply
WBG	Wide-Bandgap
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

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Chapter 1

Introduction

"Science is a way of thinking much more than it is a body of knowledge."

Carl Sagan

1.1 Motivation

Today, intensive research and technological development provide increasingly sophisticated goods that improve our quality of life. The demand for these goods is also growing, forcing the construction of new factories, mines, supply chains, etc. In addition, combining this fact with the growing population of our Planet, which has exceeded the staggering 8 billion lives (November 15, 2022; Fig. 1.1 [7]), and therefore growing needs for food, social, transportation, etc., the production of greenhouse gases (GHGs) steadily increases. Therefore, the harmful effects of human impact on the planet have been noticeable in recent years. The emitted greenhouse gases are not only harmful to the environment but also to human beings. Increased concentrations of greenhouse gases are causing climate change to occur at a much faster rate than predicted, with catastrophic consequences [3]. Increasing concentrations of CO_2, global warming and rising sea levels [18] are being reflected in more numerous local disasters, leading to greater public and political awareness.

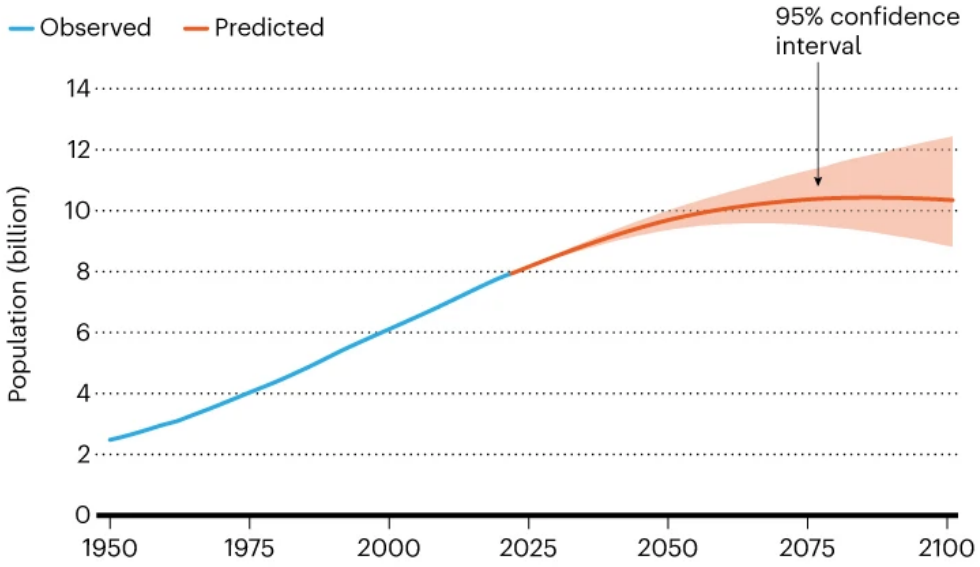
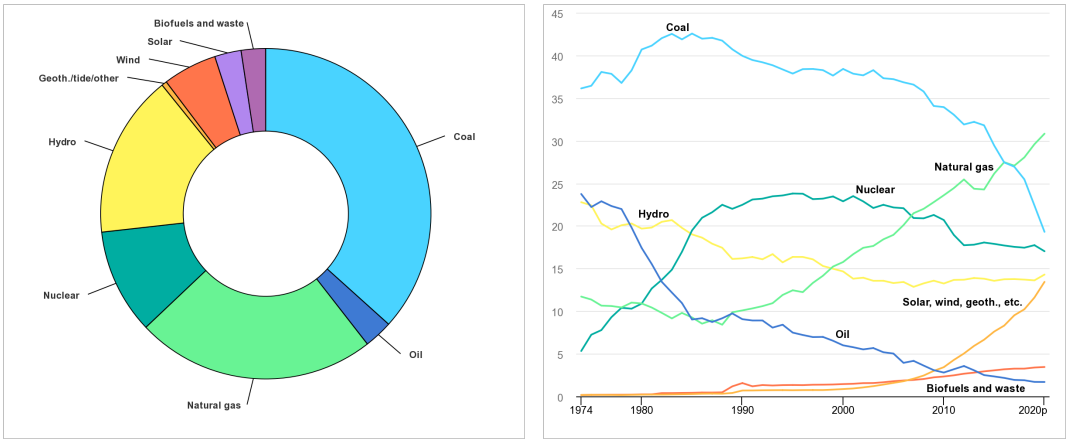


Figure 1.1: Global population prediction [7]

To mitigate the effects of climate change, further development strategies are being introduced, such as those defined by the European Commission, which aims to achieve climate neutrality by 2050 [23] (reducing net greenhouse gas emissions by at least 55% by 2030 compared to 1990 levels). The idea is an economy with net-

zero greenhouse gas emissions in 2050. This goal is established in the European Green Deal and consistent with the Paris Agreement [40], the main provision of which is to limit the global average temperature increase to well below 2°C above pre-industrial levels and to pursue strongly the objective of limiting the temperature increase to 1.5°C above pre-industrial levels.

Achieving the desired goals will therefore require many changes in the energy generation sector, in decarbonization of transport, and in conscious use of electricity, as well as an overall increase in the efficiency of electrical appliances. To meet the growing demand for electricity, the modernization of existing infrastructure and the construction of new facilities should be based on modern renewable energy sources such as wind and solar power. According to Fig. 1.2, 13.4% of the world's electricity generation in 2020 will come from these (wind, solar, geothermal) renewable energy sources. However, in order to meet the goals of the European Commission and the Paris Agreement, their contribution should be 18% in 2030 and 32% in 2050 [69, 43]. Accordingly, the intensive deployment of these energy sources is necessary, which strongly depends on the available power conversion technologies, their reliability and efficiency.



(a) (b)

Figure 1.2: (a) World gross electricity production by source (2019) [4], (b) Share of OECD gross electricity production by source (1974-2020) [4]

Besides the power sector and industry, the transportation sector is the third largest source of GHG emissions related to human activities. Broadly speaking, GHG emissions are directly related to the use of fossil-fueled engines (combustion,

jet, gas, turbojet) in road vehicles, planes, railways, and ships. According to [5], transportation will account for 24% of global CO2 emissions in 2021. Changes in this sector have been underway for several years. This is mainly due to the intensive promotion of eco-friendly forms of transport such as personal Electric Vehicles (EV): Battery Electric Vehicles (BEVs), Plug-in Hybrid Electric Vehicles (PHEVs), Fuel Cell Electric Vehicles (FCEVs), and hybrid & electric public transport buses.

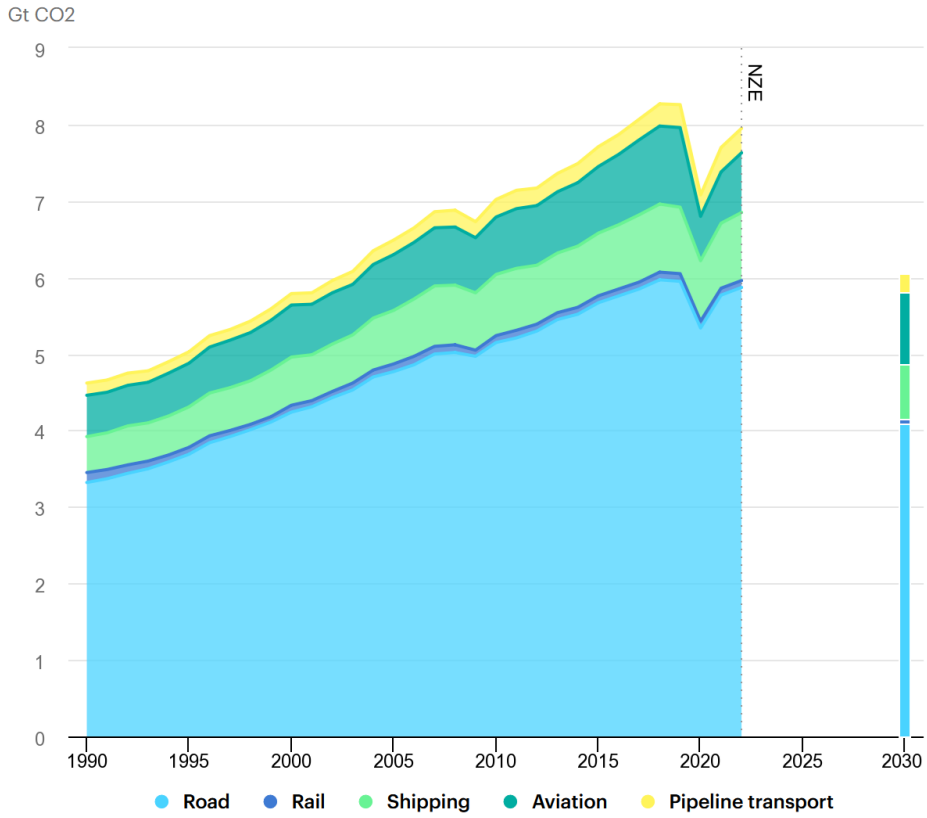


Figure 1.3: Global CO2 emissions from transport by sub-sector in the Net Zero Scenario, 2000-2030 [6]

Sales of electric cars continue to grow and in 2022 a rate of 10 million cars sold globally was reached, constituting 14% of total car sales [6]. Nevertheless, CO2 emissions from the transportation sector increase by 3% in 2022 (compared to 2021). Air transport was a major contributor, as demand rebounded after a difficult pandemic period, leading to an increase in air travel. In the field of avionics, work is also being done on the introduction of electric propulsion (MEA - More Electric Aircraft) [13, 33, 77, 89]. However, its development is not in line with the short-term perspective of implementation. In conclusion, systemic

changes are still needed in the field of transport as well. Achieving the Net Zero Emissions (NZE) scenario by 2050 is realistic, but will require a sustained 3% annual reduction in CO2 emissions from the transport sector until at least 2030 [6]. However, such radical technological changes in the transportation sector will lead to a significant increase in electricity demand. An increase of about 6 times in the EU and up to 32 times in the US is predicted [21, 57]. As a result, the development of the power generation sector will be significantly affected.

Accordingly, Next Generation Power Electronics such as EV drivetrain systems with on-board/off-board EV chargers, compact inverters for Photovoltaic (PVs) systems, wind turbine power systems, Solid State Transformers (SSTs), energy storage systems, fuel cell drives, next-generation traction vehicles play an important role and enable new types of devices to come to market relatively quickly. According to [83, 53], the amount of electricity processed by various types of power electronic devices in the U.S. is projected to be 80% by 2030. Given the above, power electronics will play a key role in the global energy transition. The challenge for this domain becomes to provide high-efficiency power conversion (i. ex. in [22] the 52% improvement of energy efficiency for vehicle by 2050 (in relative to 2015) is assumed), active control of the instantaneous power flow, further reduction of the functional volume and weight of devices, to ensure highly compact design (high energy density of devices), with increased reliability and self-diagnostic systems, to ensure correct operation and cooperation of systems composed of dozens of converters.

To face these challenges, several technological developments have been initiated. Among them, the Wide-Bandgap (WBG) (as Silicone Carbide (SiC) and Gallium Nitride (GaN)) are promising in terms of efficiency gain (lower on-state voltage drop at same breakdown voltage), and mass reduction of the converter (due to higher switching frequency). However, the outstanding performances of these devices involve many challenges due to very high commutation speed. This requests a careful investigation in terms of layout optimization to avoid in particular voltage overshoots at turn off, and also a specific attention to the Electromagnetic Emissions (Electromagnetic Interferences (EMI)), which should be mitigated.

1.2 GaN power devices

Traditional silicon-based semiconductor technology dominates the market for low and high power converters, ranging from mobile phone chargers to railroad power stations or high voltage direct current (HVDC) links. The silicon semiconductor manufacturing process is very mature, resulting in products offering proven performance, high reliability and low production costs. However, the needs and requirements for power conversion devices are constantly increasing, especially in high voltage, high efficiency or high power density applications, or a combination of both [19]. Due to the limitations of the silicon material, it is no longer possible to achieve higher performance with semiconductors based on this material. In order to meet the demands of the market, research centers, together with the electronics industry, have conducted a wide range of research and experimentation to develop semiconductor devices based on new materials such as Gallium Arsenide (GaAs), Aluminum Arsenide (AlAs), Silicon Carbide (SiC), Gallium Nitride (GaN) and Aluminum Nitride (AlN) [56, 20]. The possibilities of using semiconductors based on new materials, especially in power electronics, have been presented in many publications [47, 52, 9, 96, 90, 78, 80]. Research has led to the highly advanced development of Wide Bandgap (WBG) semiconductors from materials such as GaN and SiC.

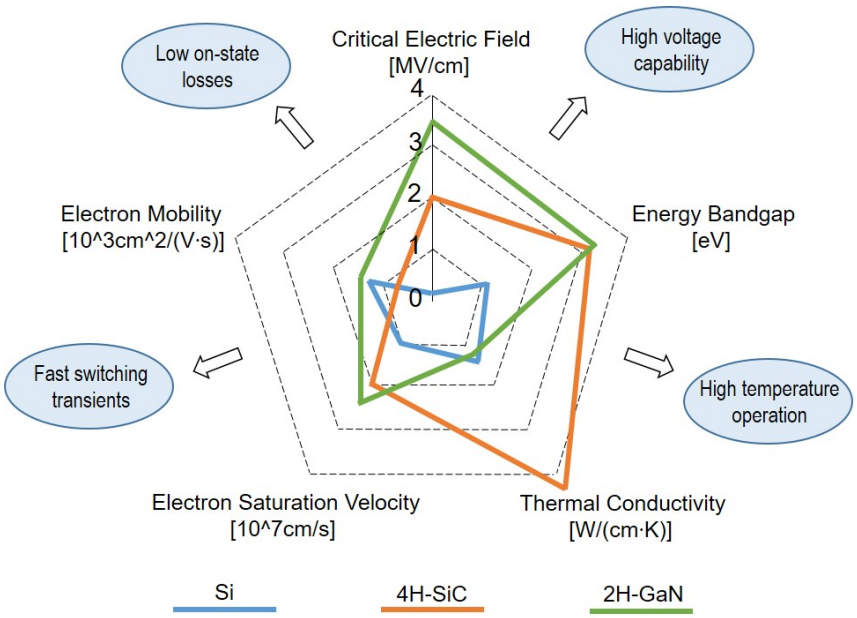


Figure 1.4: The merits of Si, SiC, and GaN materials

Wide Bandgap semiconductors have a much larger energy gap E_g compared to silicon semiconductors. The physical properties of the various materials are summarized in Table 1.1 and shown graphically in Fig. 1.4. The energy gap of a given semiconductor determines the strength of the chemical bonds between the atoms in a molecule. Stronger bonds also mean that it is more difficult for electrons to move. This results in lower leakage current and higher operating temperatures for semiconductors with large energy gaps. Referring to the Table 1.1, GaN and SiC materials have significantly higher E_g than silicon.

Table 1.1: Properties of Silicon, Silicon Carbide, and Gallium Nitride materials[62]

Property	**Unit**	**Silicon (Si)**	**Silicone Carbide (SiC)**	**Gallium Nitride (GaN)**
Band Gap E_g	eV	1.12	3.26	3.39
Critical Field E_{crit}	MV/cm	0.23	2.2	3.3
Electron Mobility μ_n	$cm^2/V \cdot s$	1400	950	1500
Permittivity ϵ_r	-	11.8	9.7	9
Thermal Conductivity λ	$W/cm \cdot K$	1.5	3.8	1.3

Stronger chemical bonds also result in a higher value of the maximum electric field strength. This means that it takes a high value of electric field strength to initiate impact ionization, resulting in avalanche breakthrough of the junction. The voltage at which avalanche breakdown (device destruction) occurs can be approximated by the formula 1.1. The breakdown voltage is directly proportional to the width of the drift region. This means that for SiC and GaN semiconductors, the drift area can be up to 10 times smaller than for silicon semiconductors for the same breakdown voltage. So the distance between electrodes can be 10 times smaller [62].

$$U_{BR} = \frac{1}{2} \cdot w_{drift} \cdot E_{crit} \tag{1.1}$$

Where:

U_{BR} – breakdown voltage of a device $[V]$

w_{drift} – width of the drift region $[m]$

E_{crit} – critical electrical field $[V/m]$

The significant reduction of the drift area in GaN and SiC affects the conduction on-resistance. The theoretical resistivity can be calculated from the data in the Table 1.1 using the formula 1.2:

$$R_{DS(on)} = \frac{4 \cdot U_{BR}^2}{\varepsilon_0 \cdot \varepsilon_r \cdot E_{crit}^3} \tag{1.2}$$

Where:

$R_{DS(on)}$ – theoretical on-resistance $[\Omega \cdot m^2]$

U_{BR} – breakdown voltage of a device $[V]$

ε_0 – vacuum permittivity $[8.854 \cdot 10^{-12} F/m]$

ε_r – permittivity of the material $[-]$

E_{crit} – critical electrical field $[V/m]$

On the basis of the equation 1.2, the comparison of theoretical relationship between the conduction resistance (dashed lines) together with data of commercially available devices (points) versus breakdown voltage for various materials is presented in Fig. 1.5. It should be noted that real semiconductors are not always characterized by an ideal structure, so reaching the theoretical limits is a challenge that has not yet been achieved for SiC and GaN.

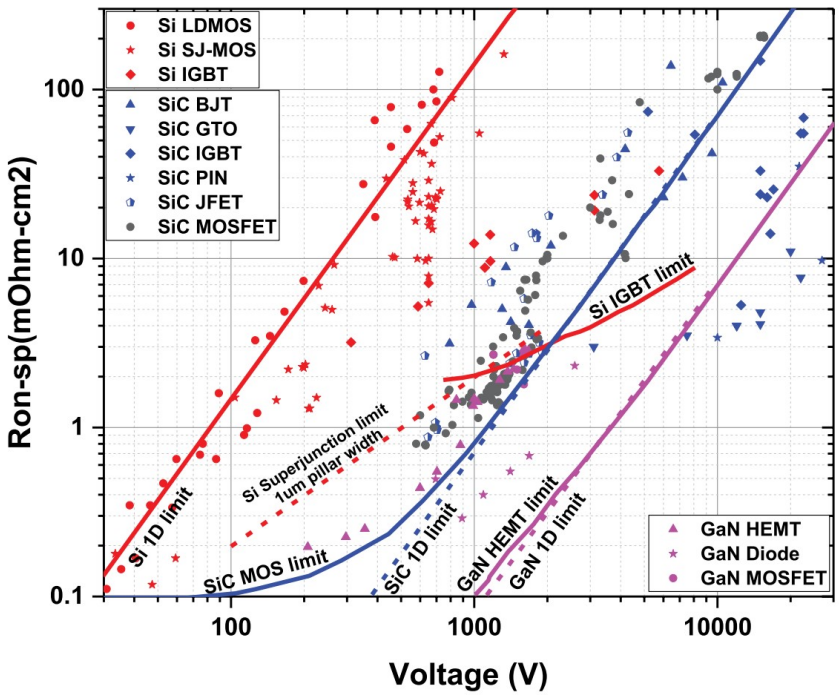


Figure 1.5: Specific on-resistance versus breakdown voltage achieved by modern power devices [41]

In summary, the properties of SiC and GaN materials result in the possibility of producing semiconductors with much better electrical and functional performance compared to silicon technology. SiC and GaN transistors can operate at a higher permissible operating temperature, with a higher switching frequency and higher speed (extremely high voltage and current gradients), while maintaining low conduction resistance and high current density in the semiconductor junction region. The use of such switches in power electronics makes it possible to operate transistors at higher voltages (typically 650V), reducing power dissipation, miniaturizing the device (higher power density) and increasing overall efficiency.

1.2.1 Vertical and lateral GaN devices

Vertical GaN devices have an internal structure similar to their Si and SiC counterparts, while taking advantage of GaN's material superiority. In such a structure, current flow is along the semiconductor channel (Fig. 1.6). The main advantage of such a solution is the ability to adjust the thickness of the semiconductor layer to achieve a higher breakdown voltage. In addition, it is possible to

stack such structures. Unfortunately, this structure is still in the research and development phase and has not yet been commercialized. The reason is mainly due to the difficulty of fabricating such devices (compared to lateral structures) and the lack/limited availability of high quality and cost-effective GaN wafers.

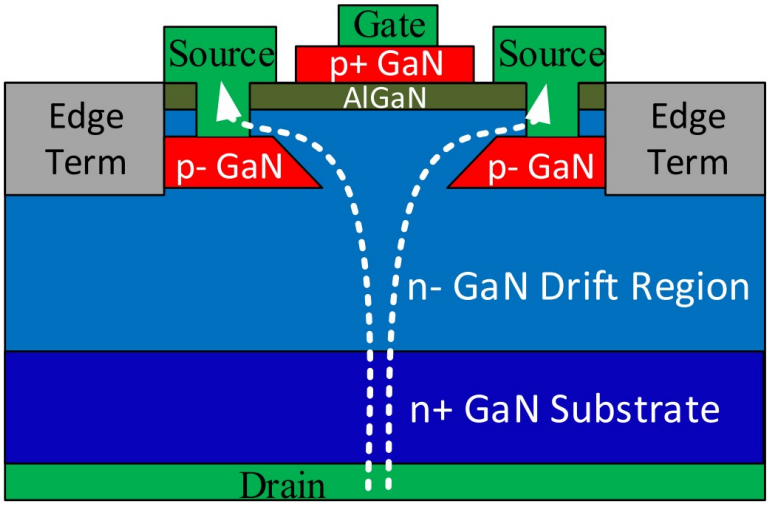


Figure 1.6: Vertical GaN transistor structure [44, 70]

However, it is important to note the research that has been done so far. In [29], the first vertical GaN Schottky and p-n diodes were presented, in which blocking voltages of 600 V (Schottky) and 1700 V (p-n) were achieved. In addition, a p-n diode with a relatively large semiconductor area (16 mm^2) was successfully fabricated, which can withstand a current pulse of 400 A and a blocking voltage of 700 V [54]. First non-commercial samples are available for 600 V, 1200 V and 1700 V diodes with a current rating of 5 A in a TO-220 package [81]. A vertical GaN transistor with a breakdown voltage of 1500 V and a drain current of 2.3 A has also been developed in 2014 (Fig. 1.6). Its structure is a combination of a traditional JFET with an AlGaN/GaN heterojunction structure used in lateral devices [44]. It has a gate threshold voltage of 0.5 V and this device is enhancement-mode (e-mode), so it is a normally-off transistor [70]. Now, the first commercializations of vertical transistors are emerging, and [81] offers as an example 700 V and 1200 V transistors with a maximum drain current of up to 35 A. However, this immature solution is characterized by a high turn-on resistance (from 40 $m\Omega$ to 1000 $m\Omega$).

Due to the technological problems with vertical devices, lateral GaN devices have been developed and implemented more quickly. They are commonly known as lateral Heterojunction Field Effect Transistors (HFETs), also called High Electron Mobility Transistors (HEMTs). Typically, these devices have breakdown voltages of up to 650 V/maximum of 1200 V (the latest on the market). Due to the lateral organization of the semiconductor, these devices are fundamentally different from MOSFETs and have unique characteristics. First of all, this structure is an AlGaN/GaN heterojunction, where highly mobile electrons called "two-dimensional electron gas" (2DEG) are inserted between these two material layers. The 2DEG forms a native channel between the source and drain of the device. The substrate is most commonly Si, but other materials such as SiC or diamond can also be used.

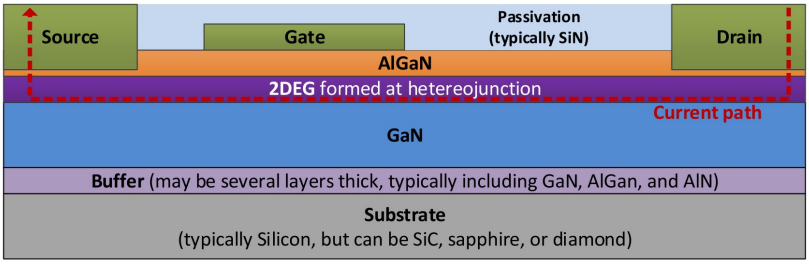


Figure 1.7: Vertical GaN transistor structure [44, 45]

As shown in Fig. 1.7, the current path is quite different from vertical and in this case current flows laterally across the semiconductor channel. At the same time, this means that achieving higher breakdown voltage or drain current requires an increase in lateral dimension, which, due to increased size and cost, limits manufacturers to circuits with maximum parameters of 1200 V and about 100-150 A. Because of the native 2DEG channel, the HFET is inherently a depletion mode (normally-on, d-mode) device [44], which is an unfavorable feature in power electronics terms, so further work has moved toward the development of a normally-off device.

1.2.2 Lateral GaN transistor types

GaN transistors are produced in different varieties depending on the technology used by the manufacturer. There are four main types of GaN transistors:

- Depletion-Mode GaN Transistor (d-mode),
- Enhancement-Mode GaN Transistor (e-mode),
- Gate Injection Transistor (GIT),
- Cascode GaN Transistor.

The first GaN HEMT transistors developed were in the low-voltage class - depletion mode. Their main features are low conduction resistance, small semiconductor dimensions and very low parasitic capacitance values. However, the main disadvantage is the normally-on channel of the transistor. In power electronics applications, the use of normally-off transistors is preferred for safety reasons. When normally-on transistors are used, it is necessary to use additional protection circuitry to provide constant power to gate drivers or similar devices. An enhancement-mode (e-mode), cascode and GIT structure has been developed to achieve normally-off devices.

E-mode transistors have been developed by modifying the gate region to shift the threshold voltage to a positive value. To accomplish this, a p-doped layer of GaN is deposited under the gate, creating a diode-like characteristic on the gate that shifts the threshold up by the magnitude of the diode voltage drop [9]. Thus, the 2DEG carriers under the gate are depleted when no voltage is applied to the gate. However, when the threshold voltage is exceeded, the depleted 2DEGs under the gate are enhanced and the transistor is turned on (conduction of the semiconductor channel occurs) [44].

GIT transistors also use a p-type gate layer that depletes 2DEG carriers in the region below the gate at zero gate bias. However, in this case, the required voltage drop across the gate causes a constant current (several milliamps) to flow into the gate at steady state. This internal structure allows the injection

of minority carriers, which further enhance the 2DEG and consequently reduce the on-resistance. However, such a solution greatly complicates the design of the gate circuit [63, 32, 44]. Table 1.2 shows the main characteristics of each GaN transistor type.

A normally-off GaN device can also be achieved with a Depletion-Mode HFET using a cascode structure. The approach involves packaging a d-mode GaN together with a low-voltage MOSFET (usually Silicon) in a single package (Fir. 1.8. The two dies are connected in series so that the drain of the MOSFET is wired to the source of the GaN. The V_{DS} voltage of the MOSFET then controls the input (gate-source) voltage of the HFET. As a result of the series connection, both dies conduct the same channel current in the on-state, and the blocking voltage is shared between them in the off-state. Internally, the two dies are typically connected by wire bonding or planar structure (PCB based). The switching quality of the cascode device depends mainly on the parasitic inductances inside the package (especially at the interconnection tracks of the two dies) and on the matching of the junction capacitances of the dies used. If the inductances are too large or the capacitances are not well matched, the switching losses of such a device increase significantly.

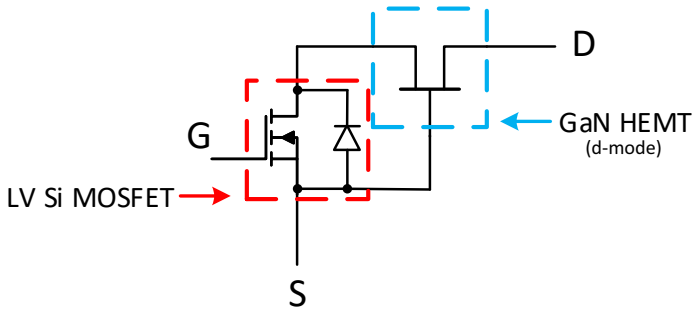


Figure 1.8: Cascode GaN transistor structure

Table 1.2: Features of different lateral GaN structures

Transistor type	**Features**
Depletion-Mode (d-mode)	• Normally-on • No body diode • Capability of conducting current in both directions • Zero recovery charge Q_{rr} • Low gate charge Q_G
Enhancement -Mode (e-mode)	• Normally-off • No body diode • Capability of conducting current in both directions • Zero recovery charge Q_{rr} • Low gate charge Q_G • Low threshold of Voltage V_{GS} • Narrow range of Gate-Source Voltage V_{GS} (recommended maximum 6 V) • Recommended connection (or creation) of Kelvin source • Possible problems with Miller effect
Gate Injection Transistor (GIT)	• Normally-off • No body diode • Capability of conducting current in both directions • Zero recovery charge Q_{rr} • Required flow of constant current (0.5-1.0 A) into the gate to keep the device turned on (steady state) • Lower on-resistance
Cascode	• Normally-off • Series connection of Depletion-Mode GaN and low voltage Si MOSFET • Fast parallel built-in body diode with low recovery charge Q_{rr} • Capability of conducting current in both directions (however in one direction higher losses may appear due to body diode) • Practically no Miller effect • Higher immunity to voltage spikes ($C \cdot du/dt$) • Low gate charge Q_G

1.2.3 Gan devices: applications and problems

The development of power electronics has been slowed mainly by the limitations of silicon switches. Their production has become so mature that the material properties themselves are now the limiting factor. The emergence of new semiconductors has opened up a sea of possibilities. GaN transistors (along with SiC) break through the limitations of Si due to their physical properties. The key factors are [36, 82, 60]:

- Significantly lower conduction resistance, which allows for reduced losses in the device and improved converter efficiency;
- Low junction capacitance - enabling switching at unprecedented rates (dv/dt on the order of tens or even hundreds of V per ns, di/dt on the order of tens of A per ns);
- Ability to operate at higher temperatures - allowing the design of high power density power electronic converters;
- Increased steepness of voltages and currents allows a significant increase in the switching frequency of converters - this has a significant impact on the value and volume of passive components (inductors, transformers, capacitors) and an overall increase in power density.

However, the applications for SiC and GaN are not identical. This is at least due to technological limitations. At present, SiC production technology is much more mature and high-voltage switches are being produced based on this technology (although GaN has a better predisposition for high-voltage operation (Fig. 1.4), such switches have not yet been developed). Thus, according to the current state of development of WBG devices, Fig.1.9 shows their current and possible applications. Note that the application area for GaN includes power electronic converters switched by hundreds of kHz (sub MHz range) with a power of a few to several kW (max 20 kW). The main applications are consumer power supplies, UPS, PV inverters and on-board and off-board EV chargers. Thus, GaNs are a key part of the energy transformation that will take place in the coming years (as mentioned above in Chapter 1.1).

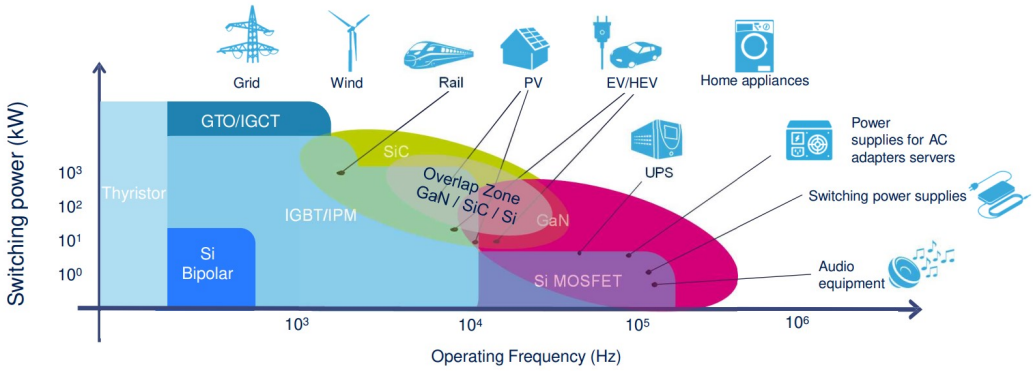


Figure 1.9: Power Device Technology Positioning (2018) [37]

However, applying and taking full advantage of the new devices' capabilities is not straightforward. There are still several challenges in the application of WBG [84, 60, 36]:

- Increased generation of electromagnetic interference (EMI) due to the large steepness of voltages and currents, and the increased importance of the existence of parasitic elements for such high frequencies corresponding to these slopes (and such high switching frequency),
- Overvoltages and oscillations associated with the parasitic inductance of the power circuit,
- High demands on the package design and circuit layout of the power converter,
- Management of stray capacitance currents (common mode paths),
- Need for faster protection circuits,
- Need for high performance controllers (e.g. to ensure high frequency switching),
- Need to select power converter components (inductors, capacitors, sensors, etc.) that are compatible with GaN and SiC,
- High thermal fatigue,
- Temperature compatibility with other components,
- Need for better EMI filters,
- False turn-on protection (Miller effect mitigation).

In this thesis, some of the above challenges are taken into account and will be discussed in detail in later chapters.

1.3 Electromagnetic Compatibility (EMC) in Power Electronics

In power electronics, semiconductor power devices (transistors, diodes, thyristors, etc.) are the main source of EMI. Their operation at very high switching frequencies, huge dv/dt and di/dt generated in different floating point of the system produce disturbances that propagate to other circuits and devices. Then, the EMI aspect that cannot be overlooked. Nowadays, with WBG, where the steepness has increased many times over silicon devices, the impact and nature of these phenomena have become critical in the design of power electronic converters.

According to the International Electrotechnical Commission (IEC), EMC is described as "the ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment", while EMI (disturbances) is "any electromagnetic phenomenon which, by being present in the electromagnetic environment, can cause electrical equipment to depart from its intended performance" [2]. Thus, any EMI disturbance leads to an overall EMC degradation. The level of EMI is regulated by a number of standards developed by organizations such as the IEC, the Federal Communications Commission (FCC), and the Comité International Spécifique pour les Radiofréquences (CISPR). Depending on the application of a specific device, it must comply with different standards. Therefore, a better understanding of this phenomenon is necessary to predict, minimize and reduce EMI generation. In addition, it is very important to focus on EMI performance prior to the final manufacture of the converter, as some of the considerations for predicting or estimating EMI can be made during the design phase and some optimization can be implemented immediately.

Design of Power Electronics Converter must therefore account for the very essential characteristics of EMC. For this purpose, new approaches and tools are needed to understand the laws and phenomena in this challenging area. Three components of EMI disturbances should be understood and described:

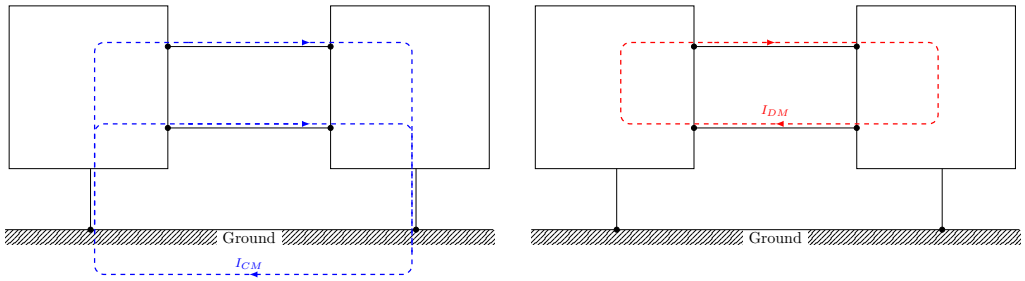
- The source: This is the device or equipment where the noise or disturbance is generated. The source of this interference can be, for example, fast signals, reduced rise and fall times, resonance, oscillations and surges, reflections, improper termination, antenna structures, and differences in electrical potentials,
- The victim: is an electrical circuit that is affected by disturbances from the source and suffers a significant impact on the functioning of the internal signals and the operation of the entire device (application),
- The coupling path: is the path or medium whereby the disturbance is propagated from the source to the victim.

In the context of EMC, the management of two key aspects is carried out. The first is emission: it represents the noise generated by a component, equipment or electronic/electrical system. The second is susceptibility: it defines the ability of electronic equipment to withstand a certain level of noise that does not cause the electronic/electrical equipment to malfunction. Based on the type of integration and the type of medium in which EMI noise propagates, 4 groups can be categorized:

- Conducted emission (CE), which means that the noise generated by the device or equipment is transmitted to the victim via wires,
- Radiated emission (RE), which indicates that the noise generated by the device or equipment is transmitted to the victim through the air,
- Conducted susceptibility (CS), which determines the ability to reject noise transmitted through wires,
- Radiated susceptibility (RS), which determines the ability to reject noise transmitted through air.

In addition, according to generally accepted standards, the frequency range of measured noise from 150 kHz to 30 MHz is referred as conducted emissions, and the range from 30 MHz to 1 GHz is referred as radiated emissions. In this thesis, all considerations of EMI are based on conducted emissions.

Based on generation mechanism, total conducted EMI can be divided into two basic types: Differential-Mode (DM) and Common-Mode (CM). In general, DM noise (also known as symmetrical noise) is associated with switching current flowing along the supply wire (plus or minus wire) and back through the other supply wire (Fig. 1.10b) - the current flows in a closed loop and in different directions in both wires. In contrast, CM noise (asymmetrical noise) is mainly associated with parasitic capacitances of self and ground components of a given electrical circuit and causes the flow of noise current in the same direction through both supply wires and back with the reference ground - noise is conducted on all wires simultaneously in the same direction and phase (Fig. 1.10a).



(a) (b)

Figure 1.10: (a) Common-Mode noise path, (b) Differential-Mode noise path

According to all EMC standards defining individual device testing, conducted EMI measurements, both in the time and frequency domains, should be carried out by using a standardized Line Impedance Stabilizing Network (LISN). The LISN is used to block all noise from the power supply network side and provides a balanced, known and constant impedance over a wide frequency range that reflects the "real" grid. There are several variations of the LISN in the literature, but the network shown in Fig. 1.11 is used in the thesis. Measurement results can be obtained in two ways: either by measuring the LISN voltages V_{L1} and V_{L2} and then performing calculations (Eq. 1.3 and 1.4), or by using a current probe placed on both wires in the appropriate configuration (as in Fig. 1.11).

$$V_{CM} = \frac{V_{L1} + V_{L2}}{2} \tag{1.3}$$

$$V_{DM} = V_{L1} - V_{L2} \tag{1.4}$$

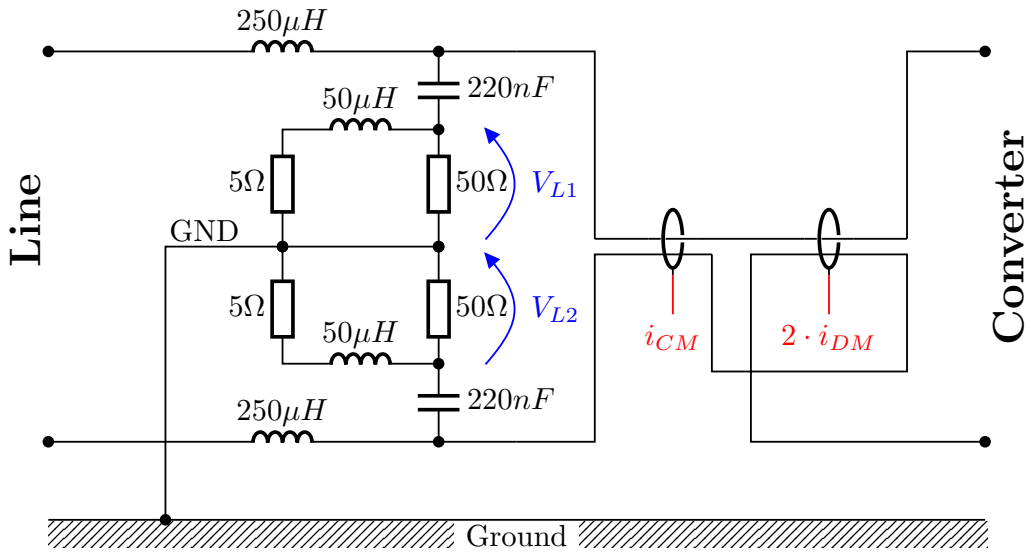


Figure 1.11: Schematic of Line Impedance Stabilization Network

The level of disturbance, its distribution between CM and DM, and the likely propagation paths can be studied using several different approaches:

- Expert knowledge and experimental studies
- Simplified calculations in the time or frequency domain
- Computer simulations incorporating reasonably accurate models of the converter components.

The thesis presents two approaches to EMI research. The proposed concepts were first simulated and validated using ANSYS and Saber software. Then, extensive experimental testing was performed in an EMC laboratory to confirm the results and acquire final confirmation in real-life conditions.

1.4 EMI issues and challenges in GaN-based Power Electronics

High switching speed and the ability to operate at high switching frequencies bring new challenges, one of those being electromagnetic interference (EMI). Issues related to impact on noise source, noise propagation paths, EMI reduction techniques or reliability issues related to EMC are becoming a broad area of interest and development. High dv/dt and di/dt during switching, together with the existence of parasitic inductances in the circuit, cause ringing (the frequency of which can reach up to 100 MHz) and, combined with high switching frequency, increase EMI concerns. In addition, HF switching along with EMI problems and the sensitive structure of WBG semiconductors leads to converter reliability problems. Therefore, it is inevitable to consider a special design approach in which the EMI issues must be addressed accordingly. Otherwise, the advantages of WGB will be compromised [92].

From an EMI perspective, all the merits of WBG have a negative impact on conducted and radiated interference. The aforementioned ringing of several MHz during switching leads to an increase in conducted interference in the high-frequency range [94]. In addition, such noise may not be easily reduced by EMI filters because the HF performance of magnetic materials is limited and the impedance characteristics of the filter are reduced by the effect of parasitic elements [88, 87]. The switching frequency and amplitude of the switched signals determine EMI in the low-frequency range, and the switching speed (rise and fall times) and ringing determine EMI in the high-frequency range. Another factor that determines conducted noise is the impedance of the propagation path. This impedance depends on the circuit topology, ground connections, and component characteristics.

Radiated noise is part of the EMI concerns. In WBG devices, near-field radiated EMI increases significantly compared to Si due to the high power density and tight packing of components very close together. Then the influence of near-field coupling increases. Electrical near-field coupling can be represented as capacitive coupling, where the value of the capacitance is determined by the geometry of

the physical layout (tracks layout, etc.). The sources of this emission are usually nodes with pulsed voltage. The second is magnetic near-field coupling, where the noise sources are current loops and can be represented as a mutual inductance model. Of course, the influence of WBG is also evident in far-field EMI mainly because of the higher frequencies involved: higher switching frequency, and shorter transition times, which increase the high frequency part of the spectrum. Here, the source of radiation is usually capacitive coupling between cables and the printed circuit board (PCB) [93]. In addition, any non-intentional antennas that exist in the design lead to an increase in radiated EMI. As evidenced by [11, 12], ringing during switching also increases the level of radiated EMI at these frequencies.

Therefore, interference reduction approaches are needed, and can be divided into two groups: 1) EMI reduction at the level of the noise sources; 2) EMI reduction by modification and control of the propagation paths; 3) filtering. A summary of the problems and challenges of EMI in power electronics with GaN devices is shown in Table 1.3 [92].

Table 1.3: EMI issues and possible future research fields [92]

EMI issues	**Future research fields**
Conducted EMI (150 kHz - 30 MHz)	Aim: To reduce EMI noise source without sacrificing efficiency Research: Advanced circuit topology and switching control
	Aim: To reduce ringing oscillations Research: Package and PCB layout optimization, damping scheme
Radiated EMI (far-field) (>30 MHz)	Aim: To understand the generation and propagation of radiated EMI Research: Modeling and measurement of radiated EMI
	Aim: Reduce radiated EMI Research: switching frequency modulation, advanced driving scheme, filter components with large high frequency impedance, shielding techniques, grounding techniques, PCB layout, packaging optimization
Radiated EMI (near-field)	Aim: Influence of near-field coupling to conductive and radiated EMI Research: Modeling of near-field coupling
	Aim: Influence of near-field coupling on the reliability of power converters Research: Identification of near-field coupling between the power loop and the drive loop
	Aim: To reduce the near-field coupling Research: Passive components with low near-field emission and near-field immunity, shielding techniques, cancellation technique

1.5 Contributions and Thesis Outline

Addressing the need for research and technology development on EMI mitigation in power electronic converters with GaN transistors, this thesis presents a number of solutions. Three approaches to identify and optimize conducted disturbances are presented. First, the effect of control mode (hard versus soft switching) is evaluated. Next, general converter layout considerations are presented, along with the idea of shielding and the Power-Chip-on-Chip (PCoC) concept. Finally, a new approach to the design of magnetic elements and their possible integration into a GaN-based converter has been investigated. In each of these activities, the EMI mitigation aspect has been a priority.

The aim of thesis is to prove that EMI mitigation is possible via proper selection of control strategies, layout changes and implementation of a new approach to magnetic elements.

The core of the work consists of three chapters, the contents of which are summarized below. The chapters are designed to have minimal interdependence, therefore each chapter can be read independently:

- Chapter 2 focuses on the effect of the control strategy on the generated EMI. The analysis is based on a buck converter realized on a prototype of single inverter leg with GaN transistors. An exhaustive characterization of the sub-periods of the converter operating in Discontinuous Current Mode (DCM) (with one switching transistor and one diode) and in Triangular Current Mode (TCM) (synchronous operation of two transistors) is presented. The results of the electrical performance of the waveforms for both modes of operation are presented. An application and procedure for the sizing of a capacitive snubber circuit is proposed in regard to the large overvoltages experienced. Finally, for the 3 cases considered (DCM, TCM, TCM with snubber), a comparison of the experimental results in terms of conducted disturbances, electrical performance quality and converter efficiency is presented.

- Chapter 3 presents considerations for reducing EMI by redesigning the converter layout. An extensively described identification of parasitic elements in a single inverter leg is presented. A simulation workflow for the Digital Twin has been developed and applied to study in detail the effects of individual layout elements on EMC. Then, the EMC environment and the precautions required for laboratory measurements of conducted emissions are described. The shielding concept is presented and the experimental validation is presented. Finally, the idea of adapting the Power-Chip-on-Chip (PCoC) concept to GaN transistors is presented and experimentally validated.

- Chapter 4 presents a new approach to the design and use of magnetic elements. The Integrated Inductor is introduced along with its manufacturing process. The methodology for characterizing the impedance of the Integrated Inductor is then presented, with special attention given to the extraction of key parasitic elements that affect the EMC behavior. Finally, the advantage of using the new solution compared to the classical inductor was presented based on simulation studies.

- Chapter 5 summarizes the doctoral thesis and presents the main contributions and key studies. In addition, a brief description of possible future work is outlined.

Chapter 2

Control strategy impact on EMI generation

The results presented in the following chapter have already been the subject of a number of published papers:

- Derkacz, P. B., Musznicki, P., & Chrzan, P. J. (2020). EMI attenuation in a DC–DC buck converter using GaN HEMT. IEEE Journal of Emerging and Selected Topics in Power Electronics, 9(4), 4146-4152.
- Derkacz, P., & Musznicki, P. (2019). Gate driver with overcurrent protection circuit for GaN transistors. Przegląd Elektrotechniczny, (2), 125-128.

"The greatest enemy of knowledge is not ignorance,
it is the illusion of knowledge."
Stephen Hawking

2.1 Introduction

As is was previously referred in the section 1, Electromagnetic Interferences (EMI) in power electronics are related with the switching events. At these instants the high $\frac{dv}{dt}$ and $\frac{di}{dt}$ occur and together with existence of stray elements provoke the conducted noise currents.

In the converters with Wide-Bandgap (WBG) semiconductors, the switching conditions are rised up to tens time faster than for silicon devices. It causes much bigger value of the voltage and current transients and further extremely greater noise generation. Mitigation of the EMI noise can be achieved by improvement of the PCB layout and overall construction of converter - what is presented in details in the Chapter 3. However, considering only control algorithm of converter (without any change of layout), the following question can be pose: is it possible to limit the EMI generation by adapting the control strategy? The answer is YES, as it will be shown hereafter.

The control strategies are varying widely on converter type, topology, voltage/current level, type of used semiconductor switches. However, two main types of control are distinguished (based on the semiconductor switching conditions): hard-switching and soft-switching. In the hard-switching, the current and/or voltage of semiconductor is interrupted/turned-on rapidly. It imposes creation of high $\frac{dv}{dt}$ and/or $\frac{di}{dt}$ at the switch location. In the soft-switching, the change of the semiconductor state occurs in Zero-Voltage or Zero-Current conditions, then the $\frac{dv}{dt}$ and/or $\frac{di}{dt}$ creation and switching loss are reduced. Thus, generation of EMI noise is also mitigated.

In the following chapter, the Half-Bridge prototype is used in the Buck application. The case of Buck is utilized to identify the impact of control strategy on EMI generation. EMI conducted emission of a DC-DC Buck converter operation in the soft-switching triangular current mode (TCM) was investigated and compared with the conventional hard switching discontinuous current mode (DCM) control technique. The chapter objective is to specify the power conversion efficiency as well as attenuation of common mode (CM) and differential mode (DM) noise voltage of the compared switching control strategies.

In high frequency DC-DC Buck converters, the zero voltage switching (ZVS) conditions are strongly recommended for limitation of turn on switching losses. The

ZVS operation may be directly achieved in a resonant circuit consisting of the filter inductor (output inductor of Buck converter - L in Fig. 2.1) and the switches capacitance. By applying control of the TCM [14] (defined also, as critical current mode [42]), resonant transitions are evoked at successive converter state commutations. Relatively large triangular current waveform ripples characterizing TCM operation can be attenuated by introducing interleaved multi-phase topology [75], in a form of coupled inductors [42] or using circuit extension with additional clamp switch [55].
In section 2.2 the overview and description of converter prototype used in this research togehter with experimental setup are presented. In sections 2.3 and 2.4, the switching strategies are briefly introduced. In section 2.5, implemented control strategies with energy based analysis of snubber capacitor is presented. Next, experimental results of EMI and converter efficiency measurements are compared in section 2.6. Finally, all the key observations of the research described in this chapter are resumed in conclusions 2.7.

2.2 Demonstator of Buck converter with cascode GaN transistors

2.2.1 Test setup

The DC-DC Buck converter shown in Fig. 2.1 was built using half-bridge connected two GaN HEMT in cascode structure of Transphorm ($TPH3207WS$: $650\,V/50\,A$) with a low pass LC filter on output side (Fig. 2.1), sized to the cut-off frequency $f_c = 1630\,Hz$. The converter was supplied from dc input voltage source V_i by the LISN Schaffner NNB 41. The resistive load R_l was set to dissipate $350\,W$ at the output voltage $V_o = 55\,V$. The L_s in Fig. 2.1 illustrates the stray power loop inductance of the layout, and C_{T1} and C_{T2} illustrate the nonlinear output capacitance of transistors.

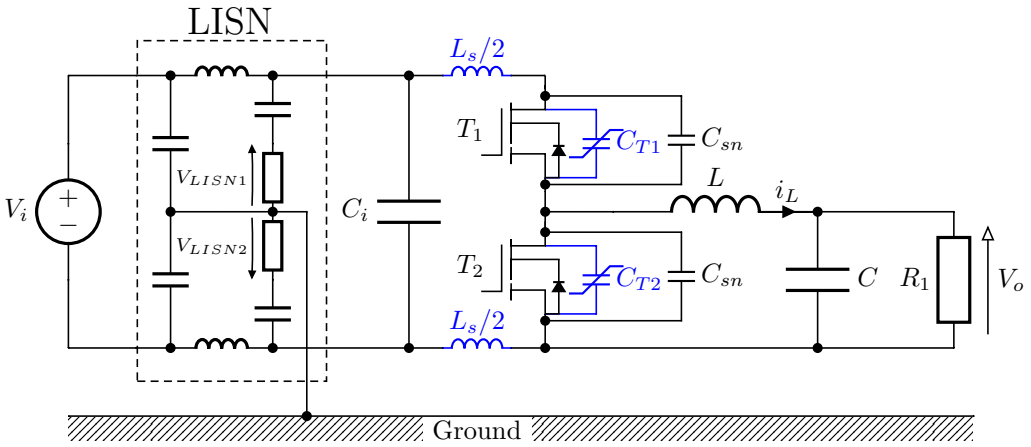


Figure 2.1: Test circuit of GaN HEMT Buck converter

Switching of GaN transistors was accomplished by the gate driver with two gate circuit branches as presented in Fig. 2.2. In this configuration, turn on and off time can be set individually using various values of R_1 and R_2 resistors respectively. Thus, switching performance is limited by resistor values, which determines the value of dv/dt existing in the converter.

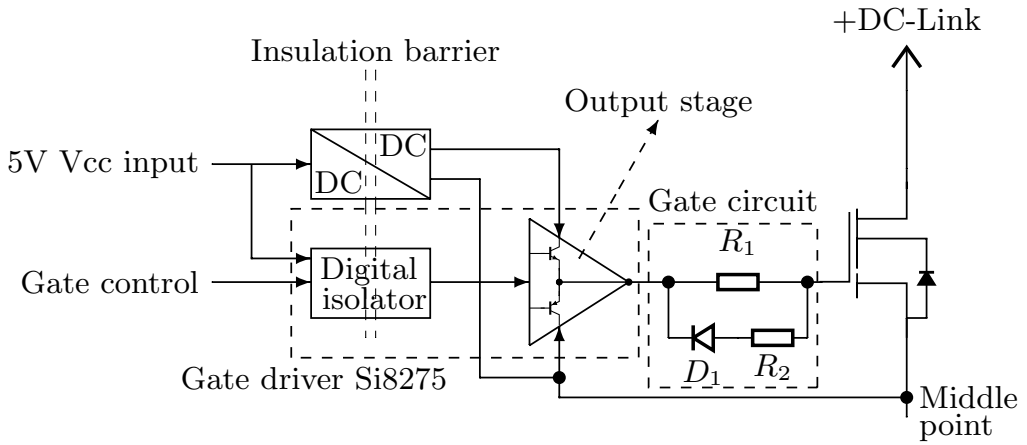


Figure 2.2: Schematic of the gate driver

In the considered setup, a gate driver based on Si8275 IC was used to accomplish a signal insulation and the output stage of the driver. Moreover, two commercial DC-DC power supplies were used to provide independent powering of upper and lower switch. They create positive and negative voltages for driving each GaN device. Gate circuit DC-DC power supply's and digital isolator's stray capacitances are in the range of tens pF to minimize circulation of CM currents in the

gate part (see Fig.2.2). Gate circuits contained $R_{on} = 36\,\Omega$, $R_{off} = 10\,\Omega$ and provided voltages $V_{GS} = +8\,V/-2\,V$ for turn on and turn off switching [25].

The gating control pulses were generated using the STM32F407VG microcontroller. To obtain tight timing of gate signals, control program with three master-slave counters was configured to avoid delays from internal interruptions in the microcontroller. In this way, the $40\,ns$ resolution for gate signal and dead times was obtained at the switching frequency $f_s = 80\,kHz$.

2.3 Discontinuous current mode control of Buck converter

The starting point for this comparison is the DCM operation of buck converters. This is a classical approach with only one active switch. The discontinuous conduction mode in the inductor leads to ZCS conditions when the transistor T1 is turned on. However, the diode losses due to Qrr are not neglected. For the purpose of comparative study, the DCM waveforms are recalled in Fig. 2.3. with corresponding operation modes presented in Fig. 2.4. During the interval $[t_0 : t_1]$ when T_1 is on, the inductor current i_L increases linearly. At instant t_1, T_1 turns off. Voltage v_{T1} is rising and capacitance C_{T1} changes from a large to low value according to the nonlinear capacitance characteristic. This involves providing a charge to C_{T1} and discharge of C_{T2}. After T_1 is turned off $[t_2 : t_3]$, the inductor current i_L decreases linearly flowing through the load and the body diode of transistor T_2.

When i_L reaches zero, the reverse recovery charge Q_{rr} has to be provided to turn off the body diode – exciting oscillatory currents from capacitances: C and C_{T1}. In the interval $[t_4 : t_5]$ C_{T1} and C_{T2} are reloading in resonant circuit with the inductor L causing voltage oscillations across transistors until next period begins [86].

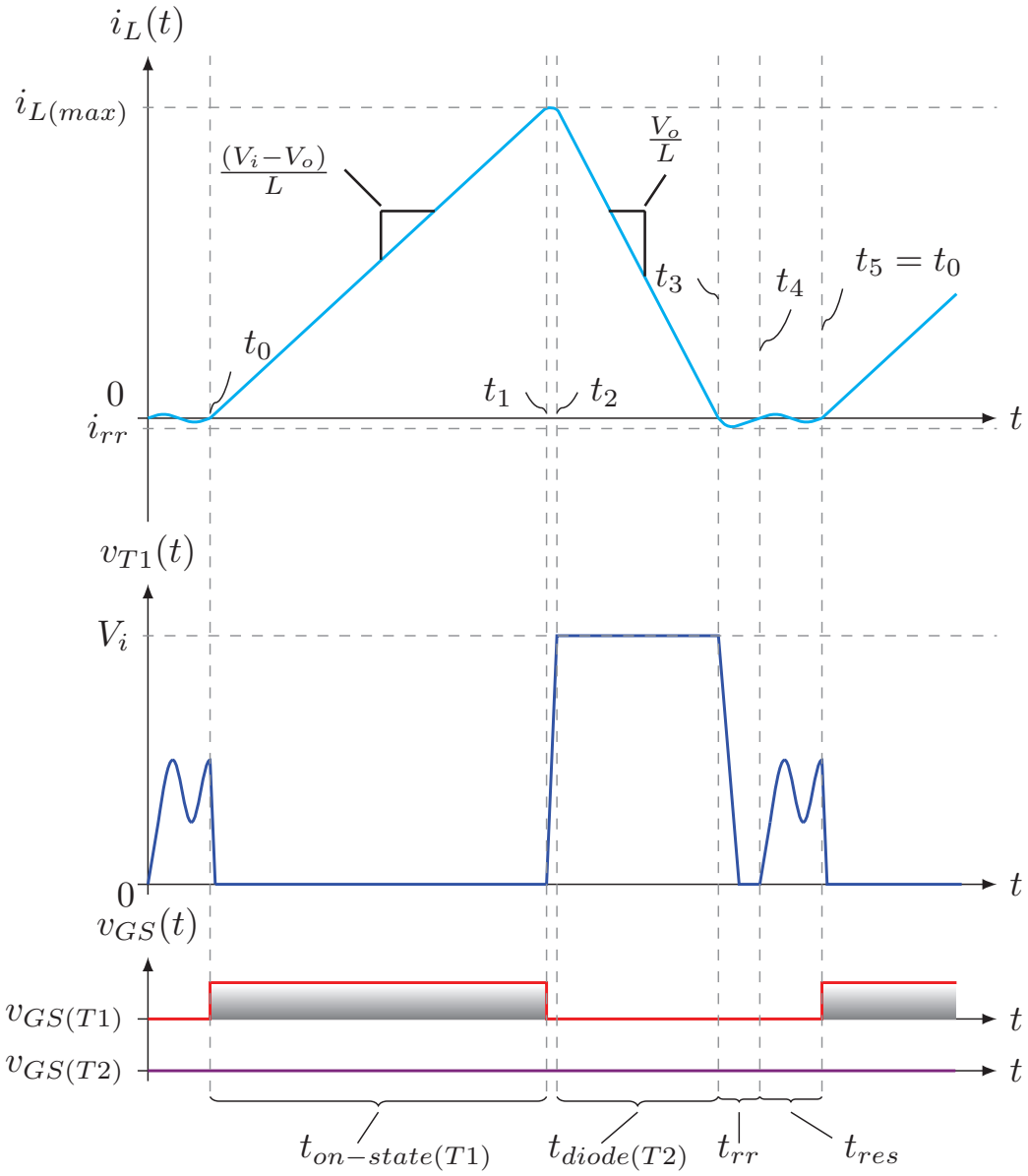


Figure 2.3: DCM waveforms

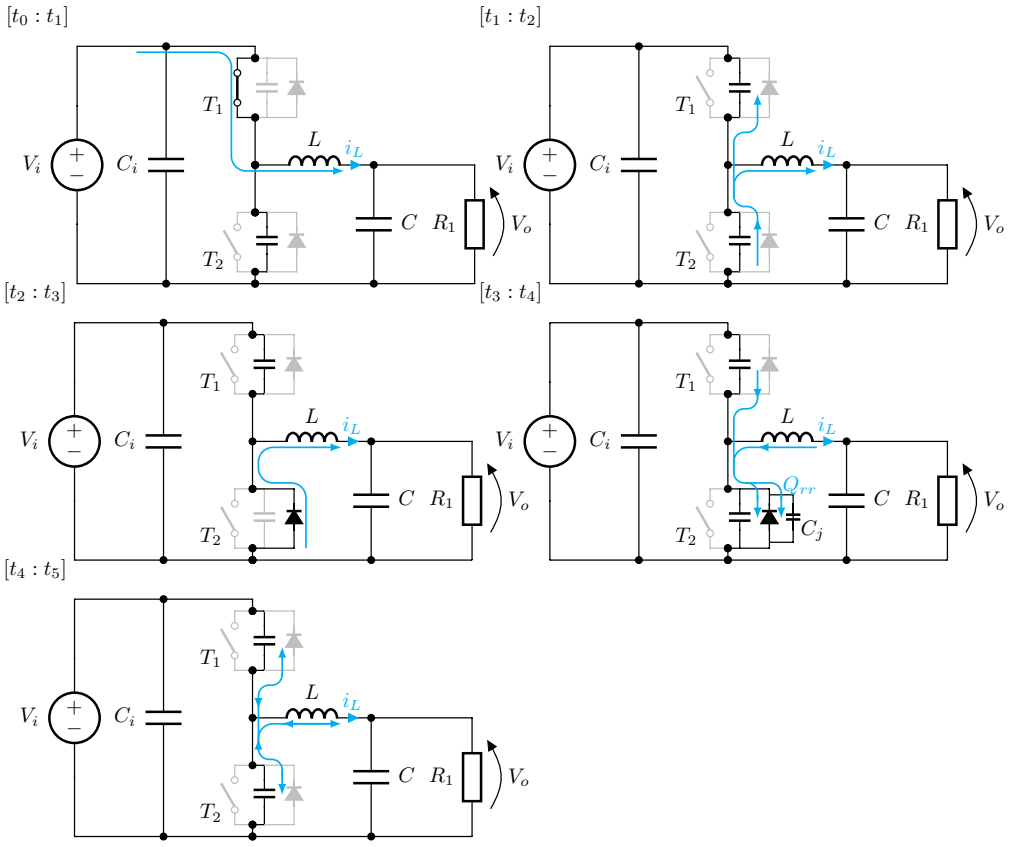


Figure 2.4: DCM operation subcircuits

2.4 Triangular current mode control of Buck converter

Similarly to the preceding case, the TCM waveforms are presented with operation modes respectively in Fig. 2.5. and Fig. 2.6.

In the active subinterval $[t_0 : t_2]$, when T1 is turned on, the inductor current i_L rises linearly in the range from $i_{L(min)}$ to $i_{L(max)}$. At instant t_2 T_1 turns off. Next, the energy exchange proceeds in a resonant circuit consists of L (output inductance), C_{T1} & C_{T2} (nonlinear drain-souce capacitance of each transistor). Accumulated energy of the inductor L is sufficient to discharge the C_{T2} and charge the C_{T1} capacitances in a resonant transition to enable ZVS turn on of T_2. Next, in the passive subinterval $[t_3 : t_5]$ the inductor current i_L decreases linearly flowing through the load and T_2. When i_L reaches predetermined negative threshold $i_{L(th)} > i_{L(min)}$, T_2 turns off reinitiating resonant transition to recharge

C_{T2} and discharge C_{T1} capacitances. After half of the resonant period, the ZVS conditions occur to turn on T_1 and to restart the TCM operation.

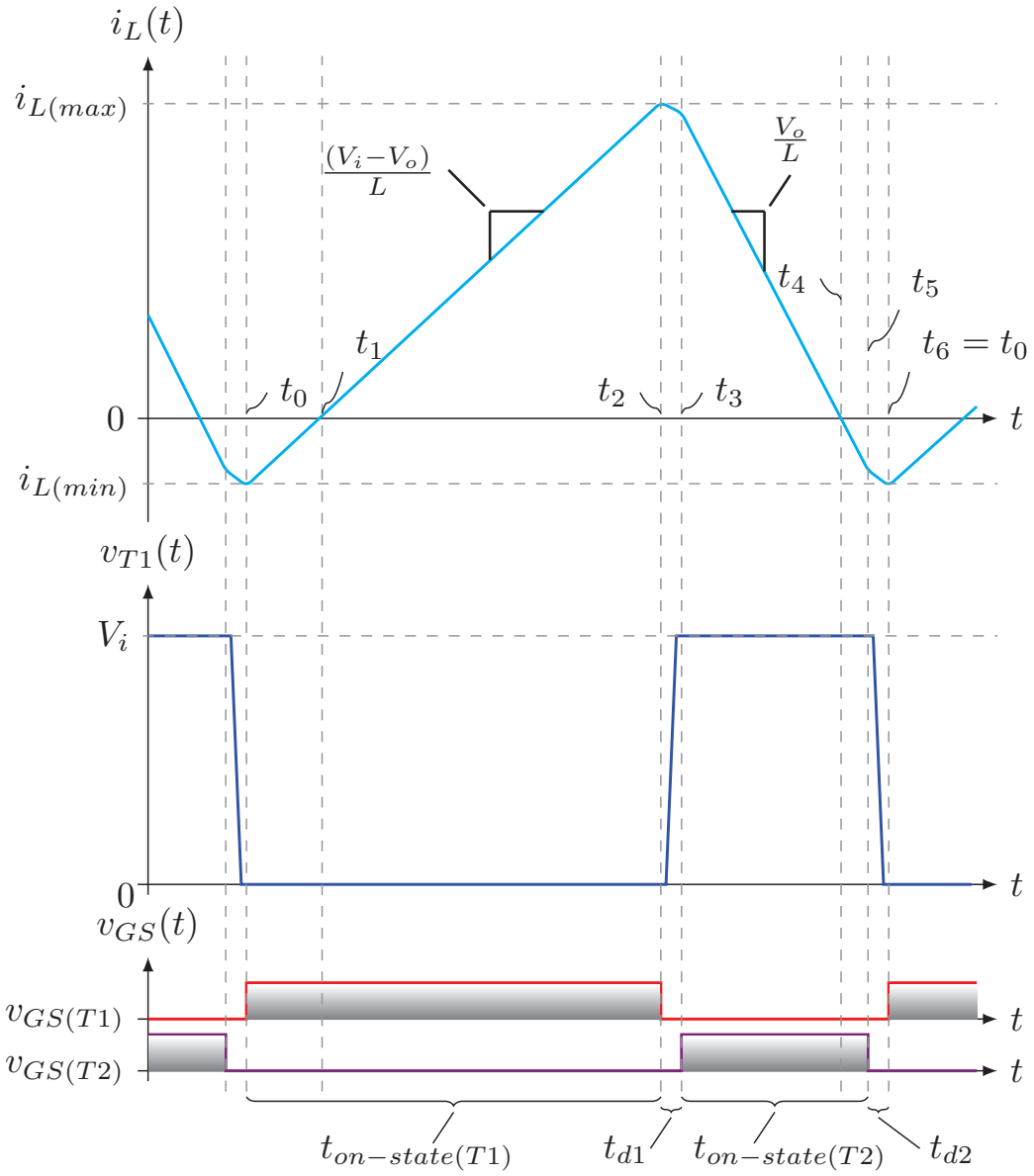


Figure 2.5: TCM waveform

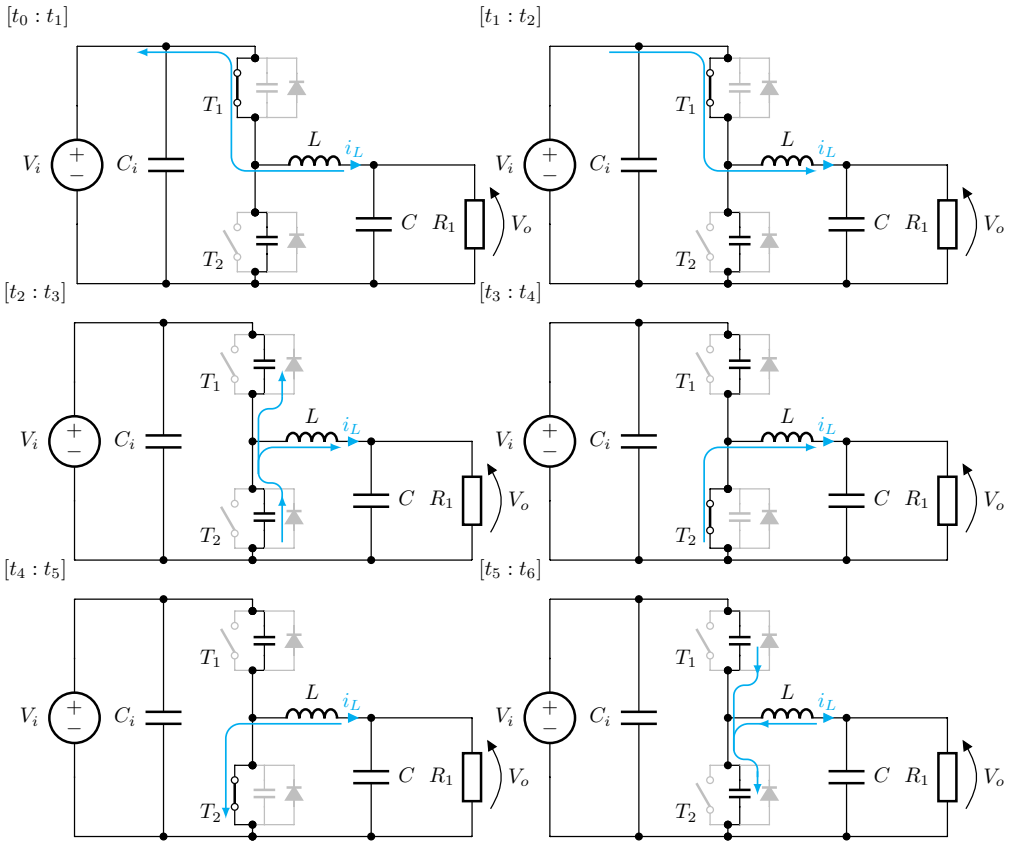


Figure 2.6: TCM operation subcircuits

2.5 Capacitive snubbers

When the circuit layout features too high stray inductance L_s of the power loop, then at transistor T_1 turn off transients (independent of hard-/soft-switching mode), an overvoltage can be induced due to rapidly decreasing current in stray inductances L_s of input power loop (Fig.2.1). In the following part, a snubber capacitor C_{sn} is applied in parallel with each device to attenuate voltage spikes (it is charged to the same voltage as its device). Sizing of the snubber capacitor is based on energy balance equations. The energy E_{bf} before transistor T_1 turn off can be approximated by:

$$E_{bf} \approx E_{inductor} + E_{transistor} + E_{snubber} \tag{2.1}$$

where:

$$E_{inductor} = \frac{I_{T1(max)}^2 L_s}{2} \tag{2.2}$$

$$E_{snubber} = \frac{V_{T2(off)}^2 C_{sn}}{2} \tag{2.3}$$

The electrical charge transferred from DC input to the drain-to-source capacitance of transistor is calculated as [49]:

$$\begin{aligned} Q\left(v_{DS}\right) &= \int_{-v_B}^{v_{DS}} C_{DS}\left(v_{DS}\right) dv_{DS} = C_{J0} \int_{-v_B}^{v_{DS}} \sqrt{\frac{V_B}{v_{DS}+V_B}} dv_{DS} \\ &= 2C_{J0}\sqrt{V_B\left(v_{DS}+V_B\right)} = 2\left(v_{DS}+V_B\right) C_{DS}\left(v_{DS}\right) \approx 2C_{DS}\left(v_{DS}\right) v_{DS}. \end{aligned} \tag{2.4}$$

Hence, the energy stored in the drain-to-source capacitance C_{DS} of transistor at V_{DS} results from the following formula [49]:

$$\begin{aligned} E_{transistor}\left(v_{DS}\right) &= \int_{-V_B}^{v_{DS}} dE_{transistor} = \frac{1}{2}\int_{-V_B}^{v_{DS}} Q dv_{DS} = C_{J0}\sqrt{V_B}\int_{-V_B}^{v_{DS}} \sqrt{v_{DS}+V_B} dv_{DS} \\ &= \frac{2}{3}\left(v_{DS}+V_B\right)^2 C_{DS}\left(v_{DS}\right) \approx \frac{2}{3} C_{DS}\left(v_{DS}\right) v_{DS}^2. \end{aligned} \tag{2.5}$$

Energy stored in drain-to-source capacitance C_{DS} at V_i [49]:

$$E_{transistor} = \frac{2}{3}\left(V_i+V_B\right)^2 C_{DS}\left(V_i\right) \approx \frac{2}{3} C_{DS}\left(V_i\right) V_i^2 \tag{2.6}$$

Finally, the energy E_{bf} before transistor turn off is calculated as follows:

$$E_{bf} \approx \frac{I_{T1(max)}^2 L_s}{2} + \frac{2V_{T2(off)}^2 C_{T2(off)}}{3} + \frac{V_{T2(off)}^2 C_{sn}}{2} \tag{2.7}$$

where:

$C_{T2(off)}$ - the voltage dependent drain-to-source capacitance $C_{DS}(V_{DS})$ of transistor T_2 in off state is obtained from the producer data-sheet capacitance characteristics $C_{DS} = C_{OSS} - C_{RSS}$ for $V_{DS} = V_i$.

C_{sn} - snubber capacitors in parallel with T_1 and with T_2, voltage across T_2 in off state $V_{T2(off)} = V_i$.

and:

$$I_{T1(max)} = \frac{V_i - V_o}{L}(t_2 - t_1) \tag{2.8}$$

The energy E_{af} after transistor T_1 turn off is calculated as follows:

$$E_{af} \approx \frac{2V_{T1(max)}^2 C_{T1(max)}}{3} + \frac{V_{T1(max)}^2 C_{sn}}{2} \tag{2.9}$$

where:
$V_{T1(max)}$ - the maximal value of overvoltage on T_1 and $C_{T1(max)}$ - the T_1 drain-to-source capacitance for $V_{T1(max)}$.

Assuming the energy before transistor turn off equals to the energy after turned off:

$$E_{bf} = E_{af} \tag{2.10}$$

the capacitance of snubber capacitor C_{sn} is derived for acceptable $V_{T1(max)}$:

$$C_{sn} = \frac{3I_{T1(max)}^2 L_s + 4(C_{T2(off)} V_i^2 - C_{T1(max)} V_{T1(max)}^2)}{3(V_{T1(max)}^2 - V_i^2)} \tag{2.11}$$

where:
V_i is the input dc voltage,
$V_{T1(max)}$ is maximal voltage at the T1 turn-off instant,
initial T_1 voltage is assumed zero,
respectively initial T_2 voltage $V_{T2(off)} = V_i$ and the final T_2 voltage is zero.

On the basis of expression (2.11), a graphical representation has been made of the magnitude of the overvoltage with respect to the supply voltage as a function of two parameters: the parasitic inductance of the power loop (L_s) and the value of the snubber used (C_{sn}). As can be seen from the Fig. 2.7, only within a narrow range of L_s (up to a maximum of $20\,nH$) it is possible to operate without an external snubber with acceptable overvoltages. Based on the above results, it can be concluded that one of the most important aspects when designing converters with GaN transistors is to pay attention to the layout of the power loop and to keep the parasitic inductance in this circuit as low as possible.

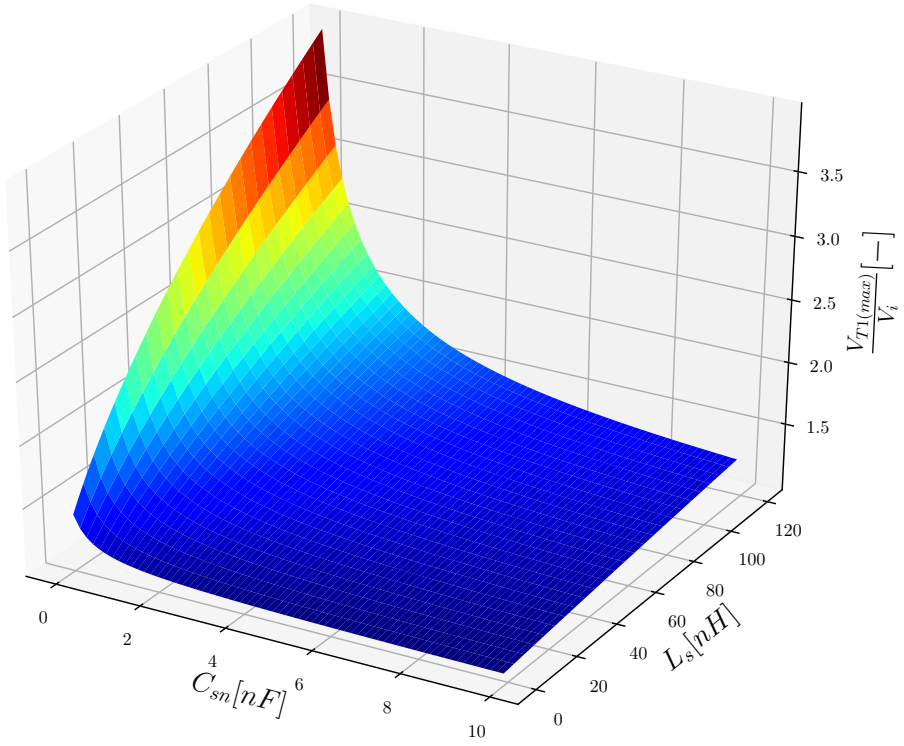


Figure 2.7: Impact of snubber capacitor C_{sn} and input stray inductance L_s on voltage overshoot at the T1 turn off

2.6 Experimental results of electrical performance and EMI attenuation as a function of control strategy type

Using Buck converter parameters from Table 2.1 in equation (2.11), an impact of snubber capacitor C_{sn} and input stray inductance L_s on $V_{T1(max)}/V_i$ voltage overshoot is calculated as in Fig. 2.7. This case study revealed increasing sensitivity of commutation transients for the input stray inductance L_s above 40 nH. Minimization of L_s by careful circuit layout design is of primary importance. Otherwise, to attenuate turn off voltage overshoot, a snubber capacitor has to be applied. In the tested buck converter to limit turn off voltage overshoot to approximately 40% $C_{sn} = 3.2\,nF$ was applied.

Table 2.1: Buck Converter Parameters in TCM

Parameter	**Value**
Output power (P_o)	350 W
Input voltage (V_i)	70 V
Output voltage (V_o)	55 V
Output current (I_o)	6.35 A
Min. value of inductor current ($I_{L(min)}$)	–1.3 A
Max. value of inductor current ($I_{L(max)}$)	15.2 A
Input capacitor (C_i)	5.11 μF
Input stray inductance (L_s)	114 nH
Input stray resistance (R_s)	90 $m\Omega$
Output capacitor (C)	1.1 mF
Inductor (L)	8.7 μH
Parasitic capacitance of T_2 in off state $C_{T2(off)}$	600 pF

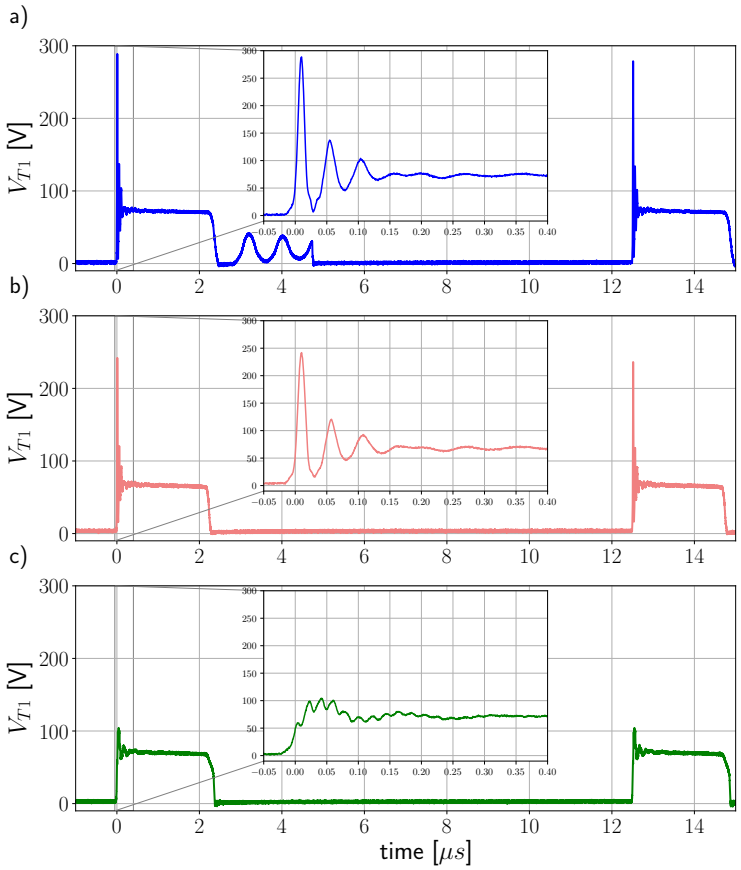


Figure 2.8: Voltage waveforms across transistor T_1; a) DCM hard switching, b) TCM ZVS, c) TCM ZVS with snubber capacitors C_{sn}

The switching strategies described above were compared in Fig. 2.8 by voltage waveforms across T_1 transistor. During DCM and TCM operation, at T_1 turn off significant overvoltage spikes had been recorded due to rapid decrease of current flowing through the stray inductances of input supply circuit. Only application of capacitive snubber attenuated overvoltage amplitudes, in accordance with analytical results of equation (2.11). In zero i_L current intervals of DCM operation, a typical resonant process between capacitances C_{T1}, C_{T2} and inductor L was evoked. In the interval $[t_4 : t_5]$ the C_{T1} and C_{T2} are reloading in resonant circuit with the inductor L causing voltage oscillations across transistors until next period begins [26]. In TCM strategy both transistors operated alternately with predetermined dead times for soft switching transitions and the V_{DS} voltage is free of any oscillation. Fig. 2.8 compares voltage waveforms across T_1 at DCM, TCM and TCM+C_{sn}.

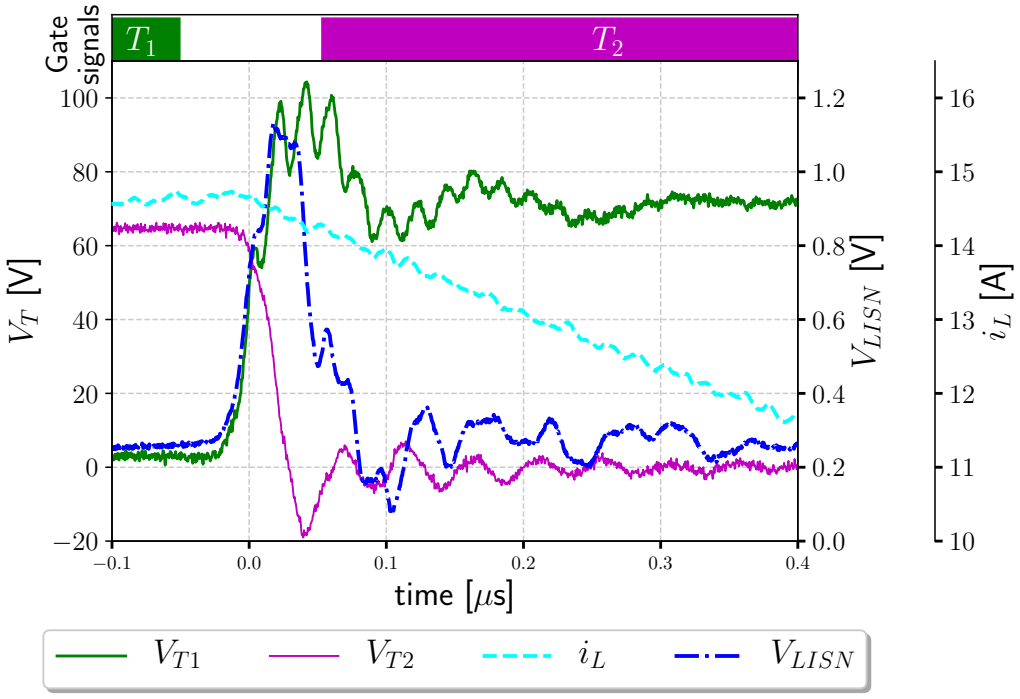


Figure 2.9: ZVS of load current i_l from T_1 to T_2

For TCM+Csn Fig. 2.9 depicts, in larger time scale, current commutation from T_1 to T_2. The T_1 gate turn off initiated resonant charging of C_{T1} and discharging of C_{T2} with corresponding rate of change of transistor voltages: V_{T1} and V_{T2} that depended on load inductor current i_L. The LISN perturbation pulse was coherent with change of transistor voltages. After the recharging process had

been completed T_2 was turned on in ZVS conditions to conduct $i_L > 0$ as synchronous rectifier. To complete TCM sequences Fig. 2.10 presents load current commutation from T_2 to T_1. At predetermined $i_{L(th)} < 0$, T_2 was turned off recharging nonlinear capacitances of both transistors. Due to near zero current transients, a lower rate of change of transistor voltages attenuated the LISN perturbation amplitude. At the end of recharging process, T_1 was turned on at ZVS. Comparative timing specification of TCM with and without capacitive snubber is presented in Table 2.2. In TCM mode, the exact period of recharging output capacitances is crucial to determine dead time and subsequent gate pulse for complementary transistor (to obtain ZVS conditions). It is confirmed that the snubber impacts on extension of resonant transition periods (t_{d1}, t_{d2}) and dV_{T1}/dt turn off decrease. Moreover, falling and rising times are naturally enlarged when snubber capacitors are applied. However, maximal $\frac{dv}{dt}$ during T_1 turn-on final subperiod is dominated by negative load current influence.

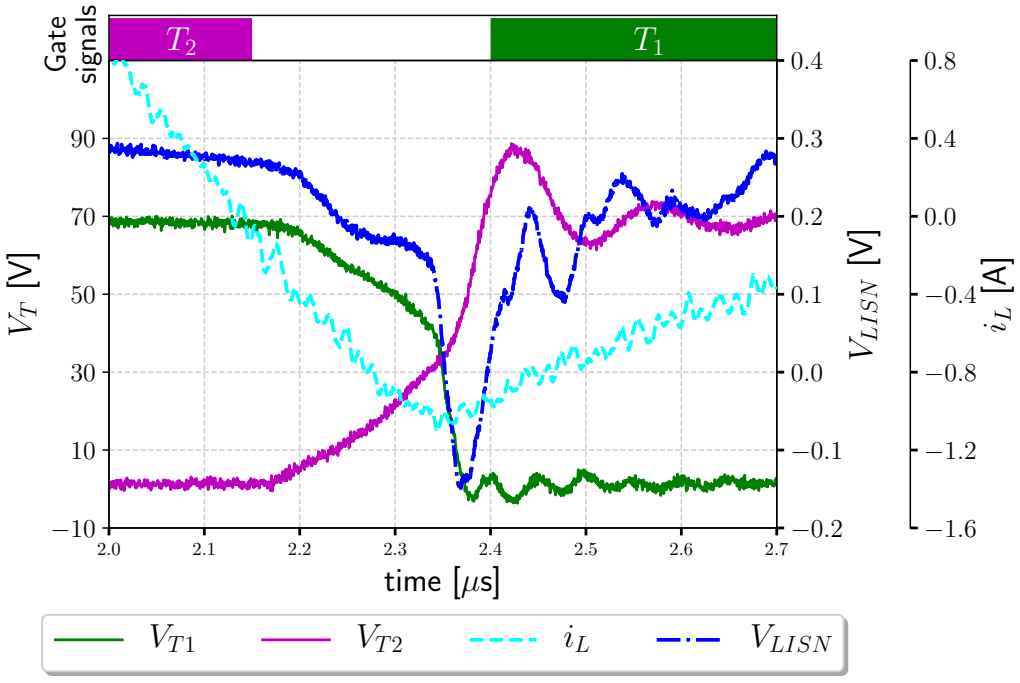


Figure 2.10: ZVS of load current i_l from T_2 to T_1

Table 2.2: TCM Operation without and with C_{sn}

	without C_{sn}	**with** C_{sn} $(3.2\,nF)$
T_1 on time $(t_{on-state(T_1)})$	10.2 μs	10.125 μs
Dead time 1 (T_1 off and T_2 on) (t_{d1})	40 ns	125 ns
T_2 on time $(t_{on-state(T_2)})$	2.05 μs	2.0 μs
Dead time 2 (T_2 off and T_1 on) (t_{d2})	210 ns	250 ns
Max. $\frac{dV}{dt}$ of V_{T1} during turn on	1 $\frac{V}{ns}$	1.3 $\frac{V}{ns}$
Max. $\frac{dV}{dt}$ of V_{T1} during turn off	25.1 $\frac{V}{ns}$	5.6 $\frac{V}{ns}$
V_{T1} falling time during turn on (t_f)	122 ns	218 ns
V_{T1} rising time during turn off (t_r)	30 ns	48.5 ns

2.6.1 Efficiency

Comparative experimental results of buck converter efficiency excluding the gate driving power are depicted in Fig. 2.11 for varying loads. An efficiency increase for ZVS TCM schemes over conventional DCM operation is evident. The highest (almost 1%) efficiency elevation was measured in the case of the TCM with capacitive snubber.

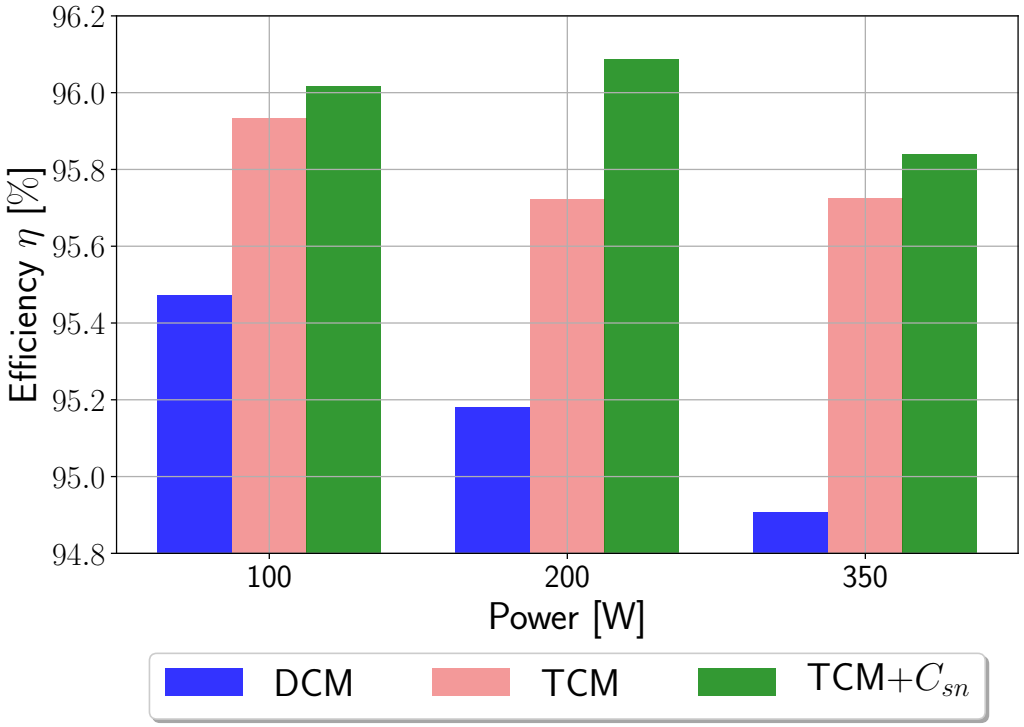


Figure 2.11: Efficiency indexes

The analytical computations of conductive and switching losses were prepared based on [49, 26] and are described below:

- Conduction loss in the GaN FET of Buck Converter in the DCM operation:

$$P_{rDS} = R_{ds(on)} I_{Srms}^2 = \frac{R_{ds(on)} D \Delta i_L^2}{3} = \frac{2R_{ds(on)} P_O}{3} \sqrt{\frac{2M_{VDC}^2 \left(1 - M_{VDC}\right)}{f_s L R_L}} \tag{2.12}$$

where:

$$M_{VDC} = \frac{V_O}{V_I} \tag{2.13}$$

$$I_{Srms} = \sqrt{\frac{1}{T} \int_0^{DT} \left(i_S\right)^2 dt} = \Delta i_L \sqrt{\frac{D}{3}} = V_o \sqrt{\frac{2}{3R_L} \sqrt{\frac{2M_{VDC}^2 \left(1 - M_{VDC}\right)}{f_s L R_L}}} \tag{2.14}$$

- Conduction loss of the diode in Buck Converter for DCM:

$$P_{rF} = R_F I_{Frms}^2 = \frac{R_F D_1 \Delta i_L^2}{3} = \frac{2R_F P_O}{3}\sqrt{\frac{2\left(1 - M_{VDC}\right)^3}{f_s L R_L}} \tag{2.15}$$

where:

$$I_{Frms} = \sqrt{\frac{1}{T}\int_{DT}^{(D+D_1)T} \left(i_F\right)^2 dt} = \Delta i_L \sqrt{\frac{D_1}{3}} = V_O \sqrt{\frac{2}{3R_L}\sqrt{\frac{2\left(1 - M_{VDC}\right)^3}{f_s L R_L}}} \tag{2.16}$$

Average diode current

$$I_{Fav} = \frac{1}{T}\int_0^T i_F dt = I_O\left(1 - M_{VDC}\right) \tag{2.17}$$

$$P_{vF} = V_F I_{Fav} = \frac{V_F P_O\left(1 - M_{VDC}\right)}{V_O} \tag{2.18}$$

Overall diode conduction loss

$$P_F = P_{rF} + P_{vF} \tag{2.19}$$

- In the case of TCM operation, due to the synchronous GaN operation, when $R_{ds(on)} = R_F$

$$P_F = P_{rF} \tag{2.20}$$

- Transistor and converter data used for loss calculation:

Table 2.3: GaN HEMT TPH3207WS: 650 V/50 A - data

Parameter	**Value**
$R_{ds(on)}$	0.035 Ω
R_F	0.035 Ω
E_{OSS} (@ $U_{DS} = 70\,V$)	2.0 μJ
V_F (@ $I_S = 10\,A$)	1.0 V
C_{DS} (@ $U_{DS} = 70\,V$)	0.6 nF
C_{DS} (@ $U_{DS} = 15\,V$)	0.92 nF

where:

$$C_{DS} = C_{OSS} - C_{RSS} \tag{2.21}$$

Table 2.4: Buck Converter data and rated conditions

Parameter	**Value**
V_I	70 V
V_O	55 V
P_O	350 W
f_s	80 kHz
R_L	8.6 Ω
L	8.7 μH
M_{VDC}	0.7857
C_{sn}	3.2 nF
L_s	0.114 μH
Δi_{Lmax}	15.2 A

- Results of conduction loss:

Table 2.5: Conduction loss for DCM and TCM operation at output power 350 W

	T_1	T_2	$T_1 + T_2$
Transistor conduction loss for the DCM operation	1.72 W	1.83 W	3.55 W
Transistor conduction loss for the TCM operation	1.72 W	0.47 W	2.19 W

- Transistor switching loss in the DCM operation:

$$P_{T1(turn-off)} = \frac{4 f_s V_I^2 C_{DS}(V_I)}{3} + \frac{f_s \Delta i_{Lmax}^2 L_s}{2} \tag{2.22}$$

$$P_{T1(turn-on)} = \frac{2 f_s C_{DS}(V_I - V_O)[V_I - V_O]^2}{3} \tag{2.23}$$

$$P_{T2(turn-on)} = \frac{2 f_s C_{DS}(V_I) V_I^2}{3} \tag{2.24}$$

- Transistor switching loss in the TCM operation:

$$P_{T1(turn-off)} = \frac{4 f_s V_I^2 C_{DS}(V_I)}{3} + \frac{f_s \Delta i_{Lmax}^2 L_s}{2} \tag{2.25}$$

- Transistor switching loss in the TCM + C_{sn} operation:

$$P_{T1(turn-off)} = \frac{4 f_s V_I^2 C_{DS}(V_I)}{3} + \frac{f_s \Delta i_{Lmax}^2 L_s}{2} - \frac{f_s V_I C_{sn}}{2} \tag{2.26}$$

The results of computed conductive and switching losses of the considered buck converter schemes are presented in Fig 2.12 for the rated output power.

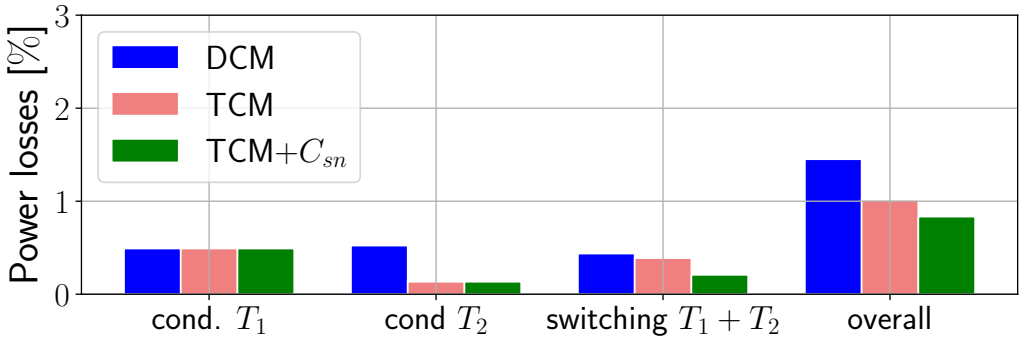


Figure 2.12: Power loss distribution (P_o=350W)

The T_1 conduction loss is approximately constant due to comparable transistor current waveforms in the DCM and TCM operation. The T_2 conduction loss is decreased in the TCM because of synchronous rectification mode of operation (due to the lower voltage drop on the conducted MOSFET transistor than on the internal diode).

Main part of switching loss is caused by T_1 turn off. This is the energy lost in the resistance $R_s = R_{ds(on)}$ of the charging path of C_{T1} capacitance and during the resonant turn off oscillations. In the DCM operation during turn on, the energy stored in the transistor capacitance is lost in the transistor on-resistance.

During TCM operation, switching power loss is reduced due to resonant transition of the energy accumulated in transistor capacitances at the ZVS between T_1 and T_2. In the case of TCM + C_{sn} the energy stored in the snubber capacitance is also recycled in a resonant transition phase. Moreover, in the resonant transition phase the energy loss in the R_s does not occur because first the capacitance recharging process is completed and then the transistor is turned on.

2.6.2 EMI attenuation

In Figures 2.14-2.13 the spectra of common and differential modes are respectively presented for three switching strategies. The signals have been registered in time domain using LISN and separated offline for common and differential

modes [64] using (2.27) and (2.28). This method was used to perform the EMI identification in the test bench without EMI spectrum analyzer. In this specific case the waveforms must be captured in time domain to identify phase shift between them and calculate CM and DM noise correctly.

$$|V_{CM}| = \left| \frac{V_{LISN2} + V_{LISN1}}{2} \right| \tag{2.27}$$

$$|V_{DM}| = \left| \frac{V_{LISN2} - V_{LISN1}}{2} \right| \tag{2.28}$$

Both CM and DM EMI spectra indicate significant peaks of the switching frequency f_s harmonics, that are related to the triangular inductor current waveforms of converter operation including multiples of switching frequency.

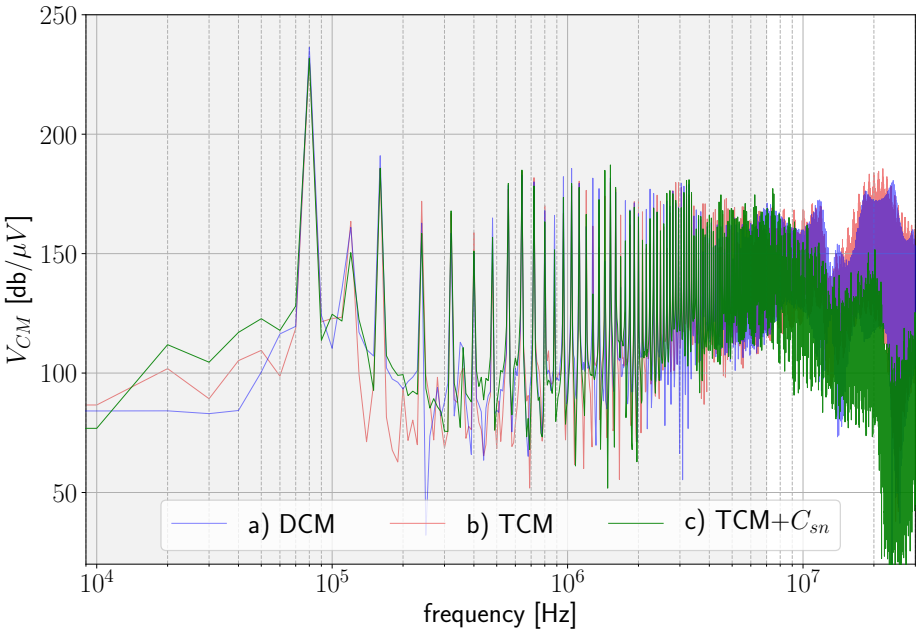


Figure 2.13: EMI common mode spectra

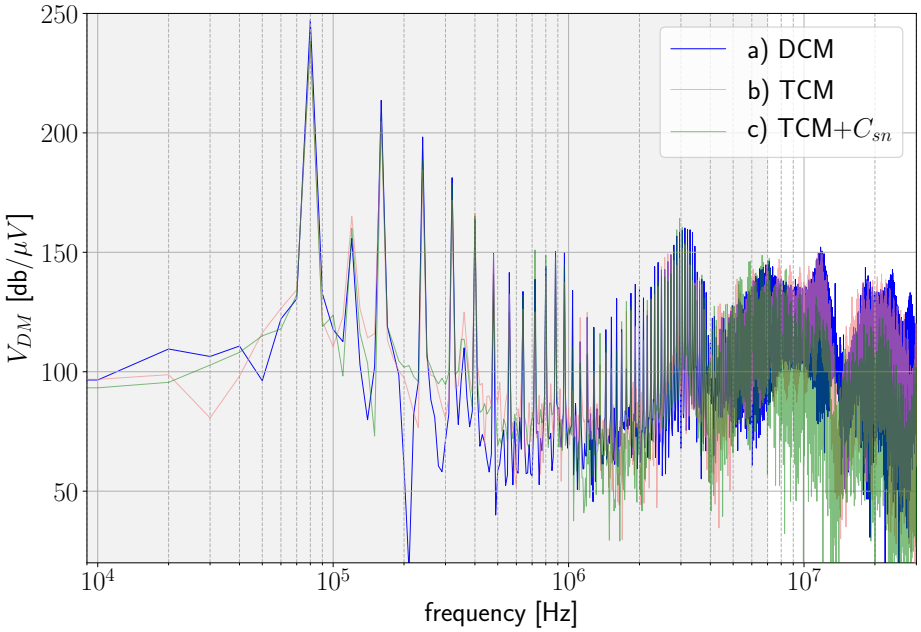


Figure 2.14: EMI differential mode spectra

In order to analyze CM current loops during switching from T_1 to T_2, based on the buck converter test scheme from Fig 2.1, an equivalent circuit is derived as in Fig 2.15. The CM interference is propagated to the LISN RC branches in the loop containing parasitic capacitances between the heat-sink and the drain node $T_1 : C_{t-h}$, the drain node $T_2 : C_{m-h}$, the source node $T_2 : C_{b-h}$ and the ground C_{h-gnd} which affect the CM level.

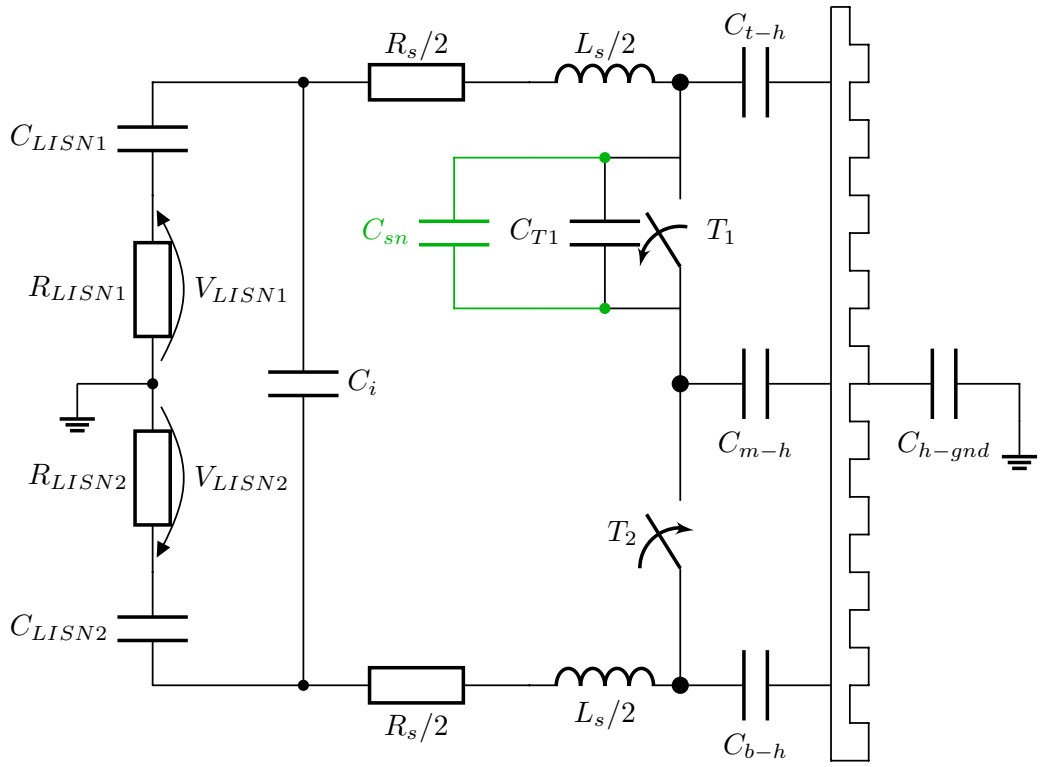


Figure 2.15: Equivalent circuit of CM current loops during switching from T_1 to T_2

CM perturbations propagate through parasitic capacitances $C_{t-h}, C_{m-h}, C_{b-h}$ and C_{h-gnd}. The envelope spectra obtained for CM emission are higher than for the DM emission. In the range above 10 MHz an impact of overvoltage peeks with ringing effects when T_1 turns off is observed (as was depicted by large scale voltage transients in Fig 2.16). To be noticed, emission levels are comparable for the DCM operation and for the TCM without snubber operation. This is because in both cases the voltage waveforms are dominated by extremely high overvoltage peaks at the T_1 turn off instant. But in the case of the TCM+C_{sn}, attenuation of the CM interference in the range starting from 7 MHz reached almost -40 dB at 20 MHz.

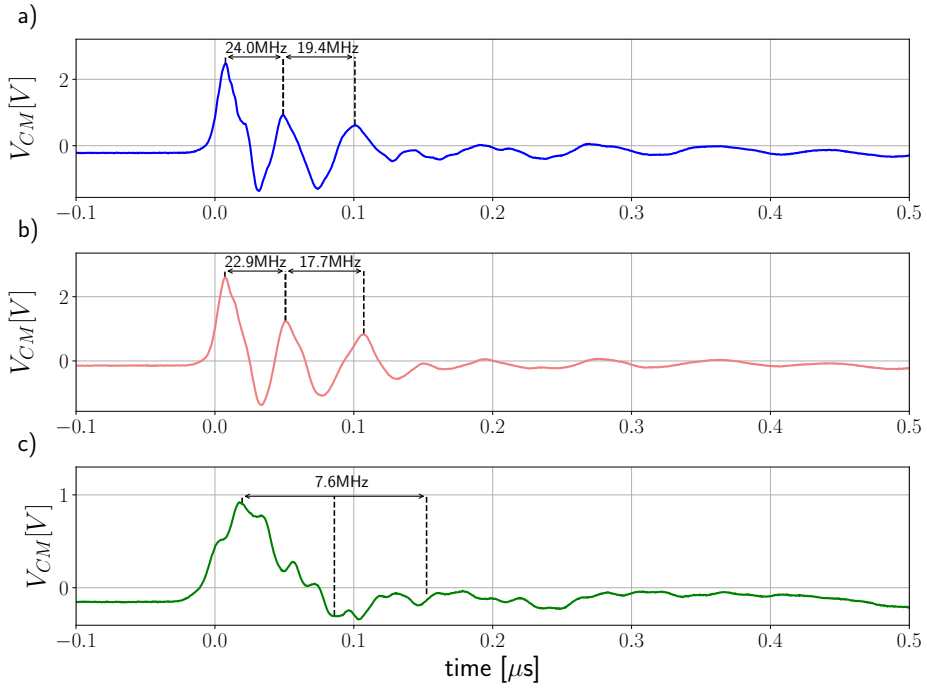


Figure 2.16: CM voltage ripples during switching from T_1 to T_2 a) DCM b) TCM c) TCM+C_{sn}

The main components of parallel resonant circuit where the ringing interference is generated are the input stray inductance L_s, the nonlinear drain-to-source capacitance $C_{T1}(V_{DS})$ and the conductive path resistance R_s that are shunted by input filter capacitor C_i. Hence, the ringing frequency:

$$f_r \approx \frac{1}{2 * \pi * \sqrt{L_s * C_{T1}(V_{DS})}} \tag{2.29}$$

Since the nonlinear capacitance depends on drain-to-source voltage, the f_r varies in the range from 27 MHz for $C_{T1}(V_{T1(max)})$ to 17 MHz for $C_{T1}(V_i)$ (Figure 2.16). The parasitic capacitances to the heat sink are resulting in an increase of C_{DS} capacitance (C_{t-h} in series with C_{m-h}), but they are very small then it is neglectible. Augmentation of C_{T1} by the snubber capacitance C_{sn} leads to attenuation of the voltage overshoot with frequency decrease of the ringing interference:

$$f_r \approx \frac{1}{2 * \pi * \sqrt{L_s * (C_{T1}(V_{DS}) + C_{sn})}} \tag{2.30}$$

The frequency f_r calculated using eq. 2.30 for parameters from Table 2.1 equals 7.64 MHz - see Fig. 2.16.

2.7 Control strategy - conclusions

In a GaN HEMTs based DC-DC Buck converter the EMI conducted emissions were measured for Discontinuous Current Mode and Triangular Current Mode control strategies. Zero Voltage Switching that was achieved for the TCM operation revealed improvement of power conversion efficiency with the reference to the DCM operation. In the TCM a ZVS occurs at turn-on and turn-off, due to resonant recharging transitions with adapted gate pulse control. Implementation of capacitor snubbers across transistors for TCM operation slowed down transistor turn off process clamping voltage spikes. In consequence significant attenuation of common mode EMI emission with slight increase of power conversion efficiency were obtained.

Chapter 3

Design and implementation of GaN devices for mitigation of EMI noise

The results presented in the following chapter have already been the subject of a number of published papers:

- Derkacz, P. B., Schanen, J. L., Jeannin, P. O., Chrzan, P. J., Musznicki, P., & Petit, M. (2022). EMI mitigation of GaN power inverter leg by local shielding techniques. IEEE Transactions on Power Electronics, 37(10), 11996-12004.
- Musznicki, P., Derkacz, P. B., & Chrzan, P. J. (2021). Wideband modeling of DC-DC Buck converter with GaN transistors. Energies, 14(15), 4430.
- Derkacz, P. B., Schanen, J. L., Jeannin, P. O., Musznicki, P., Chrzan, P. J., & Petit, M. (2020, September). 3D PCB package for GaN inverter leg with low EMC feature. In 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe) (pp. P-1). IEEE.

"The most beautiful experience we can have is the mysterious."

Albert Einstein

3.1 Evaluation of inverter leg

The research results presented in the Chapter 2 show the impact of control strategy on EMI. However, the need of a capacitive snubber to achieve noticeable noise reduction and to improve electrical performance of converter waveforms (smoother current and voltage waveform with reduced overshoots and oscillations) indicates additional problems and limitations in the studied system. Further detailed analysis of the converter circuit has led to conclusions that parasitic (stray) elements are the main factors and they need deep identification of their location, value and impact. They are directly related and dependent on layout. The term layout includes an arrangement of electrical components in a given geometry (usually on a PCB printed circuit), connections between components through copper tracks, their shape and relative reference to other tracks, their arrangement on successive conductive copper layers inside the PCB, and structure of conductive layers and distances between them (Stack-up). Even the greatest effort devoted to control strategy with inadequate layout of GaN converter will reduce EMI distortions and improve electrical performance (voltage and current shapes) only slightly. Thus, there is a need for in-depth studies of the layout impact of the electrical performance and EMI generation inside of the converter.

For the presented research, the elementary building block as single inverter leg has been considered. Inverter leg (also called switching cell) is composed of two series connected transistors, distinguished middle point (MID) from between them, decoupling capacitor connected across both transistors, gate driver circuits with its power supplies, and all interconnections between them (as presented later in Fig. 3.3). In this arrangement, the user has access to 3 power ports, two control signals, and two auxiliary supplies for the gates. This basic building block should be considered as an elementary switching unit. By developing a suitable layout, it can be ensured the highest quality of electrical performance and reduced EMI disturbance at its source. This approach allows to develop high performance switching block that can be used in many converters/topologies, many configurations and different number of blocks. The idea of elementary block and its multiplication in purpose of building full converter with more complicated topology is widely known [51, 50, 61, 24, 30, 31, 38]. In extended topologies,

therefore, this layout can be duplicated many times, and it will still provide low EMI and high signal quality for the entire converter. The above constitutes, in the author's opinion, a reasonable consideration of the inverter leg as the elementary and most important unit to be optimized.

It is necessary to distinguish nomenclature because the presented circuit is not a power module, as it contains more components than only two series connected transistors (and in some solutions a decoupling capacitor is included). Due to the impact of the gate drivers (its outputs and power supplies circuits) on EMI generation the following distinction has been adopted. However, the insights, research results, and developed solutions can be transferred to GaN-based power modules.

3.1.1 Impact of stray elements

The impact of the stray elements can be observed in both the quality of electrical performance and electromagnetic disturbance (EMI). For understanding of the origin of unwanted oscillations, overshoots and interferences in the power converters, the knowledge of stray parameters of all their components is required. Components like semiconductor switches, passive elements, drivers, connectors, but also conducting copper tracks and wires contain parasitic elements. In the process of modeling, these elements should be taken into account because they play a significant role in disturbances generation and propagation. The high frequency ringing oscillations, noise, and overvoltages are generated in the resonant circuits, including RLC stray elements. Interferences and undesirable currents to the ground are propagated mainly through stray capacitances and through the conducting tracks which are subject of magnetic and capacitive coupling.

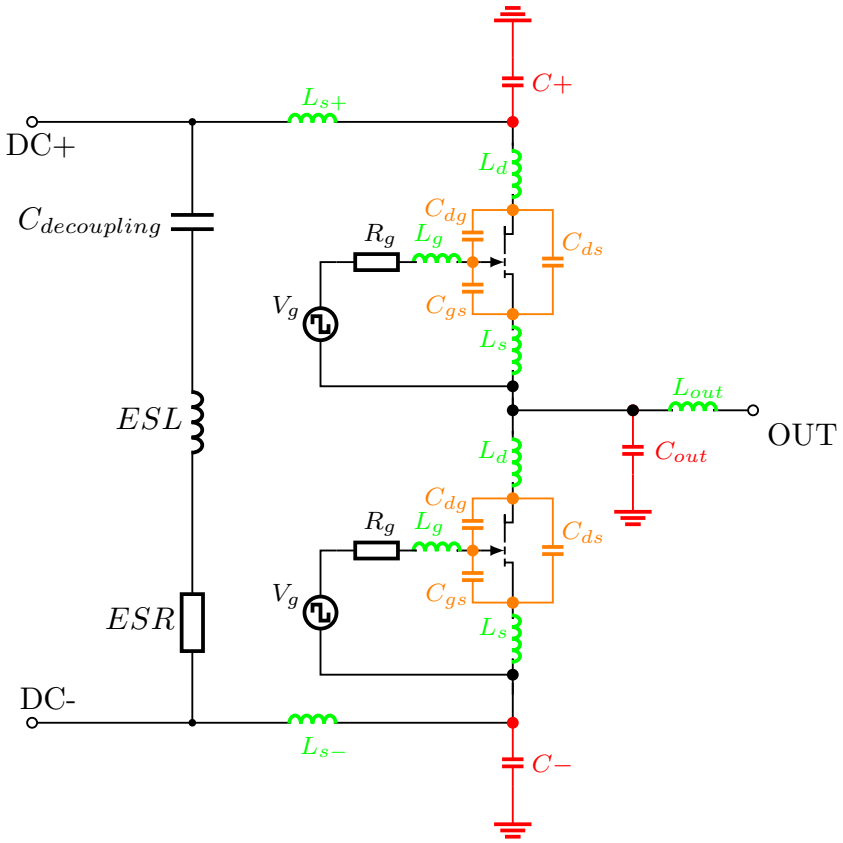


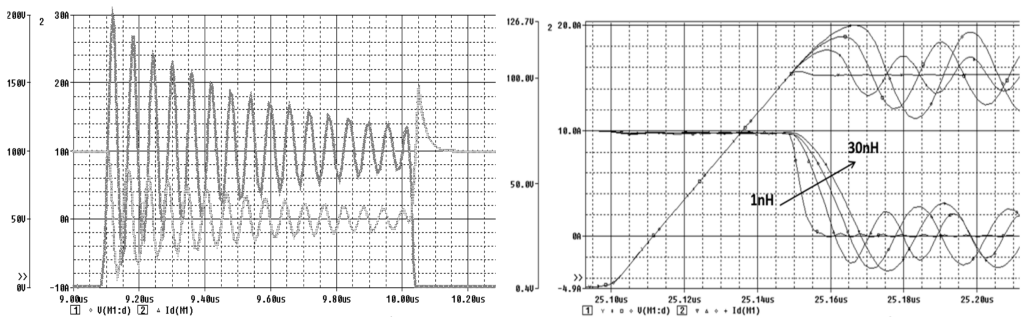
Figure 3.1: Some stray elements of a power module with decoupling capacitor

In detail, there are at least several observable phenomena caused by parasitics. They are described below with the usage of classic power module and inverter leg schemes.

Drain-source voltage (V_{DS}) overshoot and ringing

High speed switching of transistors in the inverter leg leads to a commutation overshoot across the turning off transistor. It is related to the break of current flow through the transistor and existence of stray inductance in the commutation loop (called power loop inductance L_{power}). The Fig.3.1 is presenting a scheme of power module with decoupling capacitor. Based on this scheme, the L_{power} inductance is equal to the sum of L_{s+}, $2L_d$, $2L_s$, L_{s-}, and ESL of decoupling capacitor + mutual inductances between them. The high current slope induces an voltage spike equal to $L_{power} \cdot \frac{dI}{dt}$ that is added to supply voltage. The sum of both is seen as drain-source voltage across the transistor. This phenomena prevents using the switches at their maximum voltage rating. Moreover, the

power loop inductance together with output device capacitance (C_{oss}) is creating the resonant circuit and originating the ringing of the V_{DS} voltage. These two phenomena generate additional losses [95] and also increase the EMI (adds additional peaks in the high frequency range of EMC spectrum) [76]. In the desired layout, the power loop inductance should be minimized to nano- or sub-nanohenrys.



(a) (b)

Figure 3.2: (a) Illustration of undamped voltage ringing at device turn off [76], (b) Illustration how power loop inductance reduce the commutation current transients [76]

Gate voltage ringing

Next phenomenon is related to the gate circuit. The existence of stray gate inductance (L_g in Fig.3.1) is impacting the speed of the switching transients and adding unwanted oscillations. The turn on time of the device is controlled by gate circuit impedance. Usually a certain value of gate resistance is used to set up this time. However, the excess value of stray gate inductance is notably increasing the impedance of gate circuit. It leads to excessive limit of the gate current and the input capacitance C_{iss} of the device is charged slower. The turn on time is extended resulting in higher switching losses. In addition, gate inductance combined with C_{iss} can generate ringing which affects the switching performance or the switch itself, in case of exceeding the maximum voltage rating on the gate (which is around 10 V in some GaN technologies). As a result, the transistor's drain current oscillations, shoot through current in a inverter leg or damage of the device gate may occur. To sum up, the gate circuit should be designed to achieve as low as possible gate inductance.

Common source inductance and power-drive interactions

The closer look to the surrounding of transistor allows to notice one specific common stray element for the power and gate circuit. It is a L_s stray inductance. This element is critical since the power current generates voltage drop on it (various and depending on the current value) resulting in a change of the voltage applied to the gate of the transistor. As a consequence, the speed of commutation is changed. Moreover, due to the close proximity of both gate and power circuits, the L_s and L_g stray inductances (in Fig.3.1) are magnetically coupled (and therefore the power circuit current influences the gate circuit impedance). The desired layout design should minimize the effect of interactions. One of the possible ways is to use transistor with dedicated source connection to the gate circuit which is separated from power circuit (Kelvin connection - source). However, not all transistor packages have this solution, then creation of its own Kelvin source connection in the layout track is recommended [76]. Furthermore, the Kelvin connection is not a guarantee of safe commutation, since it does not necessarily avoid the effect of mutual couplings.

Stray capacitances impact on the commutation speed

The stray capacitances of the inverter leg also have a strong impact on commutation speed. Mainly, the devices' internal stray capacitances C_{ds}, C_{gs}, and C_{dg} define the maximum switching speed - Eq. 3.1 [10]. However, the impact of external stray capacitances must be taken into account and their value should be added to internal capacitances. The illustration of this impact is already presented for a capacitive snubber - Chapter 2.5. These external parasitics can be created by the layout (in the multilayer designs) and sometimes are intentional (i.ex. capacitive snubbers). The layout design should address this requirements to achieve desired speed of the switches.

$$\frac{dV}{dt}(MID) = \frac{I_L}{C_{eq}} \tag{3.1}$$

where:

$\frac{dV}{dt}(MID)$ - voltage steepness in middle point;

I_L - load current;

C_{eq} - equivalent parasitic capacitance for the traditional gate driver architecture.

Conducted noise generation (CM and DM currents)

In the conducted noise, it can be distinguished the Differential Mode and Common Mode type of disturbances. First one flows between power source and the converter in both lines, in opposite directions. By providing clean switching conditions (no overshoots, oscillations, etc.) the level of DM can be minimized. The second one is related to parasitics in the system and with capacitive nature of the layout. The CM current is generated due to occurrence high $\frac{dV}{dt}$ and flows through stray capacitances to the ground of the system. Basically, from the point of view of the source of CM currents, the most important is the capacitance C_{out} at the middle point (MID) (between the transistors) where the high $\frac{dV}{dt}$ is created. Value of the CM current depends on the magnitude of $\frac{dV}{dt}$ and on the value of the capacitance C_{out}. This current then splits within the system and flows through other parasitic capacitances to ground [76]. However, this thesis research proved that C_{out} capacitance is not a lumped parasitic element in one place. In order to correctly identify the value of C_{out}, it is necessary to analyze circuit much wider than just the power module (Fig. 3.1). It also includes gate circuits, their power supply, and takes into account the cooling system of transistors - this circuit is called inverter leg and is presented in Fig. 3.3. Moreover, the used transistors have a dedicated thermal pad to transfer heat to the heat sink. This pad is internally connected to the source potential of the transistor. Thus, together with the grounded heat sink, it creates (in the case of high side transistor) a significant capacitance to the ground, which is a component of C_{out}. In addition, the gate circuit and the isolated side of the driver, work with respect to the source potential of the transistor. Thus, the paths connecting the high side transistor to the driver (which are at the source potential) and further the power supply tracks of the driver create another component of parasitic capacitance to ground. Their influence and specification are described in detail in Chapter 3.2. In addition, the distributed capacitances of the load create a path for CM currents coming out of the converter and increase the overall CM noise generation observed in the LISN. Therefore, it is considered to integrate an inductive output filter (or Common Mode Choke) with CM current suppression capability into the inverter leg topology. In this way, the common mode current is closed within the power module and the load effect is minimized. Detailed considerations are presented in Chapter 4.

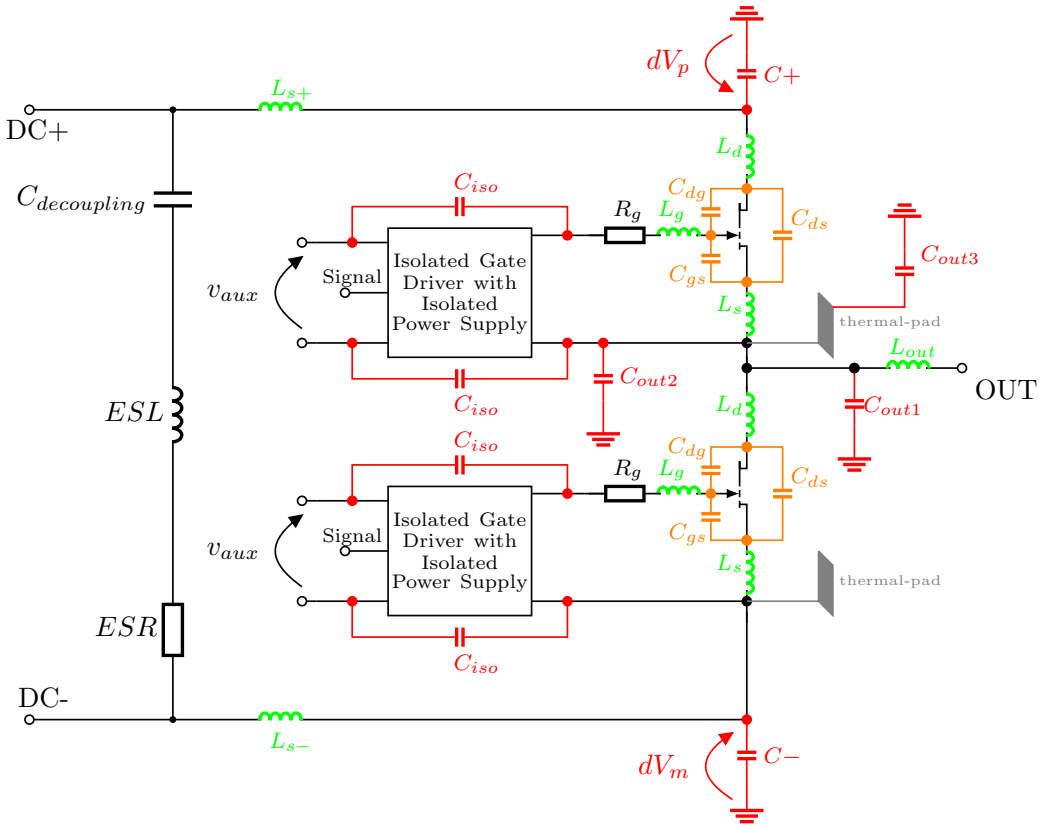


Figure 3.3: Stray elements of a inverter leg indicating the middle point capacitance C_{out} built-up.

Part of CM current can recirculate inside the converter due to the existence of $C+$ and $C-$ capacitances, as shown in Figure 3.3. Though, attention must be paid to the symmetry of $C+$ and $C-$ (as explained in [39]). High frequency DC bus current generate voltage drops dV_p and dV_m. As a result, voltage variation are induced on C+ and C-, leading to CM current. This is often referred as DM to CM conversion (mode coupling). Thus, the symmetry of stray inductances and stray capacitances $C+$ and $C-$ is required (as well as symmetry of inductive stray inductance). In that case, the $C+$ and $C-$ currents will be opposite and cancel each other out. Otherwise, it will generate a high level of CM current.

Magnetic and capacitive coupling of stray elements

Determining of stray elements is not only search of its location and value. Moreover, it is the knowledge about the coupling between them [76]. Only in the surrounding area of one transistor exist three magnetically coupled stray inductances (as in Fig. 3.4). Similar couplings can be find in other locations inside inverter leg. Also, for multilayer layout there are some mutual capacitances be-

tween tracks. Summarizing, the manual finding or predicting of the location, value, possible coupling of stray elements inside power module or inverter leg is impossible. For this reason, the only solution is a 3D quasi-static electromagnetic (EM) simulation software (e.g. ANSYS Q3D) or Partial Elements Equivalent Circuit based simulator (e.g. Altair Flux-PEEC)

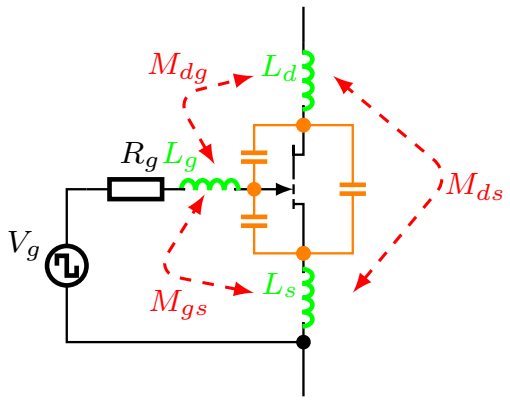


Figure 3.4: Magnetically coupled stray inductances of one transistor

Conclusions

The knowledge and understanding of phenomena is fundamental to design a proper layout of inverter leg or power module. Development of new inverter leg with high speed devices (as GaN HEMT) requires reinforced consideration of stray elements and couplings between them by designer. Awareness of an impact of the geometry, alignment and interplay of the various components and connections is key to achieving satisfying switching behavior for Wide-Bandgap devices. Presented constraints are crucial in a good power layout and next efforts have to be put to optimize EMC behavior (reduce CM emission and power-drive interactions).

The following chapter section addresses the aforementioned issues. For the detailed study of parasitics, two available options were recognized: by measurement (multiple prototype construction, observation of overvoltages, oscillations, electrical performance, and EMC measurements), or by digital-twin (a multi-platform process of design, electromagnetic and circuit simulations at the end combined with verification of the physical prototype). The first option is much more time- and cost-intensive, and furthermore does not allow to separate effectively all various contributions of layout to inductive behavior, since they only

provide global inductance value. Moreover,, the impact of measurement devices (e.g. scope probes) could be huge and leads to large errors. Therefore, it was decided to conduct further research considerations based on digital-twin. The digital twin also allows the evaluation of the impact of all stray elements on the EMC generation, offering the possibility of considering only some stray elements (and considering that other stray elements of the inverter leg are perfect), that is not possible with a practical approach.

3.1.2 Simulation method

In the following research, specific simulation procedure has been developed to obtain the values of stray elements and determine their impact on the generated EMI. Firstly, the desired layout of the inverter leg must be designed in accordance to the guidelines and constraints that we set (author's layout example is presented in Fig. 3.27). The design is made in Altium Designer and the OBD++ files are generated for further simulations. Then, the PCB layout model is created using ANSYS Q3D software, matrix of stray elements values is obtained and converted to electrical SPICE model. Next, the SPICE model of PCB is imported to Synopsys Saber simulator and the electrical models of transistors, resistors, capacitors etc. are added together with closed control loop for the converter. Finally, the Saber performs the electrical simulation and the currents and voltages waveforms are obtained. Also, the Common Mode and Differential Mode currents are captured, then subjected to FFT analysis in MATLAB and the spectra of these signals are plotted. Full simulation workflow is presented in the Figure 3.5. A detailed description of the key steps in the full simulation process is provided below.

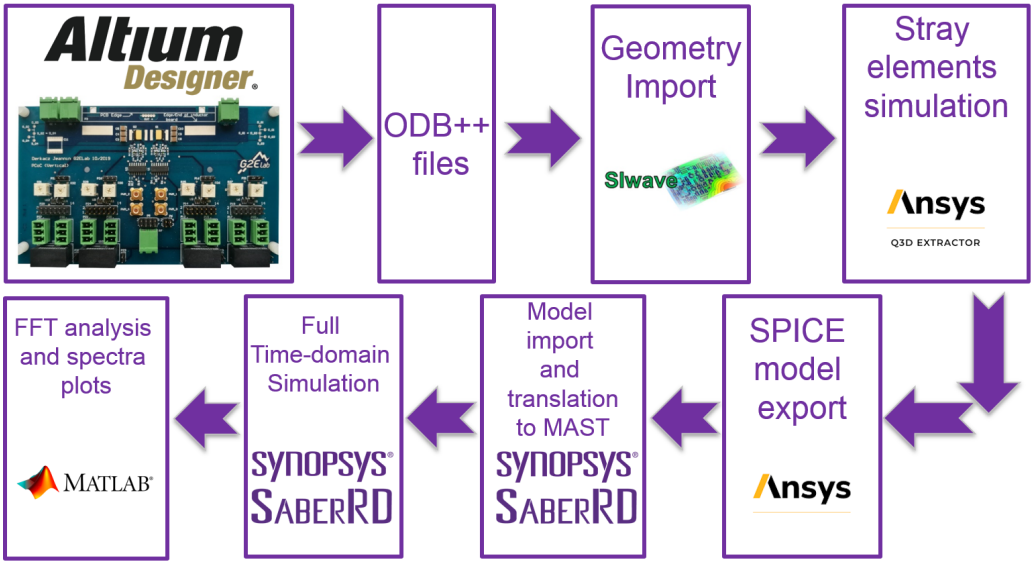


Figure 3.5: Developed simulation workflow for Digital Twin

PCB layout model

The PCB layout including the conducting tracks, wires and cables have a primary importance in high frequency behavior of the converter. The magnetic and electric couplings of conducting tracks can be represented by the coupled inductors and capacitors. Many software packages can be find in the market which are used to model PCB parasitics. The focus is on Q3D Extractor from ANSYS or PEEC (Partial Element Equivalent Circuit) method [74] used by e.g. Flux-PEEC from Altair. The geometry of layout is defined and/or exported to the applied software environment (in the considered scenario, with the generation of ODB++ files, the layout is imported from Altium Designer) and next ready-to-use model is generated. The following is a description of the rules for calculating and generating the model for both of these software programs.
The PEEC method allows to calculate the value of resistance and self & mutual inductances using geometrical and physical properties of the tracks. The formulas can be directly implemented in the computing environment. On the other hand, using the Q3D Extractor, first sources and sinks should be defined (to determine the directions of the currents inside the layout) and then the model including inductors equal to half of the total inductance between two nodes (T-type model), inductive couplings between each inductor, resistors representing of

AC and DC resistance of the tracks, and capacitors for the capacitance between previously defined sources and between sources and artificial reference point (Fig. 3.6). Using the artificial reference points allows to define the capacitance between each conducting track and the ground if it is placed within the circuit. However, user has not an access to this artificial point in generated ready-to-use model. Thus, the additional reference point of ground (if it is considered, i.ex. for EMC purposes) should be also included in Q3D model. In Q3D Extractor, models are generated for the one selected frequency, thus for other frequencies (e.g harmonics) an inaccuracy may appear. However, the great advantage of these models is their numerical stability. In the given case, the 100 MHz frequency was chosen as this is the frequency corresponding to the rise and fall times of the voltage on the GaN transistor, according to the formula 3.2 [71]

$$f \approx \frac{1}{t_{rise} \cdot \Pi} \approx \frac{0.35}{t_{rise}} \tag{3.2}$$

In the PEEC method, each conductor is segmented (meshing step). Next, resistance, self inductance and mutual inductance between each segment are calculated. In this approach a frequency-independent model, that takes into account the skin or proximity phenomena, is obtained.

The topologies of both models are totally different. However, the simulation of both models should provide the same results. In order to show the differences in the models, the simple example of two conducting parallel tracks (two microstrip lines example) is shown in Fig. 3.6. The Q3D model from Fig. 3.6b includes RL components, capacitors between A and B sources and reference point. The C and D points were defined as sinks. The magnetic coupling is realized by use of the coefficient k.

In order to keep the clarity of the diagram, the PEEC model of only one track is presented in Fig. 3.6c. It is divided into n number of segments. The presented circuit is simplified to make it easier to read: the complete model should contain the same model of the second track and the mutual inductances M between all segments of both tracks and capacitance between them [67].

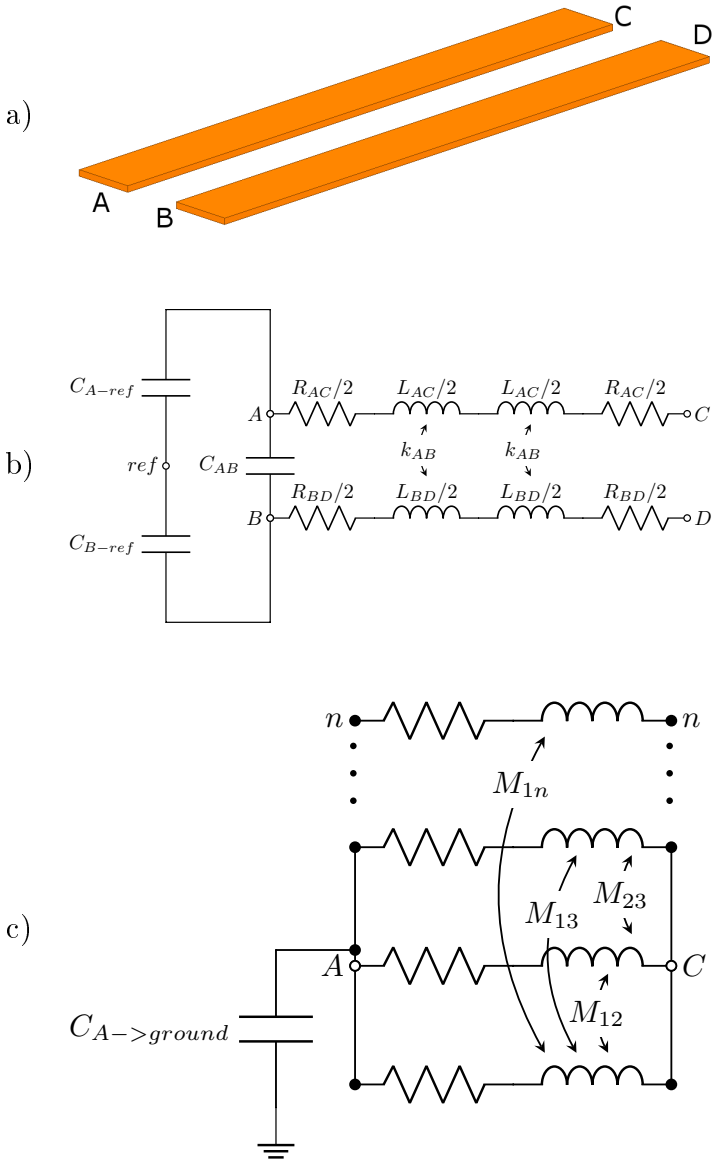


Figure 3.6: The example of two conducting copper tracks a) geometry view b) model generated with Q3D Extractor c) model generated with PEEC method [67]

As shown above, the differences between models are significant, but the operation of models in the circuit simulator is very similar, and results are almost identical. Therefore, due to ANSYS' much more convenient and comprehensive support for importing complex track geometries and PCB layer layouts, Q3D was selected and used in further simulation studies.

The basis of the research is the optimal (in terms of EMC) arrangement of the power tracks and gate circuits of GaN transistors. The verification of such a layout therefore starts with its design in Altium Designer (AD) (Fig. 3.7). AD's built-in tool then converts the designed layout, along with the selected layer stack-up, into ODB++ files (proprietary CAD-to-CAM data exchange format). The ODB++ files are then imported into the ANSYS SIwave environment where additional data processing must be performed. The stack-up should be checked for correctness, redundant paths and elements should be removed, and all elements that constitute a single path (all individual geometric shapes, vias, etc.) should be merged. The last step is due to the fact that in the CAM files each path is broken down into elementary geometries (triangles, squares, semicircles) and these must be unified to be considered as a single routing element in further steps. Once this is done, the model is transferred from SIwave to Q3D where the next steps are performed.

Fig. 3.8 shows the view of the imported geometry. Before running the simulation engine, the critical parameters must be set. For each track, the net name is aligned and the current source (+) and sink (-) points are defined. Due to the specificity of the model (as mentioned earlier), the reference ground must be added to the model. Finally, the specific model frequency is set in the solver, the meshing operation is performed, and the solver is run. The results are presented as a matrix of values, but the built-in generator allows creation of the circuit model as a SPICE netlist.

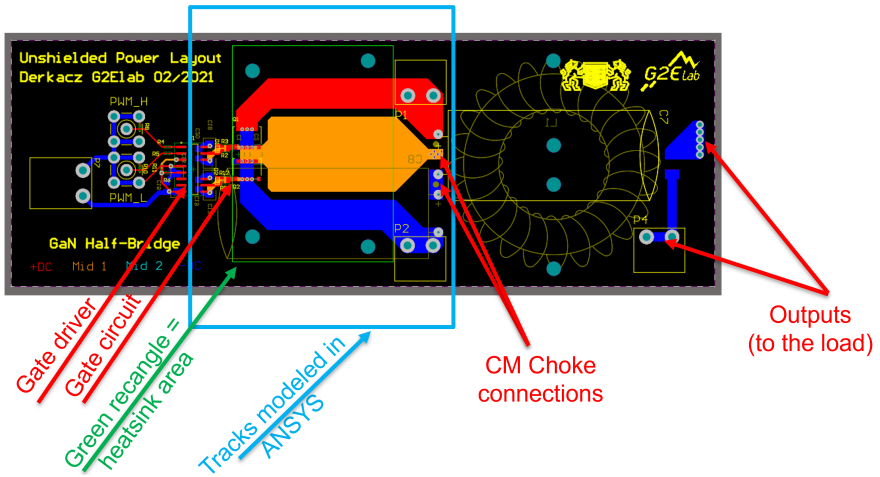


Figure 3.7: A view of the PCB layout of the considered inverter leg design, with an indication of the area being modeled in ANSYS Q3D

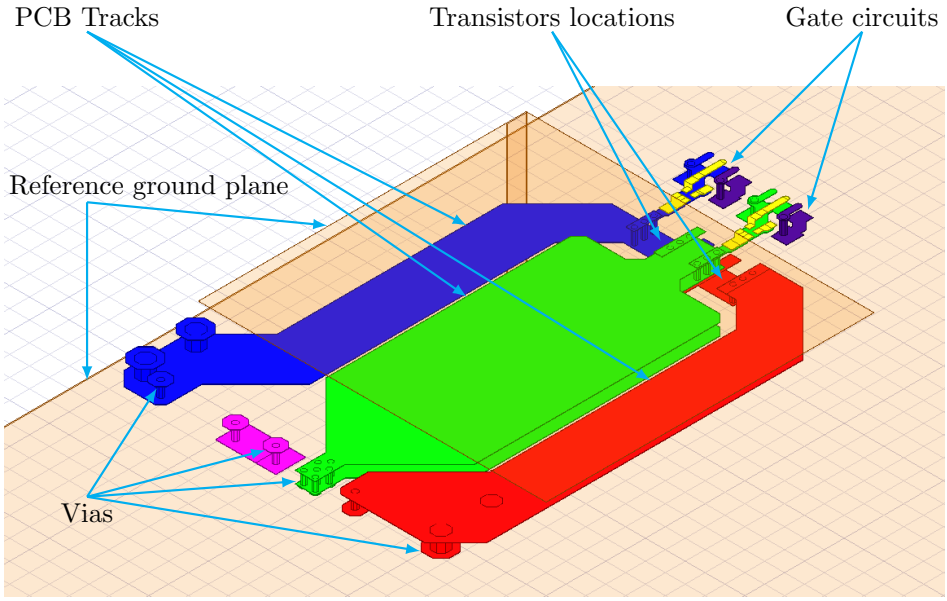


Figure 3.8: Imported model to ANSYS Q3D

Circuit model

A Synopsys Saber simulator was used to perform a full circuit simulation in the time domain. Several criteria guided the chosen simulation software.

First, the main difficulty in simulating circuits with many parasitic elements (which is essential to determine their effect on EMC) is the very small computational step compared to the time constant of the system, which is the entire converter. The considerations carried out concern signals with a corresponding

frequency of 100 MHz (Eq.3.2). Therefore, according to the Nyquist-Shannon statement, the sampling (calculation) frequency should be at least two times higher than the highest frequency considered in the system. Thus, for the system under consideration, the computation step should not be larger than $5 \cdot 10^{-9}$. Secondly, the chosen calculation engine/method together with the specified minimum calculation step should provide a stable steady-state solution. In the presented solution, the Newton-Raphson algorithm was used with a variable calculation step ranging from $5 \cdot 10^{-9}$ to $1 \cdot 10^{-14}$. It should also be mentioned that numerous nonlinear elements together with differential equations lead to stability of solutions in a very narrow range. Therefore, depending on the specific simulation, the parameters of the Newton-Raphson algorithm were adjusted accordingly.

Finally, from a utility point of view, the computation time for a single solution is also important. It is evident that calculations with such a small step require large resources of computing power and computer memory. Based on the same hardware platform, a comparison was made between an identical scheme with GaN transistors in SPICE (LTspice) and the Saber simulator. The results showed that the Synopsys Saber simulator was more than 5 times faster, which was another key factor.

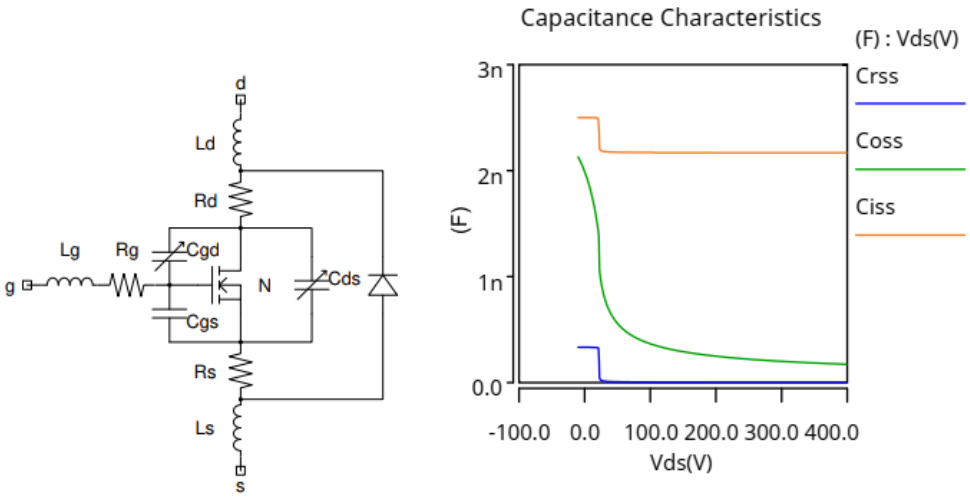


Figure 3.9: GaN transistor model schematic and its nonlinear junction capacitances - view from internal Power MOSFET Tool of Saber

Saber allows for behavioral simulation, and this fact was used in the research described here. To accurately reproduce the shape and the slew rate of voltages and currents associated with fast switching GaN transistors, a behavioral model of this transistor was created. Using Saber's internal tool, a custom model was created based on nonlinear characteristics: output (I_{DS} vs. V_{DS}), transition (I_{DS} vs. V_{GS}), gate charge (Q_G vs. V_{GS}), conduction resistance ($R_{DS(on)}$ vs. I_{DS}), reverse conduction characteristics (I_{DS} vs. V_{DS}), and junction capacitance characteristics ([C_{ISS}; C_{OSS}; C_{RSS}] vs. V_{DS})). In addition, internal device package parasitic inductances and internal gate resistance were also included in the model (based on one of the models provided by the manufacturer). By considering all of these parameters, it was possible to develop a high-level transistor model that accurately represents actual operating conditions - Fig.3.9. A full model of the transistor in MAST language is included in Appendix B.

The next step is to create a complete schematic of the simulation circuit. For that purpose transistor model is inserted. The next step is the import of the PCB layout model - the SPICE model generated by ANSYS Q3D must be translated into the MAST language of the Saber simulator. This is achieved using its internal conversion tool. The schematic is then completed with small-signal models of the input, decoupling and output capacitors, the output inductor and the load resistor. Small-signal modeling means that the model of each device includes parasitic elements and reproduces the impedance changes of each device up to at least 100 MHz. The stray element values were previously measured with a Keysight E4990A impedance analyzer. The LISN network model is added to simulate the same condition as further EMC laboratory tests (the LISN model is presented in Appendix D). In addition, a control loop generating gating signals for transistors has been added to the schematic in order to simulate the proper operation of a half bridge inverter. The complete simulation schematic is shown in Appendix C. Examples of simulated voltage and current waveforms are shown in Fig. 3.11.

Results comparison

The results and considerations presented below concern the solutions discussed later in the thesis. A comparative simulation study of two circuits (shielded and unshielded inside the PCB Middle Point of the inverter leg), described in detail in Chapter 3.2, is presented here. The general simulation diagram is shown in Fig. 3.10 and the complete simulation diagram is shown in Appendix C. Here, the usefulness of simulation tools to determine the value of parasitics and their effect on the generated EMI is demonstrated, which greatly accelerates the research work. The example of two simulations shown below demonstrates the differences between them in terms of EMI generation, which can be the first step in selecting the correct layout.

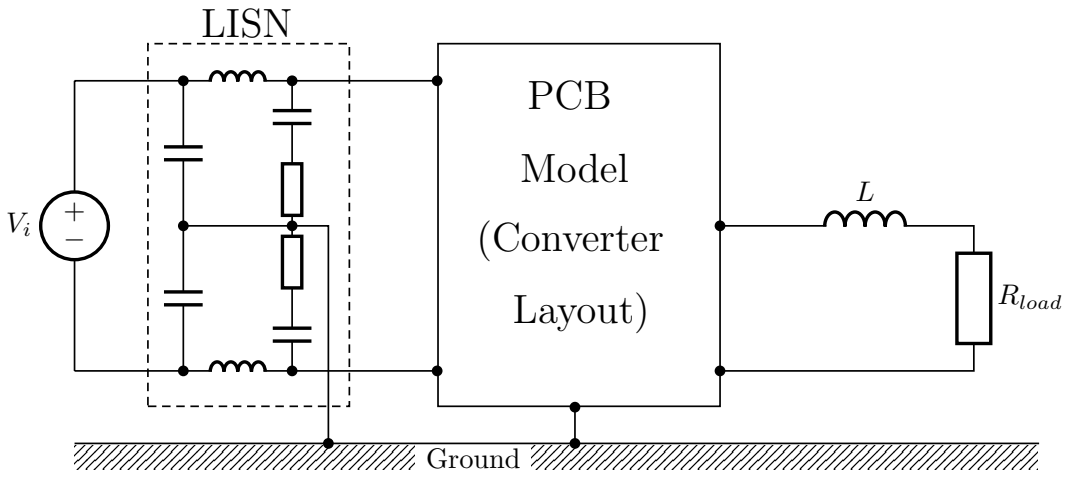
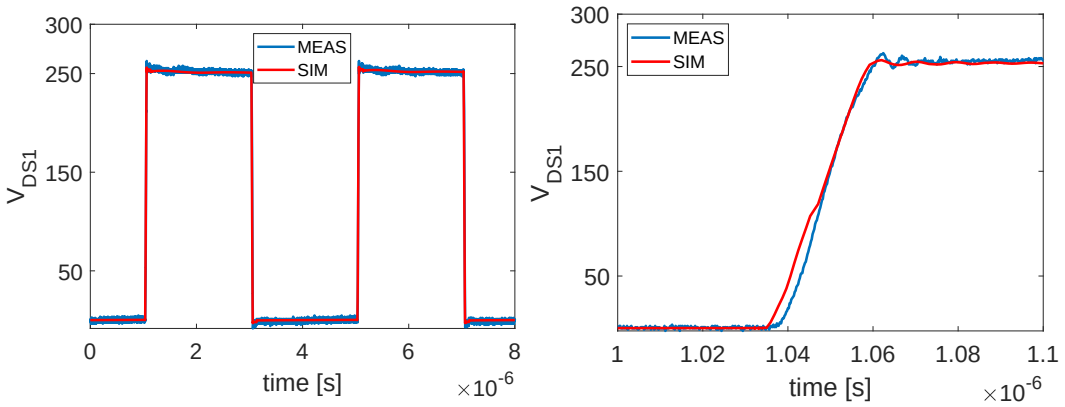


Figure 3.10: General simulation diagram

As mentioned above in previous subsections, the main purpose of simulation is to verify the concepts and their effectiveness in terms of EMC. Therefore, in order to study such relationships, simulation conditions must be as close as possible to the actual converter waveforms, reproducing, for example, the same voltage and current steepness. Fig. 3.11 shows a comparison of the drain-source voltage for the high-side T_1 transistor during operation as a half-bridge converter. The comparison between the voltage measured in the real system and the waveform obtained in the simulation is very consistent. The voltage levels are exactly the same, as well as the voltage steepness. The only noticeable differences are the beginning of voltage rise at the transistor and the smaller value of oscillation

amplitude after the transistor is turned off. However, these are differences in the order of a few volts, which is an outstanding result.



(a) (b)

Figure 3.11: Comparison of V_{DS} voltage of transistor T_1 obtained from simulation and measurement: (a) example of two switching periods, (b) zoom on the voltage slope during transient

The performed comparison of the generated CM disturbances obtained from the simulation with those collected experimentally is shown in Fig. 3.12. The two spectra differ, but this is normal since simulation does not reflect the full EMC environment. Thus, several dB of difference may exist. However, it is noteworthy the excellent agreement in terms of noise levels. The behavior in the low frequency (LF) range is also very similar. In the high frequency (HF) range, the influence of parasitic elements in the test bench is more prominent. In general, the results obtained can be considered reasonable and can be used as a basis for further considerations.

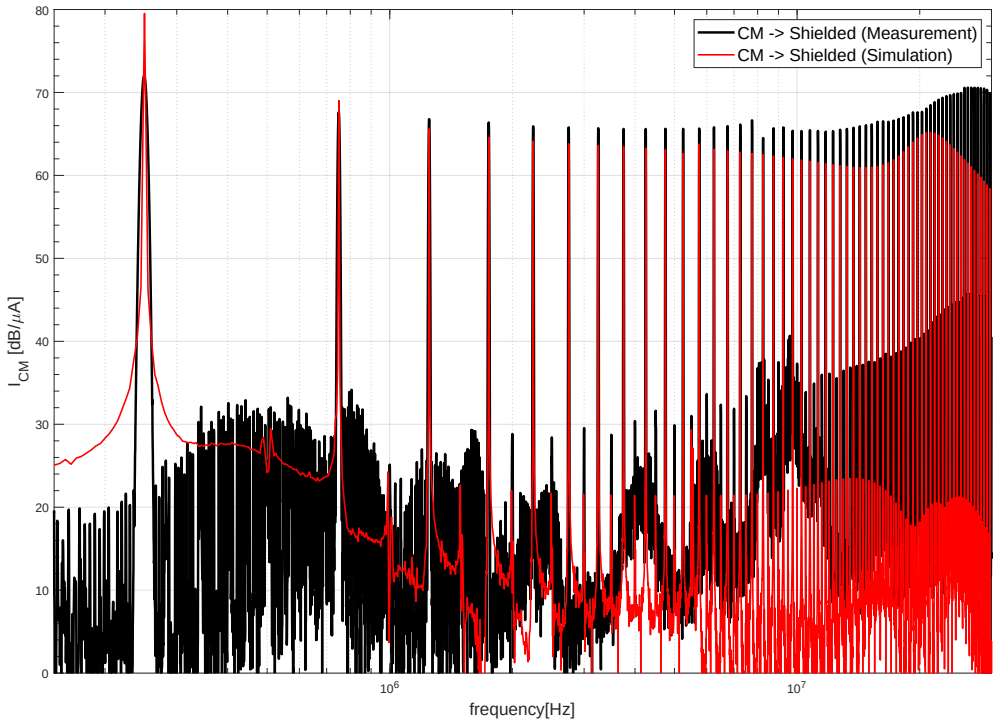


Figure 3.12: CM noise spectra obtained for PCB layout with shielded Middle Point Track - comparison of simulation and experimental results

However, the overarching goal of the presented simulation workflow is not to perfectly reproduce the experimental results in the simulation. Of course, one should be as close as possible, but some discrepancies are acceptable. The most important one is the fact of achieving the same efficiency in simulation and experiment for the considered treatments of changes in layout or control strategy. Thus, if we compare the simulation study of the shielding effectiveness for the middle point track (Fig. 3.13) with the same experimental study (presented later in Chapter 3.2.4, Fig. 3.38), the results are very consistent. The simulations show a reduction of about 6 dB in the HF and a very small reduction for the fundamental LF harmonic associated with the switching. Exactly the same reduction was found in the experimental study, and the differences in this comparative study between simulation and reality are 1-2 dB. Thus, the developed simulation workflow provides a very accurate tool for layout analysis and prediction of the generated conducted disturbances.

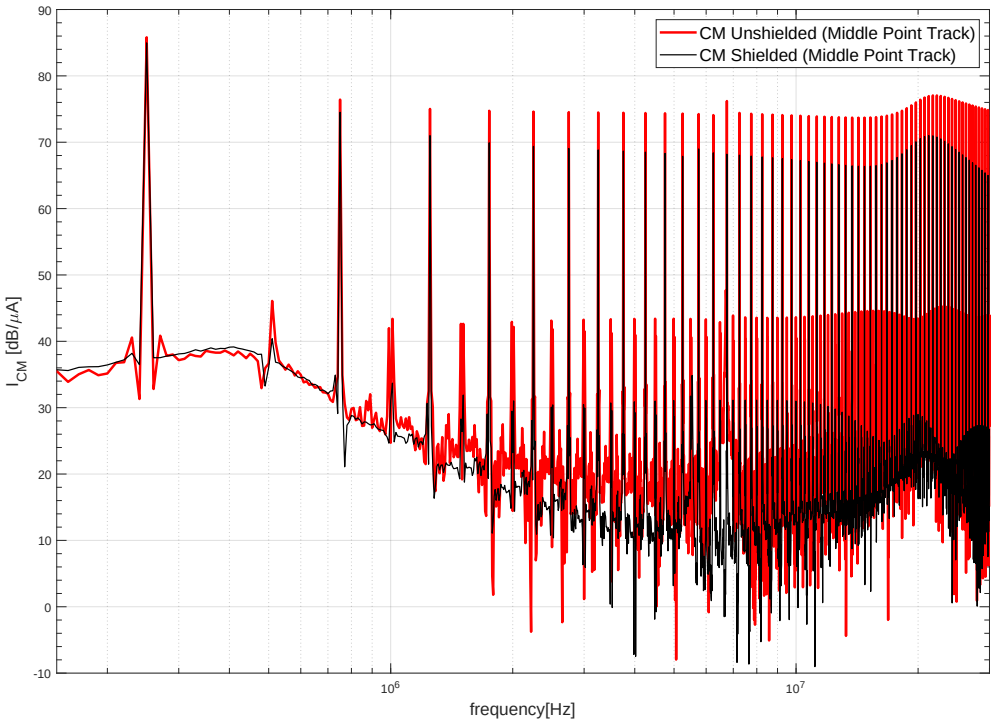


Figure 3.13: Shielding effectiveness for CM noise obtained in simulations

3.1.3 EMC environment

Simulation (as described in Chapter 3.1.2) is used to verify certain concepts, the effect of layout changes on EMC, etc., but the EMC environment around the converter is always assumed arbitrarily. In other words, conditions of the EMC environment are assumed in advance as an assumption or model of how it is interpreted by ourselves. However, in the real world, many different propagation paths and additive noise can exist (and have not been included in the simulation, e.g. due to lack of awareness of their existence). The laboratory environment is completely different from the simulation environment due to the presence of noise from the network, power supply, measurement equipment, etc. In fact, the above-mentioned sources of unwanted noise can affect the noise captured on LISN to falsify the measurement result. Thus, a prior simulation followed by laboratory measurements and their comparison leads to two effects. First, such a comparison is very important to carefully monitor the conditions of the experimental measurements, and any deviations are the basis for further discussion and search for sources of discrepancies. Second, experimental measurements lead

to a validation of the concept tested under simulation conditions.

A dedicated bench test has been designed to characterize the EMI inverter leg (Fig. 3.14). The converter is supplied from an external power source through a CISPR-16 compliant LISN (NNB-4/63TL). The CM and DM current is captured from the Spectrum Analyzer (Rohde & Schwarz ESRP EMI test receiver and spectrum analyzer) with a current probe (Tektronix P6021 60 MHz Bandwidth) including both plus and minus wires between the LISN and the converter input.

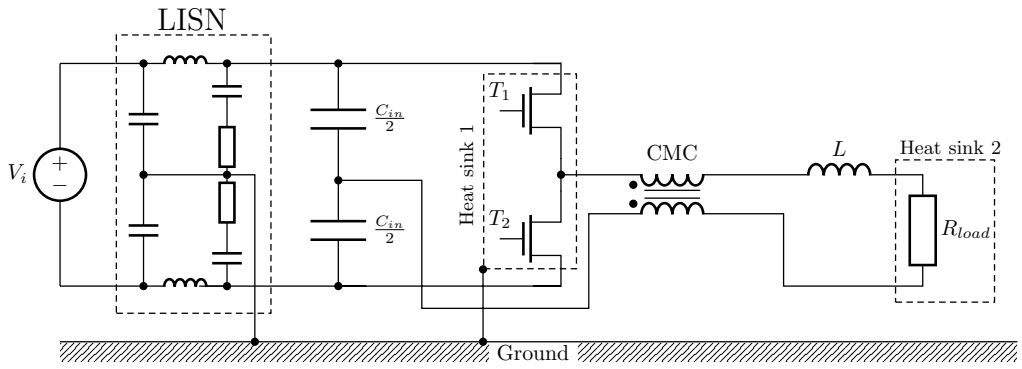


Figure 3.14: Test bench for EMI measurement

According to the diagram in Fig. 3.14 the first measurement station was built (Fig. 3.15). The results obtained from the measurements at this test bench did not coincide with the simulation results. So, special attention was paid to the design and organization of the EMI bench itself to find the explanation for the discrepancy in the results. A series of measurements with a variety of bench configurations made it possible to note the influence of certain factors. More specifically, power cables lying directly on the reference ground create additionally increased ground capacitance, which is one of the propagation paths of CM disturbances. In addition, for performing a comparative study (studying 2 different PCB layouts), it is necessary to replace the PCBs. Hence, there may be a change in the alignment of the wires with respect to each other and with respect to the reference ground, which alters the measurement conditions and introduces additional error affecting the result of the comparison of the two layouts. Another issue is the placement of power supplies on the bench. A slight (but non-negligible) effect of placing power supplies on and near the reference ground has been observed. In this case, parasitic capacitance is created between

the power supply chassis and the reference ground, and an additional path for disturbance propagation is created. These phenomena were noticed even though a LISN was used between the main power supply and the Equipment Under Test (EUT), and common mode filters between the auxiliary power supplies and the EUT.

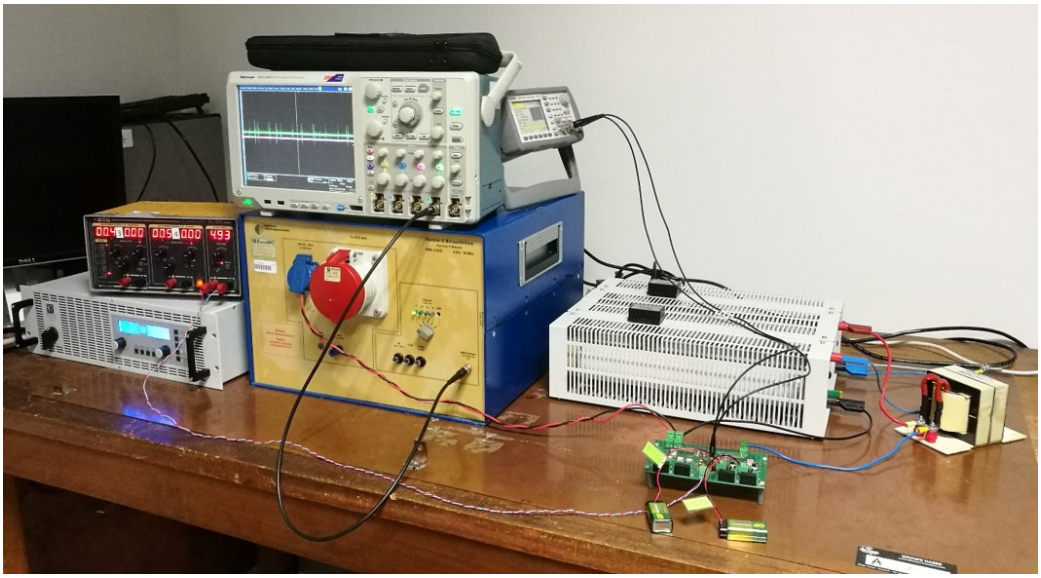


Figure 3.15: View of the first version of the EMI test bench

Finally, it was found that there is a huge impact of the load on captured disturbances of the entire converter. In the chosen test bench configuration, a RL load is used. The parasitic capacitances between the coil and the reference ground and between the resistor and the reference ground are crucial. By placing the load elements directly on the reference ground, the unwanted capacitances are significantly increased, which increases the CM current flowing through the load to LISN. The measured total CM noise seen on the LISN and the noise flowing only through the load are collected and shown in Fig. 3.16 Hence, special attention and solutions should be applied to the load used to minimize its effect on the disturbances seen.

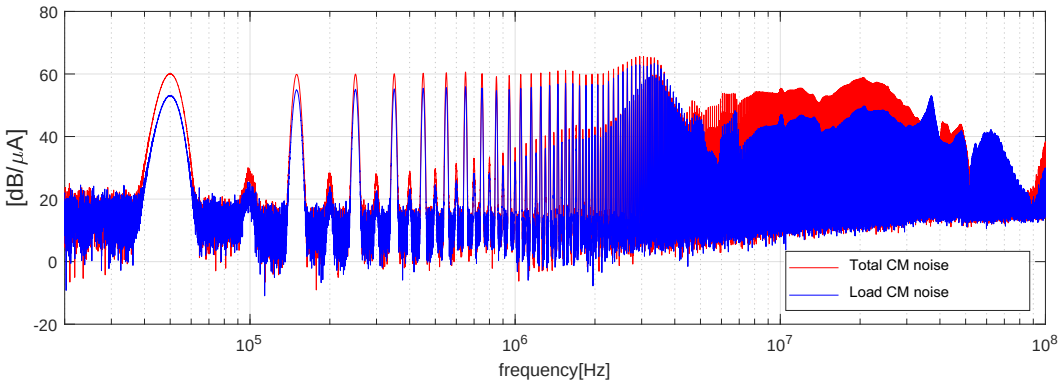
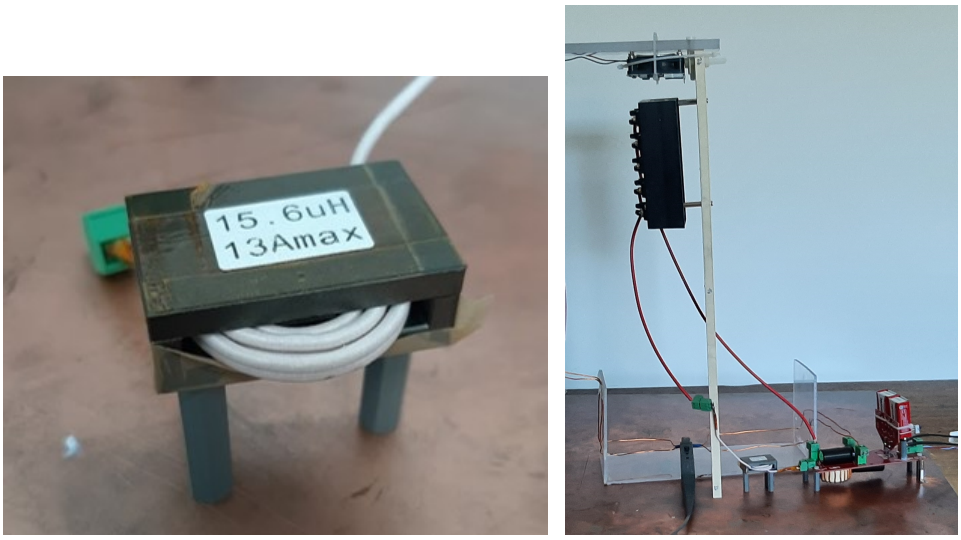


Figure 3.16: Measured CM noise at test bench from Fig. 3.15

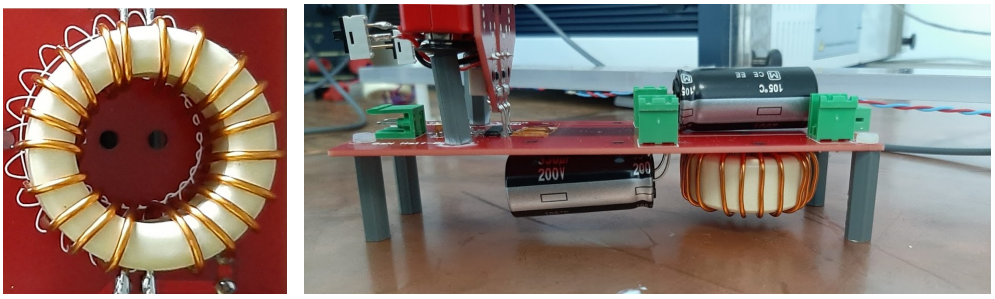
Two steps were taken to reduce the value of the load's parasitic capacitance. The inductor was redesigned to keep its geometric dimensions as small as possible and placed 2.5 cm above the reference ground (Fig. 3.17a). In addition, a load capable of dissipating at least 400 W was built on the basis of low-inductive resistors in a TO-247 package. The set of resistors was fixed on a heat sink and the whole set was mounted on a support about 40 cm above the reference ground (Fig. 3.17b). This procedure allowed the ground capacitance to be reduced to about 8-10 pF.



(a) (b)

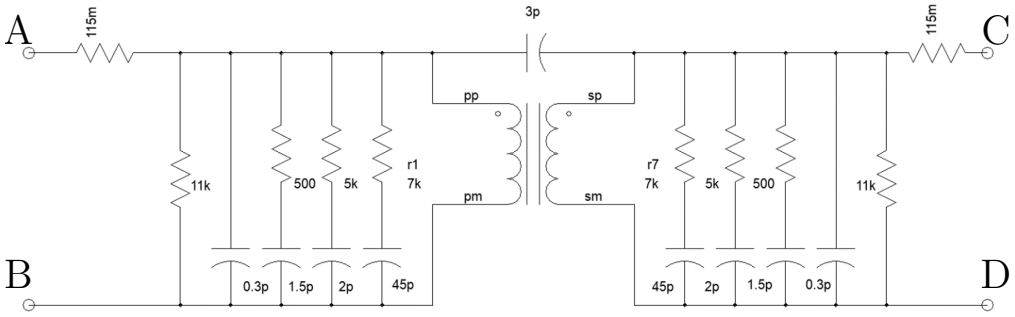
Figure 3.17: View of dedicated load for EMI test bench: (a) inductor, (b) entire load view with converter

To further reduce the CM current flowing through the load, a CM choke has been added. To cancel the CM propagation path through the load, this CM filter was placed between the center of the inverter leg and the load. The design of the filter was based on the 3E6 magnetic material (material optimized for use in wideband transformers as well as EMI-suppression filters). A view of the filter with its location inside the converter is shown in the Fig. 3.18. The CM and DM impedances were measured for the given filter. These impedances were used to develop an electrical model (Fig. 3.19) of CM Choke. The model is needed for the simulations. Using the model, a series of simulations were performed for the different layout types, which are also discussed in other subsections of this thesis.

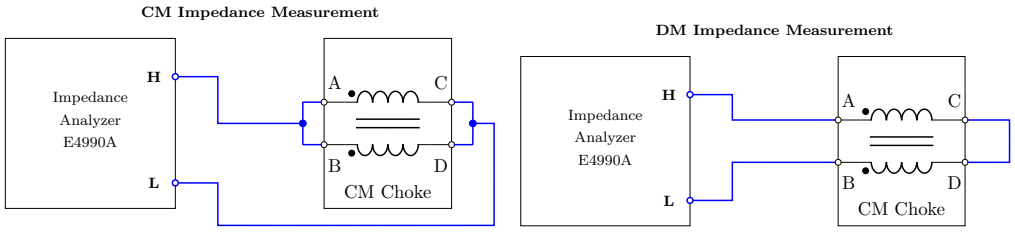


(a) (b)

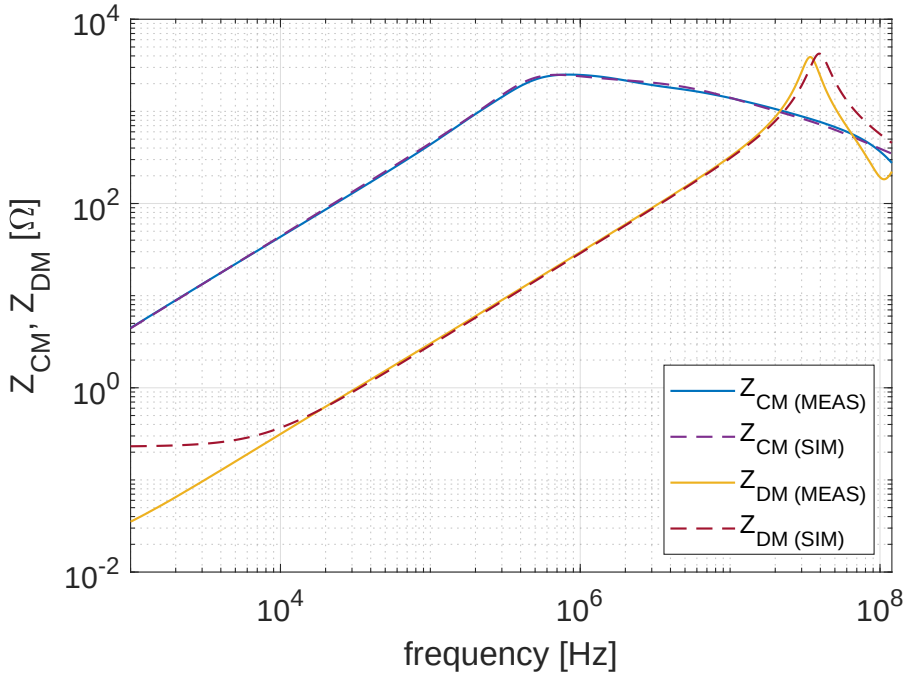
Figure 3.18: View of used CM Choke



(a)



(b) (c)



(d)

Figure 3.19: (a) Electrical model of CM Choke, (b) CM and DM impedance measurement setups, (c) Comparison of the model and real CM Choke impedances

To ensure fully reproducible and of good quality measurements, several precautions were introduced in the final version:

- Power and signal wires were mounted on dedicated stands with fixed position and distance to the ground (2.5 cm above the copper ground plane)
- All unnecessary equipment (auxiliary power supplies, signal generator, oscilloscope, etc.) were moved out of the table (far from the copper ground plane) to mitigate stray capacitances and to avoid unknown or unwanted CM paths (Fig. 3.22)
- The converter board and the output filter had fixed position and distance to the ground (2.5 cm above the copper ground plane - Fig. 3.22)
- A dedicated setup with wires and spot for the current probe was used between the LISN and the converter input to provide the same conditions and position of the measurement device (Fig. 3.20)

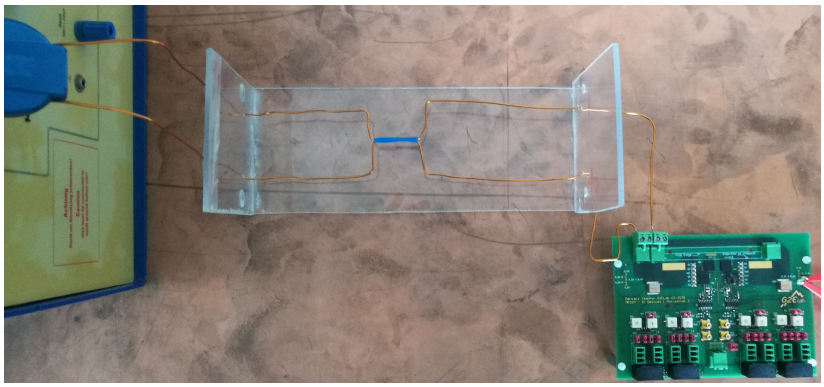
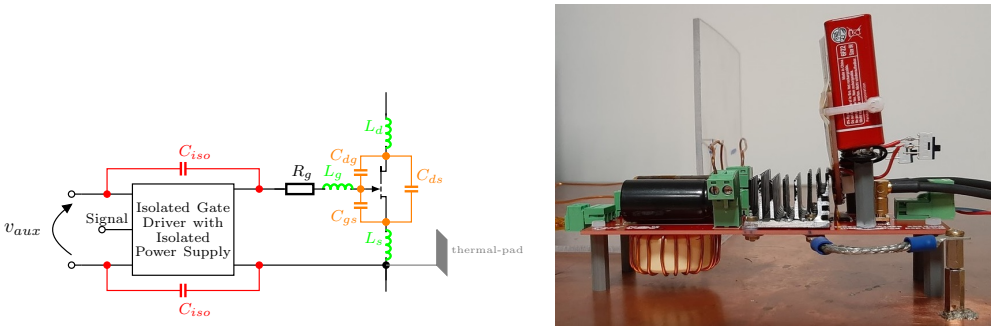


Figure 3.20: Dedicated setup for power wires between LISN and converter input. It keeps 2.5 cm distance of the power wires to the ground and provide comfortable connection of current probe at the constriction

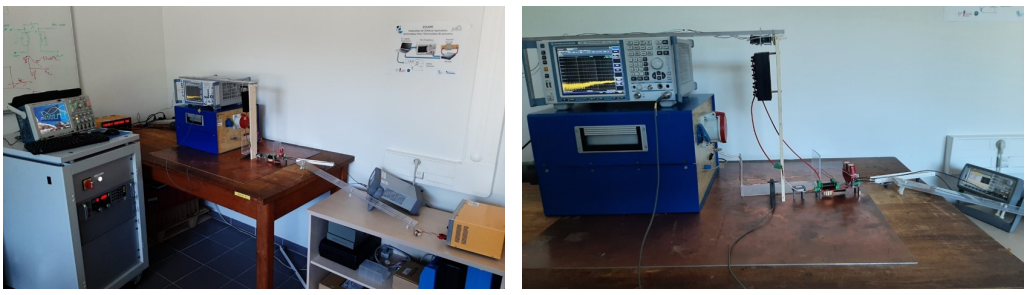
- In order to minimize disturbances in the gate circuits of GaN transistors, they were supplied from a 9 V battery. In this way, the propagation path from the gate circuits through $Ciso$ to the external power supply of the gate driver was strongly limited (Fig. 3.21a)



(a) (b)

Figure 3.21: 9 V batteries used for gate supplies: (a) Solution which eliminates the additional propagation CM path through *Ciso*, (b) Batteries arrangement inside of converter

- As previously mentioned, the resistive load was built from discrete parts in a TO-247 package mounted on the aluminum heat sink. This set is placed perpendicularly 40 cm above the ground plane to reduce stray CM capacitance of the load (Fig. 3.17)
- CM Choke was placed between the middle point of the inverter and the output inductor. Its aim was to significantly increase the CM impedance path through the load and therefore to prevent flowing of CM current in this direction (Fig. 3.18)



(a) (b)

Figure 3.22: View of the final version of the EMI test bench

All these precautions were necessary to be able to measure correctly the set up. They help to avoid unwanted CM path and also to focus on the effect of the PCB layout. The impact of the load stray capacitance and gate drivers stray capacitance finally have been smaller than the PCB stray capacitance.

3.2 EMI attenuation by shielding concept

This part presents the basic layout of the inverter branch in 2D arrangement (both transistors placed on the same side of the PCB, as well as the other components assembled in the classical way). In addition, the layout is extended with concept of internal shielding of the noisiest paths inside the PCB to reduce generation of CM currents.

3.2.1 Shielding principles

Fig. 3.23a illustrates the basic phenomenon involved in CM generation: the switching cell generates a high $\mathrm{d}v/\mathrm{d}t$ slope which excites the CM current flow through parasitic capacitance C_{cm}, due to natural existence of grounded elements such as metal enclosure, copper/aluminum heat sink, etc, nearby PCB tracks. The LISN is used to close the CM current circulation path and to provide stable input impedance. This action can be represented by a simplified model (Fig. 3.23b) using the voltage source V_{DS}, and the LISN impedance $Z_{LISN}/2$ in CM to close the loop. Using a conductive shielding foil between the floating point of switching leg and the ground (Fig. 3.24) changes distribution of stray capacitances, as illustrated in Fig. 3.23c. Three capacitances can be distinguished: C_{cm1}, C_{cm2}, C_{cm3}. The capacitances C_{cm1} & C_{cm2} come from the capacitive divider and depend on the distance between the shield-ground and shield-track nodes. Their series association is equal to the initial capacitance C_{cm} of the unshielded case. The parasitic capacitance C_{cm3} represents the remaining capacitance between the floating point and the ground, which is not exactly equal to zero, due to misalignment of the shield (e.g when the shield area does not fully cover of the track) and some edge effects. In the case of perfect alignment of shield and middle point areas the capacitance C_{cm3} can be neglected [27].

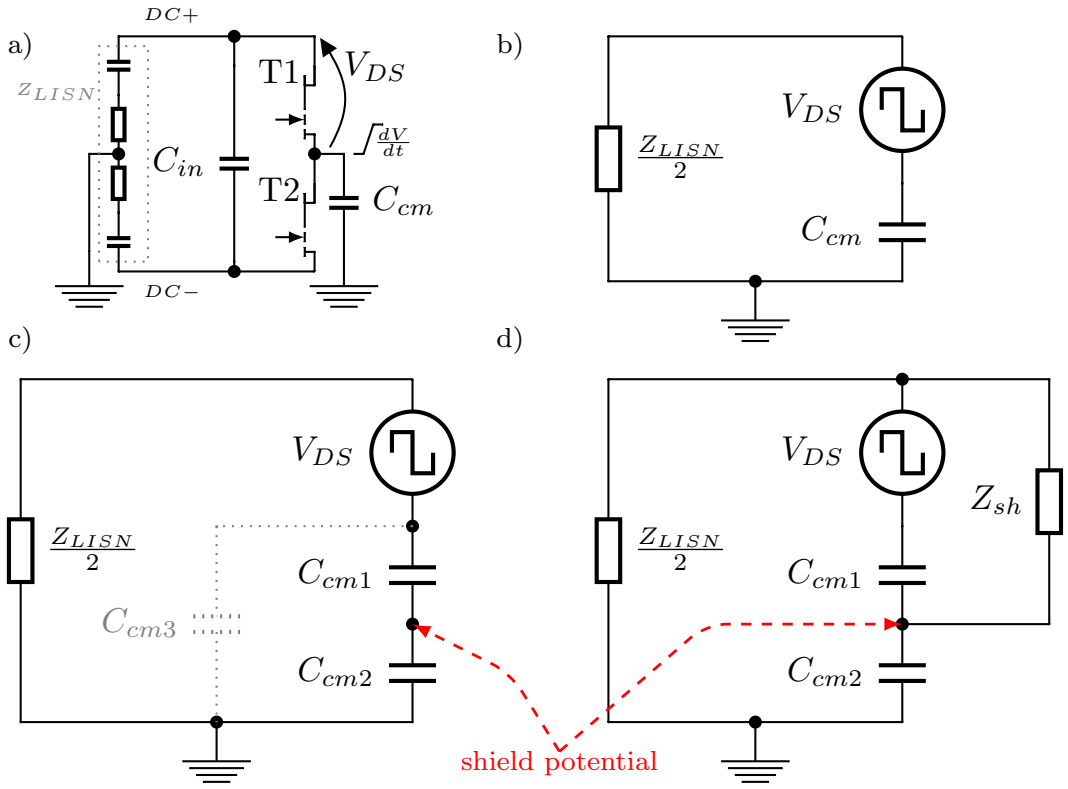


Figure 3.23: Lumped CM models of PCB track shielding: a) generic circuit of inverter leg; b) unshielded; c) conductive shielded plane floating, d) conductive shielded plane with bus-bar connection

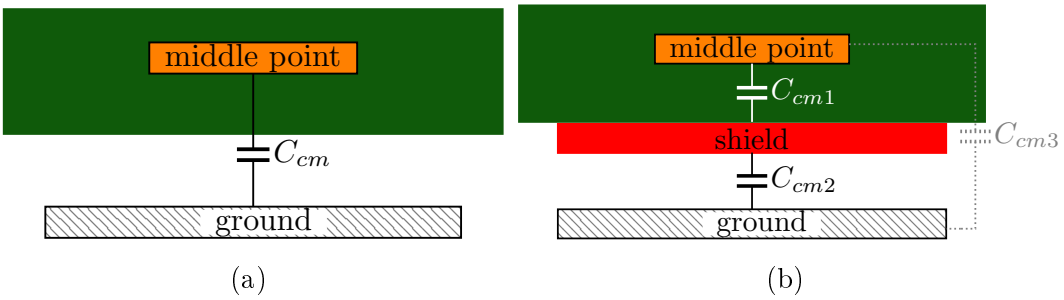


Figure 3.24: Geometrical presentation of the PCB middle point track with stray capacitances: a) unshielded; b) shielded

Hence, the use of the shield according to Fig. 3.23c will not be effective if there is no connection of the shield potential to other potentials of PCB tracks (due to no alternative path for the CM current). In [8] the authors have introduced this type of shield along a wide area of PCB as results of which alternative paths have been created through stray capacitances of other tracks. However, this approach provides paths with high impedance, which results in poor effectiveness of the

shield, except for very high frequency. Based on these considerations, a shield is proposed as a low conductive plane impedance (Z_{sh}) connected to the stable potential - positive bus-bar track of the converter (Fig. 3.23d).

In the idealized circuit of Fig. 3.23d, the CM current I_{cm} splits into two branches: one flowing through C_{cm2} and the ground to LISN, and the other circulating through the inserted shielding (Z_{sh}). The ratio between these two currents corresponds to the impedance ratio of two branches. The simulation of circuits in Fig. 3.23b and Fig. 3.23d was performed using Saber@Sketch simulator to compare the LISN CM current spectra without shielding and with shielding for two values of shielding impedance 1Ω (4% of $Z_{LISN}/2$) and 0.1 Ω (0.4% of $Z_{LISN}/2$), where $Z_{LISN}/2$ for CM was equal to 25 Ω. The V_{DS} waveform of voltage was trapezoidal with 20 V/ns slope corresponding to the experimental dv/dt, see Fig. 3.29. Performed simulation results (Fig. 3.25) confirm significant CM noise mitigation, up to 70 dB, for the low impedance conductive shielding plane.

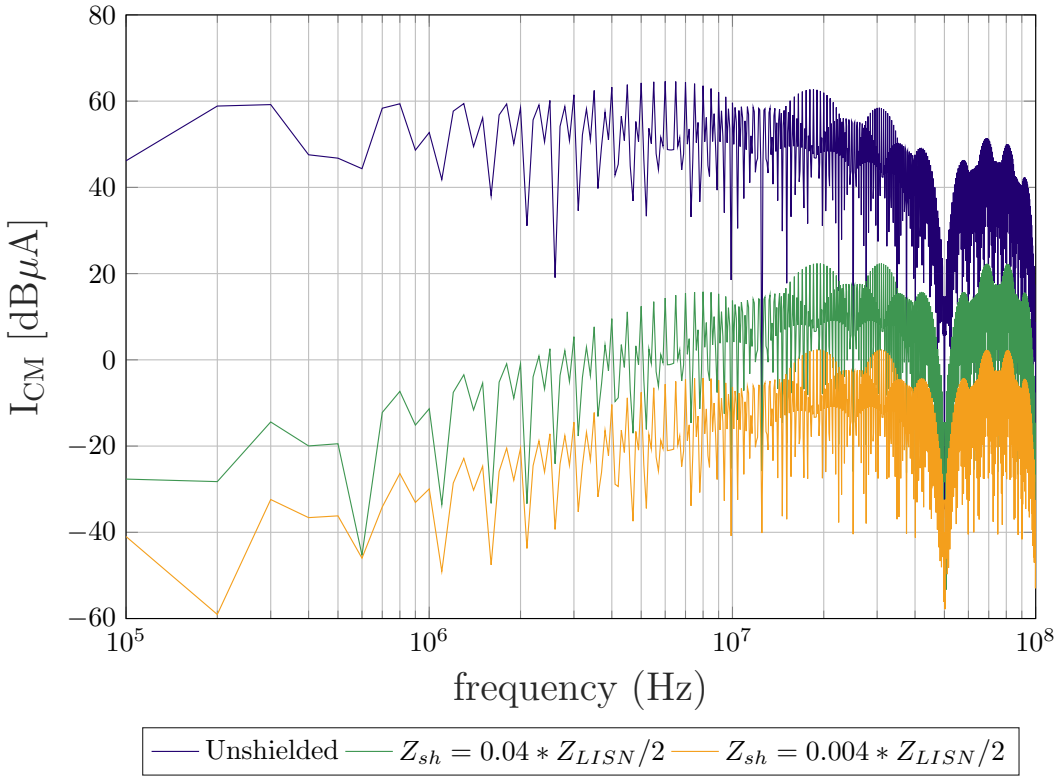


Figure 3.25: CM current spectra for different shielding conditions: unshielded referring to Fig. 3.23b, and two Z_{sh} values referring to Fig. 3.23d

This section has illustrated the basic shielding principle of CM current, with the shield being connected to a stable potential with low impedance, to facilitate internal recirculation of the CM current. The following section will describe the GaN switching cell to which the above concept was applied.

3.2.2 2D Demonstrator and system description

2D PCB layout design

The converter (inverter) demonstrator was designed using a four-layer PCB. It is composed of: positive (DC+) and negative (DC-) power bus-bars, two series-connected electrolytic capacitors $C_{in}/2$, T1-T2 inverter leg, decoupling capacitors C_{decoup}, and CM filter choke L_{CMC}.
The enhancement mode GaN power transistors (GS66506T from GaN Systems) T1 and T2 are used in the inverter leg. Since GaN HEMT transistors have reverse conduction capability, the synchronous operation of the inverter leg is obtained without freewheeling diodes. The transistors are top-side cooled: they possess thermal pads internally connected with the source terminal and substrate (Fig. 3.26). A planar 2D placement of power switches [28] has been chosen where both transistors are soldered at the top of the PCB. Owing to top-side cooling devices, heat dissipation is easily realized by the heat sink mounted directly on both devices. In further consideration, the heat sink potential is assumed as the ground. Its location is crucial for CM noise generation. In detail, the source potential of the high-side switch (T1) is connected to its thermal pad located close to the grounded heat sink. It increases the total CM stray capacitance C_{cm} of the inverter middle point.

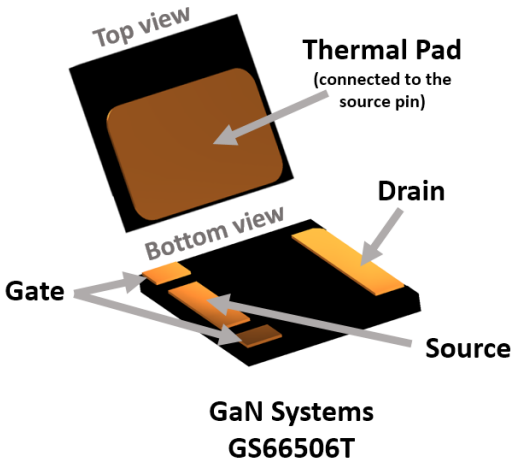
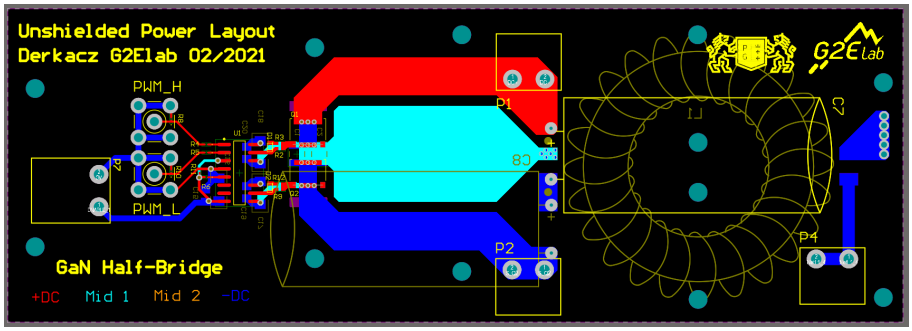


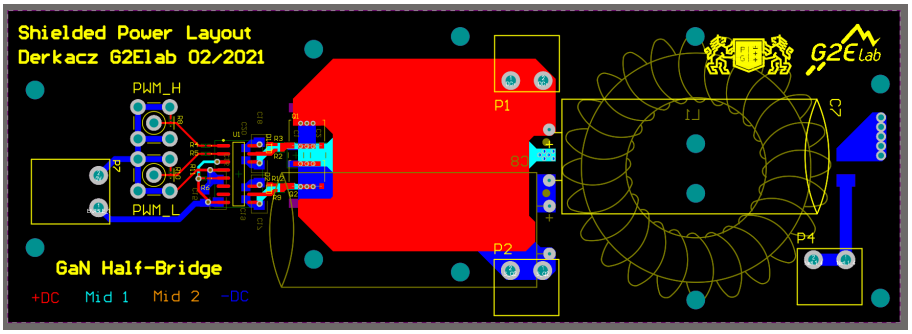
Figure 3.26: Description of GaN package [28]

To reduce the power loop, decoupling capacitors have been placed directly beneath the transistors, on the bottom side of the PCB. Also, the layout of the DC+ and DC- tracks (bus-bars) has been designed such as to provide a symmetrical and as-short-as-possible power loop (Fig. 3.27). Close to the transistor gate terminals is placed a half-bridge driver with two isolated channels for top and bottom transistor control. The gate circuit consists of two branches with resistors R_{on} & R_{off} and diode D_{off} to separately tune the speed of transients. The isolated secondary sides of the driver are supplied from a separate PCB, mounted perpendicular to the main board to reduce the impact of parasitic capacitances of the power supply circuit on CM current generation. Particular consideration has been taken to the layout of the inverter middle point track, which is exposed to rapid voltage transitions during inverter operation. The layout of this track was designed using the two middle layers of PCB (Yellow & Cyan layers in Fig. 7) with the same tracks' geometry connected by vias to increase the current capability of the converter. The size of this track was intentionally increased to obtain the values of track stray capacitances comparable with the capacitance between the GaN transistor thermal pad and the ground (Fig. 3.27).

a)



b)



c)

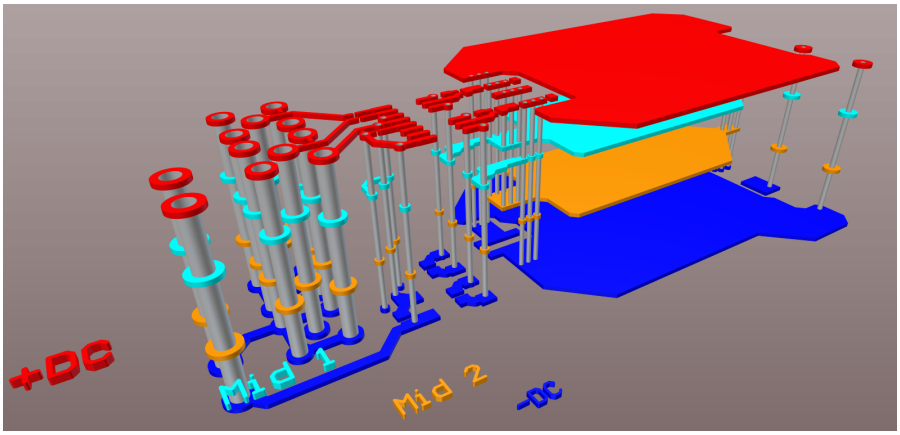


Figure 3.27: View of the demonstrator with middle track: a) unshielded, b) shielded, c) exploded 3D view of shielded PCB: sandwich between DC+, middle point and DC-, (thickness of the board in scale 10:1) (colors: Red - Top Layer, Blue - Bottom Layer, Yellow&Cyan - Middle Layers)

Half-bridge inverter description

A half-bridge inverter leg (Fig. 3.28) is used to investigate CM stray capacitances and the impact of shielding techniques on modification of CM current paths. The inverter is fed from a DC voltage source (V_i=250 V) through the LISN. Two input capacitors $C_{in}/2$ split the DC link voltage V_i to create a 0 V midpoint connection for the load. The inverter feeds the resistive load R_{load} via an inductive output filter L=15 µH. As has been mentioned earlier, to attenuate CM current circulation path through the load circuit, a CM filter choke L_{CMC}=705 µH with coupling factor k=0.99675 and differential inductance of 3.4 µH is installed between the inverter output terminals and the filter.

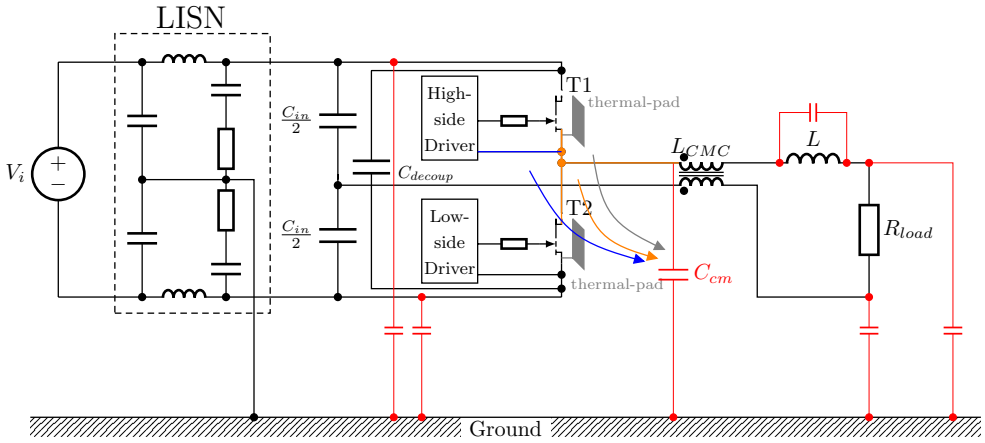


Figure 3.28: Half-bridge inverter in the laboratory setup with stray capacitances location (C_{cm} contribution of 3 factors is described later in this Chapter 3.2)

The inverter is switched at 250 kHz. The global waveforms of load voltage and current are depicted in Fig. 3.29. Due to the resistive-inductive load, all four consecutive conduction states of the half-bridge inverter at rectangular voltage operation mode are obtained. The zoom of the voltage waveform at turn off in Fig. 3.29 shows a reduced voltage overshoot, which validates the inverter circuit design layout by minimizing the stray inductance.

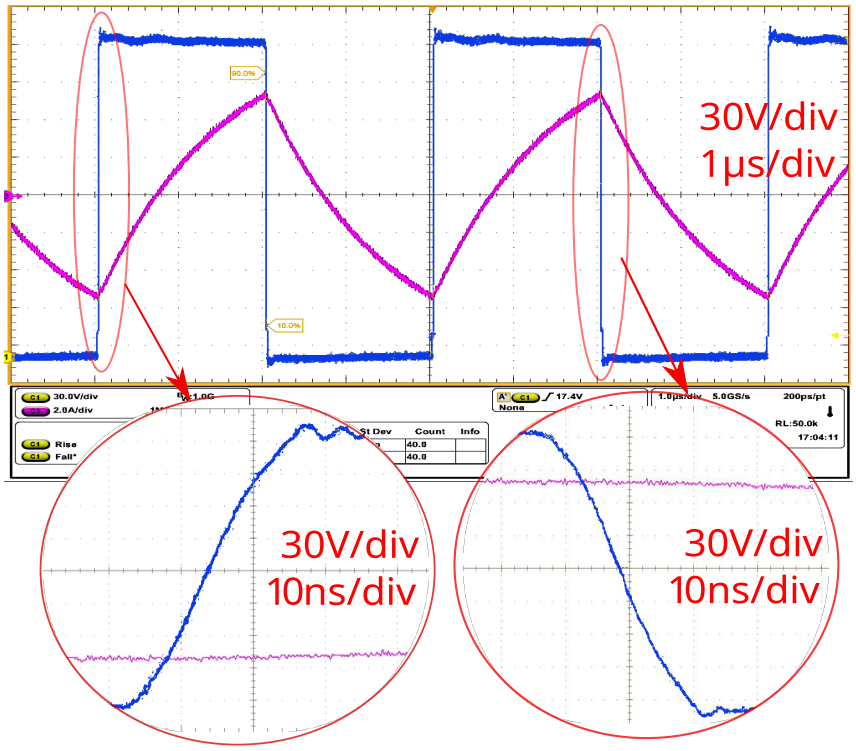


Figure 3.29: Inverter voltage and current waveforms

3.2.3 Shielding of The Three Main CM Capacitance Contributors

Common mode noise generation in inverters is mainly related to the existence of parasitic capacitance between the inverter leg midpoint and the ground. A systematic experimental study of a half- bridge inverter leg based on the lateral GaN HEMT structure has indicated three main contributors of CM capacitance: middle point PCB track to ground, thermal pad of the top switch (T1) to ground, gate circuit of the top switch (T1) to ground (Fig. 3.30). All these three parts are connected to the point with high $\mathrm{d}v/\mathrm{d}t$, and each of them increases the area of this point (by copper tracks), thus resulting in the increased stray capacitance to ground. The application of shielding techniques, as described in details in next paragraphs, provides new paths for the CM current to recirculate inside the converter (Fig. 3.31), which leads to the reduction of CM noise.

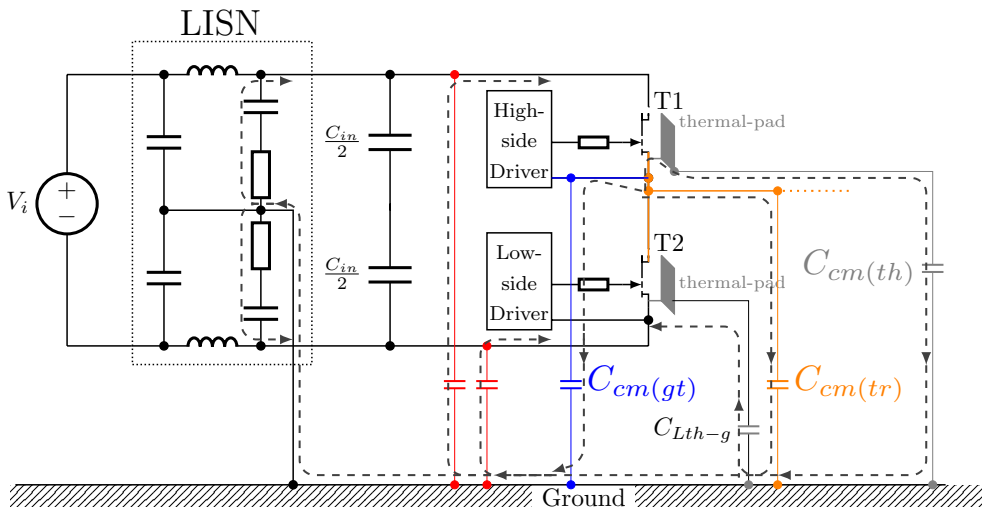


Figure 3.30: CM stray capacitances and current circulation paths of the unshielded converter

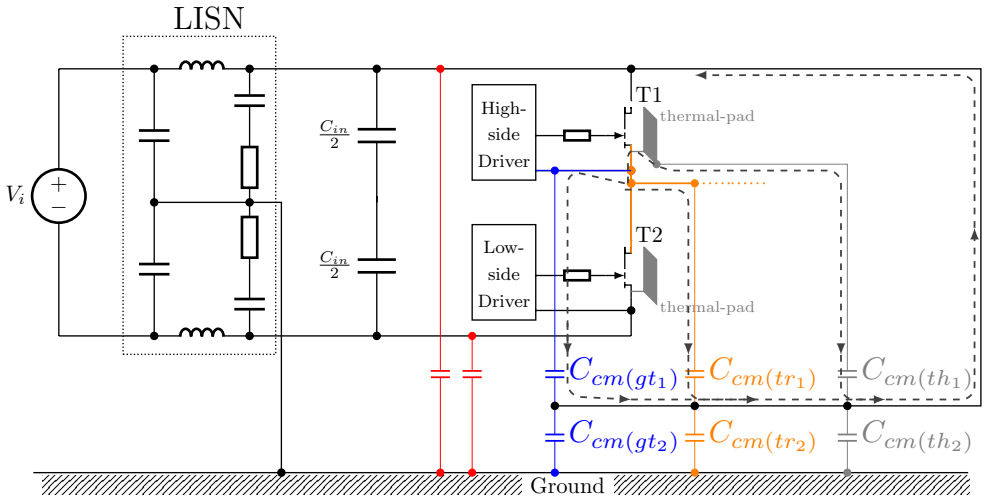


Figure 3.31: CM stray capacitances and CM current paths (recirculation) for shielded converter (shielded: middle point track, thermal pad, gate supply circuit)

Inverter middle track shielding

The middle point track (power part) shielding by conductive local plane is realized by extending the surface of the DC+ and DC- bus-bars planes. These planes are acting as a shield, as referred to in Chapter 3.2.1, and overlapping the middle point track in 92.55% of the area for shielded layout (Fig. 3.27b). For comparison, only 2.14% of the middle point area is overlapped for unshielded layout (Fig. 3.27a). For the unshielded version shown in Fig. 3.32a the CM

current flows mainly through the capacitance between the middle track and the heat sink. The capacitance C_{cm} [7.2 pF] (as in Fig. 3.24) is approximately equal to $C'_{m\leftrightarrow h}$ [5.8 pF] (Fig. 3.32a), since the capacitances $C'_{m\leftrightarrow DC+}$ [1.09 pF] and $C'_{m\leftrightarrow DC-}$ [0.9 pF] between the middle track and DC+ and between the middle track and DC-, respectively, are relatively small (Table 3.1). It is noteworthy that in the unshielded version, the capacitance $C'_{DC+\leftrightarrow h}$ [3.7 pF] between DC+ and heat sink has a significant value, but it is series connected with small $C'_{m\leftrightarrow DC+}$ [1.09 pF], and therefore can be neglected as a component of capacitance C_{cm}. Additionally, this capacitance is not connected to a floating point but to a stable potential. Therefore, it does not contribute to CM generation, but rather to CM internal recycling.

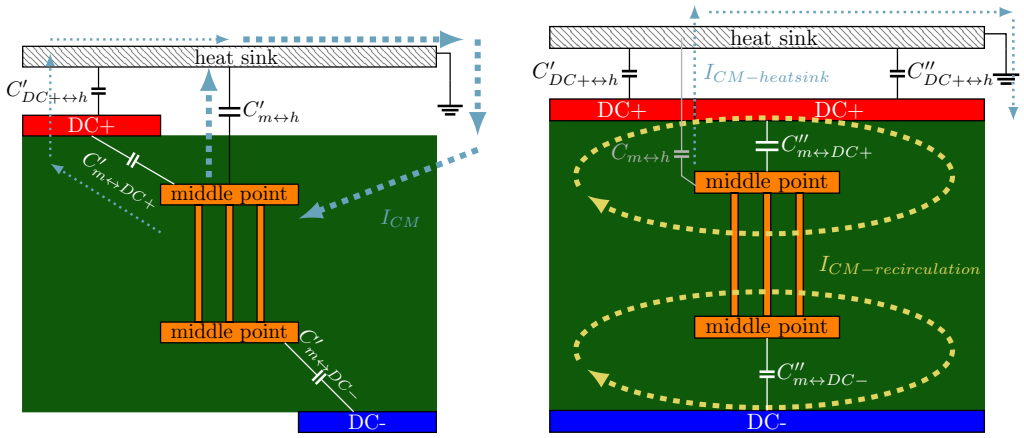


Figure 3.32: Stray capacitance distribution in the PCB cross-section a) unshielded, b) shielded middle track

When shielding is applied, the extended surfaces of DC+ and DC- bus-bars (Fig. 3.32b) increase the capacitances between the bus-bars and the middle track, which affects the switching speed (as described later in Chapter 3.2.4). The capacitance $C'_{DC+\leftrightarrow h}$ [3.7 pF] between DC+ and the heat sink is increased by the parallel-connected capacitance $C''_{DC+\leftrightarrow h}$ [10.3 pF]. The CM current I_{cm} flows through the capacitance $C''_{m\leftrightarrow DC+}$ [33.7 pF]. At the DC+ node, I_{cm} splits in two parts: the - first component recirculates within the switching cell through low impedance of the shield and the DC+ tracks, while the - second component flows through capacitance $C'_{DC+\leftrightarrow h}$ [3.7 pF] + $C''_{DC+\leftrightarrow h}$ [10.3 pF] to the heat sink. Since the value of $C''_{m\leftrightarrow DC+}$ [33.7 pF] is much larger than that of $C'_{DC+\leftrightarrow h}$

[3.7 pF] + C"$_{DC+\leftrightarrow h}$ [10.3 pF], a proportionally smaller current flows to the heat sink. Most of the I_{cm} current recirculates inside the switching cell according to Equation (3.3) (with a given value of C"$_{DC+\leftrightarrow h}$ [10.3 pF] and the assumption that Z_{sh}=0.1 Ω @1 MHz):

@150 kHz, $I_{cm\text{-}heatsink}$= 0.00000097·$I_{cm\text{-}recirculation}$,

@30 MHz $I_{cm\text{-}heatsink}$= 0.00019·$I_{cm\text{-}recirculation}$.

$$\frac{I_{cm-heatsink}}{I_{cm-recirculation}} = \frac{Z_{sh}}{\frac{Z_{LISN}}{2} + j\omega C''_{DC+\leftrightarrow h}} \tag{3.3}$$

It is clear that C"$_{m\leftrightarrow h}$ [0.56 pF] capacitance is still present in the circuit due to the inability of 100% shield the middle point track (due to constraints: transistor package, clearance and creepage related to maximum voltage, etc.). However, simulation studies show that the value of C_{cm} for the shielded case equals 0.68 pF, indicating a more than 10 times reduction in C_{cm} capacitance compared to the unshielded layout.

Table 3.1: Stray capacitance values for unshielded and shielded middle point track

Capacitance	**Value [pF]**
Unshielded (Fig. 3.32a)	
C'$_{m\leftrightarrow h}$	5.8
C'$_{DC+\leftrightarrow h}$	3.7
C'$_{m\leftrightarrow DC+}$	1.09
C'$_{m\leftrightarrow DC-}$	0.9
Shielded (Fig. 3.32b)	
C"$_{m\leftrightarrow h}$	0.56
C"$_{DC+\leftrightarrow h}$	10.3
C"$_{m\leftrightarrow DC+}$	33.7
C"$_{m\leftrightarrow DC-}$	33.6

GaN thermal pad shielding – lab solution

The next step of recirculating the I_{cm} current in internal path is mounting the shielding layer between the thermal pad and the heat sink (Fig. 3.33). This approach is a further extension of middle point shielding. However, its practical realization in this study had to be adapted to laboratory conditions. A copper foil was used as a conductive shield connected to the constant potential DC+. The isolation between the thermal pad and the shield, and between the shield and the heat sink was made using a Kapton insulator, as presented in Fig. 3.34. It ensured capacitive coupling between the transistors' thermal pads (source connected) and the DC+ bus-bar, which resulted in increasing the total C_{cm} capacitance but also in providing an additional path for CM recirculation (as described in the previous paragraph) The application of thermal pad shielding to the lower switch (T2) created an additional stray capacitance C_{Lth-g} (Fig. 3.30) which increased the total DC- to ground stray capacitance and helped in CM current recirculation inside the GaN power inverter leg.

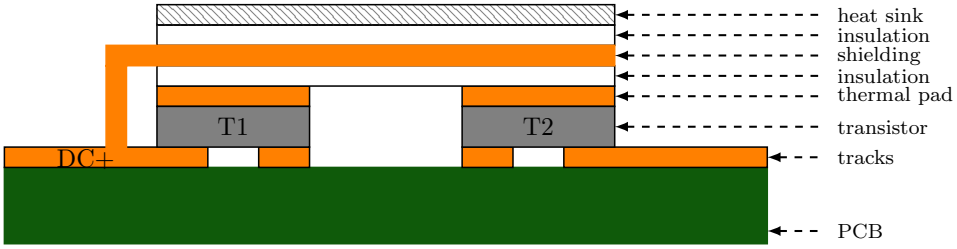
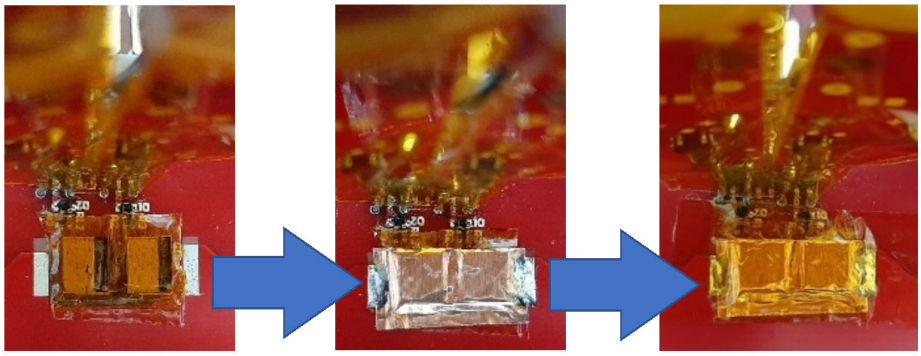


Figure 3.33: Thermal pad shield cross view

The thermal pad shielding requires two layers of insulation. It doubles the thermal resistance from the case to the heat sink ($R_{th(c-h)}$), which is one of the disadvantages of this CM suppression method. The use of Kapton as insulation and thermal interface material, is sufficient to verify the effectiveness of the thermal pad shielding. However, it does not present a commercial solution. The impact of doubling Kapton can be minimized in the designing step by the appliance of other materials. These constrains should be taken into account in the designing process and global optimization of the converter to achieve the trade-off between CM current emission, power switching losses and thermal performance [91].

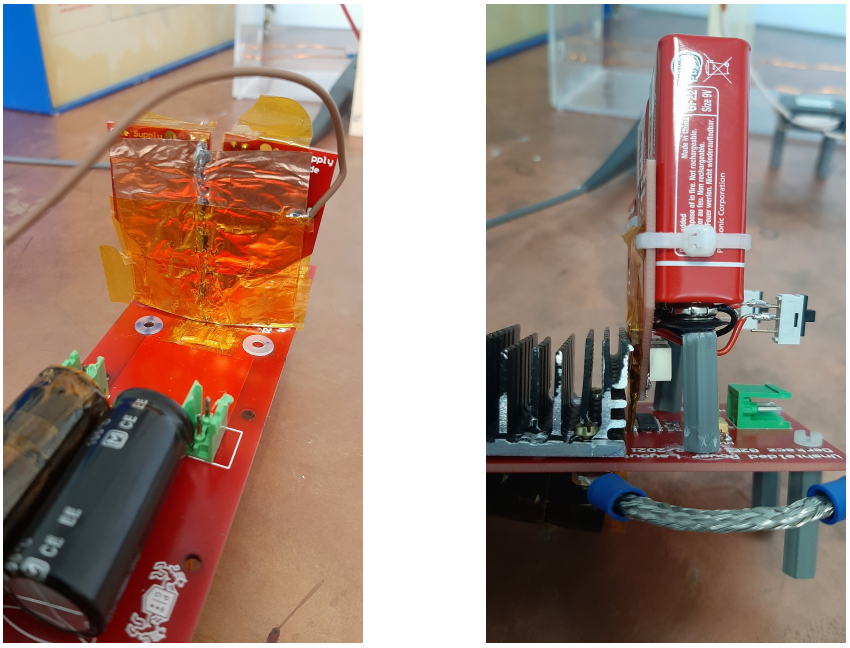


(a) (b) (c)

Figure 3.34: Stages of thermal pad shield application: a) placing 1st insulation layer on thermal pad of GaN package, b) applying copper foil shield and soldering it to the bus-bar, c) placing 2nd insulation layer between shield and grounded heat sink

Shielding of Power Supply Boards for Gate Drivers

The isolated secondary sides of the gate driver are supplied from dedicated PCB boards. On these boards, 9 V batteries with voltage conditioning circuits are used as the voltage sources for each channel of the dual channel gate driver. To minimize CM capacitance of these circuits to the reference ground plane, the boards are mounted perpendicularly to the main board (Fig. 3.35b). However, a grounded heat sink is still placed in the nearby of these boards, which increases the CM capacitance. As in the previous case, shielding can also be applied to this part of the converter. In laboratory conditions, similarly to the thermal pad, Kapton insulation and copper foil were used to create the shield, which was by short wire connected to the DC+ potential (Fig. 3.35a).



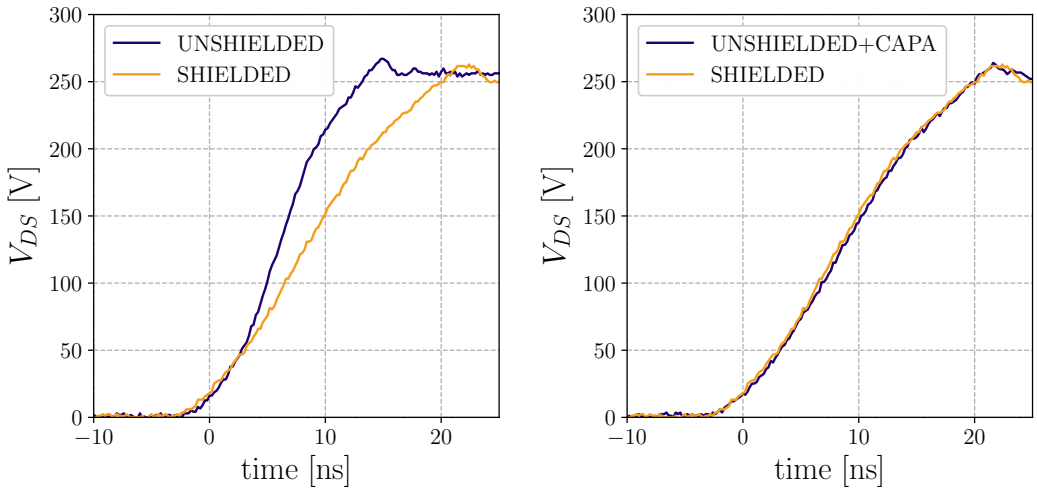
(a) (b)

Figure 3.35: Gate driver power supply boards: a) view with applied shielding, b) perpendicular installation of supply boards in the converter

3.2.4 Experimental Results

Impact of individual shielding

The laboratory measurement of I_{cm} current was performed in four steps for progressive shielding application variants. The first variant represented the middle point track shielding being the result of introduction of additional parasitic capacitance parallel to the transistor internal capacitance C_{DS} which changed the rising time of V_{DS} (Fig. 3.36a). To check the effectiveness of shielding, an additional capacitor $C = 80\,pF$ was installed in the unshielded PCB between the drain and source transistors' nodes to get the voltage slopes the same in both cases, as presented in Fig. 3.36b. The I_{cm} spectra of unshielded PCB with additional capacitor and the PCB with unshielded middle point are compared in Fig. 3.37. Slight differences are noticed in the spectrum for frequencies above 15 MHz. Then, a significant difference is observed above 20 MHz, which depicts the impact of slope reduction on I_{cm} generation. Adding $80\,pF$ to the (unshielded) reference case allowed having the same dv/dt for comparison.



(a) (b)

Figure 3.36: Comparison of V_{DS} slopes: a) PCB with shielded (orange) and unshielded (blue) middle point; b) PCB with shielded (orange) middle point and unshielded with additional lumped capacitors C=80 pF (blue)

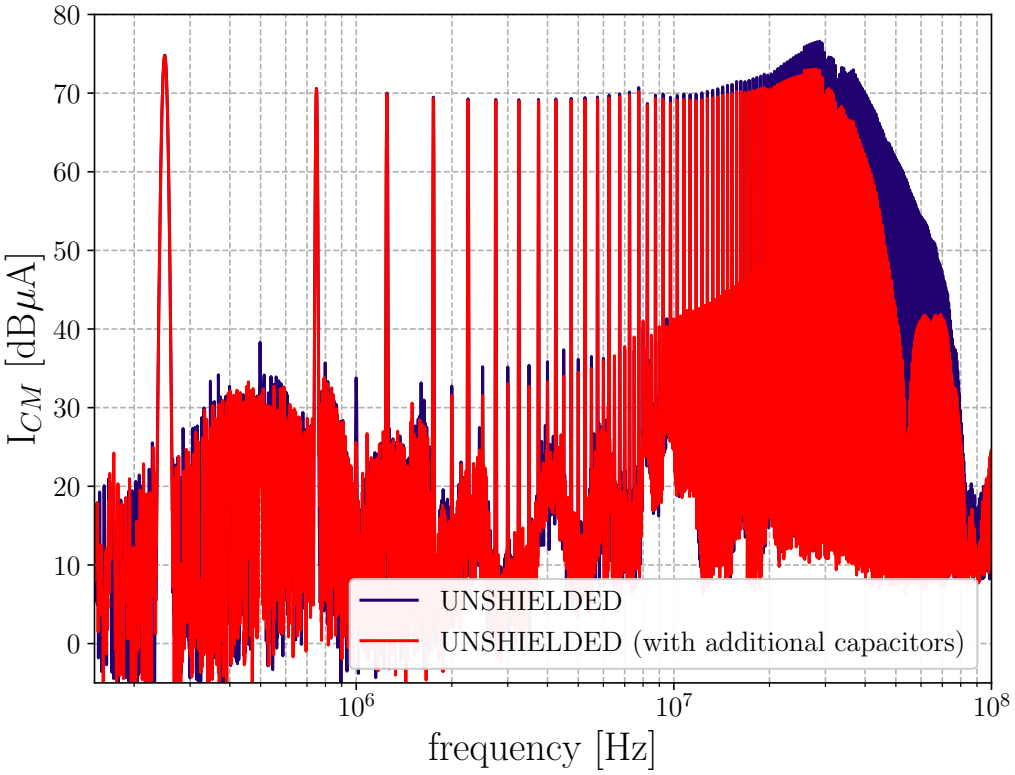


Figure 3.37: CM current emissions of unshielded middle point and unshielded with additional lumped capacitors

The I_{cm} spectra for the unshielded PCB and with the shielded middle point track are compared in Fig. 3.38. It can be noticed that for PCB with shielded middle point track, the basic harmonic and its subharmonics are reduced by about 2-3 dB, while for frequencies above 10 MHz, this reduction reaches 5.5 dB. Comparing these results with Fig. 3.37 proves that the reduction of I_{cm} emission in the frequency range up to 20 MHz is caused by shielding the middle point track (and not due to dv/dt reduction, as the dv/dt values have been equalized with the $80\,pF$ capacitance in the unshielded case).

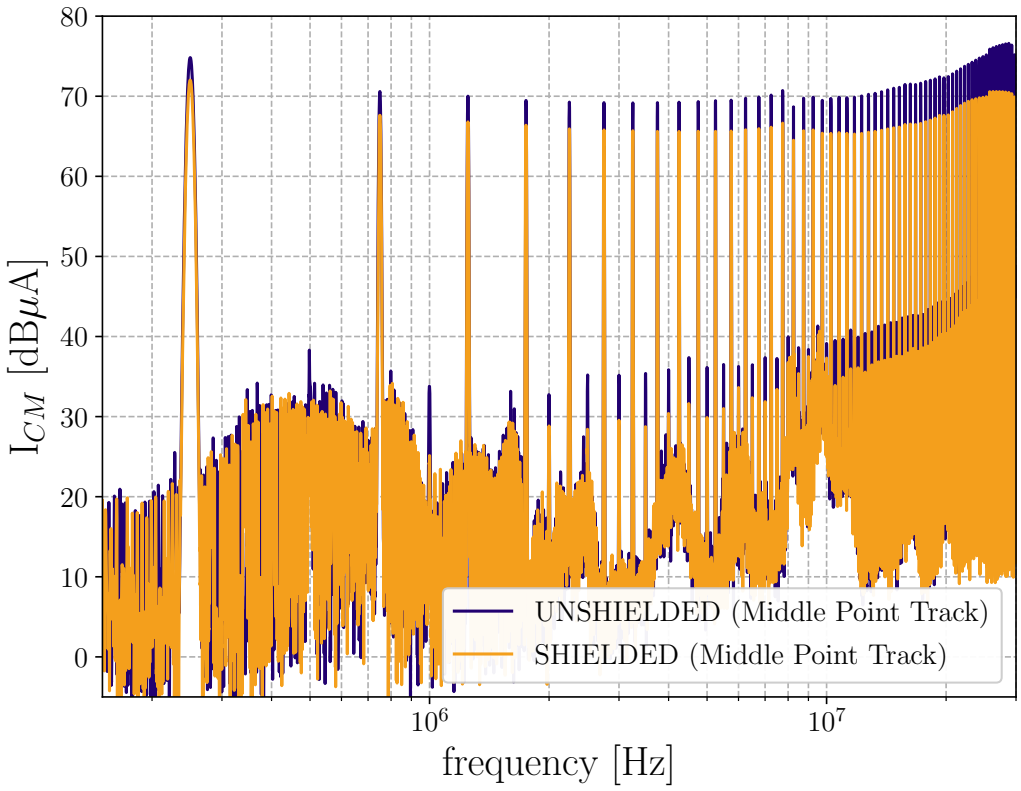


Figure 3.38: CM current emissions with and without shielded middle point track

Further reduction of I_{cm} can be obtained via shielding of the thermal pad. The effectiveness of thermal pad shielding is demonstrated in Fig. 3.39 by comparing the spectrum of shielded middle point track with that of shielded middle point track and shielded thermal pad, (here the orange spectrum from Fig. 3.38 is used as reference and plotted blue). The emission attenuation is observed in the whole frequency range, from 0.8 to 30 MHz, with the greatest diminution amounting to 7 dB.

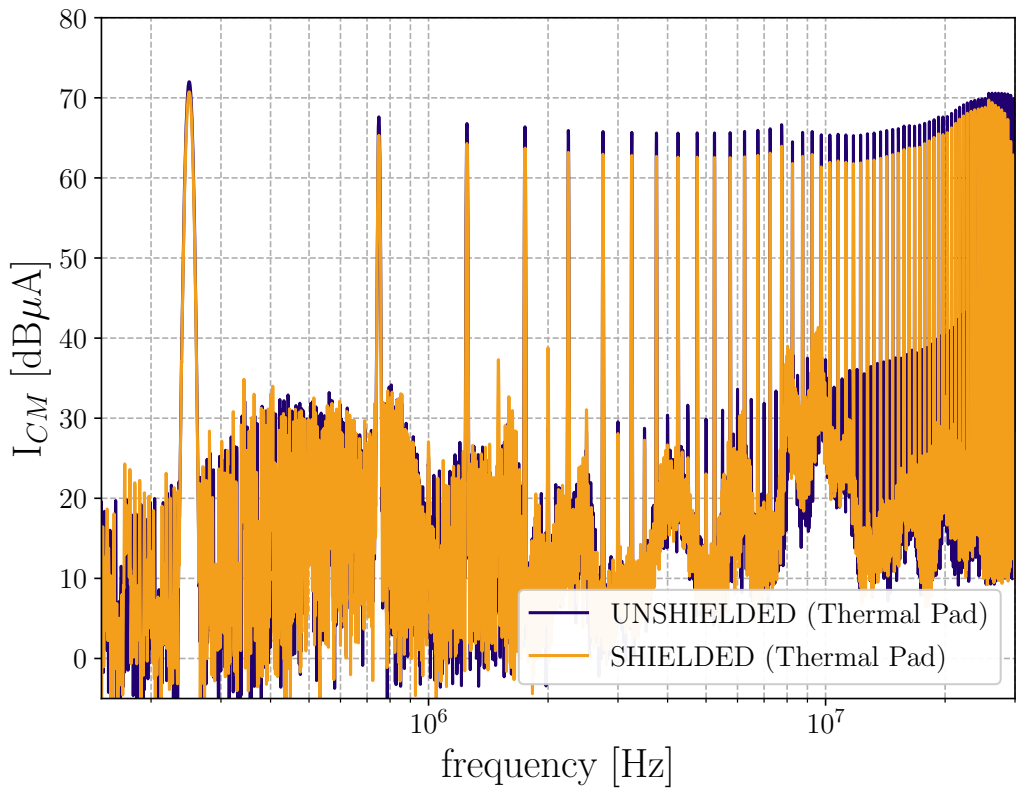


Figure 3.39: The effectiveness of thermal pad shielding

In the next step, shielding of the gate circuit power supplies was investigated. The copper foil was used to create a low conductive shield. As a result, successive decrease of I_{cm} level by 2-5.5 dB was observed in the spectrum (Fig. 3.40).

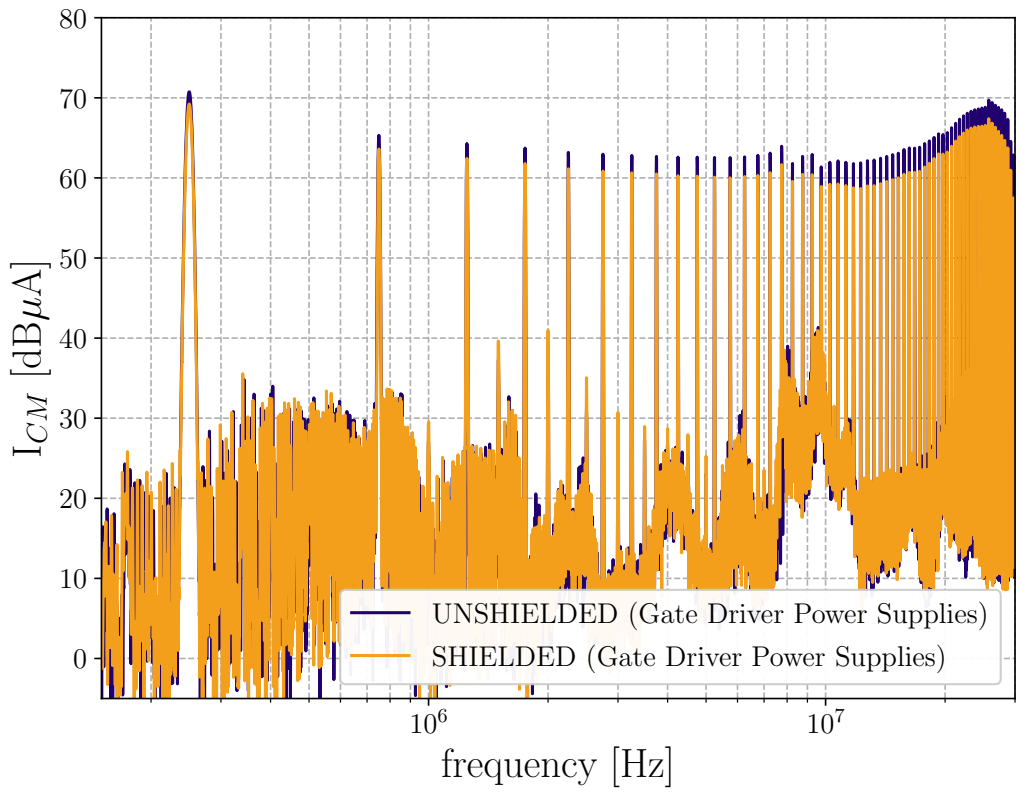


Figure 3.40: The effectiveness of shielding of gate driver supplies

Total shielding effectiveness and quantitative data comparison

The comparison of the unshielded and totally shielded converters is presented in Fig. 3.41, where significant reduction of I_{cm} noise is achieved in the whole investigated frequency range.

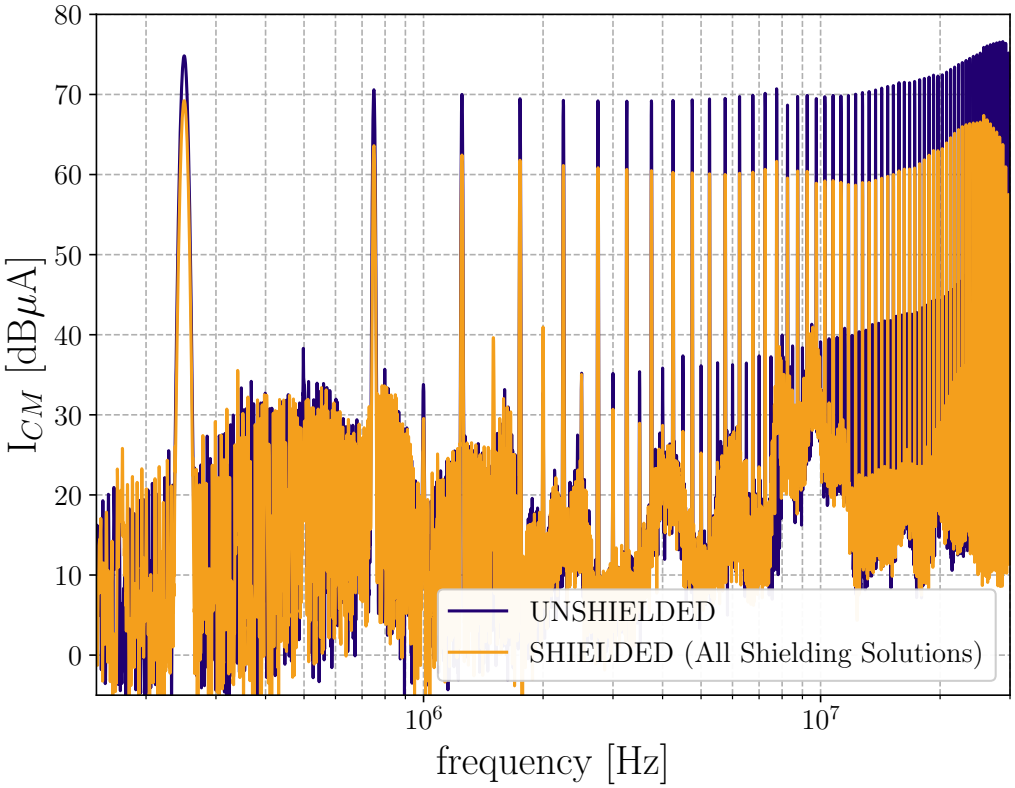


Figure 3.41: CM current emissions with and without total shielding solutions

The comparison of quantitative data is presented in Table 3.2. The noise levels for specific frequencies (beginning, middle and the end of the conducted emission spectrum range) are put together. In this way, the impact of individual contributors of shielding can be compared. Moreover, the scale of reduction with respect to the unshielded version is given in Table 3.2 in brackets for each shielding step.

Table 3.2: Comparison of cm noise levels at specific frequencies (reduction indicated in brackets)

Specific frequency of spectrum	**Unshielded [dBµA]**	**Shielded: middle point [dBµA]**	**Shielded: middle point & thermal pad [dBµA]**	**Shielded: middle point & thermal pad & gate power supplies [dBµA]**
1.25 MHz	70.01	66.79 **(-3.22)**	64.29 **(-5.72)**	62.43 **(-7.58)**
10.025 MHz	69.72	65.36 **(-4.36)**	61.95 **(-7.77)**	59.2 **(-10.52)**
29.76 MHz	75.17	69.91 **(-5.26)**	62.87 **(-12.3)**	57.5 **(-17.67)**

3.3 Power-Chip-on-Chip (PCoC) concept

This chapter introduces the idea of 3D layout design, describes it in detail, shows its adaptation to lateral GaN devices, and presents a fair comparison of 2D (horizontal arrangement of power devices and decoupling capacitors), 2.5D (vertical arrangement of power devices with horizontal decoupling capacitors), and 3D (vertical arrangement of power devices and decoupling capacitors) approaches. It is another approach to improve the layout in terms of EMC attenuation.

3.3.1 Concept description

The concept is based on the technology invented for Silicon devices (IGBTs) in which the vertical current flow occurs. The structure presented in [85] examine a hybrid integration of power dies, where one chip is placed on the top of the other one (Fig. 3.42). Authors of this publication name it as a Power-Chip-on-Chip 3D configuration. In PCoC the power dies are inserted between two electrical plates (usually copper plates) and joined together creating a bus-bar-like power module.

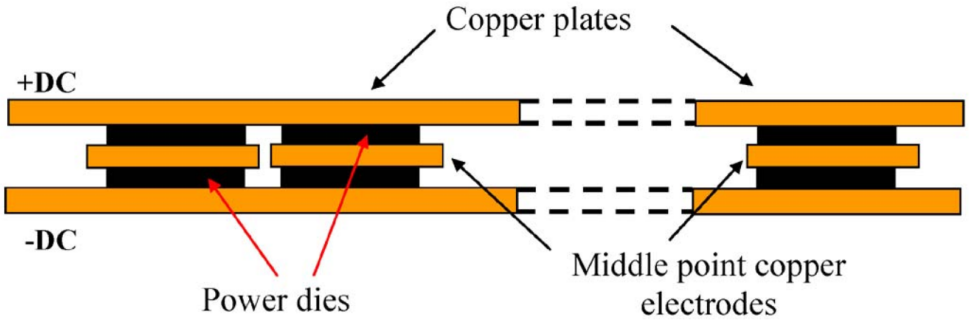


Figure 3.42: PCoC concept basis using vertical devices (Silicon based transistors) [85]

According to the authors [85], the PCoC design offers a number of advantages due to its unusual component arrangement. First, the bus-bar structure allows extreme reduction of parasitic inductance of the power loop [16, 72]. In addition, parasitic coupling is minimized within a single switching cell or switching cells (e.g. for multiphase solutions). The sandwich of semiconductor elements between two conductive plates also reduces radiated and conducted EMI (tested in simulations). The reduction in conducted EMI is due to a significant reduction in direct electrostatic coupling between the center point and ground. In addition, decoupling between the power and gate circuits is observed in the 3D structure.

The next evolution of the PCoC concept [66] represents an extension of the design with the additional integration of decoupling capacitors and gate circuit inside the bus-bar structure (Fig. 3.43). This further reduces parasitic inductance (11 nH is shown for the planar layout and 0.5 nH for the 3D). Moreover, magnetic coupling between the gate and power circuits is reduced. In additionally, for the first time, a PCB was used as the core of the PCoC structure, to which external copper planes were added on the outside. In addition, some drawbacks of the solution are detailed:

- difficulties in connecting the gate circuit, -integration of SMD decoupling capacitors is a challenging task,
- the solution requires an external compression system to hold the sandwich together,

- electrical isolation between the heat sink and the connectors/boards is required,
- a appliance of heat sink on both sides is required.

In addition, the possibility of adopting the structure to fast switching transistors (e.g. SiC and GaN) is mentioned for the first time - in such an application the overvoltage reduction should be more noticeable[73].

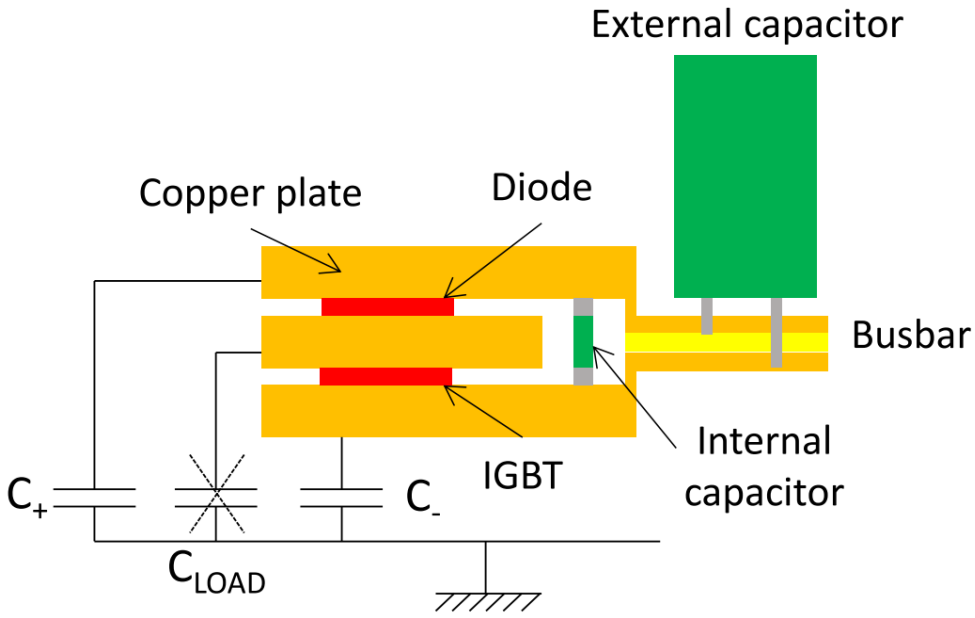


Figure 3.43: Cross-view of PCB-based PCoC concept with integrated gate circuit and decoupling capacitor [65]

3.3.2 PCoC adaptation to GaN devices

The proposed design utilizes only the PCB to arrange all interconnections and provides a high level of integration between discrete components and PCB copper layers (planes/polygons) and tracks. The basic idea from [35] is shown in Fig. 3.44. In this paper, the proposed design focuses on the simplicity of manufacture and assembly of the boards. Thus, the multilayer board is designed with the minimum number of layers which gives satisfied results (4 layers) was used to implement the PCoC structure.

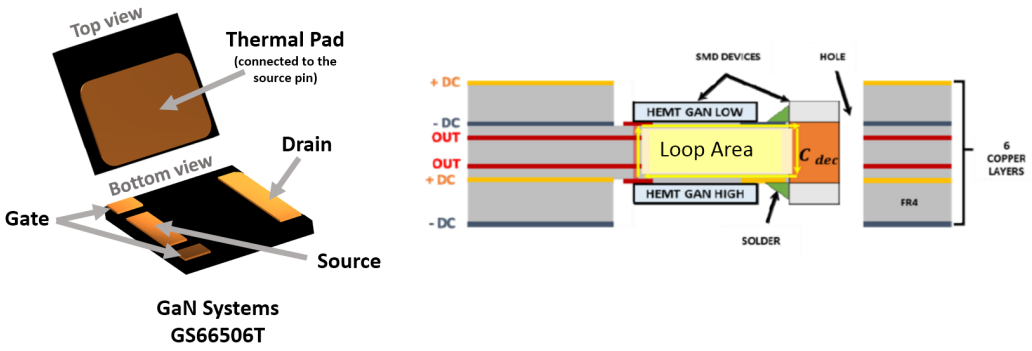


Figure 3.44: PCoC concept basis using lateral devices (GaN transistors) [28, 35]

In this PCoC concept, the thermal path must be separated from the electrical connections since the PCB used for this purpose cannot easily dissipate the generated heat. Therefore, external heat sinks are used on both sides of the switching cell, as shown in Fig. 3.45. Using a technology other than Insulated Metal Substrate (IMS) instead of PCB would allow the heat flux to be conducted through the same side of the chip, but this is usually only a single layer substrate that disabling all necessary interconnects, e.g. for gate circuits. Therefore, some specific packages of GaN transistor are used allowing the different use of each side: one for the electrical connection and one for thermal pad for the heat sink [1].

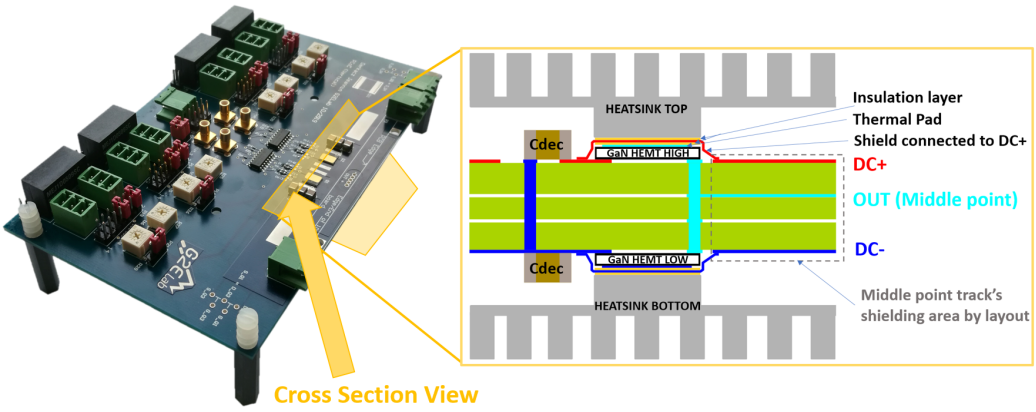


Figure 3.45: Prototype of converter with the "3D/2.5D" PCoC layout and cross view of arranged cooling system

Once again the GaN Systems GS66506T transistors are used. Moreover, the decoupling capacitors placement differ from the Fig. 3.45. They are placed horizontally (on the both sides of PCB) and connected to the bus-bars directly and by

dedicated vias. Twelve 100 nF 630 V SMD capacitors (KEMETC1210C104KBR) in case 1210 were used to decouple two phase-legs of converter (6 capacitors per phase-leg). Those capacitors, together with two EPCOS CeraLink capacitors 500 nF 700 V, are creating a DC-Link with 2.2 µF capacity. All of those components are placed symmetrically on the both sides of PCB. Due to horizontal arrangement of decoupling capacitors (on the surface of the PCB), the design with PCoC transistors layout is called 2.5D (not full 3D layout as presented in Fig. 3.45).

The exploded 2.5D view of the power layout is shown in Fig. 3.46a. The GaN switches are marked by arrows, indicating the placement one below the other corresponding to the PCoC idea. The transistors are connected directly to the DC+ and DC- bus bars and the common point (middle point of inverter leg) is created by the vias connection. The converter's inverter leg middle point track is arranged on the inner layer of the PCB, therefore being in the middle of the DC bus, as in the PCoC basic concept. The decoupling capacitors are placed as close as possible to the switches on each side of the PCB (6 capacitors for each inverter leg – 3 on the top and 3 on the bottom). The switching loop is illustrated in Fig. 3.46a: The loop area is as small as possible, since it is contained inside the PCB thickness. In order to reduce more the switching loop, the PCB with a reduced thickness can be considered. Embedded dies technology is another option that could permit also to place GaN components closer one to the other. Regarding gate drive layout design, short connections and perpendicular plane with power layout have been chosen to meet the design criteria described in Chapter 3.1.1.

To assess the electrical and EMC performances of the inverter leg, two different versions have been built: one 2.5D corresponding to Fig. 3.46a and another one using a more conventional 2D layout illustrated in Fig. 3.46b. Both layouts look quite similar, except that in the 2D version all 6 decoupling capacitors and 2 power devices are placed on the same side of PCB.

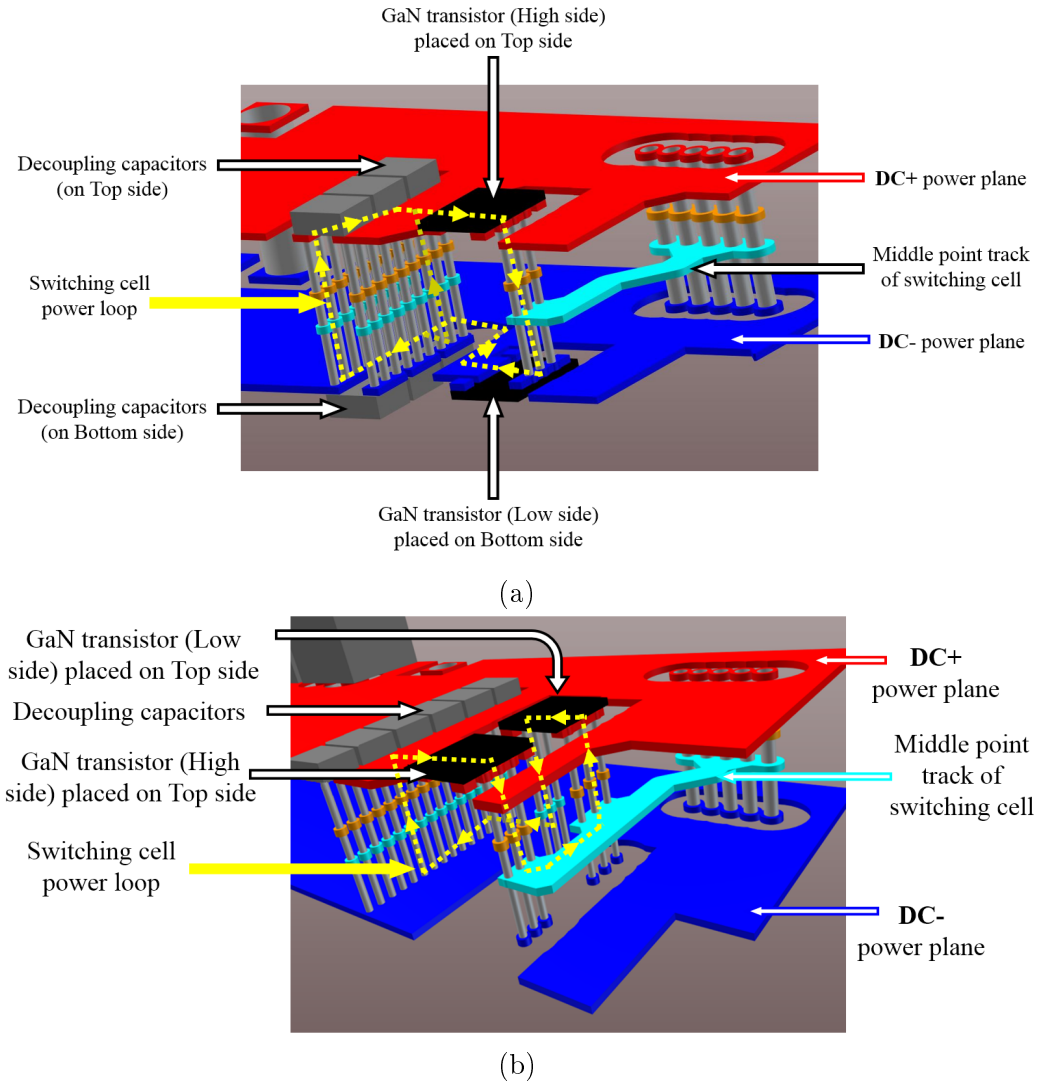


Figure 3.46: Exploded 3D view of: a) proposed PCoC 2.5D layout; b) conventional 2D layout (thickness of the board in scale 10:1)

After gathering of first results of 2D & 2.5D design, some of drawbacks for proposed layout have been identified and new, a fully PCoC-compliant 3D layout have been designed and tested (Fig. 3.47). Again, the design is based on a 4-layer PCB, the transistors used are the same GaN Systems GS66506T, and the number and volume of capacitors have not changed. On the other hand, the location of these capacitors has changed - they are mounted vertically in dedicated holes in the PCB, which have metallization on the edges in order to be able to solder SMD components. In addition, it should be noted that the loop area is even smaller than in the 2.5D layout. The number of vias has additionally been reduced - due to the lack of surface-mount capacitors. All these procedures should result

in a further reduction of the parasitic inductance of the power loop and better quality of the drain-source voltage waveforms.

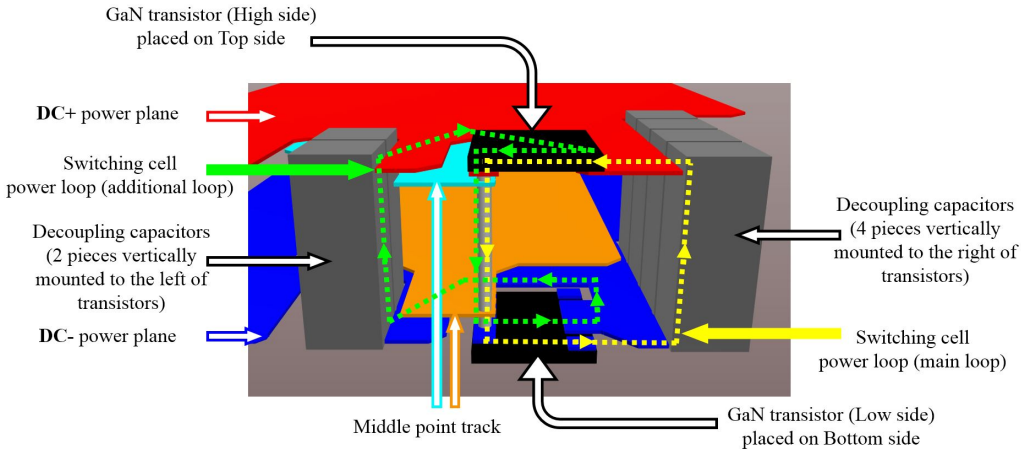


Figure 3.47: Exploded 3D view of fully 3D PCoC layout (thickness of the board in scale 10:1)

3.3.3 Electrical performance of 2D, 2.5D and 3D layouts

The electrical performance tests have been conducted in terms of voltage overshoot and power loop inductance identification. Using the simulations from Q3D the stray inductance of the 2D, 2.5 and 3D layouts has been compared and plotted in Fig. 3.48 (the apparent increase in inductance values around 50 MHz and above is not an error but the result of resonance occurring at 120-150 MHz). For each design the minimum power loop value is around 10-20 Mhz. It is worth to notice that for full 3D layout inductance [1.49 nH] is 3 times lower than for 2.5D [4.66 nH]. A summary of several values of parasitic inductance, for different frequencies, can be found in the Table 3.3. As expected, the 2D design has the highest parasitic inductance [4.83 nH], however, not much different from the value for 2.5D layout. It should be noted that the plotted characteristics and data in the table do not include the internal parasitic inductance of the transistor package (which totals 0.4 nH for one GaN transistor).

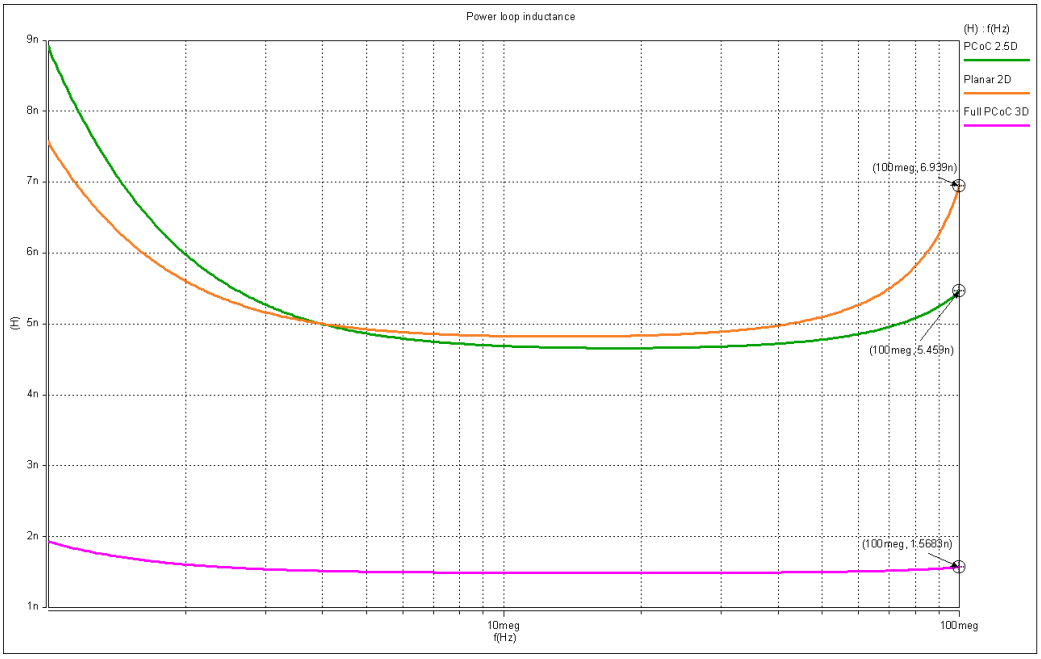


Figure 3.48: Power loop inductance plot based on simulation results

Table 3.3: Stray inductance of the switching cell (results from simulations). Comparison between 2D and 3D layouts at 100 MHz

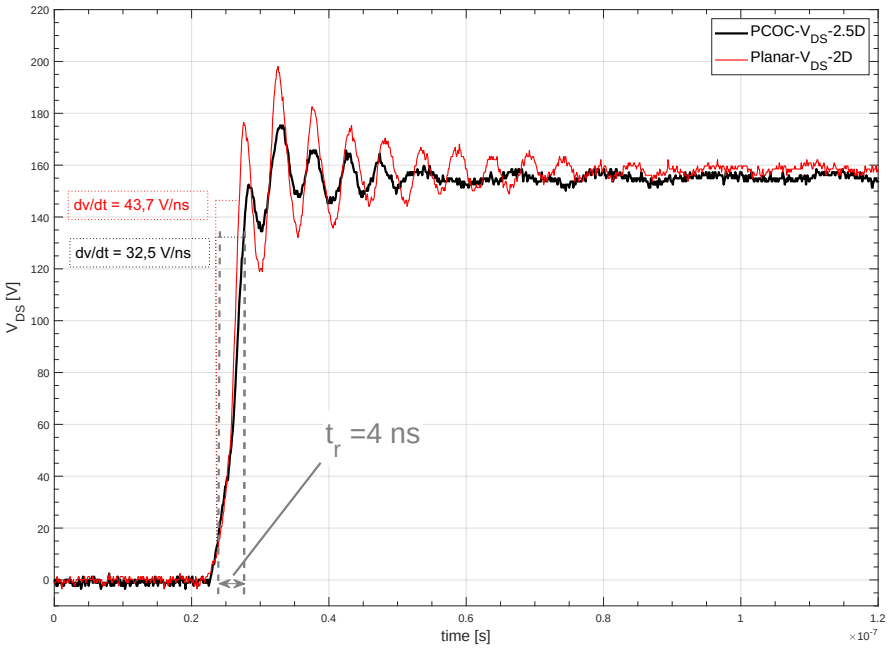
Layout	**2D**	**2.5D**	**3D**
Stray inductance @1 MHz	8.9 nH	7.56 nH	1.93 nH
Stray inductance @10 MHz	4.83 nH	4.69 nH	1.49 nH
Stray inductance @20.5 MHz	4.84 nH	4.66 nH	1.49 nH
Stray inductance @87.5 MHz	6.13 nH	5.2 nH	1.54 nH
Stray inductance @100 MHz	6.94 nH	5.46 nH	1.57 nH

The direct effect of layout on the resulting parasitic inductance value also translates into the quality of electrical parameters. For each of the cases considered, the drain-source voltage V_{DS} waveform on one of the transistors was measured. A significant reduction in the overvoltage and the presence of oscillations at the transient can be seen. The waveform for the 3D layout looks very clean. However, it should also be noted that the steepness of the voltage has significantly decreased. This is an effect due to 2 factors:

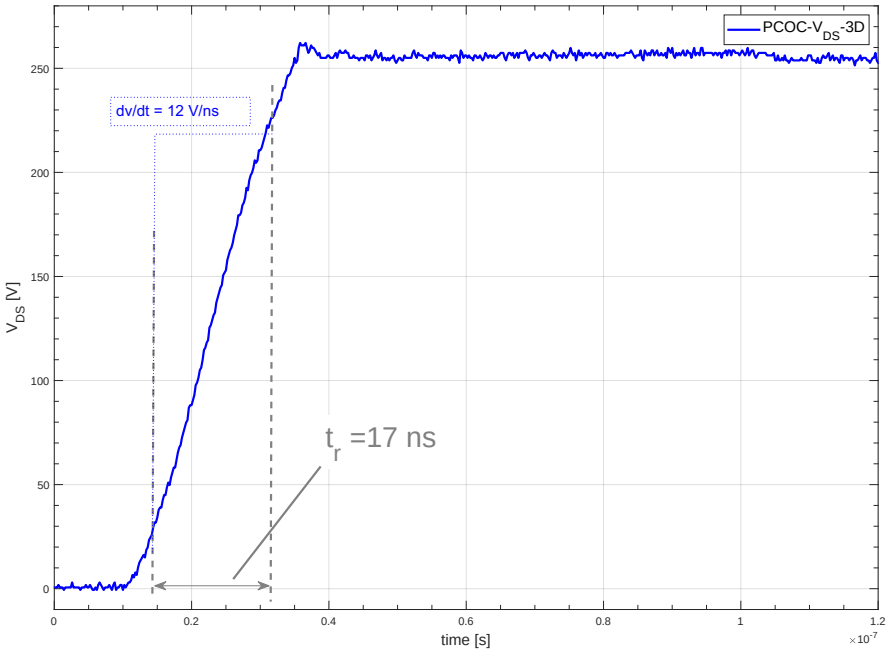
- all designs were tested in the option with center point shielding. In such a situation, the full PCoC layout allows even greater coverage of the middle

point by the shields. So the parasitic capacitance between the middle point and $DC+$ and $DC-$ is also increased, which is equivalent to adding additional capacitance to the C_{DS} capacitance of each transistor,

- Layout full PCoC had an increased middle point track shape, therefore equivalent C_{DS} capacitance was larger.



(a)



(b)

Figure 3.49: Voltage overshoot comparison: a) 2D and 2.5D layout; b) 3D layout

3.4 Final comparison of EMC for 2D with shielding, and 3D (PCoC) with shielding

The effectiveness of shielding has already been demonstrated and presented in Chapter 3.2. At that time, the study was conducted on a 2D layout version, principally because of the simplicity of the design and the easier application of shielding on thermal pads.

However, once the fully 3D PCoC layout is developed and manufactured, it should be tested and compared with previously collected results to determine how much this design affects conducted EMI.

In the Fig. 3.50, the CM noise generation for 2D and 3D with only middle-point track shielding is presented. It proves that shielding is working in the same way, and PCoC is more shielded thus high frequency resonance is earlier (it is an effect of increased stray capacitance between drain and source, resulting in a bit slower V_{DS} slope). In the remaining frequency range reduction is the same = the same effectiveness of shielding.

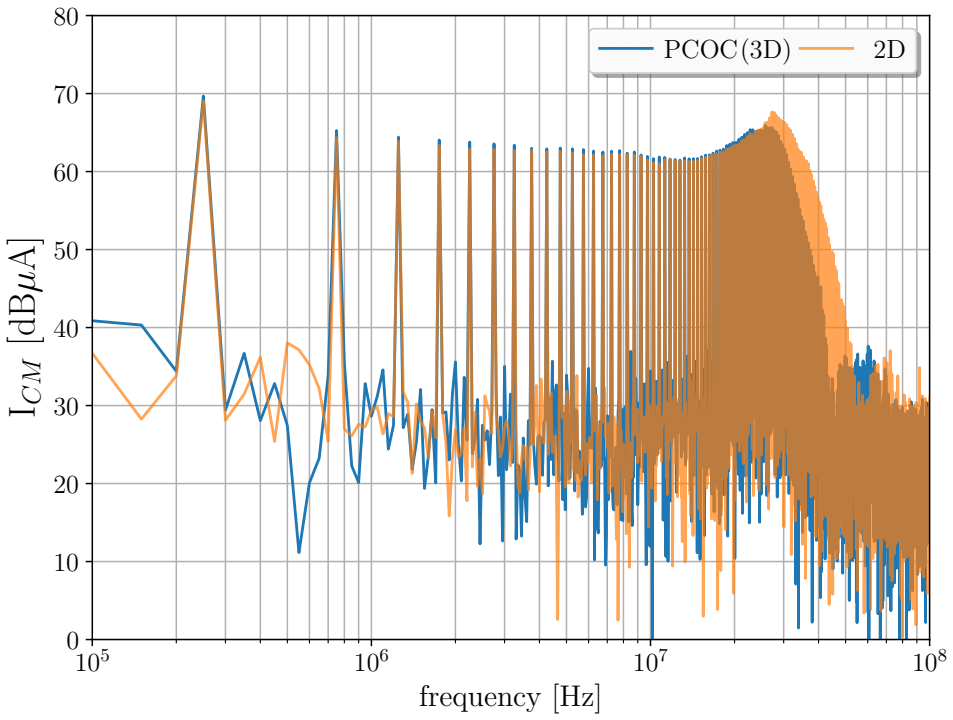


Figure 3.50: PCoC and 2D layout - CM noise comparison limited for middle point shielding case

Then Fig. 3.51 compares the fully shielded 3D and 2D - the effectiveness of the shielding is almost the same. Slightly better attenuation (1 dB @250 kHz to 5 dB @30 MHz) is noticed for PCoC layout - it could be the contribution of PCoC in reduction of CM noise. Comparison of DM noise (Fig. 3.52) shows that in general PCoC has an effect by reducing DM in almost the whole frequency range except 1-10 MHz where the layout change results in a slightly higher generation.

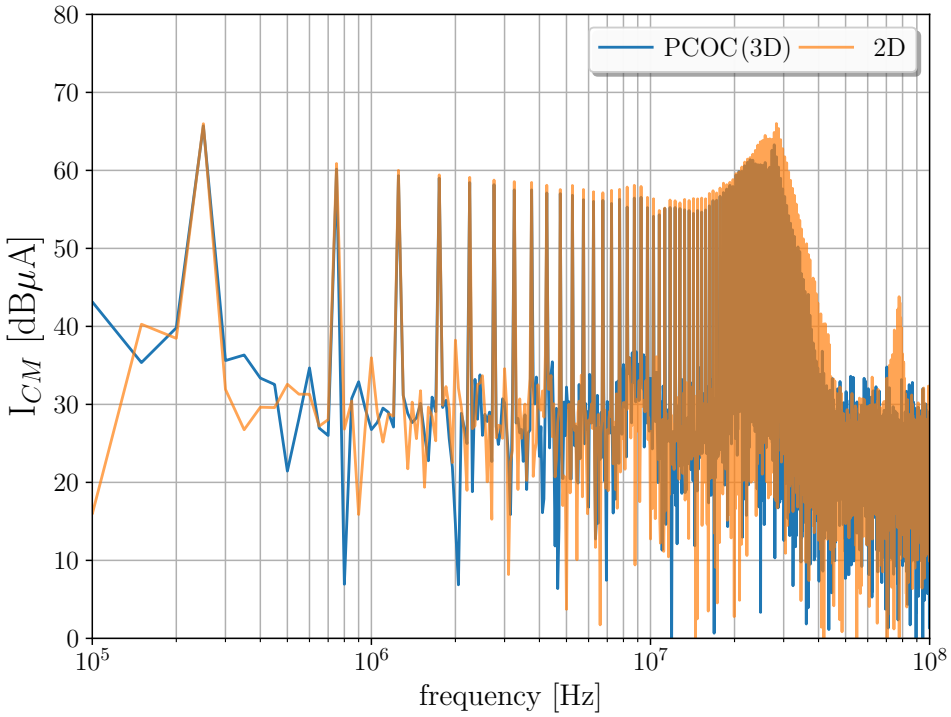


Figure 3.51: PCoC and 2D layout - CM noise comparison for fully shielded boards

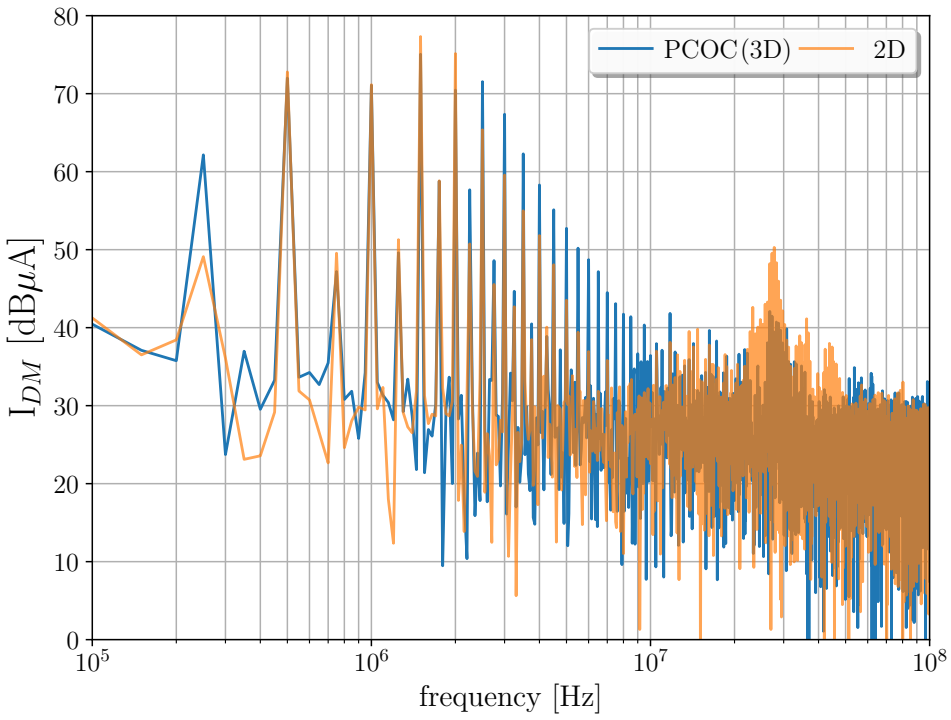


Figure 3.52: PCoC and 2D layout - DM noise comparison for fully shielded boards

3.5 Layout - conclusion

This chapter presents a comprehensive layout consideration for power electronics with GaN devices. The critical elements (mainly parasitics) and interactions are identified and described in detail. Then, a proposed simulation workflow is presented as a tool for fast and low-cost layout verification. A set of practical rules for EMC experiments is also given and elaborated.

The proposed shielding technique is described and explained in detail. The new approach by shielding applied to the positive or negative potential of the stable bus-bar has been presented, simulated, and measured, and its effectiveness has been proved. Moreover, three different contributors of Common Mode capacitance: middle point track, thermal pad and gate circuit power supplies were extracted and highlighted. The shielding concept was successfully applied to each of them, which resulted in a total of over 17 dB reduction of CM noise. In order to guarantee that the CM reduction is directly the effect of shield imple-

mentation, care has been taken to have the same $\mathrm{d}v/\mathrm{d}t$ for the unshielded and shielded cases.

The proposed shielding solutions can be used in embedded integration of power device dies in PCBs. Due to the obtained reduction of CM current noise, they can be essentials for WBG power devices. Resulting in weight and volume reduction of EMI filters, and do not impacting power density of converter without noticeable increase of additional copper layer weight.

The application of shielding by conductive copper layers increases parasitic capacitances between drain and source terminals of switching transistors, thus introducing extra power switching losses. The use of Kapton leads to a quite large impact of doubling the ($R_{th(c-h)}$) in the shielded converter but it can be minimized in the designing step by appliance of other material. This thermal material aspect should be considered in the designing process and global optimization of converter to achieve the trade-off between CM current emission, power switching losses and thermal performance.

Finally, an adaptation of the 3D approach to GaN design was presented and a successful adaptation of the PCoC concept to lateral devices was achieved. Significant improvements in electrical performance were demonstrated, in particular a reduction of the power loop parasitic inductance to 1.49 nH, which also leads to a significant reduction of overvoltages and oscillations occurring at the transistor voltage. This approach is relatively easy to implement in any converter topology. The only drawbacks are the difficulty of the assembly process (due to the vertical capacitors used) and the need for heat sinks on both sides of the PCB.

Chapter 4

The new generation of magnetics for high-speed devices

"The greatest discoveries often lie not in finding new things,
but in seeing familiar things in new ways."
Alexander Fleming

The Wide-Bandgap devices on the power electronics market has revolutionize thinking about the new converters. The properties of WBG have been widely described in Chapter 1.2. The emergence of GaN devices provides lower conduction losses, higher switching speed together with endurance of higher junction temperature than in Silicon devices even if the price to pay is the effect of high transients of $\frac{dV}{dt}$ and $\frac{dI}{dt}$ in terms of EMI generation. All these attributes together permit building the power electronics converters with smaller size, volume, weight, reduced cooling system, very high power density and good form-factor.

However, the magnetics are often the bottleneck for new solutions with WBG [15]. The inductors and transformers occupied a significant amount of space in power converters. In order to obtain high power density of full converter, their miniaturization is indispensable and possible due to high switching frequency of WBG. However, it creates a lot of problems to be solved for magnetic components [17]. High frequency operation of the converter is affecting the volt-second balance of magnetic component, increasing the proximity effects, imposed higher ac resistance and current crowding problems [59]. Also, the problem of inductance drop around the certain current value cannot be omitted [15]. Due to the high peak-to-peak current ripple the higher core losses are generated and the problems with saturation of magnetic core appears. Constant research is needed in this field to improve the properties of magnetic materials [48, 68]. This field is right now a bit lagging by the development of WBG devices. However, there are noticeable works in the field of new soft magnetic materials, nanocrystalline and amorphous alloys. Also new research of magnetic nanocomposites are started and it might be possible 3D printing and microfabrication in the near future [79]. Further problems - high frequency switching increases winding losses, winding suffers greater stress and significantly high termination connections losses [59]. The Litz wires are partially solving these issues but it might be worth to consider the PCB technology to solve problems a bit more. Next, the increased losses at high frequency and reduced volume of the magnetic component create the difficulties with the heat removing from these passive elements, which is another design problem, especially at high power levels [15].

Additional limitations are due to stray capacitances which degrade the HF behavior: consequently, high speed transitions which generate disturbances are no more blocked by high impedance devices (implicitly magnetic elements), since their impedance is no longer high enough for high frequencies in the MHz range. Thus, the high speed of GaN devices causes a large CM current to flow through the stray capacitance of the magnetic device (as in Fig. 4.1). It is also a challenge to manage the EMI in high frequency design of magnetics [59]. In the following chapter this problem is examined in details.

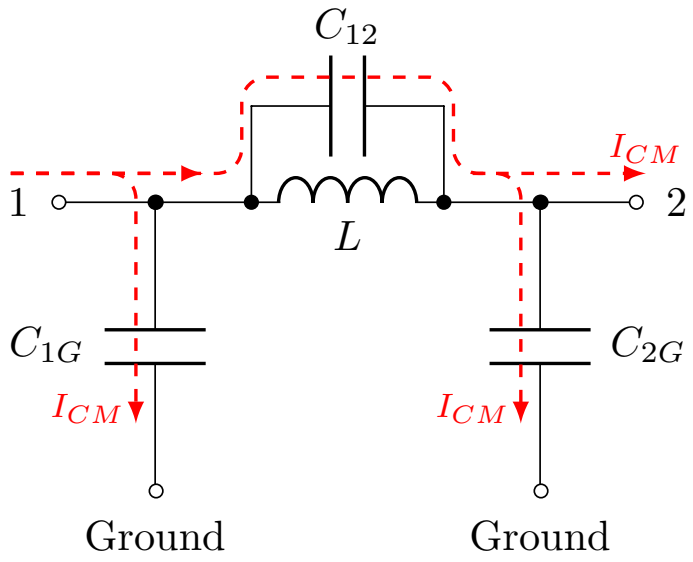


Figure 4.1: Inductor model with stray capacitances and CM current paths

4.1 The need of power module output inductor

As mentioned in the beginning of this manuscript, this work focuses on the limitation of EMI generation in power converters with WBG with the special attention for the future power module solutions. Testing of solutions for power modules, in terms of EMC, is not an easy task. The tests should be performed in conditions similar to real converter operation - it was also mentioned in Chapter 3. In works presented in previous chapter the solutions for inverter leg layout of power module were tested in the Half-Bridge Inverter conditions with R and RL load. Further, the impact of CM noise that is flowing through the load has been identified and described. Origin of this phenomena is related to the stray

capacitances around middle point of inverter leg and other parts of converter (i.ex load stray capacitance to ground). The middle point is the node with high $\frac{dv}{dt}$. If around this node exists any stray capacitances the CM current circulation is introduced. Therefore, if there is any blocking device between middle point and load, the direct connection of classical load (R or RL with large parasitics) creates additonal CM current through this load increasing total CM distortion seen on the LISN. To limit this phenomena, during the laboratory tests it has been applied the Common Mode Choke with a careful setup of the EMC test bench.

Based on this expertise, application of the additional decoupling EMI inductor has been proposed. Cut off the CM noise path to the load (output stage of converter) can be achieved by adding the dedicated inductor to middle point of inverter leg. Placing of additional impedance as close as possible to the middle point reduces $\frac{dv}{dt}$ in the output stage of converter, thus limiting CM currents there. Clearly the decoupling inductor is not a perfect device and also has parasitics (mainly stray capacitances). They can change or enhance the CM noise generation. Thus, an impact of parasitics should be taken into account during the designing step.

The aim of decoupling EMI inductor is very similar to decoupling capacitors. Its role is to prevent from the oscillations on the DC Bus and V_{DS} voltages across the transistors. Thus, they are providing high quality of the voltage transients across inverter leg (power module). Therefore, decoupling EMI inductor is as essential, as decoupling capacitors and should be always placed to reduce the CM emission and provide high quality of the power module's EMC performance. In this manner, the future GaN based power module should be developed and commercialized (Fig.4.2). In this study, the solution with a Common Mode Choke is not taken into account because it is built with two windings through which the out and returning current is flowing. Thus, the power module number of ports should be extended by additional 2 ports for returning current of CM.

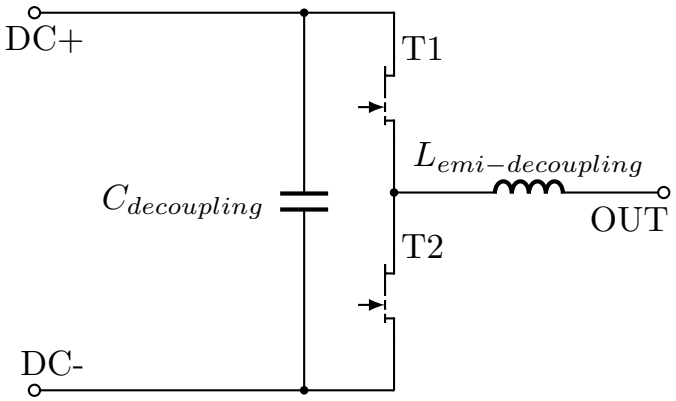


Figure 4.2: Proposal of new generation of GaN based power module

4.2 Integrated Inductor concept

The inductor should provide certain and stable impedance to limit the CM noise but also to carry the main high frequency current of the converter. The design of proposed decoupling inductor can be described as Integrated Inductor. The geometry is designed as a planar inductor based on the PCB manufacturing method. Magnetic core is inserted into the PCB and the winding is created by PCB tracks on the both sides and interconnected by vias. The proposed solution was arbitrarily selected in order to apply this technology and validate it. In the further considerations, the two layouts of Integrated Inductor have been analyzed: unshielded and shielded. Shielding of Integrated Inductor involves the introduction of stable potential planes (connected to DC+ on top and DC- on bottom) on the both external layers of inductor (Fig. 4.3) to close the winding between them. The concept of shielding with a theoretical explanation has already been described in Chapter 3.2.1. The goal is to change the capacitive behavior of stray elements inside the inductor.

Chosen solution meets some of the critical requirements for high frequency magnetics. Planar arrangement on winding on the PCB layers should minimize winding losses. Due to the fact that integrated inductor is PCB based, the termination losses are limited to minimum. If connection between inductor and middle point is created by the same track inside the PCB, then any additional resistive point is not created. Magnetic material losses are limited by choos-

ing the high frequency material 3F4, which has a stable permeability of up to 3 MHz. Planar, PCB based arrangement of the inductor allows to apply the heat sinks on the both sides of inductor to facilitate removing the heat from magnetic component. Also, building of the winding based on PCB tracks limits the stray capacitance between input and output (C_{12} in Fig. 4.1) compared to classic solutions. Moreover, the PCB technology based design is very easy and convenient to introduce the shielding concept which was successfully validated for the power layout in Chapter 3. In this way, the crucial CM paths can be re-arranged and provide effective blocking inside the inductor/power module. Also, PCB technology of production provides repeatability of parasitics of Integrated Inductor, which is important for certainty of EMC behavior of power module. Summarizing, main positive features of integrated inductor are: direct and short interconnection with inverter leg (switching cell), very good shape factor, better cooling performance than classical solutions, and possibility of production with repetitive stray element values.

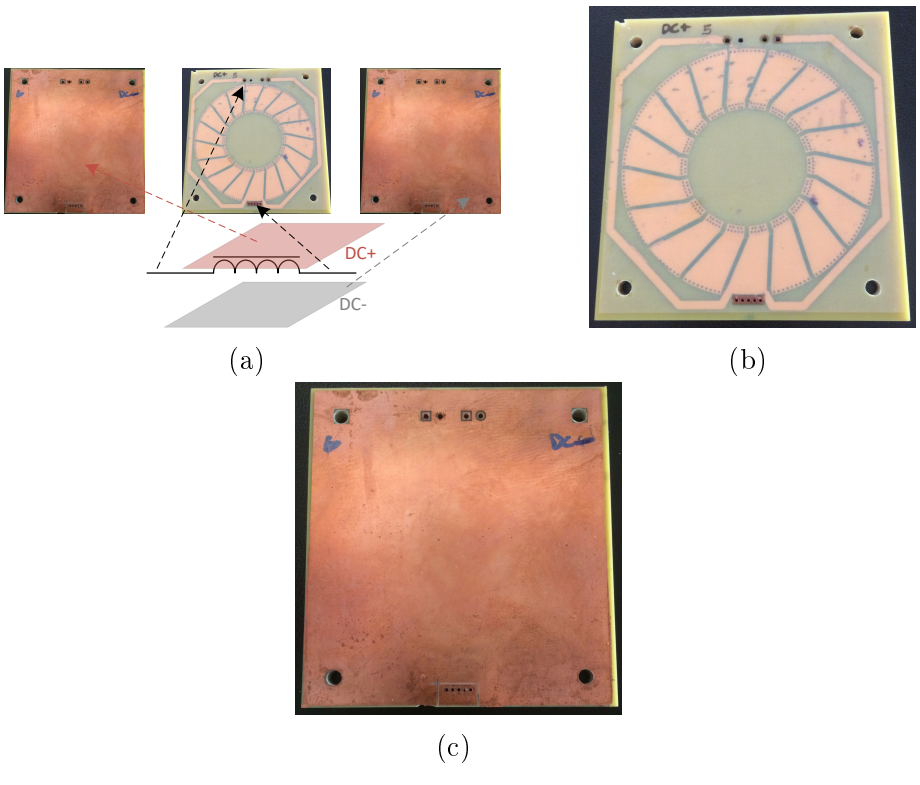


Figure 4.3: Integrated Inductor prototype: a) concept view; b) manufactured unshielded inductor; c) manufactured shielded inductor

To evaluate performance of the presented concept, a first prototype of Integrated Inductor (Fig. 4.3) is built, but no specific requirements were included in this first design approach. Proposed Integrated Inductor has been built as a 18 turns coil made on two PCB layers. Inside the PCB, the toroidal 3F4 ferrite core ring of the thickness of 2.5 mm is embedded. The procedure of manufacturing is quite complex and requires professional machines. First of all, the core of PCB without the copper layers (only FR4 prepreg layers) with the thickness of 2.5 mm is prepared. Thickness of the core must be the same as the desired thickness of magnetic core. Then, place for the magnetic core must be created in the PCB by milling. Also, the full toroidal magnetic core is cut into 2.5 mm thick slices by the usage of diamond disc on saw. Next, the slice of magnetic material is places into PCB core and additional layers of FR4 prepreg and copper are added on the both sides. At this stage, the PCB is placed into a press (with pressure and temperature regulation), where all the layers are pressed together and high temperature is applied to laminate it. Next, the drilling and metallization (electroplating) is made to provide the electrical contact between different layers of PCB. Next, on firstly cleaned PCB, the photosensitive film is applied on the both sides, and the mask with turns shape is placed and fitted with magnetic core. After appliance of UV light, revelation of the film, the PCB is ready for the etching process. Finally, the inductor prototype is obtained. In the case of shielded inductor, the another FR4 layer and copper is added, pressed, laminated, drilled, metallized, and etched (Fig. 4.4).

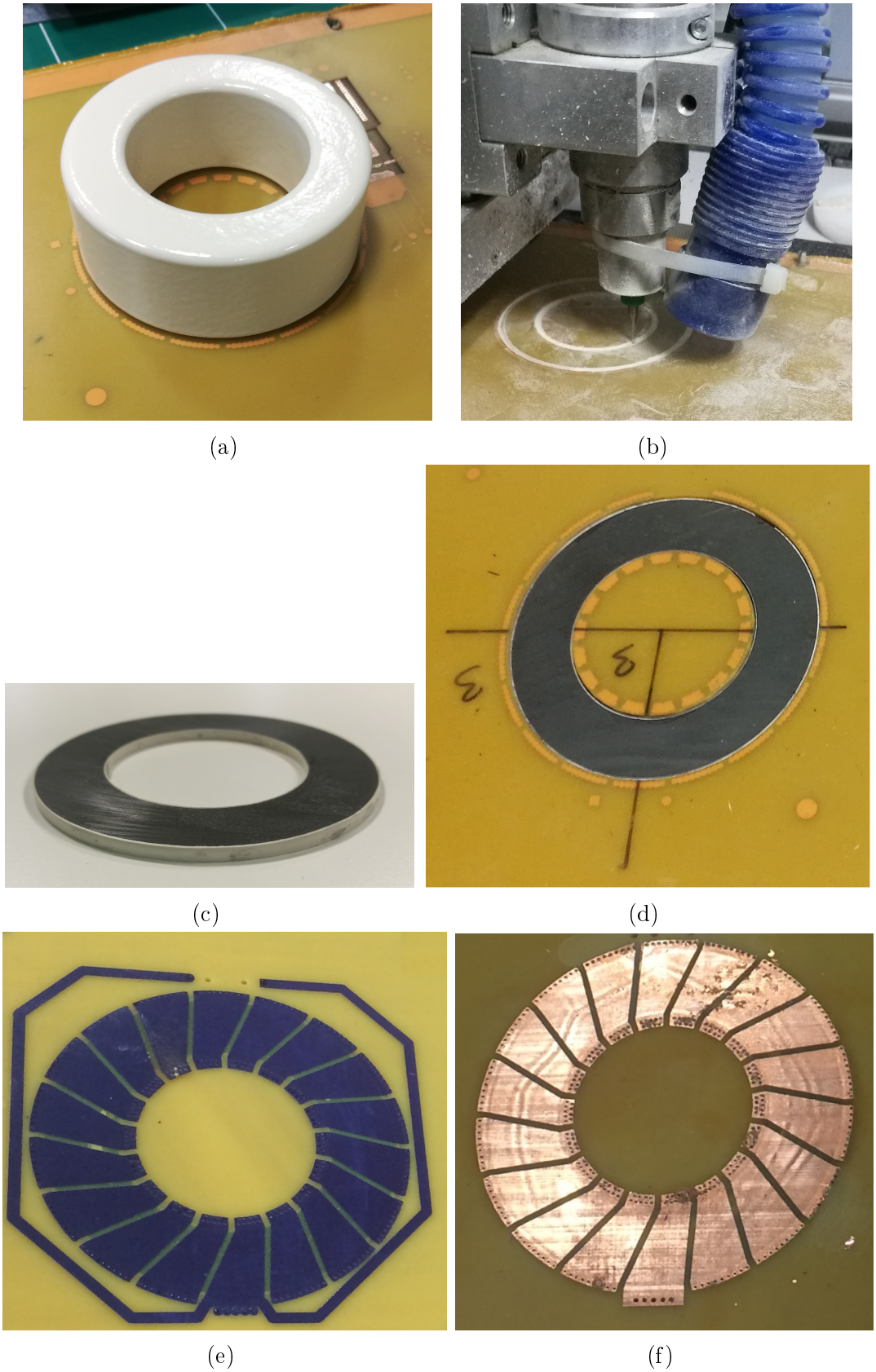


Figure 4.4: Integrated inductor production process: a) PCB view with full toroidal magnetic core; b) milling of PCB to create the space for ferrite core; c) cut 2.5 mm slice of toroidal magnetic core; d) PCB and core fitted together; e) view after etching; f) view after drilling and metallization

4.3 Integrated Inductor model and characterization

Two possible ways could be chosen in order to validate the impact of Integrated Inductor and its shielding. First one is based on the manufacturing of few prototypes of full converters (with integrated active devices and magnetic element). Also, it is more time consuming and expensive method. Second one is structured around simulation tools. In this way, the full converter model from Chapter 3 can be used and the only missing element is model of Integrated Inductor. The simulation approach was chosen to explore possible performance and concept evaluation in terms of Electromagnetic Compatibility for such integrated devices.

Model of inductor should be coherent with the reality to be as close as possible to physical representation, to understand an impact and validate the functional aspects of Integrated Inductor. The arbitrary playing with the values of inductor stray elements (for simulation purpose) is not even close to the reality - there is no connection between the value and real dimensions of the winding, core, distance between layers and so on. For the given research purpose, models of unshielded (simpler one with lower number of parasitics) and shielded (more complex) Integrated Inductor have been considered. Thus, the characterization procedure has been developed and is described below (the following description concerns the characterization of a shielded inductor). It is worth to mention that the characterization object has many parasitics, hence it is complex to identify and the procedure is complex.

Model topology was created in accordance with the partial capacitance method [34]. This method describes modeling electric interconnections between conductors (electrical ports) through network of $n(n+1)/2$ fictitious capacitors. In the physical layer it means that around each conductor (port) the electric fields are created by this inductor and the other ones in the nearby. Therefore, a system with, for instance, 3 ports and stable potential (i.ex. ground) can be represented as a system of capacitances $n(n+1)/2 = 6$ connected to the complete object, as presented on the Fig. 4.5. The total electric energy stored in this multiple conductor system is the sum of electric energies of all capacitors in the system

[34].

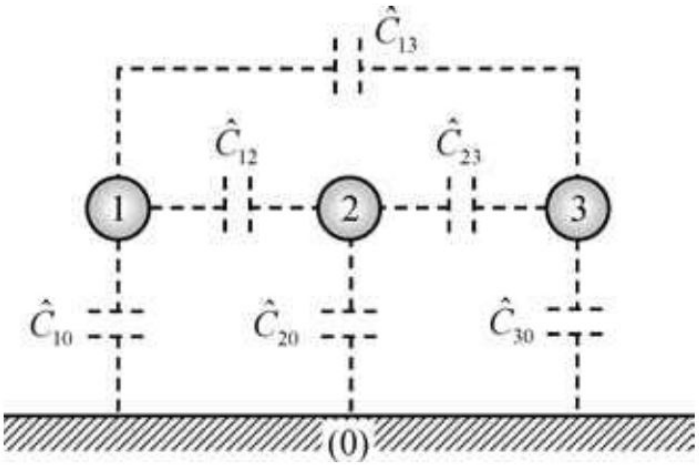


Figure 4.5: Partial capacitance method for 3 port system with ground [34]

Based on this theory, in the shielded Integrated Inductor, it can be distinguished 4 electrical ports (inductor input, output, top shield connected to DC+, bottom shield connected to DC-) + stable potential of ground. Thus, the electrical model should contain 10 stray capacitances. Full model should contain also the inductance of inductor and two resistances: (core and winding losses). On this basis, the Integrated Inductor model was proposed as shown in Fig. 4.6. After determination of the model scheme, the characterization process has been developed and described in details below.

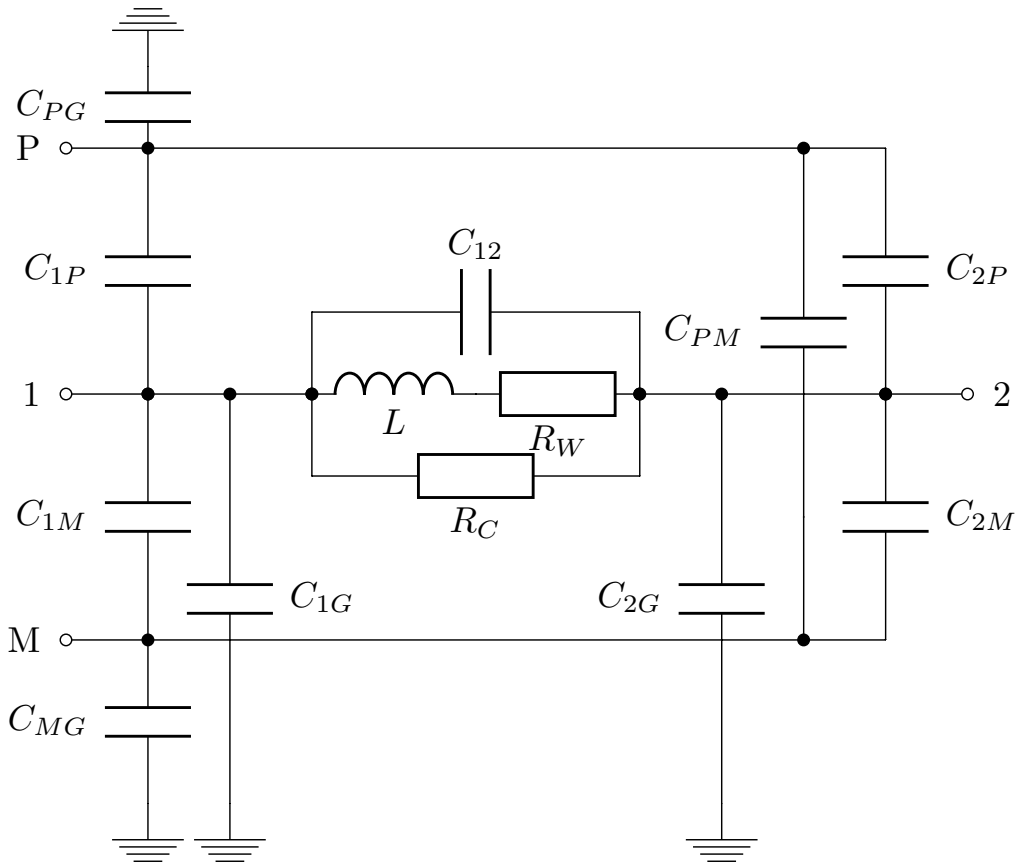


Figure 4.6: Integrated Inductor model scheme

Proposed characterization method is based on two steps. Main assumption for the system is to compose it from elements depended on power path (from point 1 to 2 on Fig. 4.6) and the electrostatic part which is created by plate capacitances (shields) inside of integrated inductor and not connected directly with power path. Thus, the first step is the electrostatic measurement with shorted 1 and 2 terminals. In this configuration, system can be presented as in Fig. 4.7 and newly introduced capacitances C_{1-2P}, C_{1-2M}, C_{1-2G} are related to the origin scheme by relations described by equations 4.1.

$$\begin{cases} C_{1-2P} = C_{1P} + C_{2P} \\ C_{1-2M} = C_{1M} + C_{2M} \\ C_{1-2G} = C_{1G} + C_{2G} \end{cases} \tag{4.1}$$

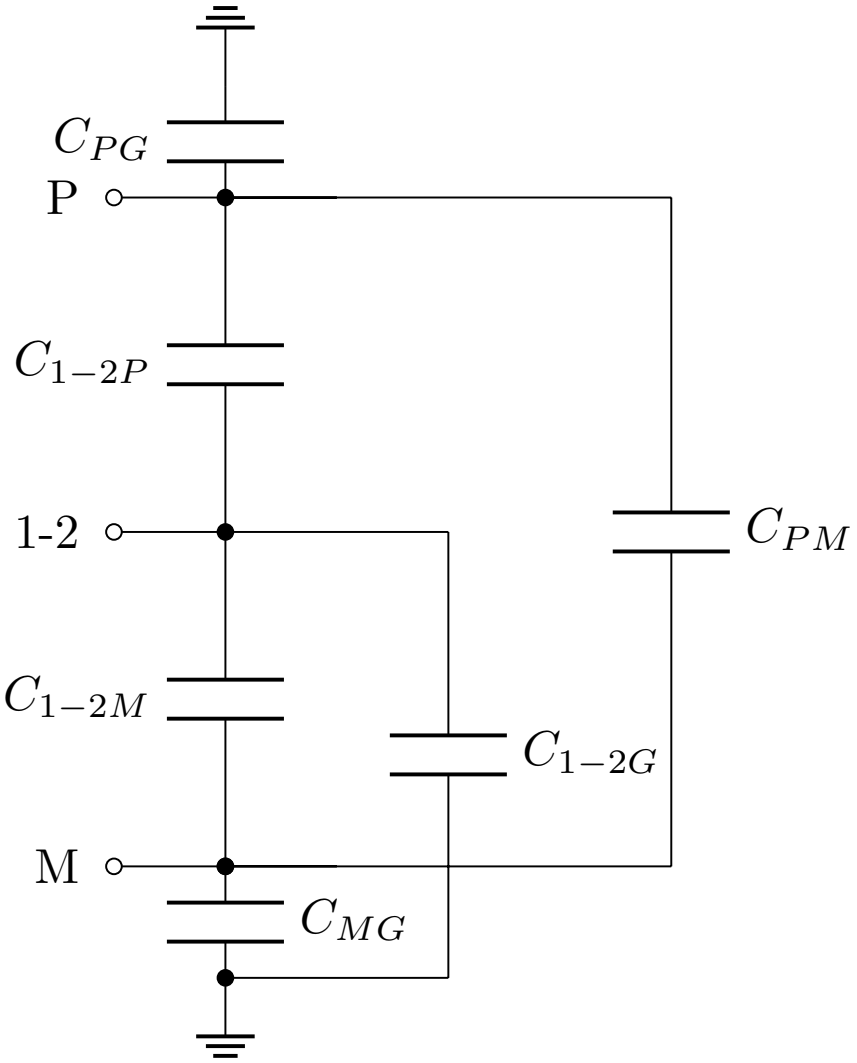


Figure 4.7: Integrated inductor scheme reduced to only electrostatic related elements

The measurement procedure consists of applying the short circuit between terminals (marked by yellow color in Fig.4.8) to cancel some specific capacitances (marked by red color) and measure the others by connecting particular terminals to impedance analyzer (marked by blue color). In this manner, the system of equations is built up, as in equations 4.2. As a result of this step, values of 3 capacitances are calculated - C_{PG}, C_{MG}, and C_{PM}. Remaining equations from 4.2 will be used in further considerations.

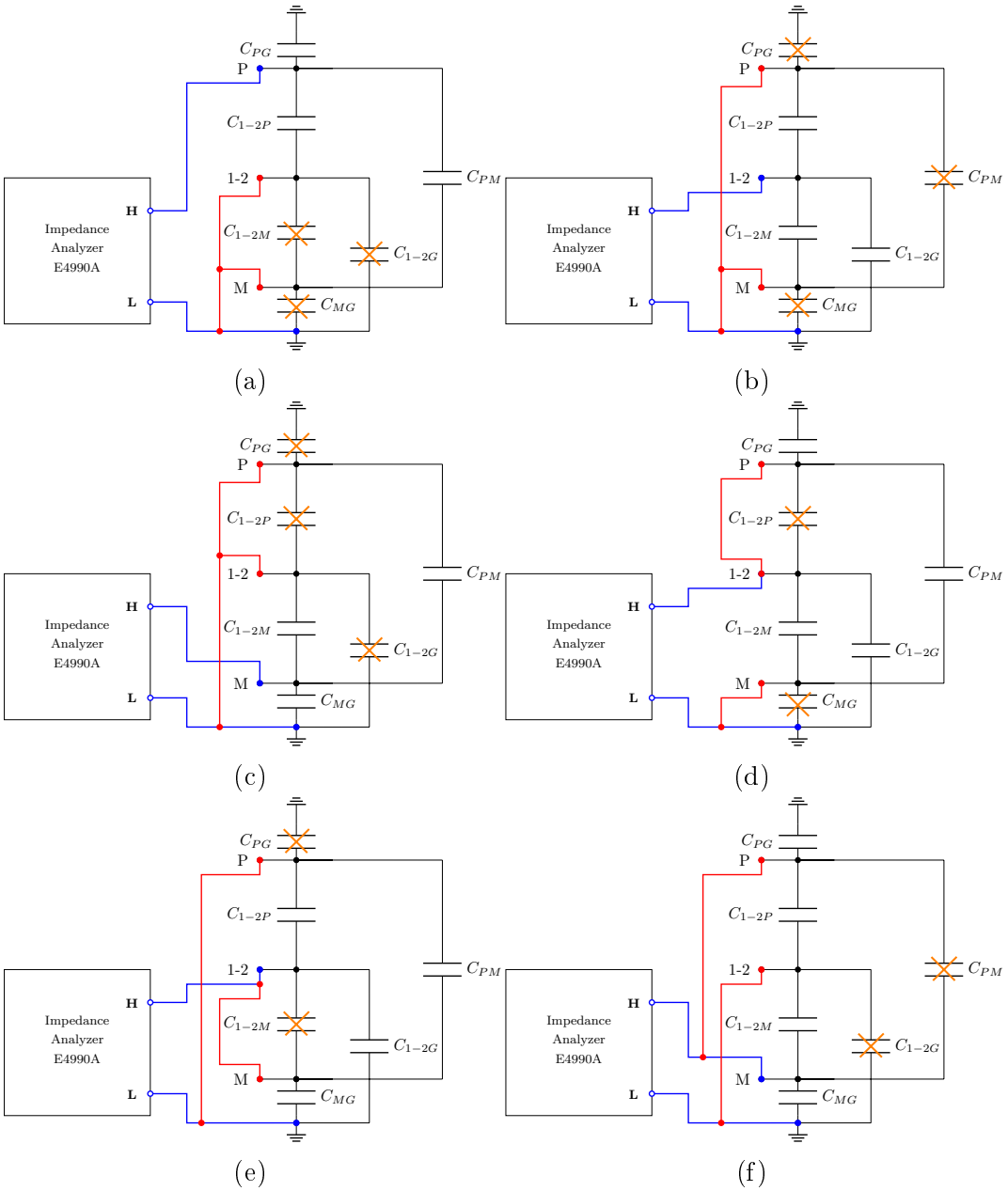


Figure 4.8: Electrostatic measurements configurations

$$\begin{cases} C_{PG} + C_{PM} + C_{1-2P} = 731pF \\ C_{1-2G} + C_{1-2P} + C_{1-2M} = 1,166nF \\ C_{MG} + C_{1-2M} + C_{PM} = 625pF \\ C_{PG} + C_{PM} + C_{1-2M} + C_{1-2G} = 632pF \\ C_{1-2G} + C_{1-2P} + C_{PM} + C_{MG} = 739pF \\ C_{MG} + C_{1-2M} + C_{1-2P} + C_{PG} = 1,301nF \end{cases} \tag{4.2}$$

$$\begin{cases} C_{PG} = 731pF \\ C_{MG} = 625pF \\ C_{PM} = 739pF \end{cases} \tag{4.3}$$

In second step, the system scheme as in Fig.4.6 is considered and resonant frequency method is applied. By making the short circuit (marked by yellow) between some specific terminals of the system, cancellation of particular capacitances (marked by red) is obtained, similarly as in case 1. However, right now, impedance analyzer is connected to 2 ports (marked by blue) and full frequency range of impedance plot is investigated. Then series and parallel resonances are identified on the plot. Based on the resonance frequency, known value of inductance L and specific system capacitances, the equivalent capacitance is calculated to each case. For the presented integrated inductor, 8 measurement setups have been found (Fig.4.9) and the following system of equations has been built (4.4).

$$\begin{cases} C_{2P} + C_{2M} + C_{2G} + C_{12} = 352pF \\ C_{1M} + C_{1P} + C_{1G} + C_{12} = 249pF \\ C_{1M} + C_{12} + C_{2P} + C_{PM} + C_{1G} + C_{PG} = 625pF \\ C_{1G} + C_{MG} + C_{1P} + C_{12} + C_{2M} + C_{PM} = 306pF \\ C_{2G} + C_{PM} + C_{2M} + C_{12} + C_{1P} + C_{PG} = 308pF \\ C_{PM} + C_{2P} + C_{12} + C_{1M} + C_{MG} + C_{2G} = 466pF \\ C_{12} + C_{2P} + C_{2M} + C_{PG} + C_{1G} + C_{MG} = 479pF \\ C_{1P} + C_{1M} + C_{12} + C_{2G} + C_{PG} + C_{MG} = 371pF \end{cases} \tag{4.4}$$

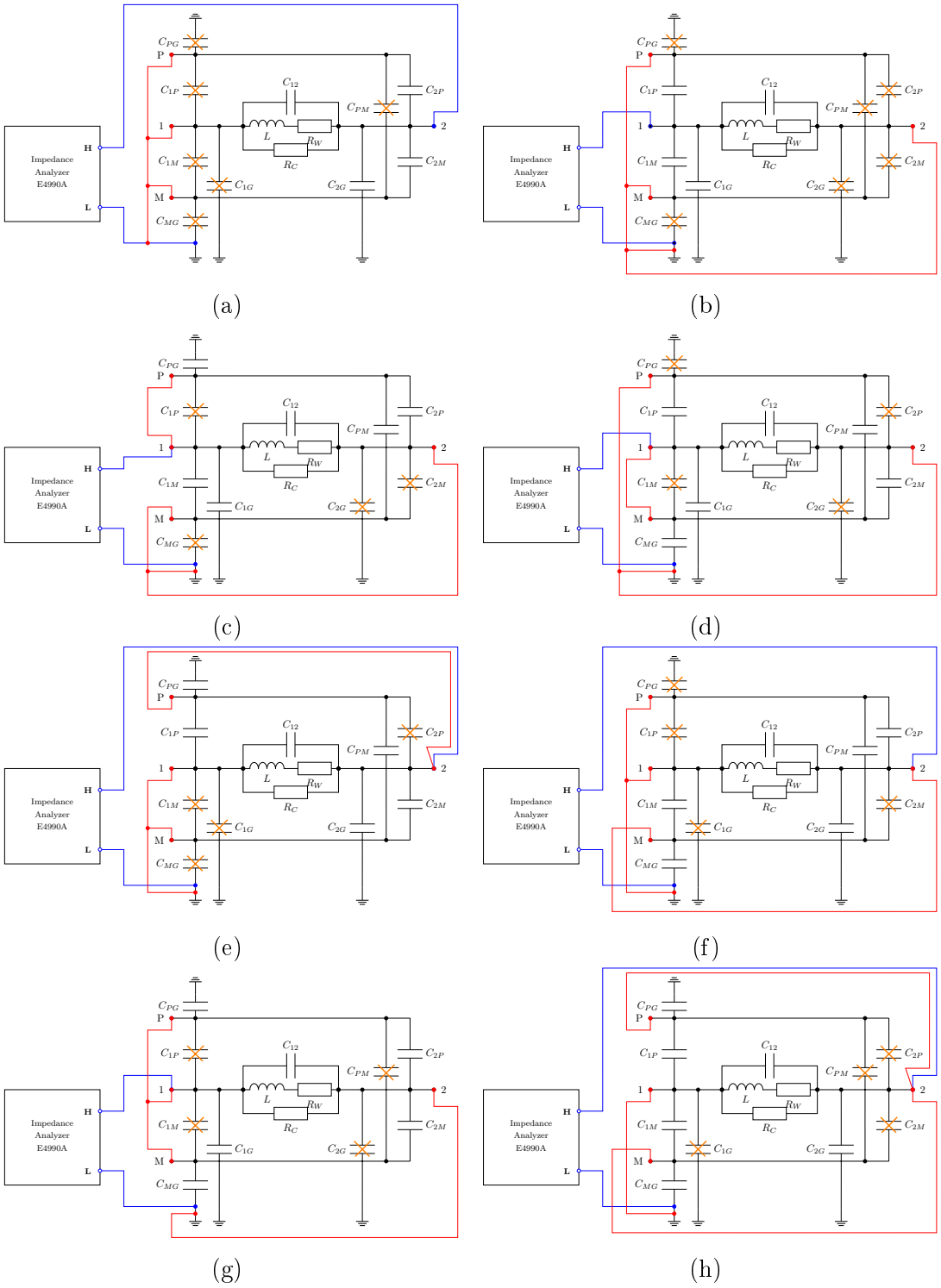


Figure 4.9: Frequency resonant measurements configurations

To calculate values of the whole system, 7 unknown values of stray capacitances must be evaluated. There are 3 equations from electrostatic method and 8 equations from resonant frequency method. To compose the proper system of equations, 7 different equations have to be used. In further consideration, always the 3 equations from electrostatic method are used together with 4 equations from resonant frequency method. Due to the excess number of equations, 10 different options for system of equations have been assembled in Tab. 4.1 and final calculations for each of them are presented in Fig. 4.2.

Table 4.1: Equation choice (10 options) to calculate all capacitances of the Integrated Inductor

Eq. No.	**Resonant Freq.**	**Option**									
		1	2	3	4	5	6	7	8	9	10
1	1.29 MHz	x		x		x	x		x		
2	1.46 MHz	x		x	x			x			x
3	1.16 MHz	x	x		x	x					
4	1.35 MHz	x		x	x	x	x			x	
5	1.35 MHz			x		x	x	x		x	x
6	1.16 MHz		x					x	x	x	
7	1.15 MHz		x					x	x		x
8	1.26 MHz		x		x		x		x	x	x

Table 4.2: Results of calculation (options with 10 capacitances) of an Integrated Inductor.

Capa. name	Option										Avg. val.
	1	2	3	4	5	6	7	8	9	10	
From Electrostatic Method											
C_{PG}						71.52 pF					
C_{MG}						72.08 pF					
C_{PM}						27.3 pF					
From Resonant & Electrostatic Method											
C_{1G}	-7.911 pF	2.713 pF	2.639 pF	11.66 pF	2.639 pF	2.639 pF	4.627 pF	-4.009 pF	2.639 pF	11.66 pF	2.9296 pF
C_{1P}	255.4 pF	246.5 pF	244.9 pF	255.4 pF	244.9 pF	244.9 pF	253.5 pF	246.5 pF	251.5 pF	260.5 pF	250.4 pF
C_{1M}	281.2 pF	277.3 pF	281.2 pF	281.2 pF	270.7 pF	272.2 pF	279.2 pF	270.6 pF	272.2 pF	272.2 pF	275.8 pF
C_{2G}	15.91 pF	5.282 pF	5.356 pF	-3.662 pF	5.356 pF	5.356 pF	3.368 pF	12.0 pF	5.356 pF	-3.662 pF	5.066 pF
C_{2P}	376.9 pF	385.9 pF	387.5 pF	376.9 pF	387.5 pF	387.5 pF	378.8 pF	385.9 pF	380.8 pF	371.8 pF	381.95 pF
C_{2M}	244.6 pF	248.5 pF	244.6 pF	244.6 pF	255.2 pF	253.7 pF	246.6 pF	255.3 pF	253.7 pF	253.7 pF	250.05 pF
C_{12}	-285.9 pF	-301.6 pF	-285.9 pF	-305.5 pF	-296.5 pF	-294.9 pF	-294.5 pF	-301.6 pF	-301.6 pF	-301.6 pF	-296.96 pF
Error(avg.)	5.89675 %	4.45375 %	4.18675 %	5.614 %	76.0215 %	2.88825 %	126.6698 %	5.037 %	34.823 %	5.76325 %	1.317 %
						Selected					

Divergence of data presented in Table 4.2, which can be observed in error varying from 1.3% up to 126,7%, indicates problems with stability of the identification process. After deep insight into the model, author identified the possibility of reducing the stray capacitance quantity up to 7 without losing physical sense of the model. The C_{1G} & C_{2G} and C_{PM} can be neglected. In the most simplified interpretation, given ideal shielding of the P and M conductors, C_{1G} and C_{2G} are eliminated by shield planes on the outer layers, and the winding tracks cancel out C_{PM}. However, the perfect case has never existed, so the values of C_{1G}, C_{2G}, and C_{PM} can be considered as part of other capacitance values.

The new iteration of electrostatic + resonant frequency method has been performed for the system with the 7 stray capacitances and one inductance, as presented in Fig. 4.10.

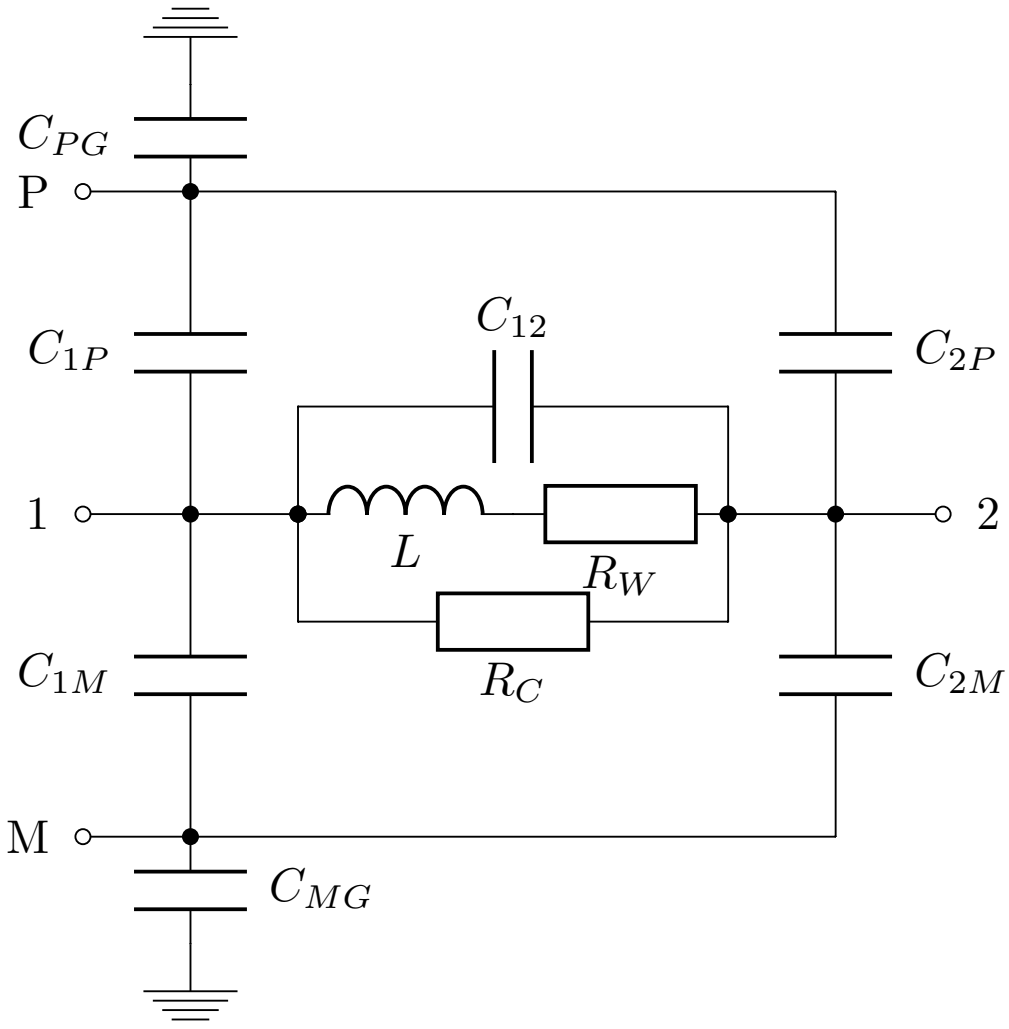


Figure 4.10: Integrated Inductor model scheme with 7 stray capacitances

Characterization process of 7 stray capacitances has been described in Appendix E. Final parameters of the model are presented below in the Table 4.3. The listed negative value of capacitance C_{12} is not an error - it should be understood as negative capacitive coupling, as well as negative mutual inductance. Inductance L shown in the Table 4.3 is the average of individual inductance measurements made using the resonant frequency method. For each instance, the inductance value was measured for a specific resonant frequency. Thus, presented L value is the average of 8 values from the measurements shown in Fig. E.4 presented in Appendix E.

Table 4.3: Final parameters of Integrated Inductor model

Parameter	**Value**
C_{1P}	240 pF
C_{1M}	266 pF
C_{2P}	392 pF
C_{2M}	268 pF
C_{PG}	99 pF
C_{MG}	91 pF
C_{12}	-194 pF
L	42,97 μH
R_W	74,6 $m\Omega$
R_C	3,8 $k\Omega$

4.4 Integrated Inductor topology – simulation study

Previously presented results of EMI spectra (in Chapter 3) clearly indicate that the load impact is not neglectible. Thus, in chapter 3.2 all measurements have been conducted with the Common-Mode Choke between inverter leg and the load. Moreover, additional effort has been put to the test bench configuration, to limit the load impact on generated EMI as much as possible (e.g. placing the load resistor on the special construction, very far from the ground).

In the design steps of power converters there are some unbreakable rules that must be fulfilled to prevent unwanted and harmful phenomena inside device.

One of these rules is placing decoupling capacitors. They should be placed as close as possible to inverter leg, made by capacitors with extremely low ESR and ESL. The best designs integrate decoupling capacitors inside power modules. By these actions, the power loop inductance is reduced and unwanted oscillations and overshoots are dumped and limited to minimum.

By this research, it is proposed, similarly to decoupling capacitors, a new unbreakable rules: integration of inductor to the inverter leg by connecting the passive component to the middle point. In this way, the CM noise (mainly) is blocked at that point and does not leak from converter into the load. Together with very good layout of converter it provides enhanced EMI performance of converter. However, the question is: how to provide a design of this inductor with respect to the stray capacitance behavior: should it be shielded in order to provide built in C_Y, or not to reduce possible HF propagation path through shields?

A few different topologies have been proposed and their impact have been tested in the simulation study (Fig.4.11). The simulation study is coherent with previously presented models of transistors and PCB layouts. Simulation model based on Power-Chip-on-Chip layout (ANSYS model of this layout) is processed in Saber simulator and time-domain simulation is performed.

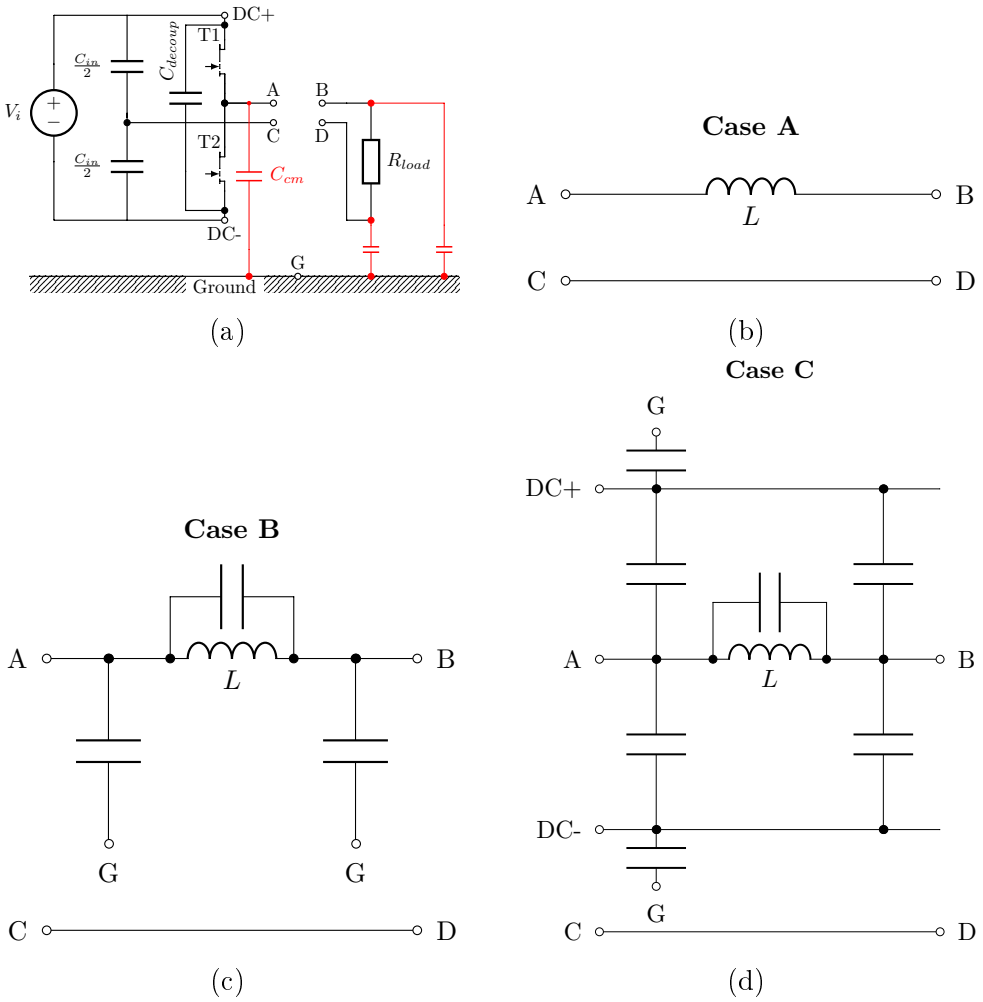


Figure 4.11: Investigation of proper topology of output inductor for inverter leg: a) Time-domain simulation circuit; b) Case A - ideal inductor; c) Case B - unshielded integrated inductor model with stray elements; d) Case C - shielded integrated inductor model with stray elements

First considered situation of placing the perfect inductor without any stray elements (case A) - it gives the reference point of generated CM and DM noise. Case B is representing the classical wire wound inductor with stray capacitances across wounds and to the ground. Case C presents the integrated inductor, with the model and values determined as described in chapter 4.3, where shields are connected to DC+ and DC- constant bus-bar potentials.

Based on simulation study the transfer function of $\frac{I_{cm}}{V_{T1}(\omega)}$ and $\frac{I_{dm}}{I_{T1}(\omega)}$ have been calculated and are presented in Fig.4.11, where $V_{T1}(\omega)$ is a drain-source voltage of high-side transistor T1 and $I_{T1}(\omega)$ is its drain current, both in the frequency domain.

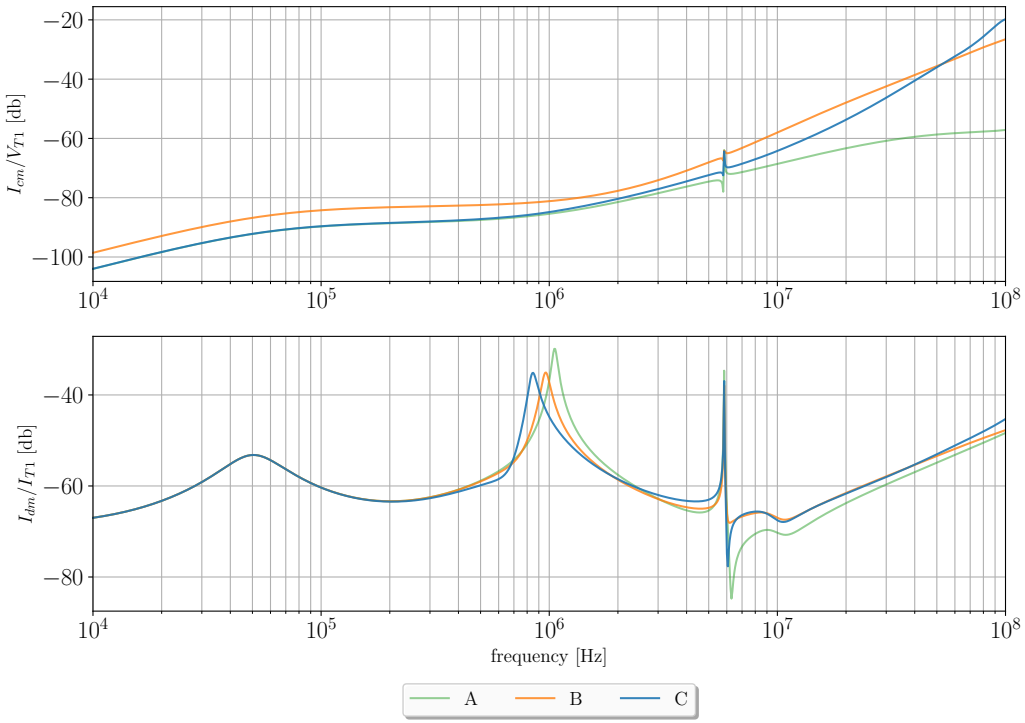


Figure 4.12: Transfer functions of I_{cm} and I_{dm} for the topologies of inductor: Case A-B-C

The transfer function allows to determine how interference are propagated from the source (in this case, the transistor T1) to the currents measured on the LISN. Comparing $\frac{I_{cm}}{V_{t1}(\omega)}$ for three cases, it can be concluded that in the frequency range up to 10 MHz, in circuit with shielded integrated inductor (case C), common mode current is transferred as in circuit with ideal inductor (case A), and is about 5 dB lower than in circuit with unshielded Integrated Inductor (case B) which indicates effectiveness of shielding and filtering properties of parasitic capacitances inside the integrated inductor. In the band above 10 MHz, filtering still takes place, but not as effectively because there is an effect of capacitances to the ground. Above 50 MHz, they play a dominant role and the I_{cm} currents are not filtered.

In the case of $\frac{I_{dm}}{I_{T1}(\omega)}$, an impact of the inductor is not so visible - it can be noticed a slight change in the resonant frequencies and the level around 10 MHz.

This analysis shows that the most promising topology of output EMC filter for inverter leg is the case C - for the CM current attenuation. However, the most trustful comparison is carried out with spectra of CM and DM noise of each case. To present it, the time domain simulation have been made for each case and then the FFT analysis made and plotted. Fig. 4.13 shows the comparison of CM and DM spectra (case A-B-C). Clearly the lowest EMI generation is obtained for the Case A - ideal inductor. It is due to the lack of stray elements through which the noise current is flowing to the load. When these parasitics are taken into consideration - the EMI generation is higher and significant amount of noise current is flowing through load. These phenomena are shown in case B. Results of case C shows that applying the Integrated Inductor with built-in shields can improve the performance of converter and limit the noise going out of converter so CY are effective.

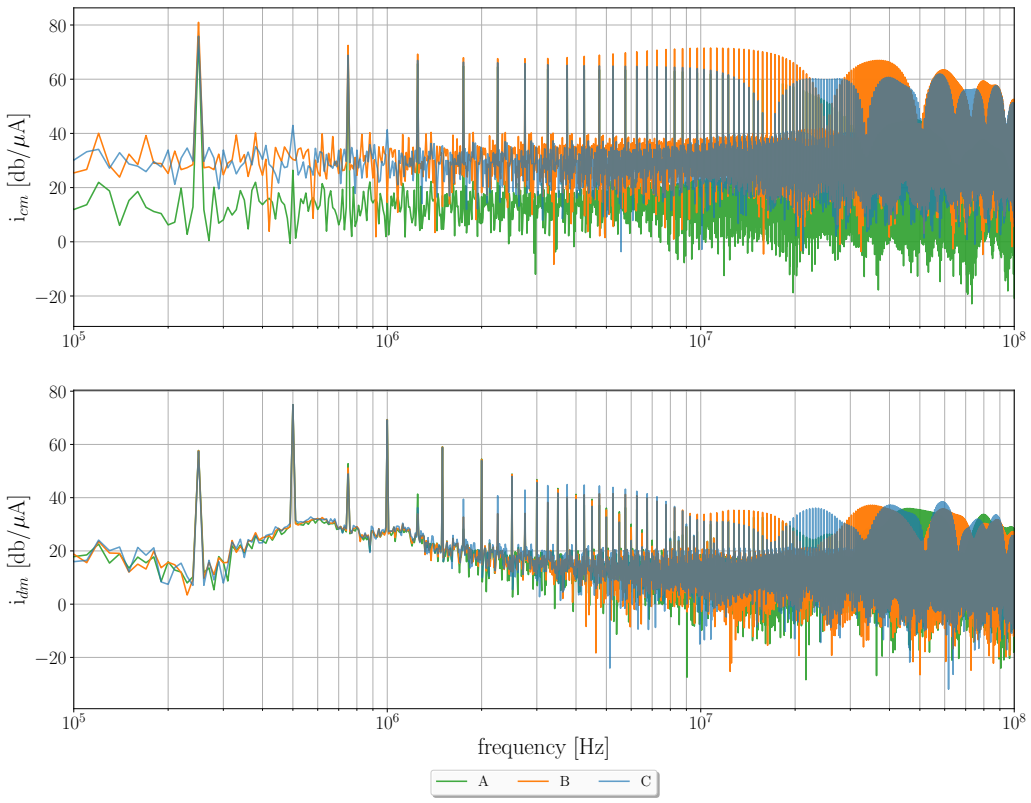


Figure 4.13: DM and CM spectra of Case A-B-C

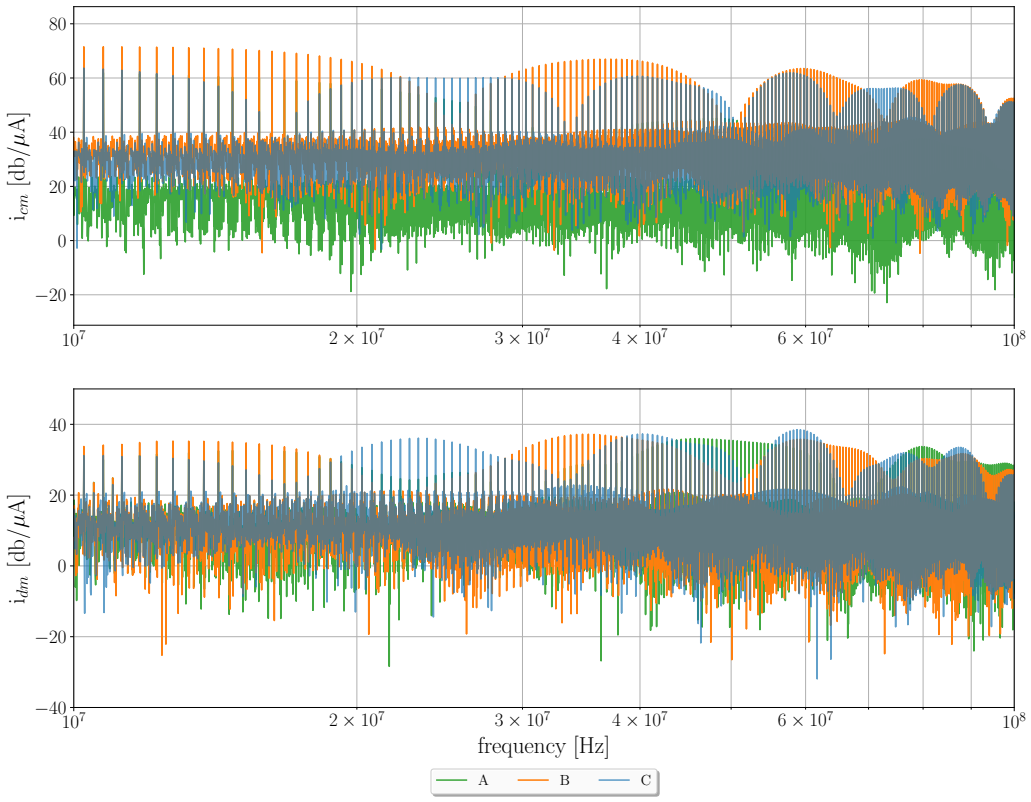


Figure 4.14: DM and CM spectra of Case A-B-C: zoom 10 MHz - 100 MHz

In this specific case, it is evident that the application of shielding engenders a reduction in the amplitude of common mode interference across the complete spectrum of frequencies, especially beyond the threshold of 10 MHz. Only in a narrow range for about 25 MHz in the circuit without shielding, the level of I_{cm} is lower as a result of shifting peaks associated with resonances as is shown in Fig. 4.14. The use of shielding has little effect on the level of I_{dm}.

An interesting comparison is shown in Figure 4.15. It compares the simulation results of a half-bridge inverter with no inductor between the bridge output and the load with the case where an ideal inductor is placed. The comparison shows directly how much the magnetic element prevents the flow of CM currents through the parasitic capacitances of the load. There is a reduction of 5 dB to more than 15 dB over the entire frequency range. Differential distortion is also significantly reduced over the entire measurement range.

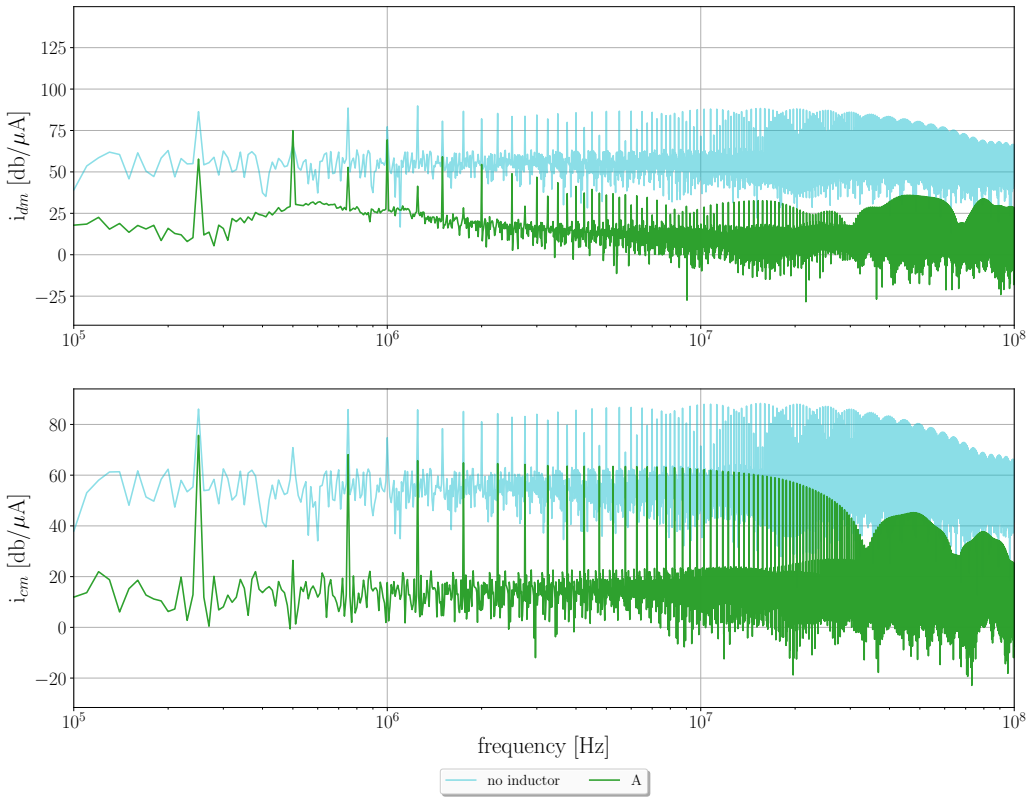


Figure 4.15: Comparison of DM and CM spectra for a case with no inductor and Case A

4.5 Integrated Inductor - conclusions

In this chapter, the concept of decoupling inductor built inside of power module has been presented and its purpose motivated. Design for this inductor has been proposed with a special attention to high frequency magnetics requirements. Then, the model scheme and characterization method has been presented. The concept was validated by simulations. Adding the Integrated Inductor limits the CM noise generation. Moreover, shielding of inductor looks promising in terms of common-mode noise reduction.

The special design of decoupling inductor as a planar inductor, embedded in 3D arrangement of power switches (as in Chapter 3) enables creation of the new generation of power module. The shielding concept can be effectively introduced to this power module due to flat and symmetrical design. These features (including decoupling capacitors) would enable clean switching performance with reduced

EMC problems.

In future work, different configurations of Integrated Inductor or CM Choke will be investigated. Also, the characterization methods will be compared and developed to obtain fast and more accurate identification. The next perspective for future research is a serious problem of saturation of a single inductor core, since the load LF current is not compensated as it would be in a CM choke filter.

Chapter 5

Conclusions and perspectives

"One never notices what has been done;
one can only see what remains to be done."
Maria Curie-Skłodowska

5.1 Conclusions

The research presented in this dissertation focuses on EMI mitigation in power electronic converters using GaN transistors. GaN devices are featured by the ability to operate at high switching frequencies and high switching speed (high $\frac{dv}{dt}$ and $\frac{di}{dt}$), making parasitic elements key factors for generated EMI and electrical performance. The study presented here describes the possibilities to reduce EMI through hardware (layout and Integrated Inductor) and software (control strategy) modifications.

The software approach to EMI reduction is to customize the control strategy for a given converter and use (if possible) resonant, quasi-resonant, etc. conditions to achieve soft switching. ZVS or ZCS ensures that at least one sub-period of the converter's operation does not experience high voltage or current rise/fall edges, leading to a reduction in the generated disturbances. Based on the buck converter, it has been proven that such a control change can be implemented without hardware modifications (assuming the construction of the converter is based on the standard building block - the inverter leg). As a result, significant attenuation of common mode EMI emissions has been achieved with a slight increase in power conversion efficiency. Significant overvoltages caused by the relatively high value of the power loop inductance were also observed during the study. However, in order to fully exploit the fast switching capability of GaN HEMTs, the recommendation of the ZVS topology cannot be a sufficient condition, but must be accompanied by a circuit design layout that ensures extremely low parasitic inductances of the commutation power loop - as discussed in Chapter 3.

Regarding CM interference, reduction of the middle point capacitance to the ground is crucial, because this capacitance (floating point capacitance) is the decisive factor causing interference. To achieve this goal, the shielding concept presented in Chapter 3 has proven its effectiveness. A shielding concept (sandwich stack-up) has been improved by a more symmetrical layout brought by the PCoC concept, where a better CM mitigation has been demonstrated together with a radical reduction of the power loop inductance ($C_{cm} = 0.68\,pF$: capac-

itance of the middle point to ground; $L_s = 1.49\,nH$ [$2.29\,nH$ considering the inductance inside the package of two GaN transistors]). Such low values of parasitic elements prove a very good EMC optimization of the converter layout and are better than in publications: [58, 38, 46]. Furthermore, it has been shown that not only the power layout has to be considered, but also the gate drivers and the thermal pads. In these areas the stray CM capacitance is distributed and must be decreased as much as possible.

Finally, concept of the decoupling inductor was introduced, and a promising planar inductor technology was introduced to filter CM emission at source. A fabrication process and a methodology for characterizing the device, including parasitics, have been developed, allowing verification of its performance by simulation. Shielding of this planar PCB inductor appears attractive due to built-in Cy function capacitors (CM current internal recycling - analogy to power layout shielding). A major disadvantage of a single CM inductor is the low-frequency current of the load, which may lead to saturation of the core, since the LF current of the load is not compensated. This effect could be eliminated by using a coupled inductor (canceling the internal flux density). This would also symmetrize the propagation path and help reduce DM noise.

5.2 Perspectives

The achievements presented in the thesis provide a good basis for further research, and the author's proposed directions are:

- To investigate the effect of ZVS and ZCS on the generated EMI in other types of converters than Buck controlled by TCM method,
- The multi-platform simulation workflow in Digital Twin can be widely used for EMC analysis of various types of power electronic converters, and is a good method for design verification at the early design stage (before device production),
- The effectiveness of the shielding concept and the PCoC should be tested

in a multi-branch converter (e.g., a three-phase or multi-phase inverter) to determine the exploration of design constraints in structures with many such elementary building blocks,

- Concepts of shielding and PCoC, due to its advantages, can be successfully implemented in many power electronic converter topologies. Of particular interest is the implementation of the above concepts within commercial power modules,

- The characterization methods could be compared and further developed for faster and more accurate identification,

- To determine the best solution for EMI suppression flowing through the load, other Integrated Inductor topologies should be considered, such as: two single inductors: on the positive and negative wires of the load, two inductors magnetically coupled together and enclosed in one PCB, different couplings of these inductors, and etc,

- The integrity of the Integrated Inductor inside a commercial power module with GaN transistors is also an interesting prospect.

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Appendices

Appendix A

Published Papers

- Paweł Derkacz and Piotr Musznicki. Gate driver with overcurrent protection circuit for gan transistors. *Przegląd Elektrotechniczny*, (2):125-128, 2019.
- Pawel B Derkacz, Piotr Musznicki, and Piotr J Chrzan. Emi attenuationin a dc-dc buck converter using gan hemt. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 9(4):4146-4152, 2020.
- Pawel B. Derkacz, Jean-Luc Schanen, Pierre-Olivier Jeannin, Piotr Musznicki, Piotr J. Chrzan, and Mickael Petit. 3d pcb package for gan inverter leg with low emc feature. pages P.1-P.10, Lyon, France, 2020. IEEE.
- Piotr Musznicki, Pawel B. Derkacz, and Piotr J. Chrzan. Wideband modeling of dc-dc buck converter with gan transistors. *Energies*, 14(4430):4430,07 2021.
- Pawel B. Derkacz, Jean-Luc Schanen, Pierre-Olivier Jeannin, Piotr J.Chrzan, Piotr Musznicki, and Mickaël Petit. Emi mitigation of gan power inverter leg by local shielding techniques. *IEEE Transactions on Power Electronics*, 37(10):11996-12004, 2022.

Appendix B

Behavioral model of GaN transistor in the MAST language

```
#<<---Descriptive Name---
# gs66508t_new4
#>>
#<<---Short Description---
# This MOSFET model was generated with the Model
   Architect Power MOSFET tool 1.1.
#>>
#<<---Long Description---
# The model "gs66508t_new4" is a N-channel power MOSFET
   model with the following features:
# @channel-length modulation
# @non-linear inter-electrode capacitances Cgd, Cgs and
   Cds
# @body diode without reverse recovery
# @statistical variability
#>>
#<<---Usage Notes---
#
# Please refer to the MOSFET tool documentation for more
   information regarding
# model characterization and usage.
#>>
encrypted element template gs66508t_new4 d g s = mosfet,
   cap, diode, tol, mc, ratings, rth_ja, rth_jc, rth_hs,
   part_type, part_class

#<<---Connections---
electrical d  # Drain (units:V)
electrical g  # Gate (units:V)
electrical s  # Source (units:V)
#>>

#<<---Parameters---
struc {
    number tempj  = 25,        # Reference temperature (
       units:C)
           vt     = 3.36,      # Vgs threshold voltage (
```

```
            units:V)
            rds     = 10m,        # Drain-source on-
               resistance (units:Ohm)
            a       = 15.13,      # Parameter for DC
               characteristic (units:-)
            b       = 150,        # Parameter for DC
               characteristic (units:-)
            c       = 27,         # Parameter for DC
               characteristic (units:-)
            d       = 2.82,       # Parameter for DC
               characteristic (units:-)
            e       = 504,        # Parameter for DC
               characteristic (units:-)
            f       = 0.8,        # Parameter for DC
               characteristic (units:-)
            x       = 5.17m,      # Parameter for DC
               characteristic (units:-)
            y       = 1.5,        # Parameter for DC
               characteristic (units:-)
            z       = 2.92,       # Parameter for DC
               characteristic (units:-)
            alpha   = 1066,       # Parameter for DC
               characteristic (units:-)
            vaf     = 203,        # Early voltage associated
                with channel-length modulation (units:V)
            rg      = 1,          # Internal gate resistance
                (units:Ohm)
            roff    = 1meg        # Parallel off-resistance
               representing leakage current (units:Ohm)
} mosfet[*] =
   [(25,1.547,0.03550169,15.41675,0.008630489,76.78599,0.5805324,3.83
   meg)]

struc {
    number crss0 = 11.56n,     # Reverse transfer
       capacitance for vds=0 and vgs=0 (units:F)
            crss1 = 3.22n,     # Reverse transfer
               capacitance for vds=v1 and vgs=0 (units:F)
            crss2 = 580p,      # Minimum reverse transfer
               capacitance value (units:F)
            coss0 = 19.57n,    # Output capacitance for
               vds=0 and vgs=0 (units:F)
            coss1 = 4.51n,     # Output capacitance for
               vds=v1 and vgs=0 (units:F)
            coss2 = 606p,      # Minimum output
               capacitance value (units:F)
            ciss0 = 13.96n,    # Input capacitance for vds
               =0 and vgs=0 (units:F)
            v1    = -0.39,     # Positive vds voltage
               corresponding to point (crss1,v1) on Crss
               curve (units:V)
            v2    = 0.74,      # Positive vds voltage
               corresponding to point (crss2,v2) on Crss
               curve (units:V)
            m     = 0.5248,    # Capacitance exponent (
               units:-)
            vgs0  = -5         # Negative gate voltage
               knee of non-linear Cgs (units:V)
} cap = (84.5p,19.4p,7.9p,1.52104847n,195.5p,86.1p,341.3p
   ,17.5,150.6,0.1819701,-1.593769)

struc {
```

```
    number tempj  = 25,       # Reference temperature (
       units:C)
           ron    = 0.01,     # Diode on-resistance (
              units:Ohm)
           vd     = 0.7,      # Voltage where diode turns
               on (units:V)
           n      = 10        # Stiffness factor for the
              transition between ron and roff (units:-)
} diode[*] = [(25,0.1089388,1.720482,9.710729)]

# Lead inductances
struc {
    number ld = 0,            # Drain inductance (units:H
       )
           ls = 0,            # Source inductance (units:
              H)
           lg = 0             # Gate inductance (units:H)
} ind = (0.4n,0.1n,1n)

# Tolerance ratings
struc {
    number vt  = 0.1,  # Tolerance on threshold voltage
           rds = 0.1,  # Tolerance on Rds (current
              scaling)
           qg  = 0.1,  # Tolerance on gate charge (
              capacitance scaling)
           rg  = 0.1,  # Tolerance on Rg
           vd  = 0.1,  # Tolerance on diode threshold
              voltage
           ron = 0.1   # Tolerance on diode on-resistance
} tol = (0.3,0.3,0.3,0.3,0.3,0.3)

mtype..mc mc = yes   # Enable variability in Monte Carlo
   analysis

# Stress ratings
struc {
    number tjmax    = undef, # Max. temperature rating (
       units:C)
           tjmin    = undef, # Min. temperature rating (
              units:C)
           pdmax_jc = undef, # Max. power diss. junction
              to case (units:W)
           pdmax_ja = undef, # Max. power diss. junction
              to ambient (units:W)
           vdsmax   = undef, # Max. drain-source voltage
              (units:V)
           vgsmax   = undef, # Max. gate-source voltage (
              units:V)
           idmaxavg = undef, # Max. average continuous
              drain current (units:A)
           idmax    = undef  # Max. instantaneous drain
              current (units:A)
} ratings = ()

# Static thermal heatsink resistances
number rth_ja = undef,  # Junction to ambient
       rth_jc = undef,  # Junction to case
       rth_hs = undef   # Junction to heat sink

string part_type = "MOSFET"
string part_class = "generic"
```

```
#>>

#<<---Global Declarations---
external number temp, include_stress
#>>
#<<---Exported Post-Processing---
export val i imos   # MOSFET DC current
export val q qds    # MOSFET drain-to-source charge
export val q qdg    # MOSFET drain-to-gate (Miller)
   charge
export val q qgs    # MOSFET gate-to-source charge
export val p pwrd   # Instantaneous power dissipated in
   both MOSFET and diode
export val tc tempj # Junction temperature
export val i idiode # Diode current
#>>
{
    electrical di, gi
    foreign mos1, tlu_map, tlu
    number tempj_tnom = 25  # Nominal temperature for
       stress measures
    number rth_eff          # Final value of thermal
       resistance
    number pdmax            # Final value of power
       dissipation rating

    number scale_vt, scale_rds, scale_rg, scale_cap,
       scale_vd, scale_ron
    number xvdsmax, xvgsmax, xidmax, xidmaxavg, xtjmax,
       xtjmin

    # TLU arrays for diode model parameters
    number vd_[*], ron_[*], n_[*]
    number math_pi = 3.14159265358979323846, vgs_delta =
       1
    number interpol = 0, extrapol[2] = [0, 0]
    number rg, roff

    number coefd, vd_th, n_eff
    number gon, goff, vd, ron, n
    number ns[*]
    number cds0, cds1, cds2, phids, slopeds, qoffsetds
    number cdg0, cdg1, cdg2, phidg, slopedg, qoffsetdg
    var i id              # Drain current (units:A)
    var i ig              # Gate current (units:A)
    val v vgs,            # MOSFET gate-to-source voltage:
        v(g,s) (units:V)
          vds,            # MOSFET collector-to-emitter
             voltage: v(d,s) (units:V)
          vdsi,           # Internal MOS drain-to-source
             voltage: v(di,s) (units:V)
          vgsi,           # Internal gate voltage
             controlling MOS current: v(gi,s) (units:V)
          vdgi            # Voltage across Miller
             capacitance: v(di,gi) (units:V)
    val c cdg,            # Miller capacitance (units:F)
          cds,            # Drain-to-source capacitance (
             units:F)
          cgs,            # Non-linear Cgs capacitance (
             units:F)
          crss,           # cdg (units:F)
          coss,           # cdg+cds (units:F)
```

```
        ciss            # cdg+cgs (units:F)
    val p pwrd_mos      # Instantaneous power dissipated
        in MOSFET (units:W)
    val p pwrd_diode    # Instantaneous power dissipated
        in diode (units:W)
    val v vdiode        # Diode forward voltage v(s) - v
       (di) (units:V)
    val i idfwd         # Diode forward current (units:A
       )
    #>>

    #<<---Group Definitions---
    group {id, vgs, vds, cdg, cds, cgs, crss, coss, ciss}
        mos_group
    #>>
!crypt_start
}
```

Appendix C

Schematic of the simulation circuit

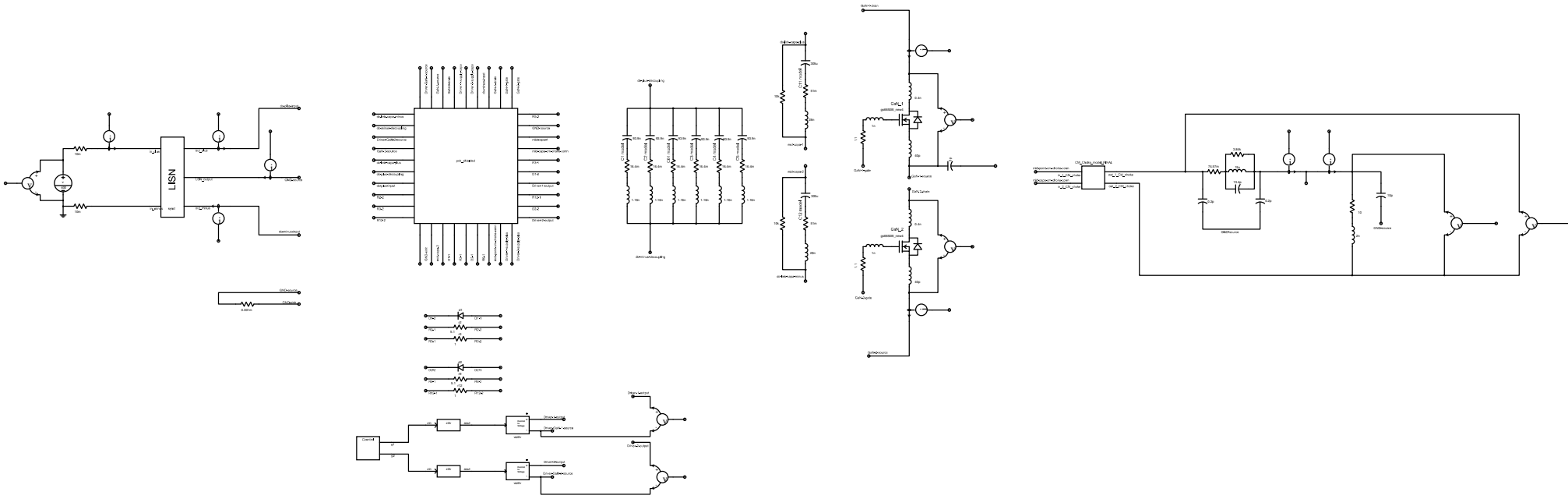


Figure C.1: Converter simulation schematic

Appendix D

LISN - Model Circuit Diagram

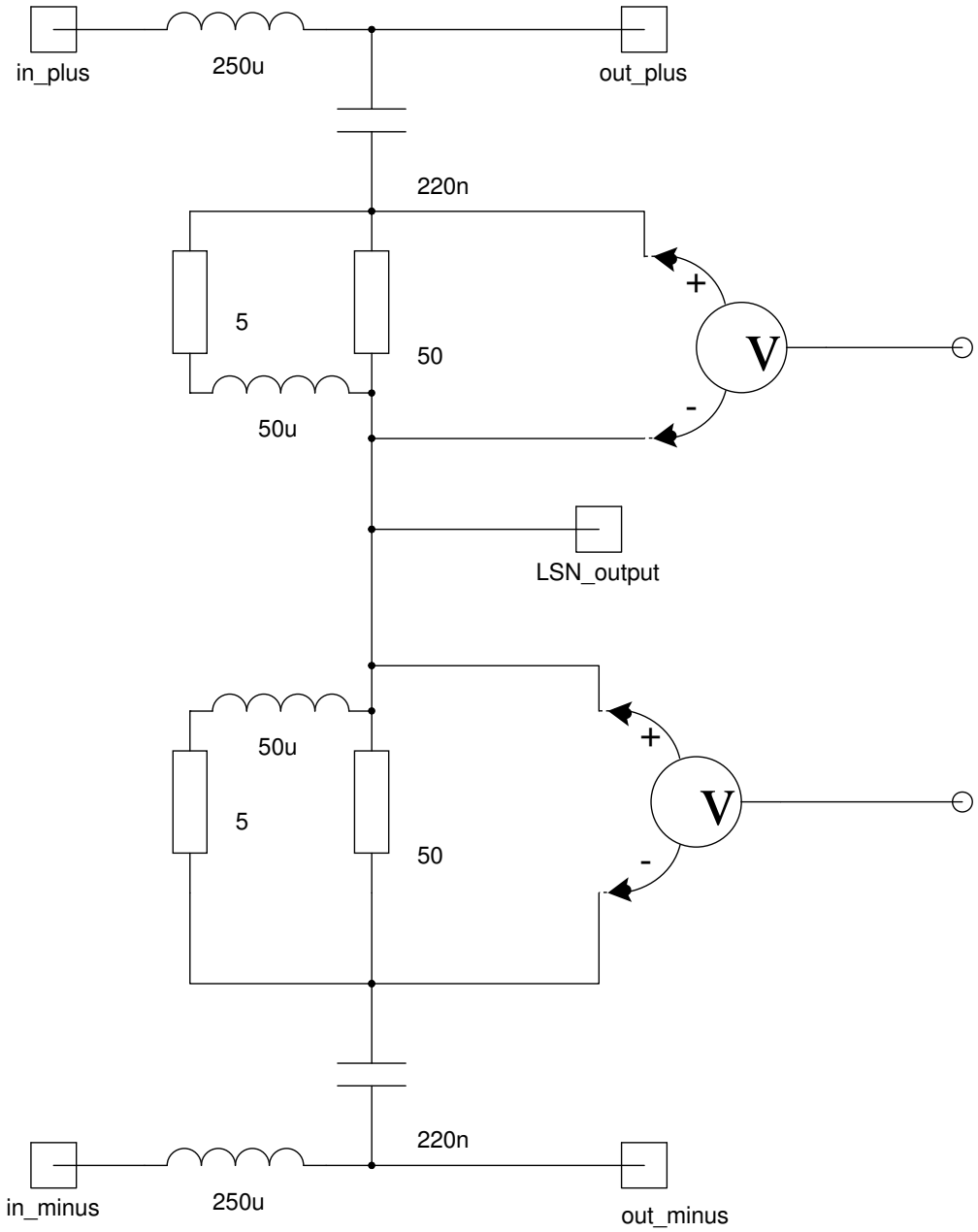


Figure D.1: Line Impedance Stabilization Network schematic

Appendix E

Integrated inductor characterization: Model with 7 stray capacitances system characterized by Electrostatic & Resonant frequency Method (E&RM)

The new iteration of Electrostatic & Resonant frequency Method in assumptions has the same procedure of measurements as in Chapter 4.3 to identify values of stray capacitances. However, in the considered characterization, the system is reduced to 7 stray capacitances, one inductance and two resistances, as presented in Fig.E.1.

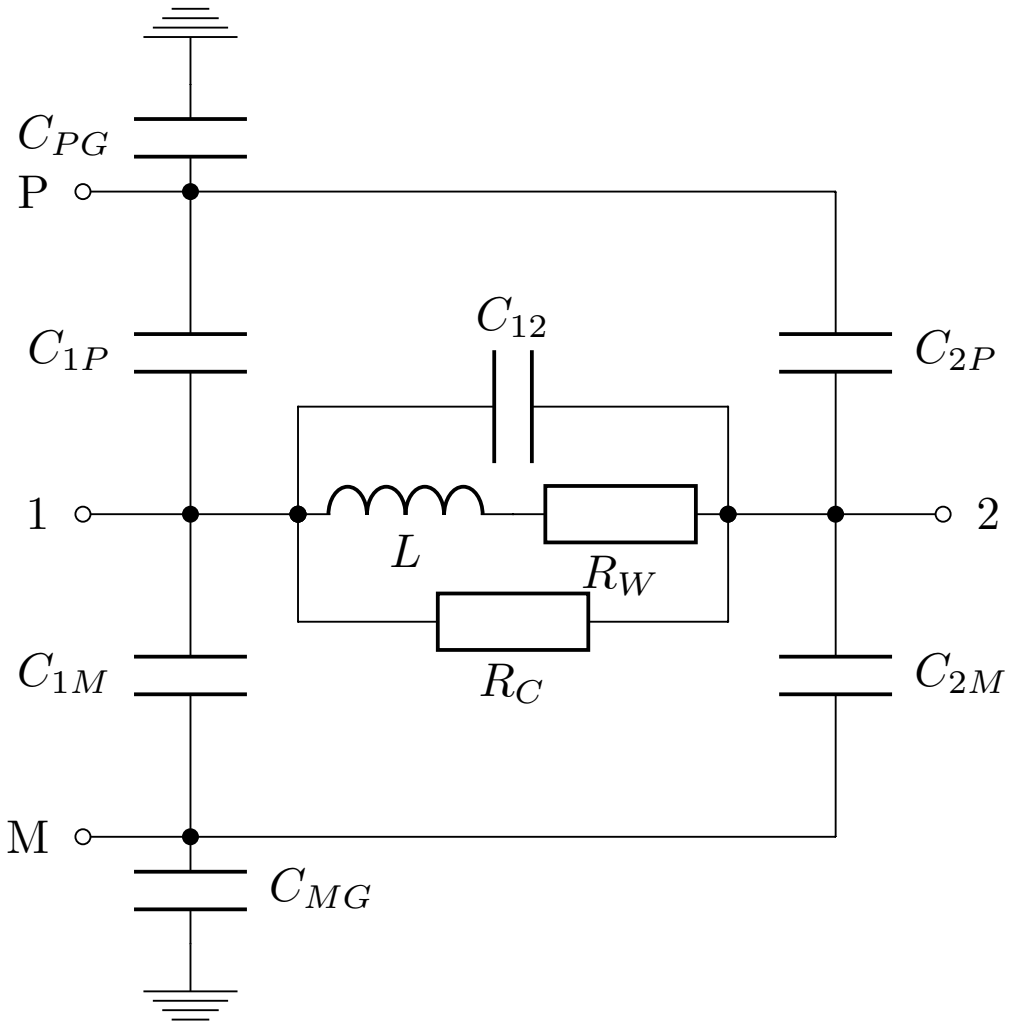


Figure E.1: Integrated inductor model with 7 stray capacitances

Comparing to 10 stray capacitances model, in the new model (as in Fig.E.1) C_{1G} & C_{2G} and C_{PM} can be neglected because its value can be taken into account as a part of other capacitance values. Thus, their existence in the model can be considered redundant. In the first part of measurements, the electrostatic method is used where it is assumed the short circuit of node 1 and 2. Then, the system can be presented as on Fig.E.2.

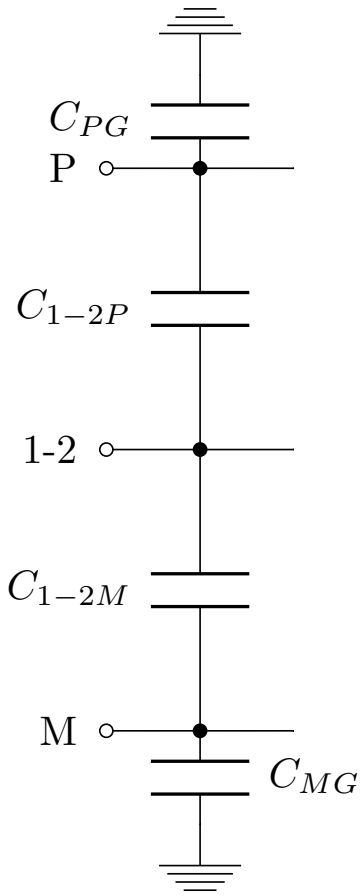


Figure E.2: Model scheme for electrostatic measurements (with shorted nodes 1 and 2)

All possible measurement configurations are presented on Fig.E.3. First 4 setups have been used to create system of equations (as presented in E.1) and calculate values of stray capacitances. Then, the measurement result of 5th configuration has been used to compare it with calculated values for determination of calculation error which is 2.1%.

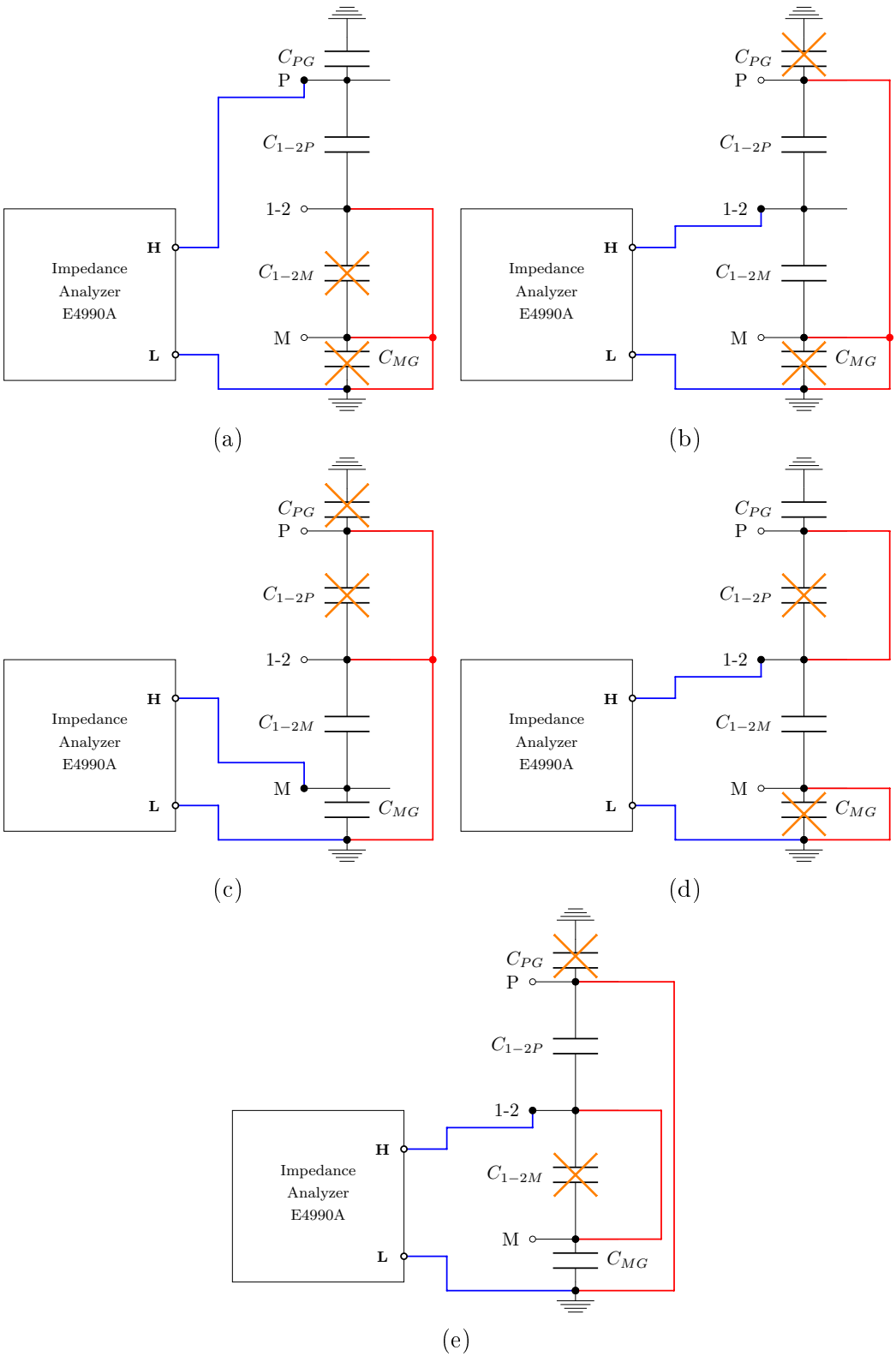


Figure E.3: Electrostatic measurements configurations

$$\begin{cases} C_{PG} + C_{1-2P} = 731,15pF \\ C_{1-2P} + C_{1-2M} = 1,1662nF \\ C_{MG} + C_{1-2M} = 625,25pF \\ C_{PG} + C_{1-2M} = 632,68pF \end{cases} \tag{E.1}$$

$$\begin{cases} C_{PG} = 98,81pF \\ C_{MG} = 91,38pF \\ C_{1-2P} = C_{1P} + C_{2P} = 632,3pF \\ C_{1-2M} = C_{1M} + C_{2M} = 533,9pF \end{cases} \tag{E.2}$$

In the second step, respectively as in Chapter 4.3 the resonant frequency method has been used to complete missing equations in the system of equations to calculate all values of parasitic capacitances. The series and parallel resonances are identified on the plot. Based on the resonance frequency, known value of inductor L and specific and known capacity system, the substitution capacity is calculated to each case. All determined setups are presented in Fig.E.4 and following system of equations have been build E.3.

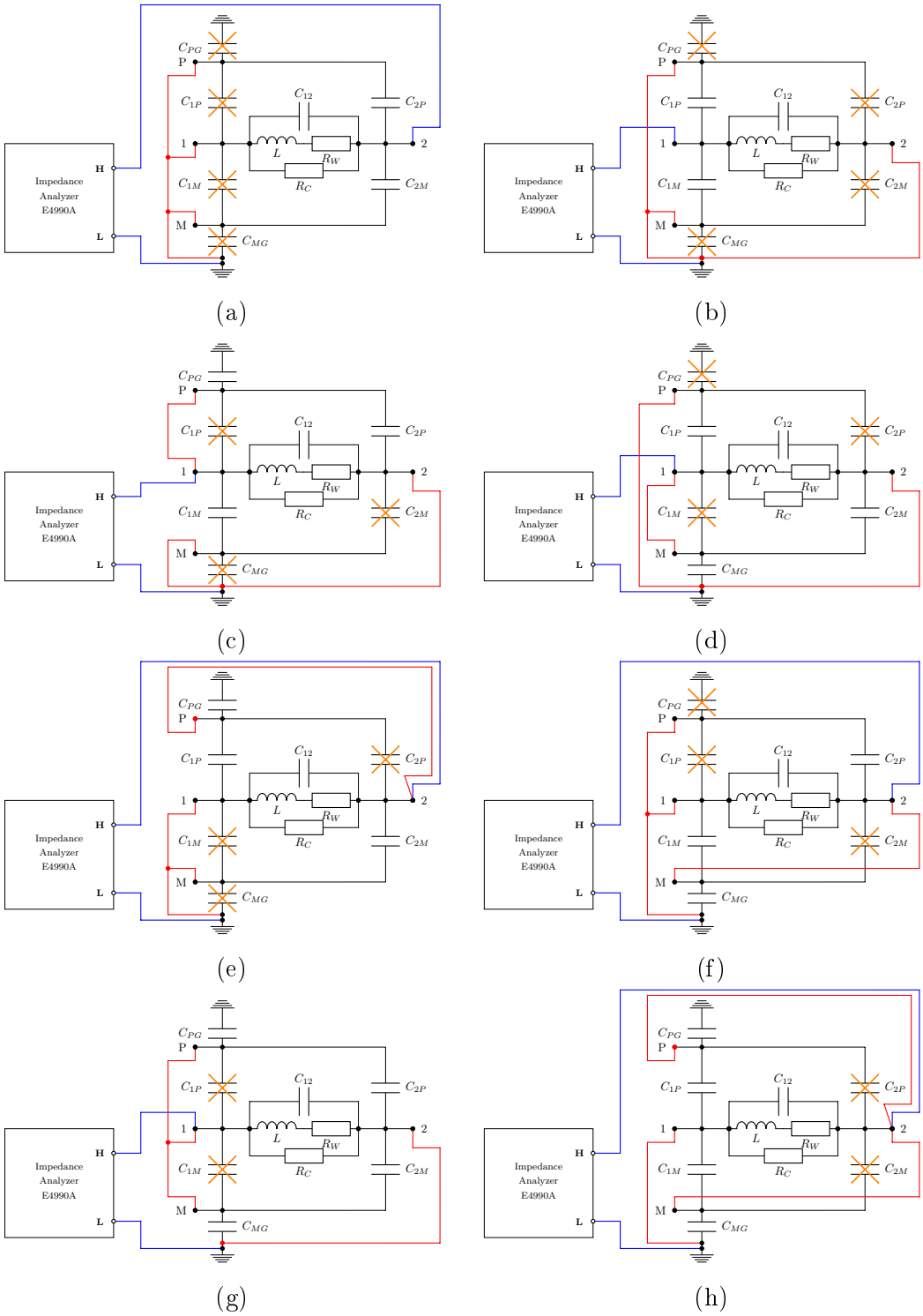


Figure E.4: resonant frequency measurements configurations - for the system with 7 stray capacitances

$$\begin{cases} C_{2P} + C_{2M} + C_{12} = 351,6pF \\ C_{1M} + C_{1P} + C_{12} = 248,8pF \\ C_{1M} + C_{12} + C_{2P} + C_{PG} = 625,25pF \\ C_{MG} + C_{1P} + C_{12} + C_{2M} = 305,6pF \\ C_{2M} + C_{12} + C_{1P} + C_{PG} = 307,8pF \\ C_{2P} + C_{12} + C_{1M} + C_{MG} = 466,3pF \\ C_{12} + C_{2P} + C_{2M} + C_{PG} + C_{MG} = 479,2pF \\ C_{1P} + C_{1M} + C_{12} + C_{PG} + C_{MG} = 371,1pF \end{cases} \tag{E.3}$$

To calculate values of full system, 7 unknown values of stray capacitances must be evaluated. There is 3 equations from electrostatic method and 8 equations from resonant frequency method. To compose the proper system of equation the 7 different equations have to be used. In further consideration, always the 3 equations from electrostatic method is used together with 4 equations from resonant frequency method. Due to the excess number of equations, 10 different options for system of equations have been considered as presented in Table.E.1 and final calculations for each of them presented in Table.E.2.

Table E.1: Equation choice (10 options) to calculate all capacitances of an integrated inductor model with 7 stray capacitances

Eq. No.	**Resonant Freq.**	**Option**									
		1	2	3	4	5	6	7	8	9	10
1	1.29 MHz	x		x		x	x		x		
2	1.46 MHz	x		x	x			x			x
3	1.16 MHz	x	x		x	x					
4	1.35 MHz	x		x	x	x	x			x	
5	1.35 MHz			x		x	x	x		x	x
6	1.16 MHz		x					x	x	x	
7	1.15 MHz		x					x	x		x
8	1.26 MHz		x		x		x		x	x	x

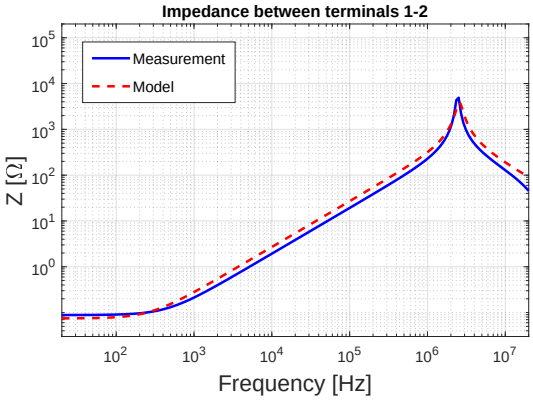
Table E.2: Calculation results of all capacitances (7) of an integrated inductor

Capa. name	Option 1	2	3	4	5	6	7	8	9	10	Avg. val.
From Electrostatic Method											
C_{PG}	98,81 pF										
C_{MG}	91,38 pF										
From Resonant & Electrostatic Method											
C_{1P}	251,4 pF	221,8 pF	246,2 pF	239,9 pF	246,2 pF	246,2 pF	263,1 pF	219,2 pF	219,2 pF	276,2 pF	242,9 pF
C_{1M}	277,3 pF	307,3 pF	282,5 pF	265,7 pF	279,3 pF	251,6 pF	296,9 pF	294,3 pF	251,6 pF	268,4 pF	277,5 pF
C_{2P}	380,9 pF	410,5 pF	386,2 pF	392,4 pF	386,2 pF	386,2 pF	369,2 pF	413,2 pF	413,2 pF	356,2 pF	389,4 pF
C_{2M}	256,6 pF	226,6 pF	251,3 pF	268,1 pF	260,6 pF	282,3 pF	237,0 pF	239,6 pF	282,3 pF	265,5 pF	257,0 pF
C_{12}	-289,9 pF	-348,2 pF	-285,9 pF	-193,8 pF	-295,1 pF	-316,9 pF	-304,2 pF	-332,5 pF	-289,9 pF	-332,7 pF	-298.9 pF
Error(avg.)	8,07 %	28,98 %	8,59 %	6,13 %	9,43 %	14,89 %	9,06 %	20,86 %	16,87 %	13,25 %	5,28 %
				Selected							

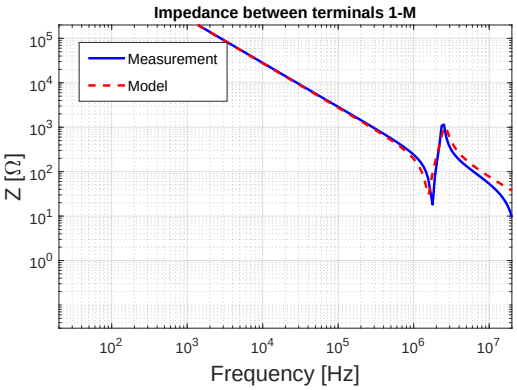
For the selected results (number 4 from Table.E.2 with the lowest error), the plots of measured and modeled (from simulation of full model) impedances are presented on Fig.B.6. These results prove the proper approach of identification for Integrated Inductor by usage of the Electrostatic & Resonant frequency Method. Moreover, for all combinations of equations choice, the error is not excessively divergent which indicates the correctness of the model scheme used. However, amount of effort needed to take measurements and perform calculations for all combinations is enormous. Thus, the simpler method has been developed & tested, and is presented in Appendix F.

Table E.3: Final values of Integrated Inductor model (obtained by E&RM)

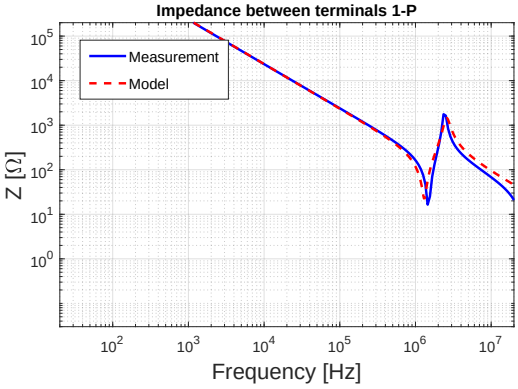
Parameter	**Value**
C_{1P}	239,9 pF
C_{1M}	265,7 pF
C_{2P}	392,4 pF
C_{2M}	268,1 pF
C_{PG}	98,81 pF
C_{MG}	91,38 pF
C_{12}	-193,8 pF
L	42,97 μH
R_W	74,57 $m\Omega$
R_C	3,84 $k\Omega$


Impedance between terminals 1-2
Measurement
Model
Z [Ω]
Frequency [Hz]

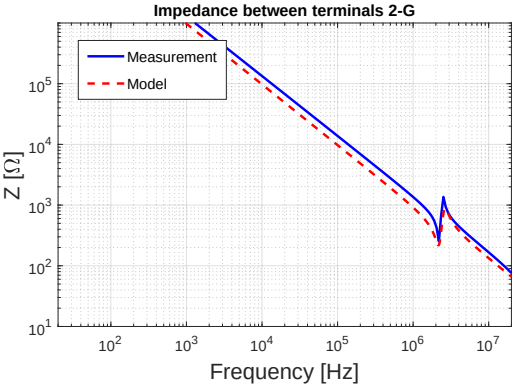
(a)


Impedance between terminals 1-M
Measurement
Model
Z [Ω]
Frequency [Hz]

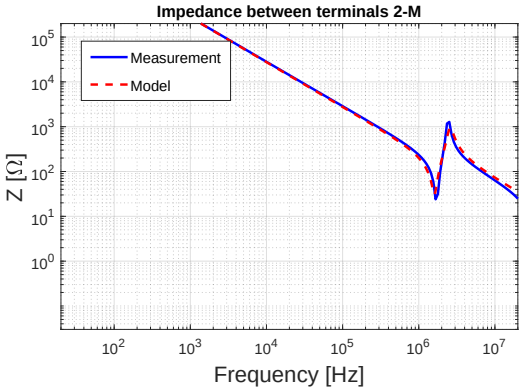
(b)


Impedance between terminals 1-P
Measurement
Model
Z [Ω]
Frequency [Hz]

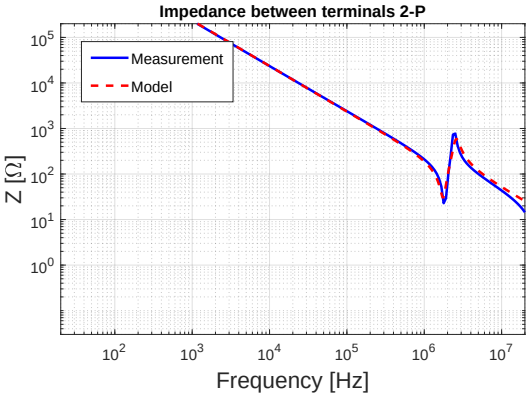
(c)


Impedance between terminals 2-G
Measurement
Model
Z [Ω]
Frequency [Hz]

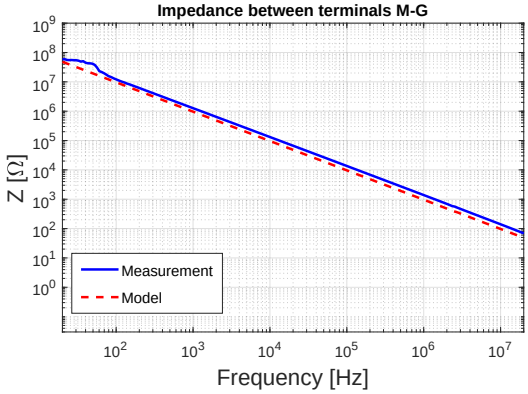
(d)


Impedance between terminals 2-M
Measurement
Model
Z [Ω]
Frequency [Hz]

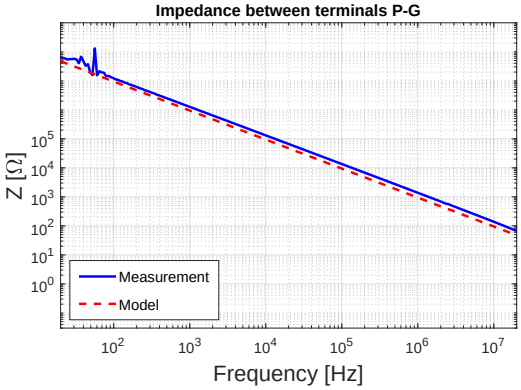
(e)


Impedance between terminals 2-P
Measurement
Model
Z [Ω]
Frequency [Hz]

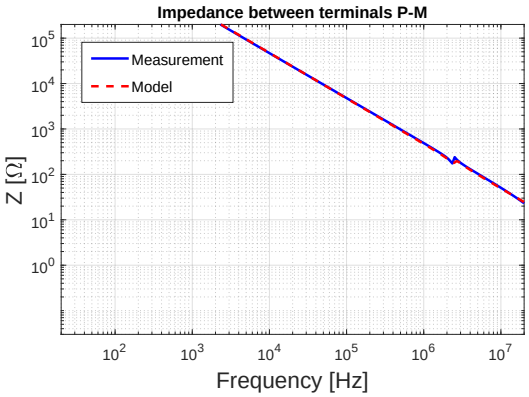
(f)


Impedance between terminals M-G
Measurement
Model
Z [Ω]
Frequency [Hz]

(g)


Impedance between terminals P-G
Measurement
Model
Z [Ω]
Frequency [Hz]

(h)



(i)

Figure B.6: Impedance plots comparison of experimental measurement and obtained model simulation (with 7 capacitances and characterized by E&R Method). Figures present results for measurement between terminals: a) 1 and 2; b) 1 and M; c) 1 and P; d) 2 and G; e) 2 and M; f) 2 and P; g) M and G; h) P and G; i) P and M

Appendix F

Integrated inductor characterization: Model with 7 stray capacitances system characterized by only Resonant frequency Method (RM)

The method is based on impedance measurement between 2 nodes and identification of first resonant frequency. The parasitic capacitance is estimated using formula for given resonant frequency f_r and measured inductance $L = 28.06\mu H$ (different inductance value than in Appendix E is due to identification of other integrated inductor piece).

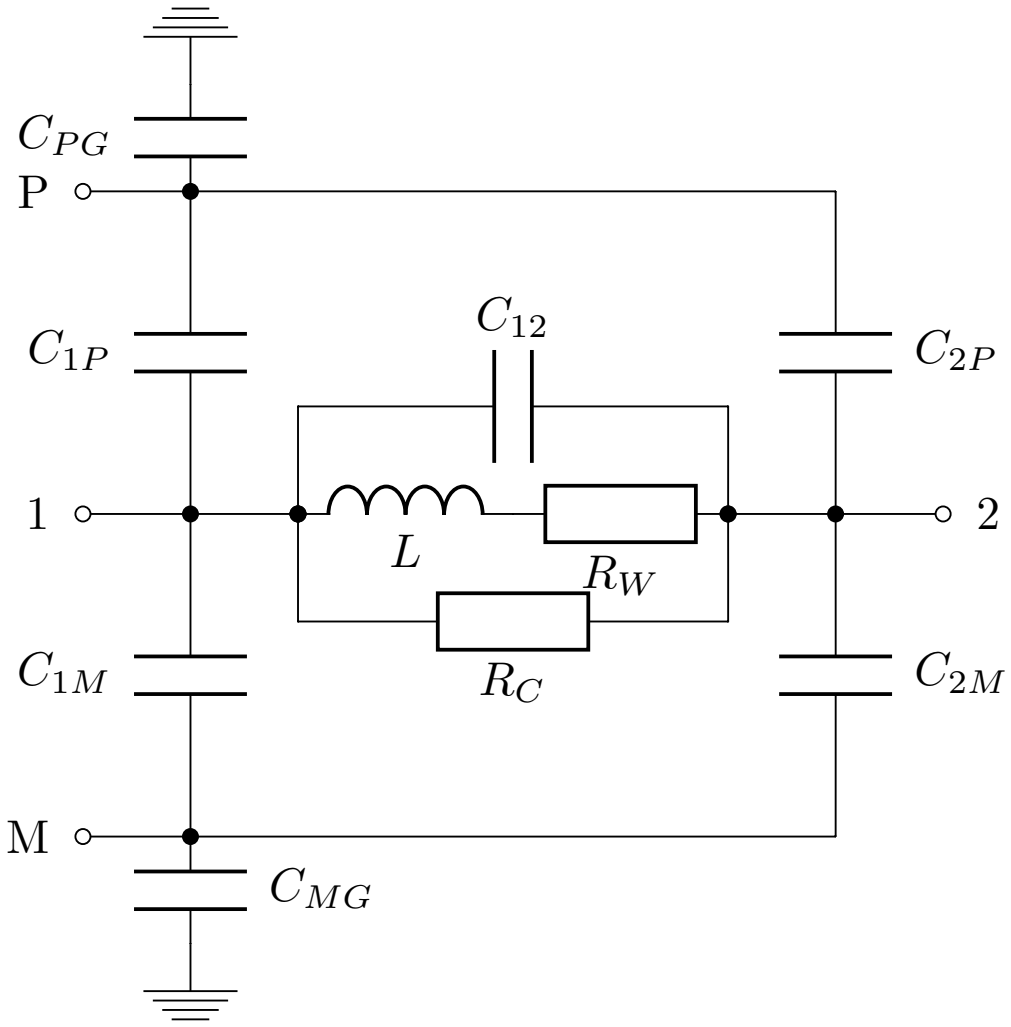


Figure F.1: Integrated inductor model with 7 stray capacitances

Table F.1: Stray capacitance values calculated by the resonance method

Nodes	**Resonant type**	**Resonant frequency**	**Capacitance calculated**	**Value**
P-2	serial	1.913 MHz	C_{1P}	246.56 pF
P-1	serial	1.810 MHz	C_{2P}	273.33 pF
M-1	serial	1.968 MHz	C_{2M}	232.99 pF
M-2	serial	1.576 MHz	C_{1M}	363.47 pF
1-2	parallel	1.576 MHz	C_{12mes}	269.79 pF

From equation for equivalent capacitance viewed from nodes 1-2, the value of C_{12} can be calculated:

$$C_{12mes} = \frac{C_{1P} * C_{2P}}{C_{1P} + C_{2P}} + C_{12} + \frac{C_{1M} * C_{2M}}{C_{1M} + C_{2M}} \tag{F.1}$$

$$C_{12} = C_{12mes} - \frac{C_{1P} * C_{2P}}{C_{1P} + C_{2P}} - \frac{C_{1M} * C_{2M}}{C_{1M} + C_{2M}} = -148.02pF \tag{F.2}$$

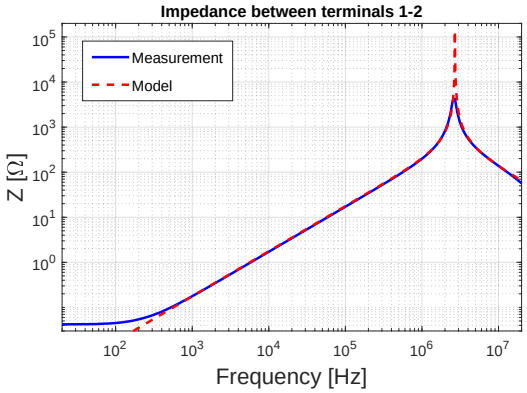
The capacitance between the P-node and ground and between the M-node and ground have been measured directly. The model capacitance was obtained by transforming the equations:

$$\begin{cases} C_{MGmes} == C_{MG} + \left(\frac{1}{C1M} + \frac{1}{C1P} + \frac{1}{CPG}\right)^{-1} \\ C_{PGmes} == C_{PG} + \left(\frac{1}{C1M} + \frac{1}{C1P} + \frac{1}{CMG}\right)^{-1} \end{cases} \tag{F.3}$$

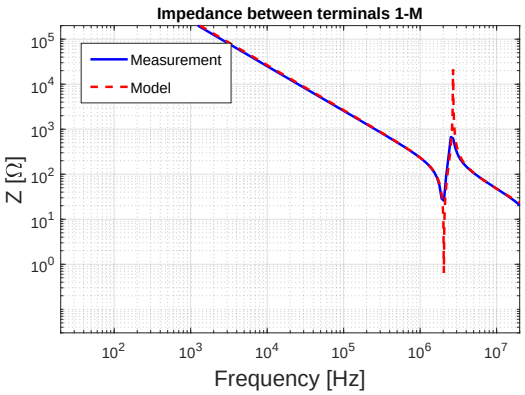
$$C_{PG} = 93.848pF \qquad C_{MG} = 90.88pF \tag{F.4}$$

Table F.2: Final values of Integrated Inductor model (obtained by RM)

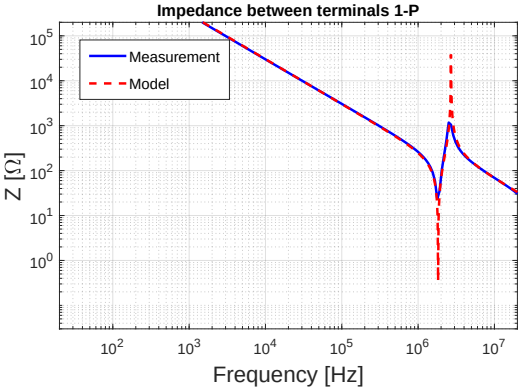
Parameter	**Value**
C_{1P}	246,6 pF
C_{1M}	363,5 pF
C_{2P}	273,3 pF
C_{2M}	233,0 pF
C_{PG}	93,85 pF
C_{MG}	90,88 pF
C_{12}	-148,0 pF
L	28,06 μH


Impedance between terminals 1-2
Measurement
Model
Z [Ω]
Frequency [Hz]

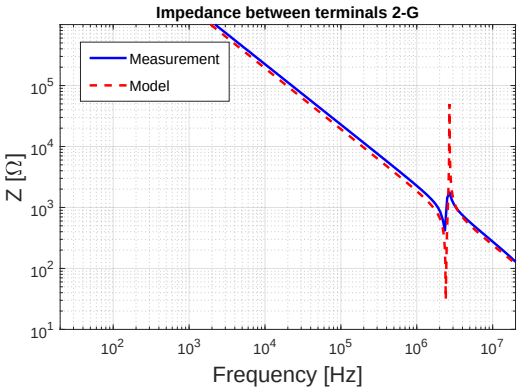
(a)


Impedance between terminals 1-M
Measurement
Model
Z [Ω]
Frequency [Hz]

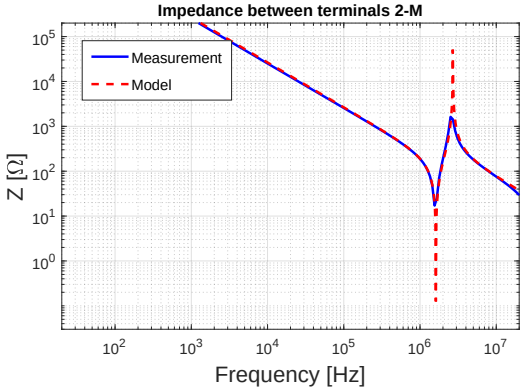
(b)


Impedance between terminals 1-P
Measurement
Model
Z [Ω]
Frequency [Hz]

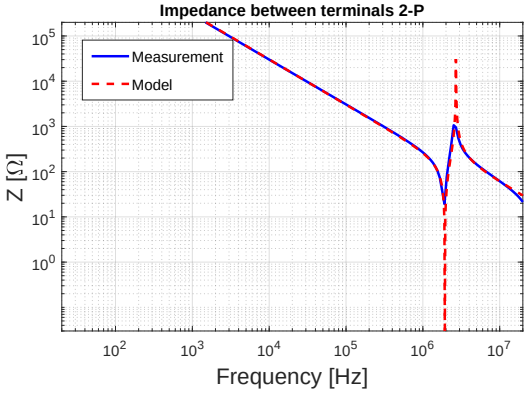
(c)


Impedance between terminals 2-G
Measurement
Model
Z [Ω]
Frequency [Hz]

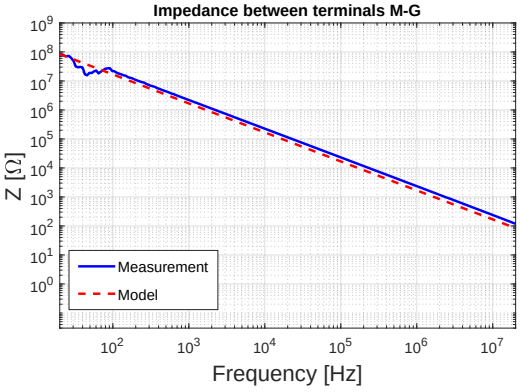
(d)


Impedance between terminals 2-M
Measurement
Model
Z [Ω]
Frequency [Hz]

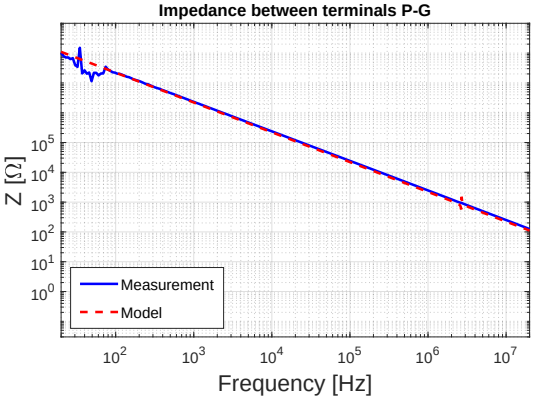
(e)


Impedance between terminals 2-P
Measurement
Model
Z [Ω]
Frequency [Hz]

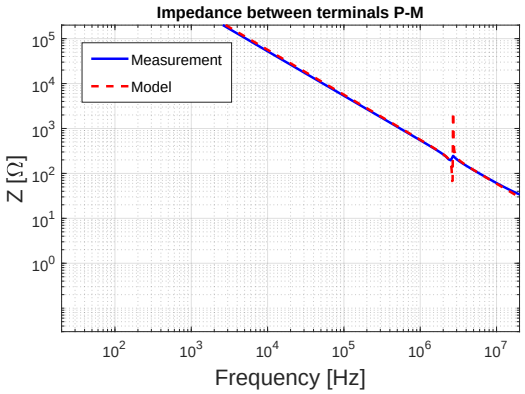
(f)


Impedance between terminals M-G
Measurement
Model
Z [Ω]
Frequency [Hz]

(g)


Impedance between terminals P-G
Measurement
Model
Z [Ω]
Frequency [Hz]

(h)



(i)

Figure C.2: Impedance plots comparison of experimental measurement and obtained model simulation (with 7 capacitances and characterized by Electrostatic Method). Figures present results for measurement between terminals: a) 1 and 2; b) 1 and M; c) 1 and P; d) 2 and G; e) 2 and M; f) 2 and P; g) M and G; h) P and G; i) P and M

Both of methods, presented in Appendix E and Appendix F, are giving similar results in values and distribution of capacitance across the model. It proves that the model based on 7 stray capacitances is validated and usable for simulation research. These two methods should be tested on the other passive elements to determine the differences between them and fully prove their accuracy. In terms of time consuming, the method presented in Appendix F seems to be faster and it is promising for the future research.

Appendix G

Résumé de thèse en français

Les dispositifs GaN se caractérisent par leur capacité à fonctionner à des fréquences et des vitesses de commutation élevées ($\frac{dv}{dt}$ et $\frac{di}{dt}$ élevés), ce qui fait des éléments parasites des facteurs clés pour l'interférence électromagnétique générée et la performance électrique. Cette thèse présente un certain nombre de solutions pour répondre au besoin de recherche et de développement technologique sur l'atténuation des interférences électromagnétiques dans les convertisseurs électroniques de puissance avec des transistors GaN. Trois approches pour identifier et optimiser les perturbations conduites sont présentées. Tout d'abord, l'effet du mode de contrôle (commutation dure ou douce) est évalué. Ensuite, des considérations générales sur la disposition des convertisseurs sont présentées, ainsi que l'idée du blindage et le concept de Power-Chip-on-Chip (PCoC). Enfin, une nouvelle approche de la conception des éléments magnétiques et de leur intégration possible dans un convertisseur à base de GaN a été étudiée. Dans chacune de ces activités, l'atténuation des interférences électromagnétiques a été une priorité.

La thèse vise à prouver qu'il est possible d'atténuer les interférences électromagnétiques en sélectionnant correctement les stratégies de contrôle, en modifiant l'agencement et en mettant en œuvre une nouvelle approche des éléments magnétiques.

Le cœur de l'ouvrage est constitué de trois chapitres, dont le contenu est résumé ci-dessous. Les chapitres sont conçus pour avoir un minimum d'interdépendance et peuvent donc être lus indépendamment les uns des autres :

G.1 Chapitre 2 - Impact de la stratégie de contrôle sur la génération d'interférences électromagnétiques - basé sur un convertisseur Buck

Le chapitre 2 se concentre sur l'effet de la stratégie de contrôle sur les interférences électromagnétiques générées. L'approche logicielle de la réduction des interférences électromagnétiques consiste à personnaliser la stratégie de commande pour un convertisseur donné et à utiliser (si possible) des conditions de résonance, de quasi-résonance, etc. pour obtenir une commutation douce. ZVS ou ZCS garantit qu'au moins une sous-période de fonctionnement du convertisseur ne connaît pas de fronts de montée/descente de tension ou de courant élevés, ce qui entraîne une réduction des perturbations générées. L'analyse est basée sur un convertisseur buck réalisé sur un prototype de bras d'onduleur simple avec des transistors GaN. Une caractérisation exhaustive des sous-périodes du convertisseur fonctionnant en mode courant discontinu (DCM) (avec un transistor de commutation et une diode) et en mode courant triangulaire (TCM) (fonctionnement synchrone de deux transistors) est présentée (exemple de TCM sur la Fig. G.1).

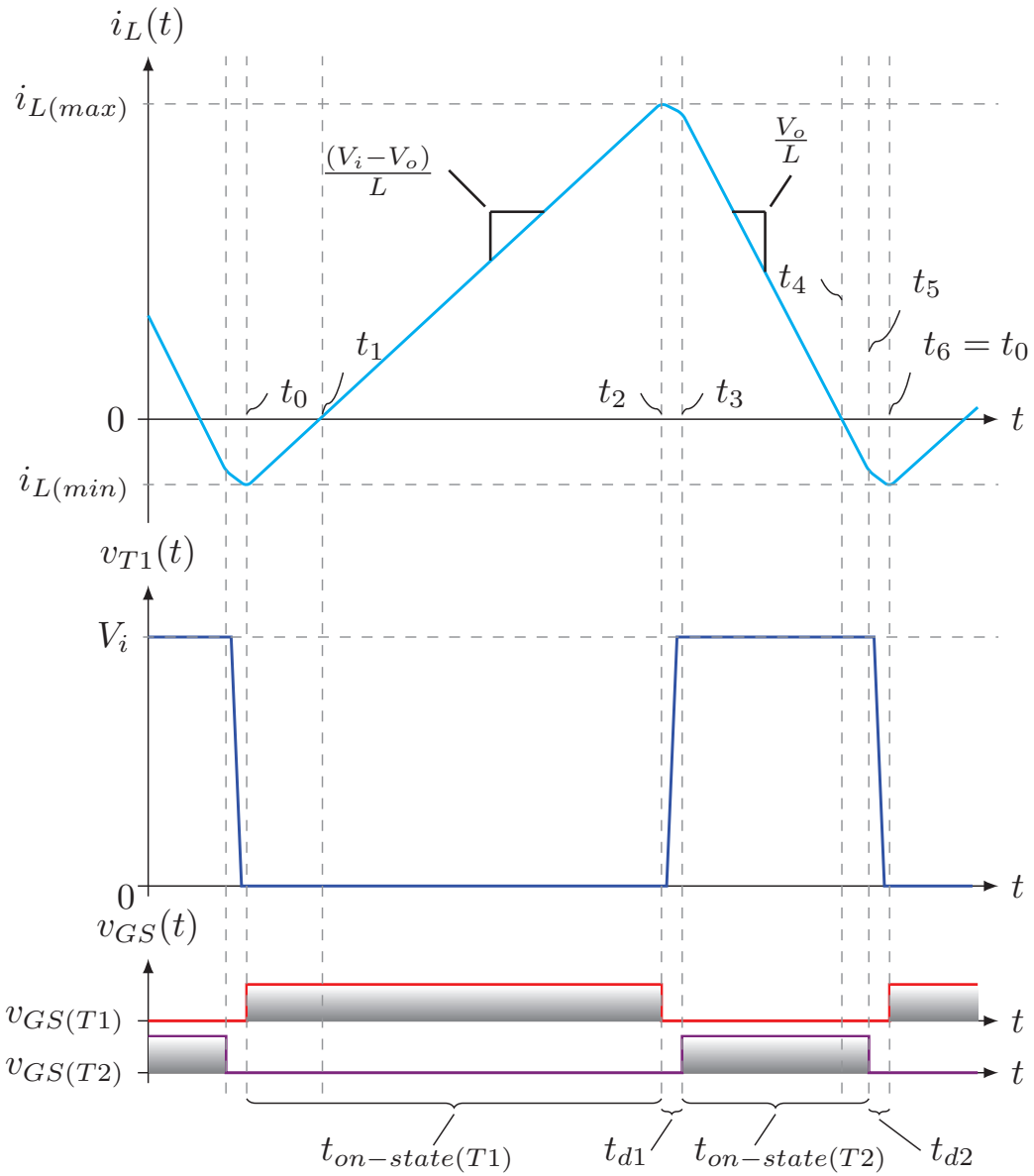


Figure G.1: Forme d'onde TCM

Les résultats des performances électriques et des formes d'onde pour les deux modes de fonctionnement sont présentés. Une application et une procédure pour le dimensionnement d'un circuit snubber capacitif sont proposées pour réduire les surtensions importantes subies (Fig. G.2).

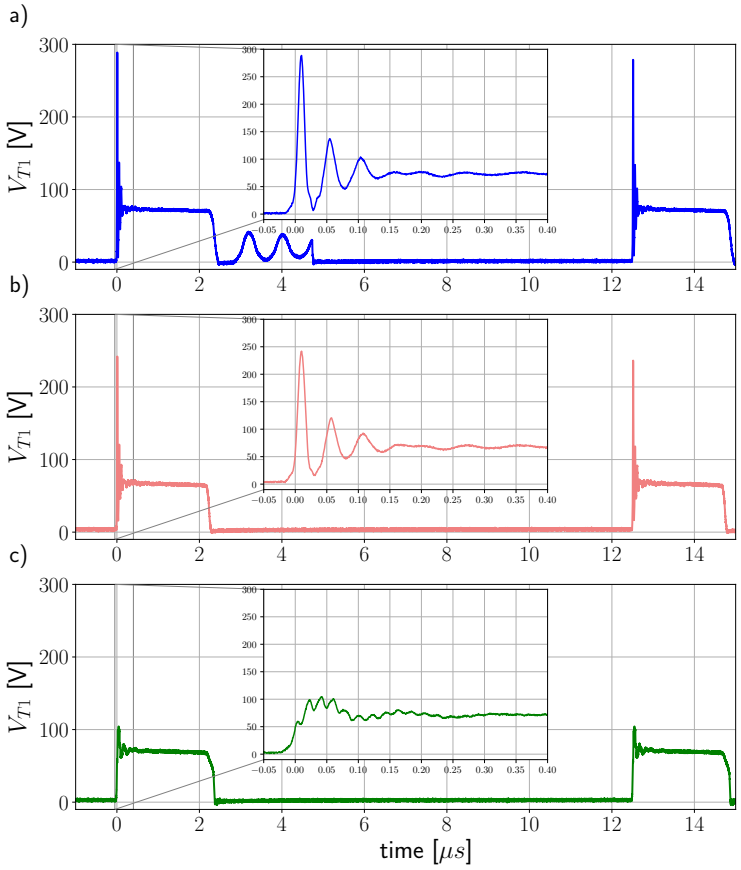
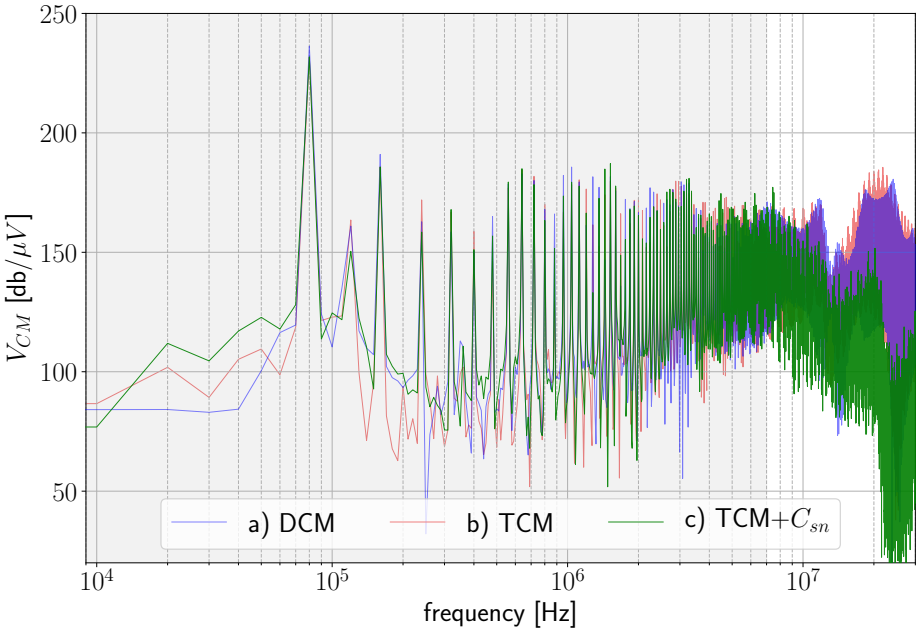
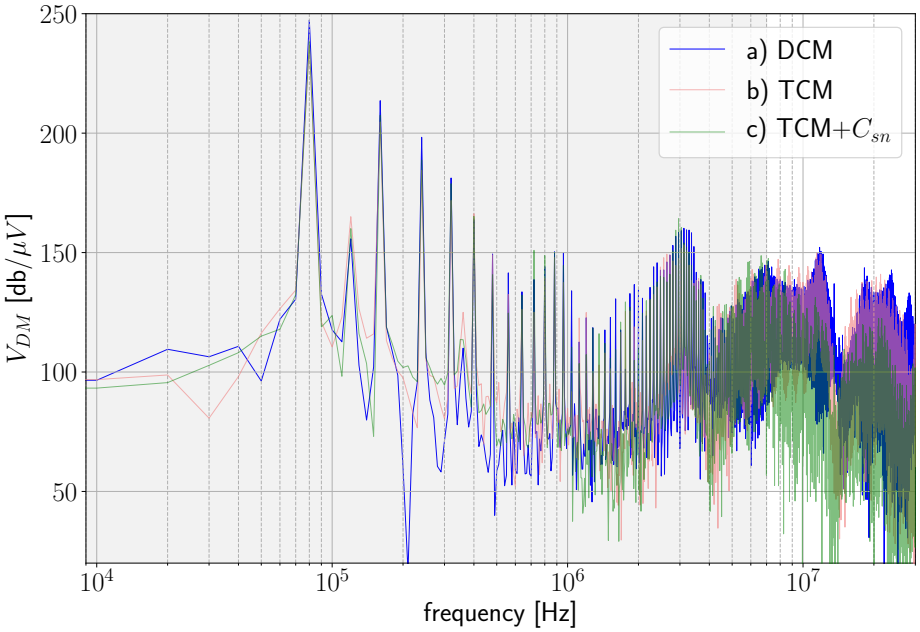


Figure G.2: Formes d'ondes de tension à travers le transistor T_1 ; a) DCM à commutation dure, b) TCM ZVS, c) TCM ZVS avec condensateurs snubber C_{sn}.

En conséquence, une atténuation significative des des perturbations électromagnétiques conduites (Fig. G.3) a été obtenue avec une légère augmentation de l'efficacité de la conversion de puissance pour la TCM. Des surtensions importantes causées par la valeur relativement élevée de l'inductance de la boucle de puissance ont également été observées au cours de l'étude. Cependant, afin d'exploiter pleinement la capacité de commutation rapide des HEMT GaN, la recommandation de la topologie ZVS ne peut pas être une condition suffisante, mais doit être accompagnée d'une conception de circuit qui garantit des inductances parasites extrêmement faibles de la boucle de puissance de commutation - comme discuté au chapitre 3.



(a)



(b)

Figure G.3: Spectres de bruit conduit EMI : (a) CM ; (b) DM

G.2 Chapitre 3 - Conception et mise en œuvre de dispositifs GaN pour l'atténuation du bruit électromagnétique

Le chapitre 3 présente les considérations relatives à la réduction des interférences électromagnétiques par une nouvelle conception de l'agencement du convertisseur. Une description détaillée de l'identification des éléments parasites dans une seule branche de convertisseur est présentée (Fig. G.4). Une simulation de cette structure a été développée et appliquée pour étudier en détail l'impact de la disposition de chaque composants sur le comportement CEM.

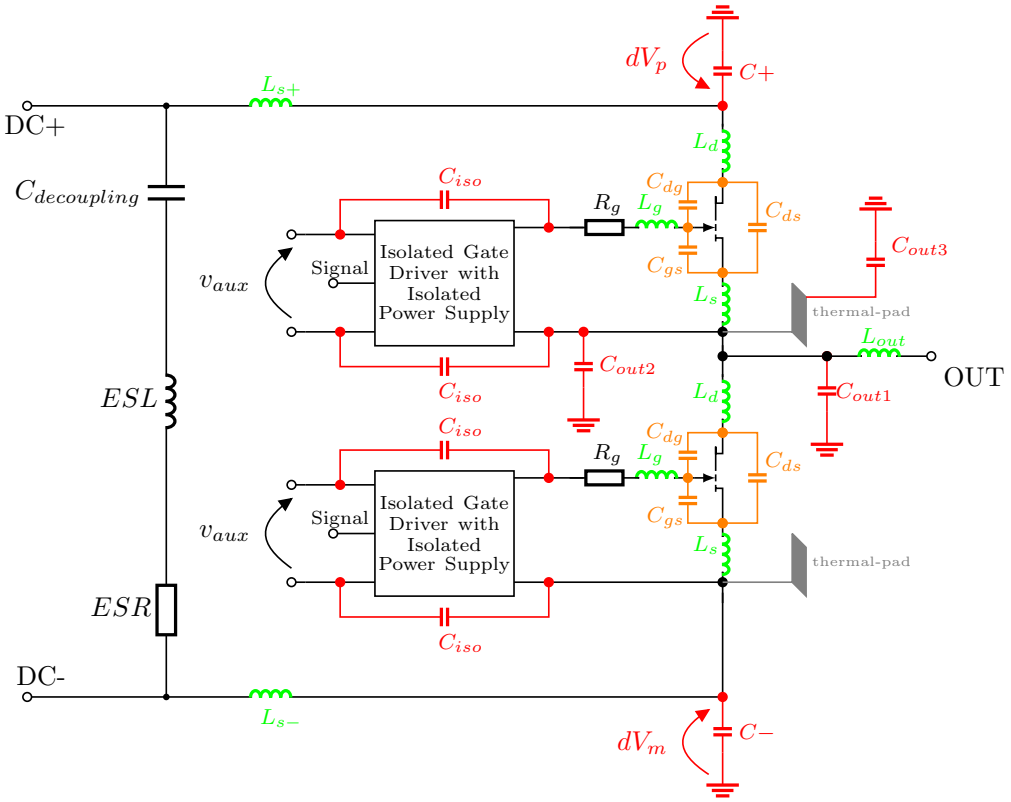


Figure G.4: Eléments parasites d'une configuration de branche d'onduleur avec condensateur de découplage

L'environnement CEM et les précautions requises pour les mesures en laboratoire des émissions conduites sont décrits. Le concept de blindage est présenté et décrit en détail (Fig. G.5).

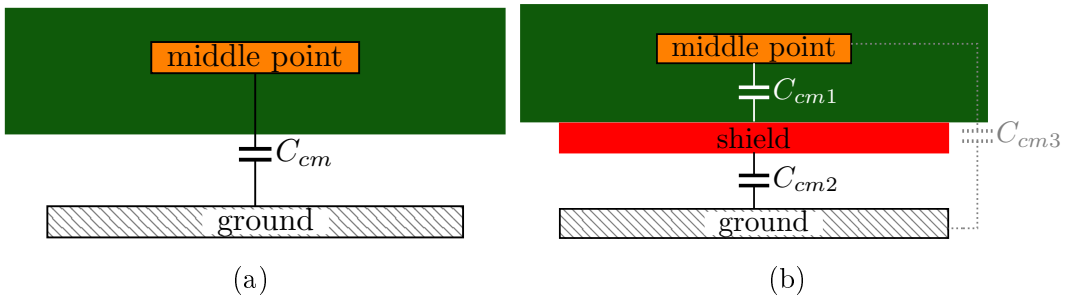


Figure G.5: Présentation géométrique de la piste du point central de la carte de circuit imprimé avec les capacités parasites : a) non blindée ; b) blindée.

En ce qui concerne les interférences de mode commun, la réduction de la capacité du point central à la terre est cruciale, car cette capacité (capacité du point flottant avec les fortes valeurs de $\frac{dv}{dt}$) sont les facteurs décisifs à l'origine des interférences. Pour atteindre cet objectif, le concept de blindage a prouvé son efficacité (Fig. G.6).

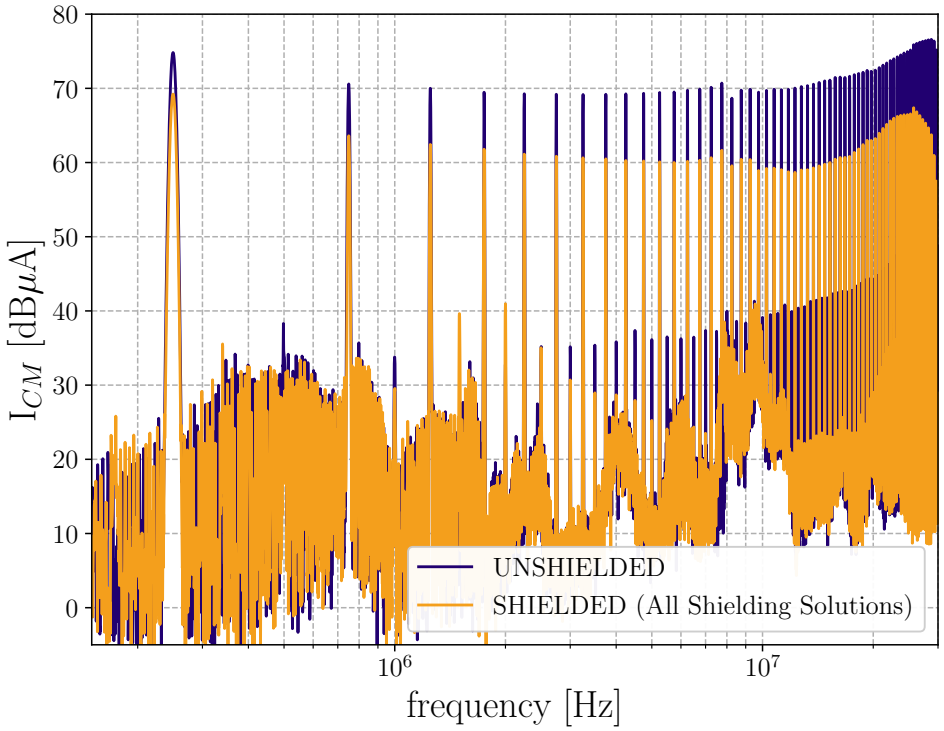


Figure G.6: Émissions de courant CM avec et sans solutions de blindage total

Enfin, l'idée d'adapter le concept de Power-Chip-on-Chip (PCoC) aux transistors GaN est présentée (Fig. G.7).

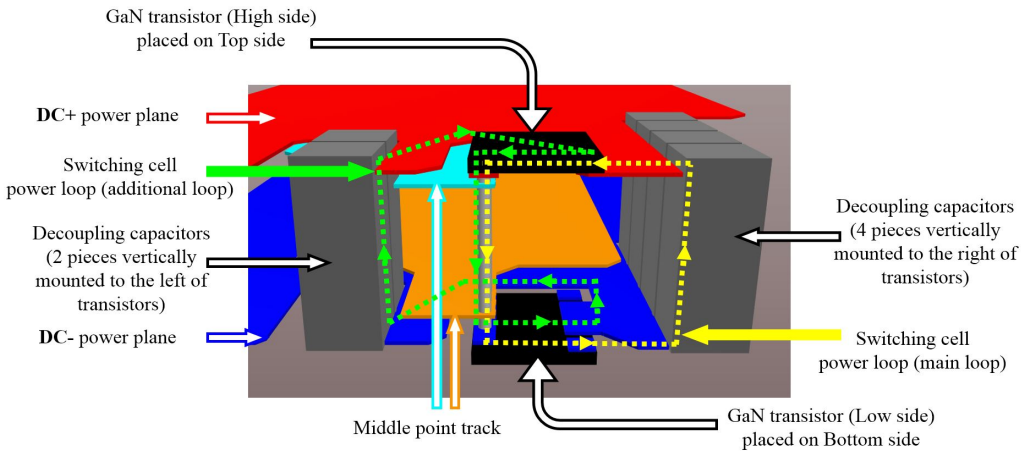


Figure G.7: Vue éclatée en 3D de l'agencement du PCoC en 3D (épaisseur de la carte à l'échelle 10:1)

Un concept de blindage (empilement en sandwich) a été amélioré par une disposition plus symétrique apportée par le concept PCoC, où une meilleure atténuation des perturbations de mode commun ont été démontrées ainsi qu'une réduction radicale de l'inductance de la boucle de puissance ($C_{cm} = 0.68\,pF$: capacité du point central à la terre ; $L_s = 1.49\,nH$ [$2.29\,nH$ en considérant l'inductance à l'intérieur du boîtier des deux transistors GaN]). Des valeurs aussi faibles d'éléments parasites prouvent une très bonne optimisation CEM de l'agencement du convertisseur. En outre, il a été démontré qu'il faut tenir compte non seulement de l'agencement de l'alimentation, mais aussi des circuits de commande rapprochées de la grille et des pads thermiques. Dans ces zones, la capacité de mode commun parasite est également distribuée et doit être réduite autant que possible (Fig. G.8).

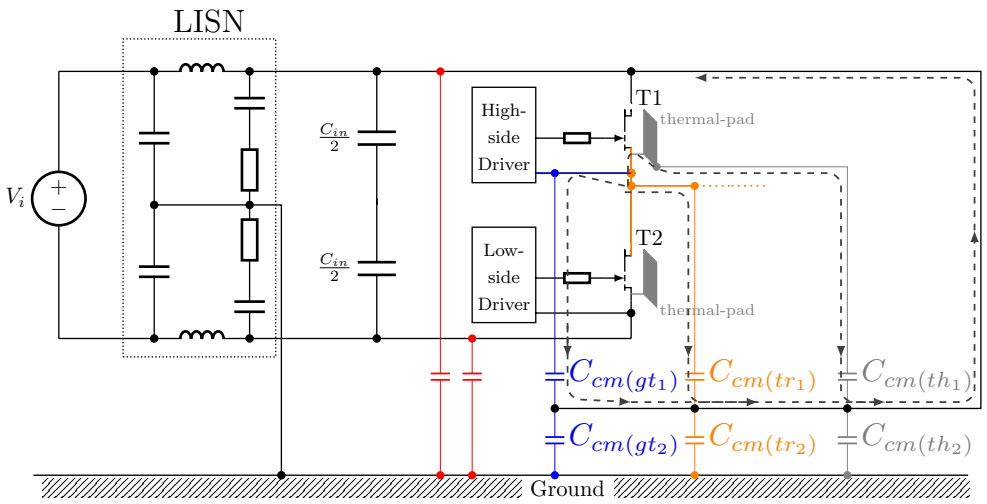
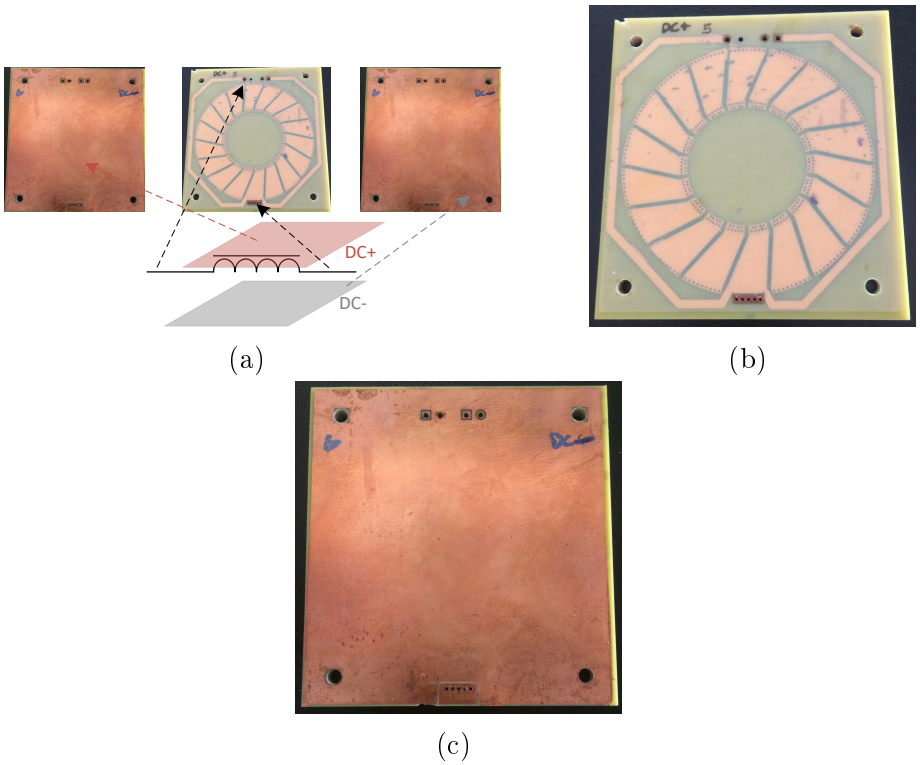


Figure G.8: Capacités parasites de mode commun et chemins de courant de mode commun (recirculation) pour un convertisseur blindé (blindé : piste du point central, patin thermique, circuit d'alimentation de la grille)

G.3 Chapitre 4 - Nouvelle génération de magnétiques pour les appareils à grande vitesse

Une nouvelle approche de la conception et de l'utilisation des éléments magnétiques est présentée. L'inducteur intégré de découplage est présenté ainsi que son processus de fabrication (figure G.9). Il est basé sur la technologie prometteuse des inducteurs planaires et a été introduit pour filtrer les émissions de mode commun à la source.



(a) (b)

(c)

Figure G.9: Prototype d'inducteur intégré : a) vue conceptuelle ; b) inducteur non blindé fabriqué ; c) inducteur blindé fabriqué

La méthodologie de caractérisation de l'impédance de l'inducteur intégré est ensuite présentée, avec une attention particulière accordée à l'extraction des éléments parasites clés qui affectent le comportement CEM (le modèle final de l'inducteur est présenté à la figure G.10).

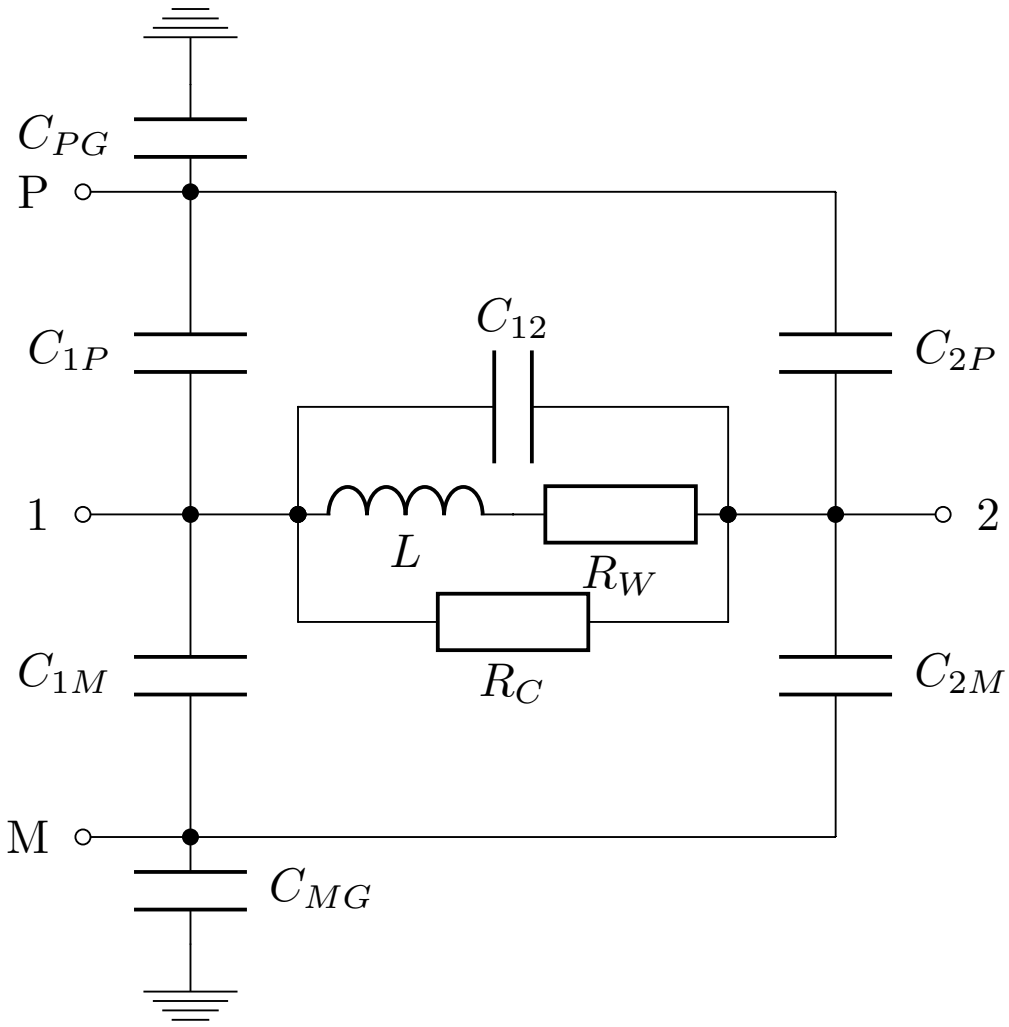


Figure G.10: Modèle d'inducteur intégré avec 7 capacités parasites

Enfin, l'avantage de l'utilisation de la nouvelle solution par rapport à l'inducteur classique a été présenté sur la base d'études de simulation. La réduction du bruit EMI est évidente et présentée dans la figure G.11. En outre, le blindage appliqué à cette inductance planaire pour circuit imprimé semble attrayant en raison des fonctions Cy intégrées (recyclage interne du courant CM - analogie avec le blindage de l'agencement de puissance).

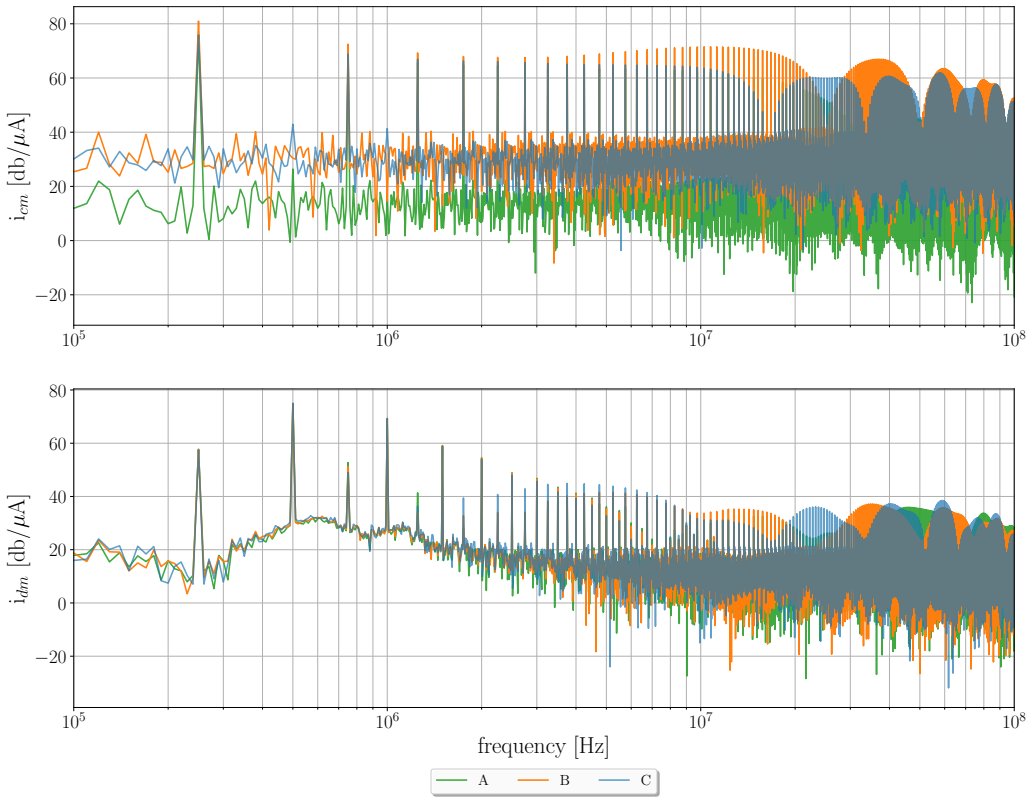


Figure G.11: Spectres DM et CM du cas : A - inducteur idéal ; B - modèle d'inducteur non blindé avec éléments parasites ; C - modèle d'inducteur intégré blindé avec éléments parasites.