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# Understanding of degradation mechanisms involving moisture diffusion into BEOL integrated dielectric stacks

Léo Mischler

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THÈSE PRÉSENTÉE  
POUR OBTENIR LE GRADE DE  
**DOCTEUR**  
**DE L'UNIVERSITÉ DE BORDEAUX**

ECOLE DOCTORALE SCIENCES PHYSIQUES ET DE  
L'INGENIEUR  
ELECTRONIQUE

Par **Léo MISCHLER**

Compréhension des mécanismes de dégradation et de diffusion  
de l'humidité dans les empilements de diélectriques intégrés

Sous la direction de : **Geneviève DUCHAMP**  
Co-directrice : **Hélène FREMONT**

13/12/2024

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Je termine sur une citation qui résume l'évolution de mes réflexions personnelles au cours de ce travail :

*“ C’est important pour les gens, surtout pour les gens qui sont plus conscients de ce qui se passe, qu’ils ne tombent pas dans les théories plus négatives, que les gouvernements, que les entreprises ont kidnappé l’humanité. Il y a beaucoup de choses qui sont vraies là-dedans, mais si on se fixe là-dessus, enfin, on participe à cette négativité. C’est important de ne pas devenir ce qu’on combat, c’est-à-dire qu’on ne peut pas changer ce système en faisant la même chose que ce système a fait. Si on devient aussi négatif qu’eux, et qu’on les combat de cette façon, on en arrive au même point. Ça n’aide pas, il faut rester positif, en restant conscients de ce qu’il se passe sans l’ignorer. Il faut avoir cette joie de vivre, cette ouverture, cette positivité, parce que la négativité, elle, se détruit par elle-même. Tout ce qu’il faut faire, c’est construire le monde qu’on veut voir dans notre futur. »*

– Nassim Haramein

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# Acronyms

<b>USG</b>	: Undoped Silicon Glass
<b>ULK</b>	: Ultra-low-k
<b>TEM</b>	: Transmission electron microscopy
<b>EDX</b>	: Energy Dispersive X-Ray Analysis
<b>EELS</b>	: Electron energy loss spectroscopy
<b>ToF-SIMS</b>	: Time of Flight – Secondary Ion Mass Spectrometry
<b>THS</b>	: Thermal and Humidity Storage
<b>HAST</b>	: Highly accelerated stress test
<b>BEOL</b>	: Back end of the line
<b>FEOL</b>	: Front end of the line
<b>PECVD</b>	: Plasma-enhanced chemical vapor deposition
<b>CMP</b>	: Chemical mechanical polishing
<b>Via</b>	: Vertical Interconnect access
<b>FTIR</b>	: Fourier-transform infrared spectroscopy
<b>IMD</b>	: Inter-metallic dielectric
<b>RH</b>	: Relative Humidity
<b>SiCN</b>	: Silicon Carbonitride
<b>TEOS</b>	: Tetraethoxysilane
<b>TTF</b>	: Time to failure

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# General introduction

The field of microelectronics has witnessed remarkable advancements over the past few decades, fueled by the continuous drive to reduce the size of transistors and improve the performance of integrated circuits. This pursuit of miniaturization, guided by Moore's Law, has been a pivotal force shaping the industry's landscape, leading to the development of technological nodes from 90 nm, introduced in the early 2000s, to 65 nm, 45 nm, and further down to 28 nm, 14 nm, 10 nm, 7 nm, and even 5 nm in recent years, with 3 nm and 2 nm nodes currently under development. In this context, a "node" refers to the technology process used in the fabrication of semiconductor devices, such as transistors, on integrated circuits (ICs). The node represents essentially the distance between two identical features in an array layout. This measurement correlates directly with the size of the smallest component that can be manufactured on the chip, with a smaller number indicating a more advanced technology. For example, a 28 nm technology node means that the smallest feature size of the transistors manufactured using this process is approximately 28 nanometers. This reduction in size allows for more transistors to be packed into the same chip area, significantly increasing computing power and efficiency while reducing power consumption. However, as integrated circuits become increasingly complex and densely packed, new challenges arise, necessitating comprehensive research into advanced interconnect technologies and environmental reliability.

An integrated circuit is a device enabling computational operations through the integration of active components (primarily transistors) and passive components (such as resistors, capacitors, etc.). Each component is locally fabricated on a silicon disk known as a wafer. Semiconductors are materials with electrical conductivity between that of conductors and insulators, which can be modified by factors such as temperature, doping with impurities, and the application of electric fields. Silicon is widely used in microelectronics due to its advantageous properties, including its abundance in nature, relatively low cost, and its ability to form a stable oxide layer ( $SiO_2$ ), which is crucial for the fabrication of transistors and other electronic components. Additionally, silicon fabrication techniques are well-established, enabling the production of complex, high-performance integrated circuits. To reduce industrial manufacturing costs, the diameter of silicon wafers has progressively increased, reaching 300 mm in the most recent production lines (as is the case at the STMicroelectronics production site in Crolles).

The fabrication of an integrated circuit typically requires an average of 4 months and over a hundred manufacturing steps. The fabrication of an integrated circuit is divided into three main stages (Fig 1) :

- The Front End Of Line (FEOL) gathers all the manufacturing steps of the transistors of the integrated circuit, which perform various logical functions. This active area is the core of the integrated circuit's operation.

- The Back End Of Line (BEOL) corresponds to all the interconnections ensuring the connections between the transistors of the integrated circuit. The interconnection area consists of several successive metal layers interconnected by vertical conducting posts called vias. This area allows for the distribution of current to the active area.

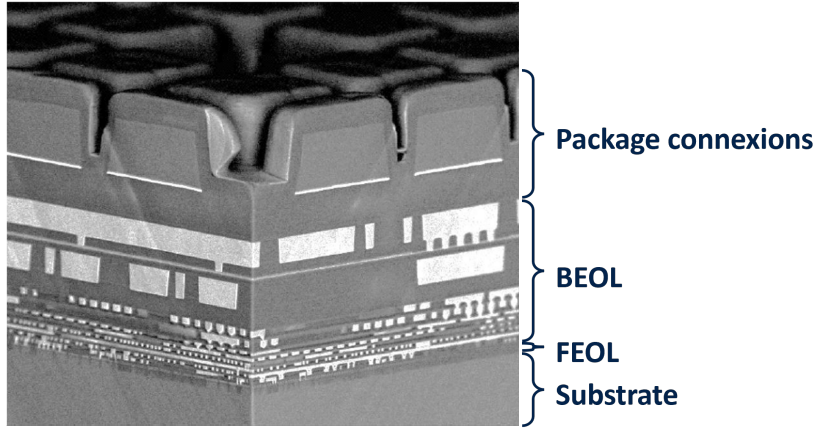


Figure 1: Integrated circuit cross-section with different areas highlighted [1]

- The connection to the package ensures the interface between the integrated circuit and the final chip package, through input and output lines for data and power supply. The interconnections are encapsulated by a passivation layer to protect them against any form of external mechanical and physico-chemical aggression. Openings are made in this passivation layer to create aluminum metal pads, called pads, for wiring the chip.

This work represents a collaboration between the Material to System Integration Laboratory (IMS) of the University of Bordeaux and STMicroelectronics in Crolles. The IMS is a research unit affiliated with the CNRS, the University of Bordeaux, Bordeaux INP and located in Talence. It specializes in the study of materials for electronic devices, the reliability of components, and process management, targeting sectors such as telecommunications, transportation, healthcare, and energy through various research projects. On the other hand, STMicroelectronics, founded in 1987 through the merger of SGS Microelettronica (Italy) and Thomson Semiconductors (France), operates in approximately 35 countries. It specializes in the design, development, and manufacturing of semiconductors, with key application areas including automotive and telecommunication. The reliability of products is a critical concern at STMicroelectronics, which aligns well with the collaboration with IMS.

The project to study the impact of humidity in the Back-End of Line (BEOL) began in 2017 with a CIFRE doctoral thesis by Vivien Cartailier. Cartailier's research focused on the behavior of bulk dielectrics (thin layers deposited on a Si substrate) in relation to moisture diffusion. Additionally, he initiated an investigation into the effects of moisture on 3D integrated structures. His work forms the foundational basis for my study.

One of the perspectives highlighted by Cartailier is the application of his research to the industry. This involves building an acceleration model under various storage conditions (temperature and humidity), which will be the main focus of my study. The objective is to develop a model, as well as determine the acceleration factors between standard industrial test condition, for instance  $85^{\circ}\text{C}/85\%\text{RH}$ ). Comparing these factors with empirical data commonly cited in the literature and used in industry will be of particular interest.

To develop an acceleration model, it is essential to first identify the specific degrada-

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tion mechanisms being accelerated. In my work, I aim to gain a deeper understanding and description of electrical degradation in integrated structures. This will be achieved through physicochemical characterizations of integrated structures, with the objective of identifying potential oxidized areas. Subsequently, by leveraging data and parameters from bulk material analysis, the goal is to establish a connection between bulk dielectrics and integrated structures through numerical simulations.

# Moisture diffusion study context

Following a brief review and historical overview of the various materials found in the metallic interconnect region, we will understand why more complex materials are used instead of traditional  $SiO_2$  as dielectric. Before focusing on the impact of moisture into real structures, the bulk materials behavior is presented thanks to the previous PhD thesis on the subject [6]. This will allow us to identify the specific areas of study for this work. Finally, the test structures utilized in this study will be presented, along with the different characterization methods employed.

## 1.1 Context

The objective of this work is to explore integrated structures without concentrating on a particular technology. To achieve this, we focus on the impact of humidity only in the BEOL part of metal interconnections which can be roughly depicted as in Figure 1.1. This area is composed by metallic lines that are separated by different layers of dielectrics. Initially, amorphous silicon dioxide ( $SiO_2$ ) with a dielectric constant of 4.2 served as the primary material for insulating interconnects (IMD).  $SiO_2$  was commonly used until the mid-1990s when interconnect performance demands were less critical. However, it persists in current architectures at global levels where dimensions are more flexible and signal transmission delay constraints are less significant. The approach for reducing the permittivity of the IMD material involved introducing atoms with low polarizability into  $SiO_2$  to reduce the dielectric constant.

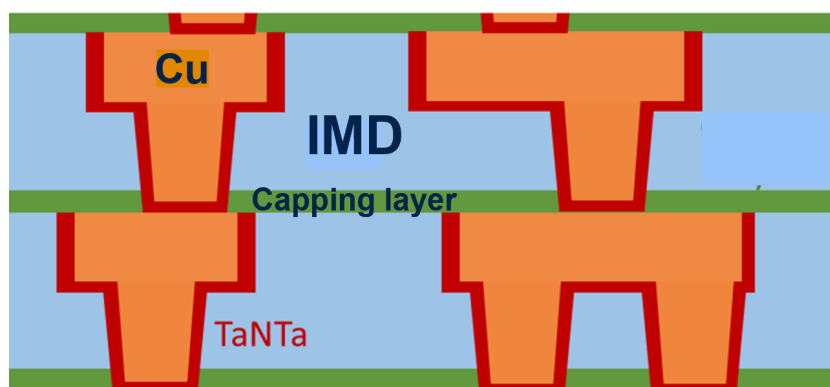


Figure 1.1: Schematic of two metal levels in BEOL

Atoms	Polarisability ( $10^{-40}$ F/m <sup>2</sup> )
Si	4.17
O	0.671
F	0.418
C	1.064
H	0.484

Table 1.1: Polarisability of some elements

For instance, Fluorine-doped silicon oxide (SiOF), or Fluoro-Silicate Glass (FSG), was developed for the 130 nm technology node. Introducing fluorine into silicon oxide reduced the dielectric constant to 3.6. Fluorine atoms, being highly electronegative, tend to strongly attract surrounding electrons, thus decreasing their mobility and the ability of the electron cloud to deform under an electric field. This reduces the structure's polarizability (Table 1.1). However, introducing too much fluorine ( $> 6\%$ ) promotes the formation of  $SiF_2$  groups, damaging the material reliability. A technological limit was then reached, necessitating the development of a new insulator.

From the 110 nm technology node, carbon and hydrogen-doped silicon oxide ( $SiO_xC_yH_z$ ), or Organo-Silicate Glass (OSG), was used as an insulator in interconnections. Introducing carbon and hydrogen into silicon oxide reduced the dielectric constant to 3. This low-dielectric constant insulator is traditionally called Low-k. Incorporating methyl groups ( $CH_3$ ) into an  $SiO_2$ -type structure reduces both the material's polarizability and density. Methyl groups exhibit lower polarizability than SiO groups (Table 1.1) and create additional "free volume" around them due to their significant steric hindrance. Thus, methyl groups decrease the density of bonds within the dielectric film, leading to a reduction in the material's dielectric constant as the rate of methyl groups increases.

From the 45 nm technology node, simply incorporating low polarizability elements into  $SiO_2$  is no longer sufficient to reduce the dielectric constant. The introduction of porosity within dielectrics reduces the density of polarizable bonds in the material, increases the free volume within the material, and thus decreases the material's density (Fig 1.2).

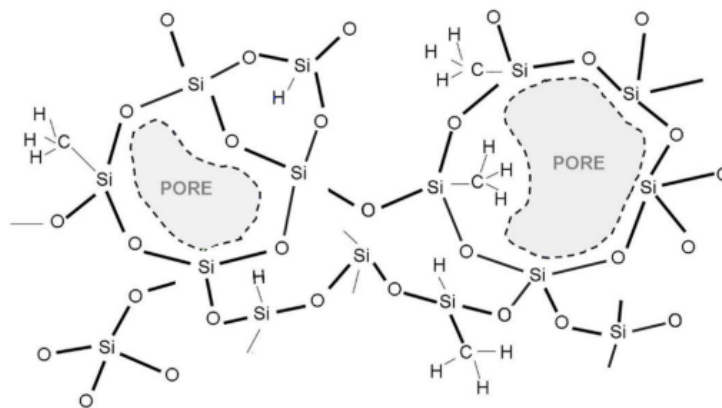


Figure 1.2: Bulk structure of ULK. Reproduced from Gourhant [2]

Incorporating porosity into carbon- and hydrogen-doped silicon dioxide, SiOCH, has lowered the dielectric constant to 2.5. This insulator, with a very low dielectric constant, is

traditionally called Ultra Low-k. It features about 20% porosity.

Among the materials found in interconnections, copper stands out due to its significant diffusion capability in dielectrics. This brings the risks of short circuits between interconnection lines and altering semiconductor properties. To address this issue, copper metal lines and vias must be effectively isolated by diffusion barrier layers. Initially, metal diffusion barriers are applied to the sides of lines and at the bottom of vias before the copper metallization step. These barriers aim to prevent copper diffusion into the dielectric through the pattern's sides, ensuring reliable adhesion between the copper and insulating material. Typically, these barriers consist of a stack of two layers: TaN for adhesion with the insulator and Ta as a copper deposition promoter. Additionally, dielectric diffusion barriers are deposited after the copper chemical mechanical polishing step, aiming to prevent copper diffusion into upper metal levels. To maintain integrated circuit reliability, these barriers must exhibit good adhesion between the underlying copper line and the interline insulating material. Introducing carbon-doped silicon oxide (SiOCH, previously cited) necessitated barriers with a lower dielectric constant than SiN, starting from the 90 nm technology node. SiCN encapsulation barriers lowered the dielectric constant from 7 (SiN) to 4 - 5 by reducing polar bonds through carbon introduction and decreasing material density due to steric hindrance from methyl groups. However, as discussed further, this material presents reliability challenges regarding moisture.

After providing contextual information on the evolution of materials in microelectronics, we will now focus on how moisture can penetrate inside a die and reach these sensitive dielectric layers.

## 1.2 Problematic

Reliability issues related to moisture in back end of line (BEOL) interconnections have been extensively investigated in the field of microelectronics. Various studies have been conducted to understand the mechanisms of moisture penetration, its effects on different dielectric materials, and the resulting degradation in interconnection reliability. We will present some of these studies later, but first, we present the technological protections implemented to prevent moisture penetration. Generally, chips are shielded by a polymeric encapsulation that connects the internal circuit to the external environment (Fig 1.3).

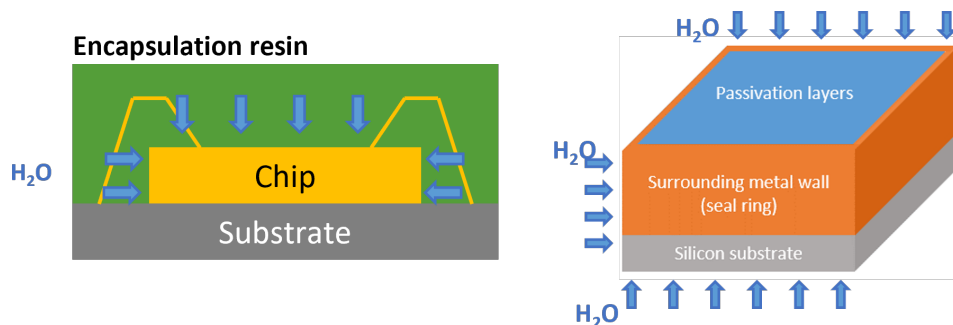


Figure 1.3: Schematic of the different protection against environmental contaminations of an integrated circuit



As expected, moisture is not intended to infiltrate the inner regions of an electronic circuit. The primary defense against moisture is provided by the chip enclosure, which bridges the internal circuitry to the external environment. Once moisture breaches the enclosure, it encounters the internal protective layers. Figure 1.3 illustrates a simplified diagram of protection against environmental contaminants :

- **Bottom-side diffusion:** Complete integration is performed on a silicon substrate known for its hermetic properties, thus shielding the chip from bottom-side diffusion.
- **Top-side diffusion:** Dense dielectric layers like silicon nitrides, termed passivation layers, are deposited to shield against top-side diffusion.
- **Lateral diffusion:** A continuous metal ring, also known as a seal ring, provides mechanical protection and shields against lateral diffusion.

Therefore, moisture penetration into the inner part of a microelectronic chip should be prevented.

However, moisture-related failure modes are occasionally observed. Defects in the seal ring or passivation layers can potentially permit moisture to reach the BEOL levels. These defects may include cracks in the passivation layer or via length that is too short in the seal ring (Fig 1.4) both of which provide pathways for moisture ingress.

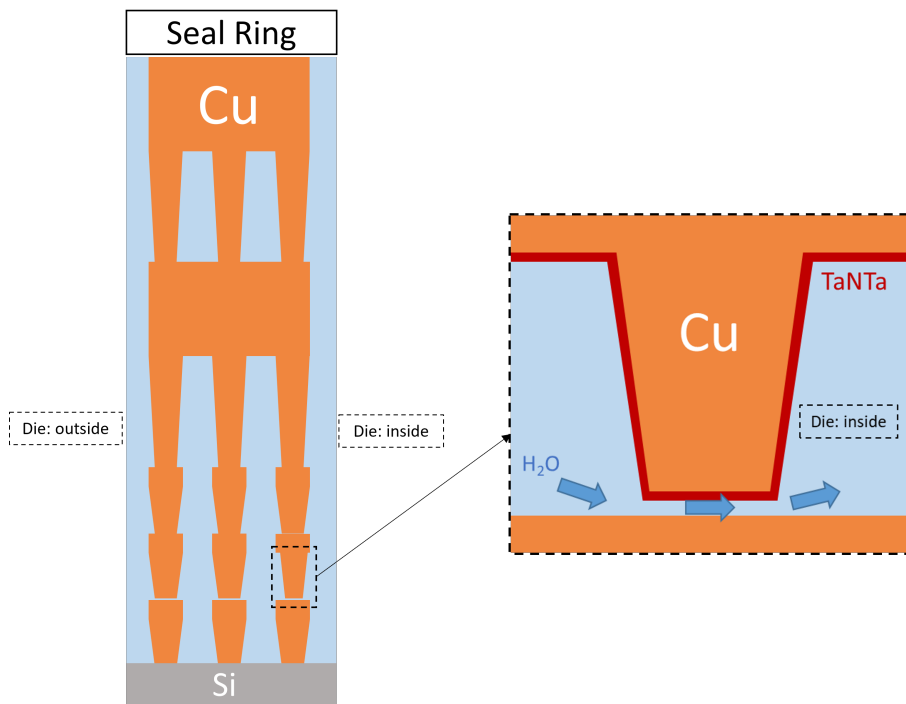


Figure 1.4: Schematic of seal ring non integrity defect

When moisture infiltrates the dielectric layers, it elevates the permittivity of the layer due to its high dielectric constant (around 79, whereas the dielectric constant of common silicon dioxide is around 4). This may pose challenges to die reliability and can affect among others signal transmission performances. For instance, to assess signal propagation performance in these structures, a commonly employed indicator used in microelectronics is the

product  $RC$ , where  $R$  represents the resistance of the metal lines and  $C$  the capacitance between conductors. Since the permittivity of dielectric directly influences the capacitance due between metallic lines, any increase in permittivity would affect signal propagation in the interconnections. So we pay attention to the dielectric constant of materials employed.

In the literature, most of the studies focus on moisture penetration during the process flow and not after deposition. Usually, a decrease in Time Dependent Dielectric Breakdown (TDDB) reliability is observed [13]. Triangular Voltage Sweep (TVS) tests and leakage current measurements are often used to have a better characterization of the degradation mechanisms due to moisture penetration [14]. These studies suggest the presence of moisture in two distinct states: physisorbed, characterized by weak bonds (hydrogen bonds), and chemisorbed, which exhibits a strong interaction with the material [10]. The chemisorbed moisture is commonly identified as the primary factor responsible for the limited reversibility of degradation observed in relation to dielectric properties [15]. One of the gaps in the literature is the connection between the behavior of bulk materials and their integrated form. The first objective of our study is to leverage the knowledge gained from the comprehensive humidity diffusion study in bulk materials conducted by Cartailier in his thesis work [5]. Results are presented in the following section.

A second recurring question in the literature, particularly relevant from an industrial point of view, concerns ageing tests and, more specifically, the acceleration factors between two test conditions. Typically, the three parameters studied are bias, temperature and relative humidity. In our study, we will focus on the last two parameters. The JEDEC standards can be found for the definition of an acceleration factor between two specific environmental conditions. For example, for diffusion in encapsulation polymers (often epoxy), JEDEC [16] presents an acceleration factor about 5 between the conditions  $30^{\circ}\text{C}/60\% \text{RH}$  and  $60^{\circ}\text{C}/60\% \text{RH}$ . Another JEDEC standard [17] states that 96 hours of Highly-Accelerated Temperature and Humidity Stress Test (HAST) storage at  $130^{\circ}\text{C}$  and  $85\% \text{RH}$  is equivalent to 1000 hours of storage at  $85^{\circ}\text{C}$  and  $85\% \text{RH}$  (acceleration factor of 10).

The problem lies in the direct adoption of empirical values of acceleration factors for studies that no longer concern diffusion in encapsulating polymers. As a general rule, industry standards are cycles of 1000 hours of temperature-humidity storage (THS) at  $85^{\circ}\text{C}/85\% \text{RH}$  and 96 hours of highly accelerated stress testing (HAST) at  $130^{\circ}\text{C}/85\% \text{RH}$ . However, each acceleration factor is specific to a degradation mechanism in a material environment and to various interactions. These approximations can lead to significant discrepancies in component lifetimes. Our second objective is therefore to identify and test an acceleration model for determining acceleration factors in our study of dielectrics in metallic interconnects.

Now that we have defined the study axes, let focus on preliminary work regarding moisture diffusion in bulk dielectric materials.

### 1.3 Previous work : bulk dielectrics

This section outlines Cartailier's study [5] on moisture diffusion in bulk dielectric materials. Various techniques were employed to characterize  $SiO_2$  (USG), dense SiOCH (low-k), porous SiOCH (ULK), and SiCN materials. Correlations between gravimetric tracking (mass variation), stress, and FTIR spectra were established, providing parameters for simulation models: moisture diffusion coefficient and saturation concentration, both dependent on storage conditions. The gravimetric method, which consist into monitoring mass variation of a dielectric layer on a hermetic Si substrate, is described in this section. Wafers have a diameter of 300 mm and layers thicknesses are 280 nm for low-k and 150 nm for SiCN (Fig1.5). Thus, the diffusion can be regarded as one-dimensional, in a semi-infinite plane structure. Moreover, silicon substrate has no influence on moisture uptake because it is an impermeable layer [11]. Since only one material is studied per wafer, diffusion coefficient can be considered homogeneous. Under these assumptions, extraction of diffusion coefficient ( $D$ ) and moisture saturated concentration ( $C_{sat}$ ) can be done using a simplified solution of the Fick diffusion law given by Crank [18].

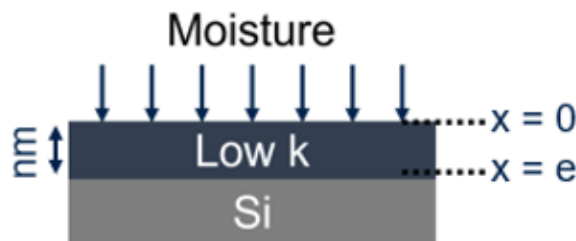


Figure 1.5: Schematic of single layer of Low-k deposit on a Silicon substrate

$$\frac{N(t)}{N_{\infty}} = 1 - \frac{8}{\pi^2} \sum_{i=0}^{\infty} \frac{1}{(2i+1)^2} \exp\left(-\frac{(2i+1)^2}{4} * \frac{\pi^2 Dt}{e^2}\right) \quad (1.1)$$

The number of water molecules that enter in the layer of thickness  $e$  at time  $t$  is expressed in Eq. 1.1. Where  $N(t)$  is the number of water molecules per unit surface area absorbed at time  $t$ ,  $N_{\infty}$  is the corresponding quantity after infinite time,  $D$  is the diffusion coefficient. This equation can be applied to any material property that is proportional to the parameter  $N(t)$  such as mass, moisture concentration, dielectric constant. Using the least squares method in Python™ between mathematical model and experimental data, the diffusion coefficient ( $D$ ) can be extracted.

The results of moisture concentration evolution regarding the time of storage for different dielectrics are presented in Fig 1.6. A good correlation between the Crank model and the experimental data can be seen. It is important to underline that the values for ULK and Low-k represent the bulk of the materials. These dielectrics are known to be impacted by integration steps. They partly become hydrophilic due to plasma effects [19]. Moreover, in integrated stacks, ULK is deposited on top of SiCN. In this case, a thin layer without carbon is first created to improve adhesion between SiCN and ULK (bulk).

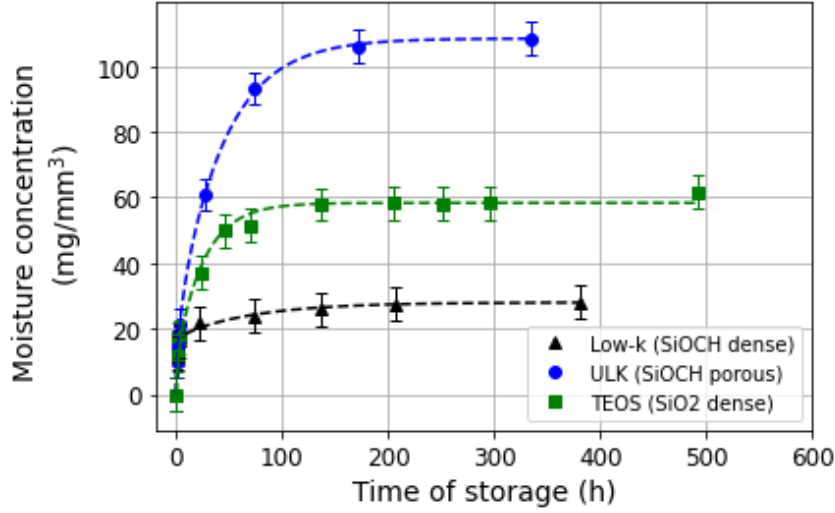


Figure 1.6: ULK, Low-k and USG moisture uptake during a 85°C/85%RH storage

For SiCN material, results are exposed in Fig.1.7. A non-Fickian behavior is observed. Indeed, it is not possible to fit experimental data with a single Crank model since two slopes are identified.

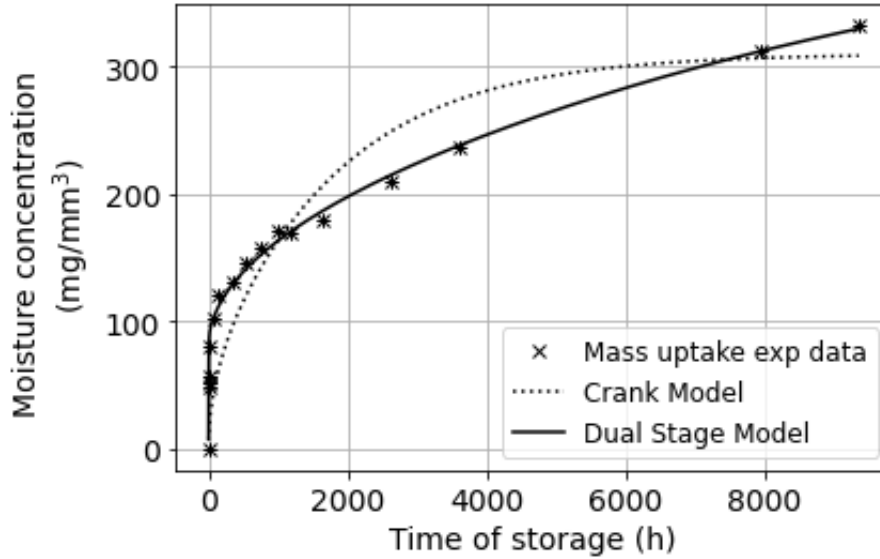


Figure 1.7: SiCN moisture uptake at 85°C/85%RH

Placette [20] showed that it was possible to model the non-Fickian model as a sum of two Fickian models (dual stage) for epoxy mold compounds. Same approach is used here. It is mathematically described as follows (eq. 1.2 and 1.3) for moisture concentration with  $n = 1$  (1<sup>st</sup> Fick) and  $n = 2$  (2<sup>nd</sup> Fick).

$$C_{H_2O}(t) = \sum_{n=1}^2 C_{n,\infty} * S_n \quad (1.2)$$

$$S_n = 1 - \frac{8}{\pi^2} \sum_{i=0}^{\infty} \frac{1}{(2i+1)^2} \exp\left(-\frac{(2i+1)^2 \pi^2 D_n t}{4e^2}\right) \quad (1.3)$$

This model does not explain the physical and chemical phenomenon behind the non Fickian absorption. These parameters are empirical and are meant to describe moisture absorption. Moreover, this approach gives a better fitting result than the simple Crank model for the Low-k dielectric. The diffusion coefficient and saturated concentration extracted for each fickian behavior (1<sup>st</sup> Fick, 2<sup>nd</sup> Fick) for SiCN are presented in Table 1.2. A comprehensive study of moisture sorption in SiCN has been proposed [6] by coupling data extracted from Tof SIMS and FTIR techniques. The fastest diffusion (1<sup>st</sup> Fick) during first hours is due to the easily accessible sites in SiCN due to its nanoporosity. Once all these sites are occupied, the oxidation process is only driven by chemical reactions (2<sup>nd</sup> Fick). Thus,  $D$  and  $C_{sat}$  values are required for both mechanisms, which is consistent with Placette approach. These parameters will be essential for the development of a moisture diffusion numerical simulation model.

	Parameters	USG	ULK	Low k	SiCN
1 <sup>st</sup> Fick	$D_1$ ( $m^2/s$ )	3.4E-19	2.6E-19	1.2E-19	8.7E-19
	$C_{sat,1}$ ( $mg/mm^3$ )	132.4	110	28	81.1
2 <sup>nd</sup> Fick	$D_2$ ( $m^2/s$ )				1.0E-22
	$C_{sat,2}$ ( $mg/mm^3$ )				577.0

Table 1.2: Bulk materials extracted properties at 85°C/85%RH

Regarding the results of stress and FTIR studies on moisture, two distinct behaviors emerge among various dielectrics. Dense SiO<sub>2</sub> (USG) and SiCN materials exhibit significant mechanical property alterations. Additionally, FTIR spectra results demonstrate the formation of strong chemical bonds between moisture and USG (also observed in SiCN), leading to modifications in material nanostructure, as depicted in Fig 1.8.

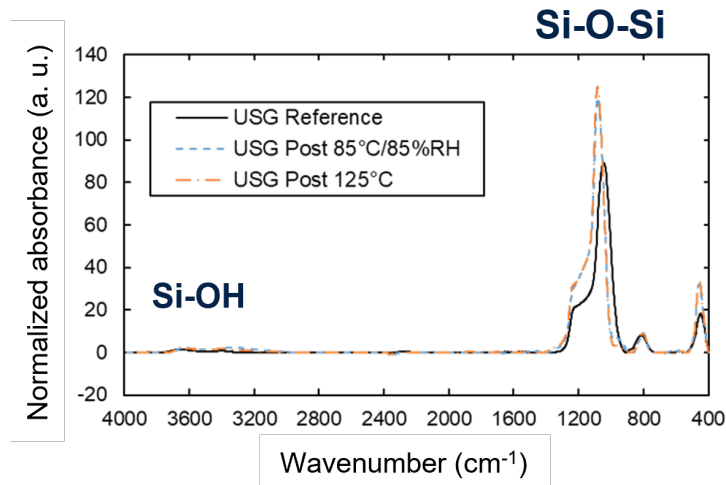


Figure 1.8: Infrared spectra of a USG stored at 85°C/85% RH and after 1600h of 125°C bake

Inversely, dense and porous SiOCH materials exhibit hydrophobic characteristics, as no influence of humidity on mechanical or physicochemical properties is observed (Fig 1.9). However, gravimetric measurements reveal  $27 \text{ mg.mm}^{-3}$  moisture uptake for Low-k

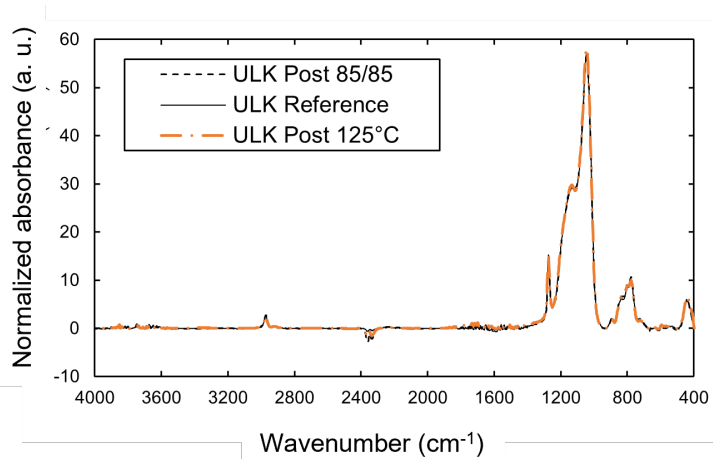


Figure 1.9: Infrared spectra of a ULK stored at 85°C/85% RH and after 1600h of 125°C bake

and more than  $100 \text{ mg.mm}^{-3}$  for ULK dielectrics. Cartailier concludes that moisture in these dielectrics is confined within the porous networks of these materials (9% for low-k, 20% for ULK), with little to no interaction with the hydrophobic bulk specific surface. Further details are available in the second chapter of Cartailier’s thesis [5].

The goal of this review was to extract the most relevant information from his work for our study. The objective of next chapter will be to exploit these results and experimental data to establish a numerical simulation model of moisture diffusion in integrated stacks. Before this, let introduce the samples and the characterization techniques employed during this work.

## 1.4 Samples and methods

A drawback of studying moisture degradation in integrated dielectric materials is the multitude of variable parameters from one study to another. These include materials, material combinations (main and capping), Front-End-of-Line (FEOL)/Back-End-of-Line (BEOL), integration processes (plasmas, CMP), sensor designs, dimensions, storage conditions, and time of moisture exposure. However, common results and hypotheses emerging from literature on integrated materials include:

- Increased dielectric constant due to water presence, with a dielectric constant of around 70 ;
- Partial reversibility of electrical properties due to chemically bound water presence, along with physisorbed (or free) water before desorption ;
- Degradation of semiconductor properties such as leakage current or breakdown field.

Ours study aims to highlight these three points for a BEOL integrated structure composed of low-k and SiCN.

### 1.4.1 Test chip description

As we saw earlier, the test chip is composed of successive layers of dielectrics stacked one above each other. In these stacks are implemented capacitance structure that will serve as sensors. The main dielectric is a 280 nm thick Low-k. The capping layer is a 40 nm thick SiCN. These layers are deposited by PECVD. After etching steps, TaN/Ta and copper metal lines are deposited. By doing so, MOM capacitance structures are created. On a single metal level, for example level 4 in Fig.1.11, the lateral capacitance is defined by two copper lines separated by low-k. Each metal level orientation is perpendicular to the one above (levels 4 and 5 are perpendicular). They are interconnected with metal vias. In this particular sensor, the vertical capacitances between two metal levels (L4 and L5) must also be considered. Thus, the total capacitance is the sum of the lateral (in grey) and vertical (in black) capacitance in Fig 1.11.

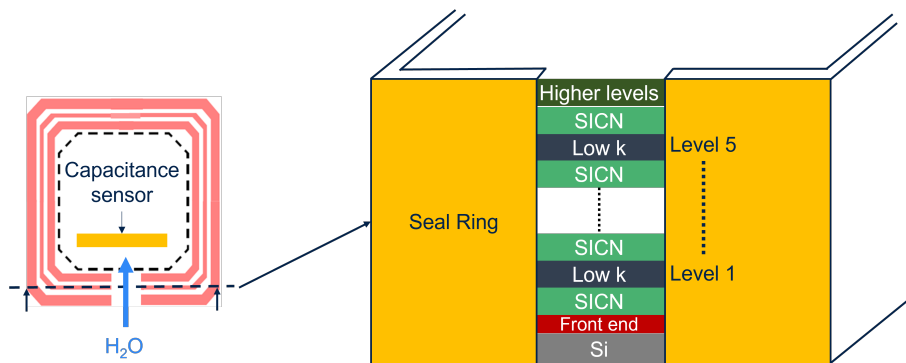


Figure 1.10: Schematic of the dielectric stack in the test chip

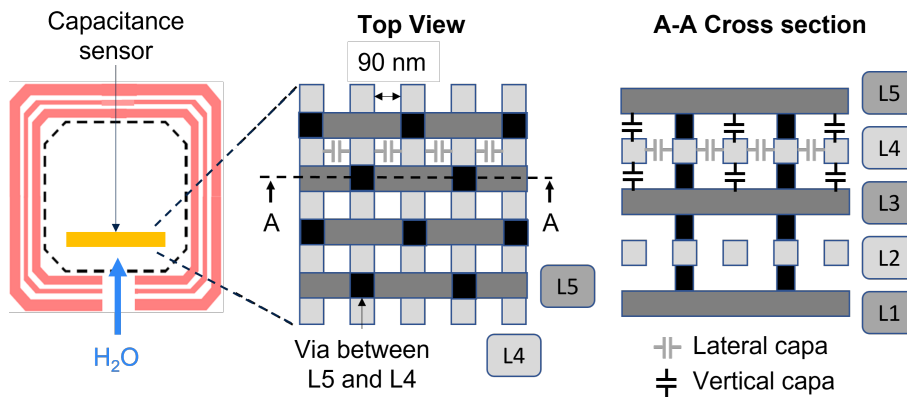


Figure 1.11: Top view schematic of test chip (left), Description of capacitance structures top view from level 5 (center), Cross section from L5 to L1 (right)

Finally, a seal ring wall is implemented to protect the die from mechanical and environmental stress. A 60  $\mu\text{m}$  opening across the entire thickness of the sample is intentionally left during design steps. In order to allow moisture to penetrate, partial sawing is performed in front of the 60  $\mu\text{m}$  opening. Within each wafer, 145 dies are fabricated, further subdivided into 231 capacitance sensors. This yields a total of 33 495 sensors per wafer. The sensors are grouped together in several mini seal rings of different configurations. The most classic is shown in Fig 1.10. The others will be detailed later in chapters 3 and 4.

Let focus now on how to exploit these samples. The next section presents the methodology for expose the samples to moisture and test them.

### 1.4.2 Methodology

As a reminder, the final objective of this work is to develop an acceleration model for moisture diffusion into integrated structures. The methodology is divided into two parts. First, we need to obtain experimental data on the evolution of moisture penetration using capacitance sensors. These data are obtained from various storage conditions at different temperatures and relative humidities. Once all the data are collected, the acceleration model can be developed.

The most challenging aspect of testing an acceleration model is to define a failure criterion. To determine the acceleration, it is essential to understand what is being accelerated. In other words, we need to identify a degradation mechanism common to all the storage conditions tested. In many studies, empirical failure criteria are often used (e.g., 10% relative resistance variation). In our case, there is no established criterion for moisture degradation in integrated moisture detectors (IMDs). Therefore, during the monitoring of moisture penetration, both material and electrical characterizations are performed. This will allow us to gain a better understanding of the degradation mechanisms and interactions of integrated dielectrics with moisture, thereby refining our future interpretations.

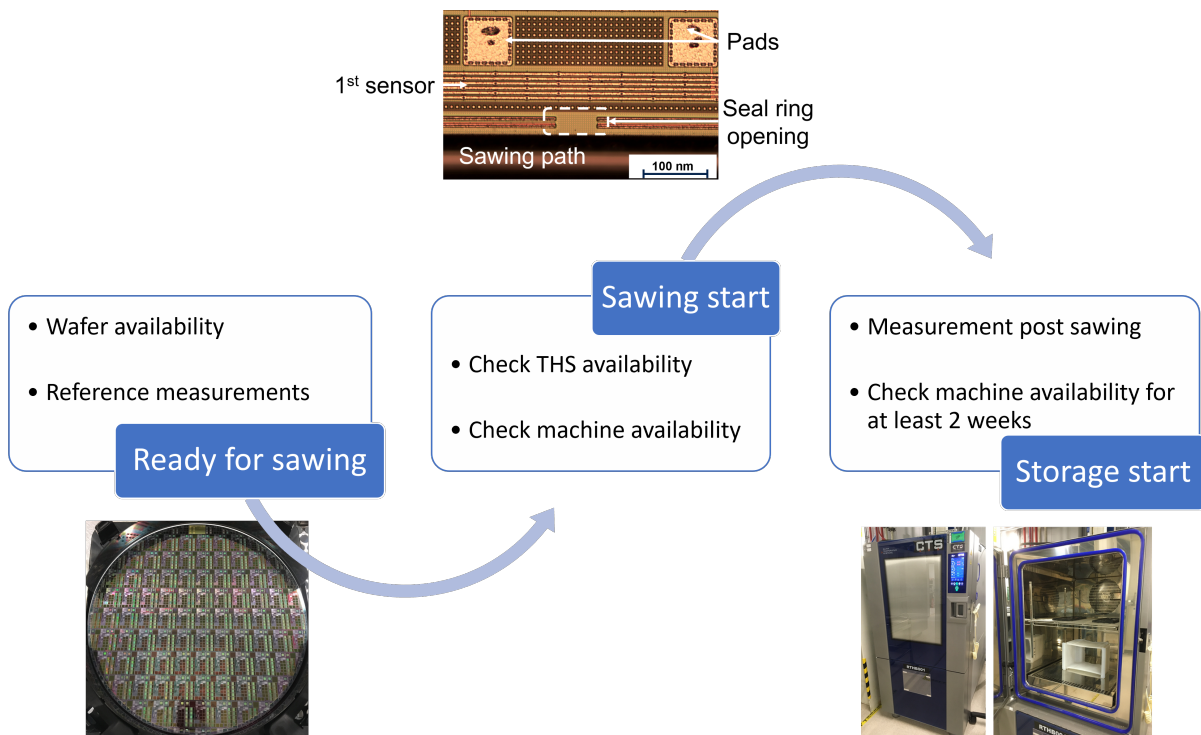


Figure 1.12: Methodology description

Regarding the monitoring of moisture penetration, Figure 1.12 outlines the several steps to be carried out for each wafer. The first step involves the reference measurement of the wafers before the sawing and exposure to humidity. The sawing is performed using laser grooving. The sawing process does not cut the entire thickness of the wafer (partial



sawing). Instead, it stops at the Si substrate, enabling the handling and testing of the entire wafers. This also prevents the samples from coming into contact with the liquid water used during this mechanical dicing that is used to cut the Si substrate.

All chips are measured both before and after sawing to confirm that no issues occurred during this process. Then, half of the chips are monitored through capacitance measurements for each storage condition. During this monitoring, leakage current measurements are also conducted. Since it is a destructive technique, a selection of the tested dies is made to ensure a sufficient number of chips remains for the final drying step. The selection process will be detailed in Chapter 3.

Now that we have reviewed the methodology and test structures, let introduce the several characterization techniques used.

### 1.4.3 Characterization techniques

Firstly, to elucidate the various types of samples studied for moisture exposure, controlled thermal humidity storage (THS) was employed. Most experiments were conducted below 100°C utilizing the climatic chamber depicted in Figure 1.12. This chamber accommodates temperature and relative humidity ranges from (10°C/10% RH) to (95°C/98% RH). However, due to limitations at atmospheric pressure, an alternative tool was utilized for experiments exceeding 100°C with elevated humidity levels. This second tool is pressurized, enabling the execution of Highly Accelerated Stress Tests (HAST) under standard conditions: 96 hours at 130°C and 85% RH. It will be interesting to examine whether the impact of pressure in HAST conditions alters the diffusion and degradation of moisture in our integrated structures compared to storage conditions at atmospheric pressure.

Regarding the characterization techniques employed, they can be categorized into two groups: physicochemical methods and electrical testing.

- **Physico-chemical Characterizations:**

Concerning the physico-chemical characterization, techniques such as Electron Energy Loss Spectroscopy (EELS) and Energy Dispersive X-ray Spectroscopy (EDX) were employed. These analysis were conducted after sample sectioning and scanning transmission electron microscopy (STEM) observation. TEM captures images using a broad electron beam across the entire sample simultaneously, excelling in structural analysis, while STEM scans the sample with a focused beam, constructing images point by point and offering superior spatial resolution. STEM's focused beam approach, combined with its use of multiple detectors, makes it better suited for EDX and EELS analyses, enabling precise elemental and chemical mapping at the nanometer or atomic scale.

It should be noted that EDX and EELS are two common characterization techniques used in materials science to analyze the chemical composition and electronic structure of materials. Both techniques involve the interaction of electrons with a sample, but they differ in the type of signal that is measured and the information that can be obtained. EDX involves bombarding a sample with an electron beam, which cause the sample to emit characteristic X-rays that are detected and analyzed. The energy of the emitted

X-rays corresponds to the atomic number of the element, allowing for the identification of the elements present in the sample. EDX can provide information on the elemental composition of a sample, but it cannot provide information on the electronic structure or chemical bonding. EELS, on the other hand, involves analyzing the energy loss of electrons that have passed through a thin sample (Fig 1.13).

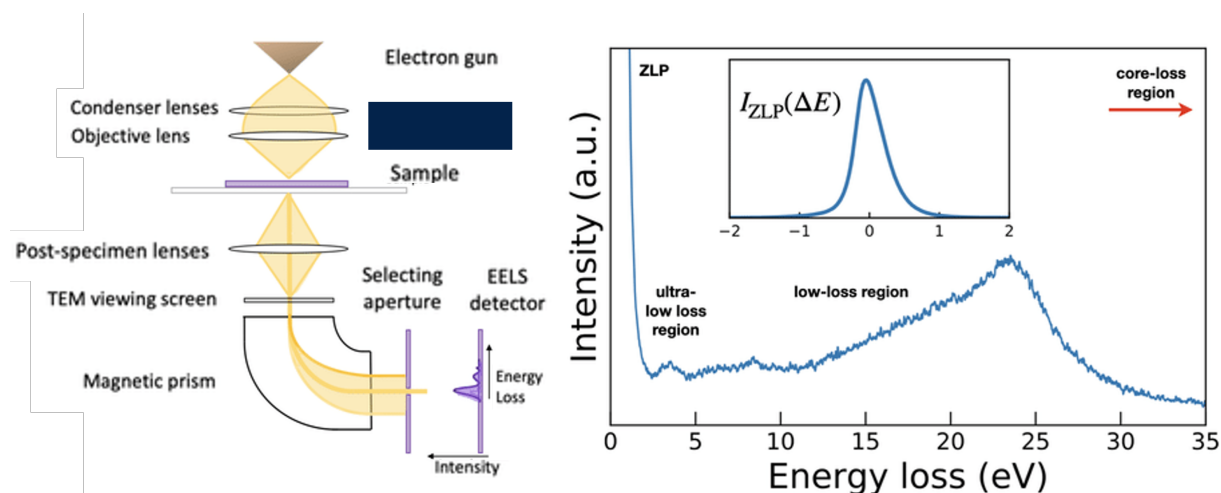


Figure 1.13: Schematic of STEM combine with EELS technique (extracted from [3])

As the electrons pass through the sample, they interact with the atoms and lose energy, creating a spectrum that reflects the electronic structure of the sample. EELS can provide information on the electronic structure, chemical bonding, and elemental composition of a sample. They are complementary techniques that can be used together to provide a more complete picture of the sample.

Additionally, Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) was used for further physico-chemical characterizations on bulk materials assembled without integration (without copper). ToF-SIMS is an advanced analytical technique used for surface characterization and analysis (Fig 1.14).

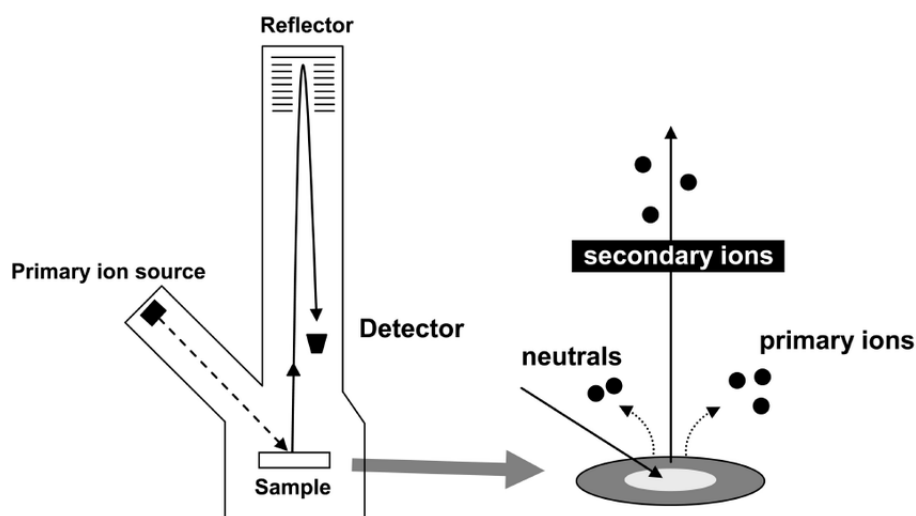


Figure 1.14: Schematic structure of the ToF-SIMS technique (extracted from [4])

This method involves bombarding a sample surface with a focused primary ion beam (in our case Cesium ions at 2 keV). This causes the ejection of secondary ions from the

surface. These secondary ions are then analyzed based on their time-of-flight, which allows for precise mass determination. ToF-SIMS provides detailed information about the chemical composition and molecular structure of the sample. It will be used to explore the moisture diffusion into the bulk and at the interfaces between the two dielectric layers.

The results of these material characterization techniques will be related to the capacitance variation observed. Therefore capacitance will serve as an indicator of moisture degradation.

- **Electrical Characterizations:**

The capacitance is influenced by both the dielectric materials and the dimensions of the copper combs. In an interdigitated finger capacitor, the total capacitance is the sum of all parallel capacitances, as illustrated in the simplified schematic in Fig. 1.15 and described by eq. 1.4:

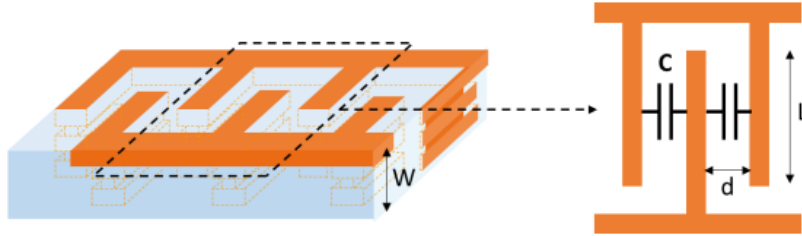


Figure 1.15: Schematic of interdigitated finger capacitor (extracted from [5])

$$C = (N - 1)\epsilon \frac{WL}{d} \quad (1.4)$$

In this context,  $W$  and  $L$  represent the width and length of the metal plates of the finger, respectively.  $N$  denotes the number of fingers,  $d$  is the distance between the two plates, and  $\epsilon$  is the permittivity of the material between the plates. The permittivity is related to the relative permittivity, or dielectric constant ( $\epsilon_r$ ), and the vacuum permittivity ( $\epsilon_0$ ,  $8.85 \times 10^{-12} \text{ F} \cdot \text{m}^{-1}$ ). Capacitance measurements were conducted using a Keysight Technologies E4980 LCR meter.

To evaluate the potential impact of temperature on the geometrical parameters (due to thermal expansion), we stored a reference structure at  $250^\circ\text{C}$ . No significant variations were observed, indicating that the geometrical parameters remain constant. Therefore, in this study, only moisture influences the capacitance variations. The observed capacitance changes are attributed to variations in the dielectric constant of each material in the presence of water.

The measurement frequency was determined by analyzing the magnitude of the complex impedance. The cutoff frequency, defined as the frequency at which a significant change in impedance behavior occurs, was found to be approximately 100 kHz. To avoid parasitic effects, all capacitance measurements were performed at a stable frequency of 10 kHz. The relative variation in capacitance due to humidity is depicted in eq.1.5. Where  $C(t)$  is the capacitance value measured at the instant  $t$  and  $C_{\text{ref}}$  is the capacitance measured before sawing steps.

$$\text{Relative capacitance variation (\%)} = 100 * \frac{C(t) - C_{\text{ref}}}{C_{\text{ref}}} \quad (1.5)$$

For the leakage current (I-V) measurements, the same Keysight Technologies was used. Measurements were taken using two manual probes. The applied voltage ramp ranged from 0 to 70 V. An example is shown in Fig 1.16 for a dry sample. The upper limit was determined from preliminary tests to identify the order of magnitude of the breakdown field ( $E_{bd}$ ). The electrical fields were accurately deduced from Transmission Electron Microscopy (TEM) analysis, which provides precise measurements of the distance between metal lines. The applied field is determined by dividing the applied voltage by the distance between the copper lines. This corresponds to electrical fields up to  $5 \text{ MV.cm}^{-1}$  for our test structures.

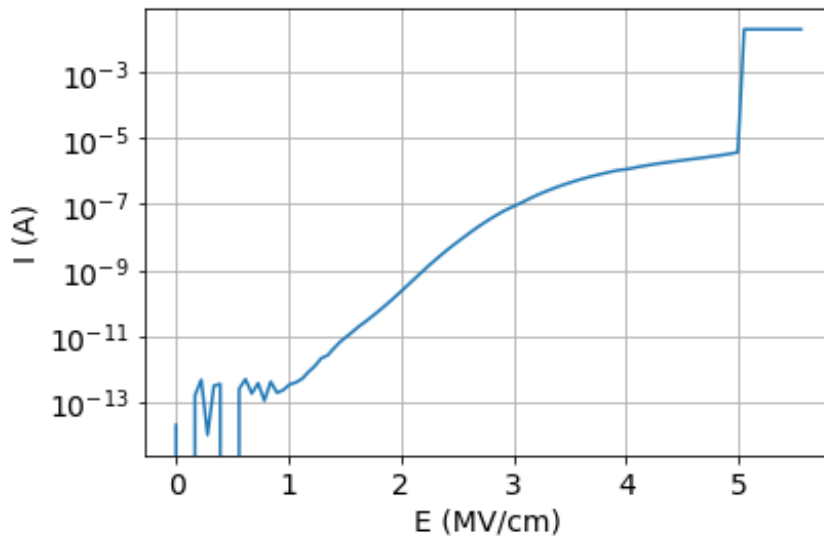


Figure 1.16: Example of leakage current (I-V) curve for a reference sample (without moisture)

The tester provides good precision in measuring the leakage current, which is on the order of  $10^{-12}$  A. However, the breakdown field exhibits a variation of 7 to 10%, likely due to fluctuations in the distance between the copper lines. This variability will be further discussed during the leakage current measurements conducted after the bake at  $250^\circ\text{C}$ .

## 1.5 Conclusion

In conclusion, this chapter has established the context for our study by providing a historical context and an overview of the materials employed in the metallic interconnections area. We saw that discontinuities may occur in the seal ring which could lead into moisture penetration inside dielectrics.

Before focusing on the impact of moisture into integrated dielectrics, the bulk materials behaviors have been presented. The results obtained by Cartailleur [5] allowed to identify two distinct behaviors concerning moisture penetration: hydrophilic and hydrophobic dielectrics. These behaviors significantly complicate the approach within integrated structures, a topic that will be further explored in the subsequent chapter. Moreover, we intend

to leverage the diffusion coefficient and the saturation concentration extracted from the previous work. These parameters will play a crucial role for the development of a numerical model. Additionally, the dual-stage approximation will serve as key information for our numerical simulation approach.

Finally, in this chapter we presented our methodology to follow moisture diffusion evolution through capacitance measurements. The main hypothesis considered in this work is that moisture content is proportional to the dielectric constant. This consideration might be simplistic as it probably does not reflect the physical reality, but as we will see, it may serve as a good first approximation for a study about moisture diffusion.

By highlighting the specific challenges and research areas related to the behavior of dielectric materials within integrated structures exposed to moisture, we have defined a clear direction for our study : Building an acceleration model based on material and electrical characterization experiments. The definition of a failure criteria for the acceleration model will be the most challenging task.

## Chapter 2

# Moisture path and materials degradation in integrated stacks

In this section, the primary objective is to gain a deeper understanding of the diffusion path and potential degradation associated with the presence of moisture in the IMD (inter-metallic dielectrics) area. This understanding will enable a more accurate interpretation of electrical degradation in a later step. Material characterizations are used as a basis to achieve this objective. Through this chapter we want to answer the following questions :

- (1) Are there any oxidation phenomena due to the presence of moisture ?
- (2) Are there any preferential diffusion paths for moisture ?

Then, by leveraging material parameters obtained from the previous thesis, a simulation method for moisture diffusion in integrated dielectrics is be developed. The research question that is addressed is:

- (3) Can the behavior of integrated structures be modeled based only on bulk material data ?

By answering these research questions, valuable insights into the impact of moisture on electrical performance and the underlying mechanisms that drive degradation can be obtained.

Efforts are focused on identifying oxidation phenomena that could be linked to degradation mechanisms in moist samples. This involves a suite of physico-chemical characterizations. First, TEM and STEM cross-sections are employed to highlight areas of interest. Subsequently, EDX and EELS analyses are conducted to obtain insights into the elemental composition evolution of these regions, as well as their surrounding environment. However, a limitation of this approach, as detailed later, is its inability to analyze oxygen content evolution at interfaces in contact with Low-k. (Parce que : mot de liaison) Given the initial high oxygen content of Low-k, variations are too subtle to be discernible.

To address this, an alternative approach is adopted, focusing on the elemental composition evolution of a sample representing a stack of dielectric layers (Low-k and SiCN) from integrated structures. In this case, the most suitable tool is ToF-SIMS, as shown further. Finally, the concluding segment of this chapter pertains to simulation models aimed at addressing the aforementioned questions.

## 2.1 Assessment of material degradations due to moisture

The objective of this section is to provide a comprehensive understanding of the moisture diffusion behavior in integrated dielectrics. Material characterizations are performed to understand the influence of the interfaces in a integrated configuration.

### 2.1.1 Methodology

The aim of this first study is to reveal traces of oxidation within the copper lines. To have a better visualization of the areas studied, the results of TEM cross-sections and EDX oxygen mapping on a dry sample are presented in figure 2.1.

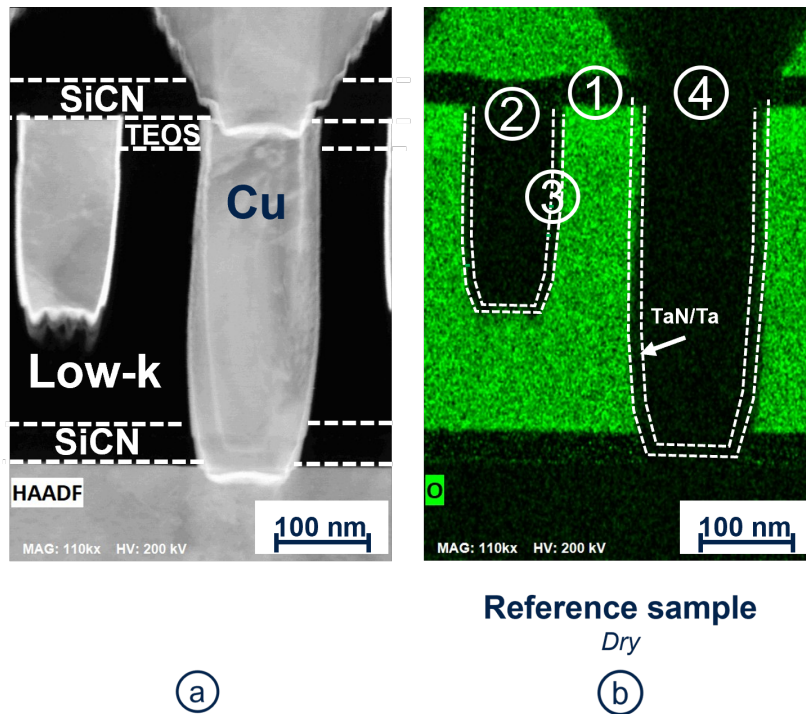


Figure 2.1: STEM (a), oxygen mapping for a dry sample (b)

Four key areas were selected for study :

- (1) SiCN : We expect an increase in oxygen and SiO levels as shown by Cartailier.
- (2) Interface between the copper line and SiCN.
- (3) Interface between the Copper, Tantalum barrier, and Low-k layer;
- (4) Via area.

These four areas were examined using EDX and EELS for four types of samples: a reference sample without humidity, two saturated humidity samples (one at ambient conditions and another at 85°C/85% RH) and a partially moisturized sample (at ambient conditions).



These represent the worst-case degradation study. The saturation state is defined by the capacity measurements detailed later (23% variation of relative capacitance). This approach allowed the monitoring of different chemical profile (Carbon, Oxygen, Nitrogen, Silicon, Copper) and their changes under storage conditions. Finally, a partially moist sample is analyzed by EDX to see if the same degradation mechanisms than saturated samples is observed.

It is essential to recognize that these analyses involve a significant amount of sample preparation work, from design, sawing, storage, electrical testing, TEM/STEM sample preparation, to data analysis and processing. This process is the result of collaboration between different STMicroelectronics departments, involving design teams, sawing specialists and CARPHY material characterization teams. Our main responsibility was to supervise the various stages, while managing storage, electrical testing and data processing. The final step was to discuss the results with experts in characterization methods, to ensure full understanding and interpretation of the results.

### 2.1.2 Results of physico-chemical analysis

The results of the EDX analysis on samples saturated with humidity after storage at 85°C/85%RH are presented in Fig 2.2. The oxygen mapping of the saturated sample is compared with the previous reference. Different impacted areas are observed, such as the SiCN layer (1), the interface between the SiCN and copper (2), copper/TaN/Ta/low-k (3) as well as the via zones (4).

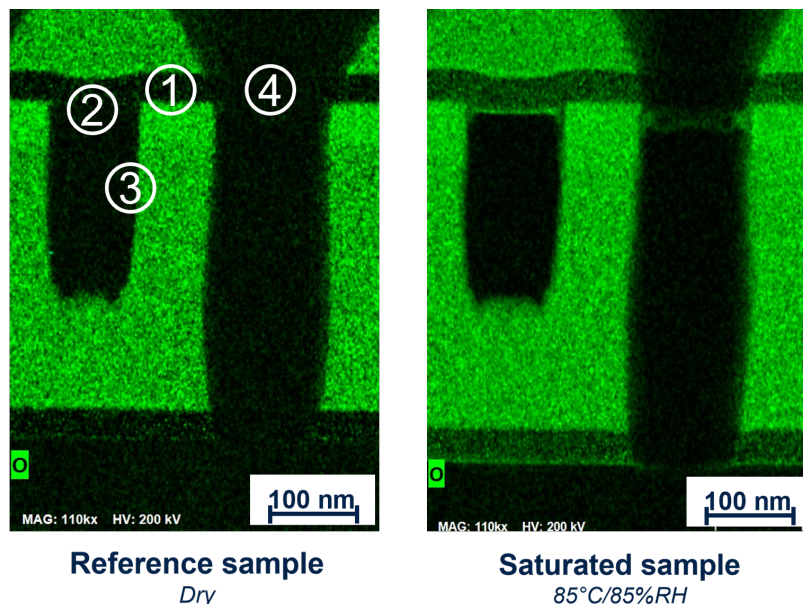


Figure 2.2: EDX oxygen mapping for the reference (left) and the saturated samples at 85°C/85%RH (right)

- **SiCN layer (1) and copper interface (2):**

The focus is initially on the SiCN layer. The linescan of the different elements (red arrow) is presented in Fig 2.3.



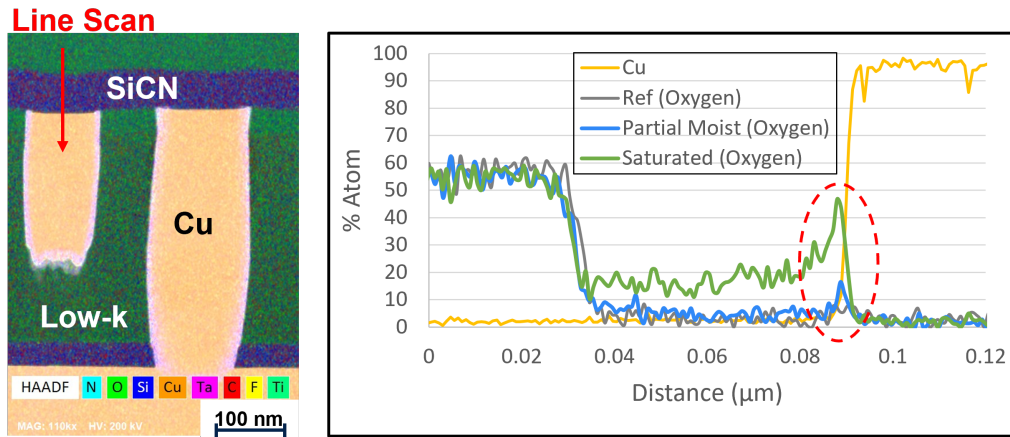


Figure 2.3: EDX linescan for the reference, partially moist and saturated samples after an 85°C/85%RH storage

Firstly, it is confirmed that there is no presence of oxygen in the SiCN and at the interfaces in the dry reference sample. For the partially wet sample, there is also no variation in the oxygen profile in the SiCN layer. However, an oxygen peak begins to appear at the SiCN/Cu interface (at 0.09 nm). For the saturated sample, a significant increase in the oxygen content in the SiCN volume is observed, as well as an even more significant peak at the interface with copper. The increase of oxygen content in the SiCN volume is consistent with the study of bulk materials. Indeed, an increase in SiO bonding in this layer was demonstrated through FTIR analysis [6]. Since the increase in oxygen is observed preferentially at the interface rather than in the SiCN volume for the partially wet sample, it is suspected that diffusion in the SiCN volume occurs after propagation at the interface. The question that arises with respect to this oxygen peak, is whether it corresponds to oxidized copper or moisture linked (or unlinked) to the SiCN.

To address this, an EELS analysis of the oxygen state in this zone was performed. Three spectra of the copper signal are presented in Fig 2.4 for the bulk SiCN region (blue), Cu interface (red), and Cu bulk (green) on the reference sample.

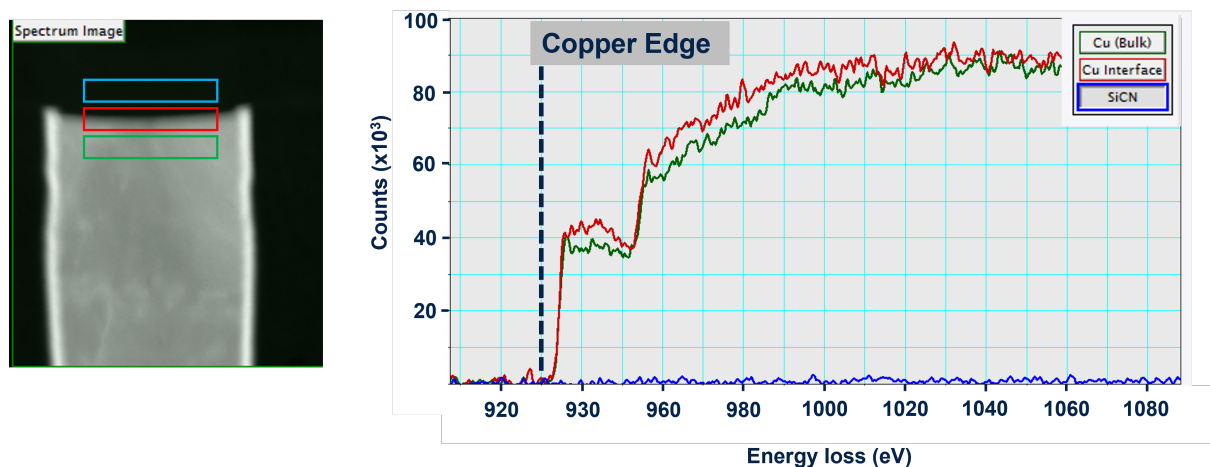


Figure 2.4: EELS spectra of Cu signal in the bulk of copper line and at the interface with SiCN layer of reference sample after a 85°C/85%RH storage

The EELS analysis shows a copper edge at 935 eV for bulk copper (green), confirming the presence of metallic copper in the line. The spectrum of copper at the interface (red) overlaps the one of bulk copper, indicating that there is no oxidation. Finally, the absence of a copper signal in the SiCN layer is consistent with the intended function of this layer, which is to prevent copper diffusion into the low-k layer. Figure 2.5 presents the EELS spectra for the sample saturated at 85°C/85%RH, which includes the same three spectra as before.

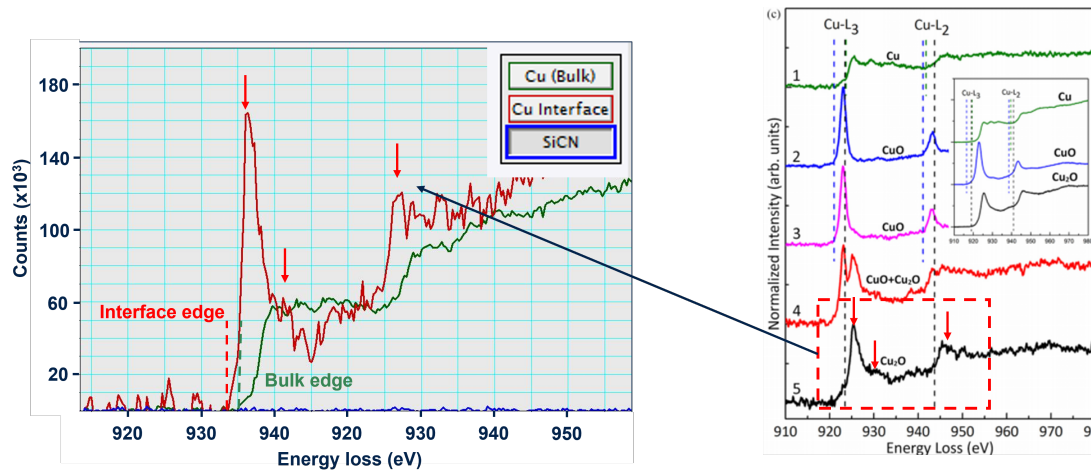


Figure 2.5: EELS spectra of Cu signal in the bulk of copper line (green) and at the interface with SiCN layer of saturated sample (red) after a 85°C/85%RH storage

A difference is observed between the two signals (red and green), notably with the shift of the edge value (from 936 to 933 eV). This indicates that there is a chemical shift between both copper spectras. Thus, copper is in a different chemical environment at the interface than in a copper line, likely linked to oxygen. The literature identifies the Cu<sub>2</sub>O phase, as seen in Figure 2.5b, which represents the EELS spectra of different oxidized phases of copper.

In addition, using an EELS mapping in Fig 2.6, the thickness extracted of the Cu<sub>2</sub>O layer is 8.5 nm. The formation of a cuprous oxide on the surface of the copper line is also observed during hybrid bonding, with a thickness of approximately 3.5 nm, which forms during planarization steps such as Chemical Mechanical Polishing (CMP), cleaning, and so on.

### • Tantalum barrier (3):

An EELS analysis was also performed to obtain the oxygen spectra at the lateral interfaces. A mapping and a linescan of oxygen is presented in Fig 2.7. Firstly, the oxygen energy spectrum in red in the figure shows a typical signal of oxygen bounds to silicon. Once again, a chemical shift is observed for the blue spectra in the tantalum barrier. Since this blue spectra is different than the one of the cuprous oxide identified in the previous section, we can conclude that the tantalum barrier that is oxidated. It is not possible to conclude about the oxide phase formed because of information is missing in the literature. Yet, it confirms the presence of moisture at the vertical interfaces of copper lines.

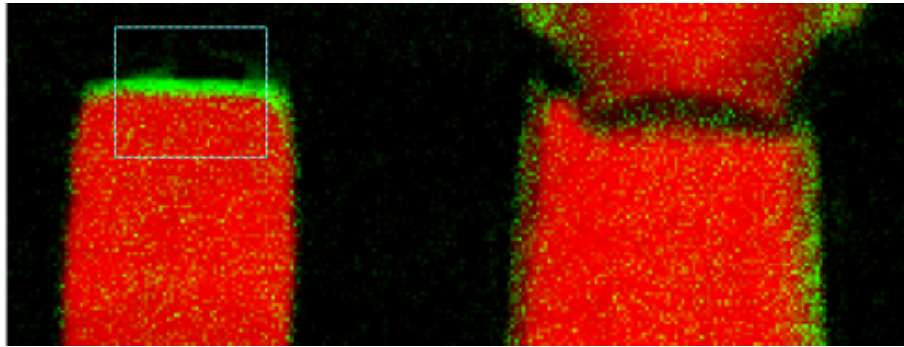


Figure 2.6: EELS mapping combining Cu "bulk" and Cu bonded to oxygen signals after a 85°C/85%RH storage

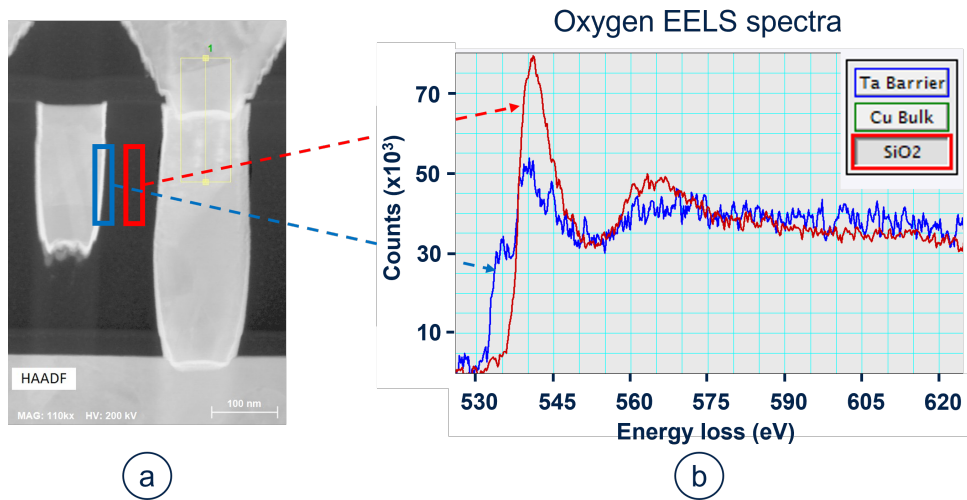


Figure 2.7: STEM imaging (a), Oxygen EELS spectra in bulk of low-k and at Tantalum interface (b) after a 85°C/85%RH storage

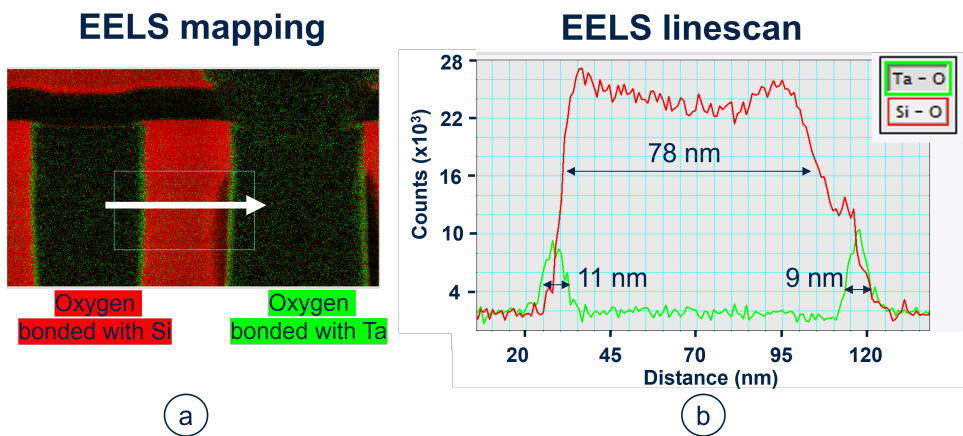
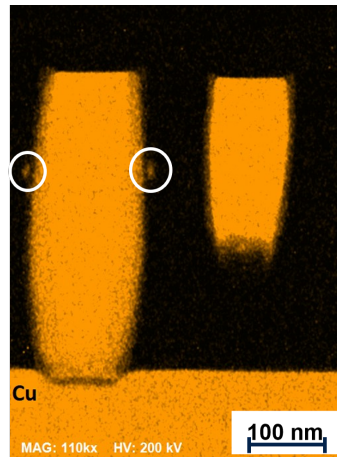


Figure 2.8: EELS mapping combining Si and Ta bonded oxygen signals (a), EELS lateral linescan of same elements (b) after a 85°C/85%RH storage

By performing a mapping and a linescan of oxygen bounded to Si (hence to low-k) or bounded to Ta, Fig 2.8a and b are obtained. The white arrow in the mapping indicates the direction of the linescan. By using these results, a tantalum oxide thickness of

approximately 10 nm is identified on samples saturated with humidity at 85°C/85%RH. Ito [21] and Baek [22] have shown that tantalum oxidizes easily to  $Ta_2O_5$  in the presence of oxygen and can no longer stop copper diffusion. They also demonstrated a reduction in TaN thickness with an initial layer of 20 nm. However, with such thick layer copper diffusion barrier is kept. Since the TaN layer in our structures is around 10 nm thick, we suspect that the thickness reduction due to moisture degradation could compromise the copper diffusion barrier property.



**Saturated sample**  
85°C/85%RH

Figure 2.9: EDX mapping for copper for saturated sample (85°C/85%RH storage)

Moreover, an EDX mapping on a sample stored for 4500h at 85/85 showed traces of copper diffusion. This failure mechanism is well-known in the literature and is primarily characterized by its irreversible nature [13] [23]. Once copper ions infiltrate the Low-k dielectric materials, they induce a notable increase in leakage current density and a consequential degradation in the dielectric breakdown field and TDDB lifetime. This showcases an irreversible negative correlation between copper diffusion and the reliability of the dielectric materials. This result is also observed by Cartailier in ULK (Ultra low-k) stacks described in [6] after saturation for the same environmental conditions as presented in Fig 2.10. The diffusion length found by Cartailier is about 20 to 25 nm.

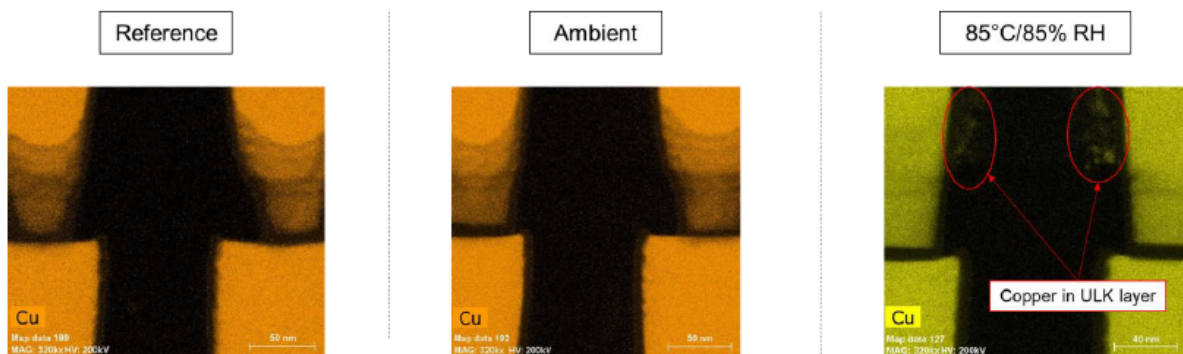


Figure 2.10: EDX mapping for copper for the three types of samples (color difference is due to the two analysis being performed separately) [6]

The presence of copper in dielectrics represents a degradation mechanism that must be carefully considered when comparing different storage conditions. Furthermore, if electrical degradation observed during testing is irreversible, it strongly suggests that copper diffusion plays a significant role.

To confirm this observation, EDX analysis was conducted on three additional samples stored under the same conditions. The results showed no trace of copper diffusion. Since this degradation mechanism is not observed systematically, we cannot definitively conclude that the degradation of the TaN/Ta barrier leads to copper diffusion. However, this finding suggests that particular attention must be paid during reliability tests conducted under 85°C/85% RH storage conditions. It may indicate that the condition 85°C/85% is not fully equivalent to the effects of ambient storage. We will examine this point in greater detail when we discuss the results of electrical degradation.

- **Via (4):**

The via region was analyzed to investigate the presence of oxidation. The linescan performed in this zone for the saturated sample is shown in Fig 2.11 (red arrow). A slight increase in oxygen is observed in the tantalum layer, indicating tantalum oxidation after a 85°C/85%RH storage.

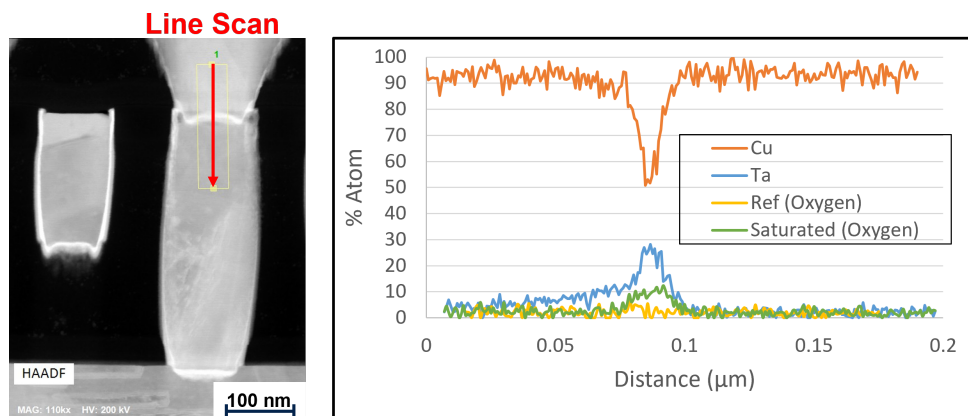


Figure 2.11: EDX linescan of bottom via area for the reference and saturated samples (85°C/85%RH storage)

To further investigate this, an EELS analysis was performed in this region (Fig 2.12). A weak oxygen signal was observed at the bottom of the via, which was difficult to compare to literature due to its low intensity and noise. However, the spectrum obtained for copper is the same as bulk one, confirming that there is no copper oxidation. These results, coupled with the observation of tantalum oxide at the lateral interfaces (Cu/TaN/Ta/low-k), indicate tantalum oxidation all around line/via areas. This finding is particularly interesting as it could potentially be used to define a failure criterion. Simple line/via resistance measurements could provide information on circuit performance and the impact of this via oxidation. This will be discussed in more detail in the final chapter.

In the literature, several studies discuss the effect of oxide formation on the reliability degradation. An impact on electromigration tests has been observed by researchers, indicating that electromigration, the gradual movement of metal atoms in a conductor due to momentum transfer from conducting electrons to metal ions, is a notable phenomenon.



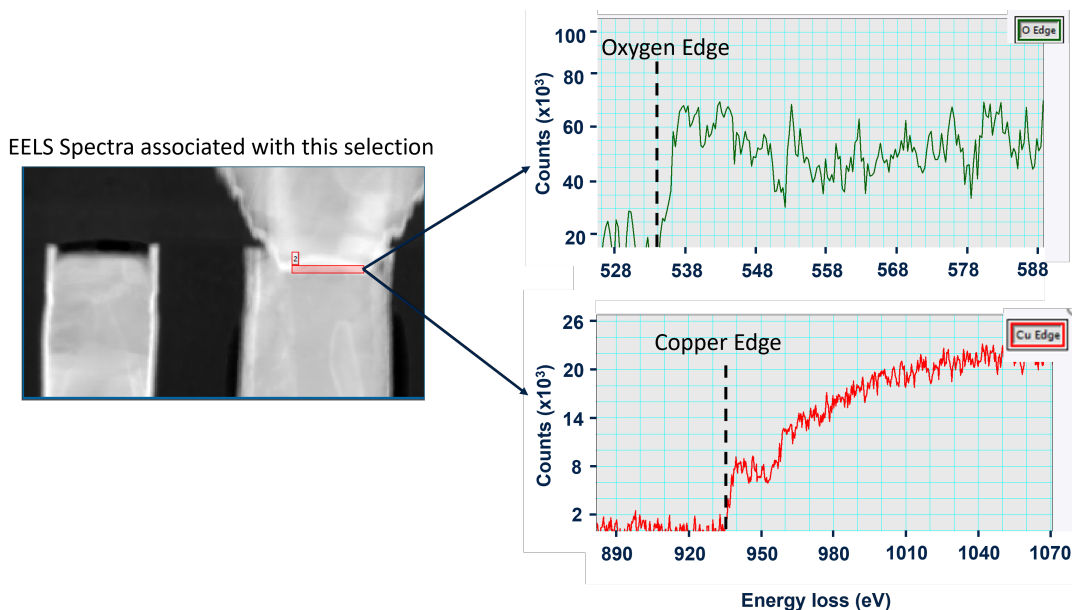


Figure 2.12: EELS spectras for oxygen and copper at bottom via area for the saturated samples after a 85°C/85%RH storage

This process, prevalent in electrical circuits under high current densities, can cause the failure of electrical connections as atoms move, creating voids or hillocks that eventually lead to open or short circuits. Given the trend towards miniaturization in microelectronic devices, electromigration represents a significant reliability concern due to increased current densities in smaller components.

Interestingly, one study [24] highlighted that the formation of tantalum oxide at the Low-k Ta interface could offer substantial protection against electromigration and reduce the resistance of Cu lines." However, it also pointed out that the Cu SiN interface is a preferred path for electromigration, with the fitted activation energy  $E_a$  being very close to that reported for Cu capped with SiN. These studies did not investigate the presence of copper oxide at this level, as identified for SiCN, yet the SiN layer is known for its hermetic properties, as demonstrated by Cartailleur. The susceptibility of SiCN to moisture might promote humidity at this interface, potentially leading to the formation of copper oxide. More over, the observed cuprous oxide layer is not controlled, homogeneous, or uniform. If the  $Cu_2O$  layer is defective or unevenly formed, it could enhance the diffusion of Cu ions under electric fields, accelerating electromigration degradation. This interface could be critical for the overall reliability.

### 2.1.3 Equivalence between storage conditions

We have reported that all interfaces related to the copper lines are impacted after a storage of 4500 hours at THS 85°C/85%RH. We may wonder whether ambient storage offers same observation after a long time storage (saturation). The goal is to compare the previous EDX and EELS results to saturated samples at ambient storage (23°C/45%RH). The establishment of an acceleration model in chapter 4 for moisture degradation requires the identification of similar degradation mechanisms between different storage conditions. In the absence of such similarities, it is crucial to identify potentially distinct mechanisms.

Fig 2.14 provides a summary of this comparison.

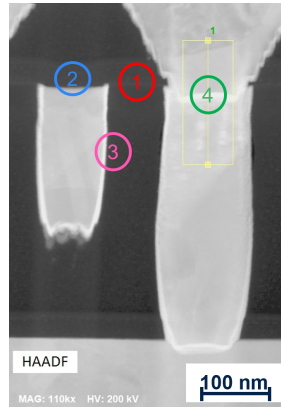


Figure 2.13: STEM image illustrating the different areas compared

85°C/85%RH	Ambient (23°C/45%RH)
① Diffusion of <b>Oxygen detected in SiCN Layer</b>	① Diffusion of <b>Oxygen detected in SiCN Layer</b>
② Presence of <b>copper oxide</b> on the top of Copper line	② Slight <b>copper oxide</b> in the interface
③ - Presence of <b>Oxygen bonded with Tantalum</b> - <b>Copper diffusion</b> may happen	③ - Presence of <b>Oxygen bonded with Tantalum</b> - <b>Copper diffusion</b> not observed
④ Presence of <b>Oxygen bonded with Tantalum</b>	④ <b>No presence</b> of Oxygen or copper oxide

Figure 2.14: Summary of moisture degradation after 85°C/85%RH and Ambient (23°C/45%RH storages)

The analysis of the SiCN layer (zone 1 in Fig 2.14) confirms the presence of oxygen for both storage conditions. At the interface between SiCN and copper line (zone 2), we have observed the formation of an 8.5 nm layer of  $\text{Cu}_2\text{O}$  on the surface of the copper line at 85°C/85%RH. For ambient storage, EELS analysis also reveals the presence of oxygen at the surface of the copper but the signal is too weak and noisy to identify a phase of oxidized copper which means it is a tiny oxidation. The cuprous oxide layer formation and dimensions likely depends on the storage conditions, particularly the temperature. Nevertheless, this degradation mechanism can be classified as common to both storage conditions.

Regarding the side walls of the copper lines (TaN/Ta interface) (3), we have observed oxidation of the TaN/Ta barrier at 85°C/85%RH, which can potentially lead to the diffusion of copper into the Low-k material. For ambient storage, we also observe the oxidation of the tantalum barrier, with a thickness of 5 nm compared to 10 nm for storage at 85°C/85%RH. This confirms the vertical diffusion of humidity at this interface for both storage. The difference here is that there is no trace of copper diffusion into the Low-k material at ambient storage. The copper barrier property is therefore maintained despite the oxidation. This result does not exclude the possibility that the acceleration of the TaN/Ta degradation with the storage conditions may cause copper diffusion. In such case, with a longer storage time, copper diffusion into the Low-k material could

potentially be observed at ambient storage. However, since this result is not observed here, copper diffusion can be considered as a degradation mechanism that occurs only at 85°C/85%RH (for the studied storage times). Therefore, we have a first degradation mechanism that is not equivalent between the two storage conditions.

Finally, at the via zone (4), we do not observe any via oxidation for ambient storage. This also marks a difference with the results of accelerated storage at 85°C/85%RH, for which a tantalum oxide has been identified. This result is interesting because, as previously described, simple resistance measurements can be used to determine when via oxidation becomes problematic and, consequently, when storages are no longer equivalent. Unfortunately, with our data, it is not possible to determine this, but this point represents an important perspective for this work.

Overall, our findings suggest that the degradation mechanisms observed for the two storage conditions are not entirely equivalent. While the oxidation of the TaN/Ta barrier is observed for both storage conditions, copper diffusion into the Low-k material is only observed for accelerated storage at 85°C/85%RH. The absence of via oxidation for ambient storage is also a notable difference from accelerated storage at 85°C/85%RH. These findings underscore the importance of identifying and characterizing degradation mechanisms under different storage conditions to establish an acceleration model for the degradation process.

## 2.2 Characterization of dielectrics interfaces

The approach for assessing moisture diffusion at the Low-K/SiCN interface involves conducting Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS). Due to the size of the sputtered area of ToF-SIMS (larger than the dimensions involved in the integrated stacks), direct utilization of this technique on the dies was not feasible as copper density would present a significant issue.

### 2.2.1 Deuterium experiment description

The ToF SIMS analysis is done after exposure to a humid environment containing deuterated water. Unlike hydrogen, deuterium is absent in the reference sample. Moreover, deuterium is both heavier and more stable than hydrogen atoms, making it more easily detectable in ToF-SIMS spectra. The dielectric stack with Low-k material was separately reproduced at the wafer level. Only dielectric materials were deposited, as depicted in Fig 2.15. The study also encompasses two other dielectric materials widely used in microelectronics, namely ULK (Ultra-Low-k) and USG (Undoped Silicon Glass, SiO<sub>2</sub>). The first category of samples (Fig 2.15a) consists of Low-k and SiCN layers. In its integrated structure, there is a thin layer of TEOS (dense SiO<sub>2</sub>) deposited above the Low-k, serving as a stop layer during the polishing steps. In order to ensure that moisture diffusion occurs exclusively through the sides and not from the top, a hermetic SiN passivation layer is deposited.



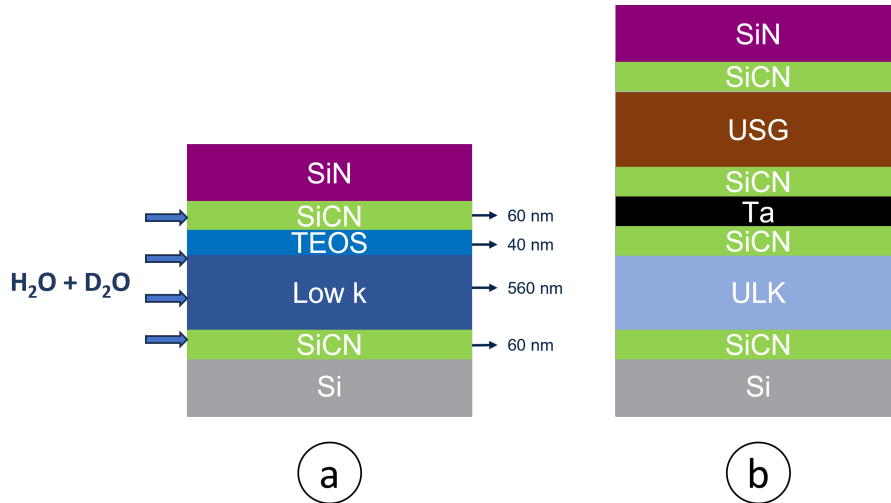


Figure 2.15: Schematic of the 2 different types of samples

This experiment was also conducted on a sample replicating a stack of 3D imaging technologies with an upper die made of USG as dielectric and a lower die made of ULK, both encapsulated by SiCN layers (Fig 2.15). The detailed structure of the integrated 3D stack is not described here but can be found in [25]. This stack was chosen because Cartailier demonstrated that there is no variation in capacitance for integrated structures composed of USG, whereas those with ULK can vary by up to 40% over the same storage period and storage conditions. This results was surprising since we have seen that USG is hydrophilic and ULK hydrophobic. This difference likely indicates distinct moisture transport behavior from the 60 microns openings to the sensors. A Tantalum layer is added to help distinguish between the upper and bottom parts and with no risk of moisture travelling between upper and lower stack.

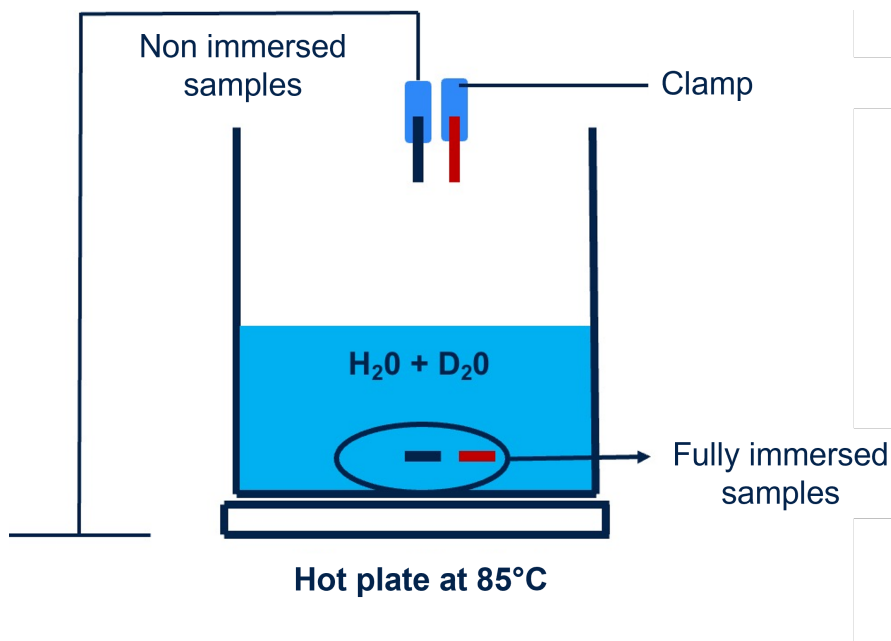


Figure 2.16: Schematic deuterium experiment exposure

The samples are submerged in a mixture of deionized water and heavy water (Dilution factor: 1/5) maintained at 85°C for 8 hours (Fig 2.16). A stand was added to keep certain samples close to the surface without direct contact with the water to evaluate if there is a difference between liquid water and water vapor. It is important to note that during the experiment we cannot ensure that the air temperature and relative humidity are precisely at 85°C/85%RH above the beaker. This experiment is qualitative and experimental in nature, not quantitative. Finally, samples are stored in a nitrogen controlled environment to minimize desorption while awaiting ToF-SIMS analysis availability. The analysis is conducted using a 2 keV Cesium ion beam on a surface located 500 μm from the edges, as illustrated in Fig 2.17, on the reference sample (Low-K/SiCN).

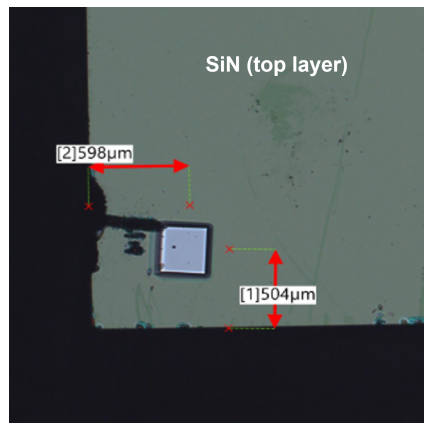


Figure 2.17: ToF-SIMS analyzed area on microscope top view of Low-k/SiCN reference sample

### 2.2.2 Reference sample

The different material layers can be identified by analyzing the elemental profiles, including carbon, SiN, oxygen, and silicon regarding the erosion time of the ion beam. For instance, in the case of Low-k (Fig 2.18), the carbon and nitrogen profiles show that the SiN layer ends at 2075 seconds of erosion.

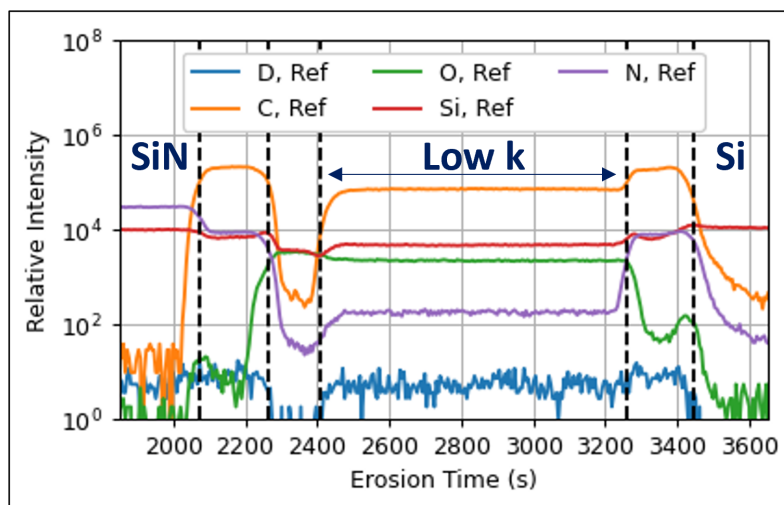


Figure 2.18: ToF SIMS spectras for Low-k reference sample

Afterward, the carbon profile increases, corresponding to the SiCN layer, and finally, there is a consequent increase in the oxygen profile at 2265 seconds, indicating the TEOS layer just before the bulk of the Low-k at 2400 seconds. Regions showing significant elemental gradients between two layers are considered as interfaces. Finally, we confirm the absence of deuterium in the reference samples, although it may seem obvious. The same method is applied to the USG and ULK samples in Fig 2.19 a and b.

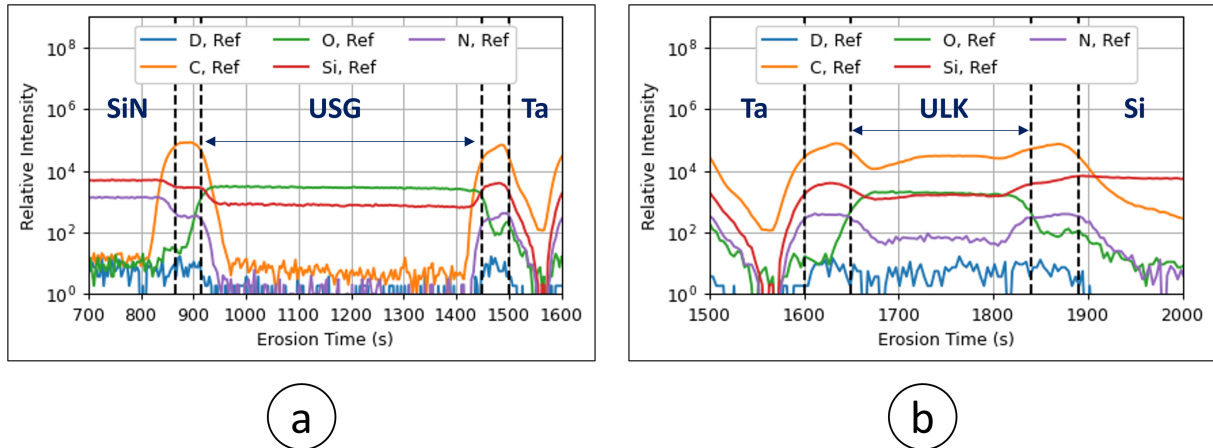


Figure 2.19: ToF SIMS spectras for USG (a), ULK (b) reference sample

### 2.2.3 Moist samples

In this section, the results of the ToF-SIMS analysis are presented for the three dielectrics (Low-k, ULK, USG) under study.

- **ULK :**

For the ULK based samples, we present the results for the fully immersed, near the surface, and far from the surface samples in Fig 2.20.

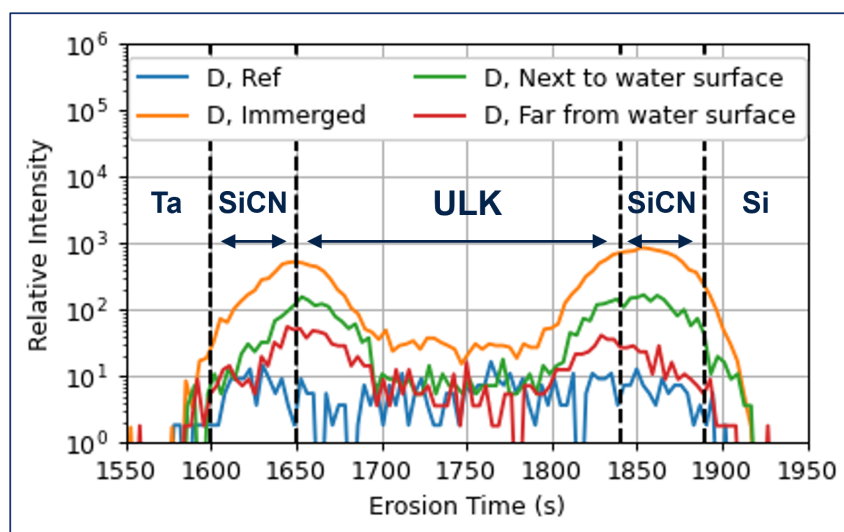


Figure 2.20: ToF SIMS deuterium spectra for ULK samples after moisture exposure

Two distinct deuterium peaks are clearly observed at the interfaces between ULK and SiCN layers (1650 and 1850 seconds) for all the exposed samples. The intensity of these peaks increases with the proximity to the liquid surface. The difference between the immersed sample and those near the surface is the elevated deuterium concentration within the volume of the ULK layer. This observation is consistent, given that the first case involves a scenario with 100% liquid water, a condition not applicable to the other samples.

- **Low-k :**

In the case of the sample composed of Low-k material, the results presented in Fig 2.21 are similar to those regarding ULK.

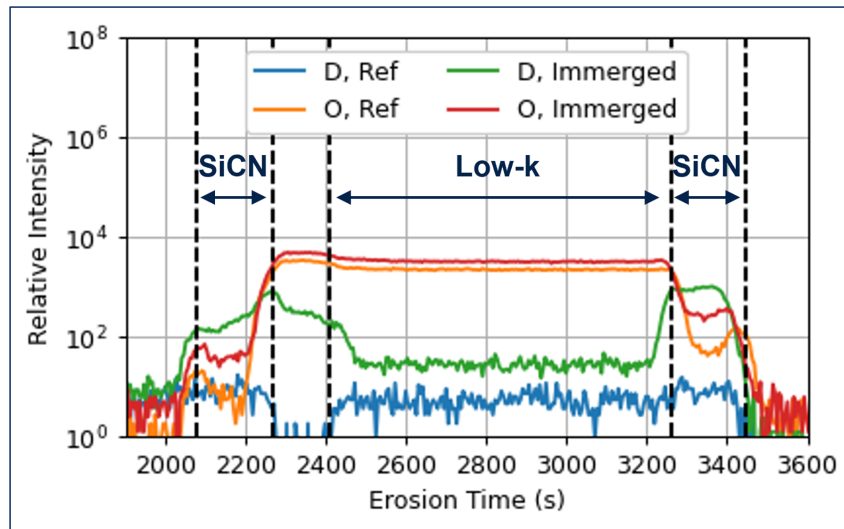


Figure 2.21: ToF SIMS deuterium and oxygen spectra for Low-k samples after moisture exposure

The presence of two deuterium peaks at the SiCN/TEOS and Low-k/SiCN interfaces, indicates the preferential diffusion paths. Deuterium gradients are observed in the SiCN and TEOS layers suggesting that the diffusion is coming from adjacent interfaces. From these interfaces moisture can then diffuse within the bulk materials. The very small quantity of deuterium inside Low-k suggests that moisture diffusion occurs in the SiCN and TEOS layers. Furthermore, Cartailleur's results presented in the introduction show that Low-k bulk is hydrophobic, while SiCN and TEOS are hydrophilic. Therefore, the moisture present at the SiCN/TEOS interface diffuses more easily into the volume of the two layers. In contrast, at the Low-k/SiCN interface, the amount of moisture mainly diffuses into the SiCN layer. These findings suggest that interfaces between dielectrics, particularly those related to SiCN, are preferential diffusion paths for moisture.

- **USG :**

The last result concerns the USG sample. Fig 2.22 shows no variation in deuterium or oxygen before and after 8 hours of exposure. This finding is particularly important when compared to the other two dielectrics. In integrated structures, samples composed of Low-k and ULK exhibit a significant increase in capacitance when exposed to moisture,

while no variation is observed for those composed of USG as presented by Cartailier [11] in Fig 2.23.

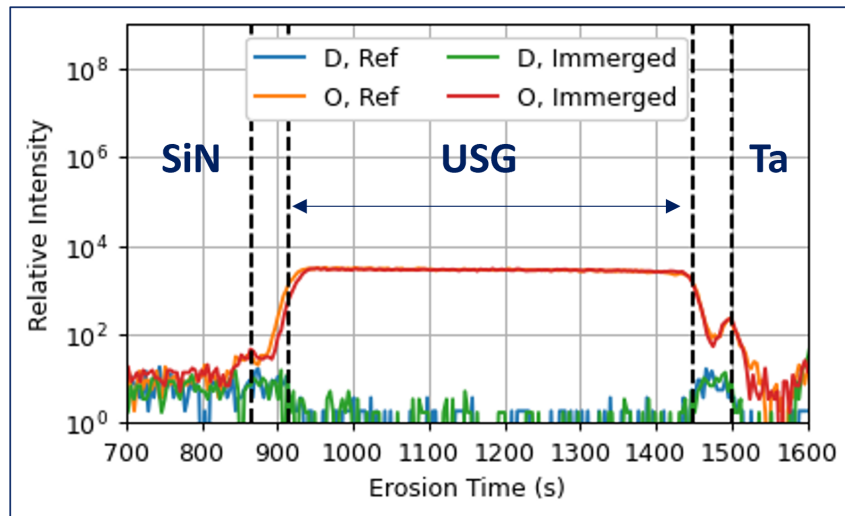


Figure 2.22: ToF SIMS deuterium and oxygen spectra for USG samples after moisture exposure

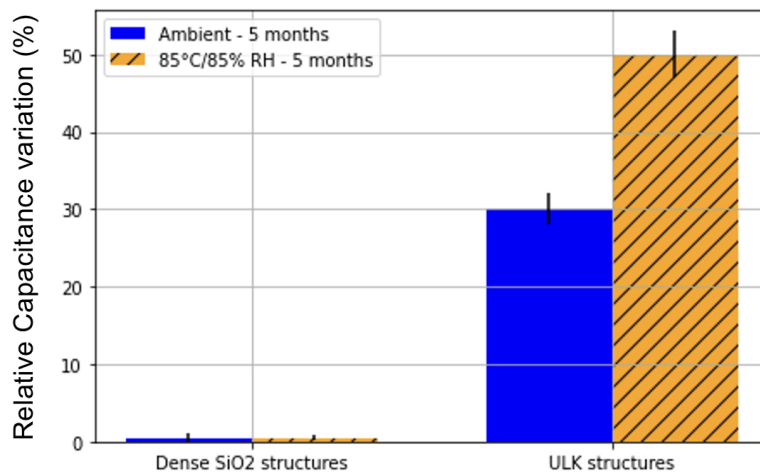


Figure 2.23: Relative capacitance variations after five months at ambient or at 85°C/85% RH for USG and ULK integrated structures [6]

Using the diffusion coefficient presented in the study of bulk materials ( $10^{-15}cm^2/s$ ), it can be roughly estimated that it takes more than 12 years for moisture to reach the sensors. Therefore, it is normal not to see any variation in capacitance for structures composed of USG after 10 hours of exposure since moisture diffusion is limited to the bulk of the dielectric. On the other hand, the significant variation observed for those composed of Low-k and ULK are directly related to the preferential diffusion path between dielectrics interfaces.

The question that arises is why Low-k and ULK interfaces with SiCN have an exacerbated hydrophilic character compared to USG and TEOS. The researchs done by Lépinay [1] and Broussous [26] provide a strong basis to support the observed impact of humidity on interfaces in our work. They highlighted the material degradation and alterations

induced by plasma treatments, particularly focusing on NH<sub>3</sub> plasma, which forms Si-N bonds by consuming methyl groups in the material. This treatment led to the formation of a 5 nm thick hydrophilic SiOCN layer on the surface, as evidenced by ToF-SIMS, Spectroscopic ellipsometry, and RRX measurements (resonant X-ray reflectivity). The destructive nature of etching plasma was underlined through an observed depletion of methyl groups leading to the emergence of silanols, which was analyzed using FTIR and ToF-SIMS. The interaction of plasma with the material was seen to break Si-C bonds, replacing them with Si-OH or Si-H bonds, and the dangling bonds formed interacted with moisture, forming silanol groups. This explains the enhanced hydrophilic feature of dielectric interfaces.

### 2.2.4 Conclusion about interfaces

We first demonstrated the presence of moisture diffusion at all interfaces surrounding copper lines. However, the behavior of interfaces between dielectrics in the presence of moisture remained unclear with the TEM/EDX/EELS analysis due to the initially high oxygen content in Low-k. Therefore we used deuterium as a tracer to identify the moisture path with Tof-SIMS technique. It was found that interfaces between dielectrics (Low-k/SiCN) play a crucial role in the mechanism of moisture diffusion. The simplified diagram in Fig 2.24 shows that the only continuous interface between the 60 microns opening of the seal ring and the sensors corresponds to the interface between the dielectric layers. Furthermore, considering the moisture diffusion coefficients in bulk materials (on the order of  $10^{-15}$  cm<sup>2</sup>.s<sup>-1</sup>), it can be inferred that moisture cannot travel through 60 microns of dielectric in less than several years. Given that the first signs of capacitance variation occur within 50 hours of storage, it can be concluded that, in integrated circuits, this interface serves as the preferential diffusion path for moisture with a diffusion coefficient much faster than that of bulk materials. This result will be further investigated first through numerical simulations and then through electrical characterizations such as the characteristic leakage current of this interface.

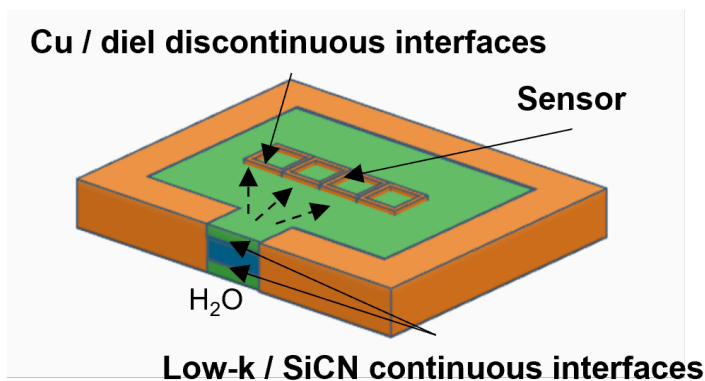


Figure 2.24: Sample schematic with a single sensor (for illustration)

However, despite these findings, the question of why the SiCN USG interface less prone to moisture uptake than those with SiOCH (dense and porous) remains unanswered. One hypothesis is that the carbon present in SiOCH plays a predominant role in the degradation of these interfaces, increasing the number of dangling bonds and thus the hydrophilic character after plasma interaction. Further research is needed to confirm this hypothesis and provide a more comprehensive understanding of the behavior of these interfaces.

Characterizations such as watability measurements and methyl degradation of these interfaces in Lepinay's works [1] would be interesting.

We have been able to collect data and knowledge about material degradations and moisture path in integrated structures. Let focus now on numerical simulations to test the observations about moisture preferential diffusion path.

## 2.3 Numerical simulations of bulk materials

As a reminder, one of the objectives of this work is to link the behavior of the bulk material regarding moisture to that of the integrated structures. To achieve this, numerical simulations are used. In this section, a methodology used to develop a 2D simulation model for moisture diffusion in bulk dielectric materials is presented. Moisture absorption in polymers has been studied through simulation. A similar approach is employed to investigate dielectric materials. The finite element numerical simulations are all performed with Comsol Multi-physics 5.6™.

### 2.3.1 Modeling by thermal analogy

The main problem when it comes to the simulation of multilayer structures is the saturated state of a variable (here moisture concentration). As shown previously, this value differs from one material to another creating a discontinuity at interfaces. To solve this discontinuity, the wetness fraction  $w(t)$  is introduced [27]:

$$w(t) = \frac{C(t)}{C_{sat}} = \frac{M(t)}{M_{sat}} \quad (2.1)$$

$$w(t = 0) = 0 \quad w(t \rightarrow \infty) = 1 \quad (2.2)$$

Where  $C(t)$  represents the moisture concentration at time  $t$  and  $C_{sat}$  is the saturated concentration that depends on temperature and humidity. Time boundary conditions are presented in eq 2.2. A simplified schematic is presented in Fig. 2.25.

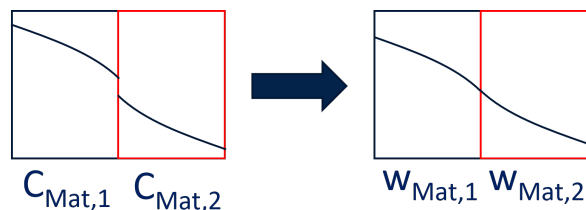


Figure 2.25: Discontinuity of saturated concentration (Left), continuity of wetness (Right)

Due to the similarities between moisture and thermal diffusion, we used the thermal module implemented in Comsol ("Heat Transfer in Solid"). The analogies are presented in Table 2.1 [28].



	Thermal	Moisture
<b>Variable</b>	Temperature	Wetness
<b>Density</b>	$\rho$ (kg/m <sup>3</sup> )	1
<b>Conductivity</b>	k (W/m.°C)	$D * C_{sat}$ (mg/(mm.s))
<b>Specific capacity</b>	$c_p$ (J/(kg.K))	$C_{sat}$ (mg/mm <sup>3</sup> )

Table 2.1: Thermal diffusion analogy

As discussed previously, SiCN layers have a non-Fickian behavior that can be described by the dual stage model suggested by Placette [20]. This model proposes to express moisture concentration  $C$  by two superposed Fickian phenomenon  $C_1$  and  $C_2$ :

$$C(x, y, z, t) = C_1(x, y, z, t) + C_2(x, y, z, t) \quad (2.3)$$

It is possible to apply two separated modules on a given material with Comsol. The modulus "Heat Transfer in Solid" solves the equation successively for  $n = 1$  and  $2$  :

$$\frac{\partial C_n}{\partial t} = D_n \Delta C_n \quad (2.4)$$

The final step is to superpose the results given by these two modules to obtain the full non-Fickian behavior.

### 2.3.2 Bulk Materials results

The purpose of simulating bulk materials is to validate the thermal analogy described above. Additionally, since the diffusion coefficient and saturated concentration obtained from experimental mass uptake are utilized as input parameters, it is crucial to confirm the dual-stage model through simulation.

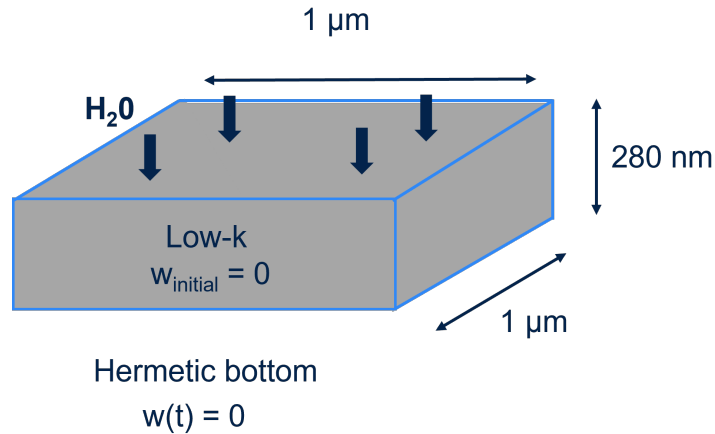


Figure 2.26: Comsol model schematic description

We model the diffusion in a thin dielectric layer deposited on a Si substrate through a cube, as shown in Fig 2.26, with a thickness similar to that of the experimentally deposited layers (280 nm for Low-k and 150 nm for SiCN). The bottom face (in contact with the substrate) is considered impermeable. This is reflected in the model through an isowetness condition ( $w(t)=0$ ) on this face. The thickness of the deposited layer is much smaller than the other dimensions; therefore, moisture diffusion is considered unidirectional through



the layer thickness (semi-infinite plane approximation). Only the upper face is exposed to humidity with an initial condition of  $w_{initial}=0$ . The diffusion coefficient and saturated concentration used in this approach are those presented in Table 2.2.

	Parameters	Low k	SiCN
1 <sup>st</sup> Fick	$D_1$ ( $m^2/s$ )	1.2E-19	8.7E-19
	$C_{sat,1}$ ( $mg/mm^3$ )	28	81.1
2 <sup>nd</sup> Fick	$D_2$ ( $m^2/s$ )		1.0E-22
	$C_{sat,2}$ ( $mg/mm^3$ )		577.0

Table 2.2: Bulk materials extracted properties at 85°C/85%RH [11]

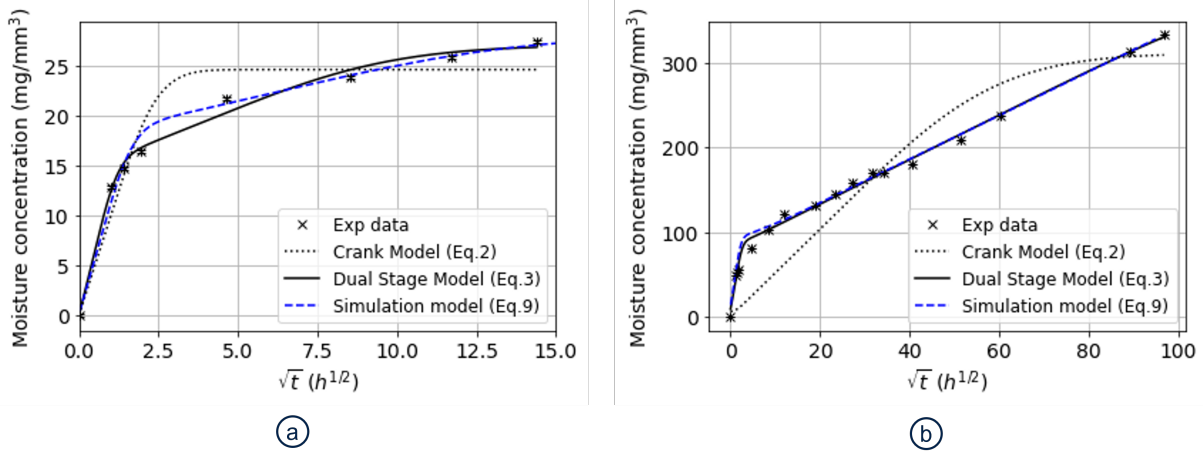


Figure 2.27: Simulation results for (a) Low-k and (b) SiCN dielectrics during a 85°C/85%RH storage

The model results for SiCN presented in Fig 2.27 are in agreement with the experimental data. The same observation is made for low-k. It is also consistent with the analytical approach (dual stage). However, it should be noted that saturation is still not reached after 9300 hours of storage at 85°C/85%RH for the SiCN. Therefore, the simulation is accurate within a certain time range between 0 and 9000 hours, which can be considered sufficient for industrial purposes. This simulation approach will now be applied on integrated material structures.

## 2.4 Numerical simulations of integrated stacks

### 2.4.1 Numerical Model description

Another challenge for integrated stacks modelling is the geometric ratio of dielectric layers. These materials are often deposited at a nanometer scale, while other dimensions are in millimeters. A mesh to build accurate models with reasonable computing times becomes a challenge. To simplify the approach, we considered moisture diffusion only along x-axis in Fig 2.28. This assumption allows moisture diffusion to be described in a

2D cross section plane in front of metals ring opening. The 2D simulation corresponds to the cross section illustrated in the simplified schematic in Fig 2.28. Seal ring blocks moisture diffusion which is represented by the wetness insulation at the end of the model (along x-axis). In addition, wetness insulation is also placed at the top and bottom corresponding respectively to the passivation layer (SiN) and substrate. Impermeability of these layers has been demonstrated by literature [11] [29]. To monitor moisture diffusion in the capacitance structures during FE simulations, an area represented in Fig 2.28 is integrated over time (with the native "intop" function in Comsol). These integrations over time give the total amount of moisture absorbed in the corresponding area. To compare with the capacitance relative variations, all values were normalized between 0 and 1 by dividing by their saturation value. In this first approach, the focus is on the first capacitance sensor. This implies the assumption that the amount of water is proportional to the variation of permittivity.

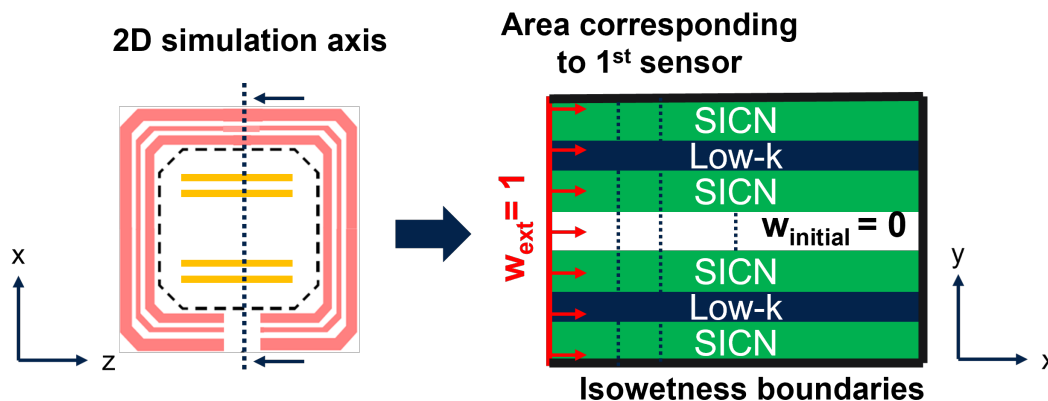


Figure 2.28: 2D simulation axis (left), Model description (right)

### 2.4.2 Experimental data

The results of relative capacitance variations located at 40 microns after up to 4500 hours of accelerated storage at 85°C/85%RH and up to 8000 hours at ambient conditions is presented in Fig 2.29.

A strong increase in capacitance is observed up to 50 hours, with saturation around a 40% variation. Based on the material characterization information obtained, diffusion is preferential at the interface level. Thus, the strong increase in capacitance can be linked to moisture diffusion through the interfaces. In a second stage, diffusion occurs in the bulk materials. The comparison with the capacitance evolution after ambient storage will be presented later (in chapter 3). Here, the objective is to show the experimental data to test the simulation model. For this purpose, two models are developed based on the 85°C/85%RH storage data. The first model considers only the bulk material parameters, while the second model incorporates the interface aspect raised in the first part of this chapter.

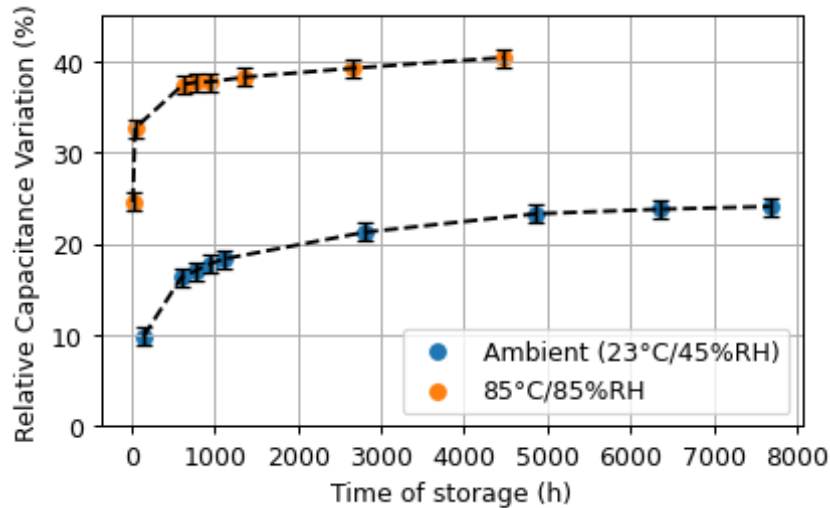


Figure 2.29: Relative capacitance variation during ambient and accelerated storage

### 2.4.3 Numerical results

#### First basic model for integrated materials

In this first model, only intrinsic diffusion parameters of low-k and SiCN (Table 2.2) are considered as input parameters for simulation. The interfacial diffusion is hence not considered. Fig. 2.30 shows that after 200 hours moisture has only diffused over 2 microns.

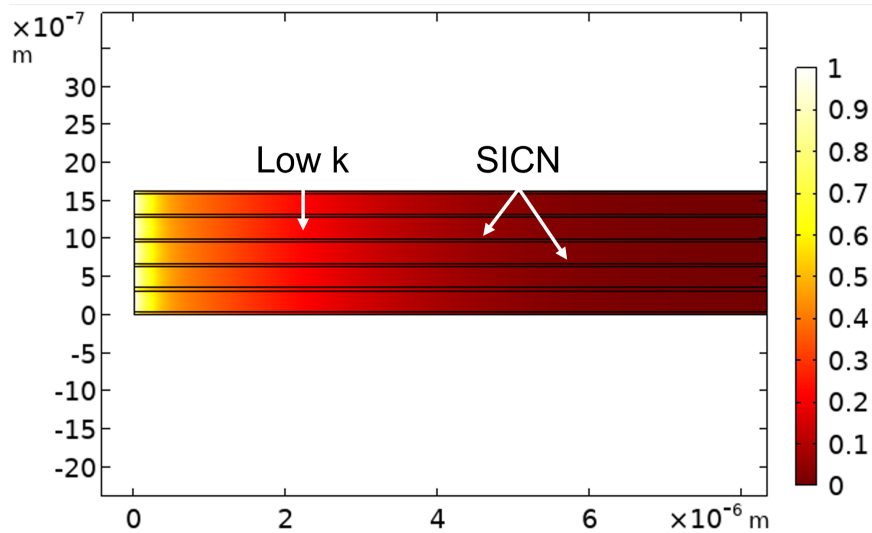


Figure 2.30: Normalized moisture concentration after 200h hours during a 85°C/85%RH storage

This explains why there is no capacitance variation with this model in Fig. 2.32, whereas significant variations are measured experimentally. The bulk material diffusion parameters are not able to describe moisture diffusion behavior in an integrated configuration.

#### Improved model with interface for integrated materials

Since bulk material properties are insufficient to explain the behavior of capacitance sensors, a second model is made by implementing an interface material. For this we have

to make the assumption that the interface is a homogenous material even if Tof SIMS results showed us that in reality interfaces are a gradient of different elements. Moreover, since metals lines are not represented in this simplified simulation approach, we only considered the interfaces between dielectrics materials as presented in Fig. 2.31. It is important to note that each degraded interface has its own moisture diffusion properties. However, for the simulation, we are forced to consider the interface parameter as global parameters for all degraded areas.

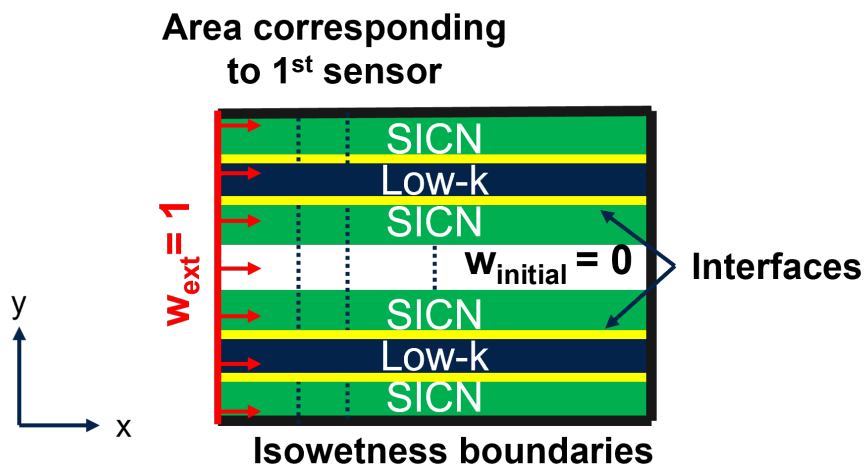


Figure 2.31: Interface implementing in numerical model

The question is what thickness to choose for this interface layer in the model. An approximate thickness of 10 nm is extracted from the Tof-SIMS results obtained with the deuterium experiment described in the previous section (Fig 2.21 in section 2.2.2). Therefore, we implemented a 10 nm thick layer for the interface. The diffusion coefficient of this layer ( $D_{int}$ ) is obtained iteratively until the best fit with the experimental data is obtained. Saturated concentration of interface is also unknown. Since it cannot be measured, this parameter must also be obtained iteratively. Results are presented in Fig 2.32 and extracted parameters for the interface in Table 2.3.

$D_{int}$ ( $m^2/s$ )	$C_{sat,int}$ ( $mg/mm^3$ )
$5.10^{-13}$	8000

Table 2.3: Interface diffusion extracted parameters for a 85°C/85%RH storage

The diffusion coefficient at the interface is much higher than that of the bulk materials (at least 4 orders of magnitude from Table 2.2). These observations and the good agreement between interface model and experimental data suggest that early hours are mainly driven by moisture diffusion at the interface. Regarding  $C_{sat,int}$  it is difficult to evaluate the model results. In fact, SiCN, which is the material that absorbs the greatest amount of moisture, has a  $C_{sat,SiCN}$  18 times smaller than the interface. This observation is not in contradiction with the model approach but it is difficult to explain the result in its physical meaning.

One possible explanation for this phenomenon is that  $C_{sat,int}$  actually corresponds to the moisture concentration considering all interfaces, rather than just a 10nm layer between the dielectrics. To investigate this hypothesis, a more complex approach involving

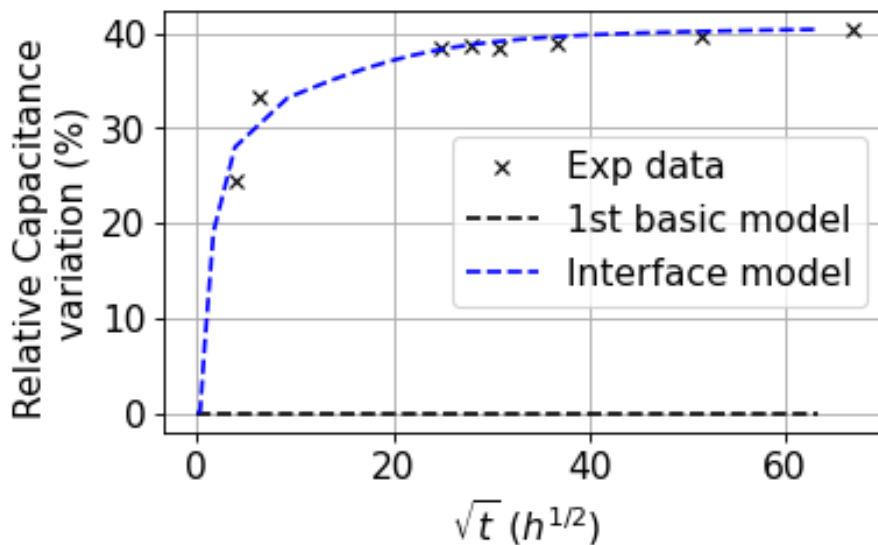


Figure 2.32: Simulations results for moisture diffusion into a stack of dielectrics during a 85°C/85%RH storage

a 3D model needs to be developed. This would allow for a more comprehensive analysis of the moisture diffusion pathways and the role of the different interfaces in the overall moisture behavior.

## 2.5 Conclusion

In this chapter, we have successfully answered the three questions raised in the introduction. Firstly, we have observed oxidation phenomena at the TaN/Ta barrier and SiCN/Copper interface, which are accelerated by storage conditions. These oxidation phenomena are found to be of primary importance in terms of kinetics compared to the increase in water concentration in the dielectrics.

Secondly, we have demonstrated that all interfaces are impacted by moisture diffusion, and it is not possible to determine which interface has the fastest diffusion coefficient or the highest affinity with moisture. However, we have shown that the dielectric interfaces between SiCN TEOS and Low-k (dense and porous) are the preferential paths for moisture diffusion, as they represent the only continuous interface between the seal ring opening and the sensors. This finding is confirmed by simulations, which indicate that there is a difference of about 4 orders of magnitude between bulk and interfacial diffusion.

Finally, we have answered the last question by showing that the moisture diffusion parameters in bulk materials are insufficient to explain the observed moisture behavior in integrated devices.

Since oxidation at the bottom via area is only observed after storage at 85°C/85%RH, resistance measurement should be a good way to access the equivalence between storages. However, the sensor used does not allow us to measure the via resistance. This will be implemented in a further test chip. Moreover, the limit of the simulation is the geometric

ratio because the meshing becomes challenging. By using more sophisticated simulation tools, a 3D model could be achieved and be helpful to understand the geometry influence of the interfaces. In the next chapter, electrical measurement based on leakage conduction results after several storage conditions are presented and linked to the material degradation. Reversibility is also discussed in order to define a failure criteria and be able to build an acceleration model.

## Chapter 3

# Electrical degradation based on leakage current

In our methodology, we observed the degradation of materials, initially focusing on bulk dielectrics and subsequently in an integrated configuration. For bulk materials, we noted that various characterization methods were employed, such as mass measurement, stress analysis, and Fourier Transform Infrared Spectroscopy (FTIR). In an integrated configuration, material characterizations are feasible, as outlined in the previous chapter. However, directly tracking the evolution of dielectric properties is a challenge. This requires the use of electrical measurements, which serve as a means to infer the underlying material properties.

In this context, our focus will primarily be on capacitance measurements, which reflect changes in the dielectric permittivity. Additionally, leakage current measurements will also be conducted. The demonstration of the critical role of interfaces in moisture diffusion was a key finding from the previous chapter. Now, the goal is to explore these degradations through electrical characterization techniques.

## 3.1 Context on leakage current

### 3.1.1 Introduction

The most common interconnect failure mechanisms for SiOCH dielectrics are delamination, electromigration, copper diffusion into dielectrics and dielectric breakdown. In this study, we will focus on moisture influence on dielectric breakdown. This failure mechanism can be assessed by leakage measurements. Indeed, when a voltage is applied, a leakage current appears in the dielectric. When the tension exceeds the threshold value, the dielectric loses the insulating properties since a conduction path (also called percolation path) is formed between the two electrodes. This phenomenon is called dielectric breakdown. The study of conduction mechanisms (i.e. leakage behavior) in dielectrics allows to understand the different physical phenomena occurring in the volume or at the interfaces of the materials and provides important information to predict the reliability of these dielectrics. This chapter delves into the impact of moisture penetration on the electrical integrity of integrated circuits.

Existing literature predominantly addresses moisture ingress during manufacturing

processes rather than post-deposition scenarios. A notable trend observed in these studies, including those by Chen [13], is the diminution of Time Dependent Dielectric Breakdown (TDDB) reliability due to moisture effects. Techniques such as Triangular Voltage Sweep (TVS) and leakage current assessments, as explored in Tokei’s work [14], are crucial for understanding the mechanisms underlying moisture-induced degradation. These investigations reveal two distinct states of moisture interaction: physisorbed, involving weaker hydrogen bonds, and chemisorbed, characterized by a stronger material interaction, as discussed by Proost [10]. Chemisorbed moisture is identified as a primary contributor to the limited reversibility observed in the degradation of dielectric properties, a point emphasized by Y. Li [15].

Further investigation by Mutch [30] into defect structures (traps) responsible for charge transport in dielectrics shows that the conduction mechanism varies with material composition. For dense Low-k materials, dangling carbon bonds play a significant role, whereas in SiCN materials, dangling Si bonds are more influential. Given the high concentration of dangling bonds at interfaces in integrated structures, these sites are prone to increased conductivity, possibly explaining the 2D interface leaks in porous low-k, as observed in Guedj’s research [31]. Understanding the evolution of these conduction mechanisms is crucial for gaining insights into moisture diffusion at interfaces.

### 3.1.2 Methodology

I chose to focus on leakage current and capacitance measurements to gauge the extent of electrical degradation caused by moisture. While other measurement techniques like TDDB, C(V), and leakage current are available, our focus is on understanding how these two specific tests evolve under varied storage conditions (as detailed in Table 3.1).

T°C / RH	45%	60%	85%
23°C	X		
30°C		X	
60°C	X	X	X
85°C		X	X
130°C			X

Table 3.1: Temperature and relative humidity conditions being tested during this work

Storage conditions were chosen to ensure at least 3 tests at constant temperature and at least 3 at constant relative humidity. Standard industry tests, such as the THS (Thermal Humidity Storage) at 85°C/85%RH and HAST (Highly accelerated stress test) at 130°C/85%RH has been used. In addition to these last two storage conditions, another one at 60°C/85%RH was added. However, the HAST test was challenging due to its increased pressure and the lack of midpoint readings during its 96-hour fixed duration. This led to the inclusion of three less aggressive accelerated tests conditions at 30, 60 and 85°C at constant humidity (60%RH). For the extraction of the humidity parameter, three constant-temperature storages were carried out. These are 60°C/45%RH, 60°C/60%RH and 60°C/85%RH. The same procedure is used to monitor these wafers.



The storage duration ranges from 480 hours for the Highly Accelerated Stress Test (HAST), corresponding to five 96-hour cycles, to nearly 25.000 hours (2 years and 10 months) for ambient storage. The other accelerated tests last between 2.500 hours (3 months) and 9.000 hours (1 year). The time limitation generally arises from the availability of the THS (Thermal Humidity Storage) tool and electrical testers.

This approach serves two purposes. Firstly, to develop an accelerated degradation model, which will be the focus of the next chapter. Secondly, to assess the reversibility of moisture-induced damage, which, according to literature, is limited by the chemical bonding between water and the materials. We aim to explore whether there is a common threshold of reversibility, beyond which only partial recovery is observable over all the storages conditions.

Before being able to detect a threshold, we need to acquire a better understanding of how electrical properties behave in the absence of moisture, providing a reference point (dry). To achieve this, we begin by presenting a review of the conduction mechanisms that are likely to be encountered. Following this, we test reference samples to confirm which conduction mechanisms govern the behavior of our samples.

Next, we examine how moisture influences these properties. Initially, we focus on how it alters the conduction mechanism and affects the electrical breakdown of the materials for a saturated sample (worst case scenario). Subsequently, by tracking the evolution of the leakage current as a function of capacitance variation caused by moisture diffusion, I aim to gain a better understanding of the different stages of diffusion (interfaces and bulk). This analysis will allow us to draw connections between the material's behavior and the storage conditions, thereby enabling a more comprehensive understanding of the degradation processes.

The final section of this chapter concerns the reversibility of this moisture-induced degradation. Reversibility is assessed through monitoring capacitance and leakage current during a 250°C bake for 2 months, with data points collected at 24 hours, 2 weeks and 2 months.

### 3.1.3 Leakage conduction mechanism review

The conduction in a dielectric material requires the injection of charges either from the electrodes or from localized states present in the dielectric to the conduction band of the insulator. Figure 3.1a displays the energy barrier at a metal-dielectric interface. Key parameters include the barrier height  $\Phi_B$ , the metal's work function  $\Phi_M$ , the Fermi level  $E_F$ , the vacuum level  $E_0$ , the conduction band minimum  $E_C$ , the valence band maximum  $E_V$ , the bandgap  $E_g$ , and the electron affinity  $X = E_0 - E_C$ .

In part (a) of the figure, there is no electric field applied, and the energy barrier is represented by  $\Phi_B$ . In part (b), the application of an electric field leads to band bending, depicted by the bending of energy levels  $E_C$  and  $E_V$ . This bending reduces the barrier height resulting in increased leakage current through the dielectric.

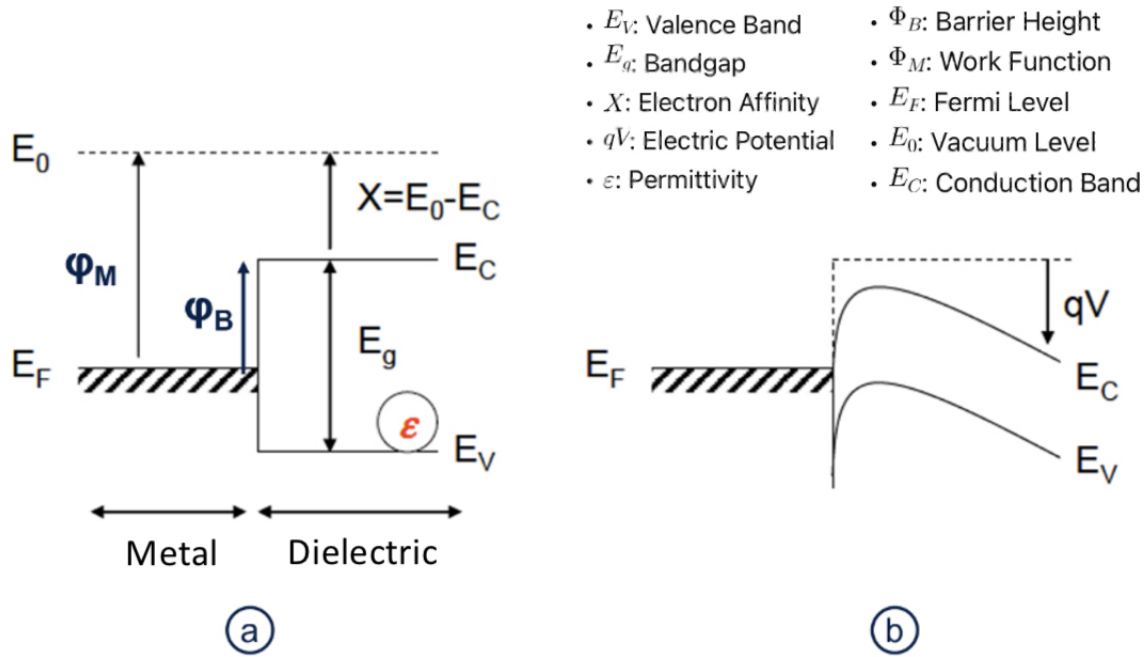


Figure 3.1: Representation of the energy barrier between the metal and the dielectric (a) without and (b) with an electric field (from [7])

There are two categories of conduction mechanisms in dielectrics. Firstly, there are those that depend on the electrical properties at the electrode/dielectric contacts. These conduction mechanisms are called electrode-limited conduction mechanisms or injection-limited conduction mechanisms. On the other hand, there are conduction mechanisms that solely depend on the properties of the dielectric itself. These conduction mechanisms are called bulk-limited conduction mechanisms or transport-limited conduction mechanisms. Figure 3.2 shows a general classification of conduction mechanisms in dielectric films.

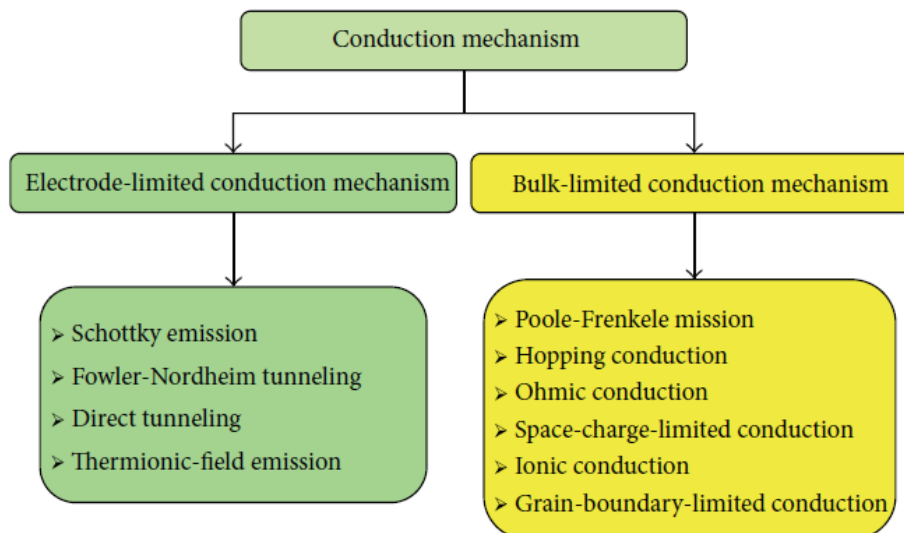


Figure 3.2: Classification of conduction mechanisms in dielectric films [8].

Several studies exist on the predominant conduction mechanism in Low-k and SiCN without moisture. The diversity of results seems to indicate that no consensus has been found on the exact physical origin of the leakage current in these dielectrics. It should be pointed out that the leakage measured in an interconnect structure is the total contribution of leakage through different layers and interfaces that compose the multi-stack structure (IMD bulk, capping layer, interfaces etc.). Thus different conduction mechanisms may occur simultaneously. The goal is to detect the dominant conduction mechanism as well as the dominant leakage pathway. A dependence of the leakage current on the exponential function of the square root of E seems to be observed in most of the configurations similar to ours [7]. The Schottky and Poole-Frenkel mechanisms are therefore investigated for dry samples.

• **Schottky:**

Schottky emission, also known as thermoionic current, occurs when electrons with energy greater than the potential barrier at the metal-dielectric interface pass over the barrier. The application of an electric field can lower the barrier height through the image force, which facilitates electron injection. The image force is a phenomenon that occurs at the interface between a metal and a dielectric material. When a metal electrode is placed at proximity to a dielectric material, the electrons in the metal create an electric field that induces a polarization charge in the dielectric material. This polarization charge creates a mirror image of the metal electrode in the dielectric material, which generates an attractive force between the metal and the dielectric. This attractive force can lower the height of the potential barrier at the metal-dielectric interface, making it easier for electrons to pass through the barrier. The height of the barrier is expressed in eq 3.1:

$$\phi = \phi_B - \beta_{SE}\sqrt{E} \quad (3.1)$$

With  $\beta_{SE}$ , the Schottky constant, which value depends on the dielectric material considered and is expressed by the following equation:

$$\beta_{SE} = \sqrt{\frac{q}{4\pi\epsilon_0\epsilon_r}} \quad (3.2)$$

Those electrons in the metal with sufficient energy can surmount the energy barrier and enter the dielectric. The expression for the current density  $J_{SE}$  as a function of the electric field E in the dielectric and the absolute temperature T can be written as :

$$J_{SE} = A^* \cdot T^2 \exp\left(\frac{-q(\phi_B - \beta_{SE}\sqrt{E})}{kT}\right) \quad (3.3)$$

Where  $A^*$  is the effective Richardson constant, q is the electron charge,  $\epsilon_0$  is the permittivity of free space,  $\epsilon_r$  is the dielectric constant and  $k$  is the Boltzmann constant. At a given temperature, the current varies exponentially with the square root of the applied field. By plotting  $\log(J_{SE}/T^2)$  regarding  $\sqrt{E}$ , the Shottky constant  $\beta_{SE}$  can be extract, hence the permittivity. Additionally, the variation of the y-intercept with temperature allows for the determination of the barrier height.

$$\log\left(\frac{J_{SE}}{T^2}\right) = \log(A^*) - \frac{q\phi_B}{kT} + \frac{q\beta_{SE}\sqrt{E}}{kT} \quad (3.4)$$

• Poole-Frenkel:

The Poole-Frenkel conduction depends on the bulk properties of the material. Indeed, when donor traps (D) are present with a sufficient density in the dielectric volume, conduction is possible by electron emission from donor sites to the conduction band (Fig 3.3).

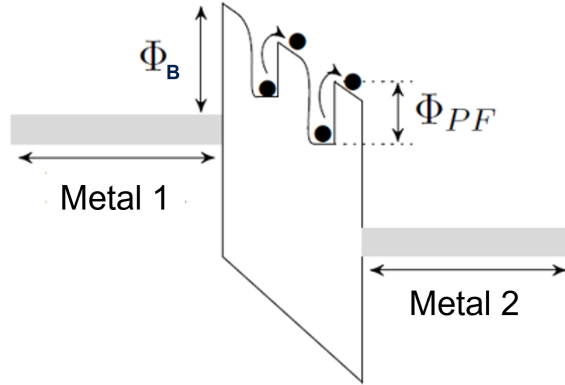


Figure 3.3: Diagram of the conduction band for Poole-Frenkel conduction (extracted from [8])

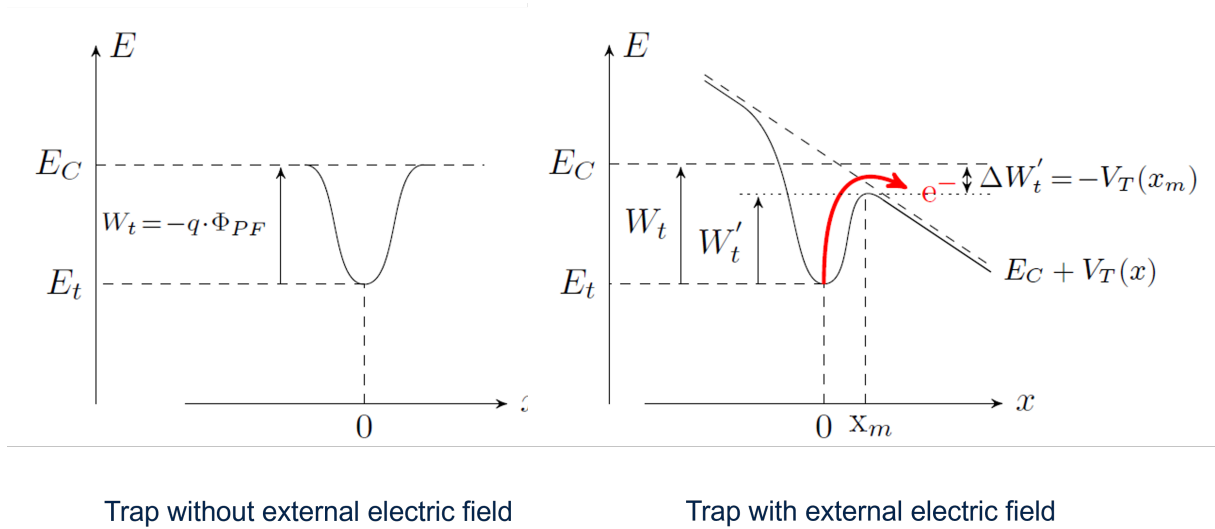


Figure 3.4: Trap state modification with an external electric field. The slope of the dotted line is proportional to the applied voltage (extracted from [8])

Thermoionic emission is effective if the trap is not too deep, i.e.  $\phi_{PF} \leq 1\text{eV}$ . As with the Schottky effect, it is the lowering of the energy barrier through temperature or external electric field that is responsible for moving an electron from the trap to the conduction band (Fig 3.4). This leads to an increase in the concentration of free electrons and therefore in the leakage current defined as :

$$J_{PF} = \sigma_{PF} \cdot E \cdot \exp\left(\frac{q(-\phi_B + \beta_{PF}\sqrt{E})}{2kT}\right) \quad (3.5)$$

Here,  $\sigma_{PF}$  represents the Poole-Frenkel conductivity, which tells us how the effect contributes to the material's overall conductivity.  $\phi_B$  is the barrier height, indicating the energy barrier that electrons need to overcome to move freely. The terms  $q$ ,  $k$ , and  $T$  refer to the electron charge, Boltzmann's constant, and the absolute temperature, respectively.  $\beta_{PF}$  is defined as expressed in eq 3.6 :

$$\beta_{PF} = 2 \cdot \beta_{SE} = \sqrt{\frac{q}{\pi \epsilon_0 \epsilon_r}} \quad (3.6)$$

The first step for Poole Frenkel mechanism identification is plotting the natural logarithm of the current density divided by the electric field, denoted  $\ln(J_{PF}/E)$  as against the square root of the applied electric field (eq 3.7). By applying linear regression to this plot, we can extract some important parameters from the slope (a in eq 3.8) and the y-intercept (Oo in eq 3.9) of the plot.

$$\log\left(\frac{J_{PF}}{E}\right) = \log(\sigma_{PF}) - \frac{q\phi_B}{2kT} + \frac{q\beta_{PF}\sqrt{E}}{2kT} \quad (3.7)$$

$$\text{slope} = \frac{q\beta_{PF}}{2kT} \quad (3.8)$$

$$\text{Oo} = \ln(\sigma_{PF}) - \frac{q\phi_b}{2kT} \quad (3.9)$$

While this method is useful for identifying the presence of the Poole-Frenkel effect, it does not allow us to independently determine the values of  $\phi_B$  and  $\beta_{PF}$ . To achieve this, we need to introduce another variable: temperature. By performing the same measurements at different temperatures, we can isolate the trap depth ( $\phi_B$ ) and  $\beta_{PF}$ , and distinguish whether the primary conduction mechanism is driven by Schottky or Poole-Frenkel effects.

### 3.1.4 Dry samples results

The purpose of this section is to gain a better understanding of the conduction mechanisms in our Low-k/SiCN integrated structures before focusing on the influence of moisture. As previously described, in order to determine the limiting conduction mechanism, it is essential to conduct temperature-dependent measurements.

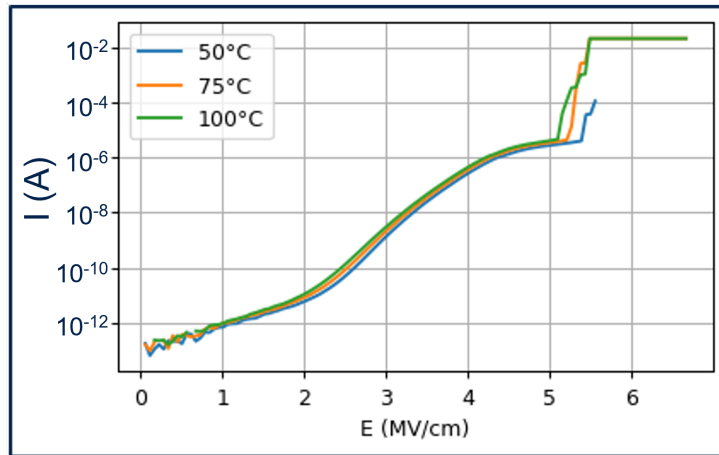


Figure 3.5: Leakage current measurements at different temperatures for dry samples

For this purpose, we performed measurements on reference samples (dry) at 50, 75, and 100°C. The results are presented in Fig. 3.5. As described in the previous section, by doing the linear regression between  $\ln(J/E)$  and the square root of  $E$ , we can extract the slope for each temperature.  $J$  is obtained by dividing the leakage  $I$  with the sensor surface. By plotting an Arrhenius graph with the extracted slopes, we obtain the beta parameter and  $\epsilon_r$  (Fig 3.6a and Table 3.2).

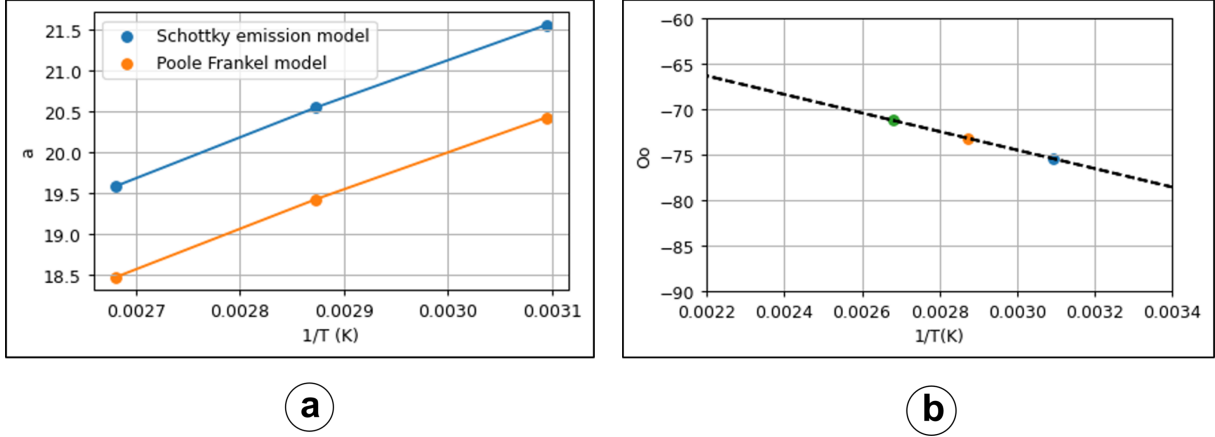


Figure 3.6: Trap state modification with an external electric field. The slope of the dotted line is proportional to the applied voltage

Parameters	$\epsilon_r$	$\phi_B$ (eV)
Schottky	$< 1$	0.7
Poole-Frenkel	3.5	0.8

Table 3.2: Leakage conduction extracted parameters for mechanism identification

Finally, by plotting the y-intercept regarding  $1/T$  (eq 3.9) on Fig 3.6b, we obtain a trap depth of 0.8 eV. The Schottky model is also tested, and the results are presented in Table 3.2. However, the permittivity extracted with Schottky model is less than 1, which is inconsistent. Therefore, we conclude that the Poole-Frenkel mechanism is the dominant conduction mechanism in our Low-k/SiCN integrated structures. These results are consistent with previous studies in the literature [7] [32], where they obtained a permittivity of 3.6 and a trap depth of 0.7 eV on structures similar to ours in terms of materials.

Other models have been proposed in the literature, such as the compensation Poole-Frenkel model, which is an extension of the original Poole-Frenkel model. The main difference between the two models is that the compensation Poole-Frenkel model takes into account the compensation of charge carriers from donor traps by acceptor (or neutral) traps. Due to the complexity of these models, we consider the Poole-Frenkel model as a first approximation of the dominant conduction mechanism in our test structures. However, it is important to note that more complex models may be necessary to fully understand the behavior of our structures in the presence of moisture. Nevertheless, this presents an exciting opportunity for future research to explore the role of water as a donor or acceptor in our integrated structures.

### 3.1.5 Charge trapping phenomena

An interesting phenomenon that is potentially exploitable in the Poole-Frenkel conduction mechanism is charge trapping, which is highlighted by successive leakage current measurements. Figure 3.7 shows a decrease in leakage current between the first measurement (without breakdown) and the second. Unlike CVD grown SiO<sub>2</sub>, PECVD deposited dielectrics have higher bulk defect density due to imperfections in atomic bonding and plasma degradation. During the first measurement, these defects act as charge trap centers [7] [33]. Electrons and holes get trapped in these defects. Then, during the second leakage measurement, these electrons are trapped and do not participate in the leakage current anymore. This result will be helpful in interpreting further results on how moisture interacts with the dielectrics.

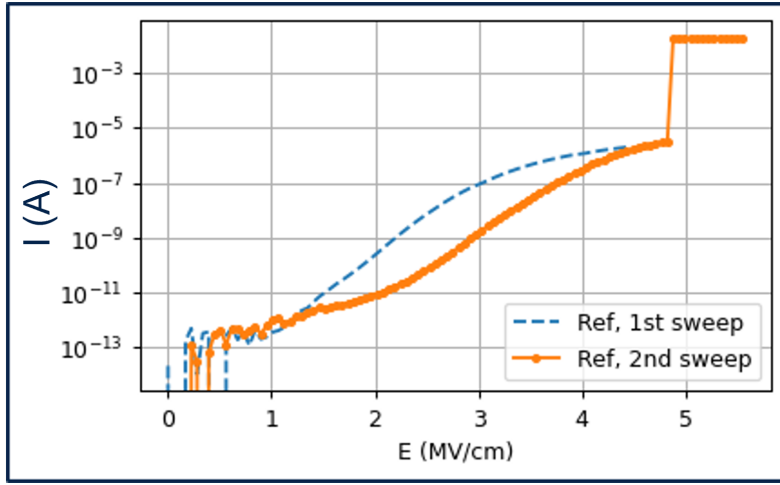


Figure 3.7: Successive leakage current measurements on reference samples

From the voltage difference it is possible to obtain the total trapped charged and then the trap density thanks to equation 3.10 and 3.11 :

$$\Delta V = -\frac{e_{ox} \cdot Q_{ox}}{2\epsilon_0\epsilon_r} \quad (3.10)$$

$$Q_{ox} = \int_0^{e_{ox}} -q \cdot n_{ox}(x) dx \quad (3.11)$$

Where  $e_{ox}$  is the dielectric thickness (90 nm),  $Q_{ox}$  is the total trapped charge ( $C.m^{-2}$ ), and  $n_{ox}$  is the trap density ( $trap.m^{-3}$ ). However, this calculation assumes that the charge density is homogeneous, which has its limitations since we are dealing with an integrated structure with a high concentration of defects at the interface between low-k and the capping layer SiCN. Nonetheless, we obtain a trap density on the order of  $3.10^{23} trap.m^{-3}$ . This value is consistent with previous studies by [7], who used the same methodology ( $n_{ox} = 9.10^{22} trap.m^{-3}$ ), as well as by [34], who used a photocurrent spectroscopy method ( $n_{ox} = 6.10^{22} trap.m^{-3}$ ). Since this phenomenon is characteristic of the conduction mechanism, it is interesting to observe the impact of moisture on the trapping and de-trapping effect.

## 3.2 Moisture saturated samples

### 3.2.1 Conduction mechanism modification

In this sections, samples studied are moisture saturated. The saturation is supported by capacitance variation data on structures without seal ring protection (Fig 3.8) at ambient conditions .

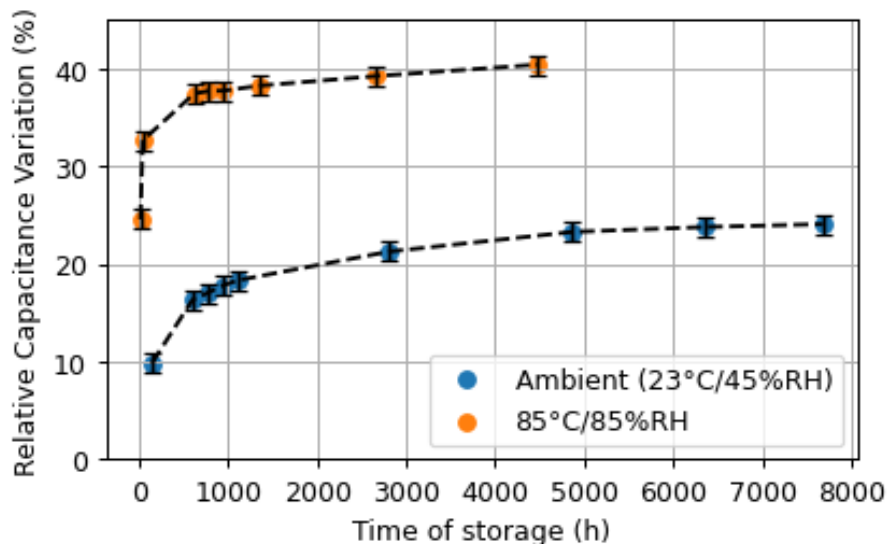


Figure 3.8: Relative Capacitance variation during ambient and 85°C/85%RH storages

To illustrate the results for the leakage measurement on these same samples, an example with 27% increase in relative capacitance is chosen (3.9). A 30 % decrease in  $E_{bd}$  (electric breakdown) is observed as well as a strong leakage current increase until 3 MV/cm. Comparing it to the reference (dry) samples, the field dependency is linear instead of the  $E^{1/2}$  Poole Frenkel model. Indeed, in Fig 3.9, a linear regression over a wide range of  $E$  is showing an  $R^2$  value of 0.99. Thus, the conduction mechanism is modified.

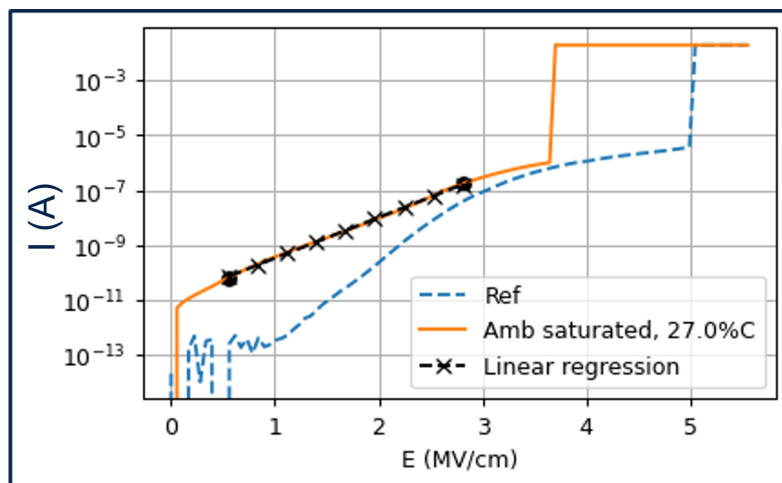


Figure 3.9: Leakage current behaviour for ambient saturated sample (23°C/45%RH)



In the literature, there is a lack of information regarding linear dependence conduction mechanisms. "A Review on Conduction Mechanisms in Dielectric Films" [8] presents a description of leakage current with a linear dependence on  $\exp(E)$  in the presence of ionic species (Equation 3.12).  $J_0$  is a proportional constant,  $q\phi_B$  is the potential barrier height,  $E$  is the applied electric field,  $d$  is the spacing of two nearby jumping sites.

$$J = J_0 \exp \left[ - \left( \frac{q\phi_B}{kT} - \frac{Eqd}{2kT} \right) \right] \quad (3.12)$$

The extraction of the slope results in a value of  $d \approx 1.7$  nm, surpassing the intermolecular distance of water molecules in their liquid form (0.3 nm). However, a complicating factor is that all extracted parameters are temperature-dependent. Therefore, conducting temperature-based measurements is crucial for accurately testing this ionic conduction model.

However, temperature measurements are challenging due to the fact that increased temperatures may also enhance the desorption of moisture. Thereby interfering with electrical measurements. A potential solution could involve assessing the model across a low to very low temperature range (e.g., 5 to 25°C), aiming to minimize the desorption's impact. This approach would necessitate a comprehensive study in its own right. Nonetheless, our observations may indicate that the conduction mechanism in saturated samples is influenced by moisturized agglomeration sites spaced by an average distance  $d$ , as discussed in the works of Chang [35] and Sodolski [36]. They describe a similar mechanism involving ionic transport between different humidity clusters in respectively POSG and porous silica xerogel. Furthermore, in [14], the authors present a study on Time-Dependent Dielectric Breakdown (TDDB) measurements coupled with Triangular Voltage Sweeps (TVS) tests on damascene structures with low-k dielectrics. The TVS technique is a well-known method for detecting the presence of ionic species. It allows for the detection of both copper and moisture. The researchers found that plasma treatment can lead to the elimination of hydrophobic groups, resulting in catalyzing moisture absorption through the formation of silanols (hydrophilic groups). The results of the TVS analysis clearly indicate the presence of ionic species  $H^+$  for samples that are not even exposed to moisture (after deposition). These results support our ionic conduction hypothesis, which is enhanced by the high amount of moisture in our saturated samples.

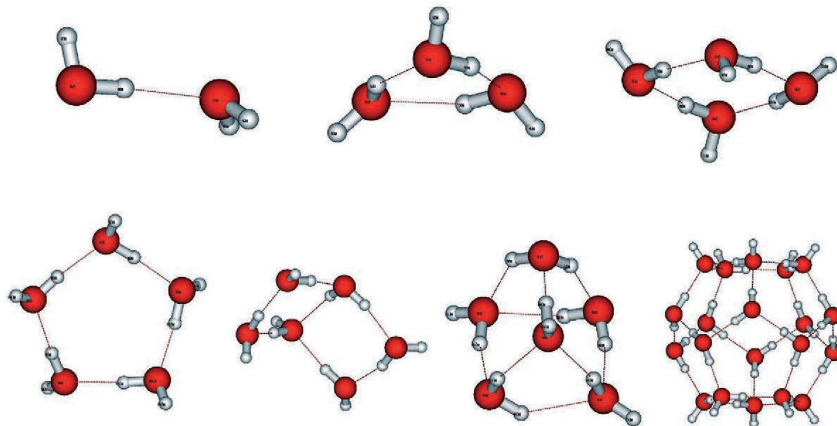


Figure 3.10: Some water aggregates expected in the vapor phase (extracted from [9]).

This argument also aligns with the description of water behavior in the vapor phase as presented in Millot’s book [9]. When a water molecule forms a hydrogen bond with a neighboring molecule, the electron cloud undergoes a reorganization that promotes the formation of a new hydrogen bond. This process leads to the formation of aggregates with various structures, including cyclic structures formed by adjacent cycles or irregular or regular cages, such as the triangular prism for  $(H_2O)_6$ , the cube for  $(H_2O)_8$ , or the dodecahedron for  $(H_2O)_{20}$ . The formation of these aggregates and the charge transfer they induce likely contribute to the modification of the leakage current behavior observed in saturated samples.

### 3.2.2 Bake results for moisture saturated samples

First step for the study of the recovery of saturated samples at ambient condition ( $23^\circ\text{C}/45\%RH$ ) is to look at dry samples (without moisture exposure) behavior after the drying process at  $250^\circ\text{C}$ . Figure 3.11 presents an example of the leakage current curves (18 samples out of 72 tested) before and after.

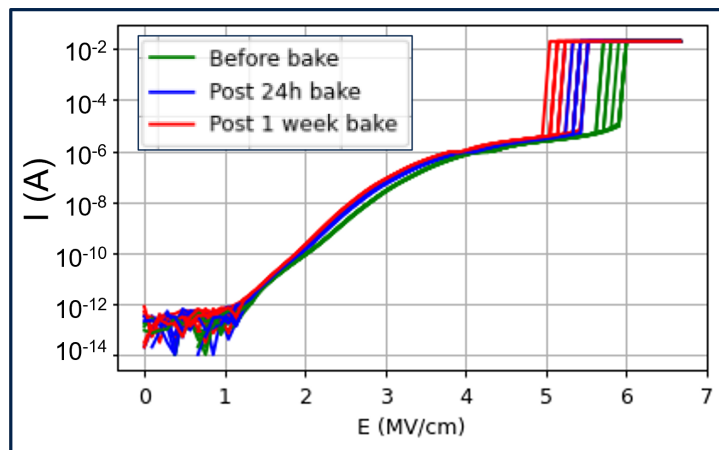


Figure 3.11: Example of leakage current curves for reference samples before and after bake at  $250^\circ\text{C}$

It can be seen that the breakdown field is clearly impacted by the drying temperature and duration. Among all the factors that can impact  $E_{bd}$ , we find, in particular, the distances between copper armatures of the capacitance sensors due to process variability. It is possible to observe a variation in dimensions due to copper expansion and the different CTEs of each dielectric. However, it is not possible to be quantitative about this observation due to the high variability of the breakdown field, even for reference samples before drying (7 - 10 %). Therefore, it is necessary to keep in mind that the breakdown field cannot be considered as a reliable criterion and focus more on the leakage current variations.

Regarding the relative capacitance variation, a slight decrease is observed after 250 hours of drying at 250 degrees. This suggests that moisture may already be present in the structures initially. It has been demonstrated that Chemical Mechanical Planarization (CMP) and cleaning steps are particularly critical due to direct exposure to liquid water [26]. However, annealing steps are routinely performed, desorbing some of the moisture weakly bonded to the materials. Conversely, our reference structures are sealed, preventing the potential desorption of initially present moisture. Therefore, the reduction in

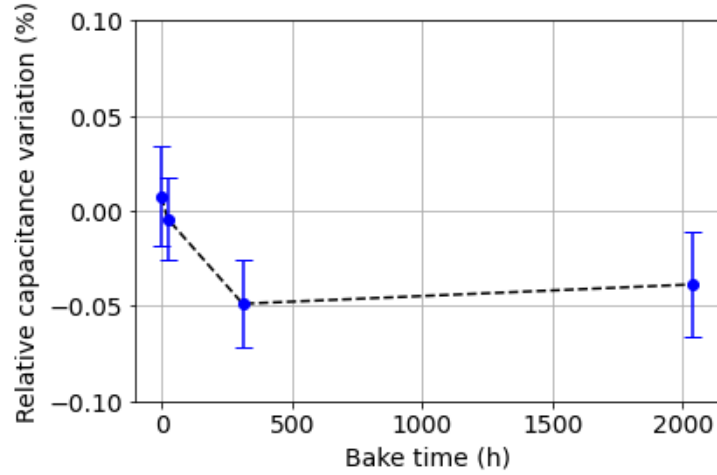


Figure 3.12: Relative capacitance variation for reference samples (without moisture) before and after bake at 250°C

relative capacitance variation over storage time cannot be attributed to the desorption of initially present moisture. The most plausible explanation for this variation could also be due to the dimensional changes in copper lines caused by temperature fluctuations. In fact, capacity is directly linked to the spacing between two copper lines, which can vary with copper thermal expansion.

Furthermore, according to the specifications of the capacitance meter, the measurement accuracy is 0.05% of relative capacitance shift. This is confirmed by Fig 3.12 that displays the relative capacitance during the bake for a dry sample. At  $t = 0$  hours, the standard deviation is indeed lower than the tester's accuracy, centered around 0. After drying, the standard deviation remains consistent with previous measurements, despite a slight decrease. This implies to reconsider the moisture detection threshold from 0.05% to 0.1% in terms of relative capacitance variation after drying.

Water	$E_a$ (eV)	Assignment
$\alpha$	$0.23 \pm 0.02$	Physisorbed water
$\beta$	$0.55 \pm 0.17$	Tightly hydrogen-bonded water
$\gamma_1$	$0.89 \pm 0.01$	Hydrogen-bonded silanols
$\gamma_2$	$2.02 \pm 0.18$	Isolated silanols

Table 3.3: Literature data about water bonds for silicon based dielectrics [10]

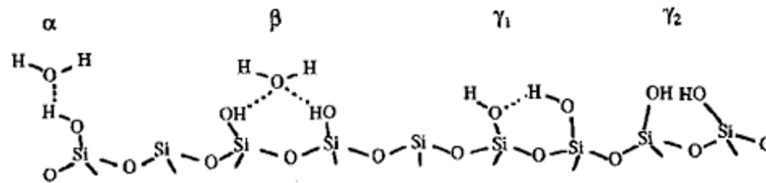


Figure 3.13: Schematic of water bonds for silicon based dielectrics [10]

Now we try to link these results to chemical consideration in the literature. For this, we focus on recovery of ambient saturated samples (at  $\approx 24\%$  capacitance shift). According

to TDS (thermal desorption spectroscopy) spectra in the literature [10] [15], moisture links to the dielectrics through different kinds of bonds, usually called  $\alpha$ ,  $\beta$ ,  $\gamma_1$ ,  $\gamma_2$  (Table 3.3). Fig 3.13 represents the different interactions between water and silicon based dielectrics. These results are similar through a large class of silicon dielectrics ( $\text{SiO}_2$ , SOG, Low-k). Their results show that moisture weakly bonded through weak hydrogen interactions are desorbed at lower temperatures than  $100^\circ\text{C}$ . Then, for temperatures between between 200 and  $350^\circ\text{C}$ , the  $\beta$  bonds starts to break. Therefore, the  $250^\circ\text{C}$  baking process should break and desorb all the  $\alpha$  bonds and starts to break the  $\beta$  ones. To confirm this, we follow capacitance recovery after drying. Fig 3.14 presents the results of capacitance variation decrease due to moisture desorption at  $250^\circ\text{C}$ .

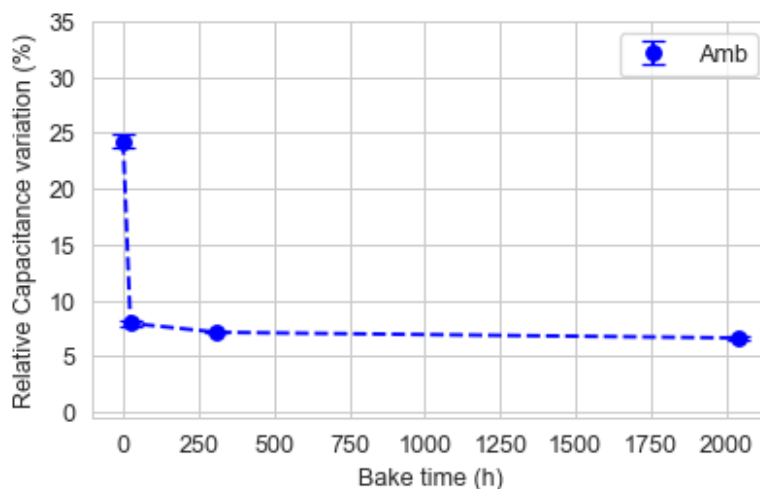


Figure 3.14: Relative capacitance variation for an ambient saturated samples during the  $250^\circ\text{C}$  bake

The 15 % decrease (in average) in capacitance variation after 24 hours of dry can be attributed to the  $\alpha$  bonds. Then, an additional 2 % reduction is observed, reaching a total decrease of 17 %. These can be assigned to the weakest  $\beta$  bonds that begin to desorb. It is interesting to note that half of the capacitance variation at saturation is related to the  $\alpha$  weak bonds. The other half is associated with deeper modifications in the materials that cannot be restored without affecting the thermal stability of the dielectrics. Therefore, in terms of capacitance, moisture degradation is partially reversible for saturated samples.

Regarding the leakage current measurements after bake, the results are shown in Fig 3.15. After 2 months of drying, the leakage current does not return to its initial behavior. The partial reversibility observed for the capacitance is confirmed with the leakage current behavior after drying. Moreover, the conduction mechanism is strongly impacted by the desorption. The leakage current dependence returns to a square root dependence of the applied field after bake. This results allow to assign the ionic conduction mechanism to the combination of free moisture (and weakly bonded,  $\alpha$ ) with strongly bonded moisture. This support the idea of conduction based on free moisture between moisture cluster that are formed near defects and polar areas. Indeed, when free moisture is desorbed after drying, only the clusters of strongly bonded moisture remain. In other words, there are no longer enough mobile charge carriers to ensure conduction. In this scenario, the Poole-Frenkel conduction mechanism becomes the limiting factor again. The leakage current lowering after bake indicates that a part of the defects that used to ensure the conduction

into the dielectric are now occupied by strongly bonded moisture and do not participate to the leakage current anymore. This phenomenon is similar to charge trapping as described previously and highlights the oxidation of the dielectrics.

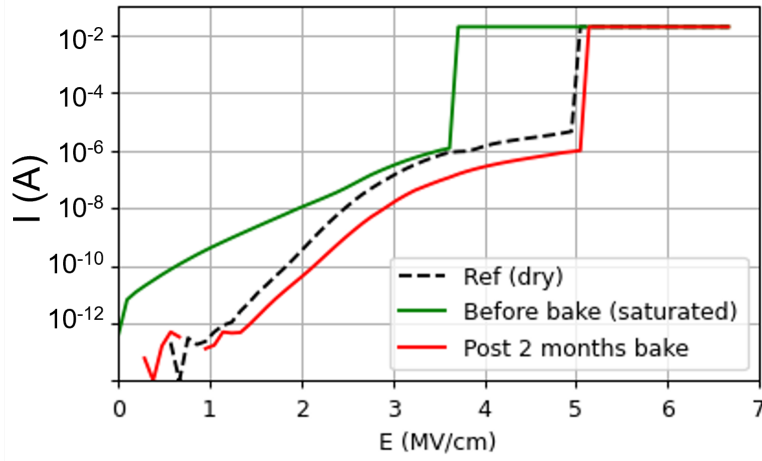


Figure 3.15: Example of leakage current curve before and after bake for saturated samples at ambient conditions

### 3.2.3 Comparison between leakage current after saturation for several storage conditions

Now that we have seen the behavior of the leakage current for a sample saturated at ambient conditions, we may look at different storage conditions. The objective is to highlight potential differences. Similarly to the ambient saturated samples, the state of saturation is considered regarding the evolution of the relative capacitance variation. Figure 3.16 shows this result for 6 different storage conditions.

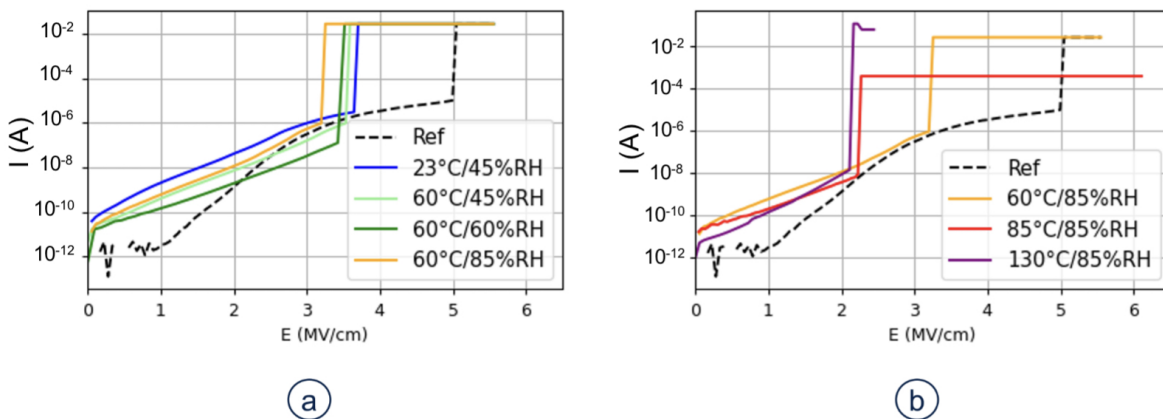


Figure 3.16: Leakage current curves for saturated samples for different storage conditions

In Figure 3.16a, the leakage current curve after ambient storage (for reminder) and three conditions with fixed temperature and varying the relative humidity parameter (60°C/45%RH, 60°C/60%RH, 60°C/85%RH) are presented. Then in (b), two others conditions are presented in order to fix the relative humidity parameter and look at temperature influence (60°C, 85°C at 85%RH). The first observation we can make is that the

modification of the conduction mechanism due to moisture is present for all conditions.

By applying equation 3.12, we can extract the parameter  $d$  for the different conditions. As a reminder, this parameter represents the distance between two jumping sites. We obtain values very close to that obtained for the sample stored at ambient conditions (1.7 nm) (Fig 3.17), with variations of 0.1 nm and a maximum standard deviation of 0.4 nm. Therefore, it is difficult to draw conclusions about the evolution of this parameter given the small variations and the precision of the measurement.

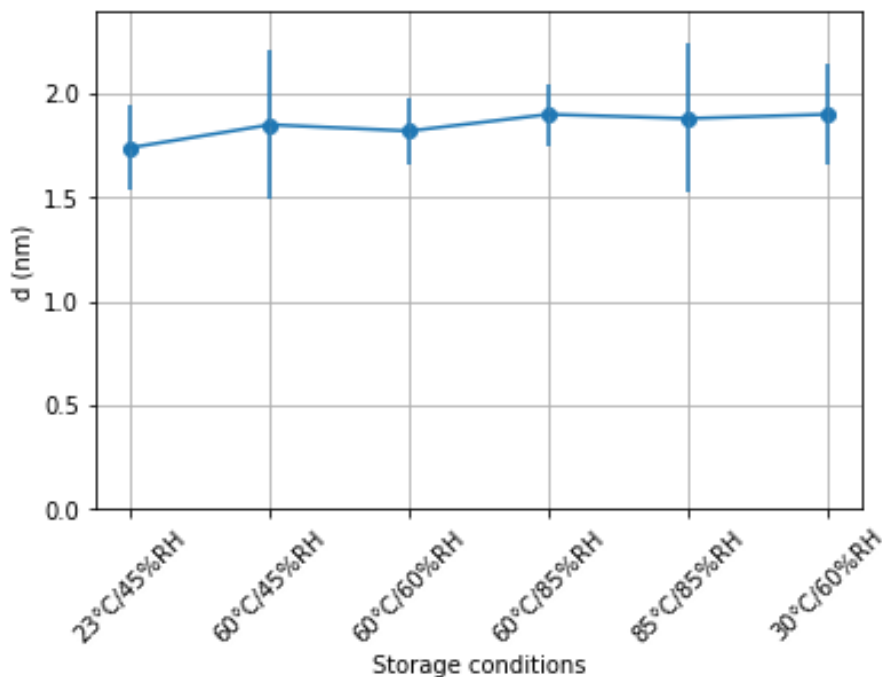


Figure 3.17: Distance between two jumping sites ( $d$ ) extracted from experimental data at various conditions

Regarding the breakdown field, much more pronounced variations are observed. The breakdown field for a reference sample is around  $5 \text{ MV.cm}^{-1}$ . For all storage conditions with a temperature below  $85^\circ\text{C}$ , we observe a decrease of about 30% in the breakdown field (approximately  $3.5 \text{ MV.cm}^{-1}$ ). For those with a temperature above  $85^\circ\text{C}$ , we observe a decrease of 60% in the breakdown field (approximately  $2.2 \text{ MV.cm}^{-1}$ ). This observation raises the question of the equivalence of degradation caused by humidity for different storage conditions. In Chapter 1, we saw that the thickness of oxide layers (at copper or Ta interfaces) is greater for storage at  $85^\circ\text{C}/85\%RH$  than at ambient conditions. Additionally, copper diffusion in the dielectric can be observed only for the  $85^\circ\text{C}/85\%RH$  storage.

It can be concluded with certainty that in the saturated state, material and electrical degradation are not completely equivalent. This result is very important, especially in the industrial context, as the acceleration factor is often assumed from empirical studies without necessarily verifying the equivalence of degradation. This will be a crucial question in the next chapter on the development of an acceleration model.



### 3.2.4 Recovery after saturation for different storage conditions

The last part of the comparison between different storage conditions concerns the reversibility of electrical degradation in terms of capacity variation and leakage current. We follow the same methodology as in the previous section, which means that we perform drying at 250°C for 2 months with read points at 24 hours, 2 weeks, and 2 months. This represents a vast amount of data, not all of which can be presented here. Figure 3.18 shows the results of drying for samples saturated at three different storage conditions in addition to ambient conditions. Like with the drying results from the previous section (on samples saturated at ambient conditions), we observe a decrease of more than half in the capacity variation for each storage condition. Indeed, we go from 28-31% saturation for storage at 85°C/85%RH before drying to 11-12% after drying. These results suggest that the degradation caused by humidity in terms of capacity variation is only partially reversible for all storage conditions.

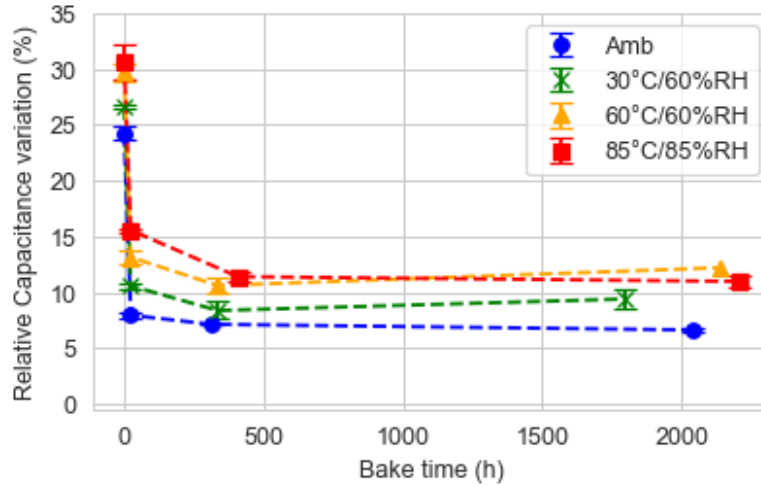


Figure 3.18: Relative capacitance variation evolution during a 250°C bake for saturated samples at different storage conditions

It should be noted that for the storage conditions 30°C/60%RH and 60°C/60%RH, a slight increase is observed between the measurements at 2 weeks (300 - 400 hours of drying) and the final measurement. This may be due to problems with the tester during measurement, which lengthens the time between taking the wafers out of the oven and the electrical test. Usually, there is a 20 minute delay between the two stages, to allow the plate to stabilize thermally after leaving the oven. For these two storage conditions, the delay was around 1.5 hours allowing re-absorption of moisture.

Regarding the reversibility, Figure 3.19 shows the leakage current curves obtained after approximately 2 months of drying for two additional storage conditions in addition to ambient conditions (30°C/60%RH and 85°C/85%RH). As with the samples stored at ambient conditions, we observe partial reversibility of the leakage current for these new storage conditions. Indeed, after drying, we find the characteristic dependence on  $\sqrt{E}$  of the Poole Frenkel mechanism for all storage conditions. However, we observe that the more aggressive the storage conditions, the lower the leakage current after drying compared to the dry reference sample. For example, for a field of  $3 \text{ MV.cm}^{-1}$ , we have a leakage current of about  $10^{-8} \text{ A}$  for the sample stored at ambient conditions, while we

are almost at  $10^{-10} A$  for the sample stored at  $85^{\circ}C/85\%RH$ . This can be explained by the following consideration: for aggressive storage conditions, the quantity of chemically bounded moisture (not desorbable at  $250^{\circ}C$ ) will increase. As we have seen in the previous section on samples stored at ambient conditions, the lowering of the leakage current indicates that some of the defects that used to ensure conduction into the dielectric are now occupied by strongly bonded moisture and do not participate in the leakage current anymore. A greater amount of bound moisture therefore implies a lower leakage current. The presence of moisture plays the role of a trapping effect like two successive leakage current as previously described. In this situation, the trapping is localized at interfaces.

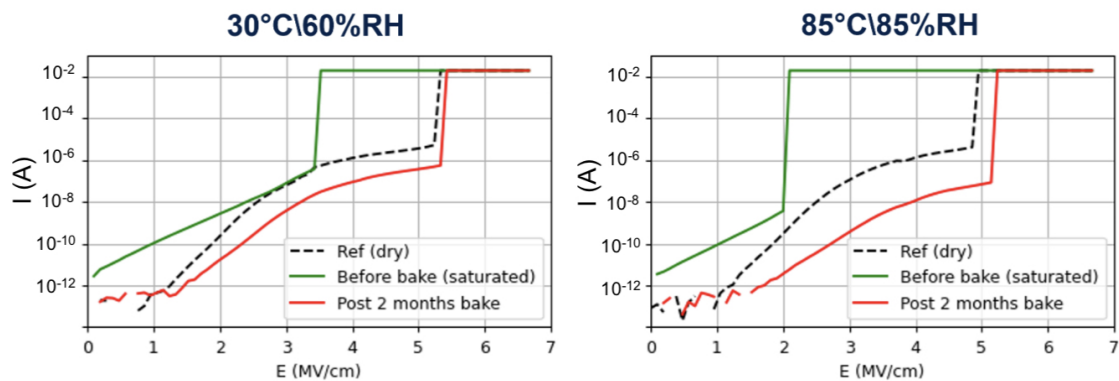


Figure 3.19: Effect of a  $250^{\circ}C$  bake and post bake behavior observed on leakage curves for 2 storages conditions

Finally, the last but perhaps most important observation regarding the reversibility of the leakage current concerns the  $85^{\circ}C/85\%RH$  storage condition. In the first chapter, we observed signs of copper diffusion in the low-k dielectric for one of the samples analyzed by TEM/EDX. However, we had doubts about the repeatability because only 1 over the 4 samples analyzed presented copper diffusion traces. In his study, Cartailier [37] was able to demonstrate much more pronounced traces of copper diffusion, but in the Ultra-Low-k (ULK) dielectric.

The signature of this copper diffusion is a non-reversibility of the leakage current and the breakdown field, as presented in Figure 3.20. The results obtained on Low-k structures differ from those obtained on ULK. We observe complete reversibility of breakdown field, and a partial reversibility for leakage current in Fig 3.19. Therefore, we strongly suspect that copper diffusion in low-k structures is not a degradation mechanism that occurs as frequently as in ULK structures. As already mentioned, only one of the four samples analyzed showed traces of copper diffusion. This suggests that the Tantalum layer maintains its copper barrier properties even after oxidation.

It can be concluded that the electrical variation of capacitance and leakage current in a moisture-saturated sample are partially reversible regardless of storage conditions. The partial reversibility is likely due to the fact that a portion of the moisture is intrinsically bound to the materials (dielectrics and metals). As mentioned in the previous chapter, the formation of copper and tantalum oxides are irreversible phenomena that can also influence the partial irreversibility. Additionally, material degradation can be grouped into two categories: diffusion at the interfaces and into the bulk. In the case of the moisture-saturated sample, it can only be said that the observed electrical degrada-



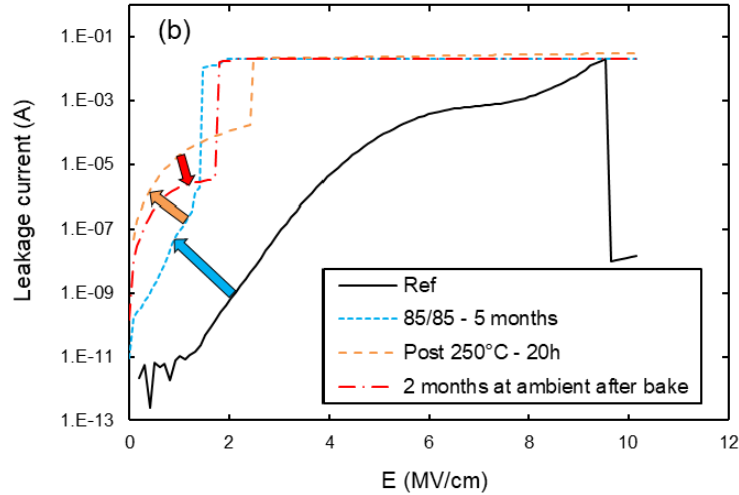


Figure 3.20: Effect of a 250°C bake and post bake behavior observed on leakage current curves for ULK samples [11]

tion is related to the overall material degradation. However, we have seen that interfaces are the preferential diffusion paths compared to bulk. Therefore, it is interesting to see if it is possible to distinguish the electrical degradation related to interfaces and to the bulk.

To do so, the evolution of leakage current with moisture content is examined to relate it to material degradation. Of course, it is not possible to accurately evaluate the moisture content, so the evolution of leakage current is categorized for different capacitance variation values. Furthermore, drying is used to determine if there is a degradation threshold below which a full recovery would occur.

## 3.3 Partially moist samples

### 3.3.1 Evolution of the leakage current

Now that we have seen the impact of moisture on the conduction mechanism in a state close to saturation, let's examine what happens for small capacitance variations, i.e., when moisture is mainly present at the interfaces. The main challenge for this is that measurements need to be made at very short storage times due to the significant increase in capacitance variation during the first few hours. In previous section I have shown that sensor was positioned 40  $\mu\text{m}$  away from the 60  $\mu\text{m}$  seal ring opening. Fig. 3.8 (section 3.2.1) shows that very short time would be needed to access lower relative capacitance variation (below 10 % of capacitance shift) regardless of storage conditions. Therefore, to access such low values, we introduced a tunnel consisting of two continuous metallic walls in front of the 60  $\mu\text{m}$  opening, as illustrated in Fig 3.21. This tunnel forces moisture to travel a distance of several millimeters before penetrating into the die, delaying moisture arrival on the capacitance sensor.

An example of relative capacitance variation of the sensor during an accelerated test at 60°C/60%RH is presented in Fig 3.22 for a tunnel length of 4 mm. The time scale

is presented in square root since the simulation results presented confirmed that a combination of Fickian diffusion mechanisms can be used to match experimental data. The delay of moisture impact on the capacitance sensor is clearly observed. After 400 hours of storage, the capacitance shift has just reached the detection threshold of 0.05 % instead of 40 % for the previous structure (no tunnel).

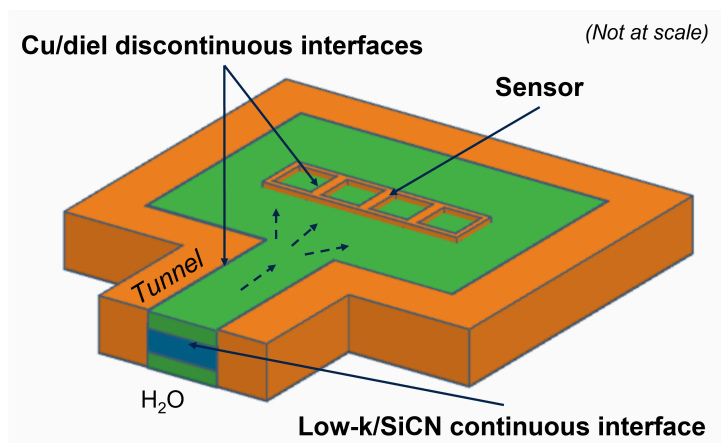


Figure 3.21: Sample schematic with tunnel configuration

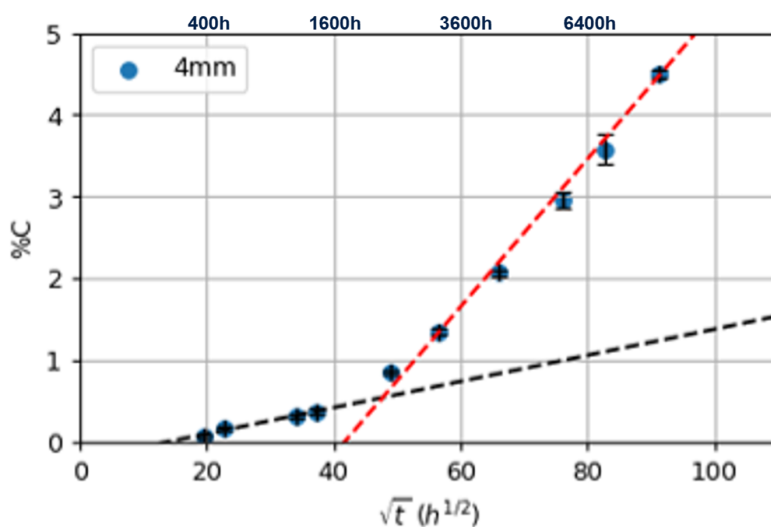


Figure 3.22: Relative Capacitance variation evolution during storage at 60°C/60%RH

Thanks to this design, we have been able to access leakage curves for low capacitance variations. Some selected results are presented in Fig. 3.23. The results are regrouped by behavior into four categories detailed below: samples with capacitance variations below 1.5 %, ranging between 2 and 5%, exceeding 5 %, saturated.

- For samples with capacitance variations below 1.5 % ;

A reduction in leakage current without a decrease in breakdown field is observed. Based on previous results, this behavior is attributed to the diffusion of moisture at the Low-k/SiCN interfaces.

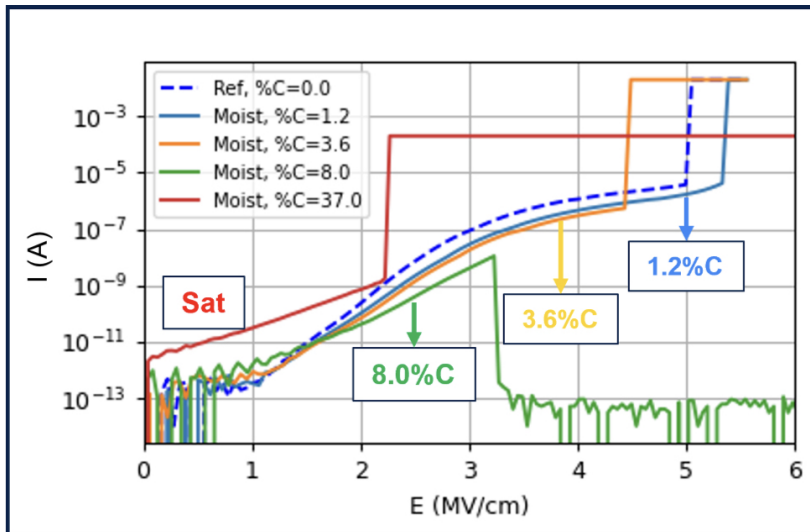


Figure 3.23: Representative of leakage current measurements for samples with different relative capacitance variations at 85°C/85%RH

Similar to the charge trapping phenomenon described previously, moisture fills the defects in this region (dangling bonds), leading to a decrease in leakage current. However, it should be noted that the signature of charge trapping is a decrease in leakage current with a (homogeneous) shift in voltage, whereas here, an increase in this shift with voltage is observed. In other words, it appears that there is more of a distortion of the leakage current curve than a shift.

In the literature, this phenomenon is explained by a non-homogeneous distribution of defects and charge carriers for an MIS system (Metal-SiO<sub>2</sub>-Si) (Fig 3.24) [12].

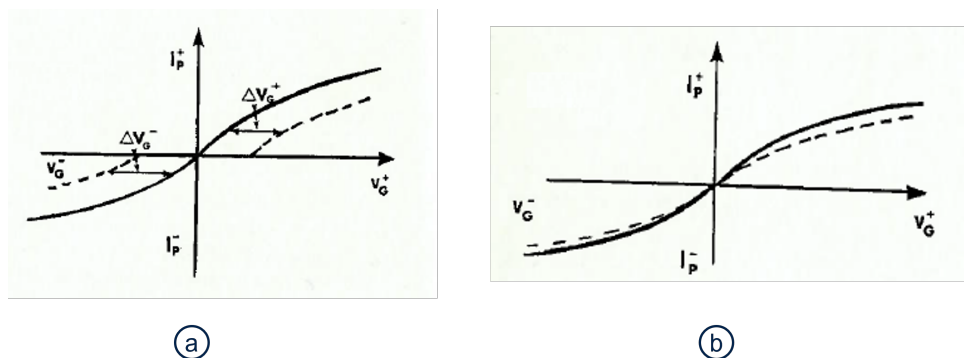


Figure 3.24: Leakage curves for (a) an homogeneous charge distribution through the bulk of the dielectric and (b) non homogeneous charge distribution [12]

Unfortunately, in this case, it is not possible to determine the quantity of charges as described by equation 3.11. Yet, this observation supports our results about the preferential diffusion at the Low-k/SiCN interface. As we have seen, moisture behaves both as charge carriers (free water) and as traps (bound water), and a high concentration of moisture in this region implies an increase in the inhomogeneity of the charge distribution in the system, resulting in a distortion of the leakage current curve.

- For relative capacitance variations ranging from 2 to 5 % ;

In addition to a decrease in leakage current, a significant decrease in electric breakdown is now observed. At this stage continuous interfaces are moist. We suppose that the vertical copper/TaN/Ta/low-k interfaces are the next preferential path for moisture diffusion. We suspect that the increase of permittivity in these interfaces could increase the effective field inside the test structure. To highlight the impact of humidity in this region on the electric field, a simple simulation is conducted using the electrostatic module of Comsol.

For this purpose, the geometry derived from the TEM cross-sections presented in the previous chapter is used (Fig 3.25). A voltage of 45 V is applied, as it is close to the experimental breakdown voltage. In a preliminary static approach, the presence of moisture is simulated by varying the permittivity at the interfaces of Copper/TaN/Ta/Low-k. The permittivity is set to 70 near the copper interface (to represent the worst-case scenario of moisture permittivity) and decreases linearly over 10 nm into the bulk of the dielectric (where  $\epsilon_r = 2.9$ ). This value is derived from TEM EELS analysis of these interfaces in the first chapter. Additionally, a reference model without moisture is created, in which the permittivity of the interfaces is simply equal to that of the bulk material (2.9).

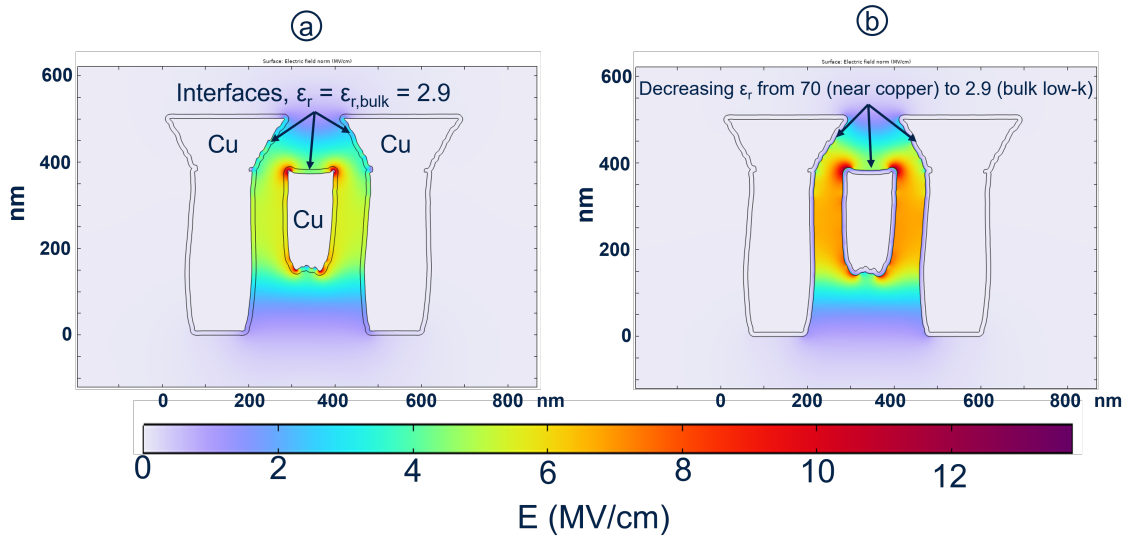


Figure 3.25: Numerical simulation representing the electric field across the sample in (a) a dry configuration (homogeneous  $\epsilon_r = 2.9$ ) and variable permittivity for the moist sample

In the dry numerical model (a), the average field is approximately  $5 MV.cm^{-1}$ , whereas in the moist model (b), it reaches about  $7 MV.cm^{-1}$ . This indicates that the effective field is higher for the same applied voltage in the presence of moisture, suggesting a lower breakdown voltage. The geometry of the copper lines also creates zones with a higher electric field amplitude. These zones are primarily located at the Low-k/SiCN interfaces, considered the preferential breakdown path whether the samples are moist or dry. However, it's important to note that the absolute values of these results should not be taken at face value, only the observed increase in electric field magnitude due to moisture impact on lateral interfaces is significant. The linear decrease chosen for the simulation is arbitrary, given the lack of precise real values and understanding of the permittivity variation near the vertical copper interfaces.

- For variations exceeding 5 % ;

A transient regime is entered where the Poole-Frenkel mechanism no longer appears to be valid. In addition, a slight increase in leakage current at low fields is observed. This behavior at low fields is intensified for the saturated sample. Unfortunately, leakage current measurements for capacitance criteria above 8 % and below saturation ( $\approx 24$  %) were not possible because of logistical aspects of the experiment. During this phase, moisture diffuses into the bulk of the dielectrics.

- Finally, saturated samples ;

We have already seen that the conduction mechanism is modified with a linear dependence between the logarithm of the leakage current and the applied field.

Now that we've characterized the different capacitance shift regimes by linking them to leakage current curve shapes, the focus now is on the the recovery of the initial properties. The recovery of the conduction mechanism, breakdown field and capacitance value will be evaluated.

### 3.3.2 Recovery of partially moist samples

In this section, we conducted experiments using samples with varying tunnel lengths and distances between the seal ring opening and the sensors, ranging from 4 mm to 20 mm. The purpose of these experiments was to investigate the effect of drying on the capacitance and leakage current of the samples.

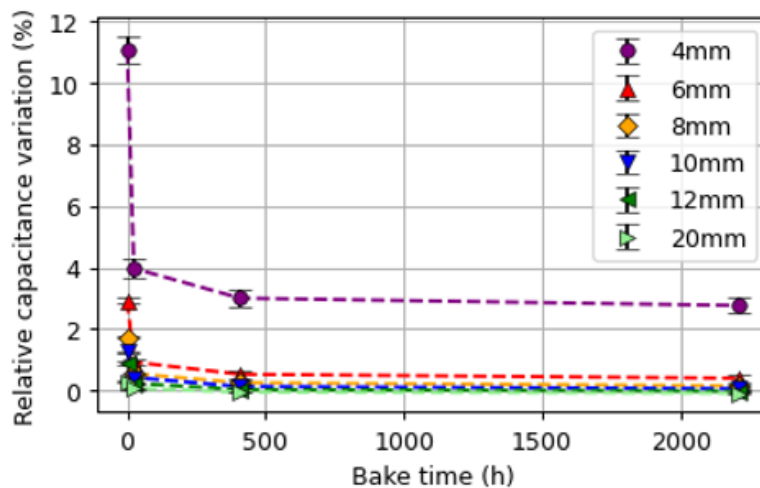


Figure 3.26: Relative capacitance shift for different tunnel length structures during the 250°C bake

To do this, we monitored the capacitance value of the samples for durations ranging from 24 hours to approximately 3 months of drying at 250°C. We found that the residual capacity variation after 3 months of drying depended on the variation before drying. For instance, the 4mm sample kept 3% variation in capacity after 3 months of drying compared to the initial 11%. This indicates partial reversibility in terms of capacity variation.

We also measured the leakage current of the samples after 3 months ( $\approx 2100$  hours) of drying (Fig. 3.27). The result shows that the effect of residual moisture on the leakage current was similar to that observed in initially saturated samples.

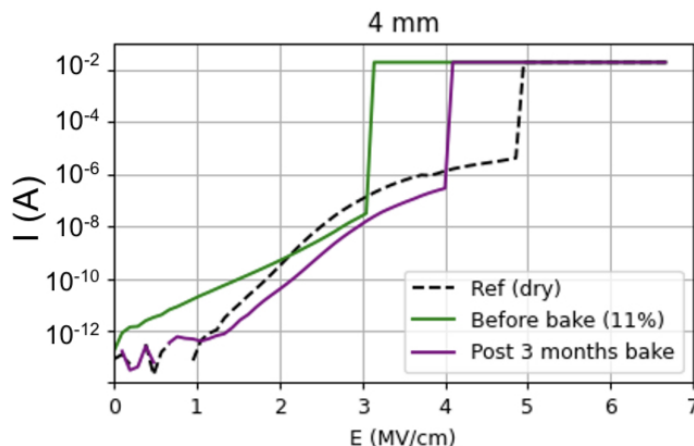


Figure 3.27: Example of leakage current curves before and after the 250°C bake for the 4 mm sample

The desorption of weakly bonded ( $\alpha$ ) and free moisture is linked to the strong decrease in leakage current at low fields. The stronger bonds seems to remain, making a full recovery impossible after 3 months of drying at 250°C. This result can be explained by the charge trapping phenomenon, where trapping centers such as concentrated dangling bonds at interfaces that previously contributed to leakage current for the reference sample no longer exert such influence due to their interactions with moisture. In other words, residual moisture acts as a charge trap, resulting in a decrease in leakage current. The same behavior is observed for the 6mm structure. The average samples have a capacitance variation of 3% before drying and 0.7% residual capacity after drying. In terms of leakage, a partial recovery is also confirmed.

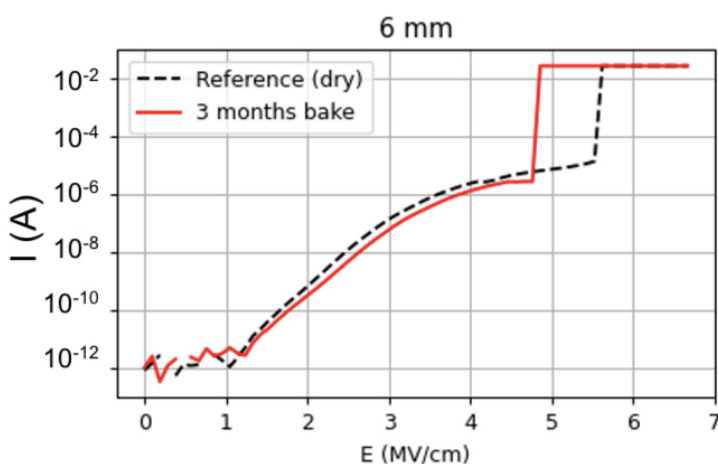


Figure 3.28: Example of leakage current curves before and after the 250°C bake for the 6 mm sample

We then look at the reversibility of capacity and leakage current for the 8 mm and 10 mm structures. It was challenging to draw systematic conclusions regarding the total

reversibility of these structures. After drying, residual capacitance variations were below  $0.2\% \pm 0.1\%$  (Fig. 3.26), which is very close to the threshold detection limit for reference samples after drying, which is about  $0.1\%$  in relative capacitance shift. This argument alone is insufficient to assert whether we have achieved full recovery or not.

In terms of leakage current, for the 8 mm structure, 8 out of 10 samples showed total reversibility (Fig 3.29). This suggests that there may be a threshold value of capacitance shift before which samples can fully recover their initial electrical properties. Furthermore, for structures ranging from 10 mm to 20 mm, the variation in capacitance before drying was less than  $1\%$ , and we observed full recovery in all samples (similar behavior than Fig 3.29 for 8 mm). These results indicate that the samples have successfully recovered from moisture-induced degradation. Therefore, beyond the threshold of  $1\%$  of capacitance shift, baking at  $250^\circ\text{C}$  is insufficient to fully recover from moisture degradation after saturation at ambient storage.

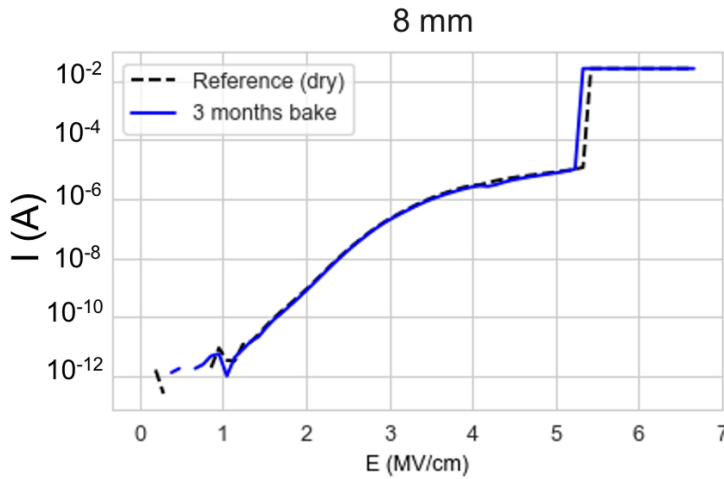


Figure 3.29: Example of leakage curves before and after the  $250^\circ\text{C}$  bake for the 8 mm sample

To confirm full recovery in this range of capacitance variation ( $< 1\%$ ), it would have been interesting to compare the leakage current with the product operating voltage. Unfortunately, this was not possible because the leakage current generated when applying a field below  $1 \text{ MV/cm}$  was too low to be detected. An additional experiment that would be interesting to perform is a TEM/EDX/EELS characterization on samples with capacitance variations below  $1\%$ . As described in the previous chapter, the partially moist sample on which these characterizations were performed had a capacitance variation of  $5\%$  after storage at  $85^\circ\text{C}/85\% \text{RH}$ . We had already observed the beginning of the copper line oxidation and the TaN/Ta barrier. Moisture-induced oxidation of the tantalum barrier and copper can have significant effects on via resistance measurement and electromigration. These effects can be particularly pronounced in high-current-density regions such as vias and interconnects, where electromigration is a common issue. Therefore, a test chip is currently being processed with integrated sensors that will allow to study the via resistance variation due to humidity. These measurements could be a valuable asset for linking moisture degradation, resistance, capacitance variation, and leakage behavior.



## 3.4 Conclusion

After observing the degradation caused by moisture penetration into integrated dielectrics using material characterization methods, this chapter investigated the associated electrical degradation. To achieve this, the evolution of capacitance and leakage current was monitored using sensors. The results show variations in capacitance on the order of 30 to 40% at saturation levels, depending on storage conditions. Furthermore, a complete modification of leakage current behavior at saturation state was observed. We have proposed a hypothesis concerning an ionic conduction mechanism between moisture clusters. The evolution of this change in the conduction mechanism was also studied. The different changes in leakage current during exposure to humidity were grouped into 4 categories of capacitance variations. The results obtained from the material characterizations in the first chapter provided a better interpretation of these findings.

The last part of this chapter focused on the reversibility of moisture degradation. By monitoring the recovery of capacitance and leakage current degradation during drying at 250°C, a reversibility threshold was defined. Samples with capacitance variations before drying of less than  $\approx 1\%$  recover their initial performance. This was confirmed across a wide range of accelerated storage conditions. This aspect is crucial for the following chapter, as it aims to define a moisture-related failure criterion for the development of an acceleration model. Since there is no defined failure criterion in the literature applicable to this study context, we propose to use this reversibility criterion.

An interesting aspect highlighted by our study is the presence of moisture in different states. Firstly, with the concept of moisture clusters, which raises the question of whether water is in a condensed state (liquid water) in these areas. The presence of liquid water could promote the ionic behavior of the conduction mechanism. Another question regarding the state of water is the presence of both liquid and bound water in different materials. Drying results showed partial reversibility attributed to the presence of bound water ( $\beta$ ,  $\gamma_1$ ,  $\gamma_2$  bonds) and chemically bounded water in the different observed oxide layers (Cu, Ta). These bonds have a desorption temperature above 250°C. It was observed that the modification of the conduction mechanism occurs only when both unbound (weakly) and bound moisture are present. If unbound moisture is desorbed, the Poole Frenkel conduction mechanism is restored.

The hypothesis that we have formulated is that moisture likely plays two roles. First, it acts as a trap, as evidenced by the decrease in leakage current observed during the initial exposure of the samples (a phenomenon similar to charge trapping). Second, moisture also acts as a mobile charge, leading to an increase in leakage current initially at low fields for capacitance variations greater than 5%. This is followed by a general increase when the samples become saturated.

In terms of perspectives, these results could be interesting for simulation. The Langmuir model [38], developed by Irving Langmuir in 1918, is a theoretical model used to describe the adsorption of molecules onto solid surfaces. This model is particularly useful for understanding how gases adhere to solid surfaces in a single layer (monolayer adsorption). However, it falls short when multiple layers are involved. The BET model [39], named after Stephen Brunauer, Paul Hugh Emmett, and Edward Teller, addresses this



limitation by allowing for the adsorption of molecules in multiple layers. In the BET model, the surface is divided into lattice sites where molecules from the gas phase can adsorb. Unlike the Langmuir model, molecules can adsorb on top of each other, creating multiple layers. The model considers various parameters like the total number of sites ( $M$ ) and introduces terms like  $\theta_1$ ,  $\theta_2$ ,  $\theta_3$ , etc., to represent the fraction of the surface covered by one, two, three, or more layers of molecules. The BET model also incorporates kinetics to describe the adsorption and desorption of molecules. It involves calculating the equilibrium conditions for various layers and solving the rate equations for adsorption and desorption.

Other models that have been developed to improve upon the BET model to include the heterogeneity of the adsorption sites in a microporous material. However, these simulations are advanced and require a real understanding of the methods and software involved. Finally, there are many avenues for improving and complementing this work by adding new characterization methods.

Among these, direct measurement of dielectric permittivity by mercury drop could be mentioned. Unfortunately, this method was not available. It would have been interesting to perform frequent measurement tracking of permittivity at different humidity exposure times. This way, the different states of water could potentially be identified. Unbound water is much more mobile than bound water. It will be capable of following higher frequencies during measurements. A cutoff in the permittivity value is expected at a frequency representing the fact that bound molecules are less mobile. These measurements could also provide data (intended for simulation) regarding the influence of plasma treatment on the surface of dielectrics. Since the interface between Low-k and SiCN is the preferred diffusion path, it would be interesting to seek optimization strategies.

# Acceleration Model for moisture diffusion

In this chapter, the objective is to develop an acceleration model under diverse aging conditions for industrial applications. Initially, the chosen model will be presented, followed by a comprehensive description of the methodology employed to execute this research. The core focus of this chapter will be on the extraction of representative parameters integral to the model. Emphasis will be placed on identifying the technological parameters pertinent to our study, with the aim of defining the most accurate and applicable acceleration factors. The model's limitations will be also highlighted.

## 4.1 Introduction

### 4.1.1 Context

An industrial application of the findings from previous chapters is the development of a model for accelerating moisture diffusion in dielectric stacks. The acceleration factor is a concept employed in environmental testing to simulate the effects of long-term exposure to aggressive environmental conditions within a shortened timeframe. This factor represents the ratio of the duration required for a product to fail under normal operating conditions to the time it takes for the same product to fail under accelerated conditions.

As discussed in the first chapter, JEDEC standards exist concerning acceleration factors mostly determined for polymers encapsulation. In this work, the focus is not on encapsulation polymers but rather on materials in metallic interconnections (BEOL). We have previously seen that simulation is a good tool for describing moisture diffusion in integrated stacks. However, these simulations require a complete understanding of the diffusion parameters of each component within the stack. They also demand significant computational power due to the dimensions involved, which makes meshing a challenge. Therefore, it is necessary to develop a simpler method to assess the moisture diffusion in a given stack using an analytical model.

Historically, D.S. Peck published a paper in 1986 reviewing about sixty publications since the 1970s dealing with accelerated tests under humid heat conditions [40]. He focused on aluminium corrosion as the degradation mechanism. His goal was to reduce test times by adopting appropriate test conditions. He proposed an analytical model (Eq. 4.1) correlating the lifetime of an encapsulated component (time-to-failure or TTF) with

temperature and relative humidity levels:

$$TTF = A_0 RH^{-n} e^{\frac{E_a}{kT}} \tag{4.1}$$

where TTF is the Time-To-Failure (in hours),  $A_0$  is a constant,  $n$  the relative humidity exponent (also called humidity parameter),  $k$  is Boltzmann’s constant and  $E_a$  is the thermal activation energy. This model extends Arrhenius equation by including relative humidity (RH) with a power law modulated by the parameter  $n$ . This empirical model has been extensively re used in other fields of semiconductors reliability [40] [41].

In order to compare different TTF for getting an acceleration factor between several sets of temperature and relative humidity conditions, the same failure mechanism has to be identified. From the previous results of chapter 3, we have been able to establish a reversibility threshold for electrical degradation at a 1% relative variation in capacitance. The nuance is that this threshold does not directly represent a failure criterion for a chip. Instead, it can be seen as the point at which moisture begins to irreversibly interact with the different materials. To establish a real failure criterion, we would need to test the active parts of the components. However, it was not feasible with our test vehicles.

To compensate the lack of real failure criterion, we redefine the Time-To-Failure (TTF) as the duration to reach a criterion of relative capacitance variation. This allows to focus on what happens at this reversibility threshold (1% capacitance shift) and also for others capacitance variation. For instance, during the transition of conduction mechanism for capacitance variations above 5%. It also enables to assess whether the extracted parameters (activation energy,  $E_a$ , and the power law exponent,  $n$ ) remain constant regarding the capacitance variation.

For parameter extraction, several wafers are stored (one wafer per storage condition). Regarding the activation energy, two sets of three storage conditions at constant humidity were performed. The first set was at 85% RH with more aggressive temperatures compared to the second set at 60% RH (Table 4.1). Then, for the humidity parameter ( $n$ ), there are three storage conditions at a constant temperature of 60°C.

<b>T°C / RH</b>	<b>45%</b>	<b>60%</b>	<b>85%</b>
<b>23°C</b>	X		
<b>30°C</b>		X	
<b>60°C</b>	X	X	X
<b>85°C</b>		X	X
<b>130°C</b>			X

Table 4.1: Temperature and relative humidity conditions being tested

To obtain both parameters, we start by taking the natural logarithm of the Peck formula (Eq. 4.1):

$$\ln(TTF) = \ln(A_0) - n\ln(RH) + \frac{E_a}{kT} \tag{4.2}$$

The methodology involves conducting linear regression across three or more conditions, keeping in a first step the relative humidity constant. Throughout these regressions, the

term associated with humidity and the constant  $A_0$  remain consistent. From this analysis, we derive the activation energy from the slope of the regression between  $\ln(\text{TTF})$  and  $1/T$ . Similarly, the humidity parameter  $n$  can be determined by analyzing at least three storage conditions at constant temperature.

Finally, to summarize, this chapter focuses on adapting the Peck model to moisture-induced degradation in representative BEOL integrated structures. We will first discuss the extraction of parameters ( $E_a$  and  $n$ ) for the model. Our discussions regarding how these parameters evolve with selected capacitance variation criteria will lead us to consider the sensor's positioning relative to the seal ring opening. Ultimately, applying the model across various storage conditions will yield a list of acceleration factors. It will be interesting to compare these factors with JEDEC standards and commonly accepted empirical considerations in the industry regarding accelerated testing under humid heat conditions.

## 4.2 Parameters extraction

The first parameter to be extracted is the activation energy. In chemistry, the activation energy corresponds to the minimum amount of energy required for a chemical reaction to occur. It is a crucial factor in determining the rate of a reaction. The Arrhenius model is an empirical model that helps to understand the effect of temperature on reaction rates. The exponential dependence of the temperature relates to the fact that even small changes in temperature can lead to significant changes in reaction rates.

### 4.2.1 Activation energy : 1<sup>st</sup> serie at 85%RH

As mentioned previously, the first three storage conditions to determine the activation energy are: 60°C/85%RH, 85°C/85%RH, and 130°C/85%RH. These tests are commonly used in industry to accelerate failure mechanisms and study component reliability. Figure 4.3 displays the results of relative capacity variation over storage time.

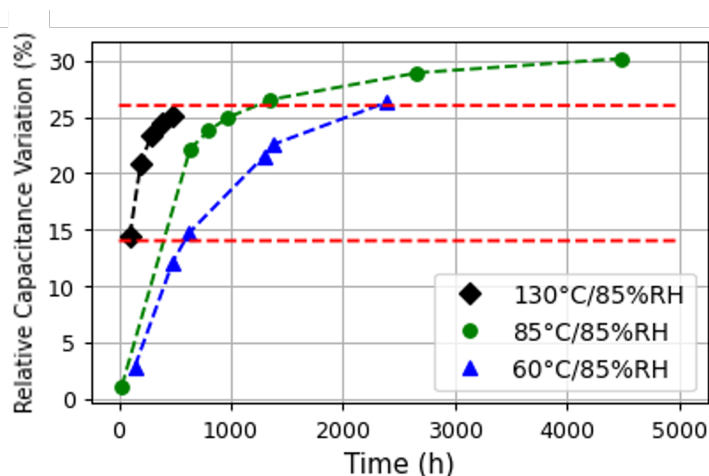


Figure 4.1: Relative capacitance variation regarding time of storage for the 1st serie of storage conditions

The comparison range in terms of capacitance shift for the three storage conditions (without extrapolating results) is limited. This range is between 15% and 25%. This is because, after the first HAST run, the capacitance variation is already around 15%. To make use of the Peck model, it's imperative to determine the time needed to reach each of relative capacity variation criteria (TTF). This determination is achieved by employing linear interpolation between each data point. A comprehensive list of TTF values for every criterion is displayed in table 4.2. It should be emphasized that a unique table is generated for each individual chip.

Relative Capacitance criteria	60°C/85%RH	85°C/85%RH	130°C/85%RH
14 %	571	212	97
15 %	600	259	113
16 %	651	305	129
...	...	...	...
22 %	1387	633	276
23 %	1658	744	363
24 %	1928	881	552

Table 4.2: Time to failure (TTF) in hours for different criteria of relative capacitance variation for the 1st sample

Subsequently, to extract the activation energy, a linear regression is performed between  $\ln(\text{TTF})$  and the inverse of the temperature for each chip and every capacity variation criterion. The result for the 14% criteria of relative capacitance variation is depicted in Figure 4.2. We observe a strong linearity with a correlation coefficient of 0.99. The activation energy is derived from the slope.

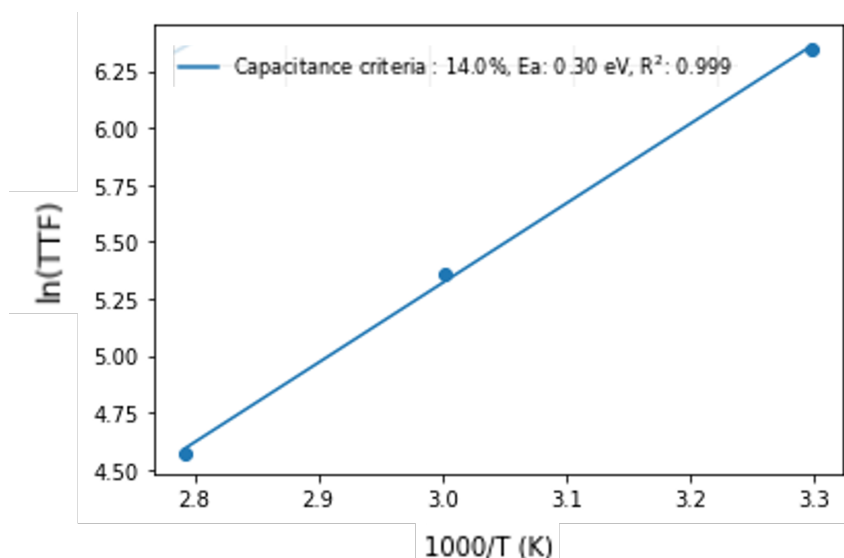


Figure 4.2: Arrhenius plot of the natural logarithm of time to failure with a linear regression ( $E_a=0.30$  eV)

Fig 4.2 result reflects the use of one sensor per wafer, positioned uniformly across all the wafers (different storage conditions) to minimize variability caused by edge effects on individual wafers. When all data is analyzed, Figure 4.3 depicting the evolution of activation energy against the criterion of relative capacity variation can be generated.

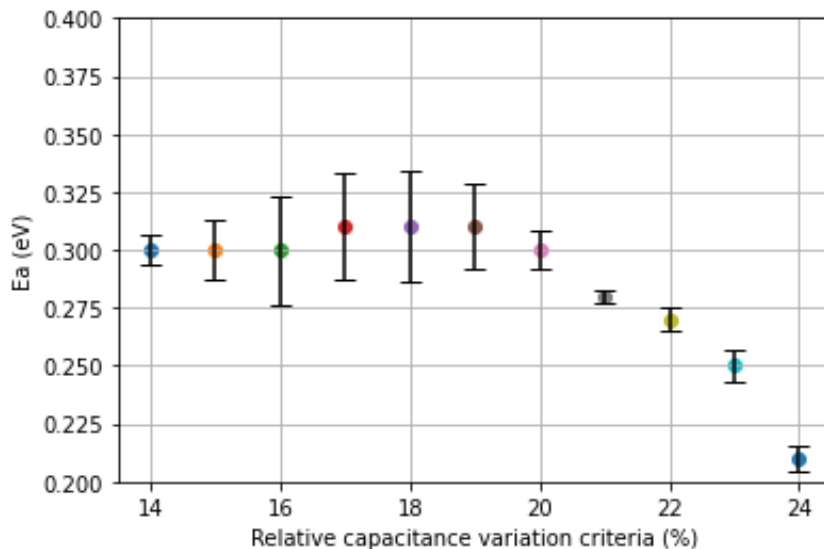


Figure 4.3: Activation energy regarding the capacitance variation criteria for the 1<sup>st</sup> serie of storage conditions

The activation energy of 0.3 eV remains almost constant across the capacity variation range. However, some variability is noted, which could be assigned to inaccuracies of the linear fitting applied to the capacitance variations experimental data. Moreover, there is a reduction in the activation energy ( $E_a$ ) observed beyond a 20% capacitance variation. This decline is suspected to be influenced by the Highly Accelerated Stress Test (HAST) conditions (130°C/85%RH). This particular storage condition introduces a variable not present in the other conditions: the effect of pressure. Perhaps that mechanisms not encountered under the two standard conditions emerge. Unfortunately, the impact of pressure is not quantifiable within the scope of this study.

For this reason, we chose to conduct a second series of storage tests. The average relative humidity of the atmosphere varies significantly, but generally, it falls within a range of 35% to 95%. Thus, we decided to use the middle of this range (60%RH) for the new storage tests. This will also allow us a broader criterion range for capacity variation, as we are once again limited by the HAST (with a 14% variation right after the first run).

#### 4.2.2 Activation energy : 2nd serie at 60%RH

The graph representing the evolution of the relative capacity variation of our structures as a function of storage time for the 3 new temperatures (30°C, 60°C, and 85°C) at 60%RH is shown in Fig. 4.4. We notice that compared to Fig 4.3, we obtain a much better common range of capacity variation between the 3 storages (from 5% to 25%). By following the same procedure as before, we obtain the activation energy for each capacity variation criterion from the slope resulting from the linear regression between  $\ln(\text{TTF})$  and  $1/T$ .

We then reach Fig 4.5 which represents the evolution of the activation energy as a function of the relative capacity variation criterion. An average activation energy of  $0.24 \pm 0.05$  eV is obtained for capacity shifts ranging from 5% to 25%. We notice an increase in the activation energy in the 5% to 14% range, then a stagnation up to 18% and finally a

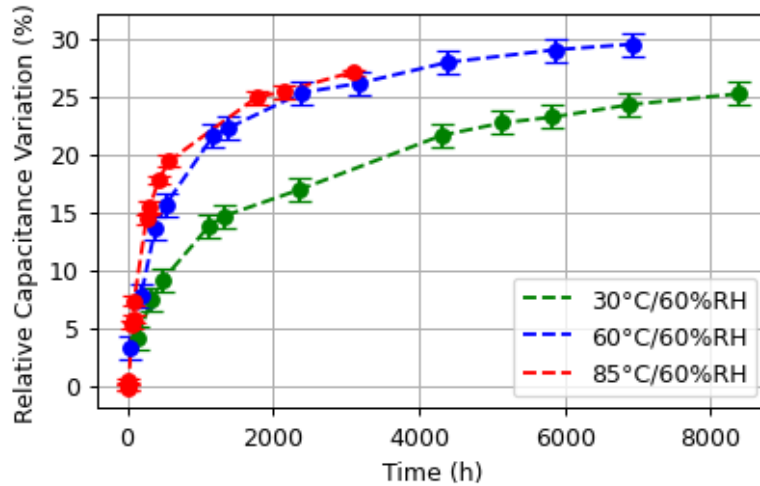


Figure 4.4: Relative capacitance variation vs time of storage for the 2nd series of storage conditions

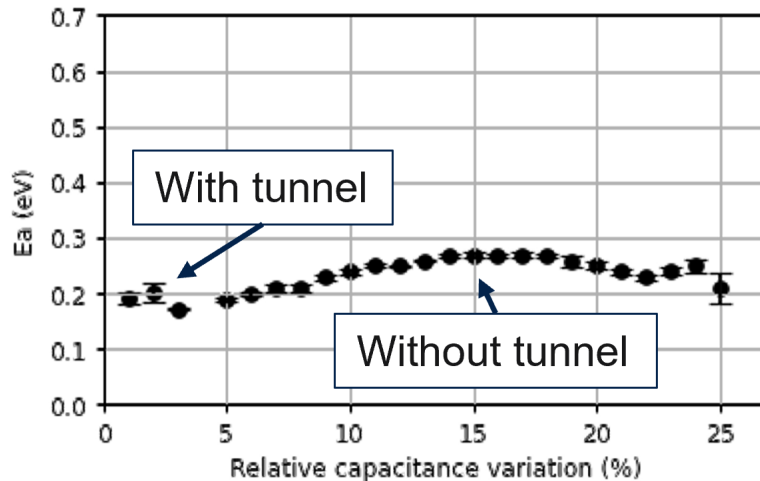


Figure 4.5: Activation energy (eV) over the range of failure criteria (Relative capacitance variation) over all the samples

decrease. Moreover, this result is consistent with that of the previous 3 storages (Fig 4.3). Indeed, we observe an activation energy ( $E_a$ ) close to 0.3 eV for capacitance variation criteria above 14%, with a decrease observed at around 18% capacitance variation. This reduction, being consistent across both storage series, indicates that the pressure conditions of the HAST are finally not that significant with respect to the activation energy results.

Like in the previous chapter, to study smaller capacitance variations below 5%, samples with different tunnel sizes were used. This approach made it possible to record the time required to reach the 1% and 2% criteria. The results have been directly added to Figure 4.5 and confirm the stability of the activation energy across the 0 to 8% interval. Beyond this interval, however, it varies. An initial argument would be to say that this variability is due to linear fitting or measurement inaccuracies. However, it must be understood that an activation energy is related to a physical mechanism and more specifically in our

Peck model, a capacity failure mechanism. But here we are in a situation where we do not initially have enough information to justify which degradation mechanism is involved. Among the possible mechanisms we have first water diffusion with and without interaction in the different dielectrics layers and interfaces. Then, the interaction of water with different metals (Copper and TaN/Ta). So, we are dealing with an effective activation energy due to the complexity the diversity of materials in the sample. The competition between different mechanisms can explain the observed activation energy variation. We can therefore consider that we obtain a constant effective activation energy of  $0.24 \text{ eV} \pm 0.05 \text{ eV}$ .

In the literature, there are several articles on this subject. Some studies show that physisorbed water has an activation energy of  $0.3 \text{ eV}$ . For instance, Raja [42] uses impedance spectrometry on low-k dielectrics moist samples before and after annealing to identify two kinds of water states: physisorbed water ( $E_a = 0.32 \text{ eV}$ ) and chemisorbed ( $E_a = 0.52 \text{ eV}$ ). This observation is also evidenced by most TDS (thermal desorption spectroscopy) studies of moisture in low-k dielectrics [10], [15]. A diffusion/reaction process is described by Doremus [43]. According to this mechanism, water molecules diffuse into the silica glass through a combination of surface adsorption and bulk diffusion. Surface adsorption involves the attachment of water molecules to the surface of the silica glass, where they can interact with surface hydroxyl groups. Bulk diffusion, on the other hand, involves the movement of water molecules through the interior of the silica glass. This process is driven by the concentration gradient of water and the mobility of water molecules within the glass structure. Doremus proposes that the surface adsorption and bulk diffusion mechanisms are linked through a reaction mechanism that involves the formation and dissociation of silanol groups.

However, in these works, all the samples studied are a simple layer of bulk material. In our case, the  $\text{SiO}_2$  stack studied is much more complex with stacks of different materials (Low-k, SiCN, Copper, TaN/Ta). Some articles have studied two-layer stacks : For example, Li [44] determined a thermal activation energy of  $0.27 \text{ eV}$  for moisture diffusion along the interface between a silicon substrate and organosilicate glass through a mechanical study and modeling. They also highlighted a loss of adhesion between these two layers. More recently, Duan [45] also pointed out a thermal activation energy of  $0.27 \text{ eV}$  using serpentine sensors in ULK stacks. However, in his work, only 2 conditions with a similar relative humidity ratio are considered.

The most interesting results are given by Xu [46] who used the Time-of-Flight Secondary Ion Mass Spectrometry (ToF SIMS) characterization technique to determine the thermal activation energy values of  $0.74 \text{ eV}$  for  $\text{SiO}_2$  bulk diffusion and  $0.21 \text{ eV}$  for interfacial diffusion, observed within a temperature range of  $8$  to  $90^\circ\text{C}$ , at the interface between TiN and PECVD  $\text{SiO}_2$ . We therefore strongly suspect that around  $8\%$  of capacitance variation, the increase of  $E_a$  is caused by the beginning of moisture diffusion into the bulk of dielectrics. This clearly shows the difficulty of associating only one degradation mechanism due to moisture penetration in complex stacks.

Furthermore, it is noteworthy that a phenomenon characterized by an activation energy of  $0.2 - 0.3 \text{ eV}$  is considered to have a low activation energy. This indicates that it can be relatively easily thermally activated at room temperature ( $25^\circ\text{C}$ ), as the average thermal energy of molecules in the environment is sufficient to overcome this energy bar-



rier. This range of energies aligns with those typically associated with hydrogen bonds, which span from 0.1 to 0.4 eV. Hydrogen bonds are relatively weak in comparison to other bond types, such as metallic, ionic, and covalent bonds, which generally possess energies ranging from 1 to 10 eV. In contrast, Van der Waals interactions exhibit even lower energies, often below 0.1 eV. Therefore, the relatively low activation energy observed suggests that the reaction is driven by weak interactions, such as hydrogen bonding, rather than stronger chemical bonds.

After reviewing the results proposed by the literature, they support our result of low activation energy about 0.2 - 0.3 eV related to interfacial diffusion as the 1<sup>st</sup> order degradation mechanism.

### 4.2.3 Humidity parameter, n

Now that we have extracted the activation energy parameter  $E_a$ , our focus shifts to the humidity parameter. As a reminder, we rely on Peck's equation (4.1) and, more specifically, the logarithm of the time to failure:

$$\ln(TTF) = \ln(A_0) - n \ln(RH) + \frac{E_a}{kT} \tag{4.3}$$

By plotting  $\ln(TTF)$  as function of  $\ln(RH)$  for three fixed temperature storage conditions, the absolute value of the slope gives us the parameter n. The three storage conditions used are all at 60°C and vary between 45, 60, and 85% relative humidity.

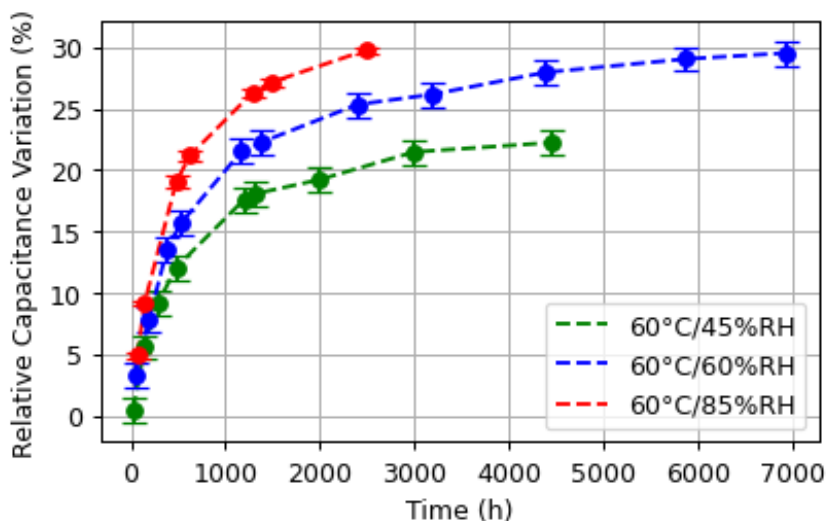


Figure 4.6: Relative capacitance variation vs time of storage for the humidity parameter determination (structure without tunnel)

Firstly, we begin by identifying the time to reach each capacitance variation criterion (unitary: 1, 2,..., 22%) by linear interpolation of experimental data (Fig 4.6). It can be seen that the common interval in terms of capacitance variation is from 5% to 22% since the first measurement point for the storage at 60°C/85%RH is at a 5% capacitance variation. This doesn't allow us to study the 1% threshold criteria established before. To study capacitance variations smaller than 5%, samples with different tunnel sizes were

also used as seen previously in chapter 3. This method allows us to record the time to reach the 1% and 2% criteria. Strictly speaking, we cannot assess the influence of the tunnel geometry on the extraction of the parameter. Therefore, a critical eye should be kept if the results differ between the two types of configurations (with and without tunnel).

Next, we plot the logarithm of the time to reach the capacitance variation criterion against the logarithm of the relative humidity rate. For example, for capacitance variation criteria of 10%, Fig 4.7 demonstrates that we achieve good alignment of points for linear regression ( $R^2 \approx 0.99$ ). The slope's value directly provides the humidity parameter, which is in the order of 1.0 for the 10% criterion. By repeating this for each capacitance variation criterion, Figure 4.8 illustrates the evolution of the humidity parameter as a function of the capacitance variation criterion.

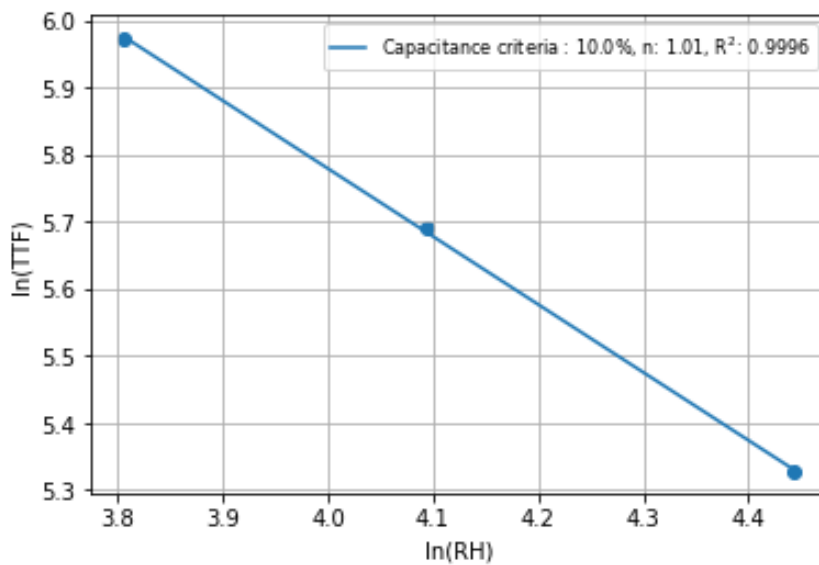


Figure 4.7: Humidity parameter extraction from Peck model (n=1.0)

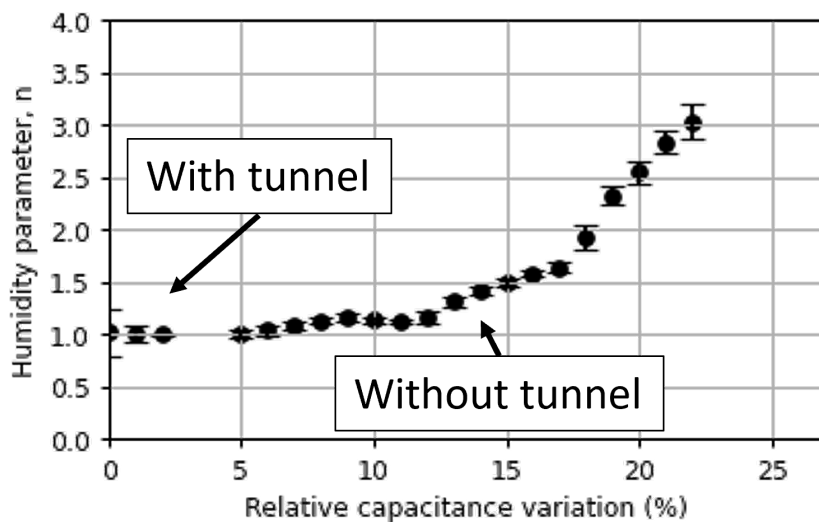


Figure 4.8: Humidity parameter vs Relative capacitance variation criteria

We observe that the humidity parameter remains constant at approximately  $1 \pm 0.2$

up to a 10 - 12% capacitance variation. This implies that the time to failure is directly inversely proportional to humidity rate variations at a constant temperature in this range of capacitance variation. Then it increases significantly to reach 3 for a 23% capacitance variation criteria.

Interpreting this result is challenging because the parameter is empirical and lacks a physical meaning. In his article, Peck reported  $n$  values around 2.5 to 3 (focusing on aluminum corrosion), while other studies, such as those on phenom, identify  $n$  values in the order of 11 - 12 but without attributing a physical significance to it, other than suggesting this parameter seems to be specific to each component.

In addition to the slope, Figure 4.7 also provides the y-intercept ( $\ln(A_0) + \frac{Ea}{kT}$ ) for each capacitance variation criterion which is around 8 at 25°C. Hence, for each of these criteria, a graph can be plotted representing the time required to reach it as a function of the humidity rate according to Peck's model at a constant temperature. An example is shown in Figure 4.9 for a 5% capacitance variation criterion and various  $n$  values :

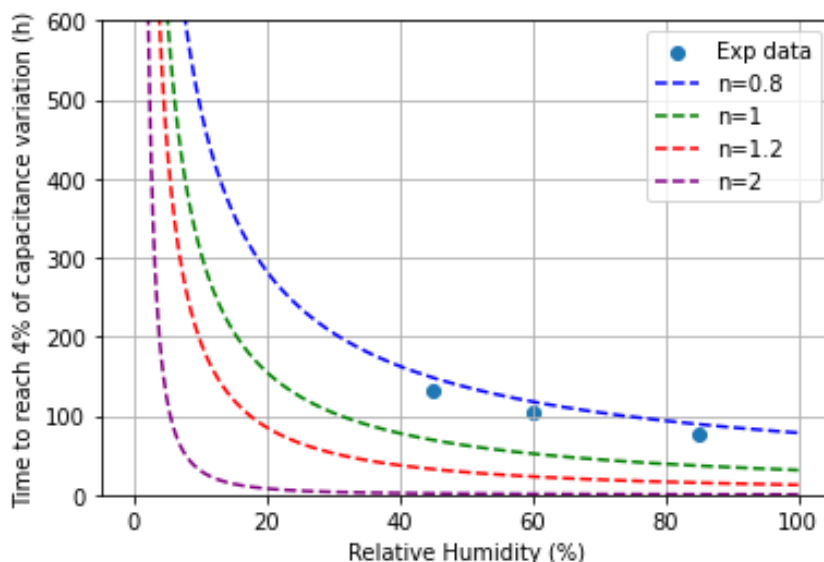


Figure 4.9: Peck model at fixed temperature (60°C) and different humidity parameter ( $n$ ) values

The experimental points well correspond to the Peck model with a  $n$  ranging between 0.8 and 1. This model appears to be consistent with the boundary conditions in terms of humidity. For very dry air (RH close to 0), the TTF tends towards infinity. Indeed, without humidity, failure cannot occur. For RH close to saturation (liquid water), we have the worst-case scenario for moisture study with the shortest time to failure.

Furthermore, to see the influence of the humidity parameter, the curve for  $n$  varying from 0.8 to 2 is depicted in Fig. 4.9. This observation reveals that for  $n=2$ , corresponding to a 12% shift in capacitance, the influence of relative humidity diminishes. This is illustrated by the curve becoming increasingly horizontal as  $n$  increases. If the influence of humidity is reduced, it is likely due to the moisture transport through the Low-k/SiCN interfaces to the sensors no longer being the dominant mechanism. Instead, it gives way to moisture diffusion within the bulk of the dielectrics, where the diffusion coefficient is much lower. These findings are consistent with earlier findings in the chapter concerning

leakage current evolution relative to capacitance variation and  $E_a$  results. All the behaviors modifications were around 10% of capacitance shift.

It would have been interesting to conduct storage with a humidity rate below 20%, but this introduces new challenges. For example, the influence of the waiting time between removing the plate from the oven and experimental measurements would need to be reevaluated to limit exposure to the ambient laboratory air, which is at 45%RH. This is why all tested storage conditions have a relative humidity rate above 45%RH.

To conclude, the various observations made through the characterizations are grouped into four categories ( $E_a$  and  $n$ ,  $I(V)$ , Reversibility, and Diffusion Path) in Figure 4.10.

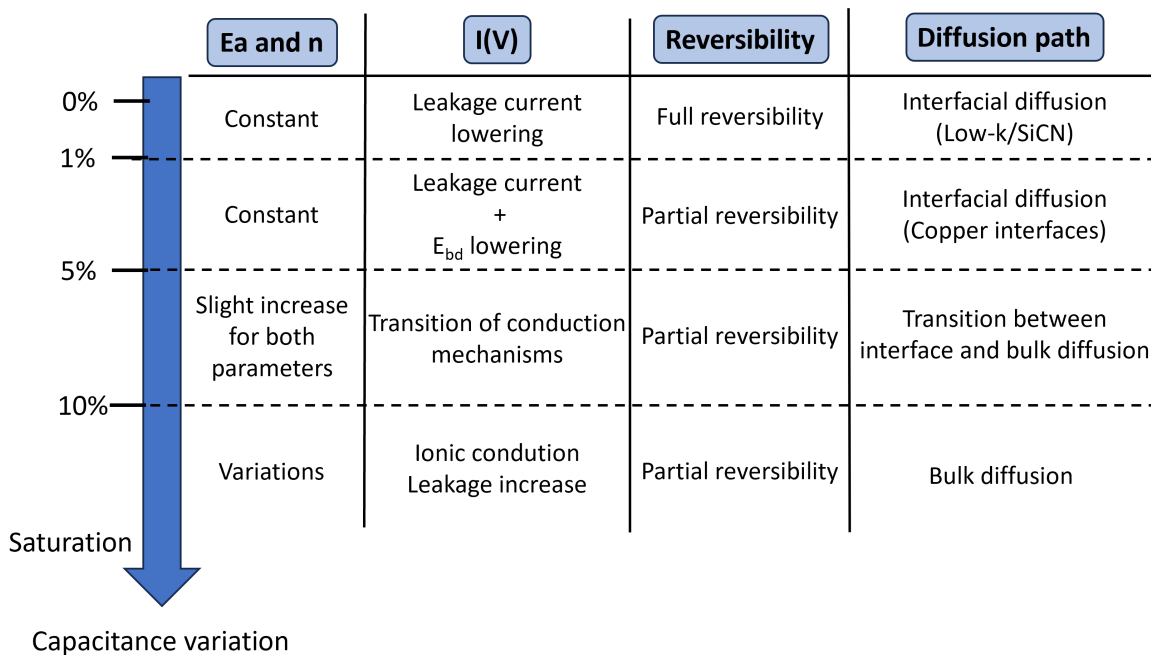


Figure 4.10: Summary of different results obtained in this work regarding the relative capacitance variation

Based on these results, we have been able to consider a constant activation energy  $E_a$  of  $0.24 \pm 0.05$  eV and a humidity parameter of  $1 \pm 0.2$  over the range of 0 to 10%. It was demonstrated that beyond a 1% capacitance variation due to humidity, the reversibility of electrical degradations by drying is completely lost. Consequently, this initial criterion can already be selected as interesting for the determination of an acceleration factor in the following section.

It is also noteworthy that the change in conduction mechanism identified in the previous chapter occurs around an 8 to 10% capacitance variation. This raises the question of whether there is a correlation between the  $E_a$  and  $n$  variations and the observed change in electrical behavior. Our hypothesis suggests that the increase in activation energy indicates that humidity initially binds to energetically favorable defects, and then gradually fills all available sites. Some water molecules also bind to other water molecules that are already attached to the materials. When the majority of sites are occupied at the interfaces, humidity begins to form clusters. We assume that the change in conduction mechanism and the variations in activation energy are due to the formation of these clus-

ters followed by the diffusion into the bulk of dielectrics.

These results highlight the dependency of both the activation energy and the moisture parameter on the chosen capacity variation criterion, thereby underlining the complexity and specificity of modeling moisture diffusion. Consequently, the acceleration factor we are about to calculate will reflect this dependency.

### 4.3 Influence of Sensor-Sawing Distance on Measurements

Before determining the acceleration factor, this section presents a particular study that reveals a counter intuitive phenomenon. The results from the previous section indicated an activation energy ( $E_a$ ) ranging between 0.25 and 0.3 eV. These findings were derived using data from sensors located approximately 4 mm from the chip opening. We now examine the variation in activation energy for sensors placed at a proximity of 40  $\mu\text{m}$  from the opening to assess the effect of proximity to the seal ring opening.

#### 4.3.1 Context

Figure 4.11 illustrates the evolution of the activation energy based on the relative capacitance variation criteria for sensors positioned 40 microns from the opening. It also recalls the results obtained for sensors positioned 4 mm away.

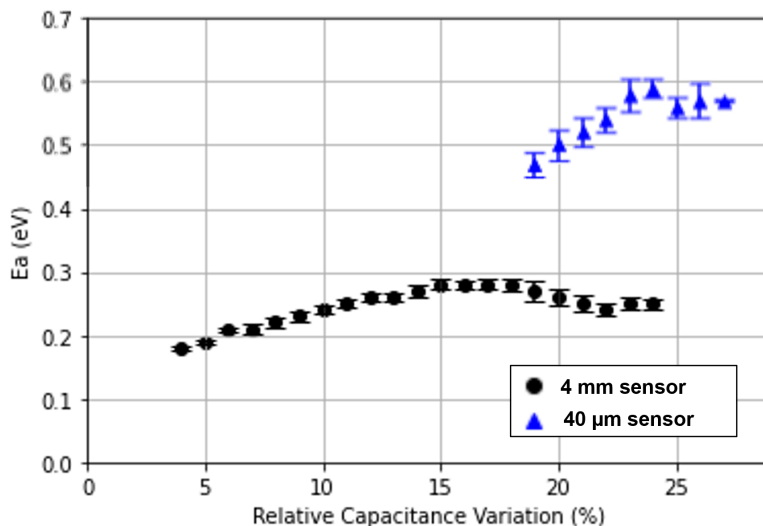


Figure 4.11: Activation energy (eV) over the range of failure criteria (relative capacitance variation) for a sample located at 4 mm and 40  $\mu\text{m}$  from the sawing.

We observe that for the 40  $\mu\text{m}$  distance, the activation energy is not within the 0.2-0.3 eV range but rather around 0.5 eV, with significant variation depending on the capacitance variation criteria. This figure clearly demonstrates that the extracted activation energy depends on the sensor’s distance from the opening, confirmed by the 18% criteria overlay. A higher activation energy indicates a phenomenon with a stronger temperature dependence. For sensors at 40  $\mu\text{m}$ , it is impossible to verify the activation energy value

for criteria below 18% capacitance variation. Indeed, after just a few minutes of storage, the sensor's capacitance has already increased by 18%. This observation is logical, as the closer the sensor is to the edge of the opening, the more rapidly the capacitance changes. Our primary hypothesis to explain the difference between  $E_a$  for criteria between 18 and 24% of capacitance variation involves a competition between desorption and diffusion. It mainly affects sensors closest to the opening.

To further investigate this hypothesis, a test structure similar to previous ones was used but with larger dimensions. This sample is composed of 26 sensors that were arranged over approximately 3.5 mm from the seal ring opening (with no sensors between 1.2 mm and 2 mm due to design considerations). The larger dimension will allow to track the evolution of moisture diffusion regarding the distance from the opening. Figure 4.12 presents a schematic of this structure (not to scale). Unlike previous structures with a deliberate 60 microns opening in the seal ring followed by sawing near the seal ring to allow moisture penetration into the chip, here, the sawing is done directly on an edge of the seal ring.

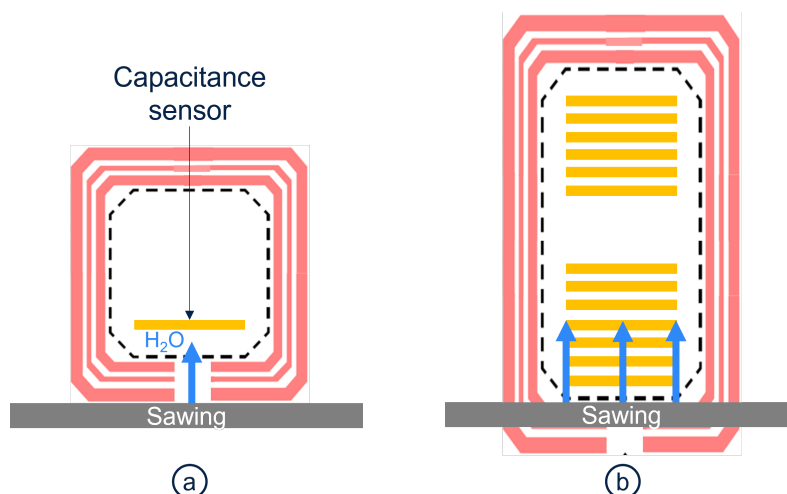


Figure 4.12: Schematic of (a) previous sample and (b) sample used in this section

Following our previous approach, we will first concentrate on the storage at ambient conditions (23°C/45%RH). Then, we will examine and compare this phenomenon across different storage conditions.

### 4.3.2 Competition between desorption and diffusion at ambient storage

We have observed that the activation energy obtained is different based on the sensor's proximity to the seal ring opening. Hence, we decided to monitor the capacitance at various positions, as illustrated in Figure 4.13 (showing 5 representative distances out of 26). The behavior of the 67  $\mu\text{m}$  sensor is unusual. It's the sensor closest to the opening, but with the slowest variation in capacitance of all the sensors. For example, the if we look at the 20% capacitance variation criteria, the sensor positioned at 964 microns from the opening is the first to reaches it in 2300 hours. Followed by the sensor at 2643  $\mu\text{m}$  and then 3361  $\mu\text{m}$ . The last sensor to reach this criterion is indeed the closest one from

the opening in approximately 10 000 hours.

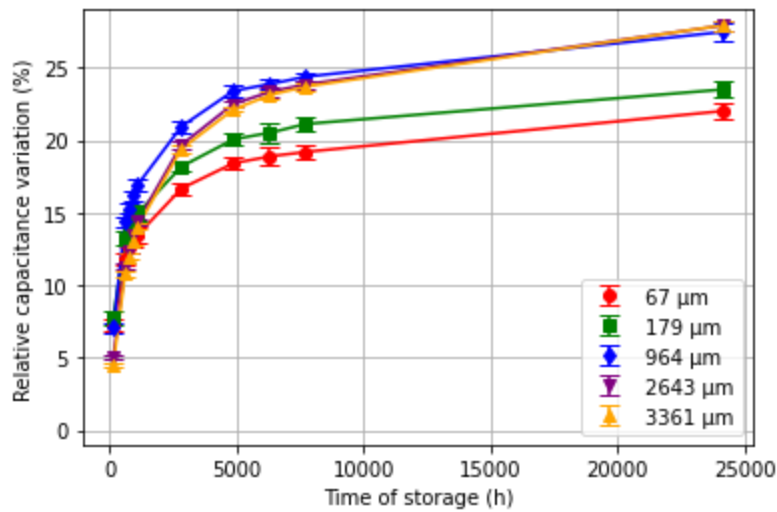


Figure 4.13: Linear interpolation of capacitance shift at ambient storage for 5 sensor at different distance from sawing

Another way to represent this graph is by re using the concept of TTF (Time-to-Failure in hours), as previously discussed, in function of the distance between the sensor and the opening (for a given capacitance variation criterion). An example is shown in Fig. 4.14 for the lowest common capacitance variation criterion among all sensors, which is 7%.

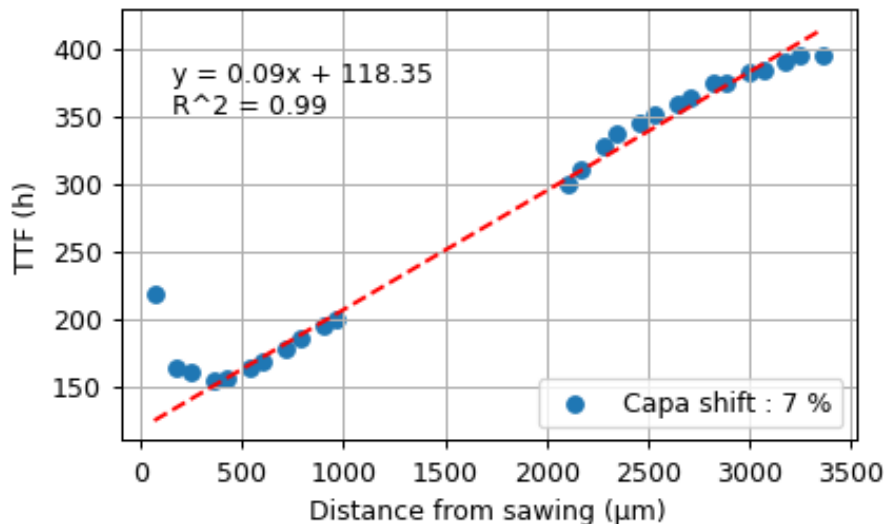


Figure 4.14: Time-to-Failure vs distance from sawing for capacitance shift criteria of 7% and ambient storage

The top-right data point on the graph represents the sensor positioned at 3.3mm from the opening, and it can be observed that it takes approximately 400 hours to reach a 7% capacitance variation. Several observations can be made from this figure. Firstly, there is a clear linear dependence of Time-to-Failure (TTF) concerning the distance, as indicated by the red line with a correlation coefficient of 0.99. This is macroscopically logical, since

the further the sensor is from the opening, the longer it takes to reach a capacity variation criterion.

However, it is evident that the behavior of the first three sensors, located at 67, 179, and 246  $\mu\text{m}$  from the edge, differs from the rest for this capacitance variation criterion. These points are excluded from the linear regression analysis. It takes about 80 additional hours of storage for the first sensor (67 microns) to reach a 7% variation compared to the one located at 425 microns from the opening. This counter intuitive result suggests the existence of an additional mechanism affecting moisture penetration, and its influence decreases with distance to the opening. The most plausible hypothesis is that there is a competition between desorption near the sensors at the opening and moisture diffusion. A threshold distance of 350  $\mu\text{m}$  (TTF around 150 hours) can be defined, beyond which the influence of desorption is minimal compared to diffusion for a 7% criterion.

Now, we aim to investigate the behavior of various capacitance variation criteria. Representing Time-to-Failure (TTF) as a function of distance for different criteria poses significant challenges. For instance, TTF ranges from 150 to 400 hours for a 7% criterion, while it varies from 1500 to 3000 hours for a 17% criterion. To enable the plotting of experimental points for different criteria on the same graph, we represent TTF as a normalized value relative to the TTF of the sensor positioned at the greatest distance (3.5 mm) for each respective capacitance variation criterion. For example, the normalized TTF for the first sensor (40  $\mu\text{m}$ ) is obtained by dividing the time required for this sensor to reach a 7% capacitance variation by the time required for the most distant sensor to reach the same criterion. This approach yields a ratio ranging from 0 to 1, as theoretically, moisture takes longer to reach sensors that are further away. Examples for the 7%, 12%, and 18% shift criteria are presented in Fig. 4.15. Our analysis focuses primarily on distances less than 1 mm, where the competition between the two mechanisms is most pronounced.

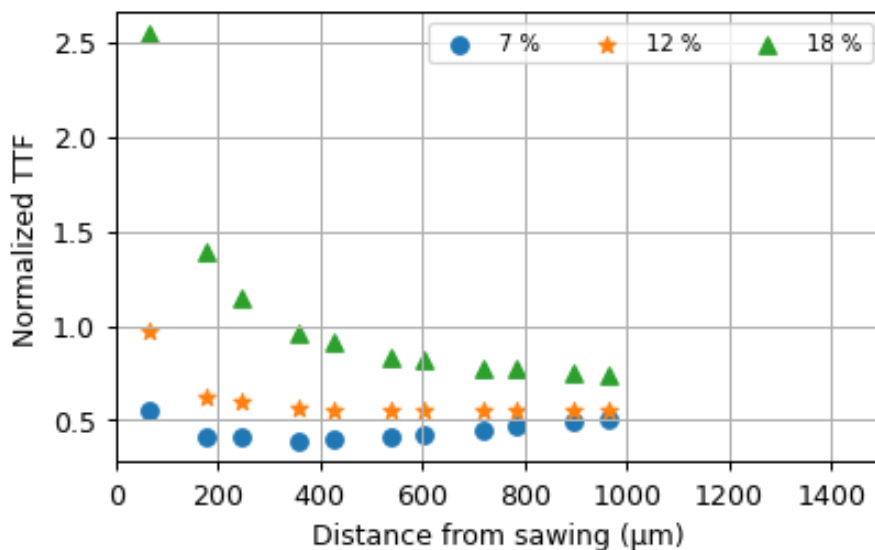


Figure 4.15: Normalized Time-to-Failure vs distance from sawing for 3 different capacitance shift criteria

For the first sensor (40  $\mu\text{m}$ ), we observe that the normalized TTF is approximately 2.5 for the 18% capacitance variation criterion. This indicates that it takes more time for



the closest sensors to reach an 18% degradation compared to farthest one. This result is counter intuitive, as we expected to obtain a ratio between 0 and 1. This likely suggests that an additional mechanism is slowing down the capacitance degradation for the sensor closest to the opening.

For a 7% shift, we observe a linear growth in TTF, except for the initial three sensors, as mentioned previously with a threshold distance about 350 microns. At a 12% variation, it is notable that the first sensor exhibits a normalized TTF of approximately 1. This indicates that it takes an equal amount of time for the first sensor (at 60 microns) and the last one (at 3 mm) to reach the 12% shift. Furthermore, we can observe that the fourth sensor, positioned at 380 microns, is now also affected by this phenomenon, as it displays a greater TTF than the subsequent sensor at 410 microns. This suggests that the threshold distance determined at 7% has evolved with the change in capacitance (i.e storage time). Unfortunately, a linear regression analysis to determine this threshold distance, as done for the previous criterion, is not feasible. Indeed, a constant normalized TTF for sensors between 400 and 1000 microns is observed. This indicates that not only the four first sensors are impacted but all of them over a range of 1mm.

This pattern is even more evident in the curve for the 18% criterion. Here, it is observed that all sensors over a 1 mm range are affected, as the TTF decreases up to this distance. However, a linear dependency is still observed for sensors positioned beyond 2 mm (not shown in this graph). As mentioned in the presentation of structures, due to design considerations, there are no sensors between 1 and 2 mm. So we can't determine the exact threshold distance for each capacitance shift criteria and look at it's evolution. Nevertheless, it can be strongly supposed that this threshold distance is a function that increases with respect to the capacitance variation criteria (i.e. the amount of humidity) but does not exceed 2 mm for the configuration and geometry of our samples.

Having identified this issue, our next step is to gather more information on how temperature and humidity influence this phenomenon. To achieve this, let's examine the outcomes under different storage conditions.

### 4.3.3 Comparison between different storage conditions

To test the hypothesis of a potential competition between diffusion and desorption, we now seek to identify this phenomenon under various storage conditions. The influence of the humidity parameter can be anticipated. Indeed, considering the case of a simple surface placed in a humidity saturated environment (without condensation), there are no available sites for desorption to occur. The only possible phenomenon is diffusion towards the area of lower concentration, namely, the bulk of the material. There cannot be any competition between desorption and diffusion. As the number of molecules at the surface decreases, some sites become available, allowing desorption to occur. Consequently, as humidity increases, we expect to see the influence of desorption decrease on the capacitance variation of sensors closest to the opening.

Experimentally, the same conditions used for extracting the activation energy and the humidity parameter from Peck's model were utilized (Table 4.1). The failure criterion has been set at 23% of capacitance variation, as this is the only criterion that is common (without extrapolation) to all storage conditions.

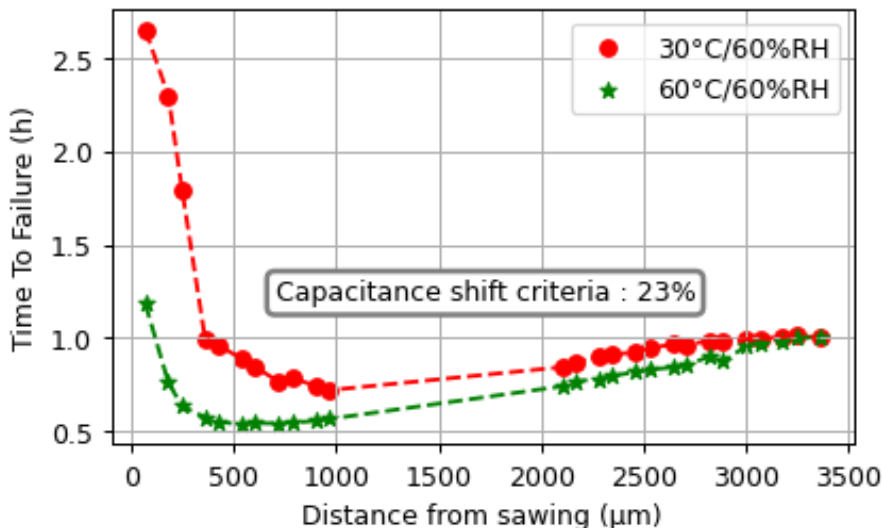


Figure 4.16: Normalized Time-to-Failure vs distance from sawing for 2 different storage conditions with fixed relative humidity (60%RH) and failure criteria (23% capacitance shift)

We begin by comparing the graphs depicting the Time-To-Failure (TTF) as a function of the distance from the sawing under fixed relative humidity storage conditions (Figure 4.16). For the 30°C storage condition, the effect of proximity to the edge is observed for the first sensors. The effect is less pronounced for the 60°C storage. For this conditions, sensors beyond  $\approx 700$  microns follow the linear dependency described earlier. This is happening only after  $\approx 2$  mm for the 30°C storage. This observation is counter intuitive, normally we would expect that the higher the temperature, the greater the desorption, similar to drying. However, when temperature is coupled with humidity, it is more accurate to think in terms of vapor pressure (or water molecules). The ratio between the water vapor pressure and the saturating vapor pressure is constant by the definition of relative humidity. However, the saturating vapor pressure of water is a function that increases with temperature, defined by Rankine [47] equation :

$$\ln(P_{sat}) = 13,7 - \frac{5120}{T} \tag{4.4}$$

If the temperature increases with a fixed relative humidity rate, the saturating vapor pressure increases, as does the water vapor pressure. In other words, warm air can hold more water molecules than cold air. Consequently, the number of water molecules at the surface of the sample increases with temperature, and the probability of desorption decreases. The analogy made previously with a simple surface helps to better understand the problem despite being in a much more complex configuration.

The results for storage conditions with a fixed temperature and varying humidity rate are presented in Figure 4.17. For storage with the highest relative humidity rate, it is observed that the linearity of the time evolution to reach a 23% capacitance variation as a function of distance from the opening is valid for almost all sensors (except the first one). Then, for storage at 60% RH, this linearity remains valid except for the first five

sensors (distance less than 500  $\mu\text{m}$ ).

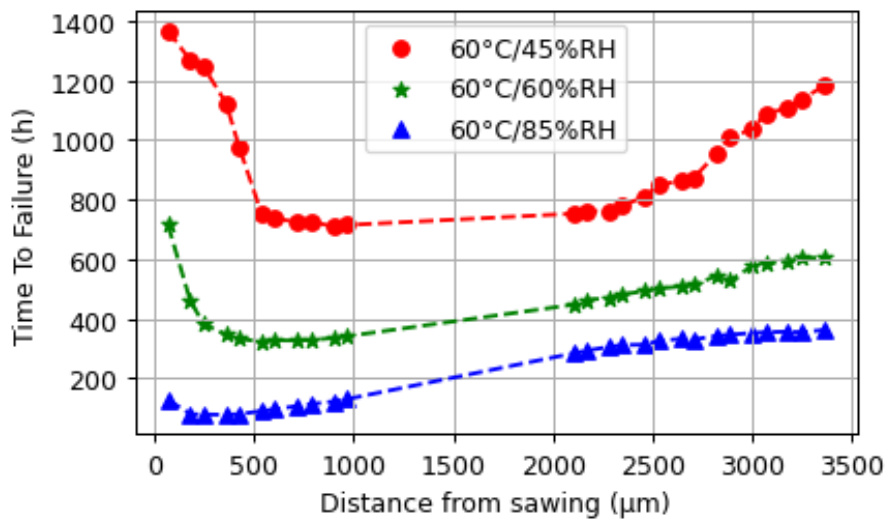


Figure 4.17: Time-to-Failure vs distance from opening for 3 different storage conditions with fixed temperature (60°C) and failure criteria (23% capacitance shift)

Finally, for storage with the lowest humidity rate, the linear aspect completely disappears up to sensors located at 2.5 mm. It is noted that the curve is decreasing up to sensors located 1 mm from the edge. Consequently, it can be said that this competition effect between desorption and diffusion decreases with an increase in relative humidity rate. However, with constant relative humidity storage, it was noted that it is the number of water molecules (or  $P_{vap}$ ) that plays a role in the edge effect. For this reason, all the previous curves are compiled into a single graph (Figure 4.18) indicating the water vapor pressure. For clarity of the graph, only distances less than 1.5 mm are represented.

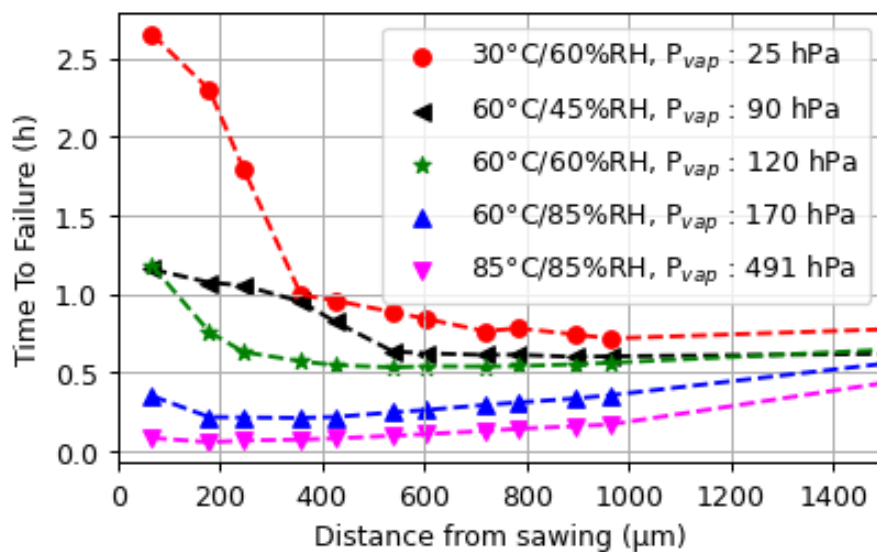


Figure 4.18: Time-to-Failure vs distance from sawing for different moisture vapor pressure at failure criteria of 23% capacitance shift

This graph confirms that the proximity effect is significantly influenced by the water

vapor pressure at the exposed surface. A comparison can be drawn with the desorption results observed after drying at 250°C, where two distinct types of moisture weakly bound and chemically bound were identified due to their differing desorption temperatures. Therefore we assume that the influence of desorption relative to diffusion mainly corresponds to a variation in the concentration of unbound or weakly bound moisture.

We have successfully shown that there is a correlation between the vapor pressure of a storage condition and the fact that the closest sensors exhibit a slower kinetics. This supports our hypothesis of a competition between diffusion and desorption. In the context of developing an acceleration model, the influence of desorption cannot initially be taken into account. It is necessary to place the sensors sufficiently far from the openings, in our case, more than 2mm away. This way, it is possible to extract parameters such as the thermal activation energy and the acceleration factors specific to the moisture diffusion phenomenon in the integrated dielectric structure. This also represents a perspective for the development of a simulation model, either Finite Element Method (FEM) or molecular, capable of resolving the coupling of both phenomena.

## 4.4 Acceleration Factor

In this section, we address the final stage of the project, which involves determining an acceleration factor using Peck’s model applied to our case study. The acceleration factor (AF) is a measure used in accelerated testing to predict how long a product will last under normal conditions by testing it under harsher conditions for a shorter time. It compares the product’s lifespan in normal use to its lifespan under these accelerated conditions. Determining the AF requires a clear definition of what counts as a product failure, which can be challenging due to the variety of ways a product can fail. This method helps to estimate product reliability quickly, but accurately defining failure criteria is crucial for its effectiveness.

### 4.4.1 Context

Using Peck’s relationship as a ratio of test conditions over use conditions enables to eliminate the constant A, as shown below :

$$AF = \left( \frac{RH_{std}}{RH_{accel}} \right)^{-n} \cdot e^{\left( \frac{E_a}{k} \left( \frac{1}{T_{std}} - \frac{1}{T_{accel}} \right) \right)} \quad (4.5)$$

It incorporates the relative humidity levels  $RH_{accel}$  for accelerated conditions and  $RH_{std}$  for standard conditions. The equation also includes the temperatures under normal ( $T_{std}$ ) and accelerated ( $T_{accel}$ ) conditions (in Kelvin).

We have seen that the definition of a failure criterion is crucial, as it directly impacts the acceleration factor and the validity of the accelerated testing results (Ea and n). We have chosen to focus on capacitance variation as a measure of electrical degradation. Through the material studies conducted in second chapter, we were able to identify several material degradations due to the presence of copper and tantalum oxides. We

also highlighted that moisture has a preferential interaction at the interfaces between dielectrics. Unfortunately, it is not possible to directly evaluate the effect of a single isolated degradation on capacitance variation. Therefore, we wanted to assess the reversibility of electrical degradations. We established a threshold of 1% capacitance variation beyond which electrical degradations become irreversible.

By considering this reversibility threshold as a failure criterion, we might be selecting a criteria too strict, which may be limiting. Indeed, by examining the data, we determined an activation energy of  $0.24 \pm 0.05$  eV and a humidity parameter of  $1 \pm 0.2$  over a range of 0 to 10%. We expect that a criterion of 1% and 10% would yield a similar acceleration factor.

The aim of this section is not only to extract acceleration factors over the range of storage conditions we have tested but also to verify if the factor determined by Peck's analytical model is consistent with the one given by experimental measurements.

#### 4.4.2 Acceleration factor

We have chosen to use ambient storage conditions as a reference. As a first step, we can calculate the acceleration factor given by the Peck model for the 6 conditions tested. The results are presented in table 4.3.

<b>AF</b>	<b>30°C/60%RH</b>	<b>60°C/45%RH</b>	<b>60°C/60%RH</b>
<b>23°C/45%RH</b>	1.7	2.8	3.8
	<b>85°C/60%RH</b>	<b>60°C/85%RH</b>	<b>85°C/85%RH</b>
<b>23°C/45%RH</b>	5.4	6.8	9.6

Table 4.3: Acceleration factor based on Peck model with  $E_a = 0.24$  eV and  $n = 1$  for the 0 - 10% capacitance variation range

The acceleration factor obtained between the standard accelerated industry storage THS (85°C/85%RH) and ambient conditions is ranging between 9 and 10. This means that the standard 1000 hours THS (85°C/85%RH) test, often recommended for reliability, corresponds to 10 000 hours of life at ambient conditions. This THS test is generally considered to be equivalent to 96 hours of stress at 130°C/85%RH (HAST) in the industry. We cannot compare HAST storage to ambient conditions since the first capacitance variation criterion obtained for HAST is 14%. However, for the 14% capacitance variation criterion, the humidity parameter ranges from 1.0 to 1.5. While the activation energy stays within the range of 0.24 to 0.29 eV, it is notably centered around 0.29 eV.

Based on these parameters obtained for a 14% capacitance variation criterion, we calculate an acceleration factor of 80 between ambient conditions and HAST. Therefore, a standard 96-hour HAST cycle corresponds to 7700 hours of ambient storage. Furthermore, using these parameters, we determine an acceleration factor of 32 between ambient conditions and THS (85°C/85%RH). This allows us to derive the acceleration factor between THS and HAST as approximately  $80/32 \approx 2.5$ .

By extrapolating experimental results from HAST, considering the activation energy ( $E_a=0.24$ ) and humidity parameter ( $n=1.0$ ) obtained for a 1% capacitance variation, we estimate an acceleration factor (AF) of 2.4 relative to THS. This value is close to the 2.5 obtained for the 14% criterion. Consequently, the 96 hours of HAST do not equate to 1000 hours of THS (85°C/85%RH), but rather to approximately 200 to 300 hours across all capacitance variation criteria. This result underscores the necessity of testing the model under specific conditions and highlights the limitations of JEDEC standards.

### 4.4.3 Model verification

To verify the correlation between experimental data and Peck’s model, we now determine the acceleration factor directly from the data. For this, we record the time to reach each capacitance variation criterion for the different storage conditions and compare them to those of ambient storage. A list of acceleration factors between ambient conditions and all storage settings for each capacitance variation criterion is then obtained. By conducting a linear regression between the experimental acceleration factor and that obtained by Peck’s model for the range of capacitance variation criteria between 0 and 10%, we obtain Figure 4.19

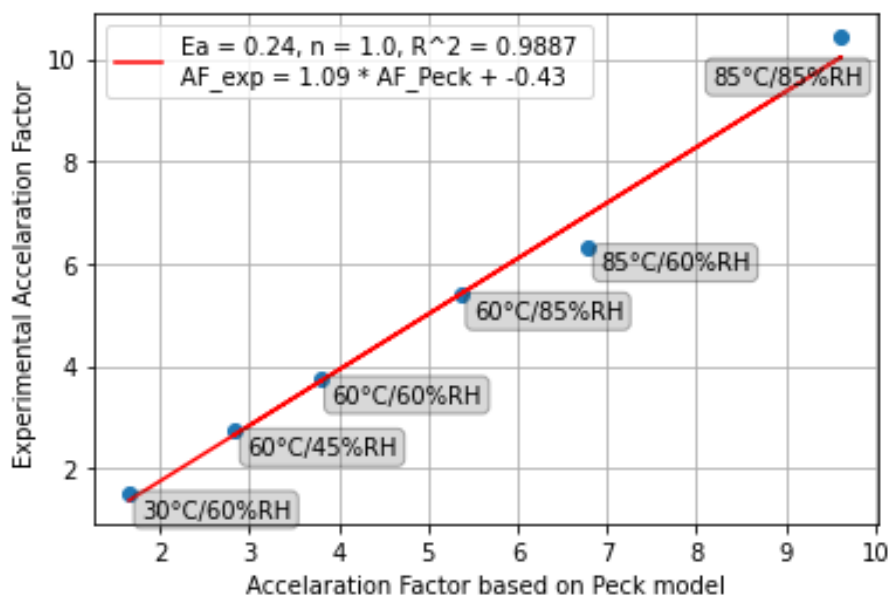


Figure 4.19: Linear regression of the Acceleration factor based on experimental data regarding the Peck model factor (up to 10% capacitance shift validity)

We observe a strong correlation between the experimental data and the model, with an ( $R^2 \approx 0,99$ ). Moreover, based on the equation of the line, we can approximate that  $AF_{Peck} \approx AF_{Model}$ , which validates the use of Peck’s empirical model applied to our study for criteria up to a 10% capacitance variation. For criteria beyond this, we conducted the analysis as a representative exercise for the 21% capacitance variation criterion to include the HAST storage, which is particularly utilized in the industry. This analysis is presented in Fig 4.20. It can be seen that once again we obtain a very good correlation between the experimental data and the model with a slope  $\approx 1$ .

We can now visually verify these results through capacitance variation curves as a function of storage time. Referring back to Table 4.3, which considers an  $E_a$  of 0.24

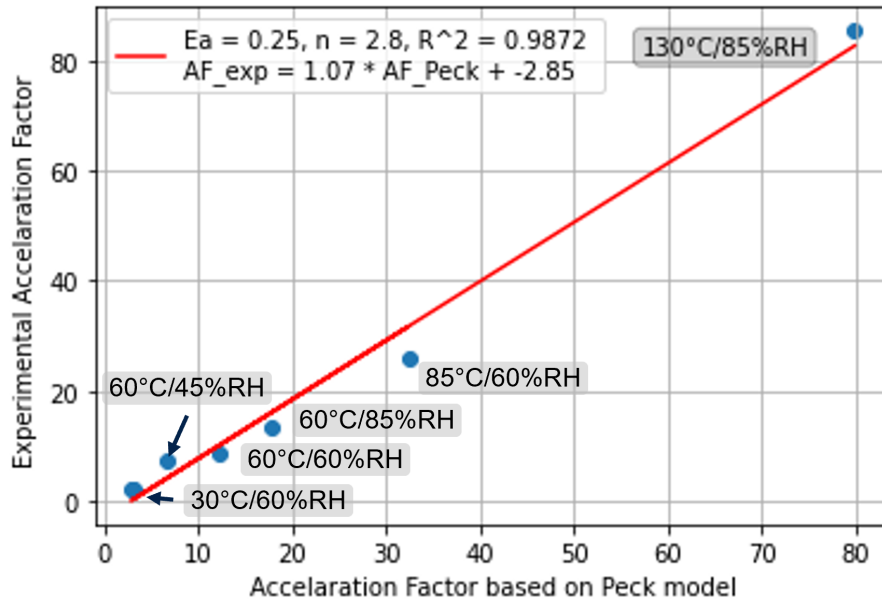


Figure 4.20: Linear regression of the Acceleration factor based on experimental data regarding the Peck model factor for 21% capacitance variation criteria

eV and n of 1, we can plot the curves by multiplying each time from the interpolation between the experimental data of ambient storage by the acceleration factor. The goal is to confirm that the acceleration model does indeed allow ambient storage data to be retrieved from accelerated conditions.

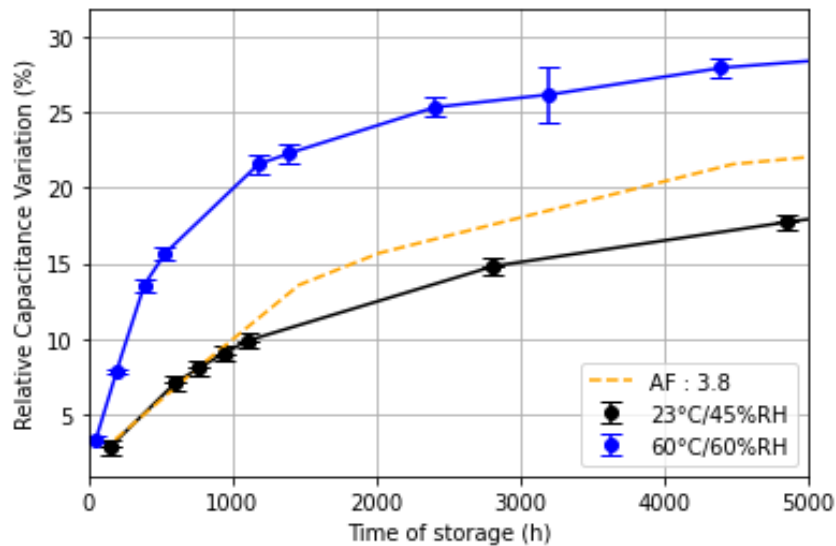


Figure 4.21: Projection of ambient storage data with an extracted acceleration factor of 3.8 for conditions at 60°C/60% RH

This approach yields, for instance in Fig 4.21 for storage at 60°C/60%RH. The dashed curve represents a projection of the curve at 60°C/60%RH with the acceleration factor. As expected, with an AF of 3.8, we obtain a good description of the capacitance evolution within the 5 to 10% interval. Results from structures with tunnels confirm this outcome for variations of 1% in capacitance as well. However, beyond 10%, the model no longer

seems valid (not shown here).

The same exercise is performed for storage at 85°C/85%RH (Figure 4.22), further confirming a good projection through Peck’s model, providing a good approximation of the acceleration factor for the first 10% of capacitance variation. Beyond this, the model is not suited to accurately describe the behavior of capacitance variation. Furthermore, it is worth recalling that a change in the conduction mechanism was observed around a 10% capacitance variation. Consequently, we strongly suspect that around this capacitance variation criterion, the degradation mechanism represented by the diffusion of unbound or weakly bound moisture is no longer the dominant mechanism. Other mechanisms, such as various oxidations, may occur.

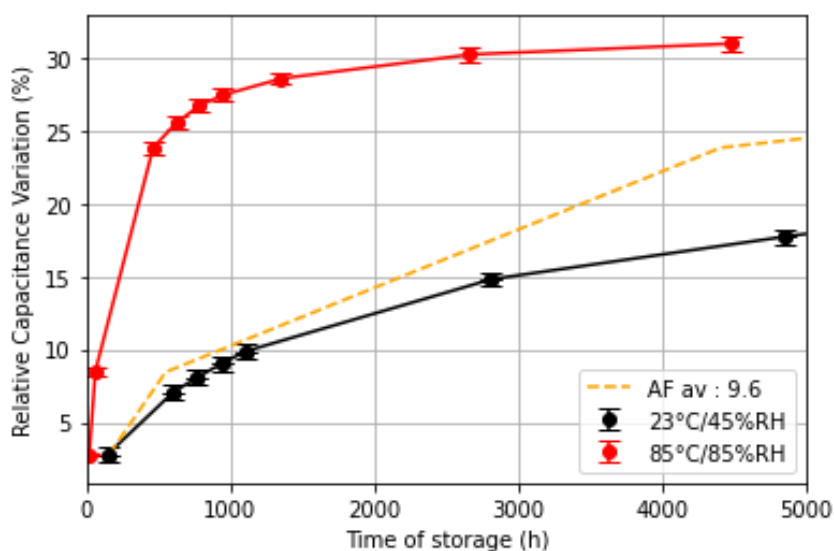


Figure 4.22: Projection of ambient storage data with an extracted acceleration factor of 9.6 for conditions at 85°C/85% RH

Finally, we notice a larger gap between the ambient curve and the dashed line for the storage at 85°C/85%RH compared to the storage at 60°C/60%RH over the 0 to 10% interval. This observation is quite visible on Figure 4.19 looking at the gap between the point representing the 85°C/85%RH storage and the linear regression in red. To achieve greater accuracy, a more extensive set of experimental data points, evenly distributed over time, would be required. Due to logistical reasons and the availability of testers and ovens, this was challenging. Thus, the use of linear interpolation is somehow limiting.

## 4.5 Conclusion and Perspectives

### 4.5.1 Conclusion

In conclusion, this section pursued two main objectives: firstly, to determine the acceleration factor between various storage conditions, and secondly, to validate the consistency of the analytical model chosen with experimental data.



To achieve this, the well-established Peck model in moisture acceleration studies, which enables linking the Time-To-Failure of a sensor with material parameters. We were compelled to redefine the Time-To-Failure as the time required to reach a specified capacitance variation criterion. Through this approach and the data collected from multiple storage conditions, we extracted values for  $E_a$  and  $n$ . We observed that within a 0 to 10% capacitance shift range,  $E_a$  and  $n$  can be considered constant. However, beyond this range, particularly for shifts greater than 10%, we encountered overlapping degradation mechanisms that caused  $E_a$  and  $n$  to vary.

Additionally, our study highlighted another limiting factor: the evolution of these parameters in relation to the distance between the sensor and the seal ring opening. Using a chip with multiple sensors distributed over nearly 4 mm, we demonstrated that sensors located within 2 mm of the opening may experience a desorption phenomenon that slows down the capacitance variation.

This hypothesis of desorption phenomenon was supported by comparing sensor behavior (up to 2 mm distance) under different storage conditions. We found that the intensity of this phenomenon depended on the vapor pressure of each storage condition, with higher vapor pressure conditions showing less pronounced effects. This suggests that the distinction between "near" and "far" sensors is not solely due to material degradation mechanisms but also involves interaction with the external environment through the 60 micron seal ring opening.

Consequently, optimal conditions for applying the Peck model to extract  $E_a$  and  $n$  parameters, which inherently correspond to the materials, involve comparing storage conditions within the 0 to 10% capacitance variation range and using sensors positioned farthest from the opening to mitigate desorption effects.

Finally, these considerations allow us to establish a consistent acceleration factor over the 0 to 10% range across different storage conditions, confirming a strong correlation between the model and experimental data. However, we highlighted a disparity between the factors driving acceleration in industry standards and our results. For instance, our experiments show that a 96-hour HAST cycle (85°C/85%RH) is not equivalent to 1000 hours of THS (130°C/85%RH), but rather corresponds to 200 - 300 hours. This underscores the fact that each study on moisture is unique to each product. The advantage of my study is that it gives a more general approach by not focusing in a particular technology but rather on IMD interconnections. Given the similarity of BEOL across various technologies, our findings can be applied to refine technology-specific characterizations, thereby enhancing the accuracy of the extracted acceleration factor.

### 4.5.2 Perspectives

To go deeper, we previously discussed how a focused study on via resistance measurement would be highly interesting. Indeed, with capacitance measurements, it is not possible to distinguish a single degradation mechanism, whereas via resistance measurement could more easily identify the formation of tantalum oxide. In the field of reliability, a 10% resistance variation criterion is often empirically considered for electromigration. Thus, with the assistance of designers, we created a test structure that is suitable for measuring capacitance, leakage current, and via resistance. A schematic is presented in

Figure 4.23.

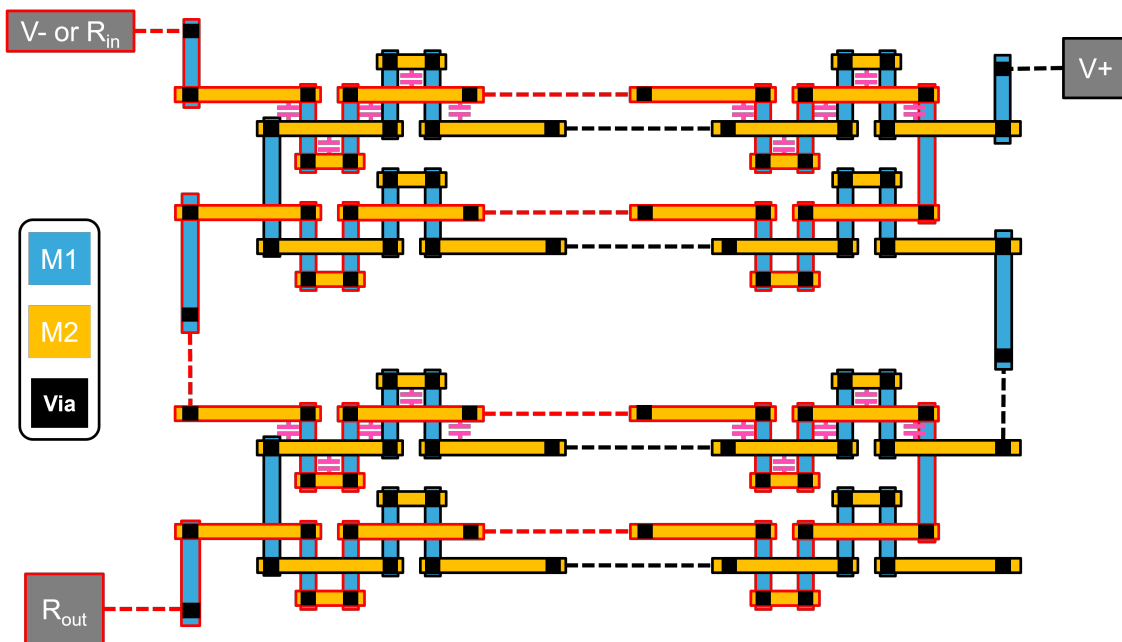


Figure 4.23: Schematic of the next sensors developed

This structure consists of two continuous metallic lines differentiated by red and black borders in the figure (the dashed lines indicate that the elementary structure is repeated). Each resembles a daisy chain, moving up and down between two metal levels. The first level is in blue and the second in yellow in the figure, connected by vias (black squares). Capacitance and leakage current measurements are made via the V- and V+ pads. The measurements for via resistance are taken from the pads ( $R_{in}$ ,  $R_{out}$ ) on a single chain. The previous sensors were on five metal levels. This reduction allows for more precise defect localization within the seal ring.

We implemented this new test structure on a test chip. The dimensions of the sensors are  $50 \times 500 \mu m^2$  and only span 2 metal levels, compared to the typical chip dimensions, which vary. For instance, for this test chip which is for image sensor applications, the dimensions are  $4 \times 4 mm^2$ . The test chip is a multi-layer structure with three types of dielectrics (ULK, Low-k, USG) as presented in Fig 4.24.

With the precision in localization of the sensors, in addition to studying via resistances, we intentionally introduced local defects at the seal ring level during the design step (Fig 4.25). The size of the intentional seal ring openings also varies among the 3 configurations from (5 to 60 microns). This is particularly relevant for this multi-layer structure as we can evaluate for instance the impact of an opening in a Low-k level on a ULK (vertical diffusion). Furthermore, these results will provide a solid database for developing a more advanced simulation model, especially improving from 2D to 3D. From an industrial perspective, these structures also enable quick localization of a seal ring integrity defect after an accelerated storage cycle.

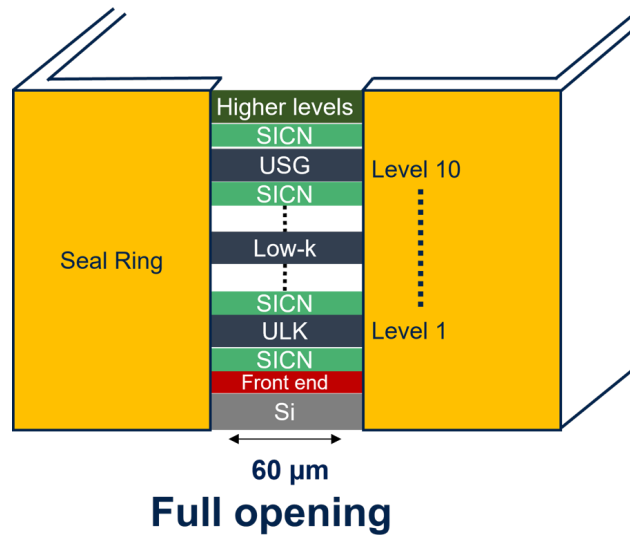


Figure 4.24: 60 μm configurations of intentional opening in the seal ring protection in the next test chip

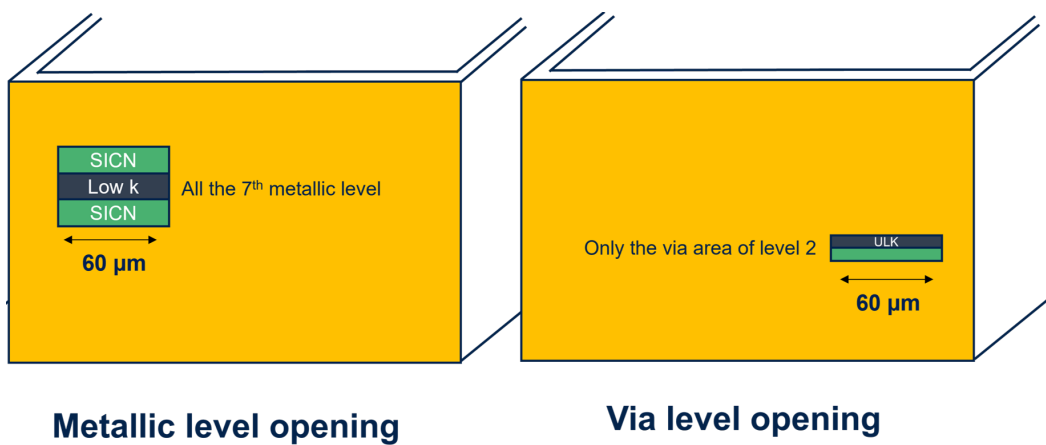


Figure 4.25: 2 Different configurations of intentional opening in the seal ring protection in the next test chip

# General Conclusion

Technological advances and the miniaturization of microelectronics components require materials with increasingly high electrical performance. However, with this improvement comes increased sensitivity to mechanical and environmental degradation. Indeed, dielectrics traditionally used in some technologies, specifically dense silicon dioxide (USG  $SiO_2$ ), have a higher permittivity compared to low-k and ultra-low-k materials, thus exhibiting less electrical efficiency. However, our study demonstrates that by introducing materials with higher electrical performance, the stability concerning environmental degradation of circuits is compromised.

From the work of Cartailier, we know that two distinct behaviors were observed for dielectrics deposited on a simple Si substrate: SiCN and USG, which are hydrophilic, and ULK and Low-k, which are hydrophobic. Regarding moisture diffusion, two categories emerged: dielectrics exhibiting Fickian behavior and others showing non-Fickian behavior (SiCN and Low-k). It was observed that the analytical dual-stage model effectively captures the behavior of the non-Fickian materials tested. Diffusion coefficients ranging from  $10^{-17} m^2.s^{-1}$  to  $10^{-19} m^2.s^{-1}$  were obtained experimentally. The objective was to investigate whether the behavior of these bulk dielectric materials is altered when they are integrated.

To achieve this, we conducted a series of material characterization studies (TEM, EDX, EELS, Tof-SIMS) on a test chip to gather more information for initial simulation. The results revealed that when Low-k or ULK are integrated with a SiCN capping layer, a hydrophilic zone forms at the edges of the Low-k layers. This is explained by the increase in dangling bonds in these zones due to interaction with the different plasmas during assembly steps. Our simulation results corroborate material characterizations by indicating that moisture diffusion occurs much faster at these interfaces compared to the bulk of the dielectrics (by at least 4 order of magnitude).

We have also shown that there are different impacted interfaces. We find firstly the main moisture diffusion path between the Low-k and SiCN layers, highlighted by the deuterium experiment. Then, the oxidation of the TaN/Ta layers indicates that all interfaces between dielectrics and metal lines are also impacted. Finally, moisture diffusion occurs in the bulk of the dielectrics, mainly in the SiCN which has a much higher saturation concentration of moisture than a Low-k or an ULK (Table 1.2 in chapter 1). The diversity of degradation mechanisms and impacted zones identified complicates the study. This diversity was particularly highlighted in the last chapter concerning the acceleration model. The activation energies obtained fluctuated between 0.18 and 0.3 eV, depending

on the storage duration. We interpret these fluctuations as indicative of the diverse mechanisms and types of interactions involved, including weak interactions between materials and moisture, as well as the self-diffusion mechanism of moisture.

In addition, defining a failure criterion posed a challenge. Due to the lack of information on real products, we selected a criterion based on the reversibility of capacity and leakage current degradation. To achieve this, we first characterized the leakage current behavior in dry samples, highlighting the Poole-Frenkel conduction mechanism. Subsequently, for samples saturated with humidity, a modification in the conduction mechanism was observed, suggesting enhanced ionic conduction facilitated by water presence. We hypothesized that humidity could act as both traps and mobile charges due to its diverse interactions with various materials and itself. Moreover, analyzing the leakage current evolution with capacitance variation provided deeper insights into the different degradation stages of moisture-induced integrated structures.

The final step in electrical characterization involved monitoring capacitance and leakage current during drying at 250°C, where we identified a 1% capacitance variation threshold beyond which complete reversibility ceased. By using this reversibility threshold as a failure criterion, we successfully extracted parameters for the acceleration model to determine acceleration factors between different storage conditions.

In the final chapter, after extracting the parameters  $E_a$  and  $n$ , we discover that the empirically accepted industry considerations regarding acceleration factors between ambient, THS (85°C/85%RH), and HAST (130°C/85%RH) storage conditions are inadequate. Indeed, we obtain an acceleration factor ( $AF = 2.5$ ) that is five times lower than expected with the industrial considerations ( $AF = 10$ ) between THS (85°C/85%RH) and HAST (130°C/85%RH). The acceleration factor reflects the degradation mechanisms involved. Therefore, each study has its own acceleration factor, and we cannot make generalizations as a standard test.

However, our study explores the impact of humidity on the Back-End of Line (BEOL), which is common to many technologies for various applications. This extends the potential for utilizing and adapting our study within STMicroelectronics. Indeed, here we chose capacitors because they are sensors that are very easily implementable in a test chip (in addition to being sensitive to the presence of moisture). Therefore, in the case of a study on the impact of humidity on the performance of active parts on a real product, a test chip with these capacitance sensors may be useful if a defect occurs in the BEOL. In that case, by identifying a failure criterion for the product's performance, it would be possible to link it to a criterion of capacity variation. If the corresponding capacity variation criterion is less than 10%, we can consider that the Peck model is a good approximation to obtain the acceleration factor between two storage conditions.

Furthermore, to improve the acceleration model, the test structure proposed in the last chapter (Fig 4.23) is particularly interesting. We showed that it allows us to link capacitance, leakage current, and via resistance measurements through a single test structure. Another advantage is that it enables local measurements at the chip level. In the next test chip developed with the STMicroelectronics design team for the humidity study, intentional defects were introduced into the seal ring. These defects include complete openings (through the thickness), similar to the samples used in this work, as well as highly lo-

calized openings on a single metal layer or via, with varying dimensions. This allows us to obtain data on vertical diffusion between metal levels, which was not considered with a complete opening across all metal levels. These data will be useful for upgrading the simulation model from 2D to 3D and simulate real defects impact. This study is ongoing within the reliability team and will likely be the subject of a future scientific publication. These structures can also be reused to qualify the reliability of new protection technologies, such as the evolution of seal ring structures.

A more research-oriented perspectives regarding the interaction between humidity and dielectrics can be explored. First of all, there is the idea of proposing to modify the nature of plasma treatments. Indeed, among the plasma treatments are  $\text{NH}_3$ ,  $\text{CH}_4$ ,  $\text{He}/\text{H}_2$ , each with its properties. It has been shown that  $\text{NH}_3$  plasmas in [48] which are also used on our samples tend to increase the hydrophilic character of the Low-k edges. On the other hand,  $\text{CH}_4$  treatments tend to densify the edges in contact with the copper lines, limiting the diffusion of moisture. This represents a considerable improvement opportunity. It would be interesting to study structures with these types of plasma treatments to evaluate the impact on the level of interfaces between dielectrics (Low-K) and capping layer (SiCN) and more generally the influence on electrical, material degradations, and acceleration factors. Finally, the last improvement axis that we were able to propose during this study is the development of a 3D simulation model. We have seen that thanks to experimental data on mass variation, the diffusion coefficient, and  $C_{sat}$  have allowed the creation of a coherent 2D model. For a full study with the influence of different interfaces, the development of a 3D model is essential but also challenging for ratio aspects (dimensions). In addition, during this study, we have seen that advanced molecular simulation methods (BET type) could be interesting to understand the molecular interactions between humidity and dielectrics. Especially to test our results over the diversity of interactions between humidity (weak bonds, hydrogen, covalent, oxidation) and the different materials involved.

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## Appendix A

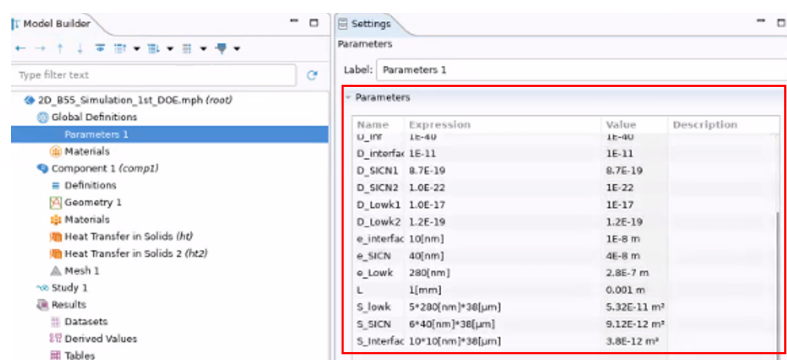
# Comsol simulation methodology

The methodology for simulating moisture diffusion using COMSOL relies on the *Heat Transfer in Solids* module. As explained in the manuscript, an analogy with thermal diffusion is employed to simplify the approach. This analogy is detailed in Table 2.1 on page 49. To address the issue of discontinuities at the interfaces between different layers, the concept of *wetness* has been introduced. The total wetness is defined by the following equation:

$$w_{\text{tot}}(t) = \frac{M_{\text{tot}}(t)}{M_{\text{tot,sat}}} = \frac{\sum_{i=1}^n w_i(t) \cdot M_{\text{sat},i}}{\sum_{i=1}^n M_{\text{sat},i}} = \frac{\sum_{i=1}^n w_i(t) \cdot V_i \cdot C_{\text{sat},i}}{\sum_{i=1}^n V_i \cdot C_{\text{sat},i}} \quad (\text{A.1})$$

where  $V_i$  represents the volume and  $C_{\text{sat},i}$  the saturation concentration for each dielectric layer. The key parameter determined through simulation is the wetness of each layer at any given time (temperature in the Comsol interface).

In the COMSOL interface, the *Heat Transfer in Solids* module is used to solve Fourier's equation, which is treated as analogous to Fick's diffusion equation. The first step is to define all necessary variables in the *Parameters* section, as shown in Fig A.1.



Name	Expression	Value	Description
U_INF	1E-40	1E-40	
D_interfac	1E-11	1E-11	
D_SiCN1	8.7E-19	8.7E-19	
D_SiCN2	1.0E-22	1E-22	
D_Lowk1	1.0E-17	1E-17	
D_Lowk2	1.2E-19	1.2E-19	
e_interfac	10[nm]	1E-8 m	
e_SiCN	40[nm]	4E-8 m	
e_Lowk	280[nm]	2.8E-7 m	
L	1[mm]	0.001 m	
S_lowk	5*280[nm]*38[μm]	5.32E-11 m <sup>2</sup>	
S_SiCN	6*40[nm]*38[μm]	9.12E-12 m <sup>2</sup>	
S_interfac	10*10[nm]*38[μm]	3.8E-12 m <sup>2</sup>	

Figure A.1: Successive leakage current measurements on reference samples

Next, in the *Heat Transfer in Solids* module, diffusion properties are assigned to each material (see Fig A.2). This involves:

1. Replacing the density of each material with 1,
2. Replacing the thermal conductivity with the product of the diffusion coefficient and the saturation concentration, and
3. Replacing the heat capacity with the saturation concentration.

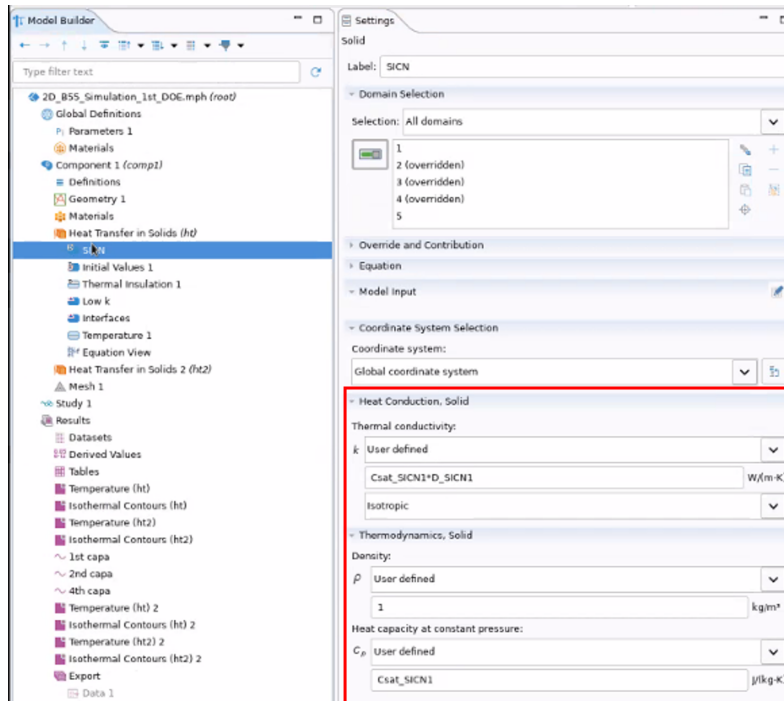


Figure A.2: Successive leakage current measurements on reference samples

The boundary conditions are defined using the *Temperature* function in the *Heat Transfer* module. In this function, regions directly exposed to moisture (such as the seal ring openings in our case) are selected, and a constant temperature (i.e., wetness) of 1 is imposed. Similarly, regions representing impermeable layers (e.g., SiN (top), substrate (bottom) layers) are selected, and their wetness is set to 0.

Once these steps are completed and the mesh parameters are adjusted to suit the geometry, the simulation can be executed. Subsequently, using the integration function in COMSOL, the temperature is integrated across the thickness of each layer in the y-direction, as well as over the dimensions of the sensor in the x-direction, positioned at 40 from the seal ring opening. By summing the temperature variations across all layers, the global wetness evolution is determined, ranging from 0 to 1.