Advanced DC and RF electrical characterisation of passive and active components in 28nm-FDSOI technology at cryogenic temperature

Quentin Berlingard

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Caractérisation électrique avancée DC et RF de composants passifs et actifs en technologie 28nm-FDSOI à température cryogénique

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Présentée par :

Quentin BERLINGARD

Direction de thèse :

Mikaël CASSE DIRECTEUR DE RECHERCHE, CEA - Centre de Grenoble	Directeur de thèse
Maryline BAWEDIN MCF, GRENOBLE INP - UGA	Co-encadrante de thèse
José LUGO ALVAREZ CEA-Leti	Co-encadrant de thèse

Rapporteurs :

Bogdan CRETU
MAITRE DE CONFERENCES, ENSICAEN
Jean-Michel SALLESE
ASSISTANT PROFESSOR, Ecole Polytechnique Fédérale de Lausanne

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Mikaël CASSE, DIRECTEUR DE RECHERCHE, CEA - Centre de Grenoble	Directeur de thèse
Bogdan CRETU, MAITRE DE CONFERENCES, ENSICAEN	Rapporteur
Jean-Michel SALLESE, ASSISTANT PROFESSOR, Ecole Polytechnique Fédérale de Lausanne	Rapporteur
Philippe FERRARI, PROFESSEUR DES UNIVERSITES, Université Grenoble Alpes	Examinateur
Valeriya KILCHYTSKA, INGENIEURE DE RECHERCHE, Université Catholique de Louvain	Examinatrice
Sylvain BOURDEL, PROFESSEUR DES UNIVERSITES, Grenoble INP - UGA	Président

Invités :

Vincent PUYAL
INGENIEUR CHERCHEUR, CEA-Leti

Abstract

The operation of electronic circuits and devices at cryogenic temperatures is generating increasing interest in fields such as aerospace and high-performance computing, where it is well established that electronic device performance significantly improves at lower temperatures. Recently, the rise of quantum computers, which integrate quantum bits, or qubits, along with their readout and control electronics, has further heightened the appeal of cryogenic electronics, leading to a remarkable resurgence in this area. Electronic circuits capable of operating at these extreme temperatures and reaching radio frequencies (RF) are proliferating. However, there remains a significant lack of reliable models to accurately describe passive and active devices under these conditions, particularly in the RF frequency range.

Among the technologies being explored, FD-SOI stands out for its high-performance passive circuits and transistors, known for their low power consumption, adaptability to RF applications, and fine control of threshold voltage through a back-gate. While many characterization studies at low temperatures have been conducted in direct current (DC), RF characterization remains scarce. However, studying devices in RF provides a complementary perspective, offering deeper insights into the physical effects specific to cryogenic temperatures.

In this thesis, we propose a comprehensive approach to the characterization and modeling of passive and active components using 28nm FD-SOI technology, over a temperature range from ambient to cryogenic conditions down to 4.2K. This approach includes the development of a dedicated measurement setup and a methodology for RF characterization at low temperatures, followed by a detailed analysis of devices operating in cryogenic conditions. RF measurements will complement existing DC data, with the aim of enhancing our understanding of the physical phenomena at low temperatures and developing accurate models. These characterizations will then be used to optimize the performance of electronic circuits designed to operate in cryogenic environments.

Résumé

La possibilité de faire fonctionner les circuits électroniques à température cryogénique suscite un intérêt croissant dans des domaines tels que l'aérospatial et le calcul haute performance, car il est bien établi que les performances des dispositifs électroniques s'améliorent considérablement à basse température. Récemment, l'essor du développement des ordinateurs quantiques, qui intègrent des bits quantiques, ou qubits, ainsi que leur électronique de lecture et de contrôle, a amplifié cet attrait pour l'électronique cryogénique, entraînant un regain d'intérêt marqué. La démonstration de circuits électroniques capables de fonctionner à ces températures extrêmes et d'atteindre des fréquences radio (RF) se multiplie. Cependant, il subsiste un manque notable de modèles précis pour décrire le fonctionnement des dispositifs passifs et actifs dans ces conditions, en particulier dans la gamme des fréquences RF.

Parmi les technologies étudiées, la technologie FD-SOI se distingue par les excellentes performances de ses circuits passifs ainsi que par ses transistors, reconnus pour leur faible consommation d'énergie, leur adaptabilité aux applications RF, et leur capacité à contrôler finement la tension de seuil via une grille arrière. Alors que de nombreuses études de caractérisation à basse température ont été réalisées en courant continu (DC), les travaux en radiofréquence (RF) restent rares. Or, l'étude des dispositifs en régime RF offre un angle complémentaire, qui permet d'approfondir la compréhension des effets physiques spécifiques aux basses températures.

Dans le cadre de cette thèse, nous proposons une approche complète de caractérisation et de modélisation des composants passifs et actifs en technologie FD-SOI 28nm, sur une plage de températures allant de la température ambiante jusqu'à 4,2K. Cette démarche inclut le développement d'un banc de mesure adapté et l'élaboration d'une méthodologie de caractérisation RF à basse température, suivis de la caractérisation détaillée des dispositifs dans des conditions cryogéniques. Les mesures RF viendront enrichir les données existantes en DC, avec pour objectif d'améliorer la compréhension des phénomènes physiques en jeu à basse température et de développer des modèles précis. Ces caractérisations sont ensuite exploitées pour optimiser les performances des circuits électroniques destinés à fonctionner dans des environnements cryogéniques.

List of main Acronyms and symbols

RF	Radio-Frequency
SOI	Silicon On Insulator
FD-SOI	Fully Depleted Silicon On Insulator
DC	Direct Current
LNA	Low Noise Amplifier
CMOS	Complementary Metal Oxide Semi-conductor
MOSFET	Metal Oxide Semi-conductor Field Effect Transistor
BOX	Buried OXide
UTBB	Ultra-Thin Body and BOX
I_D	Drain current
V_{GS}	Gate-Source Voltage
V_{DS}	Drain-Source Voltage
V_{BG}	Back-gate Voltage
V_G	Gate Voltage
V_{Th}	Threshold Voltage
V_{FB}	Flat-Band voltage
W	transistor gate width
L	transistor gate length
A	Cross-sectional area of a vertical section of the transitor channel
$f(E)$	Fermi-Dirac function
E	Energy
E_g	Bandgap energy
E_f	Fermi energy
T	Temperature
k_b	Boltzmann's constant
SS	Subthreshold Slope
n	Electron concentration

D_n	Diffusion coefficient for electrons
C_D	Depletion capacitance
C_{ox}	Oxide capacitance
C_{box}	Buried oxide capacitance
C_{Si}	Silicon capacitance
C_{co}	Body to front channel coupling capacitance
C_{inv}	Inversion capacitance
C_{gg}	Total gate capacitance
C_{gd}	Gate to drain capacitance
C_{gb}	Gate to back-gate capacitance
C_{gb}	Gate to back-gate capacitance
R_g	Gate access resistance
R_{ds}	Drain and source access resistance
g_{ds}	Drain to source conductance
g_m	Transconductance
f_t	Transition frequency
f_{max}	Maximum oscillation frequency
ZTC	Zero Temperature Coefficient
Φ_F	Fermi potential
n_i	Intrinsic carrier concentration
q	Elementary electron charge
μ	Mobility
μ_0	Low field mobility
μ_{ph}	Phonon scattering mobility
μ_C	Coulomb scattering mobility
μ_{nd}	Neutral defects scattering mobility
Q_i	Inversion charge
N_A	Acceptor concentration
N_A^-	Ionized dopant concentration
E_A	Acceptor energy level
EKV	Enz-Krummenacher-Vittoz
LF	Low Frequency
HBT	Heterojunction bipolar transistor
NF	Noise Figure
VNA	Vector Network Analyzer

DUT	Device Under Test
U	Mason gain
H_{21}	Current gain
Z	Impedance
Y	Admittance
G	Transistor gate
D	Transistor drain
S	Transistor source
BG	Transistor back-gate
GSG	Ground Signal Ground
SOLT	Short Open Load Thru
ISS	Impedance Standard Substrate
SNR	Signal to Noise Ratio
STD	Standard substrate
HR	High-resistivity substrate
TR	Trap-Rich substrate
Sub	Substrat

Author scientific contributions

- Publications :

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Table of Contents

Introduction

This chapter provides an introduction to the context of this PhD and highlights the significance of characterizing electronic devices at cryogenic temperatures. It discusses various applications where cryogenic operation is critical, as well as the local research interests in Grenoble. The objectives of this thesis are then outlined. Lastly, the structure of the manuscript is presented, with a brief description of each chapter.

Context

Applications

Nowadays, numerous applications requiring electronics at low and very low temperatures are emerging. Among these applications are space technology, high-performance computing and quantum computing. In 2023 IRDS roadmap [DS23], cryogenic electronics is defined by all devices and circuits operating below -150◦ C or 123.15K. These devices and circuit are made in different material such as insulators, conductors, semiconductors, superconductors, or topological materials. The following subsection details the need for cryogenic electronics in these fields.

Spatial

The increasing density of satellites in geostationary orbits necessitates the use of spatial and spectral filtering, as well as signal amplification [Soa+00]. Spatial filtering, facilitated by the antenna, helps reduce interference from other satellites and terrestrial sources. The implementation of multiple high-temperature-superconducting front-end filters, which are very narrow, allows for the creation of a frequency-agile system with minimal noise addition compared to systems without filtering. This spectral filtering is crucial to protect amplifiers from large out-of-band signals that could cause compression, and to prevent spurious signals in the desired band, which can arise from the mixing of these

signals.

These measures are particularly important in the challenging environment of space, where electronics, including sensors and communication circuits, often operate at extremely low temperatures, potentially below 100K. Such conditions necessitate cryogenic cooling, especially in applications like infrared sensors and bio-molecular detectors, to increase sensitivity by reducing thermal noise contributions. This is where the role of the Low Noise Amplifier (LNA) becomes critical. The LNA must provide adequate amplification without saturating subsequent stages and should introduce minimal external noise. Additionally, the LNA must maintain linearity to handle high-power interferences from wireless interfaces. For communication systems, the LNA serves the essential function of amplifying weak signals received by an antenna, strategically positioned close to the antenna to minimize feed line losses [Mud+21].

The significance of these technologies extends beyond communication systems into the realm of radio astronomy, where the pursuit of ultra-low-noise reception is of paramount importance. Receiver noise often constitutes a major part of the total system noise in these applications. The development of devices achieving the lowest noise temperatures across various frequency bands is well-documented, covering a wide range of technologies such as vacuum tubes, crystal mixers, tunnel diode amplifiers, parametric amplifiers, solid-state masers, mixers, GaAs field-effect transistors (FETs), heterostructure field-effect transistors (HFETs), and hot electron bolometers (HEBs) [WP66].

A key factor linking these devices is the use of cryogenic temperatures, which are required for the operation of mixers and HEBs. Furthermore, many other devices are also cooled to cryogenic temperatures not only to enhance their performance—often through improved electron transport properties—but also to mitigate the thermal noise generated by parasitic elements. Thus, whether in communication systems or radio astronomy, the integration of advanced filtering techniques and cryogenic technologies is vital for achieving optimal signal clarity and system performance.

High-Performance Computing

Transistor scaling has historically driven exponential gains in the performance and energy efficiency of integrated circuits, powering the evolution from mainframes to personal computers, and later to mobile and cloud computing. However, as computational demands surge with the rise of hyperscaling and emerging workloads like large-scale deep neural network training, further energy-efficient scaling of CMOS technology presents a significant challenge. These tasks involve massive data movement and require both high performance and reduced power consumption, particularly in the context of High-Performance Computing (HPC).

Cryogenic CMOS, which operates at liquid nitrogen temperatures (77 K), offers a promising solution to these challenges. Operating at cryogenic temperatures reduces dynamic energy consumption

to the attojoule (aJ) level, potentially overcoming the limitations of traditional transistor scaling. Additionally, cryogenic conditions enable transistors with a steep subthreshold slope (SS), as SS scales linearly with temperature. This improvement allows for more energy-efficient logic switching, which is critical for sustaining the high computational power required by HPC systems. As a result, cryo-CMOS could play a crucial role in enhancing the energy efficiency and performance of future HPC architectures [DCR22].

Quantum computing

Notwithstanding the considerable advancements in classical computing, which have facilitated the resolution of increasingly complex problems through hardware enhancements, certain specific challenges remain exceptionally difficult to address with precision. These problems often require an incalculable expenditure of time or resources to obtain accurate results. However, quantum computers hold the promise of addressing these challenges by leveraging quantum phenomena to perform computations that are infeasible for classical systems [Le 23; Aru+19].

In a classical computer, computations are executed by transferring bits into a central processing unit (CPU), where logical operations are implemented in physical circuitry. The fundamental role of the CPU is to produce a specified output bit string for each possible input bit string, thereby executing a desired logical operation. Due to the digital nature of this circuitry, the processor generates precisely one output bit string for each input bit string, with this input-to-output mapping being predetermined by the hardware. This mapping may involve a subset of input bits determining the logical operation applied to the remaining bits.

Transitioning to quantum computing, the fundamental unit of data remains represented by physical entities, but the key difference lies in the memory register being a quantum state [Le 23; Cha21]. The primary component of a quantum register is the quantum bit, or qubit. Similar to a classical bit, a qubit can exist in two distinct states: zero (ground) and one (excited). However, unlike a classical bit, a qubit can exist in a superposition of both zero and one states simultaneously. The state of a qubit is mathematically described as a two-dimensional complex state vector of unit amplitude:

$$|\Psi\rangle = \alpha_0|0\rangle + \alpha_1|1\rangle \tag{1}$$

Here, $|0\rangle$ and $|1\rangle$ are the computational-basis vectors representing the zero and one states, respectively, and the complex coefficients α_0 and α_1 are known as probability amplitudes. These amplitudes indicate the likelihood of measuring the qubit in the respective state: $P(|0\rangle) = |\alpha_0|^2$ and $P(|1\rangle) = |\alpha_1|^2$. This formulation uses Dirac notation, where the states are represented as kets.

The advent of quantum information processing systems has spurred the development of new mi-

crowave technologies, leading to the creation of innovative devices and techniques that operate in previously unexplored regimes [BSR21]. The quantization of microwave energy enables resonant interactions between microwave photons and other quantum objects, such as the qubits that constitute the fundamental units of quantum computers.

To minimize thermal noise, readout circuits are often operated at low temperatures and positioned close to the qubits, thereby simplifying the overall architecture of quantum computers [Das+20]. This setup allows the use of superconducting interconnects, which offer optimal thermal isolation with minimal losses. One example of qubit readout system is presented in figure 1:

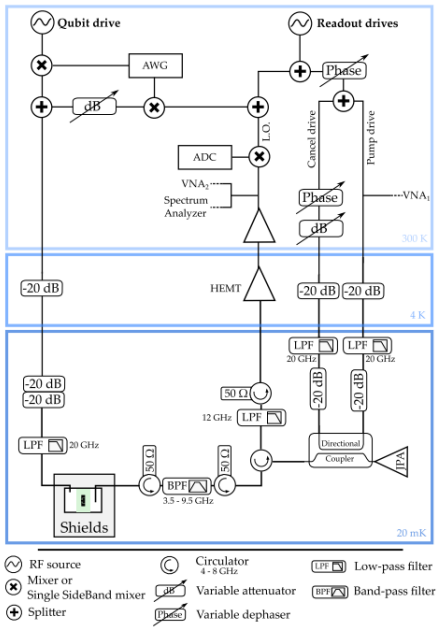

Figure 1: Schematic of superconducting qubit and its readout system. Taken from [Das+20]

As illustrated in Figure 1, qubit and readout pulses are transmitted through the same input line. The signal subsequently passes through a series of circulators and a directional coupler before being amplified by a Josephson Parametric Amplifier. Following this, the signal undergoes additional amplification stages and is down-converted to DC voltages using a mixer. Finally, the signal is digitized with an ADC and digitally integrated. This meticulous process ensures the precise readout of qubit states, which is crucial for the functioning of quantum computers.

Local interest in Grenoble

The doctoral program is situated within a stimulating research environment in Grenoble, where a multitude of endeavors pertaining to electronic devices for cryogenic temperatures are underway.

Many doctoral dissertations in the quantum field are conducted on the subject of quantum computing at CEA-Leti but in our case we focused on the qubit readout system and the conventional electronics around qubits as other PhD:

- Loïck Le Guevel's PhD [Le 23]. This PhD thesis investigates the application of advanced CMOS technologies in quantum computing. The objective of the research presented in this thesis was to investigate and assess the feasibility of utilizing the industry-standard CMOS FD-SOI 28 nm technology in quantum computing applications at cryogenic temperatures.

- Mathild Ouvrier-Buffet's PhD [Ouv23]. This PhD thesis studies a architecture for multi-qubits reflectometry readout modeling and design of a multitone frequency synthesis.

- Quentin Schmidt's PhD on integrated electronic systems for scalable readout of quantum bits [Sch+24]. This thesis main aim consists in exploring integrated electronic architectures for reading arrays of quantum bits.

All these works requires precise electrical characterization down to cryogenic temperature to design the qubits read out system. At CEA-Leti and CROMA laboratories, a lot of DC cryogenic characterizations have been performed in the past. Reference [BG17] thus provides a good summary of the physics and performance of semiconductor devices at cryogenic temperatures. This study elucidates the impact of temperature and device architecture on the different scattering mechanisms involved in carrier transport in the channel of transistors (e.g. phonon, Coulomb, neutral defects, and surface roughness scattering). An overview of the influence of temperature on other main electrical parameters of MOSFETs, nanowire FETs, and tunnel FETs, such as threshold voltage, subthreshold swing, leakage, and driving currents, is provided. FDSOI CMOS technology, which has been highly developed in Grenoble area, has also been extensively studied down to cryogenic temperatures. Reference [Cas+22] presents the status of FDSOI transistors electrical characterization for operation at extremely low temperatures. The paper emphasizes the singular transport and thermal effects occurring at low temperatures. Additionally, the physical and analytical models associated with various characteristic electrical parameters are presented, establishing a foundation for cryogenic compact models. These many works have been widely published since the early 2000's [BG01; CG22].

CEA-Leti and CROMA laboratory both possess considerable expertise in the field of radio frequency (RF) characterization at room temperature. The objective of this PhD is to leverage expertise in cryogenic and RF technologies to enable the characterization of RF phenomena at cryogenic temperatures. This PhD focused on FDSOI technology because many studies ([Le 23; Gal+18; Cas+22] demonstrate that this technology is a good candidate for cryogenic electronic as shown in the following section.

Purpose of this thesis

In recent times, a considerable amount of cryogenic DC characterizations has been conducted, and a number of DC models have emerged that are validated down to cryogenic temperatures [Cas+22; EBJ20]. However, compact models, at the basis of Process Design Kits (or PDKs) for any industrial technology platform, are still unavailable in the sub-100K temperature domain. The development of such models requires extensive DC and RF electrical characterization at cryogenic temperature. The advent of quantum computing has urged the necessity for electronic circuits that operate at cryogenic temperatures, especially at 4K, and at radio frequencies (typically in the 1-20GHz bandwidth). Some attempts to circumvent the lack of proper cryo-PDKs have been proposed to design cryogenic circuits [Bec+18; Bri+23], but they also relies on electrical data measured at the targeted temperature of operation.

In practice, designers are basing their designs on RF models that are valid at room temperature. The objective of this PhD research is to comprehensively characterize and model passive and active components across a temperature range extending from room temperature to 4K. The objectives are twofold:

- to use RF as an additional tool to investigate and gain deeper insight into the physical effects emerging at low temperatures in FDSOI transistors.
- to develop models in order to dimension and optimize cryo circuits.

Thesis structure

This thesis is organized in a systematic and logical manner, with each chapter building on the preceding one to provide a comprehensive understanding of cryogenic characterization and modeling of passive and active devices.

In Chapter 1, the state of the art of electrical characterization of CMOS devices at cryogenic temperature is presented. This section begins with a description of the 28nm FD-SOI technology used and highlights its relevance for low-temperature circuits. Then, a review of low-temperature DC characterization is provided, covering the main known physical effects at low temperatures, such as dopant freeze-out, threshold voltage variation, and mobility enhancement. Finally, this chapter gives an overview of RF characterization at low temperatures, including both passive and active devices, as well as RF circuit optimization.

Chapter 2 details the methodology used for these characterizations. It starts with the RF methodology and explains how to extract device parameters from RF measurements. The equivalent models

of the various measured devices are presented, along with the calibration and de-embedding methods. Next, the setup for performing cryogenic RF measurements is introduced, followed by a detailed discussion of the various constraints and challenges posed by RF measurements at cryogenic temperatures.

Chapter 3 presents the characterization of inductors from ambient temperature down to cryogenic temperatures. Two types of inductors are measured and compared. The first type includes inductors with a metal shield to isolate the inductance from the influence of the substrate. The second type consists of inductors directly on the substrate, allowing us to study the behavior of the substrate at low temperatures. The goal of this section is to examine whether the substrate exhibits significant losses at cryogenic temperatures, or whether, unlike at ambient temperature, the substrate no longer presents an issue.

Chapter 4 describes the characterization of transistors fabricated in28nm FD-SOI technology. This chapter is dedicated to the electrostatic characterization of the transistor, starting with the extraction of the threshold voltage and the impact of the back-gate voltage through RF capacitance measurements. A detailed study of the transistor's capacitances follows, highlighting the freeze-out of the back-gate and its impact on the capacitance values. This capacitance study is then used to measure channel mobility across all temperatures by adapting the CV-split method.

Chapter 5 continues with RF characterization of the transistor by detailing its performance from ambient to cryogenic temperatures. First, the various RF figures of merit for the transistor are presented. Then, the self-heating effect is analyzed in detail using RF methods and compared to current DC methods.

Finally, Chapter 6 applies the previous characterizations to the study of an RF circuit: a low-noise amplifier (LNA). This circuit is optimized using the back-gate voltage to compensate for the threshold voltage shift at low temperatures. The gain and noise measurements of the LNA are presented and explained in light of the previous characterizations.

The thesis ends with a conclusion, outlining future prospects for further research.

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Chapter 1

State-of-the-art DC and RF devices characterization at cryogenic temperature

Contents

This chapter presents the state of the art about characterization at cryogenic temperature. It begins with a short description of the technology characterized in this manuscript, the 28 FD-SOI. Then it presents a status about the DC characterization at cryogenic temperature and explains different low temperature phenomena useful for the understanding of the manuscript. Finally, it concludes with the state of the field of RF characterization at cryogenic temperature.

1.1 28 nm Fully Depleted Silicon On Insulator (FD-SOI)

FD-SOI technology is a planar architecture that incorporates four effective terminals: source, drain, front-gate, and back-gate. The back-gate is electrically isolated from the conduction channel by a buried oxide (BOX) layer, as illustrated in the TEM image of the transistor shown in Figure 1.1:

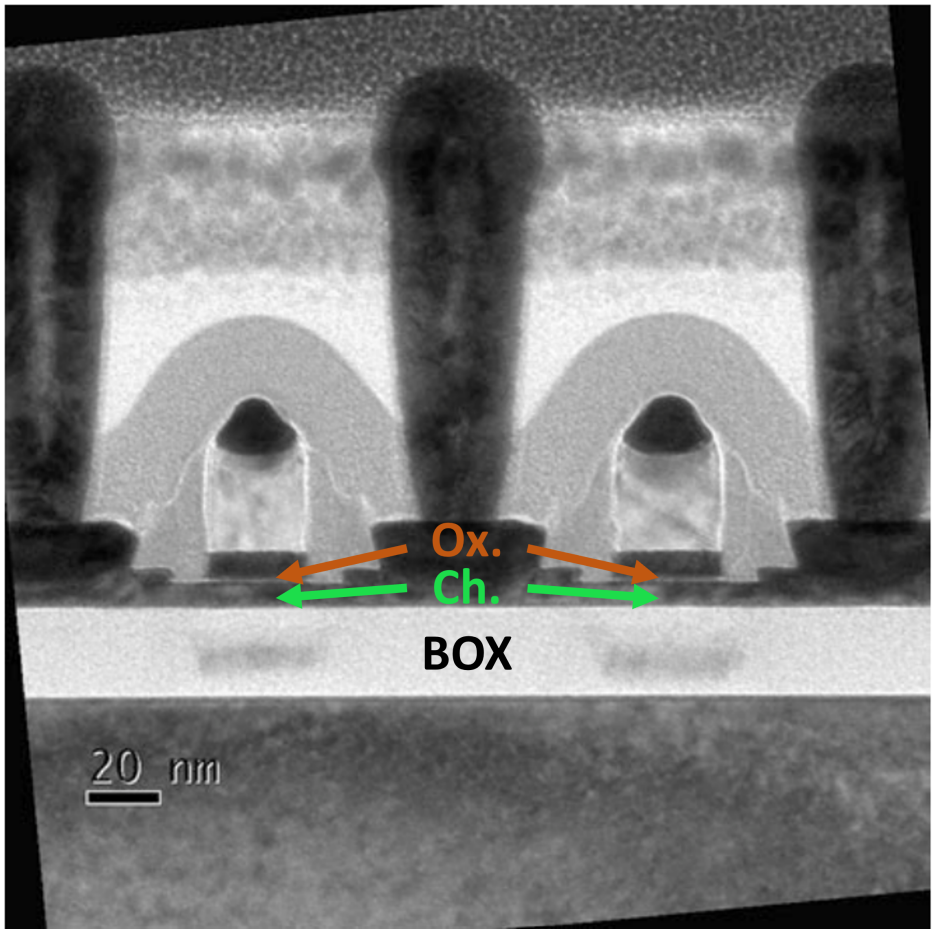

Figure 1.1: TEM image of an FD-SOI transistor. The conduction channel is located between the front and back gates, separated by the buried oxide (BOX). Taken from [CDC20].

This technology, referred to as ultra-thin body and BOX (UTBB) FD-SOI CMOS, is fabricated in the 28nm node with an high-k dielectric with an 1.1 nm equivalent oxide thickness for the front-gate

oxide and with an ultra-thin (7 nm) conduction film positioned atop a 25 nm BOX insulation layer. The thin silicon film ensures the channel is fully depleted, and as a result, pocket implants in the source and drain regions are unnecessary, leading to improved analog and RF performance. The use of the BOX layer allows the transistor to achieve full dielectric isolation, which eliminates the need for channel doping. Furthermore, the thin BOX enables electrostatic control of the front-side transistor through the back-gate, providing the ability to modulate the threshold voltage by adjusting the back-gate voltage as described later. Compared to conventional bulk technologies, FD-SOI demonstrates improved short-channel effects, lower electric fields, higher transconductance, and near-ideal subthreshold slope characteristics.

Figure 1.2 presents a cross-sectional view of an FD-SOI transistor, highlighting the fourth terminal (pink contact on the right). The back-gate is controlled by the front body bias pad located on the right side of the schematic. This device can be considered a dual-gate transistor, with the front gate acting similarly to bulk technologies, and the back-side gate providing an additional control on the channel. However, the transconductance of the back-side gate is typically about ten times smaller than that of the front gate, due to the significant thickness difference between the front and back oxides.

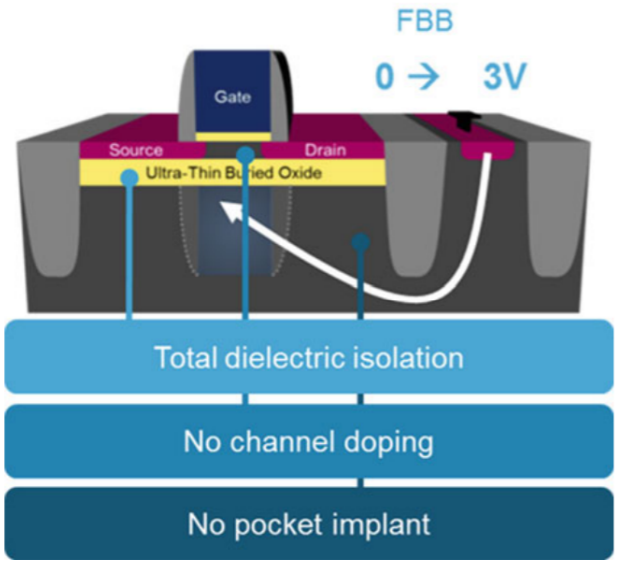

Figure 1.2: Cross-sectional view of an FD-SOI transistor, showing the fourth terminal (back-gate) [CDC20].

The application of back-gate bias voltage serves two main purposes: First, forward body bias (FBB) is achieved by applying a voltage lower than VDD for PMOS transistors, or higher than GND for NMOS transistors, reducing the threshold voltage. Second, reverse body bias (RBB) increases the threshold voltage by applying a voltage higher than VDD for PMOS or lower than GND for NMOS transistors

(see Figure 1.3, Left). Modulating the threshold voltage enhances the transistor speed and increases its transconductance g_m, without introducing significant mismatch.

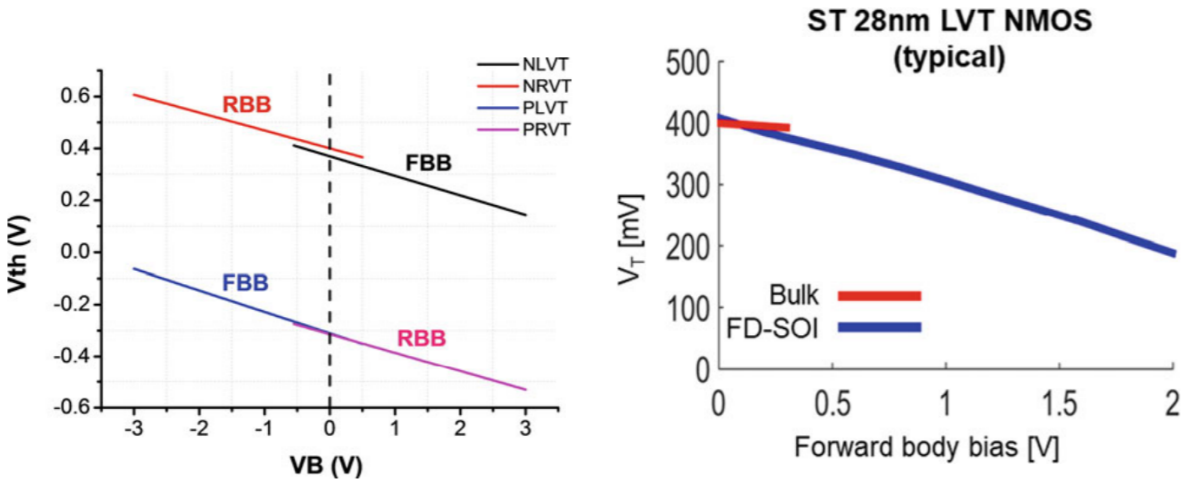

Figure 1.3: (Left) Threshold voltage variation with back-bias voltage. (Right) Comparison of threshold voltages in FD-SOI and bulk technologies [CDC20].

As demonstrated in Figure 1.3 (Right) and discussed in [CDC20], FD-SOI technology provides more efficient threshold voltage control through forward body bias compared to bulk technologies. Moreover, the FD-SOI stack allows for the integration of high-performance passive components, such as inductors with high-quality factors and transmission lines with low loss, formed from the metal layers positioned above the active silicon regions.

One of the major advantages of FD-SOI technology is its suitability for low-power applications. Its ability to operate at reduced voltages while maintaining high performance makes it ideal for energy-sensitive devices such as mobile phones, wearables, and IoT systems. Furthermore, the unique back-bias capability enables dynamic threshold voltage tuning, allowing further optimization of energy efficiency by reducing both active and standby power consumption without compromising processing speed.

FD-SOI technology also holds significant potential for cryogenic applications, as shown in [Boh+16; Paz+20]. Fully depleted SOI architectures exhibit excellent performance at cryogenic temperatures, making them suitable for quantum processor integration. This technology is especially advantageous due to its low power consumption, reduced leakage current, and proven reliability in cryogenic environments, which are critical for the stable operation of quantum systems [Cha19]. The ability to apply back-bias voltage at 4K allows for continued threshold voltage control, which is crucial for optimizing performance and power consumption in cryogenic conditions [Gal+18].

1.2 Cryogenic electronic state of the art

1.2.1 DC transistor characterization at cryogenic temperature

Figure 1.4 presents the state of the art of DC characterization at cryogenic temperature for SOI and bulk technology. Before the years 2010s some papers about cryogenic characterization has been published such as [BG01; Akt+07; Fen+04] and the identified applications were space and electronic with very low noise requirement as application. However in the 2010s, with the development of quantum computing, the cryo-electronic regain an interest. Different technology has been study such as CMOS bulk and FD-SOI with different gate length. As an example in 2016, [Boh+16] reports the first cryogenic characterization of 28nm FD-SOI technology and demonstrates that a reduced temperature operation largely improves CMOS device performance and that the back-bias allows to adjust the threshold voltage at room temperature and at cryogenic temperature. Figure 1.4 presents the state of the art until 24 years.

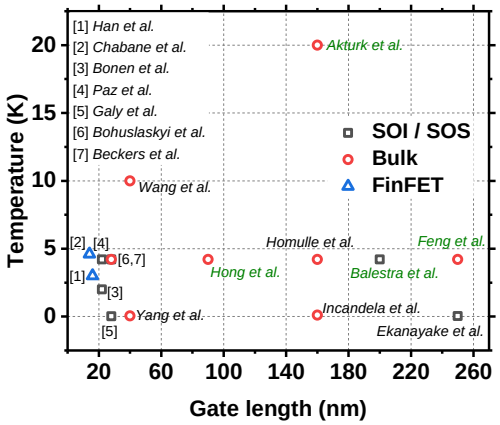

Figure 1.4: Overview of the state of the art of DC cryogenic characterization of different process. Reference [Fen+04; BG01; Eka+10; Akt+10; Hon+08; Inc+18; Wan+20; BJE18; Bec+19; Paz+20; Gal+18; Bon+22; Yan+20; Hom+17; Han+21; Cha+21a] are presented. The reference with the name in green as been published before the 2010s.

Many DC characterization has been performed from room temperature down to 4.2K and below on advanced CMOS technology transistors (bulk, FDSOI, finFETs,..). The drain current as a function of the gate voltage is plotted in figure 1.5 for FD-SOI technology:

These curve are plotted for FD-SOI technology but the following observations remains the same for other technologies (bulk, finFET, ...). Different temperature effects are seen and will be explained in the following section :

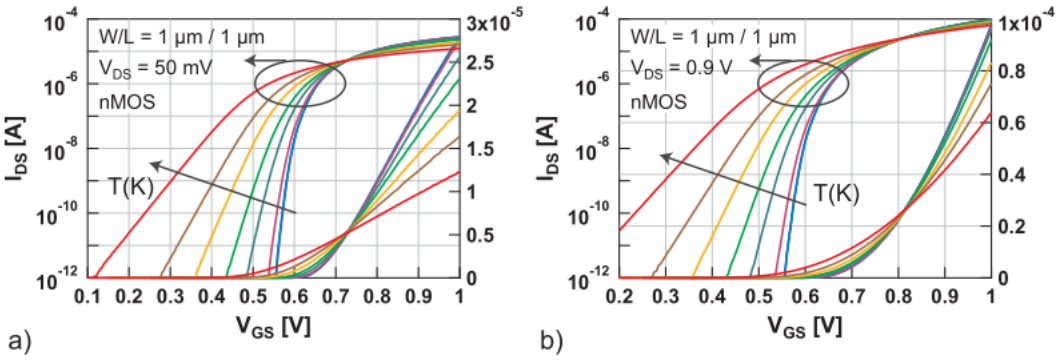

Figure 1.5: Drain current as a front gate voltage function for (a) low or (b) high drain voltage in 28 FD-SOI technology taken from [BJE18]. The temperature are the following: red= 300 K, brown= 210 K, orange= 160 K, light green= 110 K, dark green= 77 K, purple= 36 K, light blue= 10 K, and dark blue= 4.2 K.

- The subthreshold slope is sharper at cryogenic temperature (see subsection 1.2.1.2).
- The threshold voltage shift at higher front gate voltage when the temperature decreases (see subsection 1.2.1.3).
- The drain current is higher at high V_{gs} when the temperature decreases due to the mobility increase at cryogenic temperature (see subsection 1.2.1.4).
- All the temperature curves cross in one point, the Zero Temperature Coefficient (ZTC). At this point, the temperature does not modify the current value (see subsection 1.2.1.5).

A detailed investigation of the cryo-phenomena is required to fully understand the DC and RF characterization down to 4.2K. This section will discussed the temperature dependence of Fermi-Dirac distribution, subthreshold slope, threshold voltage, mobility, dopant freeze out and modeling.

1.2.1.1 Fermi-Dirac distribution

The Fermi function, denoted by the symbol $f(E)$, is a mathematical expression that describes the probability of an electron occupying a specific energy state at a given temperature. The expression is given in the reference [Lim15; Sim87] by :

$$f(E) = \frac{1}{e^{(E-E_F)/k_B T} + 1} \tag{1.1}$$

where E_F is the Fermi energy, k_B is the Boltzmann constant, and T is the absolute temperature. This function plays a crucial role in understanding the behavior of electrons in solids, particularly in

semiconductors and metals. At absolute zero temperature, all states with energies less than E_F are occupied, and all states with energies greater than E_F are unoccupied. As the temperature increases, the distribution of occupied states broadens, allowing some electrons to occupy higher energy states.

As shown in figure 1.6, when the temperature decreases, the Fermi-Dirac distribution becomes sharper. At absolute zero temperature, the Fermi function is one until a certain energy level, from where the probability will immediately decrease to zero.

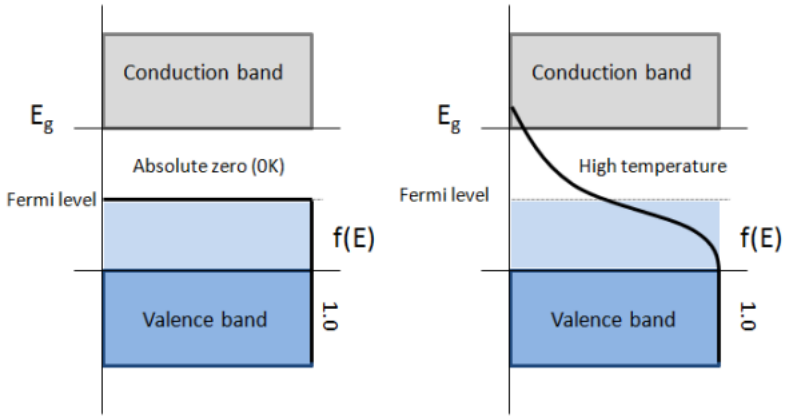

Figure 1.6: The Fermi function f(E) within a semiconductor band structure plot. Taken from [Lim15].

1.2.1.2 Subthreshold slope

The subthreshold slope is defined as the inverse of the slope of the ID(VG) curve in the subthreshold regime, presented on a semilogarithmic plot [Col04].

$$SS = \frac{dV_G}{d(log(I_d))} \tag{1.2}$$

According to [Col04], the subthreshold current of an MOS transistor is independent of drain voltage, which suggests it is due to a diffusion mechanism rather than to a drift mechanism and is expressed as :

$$I_d = qAD_n \frac{n(0) - n(L)}{L} \tag{1.3}$$

where A is the cross-sectional area of a vertical section of the channel region through which the electrons flow, D_n is the diffusion coefficient for electrons, and $n(0)$ and $n(L)$ are the electron concentrations at the edge of the source and drain junction, respectively.

Therefore, in the case of bulk transistor, the subthreshold slope is expressed as [Col04] :

$$SS = \frac{k_b T}{q} ln(10)(1 + \frac{C_D}{C_{ox}}) \tag{1.4}$$

Where k_b is the boltzmann constant, T the temperature, C_D the depletion capacitance and C_{ox} the oxide capacitance.

In this case of a FDSOI transistor, the subthreshold slope is expressed by [Col04] :

$$SS = \frac{k_b T}{q} ln(10)(1 + \frac{1}{C_{ox}} \frac{C_{Si} C_{box}}{C_{Si} + C_{box}} \tag{1.5}$$

where C_{ox} is the front oxide capacitance, C_{Si} is the silicon capacitance and C_{box} is the buried oxide capacitance. Due to the different oxide and silicon thickness, in a FDSOI transistor, we have $C_{box} << C_{ox}$ and $C_{box} << C_{Si}$ and it results in :

$$SS = \frac{k_b T}{q} ln(10) \tag{1.6}$$

The equations 1.4 and 1.6 show that the subthreshold slope is improved (lower) in a FDSOI device than in a bulk one. This reduction is due to the thin film and the buried oxide. The excellent value of the subthreshold slope in FD-SOI devices allows one to use smaller values of threshold voltage than in bulk devices without increasing the leakage current at a front gate voltage equal to 0. As a result, better speed performances can be obtained, especially at low supply voltage.

With these equations, we can conclude that the subthreshold slope decrease linearly when the temperature decreases. However, it has been demonstrated in [Cas+22; Ghi+20] that the subthreshold slope saturates at very low temperatures (typically below 100K). This behavior is effectively explained by considering a two-dimensional density of states, $N(E, \Delta E)$, with a disorder-induced exponential band tail, where ΔE represents the characteristic energy width of the band tail extension [Ghi+20; Oka+23].

1.2.1.3 Threshold voltage

The threshold voltage is a key parameter in designing circuits with CMOS transistors. Physically, this voltage corresponds to the transition from weak inversion, where the inversion charge is exponentially dependent on the gate voltage V_{GS}, to the strong inversion regime, where the inversion charge varies linearly with V_{GS} [FT11].

In a bulk n-channel MOSFET, the threshold voltage is expressed by [SK07]:

$$V_{TH} = V_{FB} + 2\Phi_F + \frac{qN_a x_{dmax}}{C_{ox}} \tag{1.7}$$

where V_{FB} is the flatband voltage, equal to $\Phi_{MS} - \frac{Q_{ox}}{C_{ox}}$, Φ_F is the Fermi potential, equal to $\frac{k_b T}{q} \ln\left(\frac{N_a}{n_i}\right)$, and x_{dmax} is the maximum depletion width, which is equal to $\sqrt{\frac{4\varepsilon_{si}\Phi_F}{qN_a}}$.

In an FDSOI device, the threshold voltage equation is different due to the thin silicon and to the buried oxide. The threshold voltage can be obtained by solving the Poisson equation and using the

depletion approximation : $\frac{d^2\Phi}{dx^2} = \frac{qN_a}{\epsilon_{Si}}$ [Col04]. As demonstrated in [FT11; CG22], the threshold voltage is expressed by :

$$V_{th} = V_{sth} + \frac{q \cdot n_{th}}{C_{ox}} + \left(\frac{C_{co}}{C_{ox}}\right)(V_{sth} - V_b) \tag{1.8}$$

with

$$V_{sth} = V_0 + \frac{k_B T}{q} \cdot \ln\left(e^{n_{th}/(k_B T \cdot A_{2D})} - 1\right) \tag{1.9}$$

being a threshold surface potential associated with a given constant inversion charge density n_{th} (here $10^{10}\,\mathrm{cm}^{-2}$) and

$$C_{co} = \frac{C_{ox} \cdot C_{Si}}{C_{ox} + C_{Si}} \tag{1.10}$$

being the body to front channel coupling capacitance.

With these two equations, it can be conclued that in both cases bulk or FDSOI, the threshold voltage increases when the temperature decreases. In the case of bulk MOSFET, this increase is due to the Fermi level temperature dependence of the body (as shown in equation 1.7 and in [TN09]).In the case of FDSOI MOSFET, the V_{th} increase is link to the threshold surface potential variation due to the Fermi-Dirac distribution [CG22]. However, as presented in many papers, for bulk and FDSOI technologies [Cas+22; BJE18; Cha+21b; Bec+19] the threshold voltage saturates when the temperature is below a given temperature. The figure 1.7 taken from [Bec+19] presents the threshold voltage shift ($V_{th} - V_{th,300K}$) as a temperature function for different FDSOI transistors.

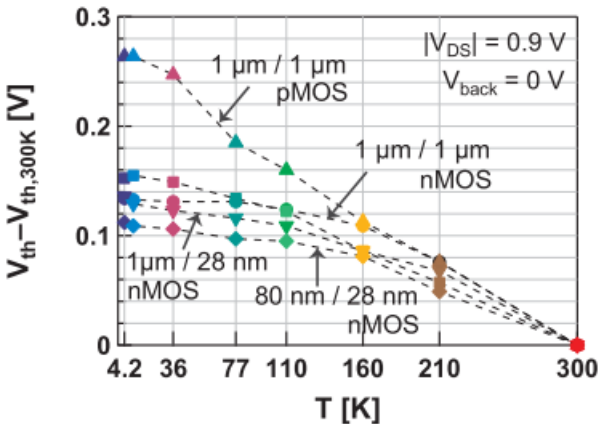

Figure 1.7: Threshold voltage shift with respect to room temperature for FDSOI devices. Taken from [Bec+19].

In this case of the NMOS device, the temperature dependence (including the saturation) of the threshold voltage is well captured by the 1D Poisson-Schrödinger equation and is mainly linked to

the charge distribution temperature variation [Cas+22; Oka+23]. However, PMOS threshold voltage does not saturate at cryogenic temperatures and shows a different slope compared to the NMOS. This phenomenon is not well captured by the 1D Poisson-Schrödinger equation and has been previously observed in earlier studies [Bec+20; Cas+22] and remains challenging to fully explain. In [EBJ20], an approach is suggested to fit the PMOS threshold voltage by incorporating an effective temperature dependence in the oxide capacitance. However, this hypothesis is contradicted by capacitance measurements presented in [Cas+22], where the oxide capacitance remains constant across varying temperatures. In [Cas+22], the observed threshold voltage variation is instead attributed to the saturation of the subthreshold slope at very low temperatures (typically below 100K). This behavior is effectively explained by considering a two-dimensional density of states, $N(E, \Delta E)$, with a disorder-induced exponential band tail, where ΔE represents the characteristic energy width of the band tail extension [Ghi+20].

The undesirable increase of the threshold voltage in MOSFETs as temperature reduces, is one the main motivator for developing FDSOI technology at cryogenic temperature due to its threshold voltage control through back-bias.

1.2.1.4 Mobility

The electron transport affects the drain current characteristic. As demonstrated in [BG17; Shi+15], a decrease in temperature results in an increase in electron mobility. Figure 1.8 depicts the mobility as an inversion charge function for varying temperatures, highlighting the main scattering mechanisms:

The main scattering mechanisms between room and very low temperature are shown in figure 1.8. As demonstrated in [Shi+15], the low field mobility can be written as:

$$\frac{1}{\mu_0} = \frac{1}{300}\left(\frac{T}{\mu_{ph}}\right) + \left(\frac{1}{T}\right)\left(\frac{300}{\mu_C}\right) + \frac{1}{\mu_{nd}} \tag{1.11}$$

where μ_{ph}, μ_C, and μ_{nd} are the phonon, Coulomb, and neutral defects scattering amplitudes, respectively.

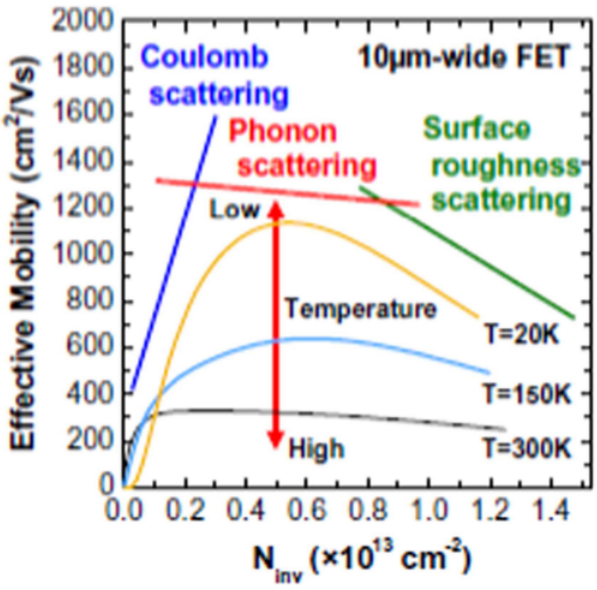

Figure 1.8: Main scattering mechanisms as a function of temperature and inversion charge for MOSFETs. Taken from [BG17].

Phonon scattering significantly affects mobility at elevated temperatures, while surface roughness scattering becomes a major factor at high transverse electric fields or inversion charges, independent of temperature. Coulomb scattering, on the other hand, can become the dominant mechanism at low electric fields or charge densities, especially at low temperatures or when a high density of impurities or parasitic charges is present. Neutral defects can also significantly impact MOSFETs, particularly in devices with very short channels. For long-channel devices with thick gate oxides, mobility is primarily determined by phonon scattering, following an approximate relationship of $\mu_0 \approx 300 \times \mu_{\text{ph}}/T$. However, as the gate oxide thickness decreases, the mobility deviates from this inverse temperature trend, indicating an increasing influence of Coulomb scattering. This shift underscores the importance of various scattering mechanisms in shaping the electrical characteristics of MOSFETs, especially as device dimensions shrink.

Figure 1.9 presents the low field mobilty as a temperature function for FD-SOI devices with different gate length.

Indeed, figure 1.9 shows typical variations of the low field mobility with temperature as obtained on FD-SOI MOSFETs with various channel lengths. For a long channel, phonon scattering dominates at high temperature leading to an increase of mobility with reducing temperature. However, at small gate lengths, the mobility remains constant with temperature. This is due to the main transport mechanisms in these short channel devices, which are limited by impurity scattering (neutral and/or Coulomb) at the edges of the channel and likely induced by source–drain implantation.

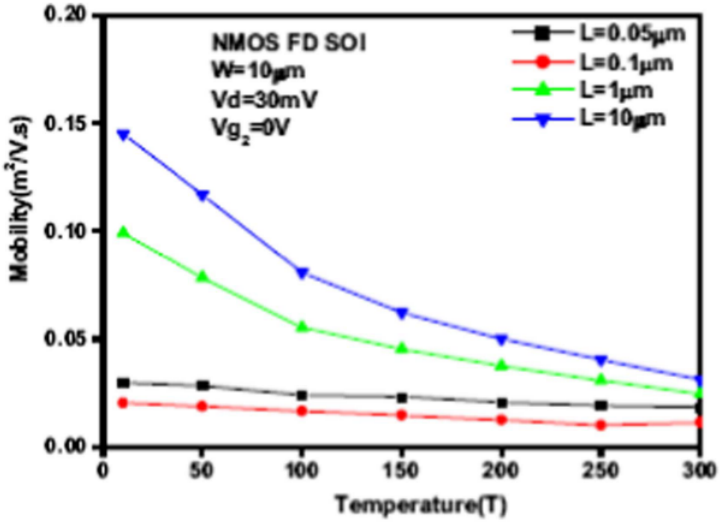

Figure 1.9: Low field mobility versus T and gate length in FD-SOI devices. Taken from [BG17].

Figure 1.9 shows the typical variations in low-field mobility with temperature for FD-SOI MOSFETs with different channel lengths. In devices with long channels, phonon scattering dominates at high temperatures, leading to an increase in mobility as the temperature decreases. In contrast, for devices with small gate lengths, the mobility remains relatively unchanged across temperatures. This behavior is due to the primary transport mechanisms in these short-channel devices, where impurity scattering—either neutral or Coulomb in nature—at the channel edges, possibly exacerbated by source-drain implantation, becomes the limiting factor.

In conclusion, the results demonstrate that as temperature decreases, there is an increase in mobility, which in turn induces a faster current increase in the $I_d(V_g)$ curves.

1.2.1.5 Zero Temperature Coefficient

On different technologies (bulk, FD-SOI, FinFET), when looking at the I_dV_g curve, there is one gate voltage where the drain current is independent of the temperature [SRD24; BJE18; Bec+19; Cas+22]. This point is called the Zero Temperature Coefficient point (ZTC). The figure 1.10 (taken from [SRD24]) present the I_dV_g curve for different temperature for a finFET device.

On this curve the ZTC point is close to 0.6V and depend on the technology, the drain voltage and transistor dimension [Cat+22].

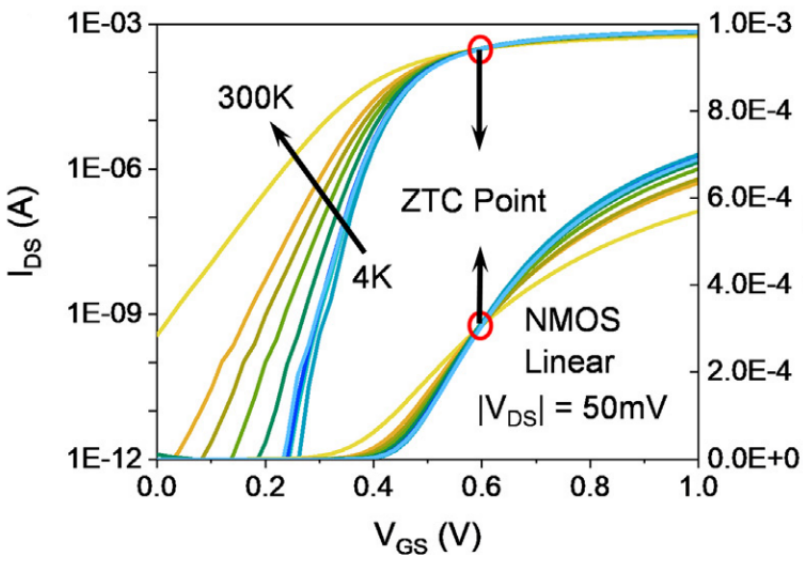

Figure 1.10: NMOS transistor drain current as a gate voltage function in linear regions. The technology used is the 14nm FinFET. Taken from [SRD24].

Many works [Bow+16; Mar+16; FA01] explain this point as a compensation between the threshold voltage shift and the higher mobility at cryogenic temperature. However another explanation proposed by [Cat+22] focused on the carrier population in FD-SOI technology. This paper demonstrate that ZTC also appears on the front gate to channel capacitance. It shows that a temperature-independent capacitance implies that both the inversion capacitance ($C_{inv} = \frac{dQ_i}{dE_F} = C_q \cdot f(E_F, T)$ with C_q the quantum capacitance. Consequently, $f(E_F, T)$ are temperature-independent. This is only true if the ratio of the Fermi energy to the Boltzmann constant and temperature remains constant. In the following, we assume that $\frac{E_f}{k_b T} = \alpha$ and α is a constant. It can thus be postulated that the existence of the ZTC point is a consequence of the compensation between the increase in the Fermi level and the decrease in temperature. In light of these assumptions and reference [Cat+22], the gate voltage at which the ZTC phenomenon emerges can be expressed as follows:

$$V_{G,ZTC}(C,T) = V_{FB} + \alpha \cdot \frac{k_B T}{q} + V_0 + \frac{Q_i(\alpha \cdot k_B T/q, T)}{C_{ox}} + \frac{C_{co} \cdot (\alpha \cdot k_B T/q + V_0 - V_b)}{C_{ox}}. \quad (1.12)$$

The existence of the ZTC point implies $\frac{\partial V_{G,ZTC}}{\partial T} = 0$, which, when substituted into equation 1.12, yields:

$$\alpha \cdot (C_{co} + C_{ox}) + C_q \cdot \ln(1 + e^{\alpha}) = 0 \quad (1.13)$$

Once the value of the constant α is known through numerical resolution of equation 1.13, it is a

straightforward process to calculate the value of $V_{G,ZTC}$ using equation 1.12.

In light of the fact that the Zero Temperature Coefficient (ZTC) also manifests in the $I_d(V_g)$ characteristics (as illustrated in [Bec+19]), the role of carrier mobility is observed. The equation describing mobility is provided in equation 1.11. In his study, E. Catapano demonstrated that a ZTC point in the $I_d(V_G)$ curves exists only if the mobility of charge carriers varies inversely with temperature, i.e. considering only Coulomb scattering. He observed that the origin of the ZTC point in the $I_d(V_G)$ curves is consistent with the capacitance one.

However, a more comprehensive scenario was examined, taking into account the effects of scattering from both phonons and neutral defects. This analysis identified a region with minimal temperature dependence for both current and transconductance, though these regions occurred at different gate voltages. The findings indicated that while a true ZTC point can be observed in capacitance curves, it is more accurate to describe a region with minimal temperature sensitivity for current and transconductance characteristics.

1.2.1.6 Dopant freeze out

In silicon at thermal equilibrium, dopant atoms will become deionized at sufficiently low (cryogenic) temperatures. The specific temperature at which this occurs depends on the doping concentration, which ranges from 10^{12} to 10^{18} cm^3.

For a p-type silicon, an acceptor dopant atom is theoretically ionized when its acceptor energy level, E_A, is occupied by an electron. Thus, the ionized dopant concentration, N_A^-, can be expressed as follows:

$$N_A^- = \frac{N_A}{1 + g_A \exp\left(\frac{E_A - E_{Fn}}{k_b T}\right)} \tag{1.14}$$

where E_A is the acceptor energy level, E_{Fn} is the Fermi level, k_b is the Boltzmann constant, T is the absolute temperature and g_A is the degeneracy factor.

The electrical neutrality at every point in the semiconductor requires that the sum of positive charges, whether mobile or fixed, equals the sum of negative charges, whether mobile or fixed. This condition is represented by the following equation:

$$p + N_D^+ = n + N_A^- \tag{1.15}$$

In this case of a p-type silicon, it gives:

$$N_v \exp\left(\frac{E_v - E_F}{k_b T}\right) = N_c \exp\left(\frac{E_F - E_c}{k_b T}\right) + \frac{N_A}{1 + g_A \exp\left(\frac{E_A - E_{Fn}}{k_b T}\right)} \tag{1.16}$$

Figure 1.11 illustrates the graphical solution of this equation at different temperature. The intersection of the curves p et $n + N_A^-$ determines the value of the Fermi level E_F. Knowing this value allows us to deduce the equilibrium concentrations n and p from figure 1.11

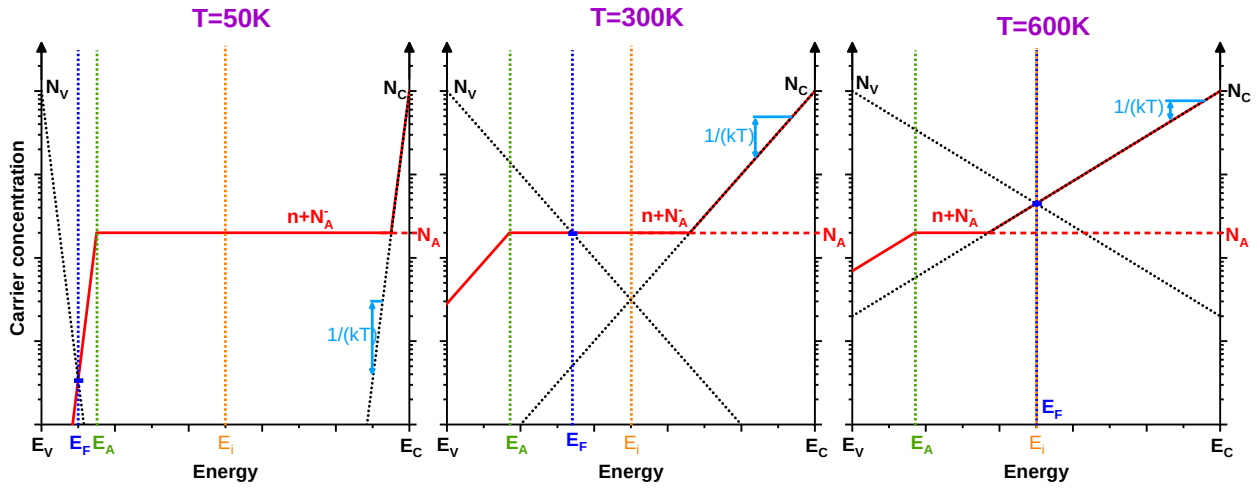

Figure 1.11: Graphical resolution in E_f of equation 1.16 for different temperature.

At low temperatures, the thermal energy may be insufficient to ionize all the impurities: $N_A^- < N_A$. The concentration of majority carriers is then less than the dominant doping concentration ($p < N_A$ for p-type). Consequently, the concentration of active dopants decreases significantly. This effect is call freeze out.

The freeze out applied in bulk MOSFET. As demonstrated in [BAL87], an abrupt change in the characteristics of the $I_d(V_g)$ curves is observed for intermediate values of drain voltage at very low temperatures. This phenomenon is primarily attributed to the floating substrate potential, which arises due to substrate freeze-out under the depletion region. The freeze-out effect causes a significant reduction in free carrier concentration within the substrate, leading to a noticeable impact on the device's electrical behavior at cryogenic temperatures.

However in FDSOI technology [CG22; Bec+19], the doping concentration is rather low ($10^{15} cm^{-3}$) compared to the inversion charge density. In the flatband condition and at 4.2 K, approximately all dopants will be frozen-out. The E_F position at 4.2 K lies under E_A, leading to freeze-out. Nonetheless, the front-gate voltage will ionize the impurities under the surface of the front-gate, when E_A bends under E_F near the surface of the front-gate [BAL87]. According to [EBJ20], freeze out is becoming important for T below 100K and can cause important kinks in the output characteristic of SOI devices at high VDS voltage. Because of the lower supply voltage, these kinks have not been observed for the 28nm FDSOI devices presented at least within the nominal operating voltage range. Freeze-out has finally little impact on the dc characteristics of MOSFETs in advanced technologies.

It is important to note that, in both bulk and FDSOI technologies, the source and drain regions are not affected by freeze-out, as they are highly doped (degenerate doping levels exceeding $10^{20}\,\mathrm{cm}^{-3}$).

1.2.1.7 Compact modeling at cryogenic temperature

To support cryogenic applications, researchers and designers have aimed to improve the models available in process design kits (PDKs) provided by foundries. However, these advancements are fundamentally linked to the complexities of cryo-physics presented before. Compared to room temperature operation, the understanding and modeling of MOSFET behavior at low and cryogenic temperatures remains less developed, primarily due to the complex physical phenomena that occur at these extreme conditions. Some models have been adapted to operate at cryogenic temperatures:

- Building on the PSP and NMOS11 models developed by NXP [LWG08; LSK03], *Incandela et al.* proposed a DC compact model for bulk CMOS technologies that is valid down to 4.2K [Inc+18]. By accounting for mobility variation and impact ionization, they successfully modeled measurements with less than 10% error. This model has been effectively utilized to simulate the performance of a low-noise amplifier (LNA) and a ring oscillator.

- Two models have been developed based on the BSIM framework [Liu+98], as reported in [Akt+10; Sin+22]. *Akturk et al.* employed Verilog-A to modify the temperature dependencies of several key parameters, including the threshold voltage, bulk mobility, the smoothness parameter for the linear-to-saturation transition, and the ideality factor n. Using this approach, they successfully modeled DC measurements from room temperature down to 20K. Similarly, in [Sin+22], the BSIM model was adapted by modifying the temperature dependence of the subthreshold swing, threshold voltage, and effective mobility, allowing accurate modeling of DC measurements from room temperature down to 10K.

- Using the EKV model [EV06], *Enz et al.* successfully modeled fully depleted SOI (FDSOI) and bulk transistors down to 4.2K by adjusting the subthreshold slope and threshold voltage [EBJ20; Bec+19; BJE18].

Despite these advancements, most circuits designed for cryogenic temperatures have not undergone simulation-based verification, as is typically done for circuits operating at room temperature. This is largely due to the ongoing development of compact models, which are not yet integrated into the process design kits (PDKs) of most advanced CMOS technologies.

1.2.2 RF characterization at cryogenic temperature

Recent works have been published on RF characterization of transistors at cryogenic temperature. Most of these characterization are driven by the qubit application and focus on the readout circuit and their needs (such as low losses RF filter and low noise amplifier due to very weak signal [Mud+21]). This section presents a review of electrical characterization of passive and active devices in RF domain, before dealing with full circuit measurement.

1.2.2.1 Passive devices at cryogenic temperature

Most of the work focus on CMOS at cryogenic temperature, few studies can be found about passive device. Passive device play a crucial role in many different application. they are needed in filter or in LNA architecture device which are two function needed in quantum readout system [Pat21]. Therefore, their analyses at cryogenic temperature is a necessary step for cryogenic circuit design.

Nowadays, there is only a few of RF passive device characterization at cryogenic temperature. In is PhD manuscript [Hom19], *H. Homulle* presents measurement of several commercial capacitor and resistor to be integrated in a printed circuit board (PCB) design. In [Kru+06] *J. Krupka* focused on the silicon electric characteristics to use this selicon as a substrate for passive devices. In [Pat+20] *B. Patra* characterizes a MoM capacitor, a transformer with high-inductance multi-turn windings. All the device are fabricated in 40-nm bulk CMOS technology with an ultra-thick metal layer to reduce the metal track losses.

In these studies, there are two main effect that impact the passive device characterization, the metal track resistivity and the substrate freeze out.

Metal track resistivity

The metal resistivity linearly increases with the temperature between 50K and 300K because the electron mobility increases as presented for a metal in [Mat79]. Below 50K, the decrease in resistivity saturates because electron-phonon scattering has been fully suppressed [VF74]. This metal resistivity induce lower losses in the passive device metal and it results in higher quality factor for inductor and capacitance as shown in [Pat+20].

Substrate freeze out

As presented before, the silicon freeze at cryogenic temperature resulting in a lower active dopant concentration and in a higher resistivity. The device is on a silicon subtrate which is doped at $10^{15} cm^{-3}$. Therefore under a given temperature the substrate freeze leading to an higher resistivity and a lower losses as presented in figure 1.12 taken from [Kru+06].

This freeze out is benefit for the passive device because it reduces the device losses and it results in a higher quality factor under the freeze out temperature [Kru+06; Pat+20].

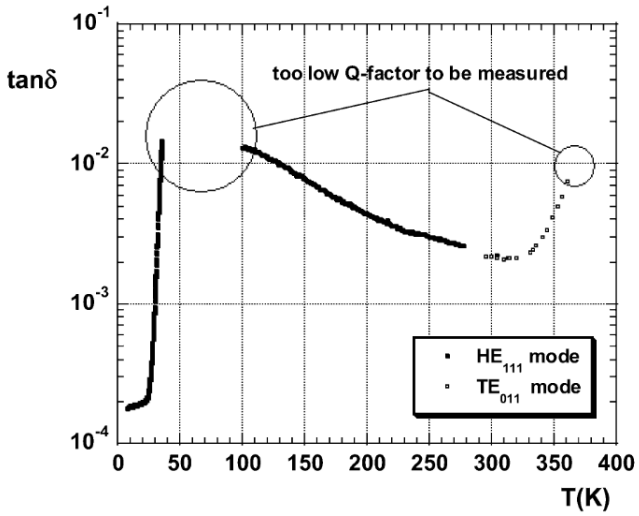

Figure 1.12: Effective dielectric loss tangent versus temperature for silicon sample. Taken from [Kru+06]

At cryogenic temperatures, passive components generally demonstrate an enhanced quality factor (approximately $2\times$ improvement between room temperature and 4.2 K), which is primarily attributed to the reduced metal resistivity and the decrease in substrate losses.

The passive device performance increase is benefit for RF circuit however, these variation modified the input or output adaptation and should be considered during the circuit design.

1.2.2.2 RF characterization of transistors

As previously outlined in section 1.2.1, a substantial amount of DC characterization has been conducted on CMOS down to cryogenic temperatures. Nevertheless, as the frequency needed to control qubits is closed to 10 GHz, RF cryogenic characterization is of paramount importance for the design and enhancement of the performance of electronic circuits at cryogenic temperatures. In this regard, some research has been devoted to the investigation of RF cryogenic temperatures on different technologies (Bulk, FD-SOI and FinFET) [Nys+20; Tan+22; Bon+22]. We give here a review of transistor performance and behaviour in RF domain at low temperature.

Transistor parameters

the RF measurements allows to extract different transistor parameters:

- the total capacitance between the gate and the ground (called C_{gg}). This capacitance is mainly dependent of the transistor dimension and remains constant with the temperature [Nys+20; Cha+21b]

- the access resistance (R_{ds} and R_g) is reduced at cryogenic temperature due to the mobility enhancement [Nys+20; Cha+21b].
- the drain to source conductance (g_{ds}) and the transconductance (g_m), which increase at low temperature due to the carrier mobility increase which impact the mobilty in the channel but also the access resistance [Nys+20; Cha+21b].

RF figure of merit

One of the main parameter to compare the RF transistor performance are the two RF figures of merit: the transition frequency and the maximum oscillation frequency (f_t and f_{max}) explain in chapter 2. The figure 1.13 presents the figure of merit values for the actual literature:

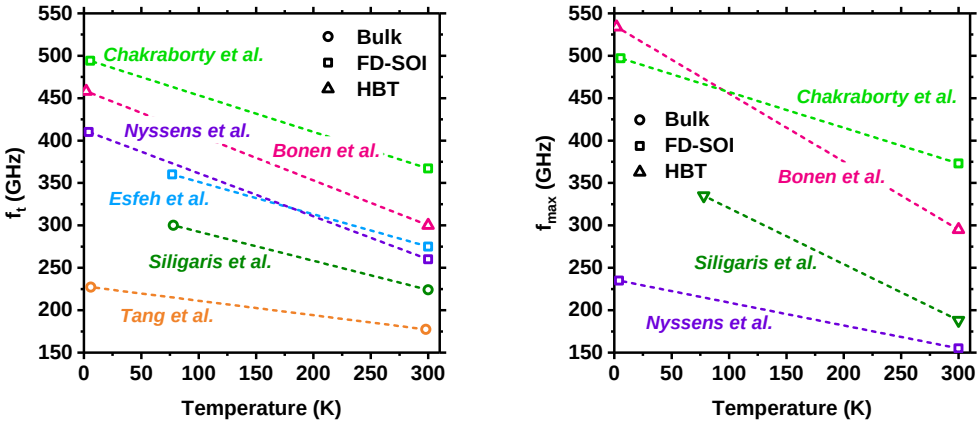

Figure 1.13: (Left) transition frequency and (Right) maximum oscillation frequency at room and cryogenic temperature for different technologies. The data are extracted from [Cha+21b; Nys+20; Tan+22; Bon+22; Kaz+19; Sil+06]

In all technologies, it is mentioned that at low temperature, transconductance increases, access resistances decrease and the capacitance values remain stable. It enables the enhancement of f_t and f_{max} for the different technologies study. Between room temperature and 4.2K the rise in the figure of merit is observed to be within the range of 20 to 30 $\%$.

RF characterization at cryogenic temperatures has been conducted on a range of technologies, with a particular emphasis on the assessment of transistor performance and the extraction of pertinent parameters. The objective of these characterizations is to provide the fundamental principles that inform the design of circuits operating at cryogenic temperatures. However for FD-SOI technologies, the impact of back-gate voltage on RF measurement has not been explored and remain one of the key feature of FD-SOI tehcnology for cryogenic temperature. Moreover, to our knowledge, there is actually no RF compact model that has been provided.

1.2.2.3 Cryogenic circuit characterization

The study and understanding of transistor characterization at cryogenic temperature has for goal to develop high-performance circuits working at cryogenic temperature for spatial of quantum computing application. In the realm of quantum computing, various cryogenic circuit architectures currently in use, particularly by industrial leaders such as Google [Aru+19], IBM [CDG21; Rie23] or Intel [Int19].

For instance, Google's Sycamore quantum processor utilizes cryogenic microwave circuits, which include circulators and low-noise amplifiers (LNAs) and filters to manage signal routing and amplification without introducing significant noise or heat to ensure high-fidelity qubit operations.

IBM's Quantum System One similarly relies on dilution refrigeration and advanced cryogenic circuits to cool superconducting qubits. IBM has developed high-density cryogenic multiplexing schemes, such as cryogenic field-programmable gate arrays (FPGAs), which allow for more efficient control of qubits while operating at cryogenic temperatures. These circuits significantly reduce the thermal load, allowing IBM systems to scale towards larger qubit arrays.

Intel's "Horse Ridge" cryogenic control chip is designed to operate at 4 Kelvin and integrates control functions that traditionally occur at room temperature, such as qubit manipulation and readout. This chip leverages Intel's expertise in semiconductor manufacturing to create high-density, low-power cryogenic control electronics, which reduce the number of wires needed between qubits and control electronics. By bringing control electronics closer to the quantum processor, Intel aims to minimize the thermal load and reduce latency in qubit operations.

Additionally, innovations in cryogenic CMOS circuits, as explored by various research groups and companies [Le 23], are showing promise for integration within control electronics directly at cryogenic levels, reducing latency and power dissipation. These technologies are essential for scaling up quantum processors and overcoming bottlenecks in heat management, qubit control, and readout fidelity.

For this section, we focus on the LNA because it is one of the key elements for reading the ultraweak signal emits by the qubit. The LNa should have a good gain whitout introducing to much noise [Pat+18].

Low Noise Amplifier characterization

In the processing of ultraweak electromagnetic signals, such as those observed in radio astronomy or the readout signal of a qubit, conventional systems operating at room temperature often exhibit noise levels that are inadequate for the intended application. To meet the requisite specifications of such systems, Low-Noise Amplifiers (LNAs) are cooled to cryogenic temperatures, thereby reducing the noise in the electronic circuitry. This underscores the importance of the LNAs in these applications, particularly in the context of ultraweak signals, where noise addition can be a significant concern.

Nevertheless, the high-fidelity readout operations require low noise amplifiers (LNAs) with a noise equivalent temperature of a few Kelvins [1]. Contrary to common cryoIII-V compound LNAs that

present sufficient noise performance, many reported recent cryo-CMOS LNA works [1-12] attempt to demonstrate such high performance. Thus, this is one of the greatest challenges on the way to the fully integrated CMOS readout circuitry.

Actually some cryogenic LNA are made with III-V material due to noise performance. In [HTL24], *Heinz et al.* demonstrate a LNA working from room temperature down to 10K and it achieve a 0.04 K of noise temperature with 31 dB of gain in a useful band between 6 and 9 GHz. To compensate for the temperature variation they have study different possibility like integrating inductor or serie resistance to reduce the noise value. However, the main problem of III-V material is the fact that it can not be fully integrated with silicon spin qubit or silicon CMOS readout circuit.

Other LNA on silicon technologies has been designed and study such as [Cag+23; Lin+22]. *Caglar et al.* use a 28nm CMOS bulk technology to design their LNA. In this case they use ultra-low V_{th} devices to avoid operating the transistors in the subthreshold region at 4.2K due to the threshold voltage shift. With this technique they reached a 0.5 dB noise figure and a 40 dB of gain at 4K. *Lin et al.* use 22nm FD-SOI technology to design their LNA. In this case, they have access to the back-gate so they can compensate the threshold voltage shift by using the back-bias property. They reached a 35 dB of gain for a noise figure between 0.07 and 0.3dB.

In conclusion, some LNA have already been characterized from room temperature down to cryogenic temperatures. The circuit exhibits optimal performance at cryogenic temperatures, particularly in regard to noise reduction due to reduction of thermal noise. Nevertheless, the advancement of these circuits can be enhanced through the utilisation of radio frequency (RF) characterisation and modelling techniques.

1.3 Conclusion

In conclusion, this chapter has highlighted the various cryogenic phenomena that influence the behavior of electronic devices operating at low temperatures. While DC characterization models have advanced to provide relatively accurate predictions from room to cryogenic temperatures, RF characterization remains an area where significant progress is needed to develop reliable and compact models. The complementary insights gained from RF measurements are essential, particularly as they provide additional perspectives beyond those obtained from DC analysis.

For effective circuit design at cryogenic temperatures, it is crucial to thoroughly characterize both active and passive components, given their intertwined roles in RF cryogenic circuits. However, circuit designers currently lack the ability to accurately simulate circuits at these temperatures, which forces them to adopt alternative strategies, such as using FD-SOI back-gate control to mitigate threshold voltage shifts.

In this PhD work, we have chosen the 28nm FD-SOI technology due to its notable advantages, including low power consumption, reduced leakage current, and proven reliability in cryogenic environments. The ability to apply back-bias voltage at 4K offers continued control over the threshold voltage, which is useful for optimizing both performance and energy efficiency in cryogenic conditions. This forms the basis for the characterization and modeling efforts that will be explored in the subsequent chapters.

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Chapter 2

RF measurement under cryogenic temperature condition

Contents

2.1 Introduction

Several RF techniques has been developed to fully characterize both passive [PS00; WW10] and active device [Woe+01] behavior at room temperature. Nowadays, due to the emergence of cryogenic applications and especially quantum computing, the RF characterization at very low temperature has earned interest and some papers are focusing on the RF device performances at low temperature [Cha19; Dij+20].

In this chapter, we begin by outlining the procedure for characterizing a RF two-port network before delving into the intricate process of extracting model parameters for inductors and transistors. Subsequently, we described the methodology for conducting RF measurements, focusing on S-parameter measurements using a Vector Network Analyzer (VNA), as well as the techniques for calibration and de-embedding to isolate the RF response of the Device Under Test (DUT). Next, we introduce two different types of RF cryogenic probers, highlight their respective advantages and limitations, and present the methodology for obtaining good quality RF cryogenic measurements. Following this, we discuss the challenges associated with cryogenic measurements, including cryogenic temperature calibration, contact issues, and temperature control. Finally, we introduce the methodology to perform RF cryogenic noise measurements.

2.2 Two-port network definition

2.2.1 Impedance and admittance matrix

To characterize the behavior of circuits operating at high frequencies (from kHz to GHz, called Radio Frequencies), they can be modeled as a two-port network, illustrated in Figure 2.1. This configuration has four terminals and two ports: a port voltage is defined as the voltage difference between a pair of terminals, with one terminal in the pair designated as the reference terminal. The current entering the network at the upper terminal of Port 1 is denoted as I_1, with an equal current exiting from the reference terminal.

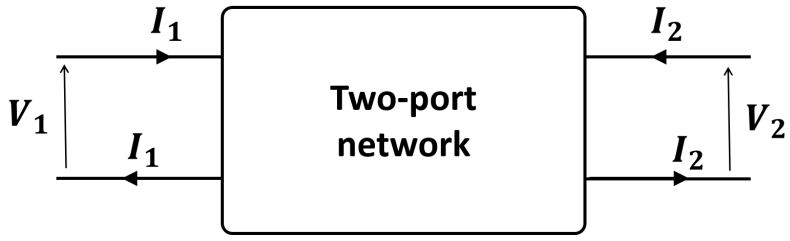

Figure 2.1: Representation of a two-port network

The relationship between two-port network inputs and outputs can be expressed through the impedance matrix $[Z]$, as presented in [Poz11]:

$$[V] = [Z][I] \tag{2.1}$$

For the case of a two-port network:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{2.2}$$

$$\Leftrightarrow \begin{cases} V_1 = Z_{11}I_1 + Z_{12}I_2 \\ V_2 = Z_{21}I_1 + Z_{22}I_2 \end{cases} \tag{2.3}$$

From the system of equations (2.3), the different Z-parameters can be expressed as:

$$Z_{ij} = \frac{V_i}{I_j} \qquad with\ I_k = 0\ for\ k \neq j \tag{2.4}$$

Z_{ii} is the input impedance observed from port i, while Z_{ij} is the transfer impedance between ports i and j. Z_{ij} is determined by applying a current I_j to port j, while open-circuiting all other ports and measuring the resulting voltage at the port i. In the case of two-port network, in order to measure Z_{12}, it is necessary to drive the current I_2 to the port 2, while open-circuiting port 1 ($I_1 = 0$ A) and then to measure the voltage V_1 at the port 1.

The relationship between inputs and outputs can also be established using admittance matrix $[Y]$:

$$[I] = [Y][V] \tag{2.5}$$

Giving for the case of a two-port network:

$$\Leftrightarrow \begin{cases} I_1 = Y_{11}V_1 + Y_{12}V_2 \\ I_2 = Y_{21}V_1 + Y_{22}V_2 \end{cases} \tag{2.6}$$

The Y-parameters can be expressed as:

$$Y_{ij} = \frac{I_i}{V_j} \qquad with\ V_k = 0\ for\ k \neq j \tag{2.7}$$

This time to measure Y_{ij}, the voltage V_j is driven to the port j and all other ports are short-circuited (V_k = 0 for k $\neq$ j) and the current I_i is measured at the port i.

The transformation of the impedance matrix into the admittance matrix is a straightforward process:

$$[Y] = [Z]^{-1} \tag{2.8}$$

The following section presents the electrical model of an inductance and of a transistor using admittance and impedance matrices.

2.2.2 Electrical parameter extraction through model representation

2.2.2.1 Inductors

Figure 1 depicts a top view schematic of a coil RF inductor. This inductor features two turns and is constructed on two metal levels, enabling the creation of a lengthy metal track. The cross-section is formed with a single metal level, facilitating the interconnection between the inner and outer coils.

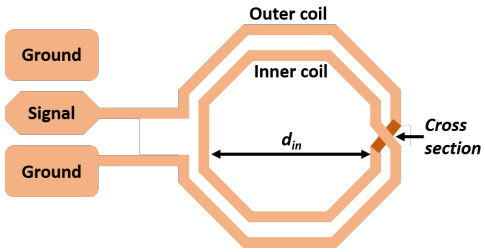

Figure 2.2: Top view schematic of a coil RF inductor

2.2.2.1.1 Inductor modeling

According to [PS00], inductors are not ideal due to their metallic composition and inherent resistivity. Additionally, at high frequencies, the capacitive coupling effect between the metal track coil or the different inductor metal levels, as well as the different capacitances between the metal and the oxide must be considered. All these capacitances can be modeled by a total capacitance Cp. Figure 2.3 depicts the model of an inductor with all these effects taken into account, L_s being the inductance value of the inductor.

The resistance R_s comes from the resistivity of the metal track. As a first approximation, this resistance value can be calculated from :

$$R_S = \rho \frac{l}{S} \tag{2.9}$$

where ρ is the resistivity of the metal used for the track, l is the total inductor length and S is the metal track section.

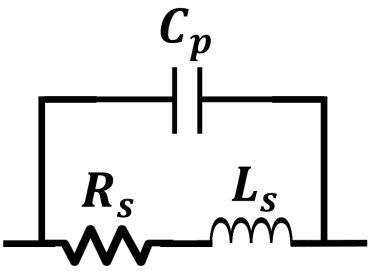

Figure 2.3: Inductance RLC model

The L_sC_p circuit creates a resonant frequency at the value:

$$f_0 = \frac{1}{2\pi\sqrt{L_sC_p}} \tag{2.10}$$

This simple model is valid up to 1GHz, and the component values can be easily extracted from 1-port RF measurements. However, for higher frequencies, two effects impact the current density inside of the metal track [Cao+03]. These effects are the skin effect and the proximity effect that create a frequency dependant resistance instead of a constant R_s.

As the frequency increases, the skin effect causes a non-uniform current density within the metal track. In particular, current density becomes higher at the metal track edge, leading to a predominant flow of current there and a reduction in the core of the metal track. Consequently, the effective resistance increases (due to the reduction of the effective conduction cross-section). This effect results in a higher radio frequency (RF) resistance compared to direct current (DC) resistance [Whe42].

The proximity effect arises from the close arrangement of inductive metal tracks. Often, these tracks are organized into multiple coils to maximize efficiency within a limited space. Consequently, each coil induces an effect on its neighboring coil. This alteration in current density results in a further reduction of the effective cross-sectional area of the metal tracks at high frequency [KI01].

These two effects on the current density are represented in figure 2.4.

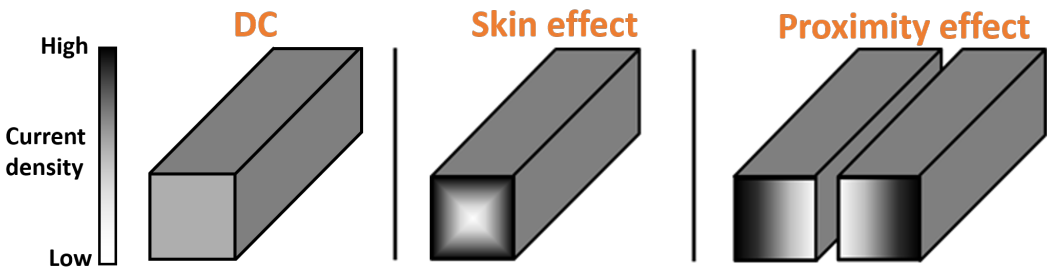

Figure 2.4: Schematics of the current densities distribution in inductor metal track (Left) for one track with the skin effect (Right) for two tracks closed to each other with the proximity effect [Cao+03]

The current densities distribution within the metallic track is observed to be uniform. However, at high frequencies, both the skin effect and the proximity effect influence the resistance value, making it frequency-dependent. To model a resistance that varies with frequency, [Cao+03] suggests adding a resistance R_{res} in parallel with an inductance L_{var}, This model is shown in figure 2.5

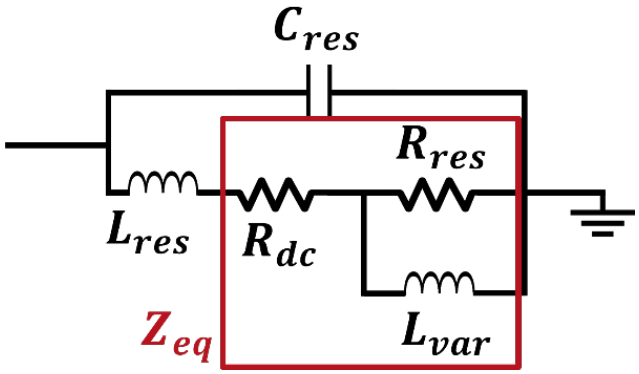

Figure 2.5: Inductance RLC model with skin and proximity effect

The new equivalent impedance, Z_{eq}, consists of R_s, L_{var} and R_{res} and shown in figure 2.5. Z_{eq} is expressed with the following equations:

$$Re(Z_{eq}) = \frac{R_s^2 R_{res} + R_s R_{res}^2 + R_s L_{var}^2 \omega^2}{(R_s + R_{res})^2 + L_{var}^2 \omega^2} \tag{2.11}$$

$$Im(Z_{eq}) = \frac{R_s^2 L_{var} \omega + 2 R_s L_{var} R_{res} \omega}{(R_s + R_{res})^2 + L_{var}^2 \omega^2} \tag{2.12}$$

The impact of the skin and proximity effects is to cause the resistance of the inductor to vary with frequency. Consequently, the impedance Z_{eq} has a real part (i.e., the resistance) that increases with frequency and an imaginary part that is negligible compared to the imaginary part of the inductance L_s.

In the previous model, the individual capacitive contributions are not separated. Instead, all capacitances are represented as C_p. This representation is true for inductors that are designed with a metal shield, isolating them from substrate influence. To take into account the substrate electric losses through the dielectric, an RC parallel circuit is added as presented in [PS00; Cao+03] and in figure 2.6.

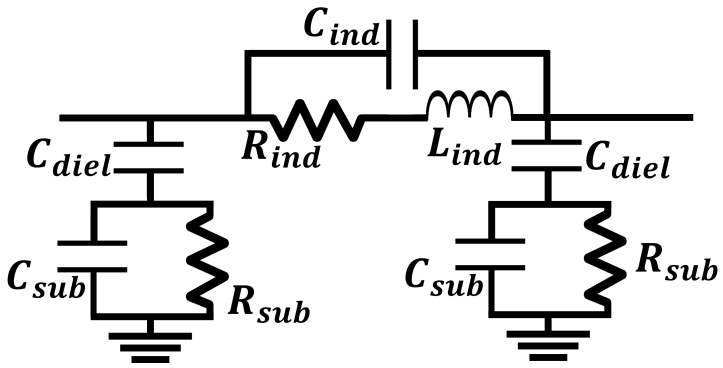

Figure 2.6: Inductance RLC model with substrate impact

The two models proposed in figure 2.5 and 2.6 are complementary. The skin and proximity effects can be incorporated into the last model by modifying the metal resistance, as shown in figure 2.5.

2.2.2.1.2 Typical inductor impedance measurements

The figure 2.7present the typical measurement of the input impedance of an inductor.

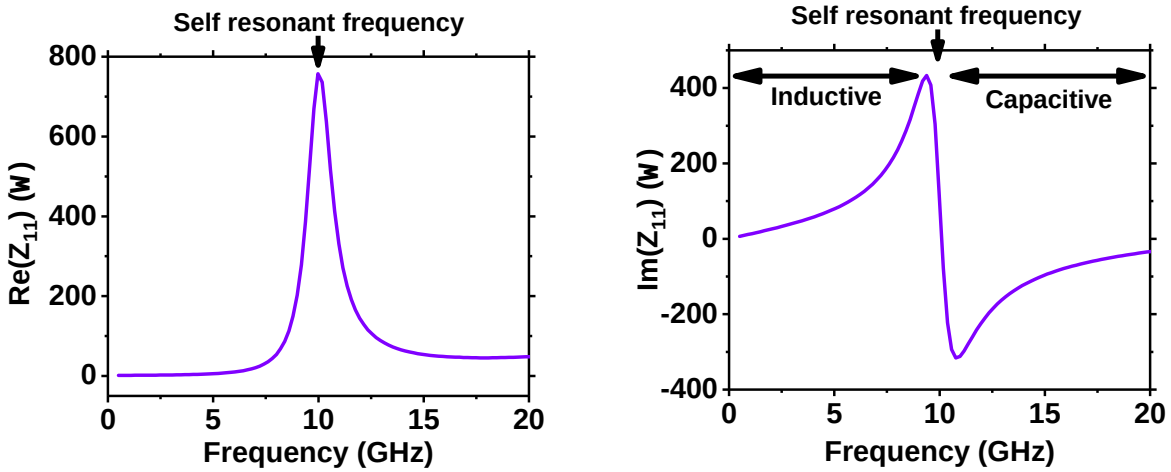

Figure 2.7: Inductor impedance as a function of the frequency

The imaginary impedance of an ideal inductor or capacitor is given by $Z = jL\omega$ and $Z = \frac{-j}{\omega C}$, respectively. Thus, when the imaginary part of a device impedance is positive, the device exhibits inductive behavior, whereas a negative imaginary part indicates capacitive behavior. The device exhibits

inductive characteristics at low frequencies, transitioning to capacitive behavior at high frequencies (due to the different parasitic capacitance), specifically after reaching the Self Resonant Frequency (SRF), which occurs around 10 GHz in this case.

2.2.2.2 Transistor

The section below presents the RF characterization of transistors. Figure 2.8 shows the small-signal equivalent model of a transistor [Kwo+02; Nys+21; El +16].

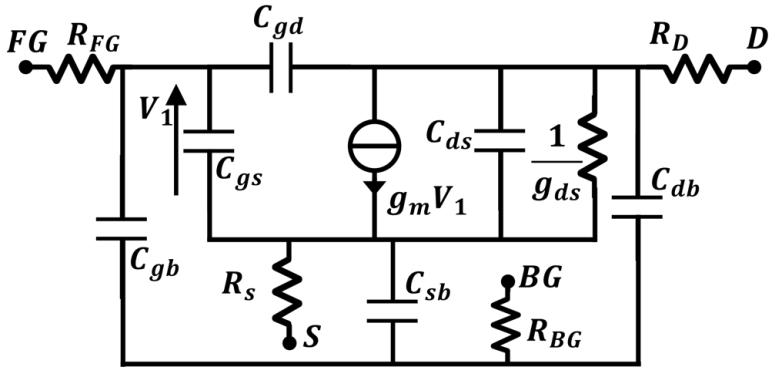

Figure 2.8: Small-signal equivalent circuit of a transistor in saturation

The current passing through the gate and drain is respectively referred to as I_G and I_d. To characterize our transistor, the source is always grounded and, depending on the study, the back-gate may or may not be grounded.

2.2.2.2.1 Parameters extraction

As an initial approximation, the drain, the source, the front gate and the back-gate access resistances are neglected due to their very low value [Nys+20]. The source and the back gate are connected to the ground. Under these simplifications, C_{gb} and C_{db} are parallel to C_{gs} and C_{ds}, respectively. Additionally, C_{gb} and C_{db} are respectively considered negligible compared to C_{gs} and C_{ds}, as the buried oxide is more than 10 times thicker than the front oxyde.

To extract the transistor characteristics, the admittance matrix is used [Kwo+02; Bou13]. First, we drive V_d to the ground to calculate Y_{gg} and Y_{dg}. The equivalent circuit is presented in Figure 2.9 (Left). Then, we drive V_g to the ground to calculate Y_{dd} and Y_{gd}. The equivalent circuit is shown in Figure 2.9 (Right).

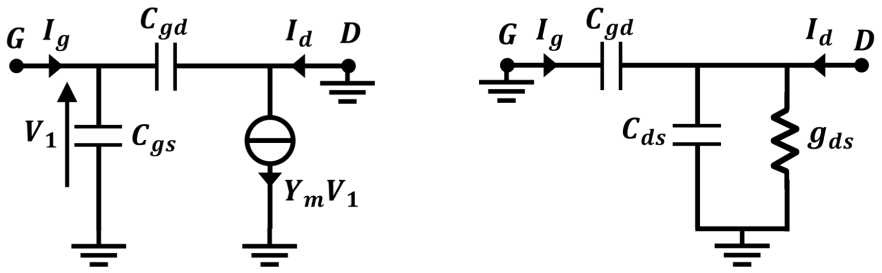

Figure 2.9: Small-signal equivalent circuit of a transistor in saturation with $V_d = 0V$ (left), and with $V_g = 0V$ (right)

The following equations are obtained:

$$Y_{gg} = j\omega(C_{gs} + C_{gd}) = j\omega C_{gg} \tag{2.13}$$

$$Y_{gd} = -j\omega C_{gd} \tag{2.14}$$

$$Y_{dg} = g_m - j\omega C_{gd} = g_m - j\omega C_{dg} \tag{2.15}$$

$$Y_{dd} = g_{ds} + j\omega(C_{ds} + C_{gd}) \tag{2.16}$$

The small-signal model components can be extracted from these parameters.

2.2.2.2.2 Figures of merit calculation

With the previous admittance expressions or the small signal parameters, the two transistor figures of merit, the transition frequency and the maximum oscillation frequency, can be calculated [Kaz+16].

The transition frequency is the frequency when the current gain ($|H_{21}|$) is equal to 1.

$$H_{21} = \left.\frac{I_d}{i_g}\right|_{V_d=0} = \frac{Y_{dg}}{Y_{gg}} = \frac{g_m - j\omega C_{dg}}{j\omega C_{gg}} = 1 \tag{2.17}$$

By definition C_{dg} is less than C_{gg} (since $C_{gg} = C_{gs} + C_{gd}$, so at high frequency, when H_{21} can be approximate by $\frac{-j\omega C_{dg}}{C_{gg}}$, f_t is always defined. At frequency of interest for f_t [Kaz+16], we can consider that ωC_{dg} is small compared to g_m and formulas become:

$$f_t = \frac{g_m}{2\pi C_{gg}} \tag{2.18}$$

Given that H_{21} represents a gain in current and is proportional to $\frac{1}{\omega}$, the slope of the function H_{21} versus frequency is equal to -20 decibels per decade.

The maximum oscillation frequency is the frequency when the unilateral gain (U) reach its cut-off frequency (meaning U=1) [Kaz+16]. U is defined as:

$$U = \frac{|Y_{dg} - Y_{gd}|^2}{4(Re(Y_{gg})Re(Y_{dd}) - Re(Y_{gd})Re(Y_{dg}))} \tag{2.19}$$

$$U = \frac{g_m^2}{4 \cdot \omega^2 \cdot R_{gg\_ext} \cdot C_{gg} \cdot (C_{gg} \cdot g_{ds} + C_{gd} \cdot g_m)} \tag{2.20}$$

Given that U represents a power gain and is proportional to $\frac{1}{\omega^2}$, the slope of the graph of U versus frequency is equal to -20 decibels per decade.

After some calculations, the maximum oscillation can be express as:

$$f_{max} = \frac{f_t}{2\sqrt{(R_g + R_s)g_{ds} + 2\pi f_t C_{gd} R_g}} \tag{2.21}$$

The transition frequency and the maximum oscillation frequency can be extracted by calculation with the different small signal parameters or by finding the point where h_{21} or U cross 0dB of gain respectively as presented in figure 2.10. Due to instrument limitation (notably, the RF K connectors present on the cryogenic prober and on the cryogenic probes permit measurements up to 40 GHz), h_{21} and U are extrapolated to extract the figure of merit.

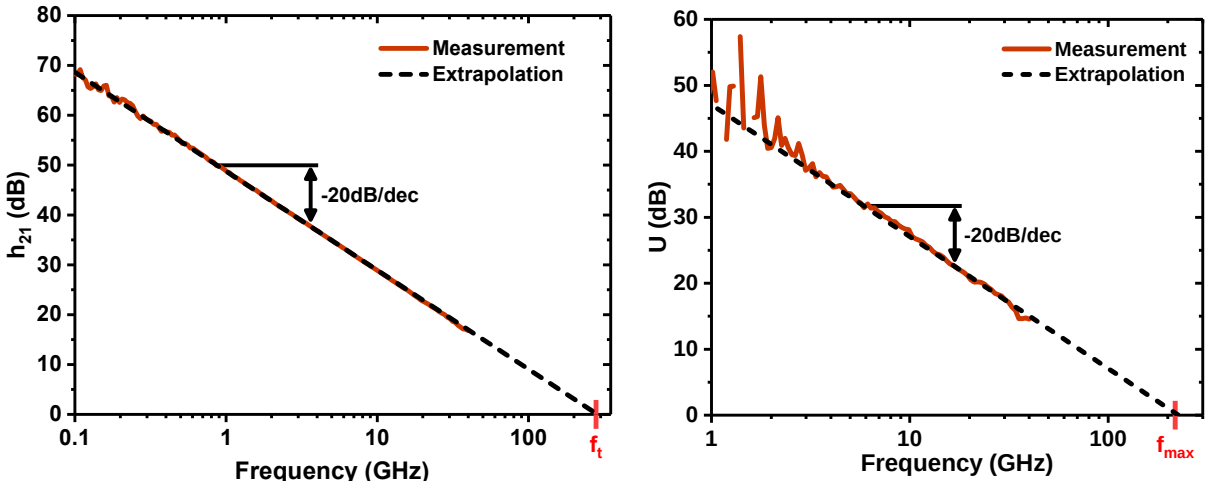

Figure 2.10: (Left) H_{21} and (Right) U as a function of frequency. The transition frequency and the maximum oscillation frequency can be determined by identifying where the extrapolation crosses 0dB. The transistor gate width is 80 fingers of 1 μm and its gate length is 28 nm.

2.2.2.2.3 Access resistance extraction

To extract the drain and source access resistance, Bracale's method can be used [Bra+00]. To perform this method, the transistor is biased in inversion regime and at drain to source voltage equal to 0V (i.e. $V_{DS} = 0V$ and $V_{GS} > V_T$). Under these conditions, the transistor is symmetric leading to $C_{gs} = C_{gd} = C$ and $g_m = 0S$ since there is no drain current. The equivalent circuit is presented in Figure 2.11.

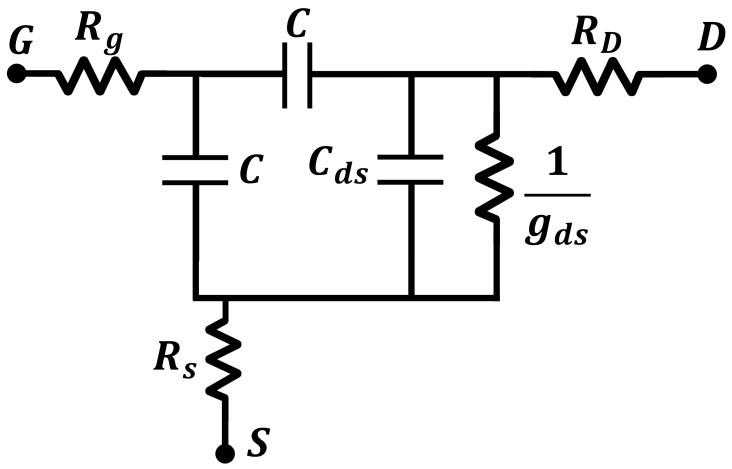

Figure 2.11: Small-signal equivalent circuit in strong inversion and V_{DS} = 0 V.

Using the impedance matrix for the previous equivalent circuit, we can obtain the following results:

$$Re(Z_{dd} - Z_{gd}) = R_d + \frac{1}{2g_{ds}} \tag{2.22}$$

$$Re(Z_{gd}) = R_s + \frac{1}{2g_{ds}} \tag{2.23}$$

$$Re(Z_{gg} - Z_{gd}) = R_g - \frac{1}{4g_{ds}} \tag{2.24}$$

With these equations, we can plot $Re(Z_{dd} - Z_{gd})$, $Re(Z_{gd})$ or $Re(Z_{gg} - Z_{gd})$ as a function of $\frac{1}{V_g - V_{th}}$. The curve will have linear variation because we consider a constant mobility at high V_{GS}, so $\frac{1}{g_{ds}}$ have linear variation with $\frac{1}{V_g - V_{th}}$. The origin ordinate is the R_d, R_s or R_g access resistance. Figure 2.12 presents the methodology to extract the different access resistances.

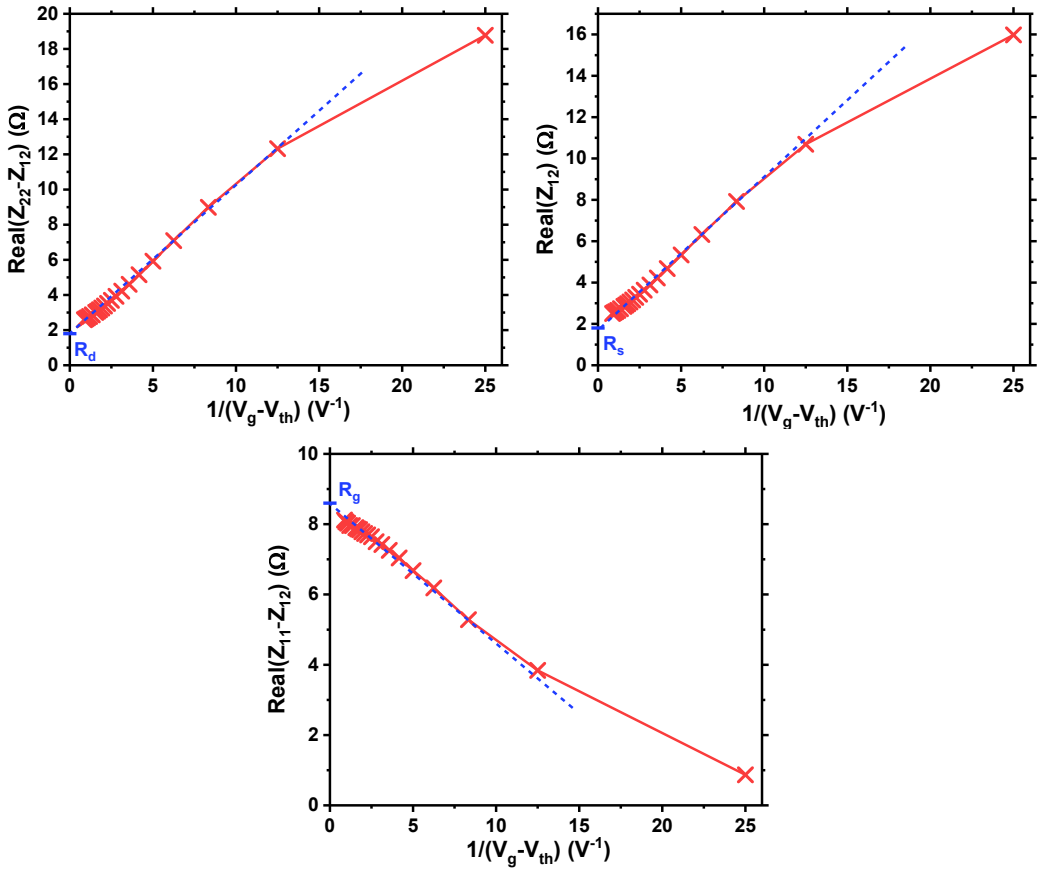

Figure 2.12: Extraction of the different access resistance with Bracale's methodology. From left to right, plot of the real part of Z_{dd} minus Z_{gd} or Z_{gd} or Z_{gg} minus Z_{gd} as a function of $1/(V_g - V_{th})$ to extract R_d, R_s or R_g respectively. The transistor gate width is 80 fingers of 1 μm and its gate length is 28 nm.

On the graphs above, the drain, source and gate access resistance are extracted and are equal to 1.95Ω, 1.9Ω and 8.6Ω respectively.

2.3 RF measurement methodologies

2.3.1 Scattering-parameters

Measuring the Z or Y matrix at high frequency directly is very complicated since it is necessary to have perfect short- or open-circuits, as explained previously [Poz11]. Achieving these conditions at high frequencies is not feasible in practice due to parasitic capacitances and inductances. Besides, some devices (such as Power Amplifier) might deal with stabilization issues because of the presence of short- and open-circuits.

To ensure accurate measurements [Poz11], it is recommended to use Scattering parameters (or S-parameters) to characterize RF devices. This method does not require perfect short or open circuits and is related to the concept of incident and reflected (or transmitted) waves. S-parameters are measured using a Vector Network Analyzer (VNA) with a reference resistance (usually 50 Ω). Figure 2.13 shows the representation of a two-port network with the S-parameters definition.

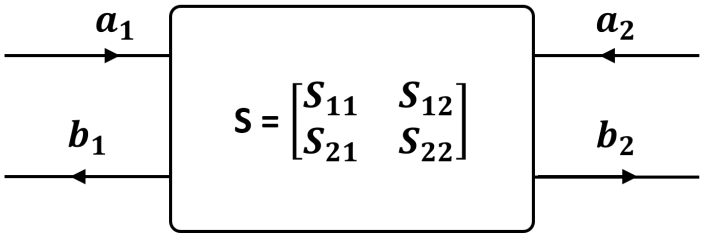

Figure 2.13: Representation of a two-port network with the power wave

a_i is the input wave and b_i the output wave. In comparison with the Figure 2.1, the wave factors can be expressed as:

$$a_i = \frac{V_i + R_i I_i}{2\sqrt{R_i}} \tag{2.25}$$

$$b_i = \frac{V_i - R_i I_i}{2\sqrt{R_i}} \tag{2.26}$$

where R_i is the resistance seen at the port i. Usually $R_i = 50\Omega$

Now that the different elements in S-parameters are defined, they can be measured. Similar to the impedance and admittance matrix, S-parameters can be expressed as:

$$\begin{cases} b_1 = S_{11}a_1 + S_{12}a_2 \\ b_2 = S_{21}a_1 + S_{22}a_2 \end{cases} \tag{2.27}$$

The measurements are carried out in two steps:

- Direct direction: the incident wave is injected in a_1 and a_2 is null. The reflected wave b_1 and the transmitted wave b_2 are measured. We obtain the parameters S_{11} and S_{21}
- Opposite direction: the incident wave is injected in a_2 and a_1 is null. The reflected wave b_2 and the transmitted wave b_1 are measured. We obtain the parameters S_{22} and S_{12}

The following formulas convert S-matrix to the admittance matrix and to the impedance matrix:

$$[Z] = Z_0([U] - [S])^{-1}([U] + [S]) \tag{2.28}$$

$$[Y] = \frac{1}{Z_0}([U] - [S])([U] + [S])^{-1} \tag{2.29}$$

Where [U] is the unity matrix and Z_0 is the normalized impedance (usually 50 Ω).

2.3.2 Calibration and de-embedding

The objective of this manuscript is to examine the behavior of electronic components at the device level. Two solutions are available to perform RF cryogenic measurements: within a cryostat with a packaged device or within a probe station with on-wafer measurements. The on-wafer measurement approach was selected for this study because it allows faster measurements, cable length is shorter and no packaging is needed which reduces the parasitic elements introduced and allows measurement at higher frequencies. Figure 2.14 illustrates the test bench used in on-wafer measurements, depicted on the left, and the configuration of the RF probes connected to the Device Under Test, depicted on the right.

As described in reference [RR08], the presence of RF cables and access lines connecting the VNA to the DUT introduces some parasitic inductance, resistance and capacitance perturbing the device measurements. To move the measurement reference plan from the VNA output to the DUT input, two methods are employed:

- A **calibration** is performed to remove the effect of the RF cables and set the plan at the end of the RF probes (figure 2.14(left))
- A **de-embedding** is made to compensate the parasitic element introduce by the access lines between RF probes and the DUT (figure 2.14(right)). The plan is moved from the probe end to the DUT input.

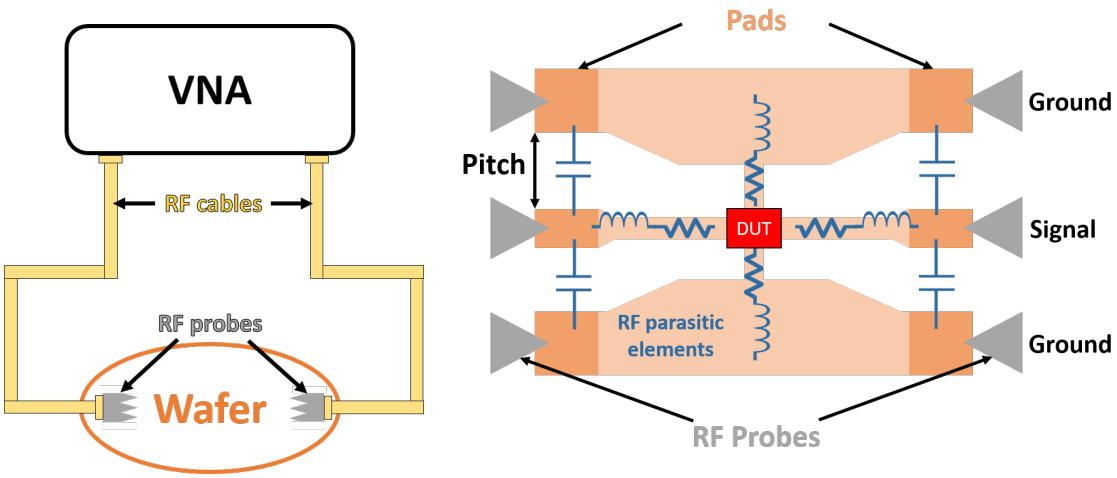

Figure 2.14: (Left) Connection of the Vector Network Analyzer to the RF probes. (Right) Connection of the RF probes to the Device Under Test (DUT)

2.3.2.1 Calibration

The calibration is conducted on an Impedance Standard Substrate (ISS), which has a variety of test structures (open, short, load, etc.). Different calibration methodologies may be employed, depending on the probes, the working frequency and the test structure available on the ISS used. The SOLT (Short-Open-Load-Thru) method as described in [Pra+21; Wil+14], is the most commonly used calibration method since the 1980s. This method involves measuring four circuits:

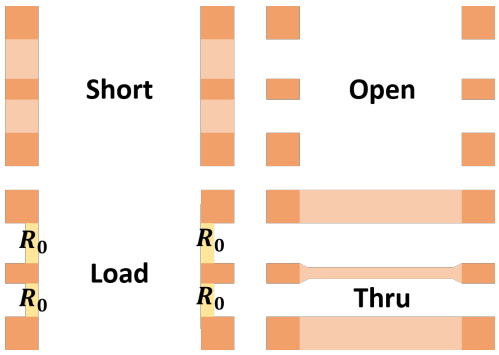

Figure 2.15: Representation of Short Open Load and Thru standards on the calibration kit

The Load sets the value of the measurement reference impedance. The Short connects the signal to the ground and compensates for the capacitance between the peaks. The Open does not connect anything and compensates for the inductance introduced by the cable. The thru connects Port 1 to Port 2 and compensates for transmission losses.

After calibration, the measurement reference plane is set to the end of the RF probes but the device

access lines still perturbed the measurements. For this reason, an additional correction is needed to be at the DUT input reference.

2.3.2.2 De-embedding

To remove the access line, a second correction called de-embedding is applied [BP74]. The probes are placed on special structures on the wafer for this correction. The de-embedding process may vary depending on the maximum frequency, the measured device and the available structure on the wafer [Med+24]. We presented in this manuscript two different methods to de-embed measurements:

- **Open-short** de-embedding which removes the pad parallel admittances and the interconnect series impedances.
- **Vandamme** de-embedding which is similar to Open-Short technique but with an extra compensation for the coupling between DUT input and output.

Figure 2.16 presents the three structures used for de-embedding. Both de-embedding techniques will be explained next.

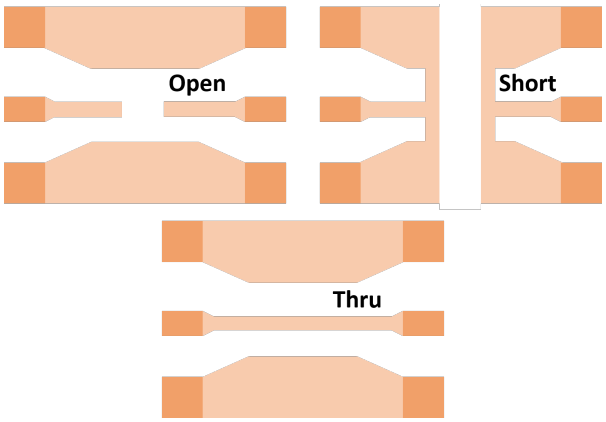

Figure 2.16: Representation of open, short and thru devices to de-embed the raw measurements

The first technique employed is the **open short** de-embedding, which is performed using the structure of the same name [Koo92]. The figure 2.17 presents the different equivalent circuits used for this extraction.

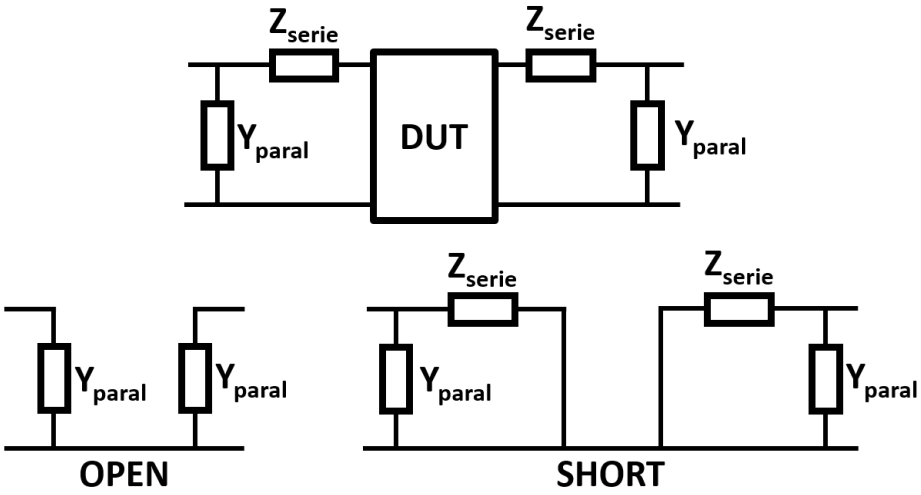

Figure 2.17: (Top) Equivalent circuit of the test structure with: DUT and the different access parameter (Z_{serie} and Y_{paral}) considered in OPEN SHORT de-embedding technique. (Bottom) Equivalent circuit of the OPEN and SHORT de-embedding pattern

The open measurement, Y_{paral}, corrects for pads and access lines capacitance and admittance. The short measurement, Y_{short}, addresses contact resistance, access line inductance and resistance. Equivalence of contact resistance between short and the device under test (DUT) is crucial for compensating parasitic elements. In semi-automatic probing, maintaining constant wafer force ensures identical contact resistances, yielding an impedance denoted as Z_{serie}. The DUT impedance can be determined using the following equations:

$$Y_{open} = Y_{paral} \tag{2.30}$$

$$Y_{short} = Y_{paral} + (Z_{serie})^{-1} \tag{2.31}$$

$$Y_{raw} = Y_{open} + (Z_{serie} + Z_{DUT})^{-1} \tag{2.32}$$

With the two previous equations we can finally express:

$$Z_{DUT} = (Y_{raw} - Y_{open})^{-1} - (Y_{short} - Y_{open})^{-1} \tag{2.33}$$

The Open-Short de-embedding technique is often used because it is easy to set up (only need two additional structures) and gives good results up to high frequency [Med+24]. However, as written before, another technique has been proposed to remove more parasitic components.

The second technique is the Vandamme de-embedding method [VSV01] which used the three structures presented in figure 2.16. This method has a higher precision compared to Open-Short de-embedding since it removes also the coupling admittance between port 1 and 2 or the ground leads

toward the DUT. However, in comparison with Open-Short de-embedding techniques, the Vandamme de-embedding method requires an additional test structure (Thru structure), resulting in a larger silicon surface requirement besides the additional measurement time. The different equivalent circuits used for this extraction are presented in figure 2.18.

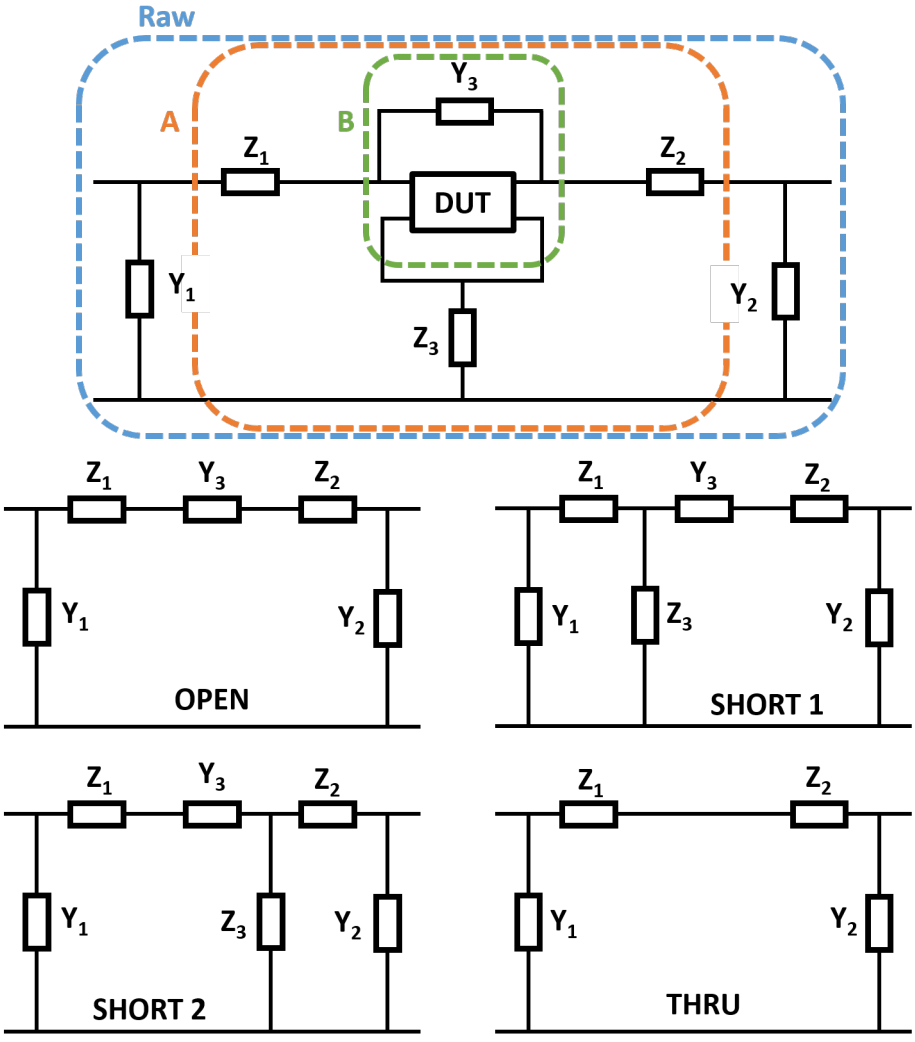

Figure 2.18: (Top) Equivalent circuit of the RF test-structure with the DUT in the middle and the different access parameter for Vandamme de-embedding technique. (Bottom) Equivalent circuit of the OPEN, SHORT and THRU de-embedding pattern

On figure 2.18, the different de-embedding step are represented in dotted lines. As for the previous technique, with the de-embedding structure measurement, we can compute the different admittance and impedance of the model with the following equations:

$$Y_1 = Y_{open,1,1} + Y_{open,1,2} \tag{2.34}$$

$$Y_2 = Y_{open,2,2} + Y_{open,1,2} \tag{2.35}$$

$$Y_3 = \frac{1}{\frac{-1}{Y_{open,1,2}} + \frac{1}{Y_{thru,1,2}}} \tag{2.36}$$

$$Z_1 = 0.5 \times (\frac{-1}{Y_{thru,1,2}} + \frac{1}{Y_{short,1,1} - Y_1} - \frac{1}{Y_{short,2,2} - Y_2}) \tag{2.37}$$

$$Z_2 = 0.5 \times (\frac{-1}{Y_{thru,1,2}} - \frac{1}{Y_{short,1,1} - Y_1} - \frac{1}{Y_{short,2,2} - Y_2}) \tag{2.38}$$

$$Z_3 = 0.5 \times (\frac{1}{Y_{thru,1,2}} + \frac{1}{Y_{short,1,1} - Y_1} - \frac{1}{Y_{short,2,2} - Y_2}) \tag{2.39}$$

$$\tag{2.40}$$

Finally we can obtained the DUT parameter by removing step by step the different admittance or impedance. Between raw measurement and stage A, Y_1 and Y_2 are removed:

$$Y_A = Y_{raw} - \begin{bmatrix} Y_1 & 0 \\ 0 & Y_2 \end{bmatrix} \tag{2.41}$$

Then to move from step A to step B, the Y_A admittance matrix is converted in a Z_A impedance matrix and the series and leak impedance are removed:

$$Z_B = Z_A - \begin{bmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{bmatrix} \tag{2.42}$$

Finally, only the coupling admittance is remaining and it can be obtained by converting the Z_B impedance matrix in to a Y_B admittance matrix and then removing the Y_3:

$$Y_{DUT} = Y_B - \begin{bmatrix} Y_3 & -Y_3 \\ -Y_3 & Y_3 \end{bmatrix} \tag{2.43}$$

After the calibration and the de-embedding, the measurement reference is now as close as possible to the DUT. These two techniques eliminate major measurement inaccuracies.

2.4 RF cryogenic set up

Two different RF cryogenic probers were accessible during this work. This section presents the advantages and draw-back of these two probers and the choice we have done for our characterization. The main difference remains the size of the cryogenic chamber.

2.4.1 Süssmictrotec cryogenic prober

A picture of the prober is presented in figure 2.19.

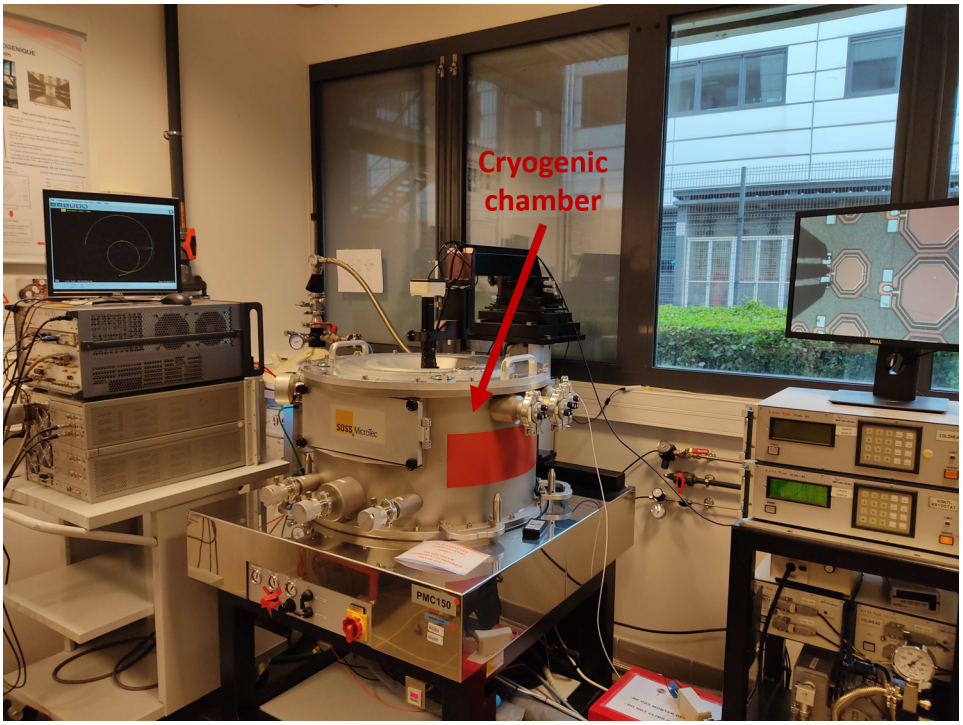

Figure 2.19: Süssmicrotec cryogenic prober with 6 arms for DC and RF measurements

Six arms are available inside this prober which allows us to perform measurement with 4 DC probes and 2 RF probes. As it can be seen on this picture, the cryogenic chamber is big (Approximately 600 mm of diameter and 300 mm of height). Due to this size it presents advantages and draw-backs which are listed in table 2.1.

2.4.2 Lakeshore cryogenic prober

The lakeshore cryogenic prober is presented in figure 2.20.

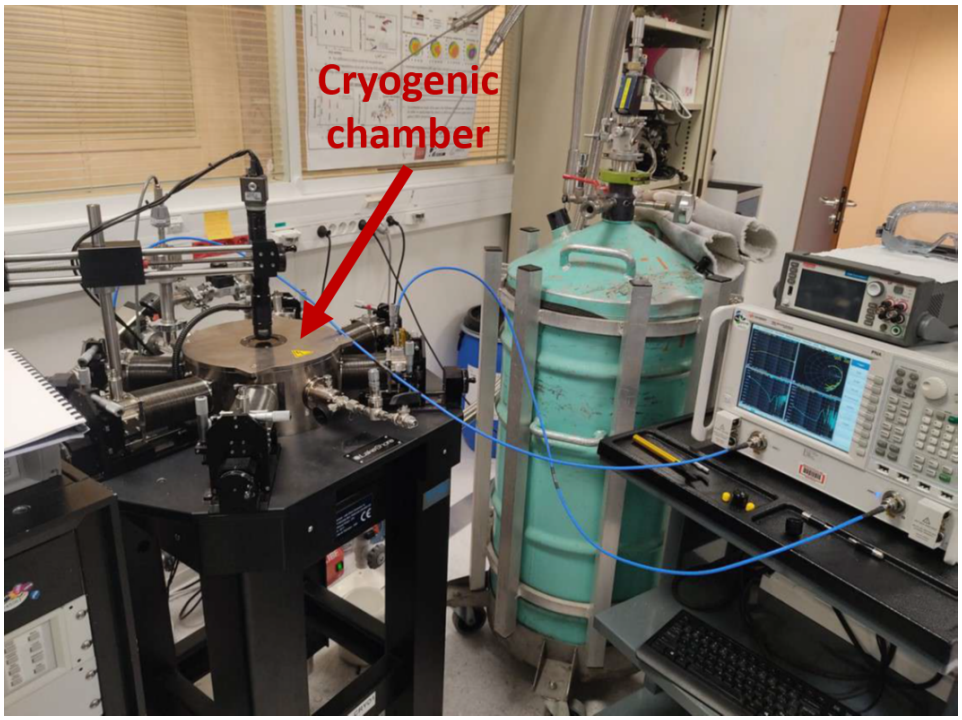

Figure 2.20: Cryogenic prober with six arms allowing DC and RF measurements.

On this prober also, six arms are available that allow measurement with 4 DC probes and 2 RF probes. In comparison to the previous prober presented, the cryogenic chamber is smaller (Approximately 280 mm of diameter and 343 mm of height) . This size presents advantages and draw-backs which are presented and compared with Süssmicrotech prober in table 2.1

Prober	Süssmicrotech	Lakeshore
Number and type of access	4 DC, 2 RF	4 DC, 2 RF
Measurement frequency	Up to 50GHz	Up to 40GHz
Theoretical T_{min}	9K	4.2K
Fluid consumption	High, 100L of helium to cool down to T_{min} and $\approx$ 6h of measurement	Low, 100L of helium to cool down two times to T_{min} and $\approx$ 12h of measurement
Probes and contact	Zprobes, very good contact quality	Picoprobes, good contact quality
Chuck diameter	200mm	$\approx$ 5cm
Cooling time to T_{min}	One entire night	$\approx$ 2h

Table 2.1: Comparison between the different cryogenic probers.

The Süssmicrotech prober is efficient to provide RF measurements of many different devices and if the wafer can not be cut or if the sample is big. For my PhD to characterize passive and active devices, we prefer to have a low cryogenic fluid consumption and a small cooling time to perform quick cryogenic measurement of many different devices, that why all the measurements presented in this manuscript has been performed on RF lakeshore cryogenic performed. However, by choosing the smaller prober, we loose the opportunity to put different die and to perform statistics measurement.

2.5 Cryogenic measurement constraints

It should be noted that additional sources of uncertainty exist that are not directly related to the prober, but rather to the cryogenic temperature. This section presents an analysis of the various sources of uncertainty that have been mitigated to ensure the precision and reproducibility of the measurements. Firstly, the calibration is performed at each measurement temperature, as the temperature of the access cable is also modified. Subsequently, we present a precise methodology for establishing a good contact at cryogenic temperatures. Furthermore, the prober is optimized to achieve optimal probe thermalization, and characterization of the real sample temperature was conducted. It is crucial to possess a comprehensive understanding of temperature, particularly at cryogenic temperatures. A slight vari-

ation of a few kelvin can result in a significant discrepancy when compared to 4.2 kelvin.

2.5.1 Calibration and contact at cryogenic temperature

The calibration goal is to remove all the access and setup parasitic contributions. They depend on the used cables and their temperature. Since some cables are inside the cryogenic chamber, it is important to perform the calibration at each measurement temperature to have an accurate and repeatable calibration. The Impedance Standard Substrate (ISS) must also be compatible with cryogenic measurements, i.e. the different correction factors of the ISS should remain the same regardless of the temperature [Las+96]. For our calibration, we use a CS-5 from GGB Industry which is presented on [ind].

The cryogenic RF measurement is conducted in a vacuum environment within the chamber, however, it is not feasible to completely eliminate all ambient air. The few remaining ambient air will condense on the coldest part at low temperature. If condensation occurs on the sample, it results in contact difficulties, thereby rendering the measurement non-reproducible. To improve the contact quality, there is a screw under the prober (called Sample stage flow control) to control the presence and the amount of the helium/nitrogen fluid under the sample holder stage. The cooling circuit of the Lakeshore cryogenic prober is shown in Figure 2.21. The goal is to first cool the 4.2K shield (the closest metal shield around the sample holder to prevent the sample from being exposed to external heat) so that the few gaz remaining in the main chamber condense on the shield. The other solution to avoid condensation on the sample is to heat the sample up to 100K and then cool it down. Since the sample holder heats up faster than the 4.2K shield, condensation on the sample will evaporate and condense on the 4.2K shield when it is cool enough.

As presented in figure 2.21, the prober also includes four different temperature sensors, one on each shield stage and sample holder stage. However, the real temperature of the sample may differ from the one displayed by the sample stage sensor due to a temperature gradient in the metallic sample holder. For this reason, it is important to perform an evaluation of the sample temperature as discussed in the following section.

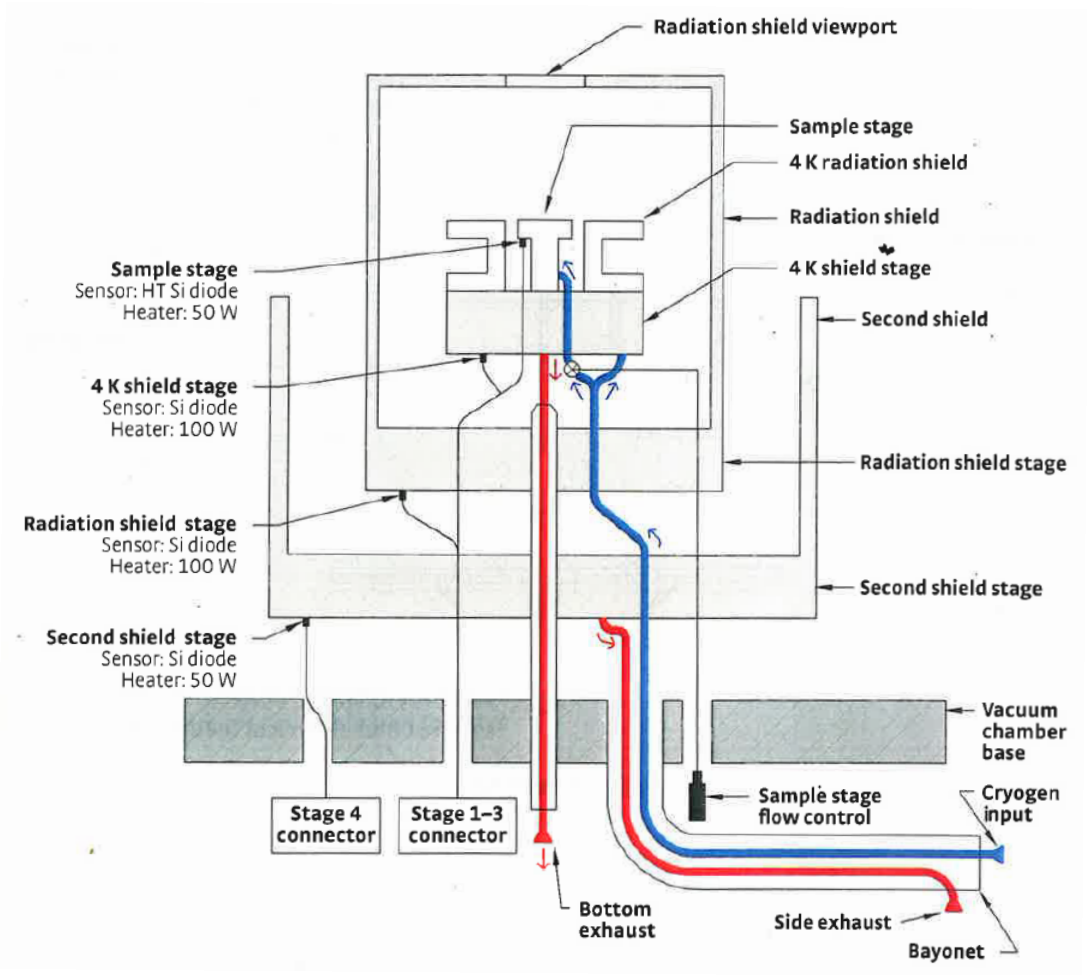

Figure 2.21: Cryogenic fluid circuit in Lakeshore cryogenic prober. Taken from [Lak09]

2.5.2 Thermalization and sample temperature

The second source of uncertainty for analyzing measurements during cryogenic RF measurements is the estimation of the sample temperature. To do this, we measured some superconducting passive devices (such as an inductor or a metal line) for different temperatures. For example, this section present the resistance value of a line in niobium, which is a superconducting metal. Below the critical temperature, the niobium becomes a superconductor, so its resistivity drops sharply. To determine the sample temperature, the resistance of the niobium line was measured with two RF probes to see at what set point temperature the resistance drops. The superconductor was previously calibrated under a dilution refrigerator to accurately know the critical temperature, which was determined to be 8.95K. Figure 2.22 shows niobium line and its resistance as a set point temperature function.

A second source of uncertainty in the analysis of measurements during RF cryogenic measurements is the gradient temperature estimation between the set point temperature, as indicated by the

thermometer on the sample holder, and the temperature of the sample itself. To achieve this, superconducting passive devices (such as an inductor or a metal line) were used to calibrate the actual sample temperature. Below the critical temperature (T_{crit}), the superconductor resistivity drops sharply. The objective is to compared the set point temperature at which the resistivity exhibits a sharp decline and to compare this with the critical temperature. The superconductors were previously calibrated under a dilution refrigerator to accurately know T_{crit}.

To illustrate this methodology, the following presents the measurement of a niobium line which as $T_{crit} = 8.95K$. Figure 2.22 shows niobium line and its resistance as a set point temperature function.

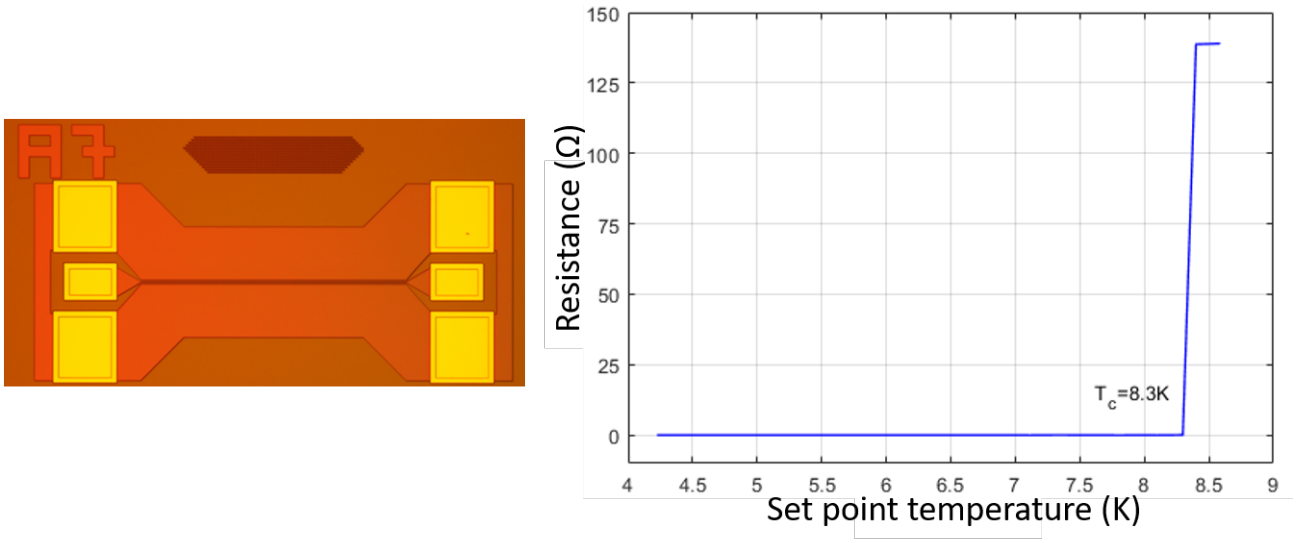

Figure 2.22: (Left) Transmission line in niobium which is a superconducting metal. (Right) Resistance of this line extracted at 30MHz as a function of the set point temperature.

On the previous graph, the transition temperature between low and high resistance is observed at 8.3K. We estimate that the temperature difference between the set point and the real sample temperature is approximately 0.6K. Additional tests were conducted on other superconducting metals with lower critical temperatures (down to $T_{crit} = 4.9K$), and the results consistently demonstrated a similar temperature difference.. This ΔT is very low and negligible due to all the precautions taken to perform these measurements.

To maintain at cryogenic temperature the sample, any heat source should be avoided. The RF probes are thermally connected to the room temperature through the measurement cables. Therefore, when the probes are in contact with the sample, some heat can be transferred to the measured device. To limit this heat transfer, it is necessary to link the probe to a cold tank maintained at 4.2 kelvins. The use of copper braid to link the probe to the 4.2 kelvin shield is therefore essential. Before doing a

measurement, the probe should be left in contact for at least 30 minutes to ensure that the probes and the sample are at the same temperature. All copper braids are shown in the figure 2.23.

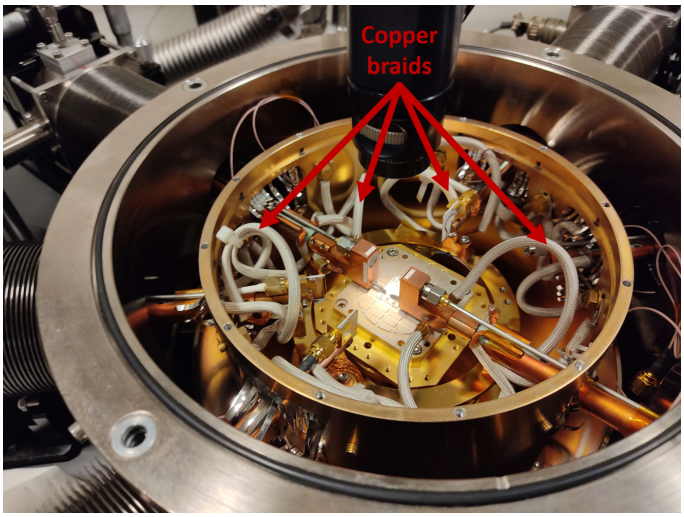

Figure 2.23: Cryogenic prober with the chamber open

2.6 Noise measurements

To extract the noise added by a device, the Noise Figure (NF) is extracted. The noise figure can be calculated by the following equation:

$$NF = \frac{SNR_{input}}{SNR_{output}} \tag{2.44}$$

Where SNR is the signal to noise ratio. It corresponds to the ratio between the signal power and the noise power (or noise floor). To understand the notion of noise figure, figure 2.24 presents the typical signal and noise levels versus frequency:

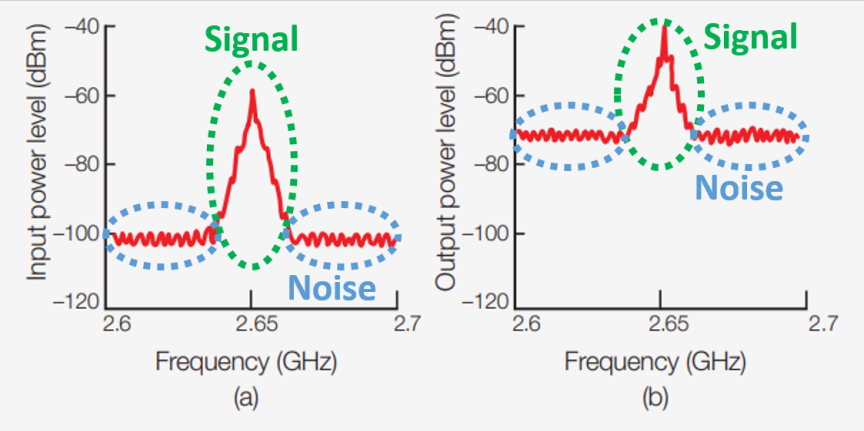

Figure 2.24: Typical signal and noise levels versus frequency (a) at an amplifier's input and (b) at its output. Note that the noise level rises more than the signal level due to added noise from amplifier circuits. This relative rise in noise level is expressed by the amplifier noise figure. Adapted from [Tec10b].

In figure 2.24 case, the input signal and noise power are -60 dBm and -100 dBm respectively, so the input SNR is 40dB. In output, the signal power is -40 dBm and the noise power is -70 dBm, so the SNR is 30dB. With the two signal to noise ratios we compute the NF which is equal to 10 dB.

For noise measurement, we used the Cold Source method because it is a known for its simplicity and ease of use [Tec10a; She+21]. The principle of this method is detailed in figure 2.25 and in the list of step under.

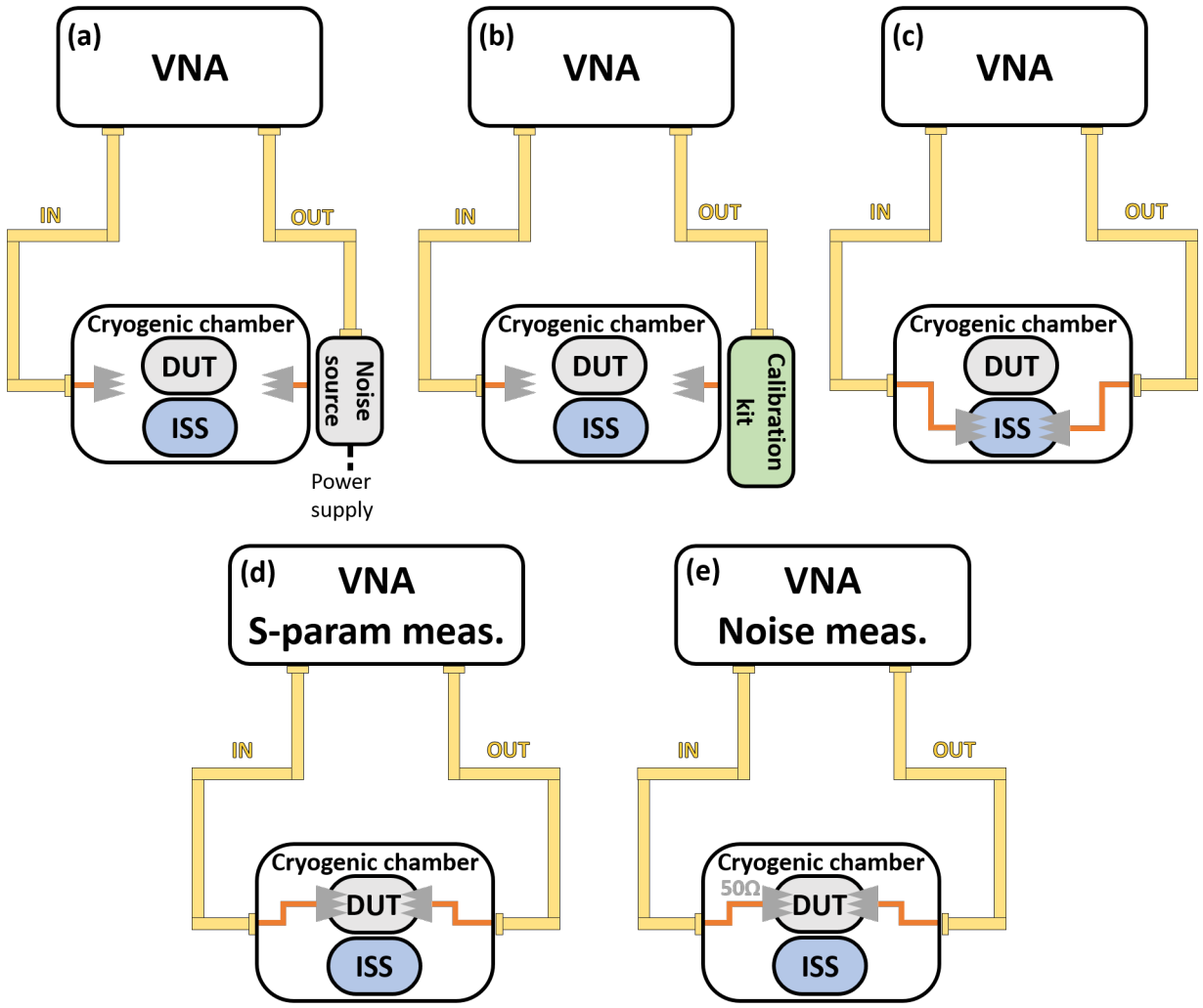

Figure 2.25: Schematics of the cryogenic noise measurement calibration and system. (a) Noise receiver calibration. (b) One port calibration with a calibration kit. (c) Calibration one the Impedance Standard Substrate inside of the cryogenic chamber. (d) DUT S-parameters measurement. (e) DUT noise measurement, a 50 Ω load is placed at the input of the DUT by the VNA.

- Figure 2.25(a): The noise source is connected to calibrate the VNA noise receiver.
- Figure 2.25(b): A one port Short-Open-Load calibration is performed with a calibration kit on the noise receiver of the VNA to compensate the cable and adapter between noise receiver and noise source.
- Figure 2.25(c): A two port calibration on ISS is performed to moved the noise and S-parameter measurement plane to the end of the RF probes.
- Figure 2.25(d): The S-parameters of the DUT is measured to known the circuit gain.

- Figure 2.25(e): The noise measurement is performed by the VNA. A 50 Ω load is placed at the input of the DUT by the VNA. The noise produce by this load is supposed to be only thermal noise (as it is a passive device [She+21]) and defined as [SK07]:

$$N_{in} = k_b T_a B \tag{2.45}$$

  where N_{in} is the thermal noise power (in watts), k_b is Boltzmann's constant, T_a is the absolute temperature of the system (in kelvins), B is the bandwidth (in hertz). The output noise is measured by the noise receiver of the VNA and the noise measured is the sum of the amplified input noise and the noise contributed by the circuit measured. With S-parameters measurement, the circuit gain is known, then the amplified input noise can be subtracted from the measurement, leaving only the noise contributed by the DUT. From this, noise figure is calculated.

When performing the noise figure measurement, in the step (e) the absolute temperature of the test system is needed (T_a) to calculate the correct value of input noise power introduce by the load. This values correspond to the temperature of the 50 Ω load placed at the input of the DUT by the VNA. As the VNA is internally heat, the temperature of this load is unknown and between the measurement temperature and the room temperature [Tec10a]. In our case, this temperature is left at 295K to ensure identical calibration at all measurement temperatures, and to be able to observe variations in noise figures rather than absolute values.

2.7 Conclusion

In conclusion, this chapter outlines the RF characterization methodology that is applied throughout this manuscript. The RF techniques presented here were originally developed for room-temperature characterizations, but the specific challenges of cryogenic measurement setups have also been addressed, demonstrating how these methodologies are adapted to remain valid at cryogenic temperatures.

The device analyses in the following sections will be based on the models and approaches introduced in this chapter, providing a solid foundation for the characterization and understanding of devices across a wide temperature range, including down to cryogenic levels.

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Chapter 3

Passive device characterization

Contents

3.1 Introduction

In the field of quantum computing, both passive and active devices play critical roles. Specifically, within the context of qubit readout systems, illustrated in Figure 3.1 (Left), Low Noise Amplifiers (LNAs) are crucial for amplifying qubit signals while minimizing noise addition. Cryogenic applications necessitate careful selection of LNAs to maintain low noise levels. Among the LNAs studied for such applications [Cag+23; PRC21; Lin+22], Figure 3.1 (Right) presents one design, incorporating three inductors. They are used for the input adaptation and to broad the LNA bandwidth.

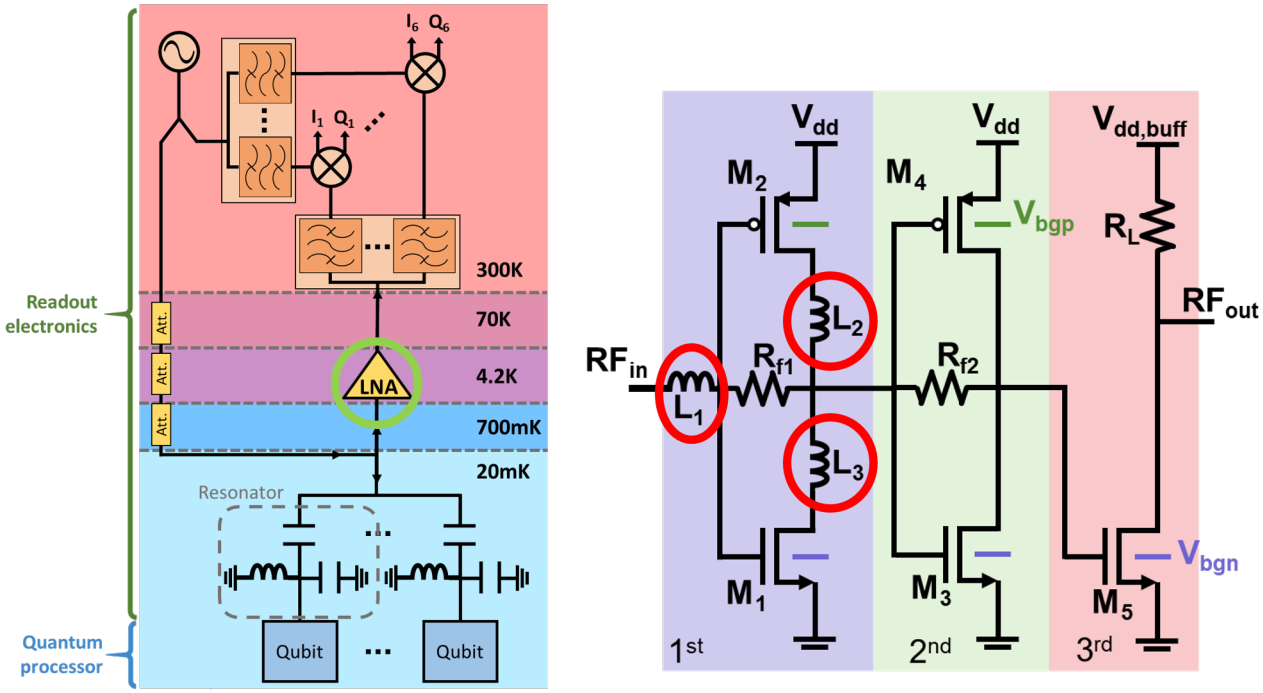


Figure 3.1: (Left) Qubit read out system. (Right) Design of one LNA to replace the LNA in qubit read out system.

In the field RF electronics, passive devices such as inductors are indispensable components for a multitude of functions, including filtering and impedance matching in low-noise amplifiers (LNA). These devices exert a direct influence on the performance of RF circuits, affecting such key parameters as signal integrity, power handling, and frequency response. As radio frequency (RF) systems operate at increasingly higher frequencies, the selection of an appropriate substrate and the design of these passive components become critical to maintaining efficiency and reducing unwanted losses.

The substrate, which serves as the supporting layer for these devices, plays a crucial role in their performance. The material properties of the substrate exert a considerable influence on the electro-

magnetic behaviour of passive devices, affecting both signal transmission and energy dissipation. An appropriate substrate can result in decreased signal loss, increased passive device performance, and enhanced circuit reliability, particularly in high-frequency applications [LRL02].

To mitigate interference and signal degradation caused by the substrate, a common solution is the integration of a metal shield [YW99]. This shielding effectively reduces substrate losses and enhances signal isolation. The use of a metal shield provides a reliable means of maintaining the integrity of RF signals while allowing passive devices to function optimally, especially in densely packed environments. The influence of a metal shield is illustrated in figure 3.2.

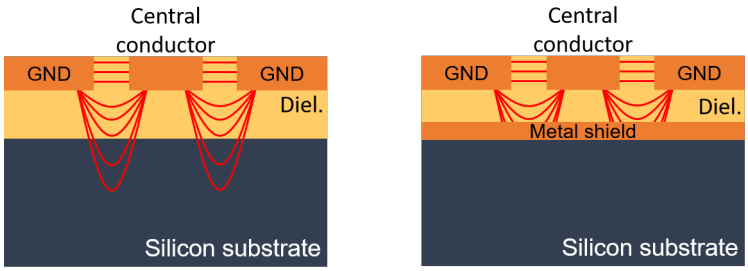


Figure 3.2: Cross section of a passive circuit with the electromagnetic field. (Left) directly on the substrate and (right) with a shield.

It appears that the issue observed at room temperature is related to the low resistivity of the doped silicon substrate, which is doped at $10^{15}\,\mathrm{cm}^{-3}$. This low resistivity leads to significant dielectric loss. As discussed earlier in Chapter 1, silicon dopant freeze out at low temperatures, which causes a substantial increase in the substrate resistivity and consequently reduces its dielectric losses.

The objective of this chapter is to determine whether a standard SOI substrate can achieve similar performance to that of a shielded substrate at cryogenic temperatures. If the standard substrate is performant at cryogenic temperature, the metalic shield can be removed and it allows the passive device to be designed on more metallic layer to reduce their resistivity and losses. To begin, a shielded inductor is measured and modeled over a temperature range from 300K down to 4.2K, establishing a reference for the analysis. Following this, the results of inductance measurements on various substrates are presented and analyzed. Finally, a comparative evaluation of the performance between the different substrates is provided.

3.2 Shielded inductors

3.2.1 Measured inductors

3.2.1.1 Inductor description

Inductors are fabricated using the last two levels of metal (top copper metal and alucap) available in the Back-end-of-Line (BEOL) of the 28nm-FDSOI technology, comprising a total of 11 levels of metal. All inductors are protected from the substrate impact by a shield in the lowest metal level, designated M1. The top copper metal is 880 nm thick and the alucap is 2155 nm thick. The design and the cross-section of the studied inductor are presented in figure 3.3

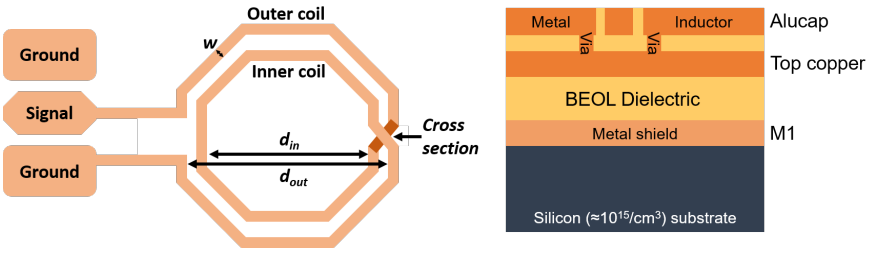


Figure 3.3: (Left) octagonal inductor design where d_{in} and d_{out} are the inner and outer coil diameter respectively and w is the coil width. (Right) Schematic cross-section of the shielded inductors

We have measured 18 octagonal spiral inductors with different numbers of turns n, metal track widths w and inner diameters d_{in}. The different geometry allows to have different value of inductance and different operating frequency. The geometry and the measurements of all the inductors are summarised in appendix A. In this section the results are presented for one inductance with the dimension presented in table 3.1.

Number of turn n	Inner diameter d_{in}	Metal track width w	Operating frequency
2	232 μm	17 μm	Around 3 GHz

Table 3.1: Parameters of the presented inductor.

3.2.1.2 RF measurement results

1-port S-parameters measurement were performed between 100 MHz and 20 GHz. For this study, 1-port measurement are performed because on inductor it allows to extracted their performance with the quality factor and it is a silicon surface gain. Note that in this 1-port configuration, the inductor output is short-circuited to the ground. We have additionally used on-wafer open and short structures close to inductors, to de-embed the access parasitic (pads and interconnect) from the raw measurements.

Figure 3.4 shows the inductance value, defined as $L = \frac{Im(Z_{11})}{\omega}$ where $\omega = 2\pi f$, as a function of the frequency f, for different temperatures ranging from 300 K down to 4.2K, and the corresponding quality factor, $Q = \frac{|Im(Z_{11})|}{Re(Z_{11})}$.

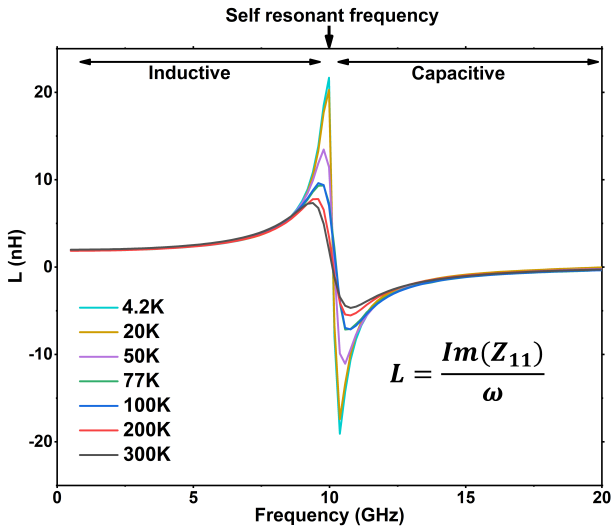


Figure 3.4: Inductance L measured vs frequency for different temperatures from 300K down to 4.2K. (here d_{in}=237.6 μm, w=13.95 μm and n=2).

As expected and for all the temperature, the device exhibits inductive characteristics at low frequencies, transitioning to capacitive behavior at high frequencies, specifically after reaching the Self Resonant Frequency (SRF), which occurs around 10 GHz in this case. Figure 3.5 provides a detailed view of the measured inductance values.

The extreme values of the inductance L at both low and high frequencies remain constant across different temperatures. A 7% variation in inductance at these frequency extremes is observed, which can be attributed to measurement uncertainties. These uncertainties arise due to the manual operation of the cryogenic prober, leading to variability in contact quality and pad degradation between measurements. Additionally, the calibration and de-embedding processes, which are performed at each measurement temperature, introduce further uncertainty. The most significant difference is observed around the self-resonant frequency (see Figure 3.5). While the resonance occurs at the same frequency

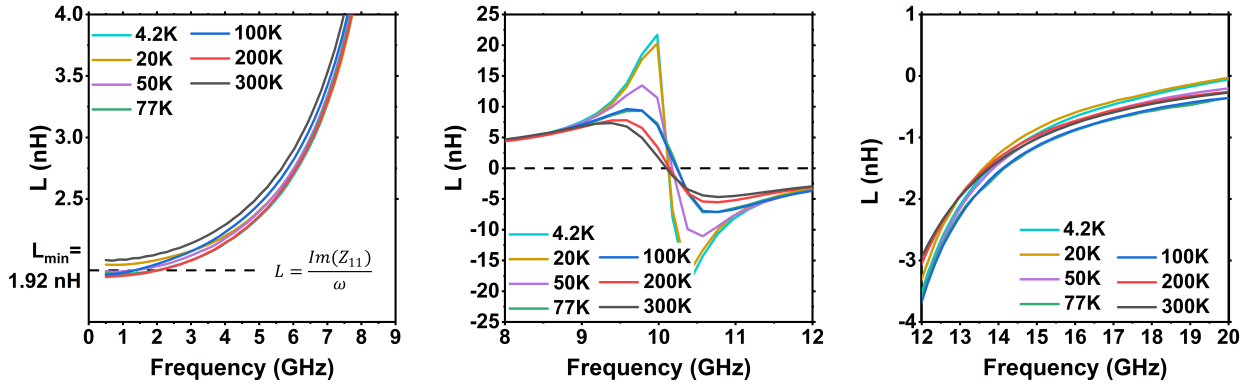


Figure 3.5: Zoom on the inductance L vs f curve shown in Figure 3.4 for different frequency ranges: (Left) low frequency, (Middle) around self-resonance, and (Right) at "high" frequency well above resonance.

regardless of temperature, the inductance value around this frequency increases by a factor of 3 when comparing measurements at 300K and 4.2K. This increase at low temperatures is due to the reduced resistivity of the metal track at low temperatures [Pat+20].

An inductor is often used for input or output matching in circuits or to enhance bandwidth. The objective is to introduce an imaginary impedance while minimizing losses, which corresponds to keeping the real impedance as low as possible. To assess the performance of the inductor, the quality factor Q, defined as $Q = \frac{|Im(Z_{in})|}{Re(Z_{in})}$, is measured. Figure 3.6 illustrates the quality factor of the inductor under study.

The frequency at which the quality factor is maximum defines the frequency where the inductor is the most efficient. The maximum of Q for a two-turn inductor with d_{in} = 237.6 μm, w = 13.95 μm is found at f_{Qmax} = 3.9 GHz regardless of the temperature (Figure 3.6 (left)). This frequency value is to be expected due to the dimensions of the inductor and remains constant because it is mainly dependent on the parasitic capacitances [Par+98]. In figure 3.6 (right), we also observed that this maximum increases from 15 at 300 K to roughly 70 at 4.2 K. This increase is advantageous for an inductor because it allows for a reduction in the losses of the inductor and the circuit in which it is integrated. This increased at low temperature is due to the reduction of the metal track resistivity at low temperature [Pat+20].

In the following, we propose and discuss models to describe and analyse DC and frequency behaviour of our spiral inductors at low temperature.

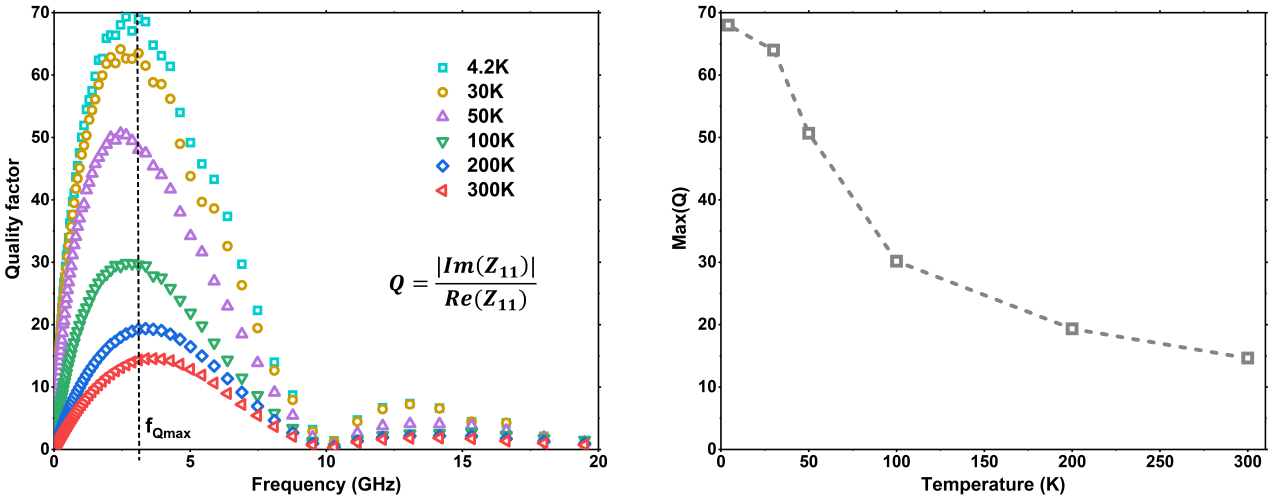


Figure 3.6: (Left) quality factor Q vs frequency, for different temperatures from 300K down to 4.2K. (Right) quality factor maximum as a temperature function.

3.2.2 Proposed model

In this section, the inductor is modeled with Figure 3.7.

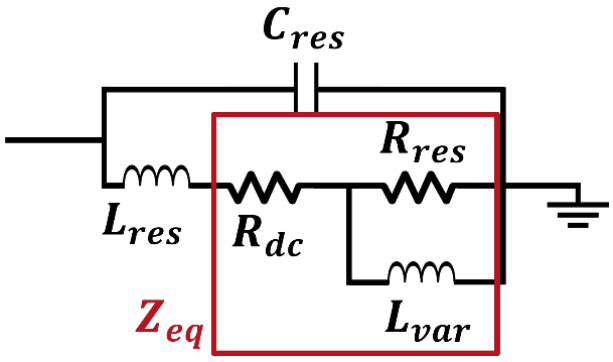


Figure 3.7: Studied RF model for the inductors inspired by [Cao+03]. RLC circuit is used to describe the self-resonance behaviour. R_{res} and L_{var} modeled the skin effect.

Figure 3.7 represents the RF model taken from [Cao+03]. It is composed of one main R_{dc} L_{res} C_{res} loop describing the self-resonant behavior, and one R_{res} L_{var} loop for coil proximity effect, and the skin effect. L_{res} and R_{dc} represent the main inductance and the DC resistance introduced by the metal track. C_{res} corresponds to the parasitic capacitance in the device such as the capacitance between the different metals tracks and to the pattern ground shield. Z_{eq} is a frequency dependent impedance to model the skin effect and the proximity effect.

This model has five lumped elements which correspond to five freedom degrees to fit the measurement. Our objective is to evaluate the value of the lumped elements based on the dimensions of the inductor, aiming to minimize the number of arbitrary fitting parameters available. Our focus centered on determining the inductance value at low frequencies, as well as evaluating the values of parasitic capacitance and metal track resistance.

3.2.2.1 Value of the inductance at low frequency L_{LF}

In the equivalent circuit, the value of the inductance at low frequency correspond to $L_{res} + L_{var}$. This value is expressed theoretically by the modified Wheeler formula [Moh+99; Whe28]:

$$L_{DC,theo} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \delta} \tag{3.1}$$

Where $d_{avg} = 0.5(d_{out} + d_{in})$ is the average diameter, d_{in} and d_{out} are respectively the inner and outer diameter of the inductor (see Figure 3.3), $\delta = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}$ is the fill ratio, $\mu_0 = 4\pi \times 10^{-7} H.m^{-1}$ is the magnetic permability of free space, n is the coil number of turns and K_1 and K_2 are layout dependent coefficients and they are arbitrary fixed to fit the curve. For the characterized octagonal inductor (d_{in}=237.6 μm, w=13.95 μm and n=2), $K_1 = 2.1$ and $K_2 = 3.55$ are used. The inductance value as a temperature function is presented in figure 3.8.

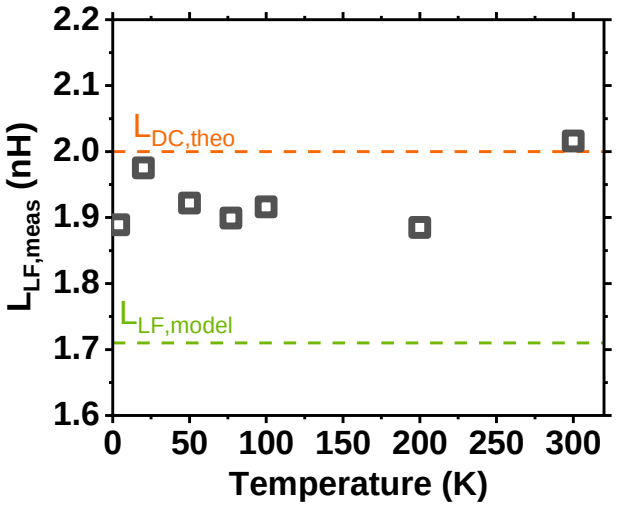


Figure 3.8: Inductance L measured at low frequency (f=500 MHz) as a function of the temperature (here d_{in}=237.6 μm, w=13.95 μm and n=2). The dash lines represents the DC theoretical value of the inductance calculated in with the modified wheeler formula and the low frequency value of the modeled inductance presented in section 3.2.3.1

The inductance value found by calculation is in good agreement with the measurement.The small discrepancy comes from the accuracy of the measurements.

In this section, by using the wheeler formula, $L_{DC,theo} = L_{res} + L_{var}$ is calculated and the number of unknown lumped elements in the model is reduced by one.

3.2.2.2 Value of the parasitic capacitance

The value of the capacitance C_{res} has been calculated with the 2D capacitance equations from reference [WLM00]. The distribution of the different parasitic capacitances and the corresponding equivalent circuit used for the calculation of C_{res} for the measured inductors are presented in Figure 3.9.

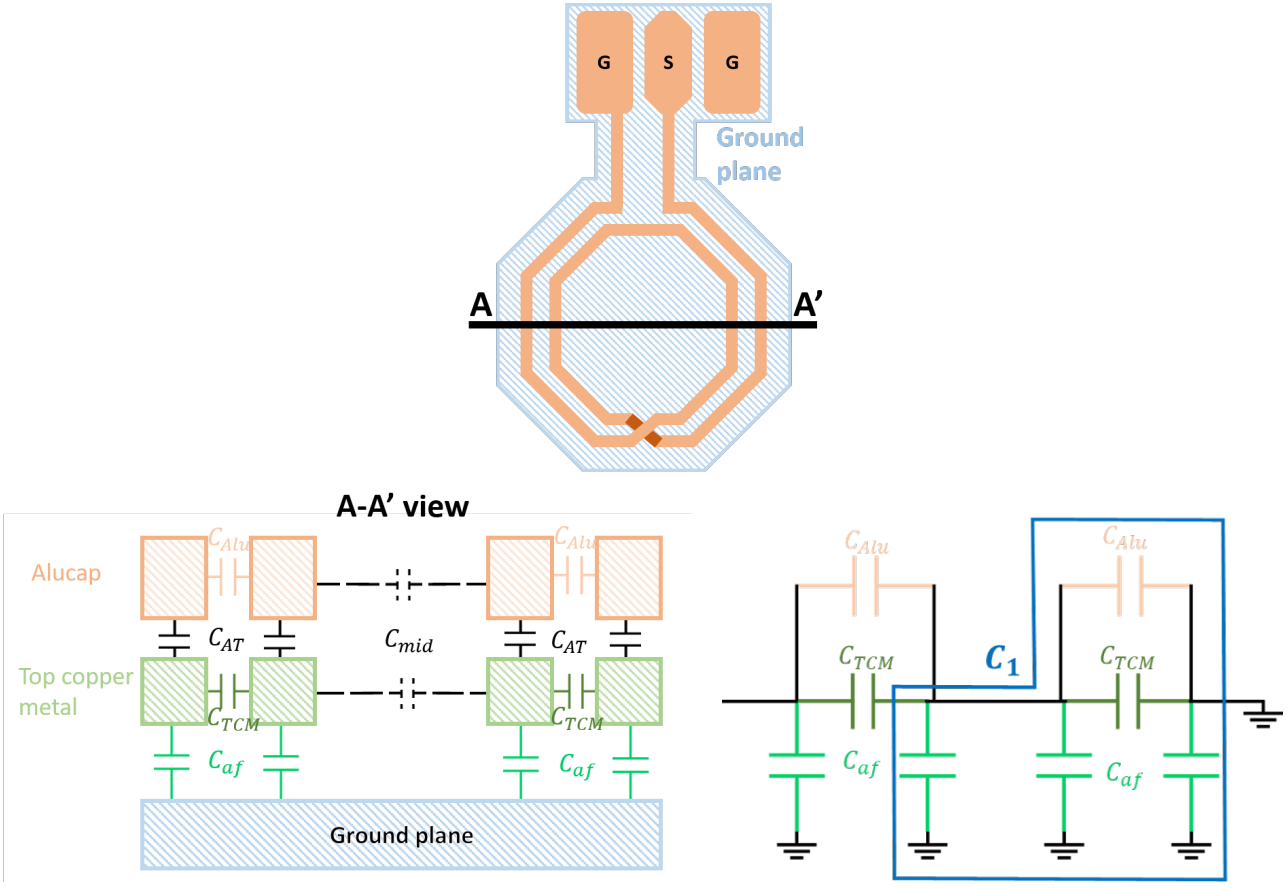


Figure 3.9: (Top) Inductor top view with the ground plane and the line of the cross section represented. (Bottom left) cross section of the inductor with the parasitic capacitance distribution. (Bottom right) Equivalent circuit of all the parasitic capacitances of the inductors

The capacitances C_{mid} are neglected because the inner diameter of the inductor is large enough. The capacitance C_{AT} are short-circuited by some vias. We finally obtain the following formula:

$$C_{res,theo} = C_{af} + \frac{C_1 \times (C_{TCM} + C_{Alu})}{C_1 + C_{TCM} + C_{Alu}} \tag{3.2}$$

$$with \quad C_1 = C_{TCM} + 2C_{af} + C_{Alu} \tag{3.3}$$

The value calculated for the studied inductors is $C_{res,theo}$=0.13 pF and it reduces the number of lumped element arbitrary fixed.

3.2.3 Metal resistivity and frequency dependence

The capacitance C_{res} and the inductance L_{res} and L_{var} do not vary with the temperature, since they mainly depend on the inductor geometrical dimensions. On the other hand, R_{dc} decreases with temperature from 1.72 Ω to 0.15 Ω as expected and presented in [Dut14]. This resistance reduction, due to electron mobility increase [Dut14], is the main contributor of the difference between the 300 K and 4.2 K results (Figure 3.6). Moreover, the skin depth and the skin effect are directly dependent on the metal resistivity (see chapter 2 and [Whe42]). According to [Pat+20], when the frequency effect can not be neglected, the inductors resistance is proportional to the square root of the material resistivity $\sqrt{\rho}$. The current density distribution, and so the frequency dependent resistance, also depend on the temperature. Figure 3.10 present the simulation results for the real part of Z_{eq} and a comparison to see the imaginary part introduce by Z_{eq} compared to $L_{res}\omega$.

Figure 3.10 (Left) illustrates the variation of the effective resistance $R_{eq} = Re(Z_{eq})$, which arises from R_{dc}, L_{var}, and R_{res}. The corresponding formula is provided in equation (3.4). As the frequency increases, the skin depth reduces, resulting in an increase in resistance. Therefore, as the temperature decreases, $Re(Z_{eq})$ decreases due to the drop in the metal resistivity.

$$R_{\text{eq}} = \text{Re}(Z_{\text{eq}}) = R_{\text{dc}} + \frac{R_{\text{res}} L_{\text{var}}^2 \omega^2}{R_{\text{res}}^2 + L_{\text{var}}^2 \omega^2} \tag{3.4}$$

Figure 3.10 (Right) presents the contributions of $L_{\text{res}}\omega$ and $\text{Im}(Z_{\text{eq}})$ to the imaginary part of Z_{11} at ambient temperature. The equation of Z_{11} is given in 3.5. The formula for the imaginary part of Z_{eq} is given in equation (3.6). This figure shows that the imaginary part introduced by the inductance L_{var} and the resistance R_{res} is negligible compared to the imaginary part of the inductance L_{res} (which is $L_{\text{res}}\omega$). This observation holds true at all measurement temperatures and is consistent with the skin effect which make the resistance increases with the frequency.

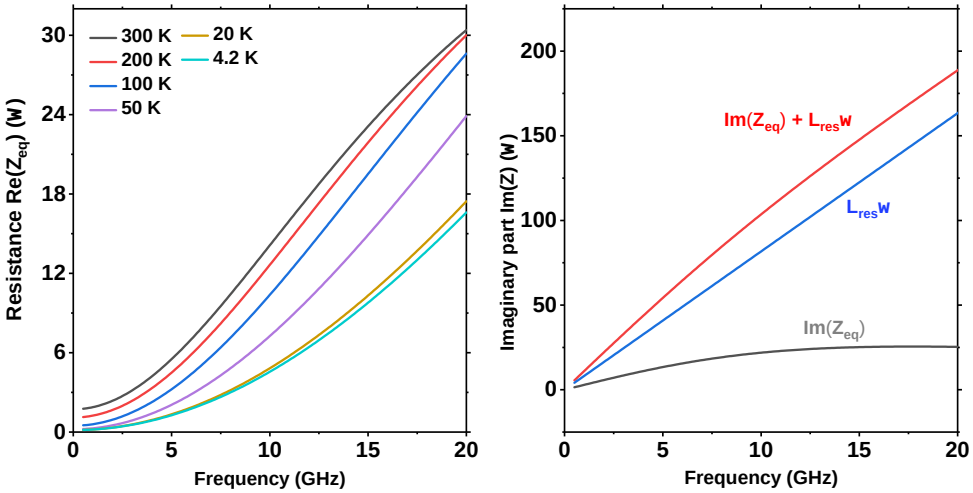


Figure 3.10: (Left) Effective resistance introduced by the skin effect modelled by R_{dc}, L_{var} and R_{res} as a function of frequency. (Right) Contribution of $L_{res}\omega$ and $Im(Z_{eq})$ to the imaginary part of Z_{11} at 300 K

$$Z_{11} = (jL_{res}\omega + Z_{eq}) \parallel \frac{1}{jC_{res}\omega} = \frac{jL_{res}\omega + Z_{eq}}{1 + jZ_{eq}C_{res}\omega - L_{res}C_{res}\omega^2} \tag{3.5}$$

$$\mathrm{Im}(Z_{\mathrm{eq}}) = \frac{R_{\mathrm{res}}^2 L_{\mathrm{var}}\omega}{R_{\mathrm{res}}^2 + L_{\mathrm{var}}^2\omega^2} \tag{3.6}$$

To understand more precisely the variation of the resistivity of the top copper metal and alucap used in the inductor, we have performed DC measurements from 4.2K to 300K, as shown in Figure 3.11. A low DC power have been used to avoid the line self-heating, and we have performed a four-point probe measurement to avoid contact resistance. The resistivity linearly increases with the temperature between 50K and 300K as shown in Figure 3.11 (Right) and as expected for a metal [Mat79]. This linearity can be used for modelling, with the temperature coefficient of alucap and top copper line determined by fit. In the graph, around 300K temperature coefficient is $\alpha_0 = \frac{0.07}{\rho_{300K}} = 3.75 \times 10^{-3} K^{-1}$ for aluminium and $\alpha_0 = \frac{0.07}{\rho_{300K}} = 3.18 \times 10^{-3} K^{-1}$ for copper. These value are consistent with the literature for a metal [Mat79]. Below 50K, the decrease in resistivity saturates because electron-phonon scattering has been fully suppressed [VF74]. The observation are the same with the DC resistance of the inductor. The DC resistance extracted with this method is integrated in the model of section 3.2.2, its value is presented in Table 3.2.

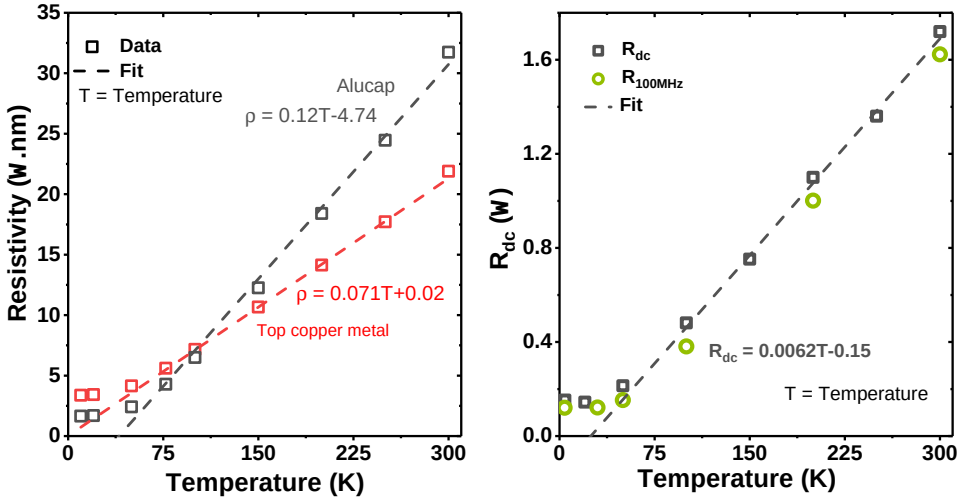


Figure 3.11: (Left) DC resistivity of top copper metal and alucap as a function of temperature and (Right) DC and low frequency resistance of the studied inductor (stack of both metals).

3.2.3.1 Comparison with the experimental Z-parameters

We fitted the experimental $Re(Z_{11})$ and $Im(Z_{11})$ with the model of Figure 9 using C_{res}, L_{res}, R_{res}, and L_{var} as fitting parameters, for each temperature (see values presented in Table 3.2). The DC resistance R_{DC} value is extracted from DC measurements presented in section III.c. The value of the capacitance C_{res} and $L_{res} + L_{var}$ are first set to the value obtained from the previous equations. and then modified to increase the accuracy of the fit. The fit is performed on ADS software. We found good agreement between the model and the measurements as shown in Figure 3.12.

Temperature	300K	200K	100K	50K	20K	4K
C_{res}	0.145 pF	0.145 pF	0.145 pF	0.145 pF	0.145 pF	0.145 pF
L_{res}	1.25 nH	1.25 nH	1.25 nH	1.25 nH	1.25 nH	1.25 nH
R_{res}	51 Ω	58 Ω	73 Ω	111 Ω	174 Ω	185 Ω
L_{var}	0.46 nH	0.46 nH	0.46 nH	0.46 nH	0.46 nH	0.46 nH
R_{dc}	1.72 Ω	1.10 Ω	0.48 Ω	0.21 Ω	0.15 Ω	0.15 Ω

Table 3.2: Model parameters extraction based on measurement.

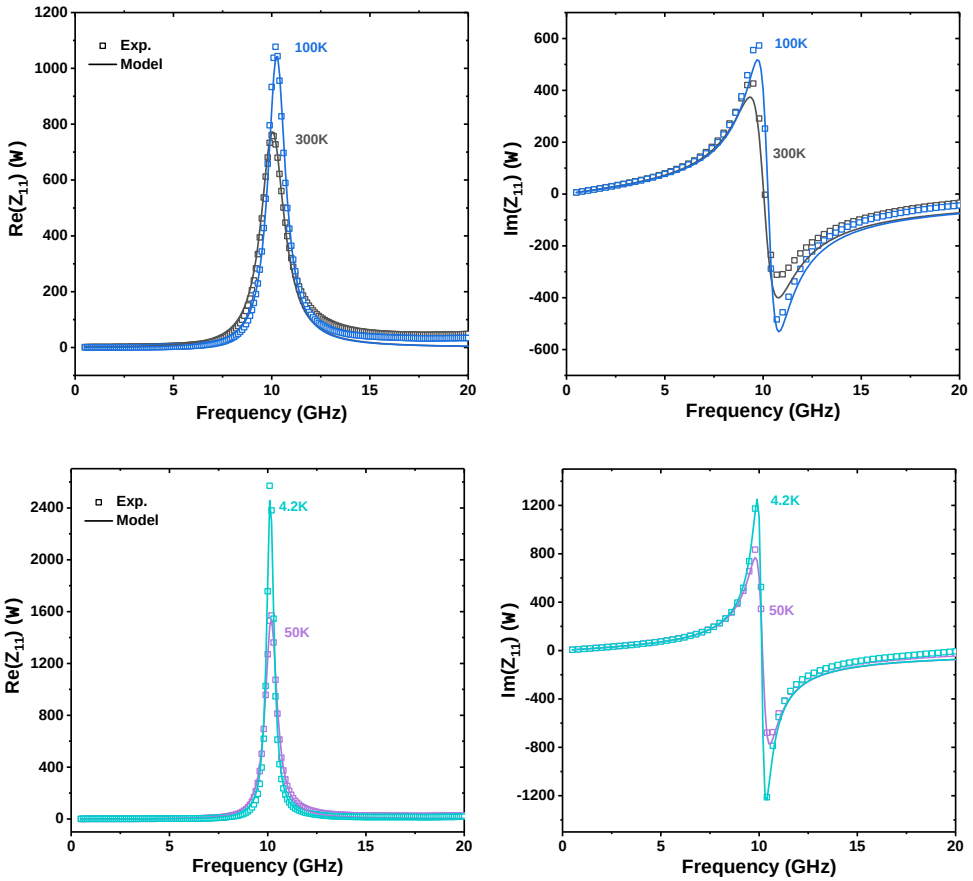


Figure 3.12: Real and imaginary part of Z_{11} for our inductor at 300K, 100K (Top), 50K and at 4.2K (Bottom). Measurements (dot) and model (line).

In this work, we presented the RF characterization of an inductors operating at cryogenic temperatures up to 20 GHz. A corresponding RLC model was proposed and validated across a range of temperatures, from ambient to cryogenic conditions. Within this model, the primary temperature dependence was attributed to the variation in metal resistivity. Specifically, we observed that the quality factor increases significantly between 300K and 50K, while below 50K, the increase becomes less pronounced due to the saturation of metal resistivity. As the resistivity of the metal decreases at cryogenic temperatures, the losses introduced by the metal tracks in passive devices are reduced, demonstrating the potential of cryoelectronics using conventional CMOS processes and materials.

3.3 Substrate performances at cryogenic temperature

3.3.1 Introduction

3.3.1.1 The different RF substrate studied

The substrate is an important part of the electromagnetic environment of passive and active RF devices, as it can be responsible for significant losses, coupling and non-linearity when its nominal resistivity is low [Ras22]. For these reasons, high-resistivity (HR) substrates with ultra-low residual dopant concentration ($\sim 10^{12}$ at.cm^{-3} vs. $\sim 10^{15}$ for standard) are preferred for silicon RF applications [Gia+08]. Despite the clear improvement of RF metrics over standard substrates, HR performance is ultimately limited by a parasitic surface conduction (PSC) related to the compensation of a finite charge density within the dielectric above [Wu+99]. In the case of Partially-Depleted SOI (PDSOI), the introduction of a Poly-Si Trap-Rich (TR) layer underneath the buried oxide has enabled alleviating markedly the effects of PSC by trapping free carriers [Esf+17]. Emerging needs for cryogenic RF Integrated Circuits in the frame of aerospace electronics or quantum computing spark interest towards studying the impact and behavior of substrates at low temperatures. Cryogenic characterization of passive components above a bare HR-Si substrate was carried out in [Kru+06], though this configuration is not representative of a standard IC with BEOL dielectrics and interconnects. To our knowledge, this is the first systematic comparison of standard, HR and TR Si substrates across a 300K-7K temperature range based on the quality factors of BEOL-embedded inductors.

3.3.1.2 Parasitic Surface Conduction

In the context of RF systems that employ silicon-on-insulator (SOI) substrates, parasitic surface conduction (PSC represents a significant challenge, largely due to the layered structure inherent to SOI technology [Led+06; LR08]. The insulating layer, which separates the active semiconductor, offers advantages such as reduced parasitic capacitance and improved isolation between devices. However, it can also lead to surface conduction issues along the interface between the silicon and the insulating layers.

A fixed charge in the dielectric (usually > 0 and with density in the $10^{10} - 10^{12}\,\mathrm{cm}^{-2}$ range [Mou+22; Mou+23]) causes the formation of a surface inversion layer in the substrate with high concentrations of free electrons, extending as deep as the p type Silicon is lowly-doped. Thus, though the same effect occurs on standard and HR substrates, the depletion depths differ by roughly two orders of magnitude as presented in the figure 3.13

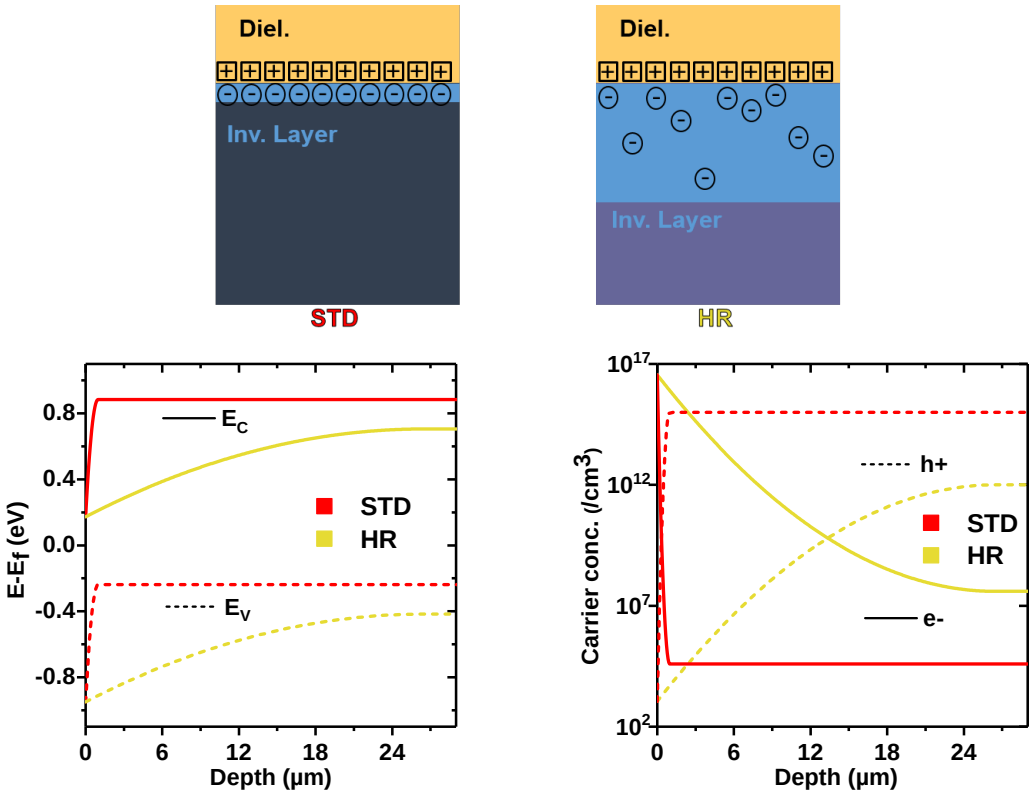


Figure 3.13: Parasitic Surface Conduction (PSC) occurs to compensate dielectric charges. Lowly-doped HR substrates are typically more affected than STD (left) simplified sketch; (right) calculated energy band diagrams and free carrier concentrations at 300K).

The aforementioned parasitic surface have a detrimental impact on RF performance, leading to the reduction of the substrate resistivity and increase substrate losses and a reduction in the effectiveness of passive components such as inductors and capacitors [Gam+99; Sek+15].

To mitigate parasitic surface conduction in RF SOI substrates, techniques such as the implementation of a trap-rich layer on top of the HR substrate has been develop [LR08]. Trap-rich substrates introduce a high-density layer of defect sites—"traps"—within the substrate, which act to capture and neutralize free carriers that would otherwise contribute to parasitic conduction. These trap-rich layers significantly increase the substrate effective resistivity which reduce the substrate losses and enhance the passive device performances.

This section is dedicated to the RF characterization of inductor on three different substrate : Standard substrate (doped at $10^{-15}cm^{-3}$), High-resistivity (HR) substrate (doped at $10^{-12}cm^{-3}$) and HR substrate with a trap-rich layer. As mentioned in the chapter 1 and in [Bec21], the silicon freeze at cryogenic temperature leading to an increase of its resistivity. If the substrate resistivity increase, the substrate losses are lower and therefore the passive device performance are enhance. The goal of this study is to see if the performance ranking between substrates, well known at 300K, remains the same

in cryogenic conditions.

3.3.2 Measured devices

The tested devices are inductors designed for 5GHz operation, and integrated on top of three types of substrates: 10 Ω·cm (STD), ∼5k Ω·cm (HR), and ∼5k Ω·cm with a top 200nm thick layer of Trap-Rich (TR) Poly-Si. All these different substrates are illustrated in Figure 3.14.

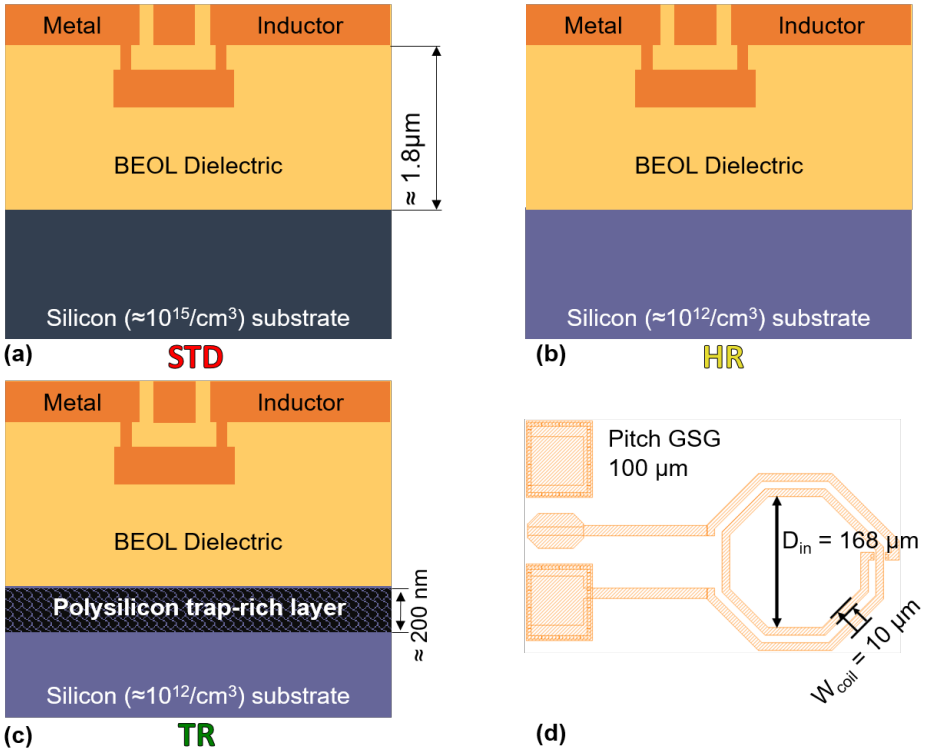


Figure 3.14: Schematic cross-sections of the tested two-level inductor on (a) standard (STD), (b) High Resistivity (HR) and (c) HR with Trap-Rich (TR) substrates. (d) Inductor layout and dimensions.

From RF S-parameter measurements on the Vector Network Analyzer we extracted a complex impedance Z_{in}. The inductance figures of merit are extracted from this impedance as a function of the frequency f using the three following equations (as for the shielded inductors):

$$Q = \frac{\text{Im}(Z_{\text{in}})}{\text{Re}(Z_{\text{in}})} \tag{3.7}$$

3.3.3 Quality factor analysis

3.3.3.1 Quality factor variation explanation

In this section, the resistance associated with the metal track is denoted as R_{ind}, while the resistance related to the substrate is referred to as R_{sub}. Figure 3.15 qualitatively illustrates the expected evolution of $Q(f)$ characteristics with varying resistive components [Liu+17; Jen+01].

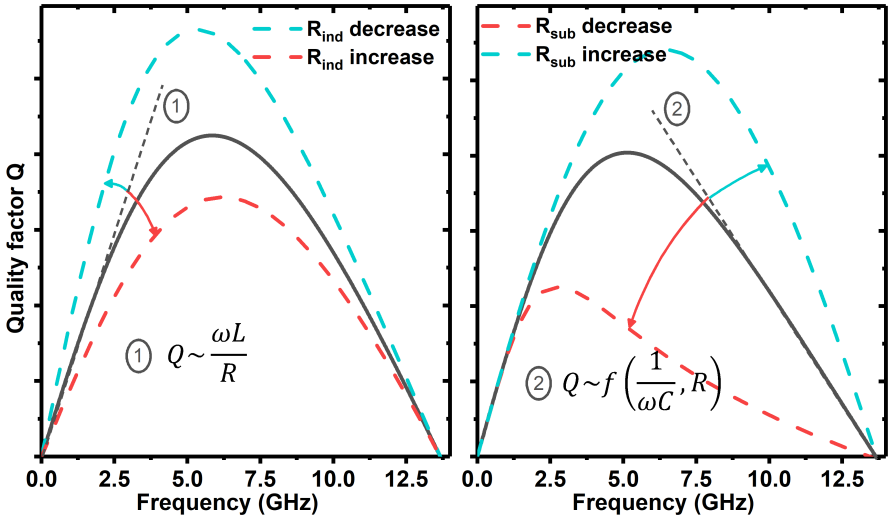


Figure 3.15: Expected qualitative variations of $Q(f)$ characteristics. R_{ind} acts on the steepness of the slope left of the peak, whereas R_{sub} impacts the slope right of the peak.

Relative to the peak, the left-hand side (LHS) slope is primarily influenced by R_{ind}, becoming more abrupt as R_{ind} decreases. Conversely, the right-hand side (RHS) slope is influenced by R_{Sub}, becoming more abrupt if R_{Sub} increases. We use this framework in the analysis that follows.

3.3.3.2 Quality factor measurements

The quality factors Q extracted as a function of the frequency on all our substrates and for different temperatures are presented in Figure 3.16.

The characteristics of all substrates show the left hand side slope increasing down to 50K, in agreement with figure 3.15 indicating that R_{ind} decreases down to 50K. This means that the increase in maximum quality factor is partly attributable to this phenomenon down to 50K.

For the standard substrate (Figure 3.16 (a)), as the temperature drops below 50K, the right-hand side (RHS) slope becomes steeper, indicating a sharp increase in R_{Sub} and a significant improvement in the quality factor. This transition is also observed, though to a lesser extent, on the Trap-Rich substrate (Figure 3.16 (c)). However, on the High-Resistivity (HR) substrate (Figure 3.16 (b)), this transition

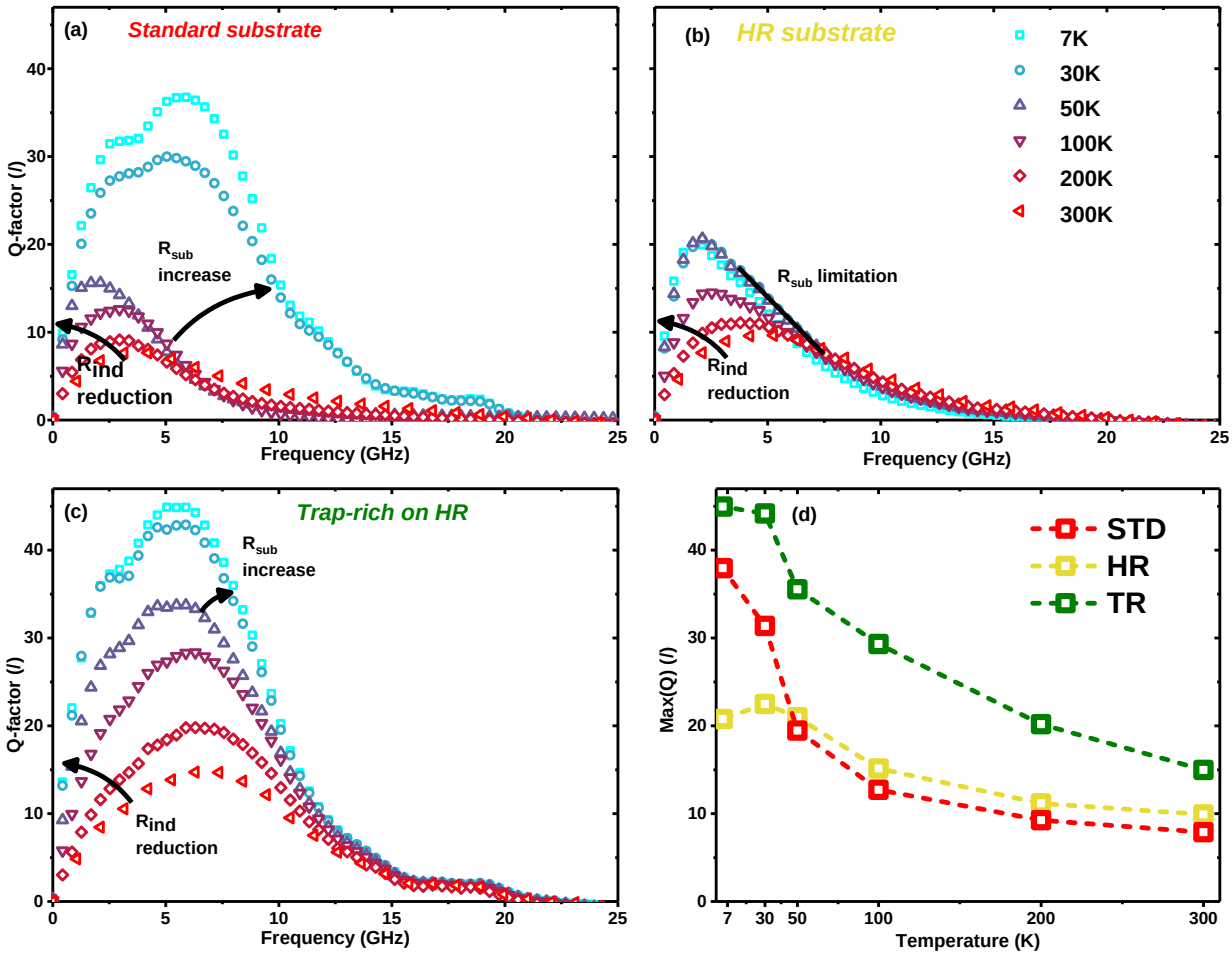


Figure 3.16: (a, b, c) Quality factor extracted as a function of frequency from 300K down to 7K on all substrates. The lower frequency behavior is consistent with R_{ind} decreasing. The observed trend for f>5GHz indicates a sharp increase in substrate resistance (R_{sub}) at T<50K. (d) Quality factor maximum as a temperature function for all substrates.

is not apparent, with $Q_{\max}$ at 7K remaining limited to approximately half of the corresponding value observed on the standard substrate. The temperature dependence of the quality factor maximum is summarized in figure 3.16 (d).

3.3.3.3 Resistance variation

In this section, we make the difference between the bulk substrate resistance (called R_{bulk}) which is the substrate resistance at depth and the PSC resistance (called R_{PSC}) which is the resistance introduce by the parasitic surface conduction at the interface.

As the Fermi level crosses the ionization energy of dopants (approximately 45meV above the va-

lence band for boron in Si [Kit57]), the concentration of available carriers in the substrate is expected to sharply drop, causing a dramatic increase in R_{bulk}, otherwise known as "substrate freeze-out". The standard and HR substrates have dopant concentrations of 10^{15} cm^{-3} and 10^{12} cm^{-3} respectively, this transition should occur between 50K and 30K for both types according to our calculations (Figure 3.17).

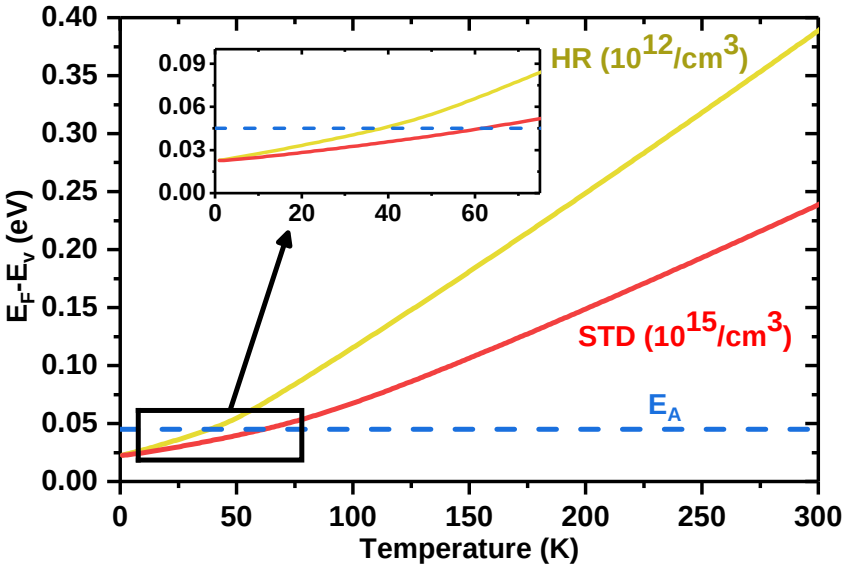


Figure 3.17: Calculated Fermi-level energy vs. temperature, for HR-like and STD-like substrate doping levels, with incomplete ionization at low T (E_A ≈45meV for B in Si). Both substrate types are expected to freeze between 50 and 30K.

At 300K, based on the free carriers depth profiles (cf. Figure 3.13), we could estimate that the PSC resistance of the HR substrate is orders of magnitude lower than the standard substrate PSC resistance. Accounting for the substrate thickness and its dopant concentration, the standard substrate bulk resistance is lower than the HR PSC resistance whereas the HR bulk resistance is the largest of all resistive components: ($R_{\text{bulk,HR}} \gg R_{\text{PSC,STD}} \gg R_{\text{PSC,HR}} > R_{\text{bulk,STD}}$). At low temperature in first approximation, R_{PSC} can be expected to decrease between 2 and 20 times (depending on acceptor concentration [MM54]) due to the larger electron mobility alone, whereas R_{bulk} diverges past T_{freeze}. The trends on R_{Sub} components can be visualized in Figure 3.18 by following the floor, i.e., $\min(R_{\text{PSC}}, R_{\text{STD}})$ for each substrate. This semi-quantitative analysis explains the observed Q-factor trends on STD vs. HR, namely sudden R_{Sub} variation due to substrate freeze-out and lack thereof.

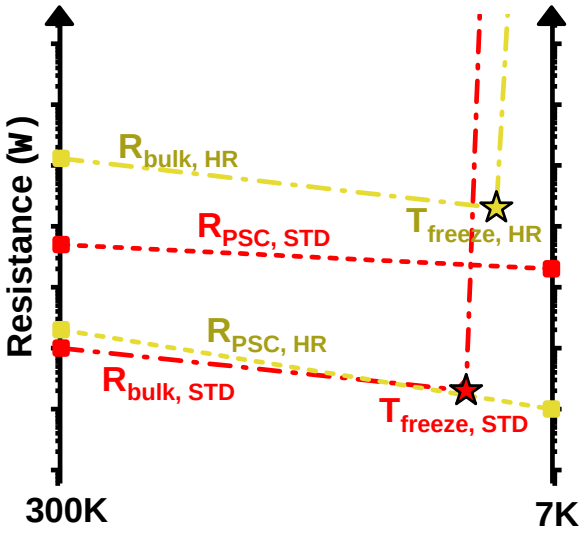


Figure 3.18: Semi-quantitative R_{bulk} and R_{PSC} evolution with temperature for HR and STD substrates (300K values from free carrier concentration profiles cf. Fig. 3 values at low T estimated from carrier mobility dependence). While substrate freeze-out causes a change in the limiting resistance for STD, this is not the case for HR (R_{PSC} always limits the substrate response).

For the Trap-rich on HR substrate (Fig. 3.16 (c)), at a temperature lower than 50K, the RHS slope is no longer limited, and an increase in R_{Sub} can be observed. It is due to the fact that TR substrates tend to boost R_{PSC} through decreasing the carrier lifetime, while retaining the high value of $R_{\text{bulk,HR}}$. This results in a "looser" RHS slope modulation throughout the whole temperature range.

3.3.4 Model and parameters

To analyze these measurements, we propose to use the following model.

3.3.4.1 Model and Z-parameter fitting

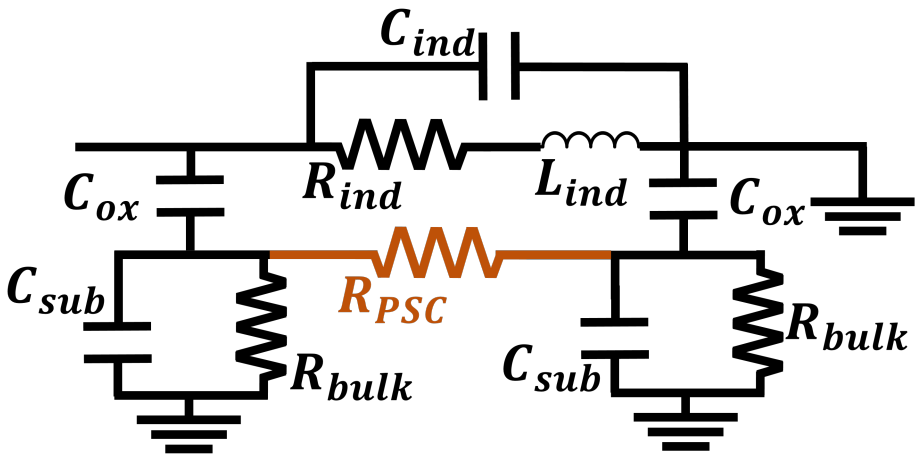
The frequency variations are fitted on $Re(Z_{in})$ and $Im(Z_{in})$ curves. Fitting requires an equivalent electrical model, in which we included the PSC resistance R_{PSC}, as shown in Figure 3.19.

With the previous model and as demonstrate in [Liu+17], we can define the substrate resistance and the quality factor as:

$$R_{\text{Sub}} = R_{\text{bulk}} \parallel R_{\text{PSC}} \tag{3.8}$$

$$Q = \frac{\omega(L_{\text{ind}} - \omega^2 L_{\text{ind}}^2 C_1 - C_1 R_{\text{ind}}^2)}{R_{\text{ind}} + R_{\text{ind}}^2 G_1 + \omega^2 L_{\text{ind}}^2 G_1} \tag{3.9}$$

where $C_1 = C_{ind} + C_{sub}$ and $G_1 = \frac{1}{R_{sub}}$



$$R_{Sub} = R_{bulk}//R_{PSC}$$

Figure 3.19: Equivalent RLC model for the inductor taken from [Liu+17].

The measured and fitted curves $\mathrm{Re}(Z_{\mathrm{in}})$ and $\mathrm{Im}(Z_{\mathrm{in}})$ versus frequency for all substrate types are shown in Fig. 4 at 300K and 7K, showing very good agreement. R_{ind} and L_{ind} are respectively determined from the values of $\mathrm{Re}(Z_{\mathrm{in}})$ and $\mathrm{Im}(Z_{\mathrm{in}})$ at low frequency, and C_{ox} is calculated from the device geometry.

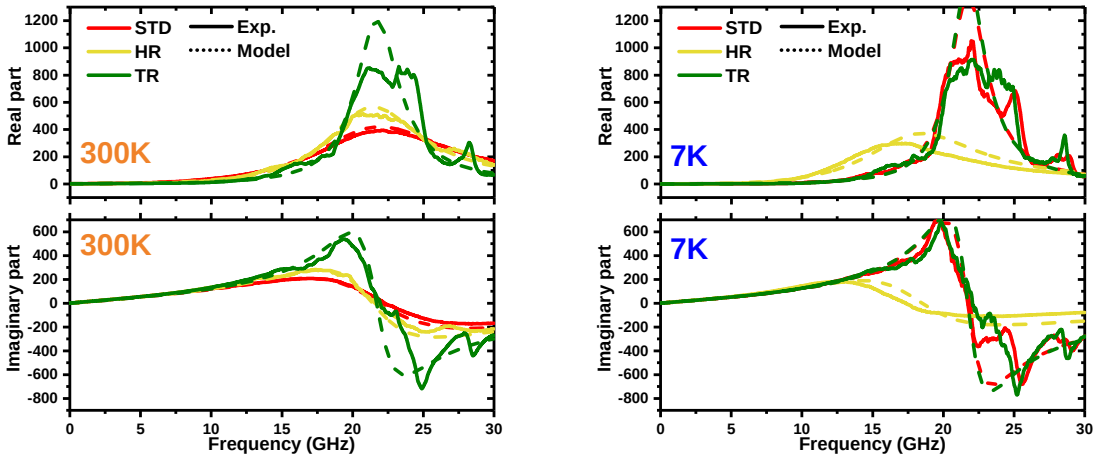


Figure 3.20: Measured and fitted complex impedance Z_{in} (top: real part, bottom: imaginary part) at 300K and 7K.

The total capacitance is adjusted near resonance, and the total resistance should reflect $|Z_{\mathrm{in}}|$ across the whole frequency span. The values of L and C parameters are independent of the temperature and the substrate type. In agreement with the literature [Ber+22], R_{ind} ($\approx$ R at 10MHz) was found to decrease linearly with temperature between 300K and 50K due to reduced phonon scattering, before

reaching a saturation (not shown). The R_{ind} values at every measurement temperature are also consistent between all substrates, validating the robustness of the measurement (calibration, contacts) and extraction methods. The last remaining parameter, $R_{\text{Sub}} = R_{\text{bulk}}//R_{\text{PSC}}$ should in principle change with both temperature and substrate type, impacting the $Q(f)$ behavior.

The lumped elements values used to fit the impedance curves are presented in table 3.3:

Temperature	300K	300K	300K	7K	7K	7K
Substrate	STD	HR	TR	STD	HR	TR
R_{ind}	2.08 Ω	2.08 Ω	2.08 Ω	0.3 Ω	0.3 Ω	0.3 Ω
L_{ind}	1.53 nH	1.53 nH	1.53 nH	1.53 nH	1.53 nH	1.53 nH
C_{ind}	29 fF	29 fF	29 fF	29 fF	29 fF	29 fF
C_{ox}	200 fF	200 fF	200 fF	200 fF	200 fF	200 fF
C_{sub}	7 fF	7 fF	7 fF	7 fF	7 fF	7 fF
R_{bulk}	400 Ω	1400 Ω	1400 Ω	1700 Ω	1700 Ω	1700 Ω
R_{PSC}	No PSC	900 Ω	No PSC	No PSC	600 Ω	No PSC

Table 3.3: Model parameters extraction to fit figure 3.20

As expected with the study of the quality factor in section 3.3.3, the main variation in the model are the resistance variation. First the metal track resistance decreases from 2.08Ω from 0.3Ω at cryogenic temperature due to the increase of the electron mobility [Dut14].At room temperature, the substrate bulk resistance of the standard substrate is lower due to the fact that dopant concentration is higher in comparison to the HR and TR substrates. The HR substrate is the only substrate where it is needed to add a PSC resistance to fit the measurements. At cryogenic temperature, the substrate bulk resistance increase due to the substrate freeze out leading to higher quality factor and performances.

To conclude, an increase in the maximum quality factor is observed across all inductors as the temperature decreases. This improvement is attributed to the reduction in metal resistivity at lower temperatures. Furthermore, for inductors on standard and trap-rich substrates, a sharp rise in the maximum quality factor is observed below 50K, which is linked to the substrate freeze-out effect. However, this effect is masked for high-resistivity (HR) substrates, likely due to the influence of parasitic surface conduction.

3.4 Conclusion

In conclusion, this chapter presented a detailed characterization of inductors with and without shields, emphasizing the impact of cryogenic temperatures on their performance. We demonstrated that at low temperatures, substrate freeze-out significantly reduces substrate losses, leading to a substantial improvement in the performance of shield-less inductors. However, the comparison between shielded and unshielded inductors remains complex due to differences in their dimensions and design, making it challenging to draw a definitive conclusion about their relative advantages. Nonetheless, for applications specifically targeting cryogenic environments, the findings suggest the potential to eliminate shields in future designs. This opens up opportunities to fabricate inductors with more metal layers, further reducing metal resistivity and enhancing overall performance.

Looking ahead, a promising avenue for future research would be the exploration of inductors designed with additional metal layers but without shields, to determine if even higher performance levels can be achieved.

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Chapter 4

RF transistor electrostatic characterization and model in 28FDSOI technology

Contents

4.1 Introduction

In the preceding chapter, we outlined the key characteristics of passive RF circuits under cryogenic conditions. In this chapter, we will shift our focus to the active components. The behavior of transistors at cryogenic temperatures is of critical importance, particularly in LNA circuits where they are the main noise and gain contributor. The following chapter examines the RF characterization of transistors operating at cryogenic temperatures and focuses on the electrostatic behavior.

As describe before, the 28 FD-SOI technology has been chosen due to its low variability, low consumption and the control of threshold voltage with the back-gate bias.

Figure 4.1 presents a cross-section of an NMOS and a PMOS in FD-SOI technology . As discussed in Chapter 1, the FD-SOI technology features a thin buried oxide layer, which enables the application of a voltage at the back of the silicon layer. This configuration allows for more precise control over the formation or suppression of a channel, compared to bulk transistors [CDC20].

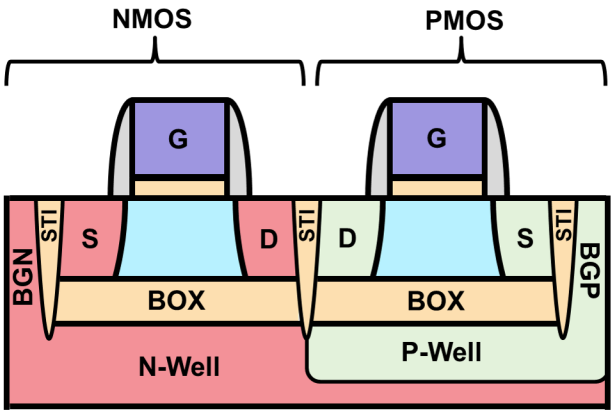

Figure 4.1: Schematics of 28nm FDSOI N- and PMOSFETs with low-V_{TH} (LVT) flavors. Measurements performed with RF access on the front-gate and drain, and DC access on the back-gate.

This section is dedicated to the electrostatic characterization and modeling of the transistor across temperatures ranging from room down to cryogenic levels. First, the threshold voltage shift at cryogenic temperature is presented through different extraction methods. Here the impact of the back-gate bias on the threshold voltage is highlighted. Then, the capacitance is characterized and modeled through RF measurements. Finally, the effective mobility is extracted using the previously analyzed capacitance.

4.1.1 DC characterization

Figure 4.2 presents the drain current as a function of the front-gate voltage for different temperatures and different back-gate voltages. Decreasing temperature has an impact on the drain current, shifting threshold voltages to higher values and increasing the drain current in inversion. As it is explained in chapter 1, the Fermi-Dirac distribution, which becomes sharper at low temperature is responsible for the threshold voltage increase. Moreover, the higher mobility at low temperature induce an higher drain current in inversion at cryogenic temperature [Bec+19]. As described in [Col04], first the back-gate voltage increases the electron densities at the front interface, then if it continues to increase it creates an electron layer at the back-interface. Therefore, when the back-gate voltage increases, reduce the threshold voltage is reduced and increase the drain current is increased [Paz+21].

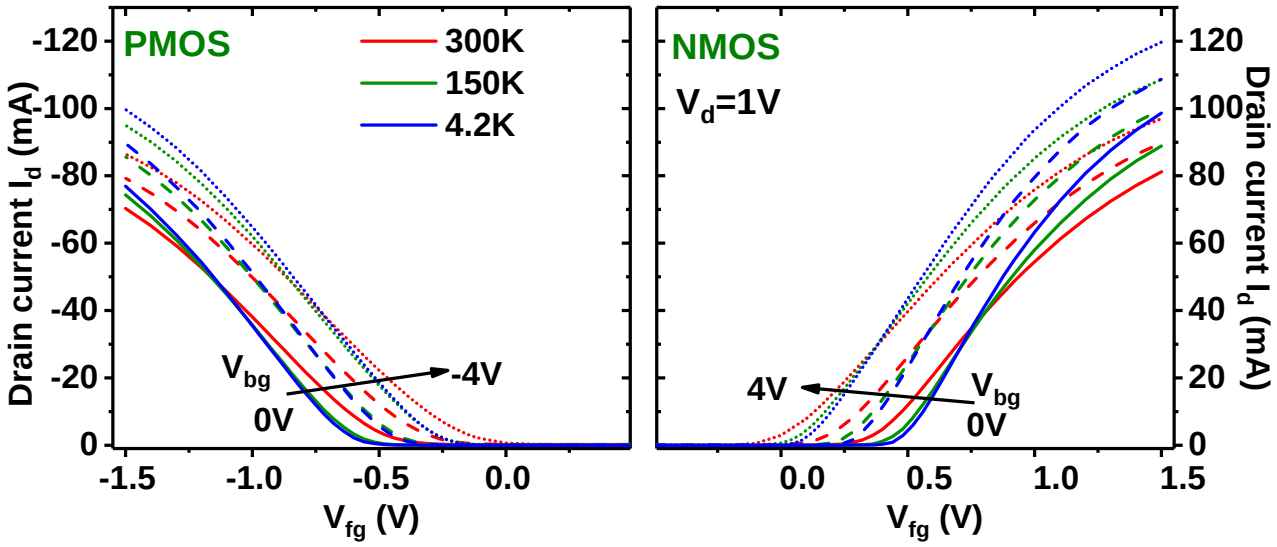

Figure 4.2: Drain current (in linear scale) as a function of the front-gate voltage for different temperatures and different back-gate voltagse. All temperature curves intersect at one point, the Zero Temperature Coefficient (ZTC)

Figure 4.3 illustrates the inversion carrier density distribution calculated for various V_{fb} and V_{bg} conditions at room temperature. When the front-gate voltage (V_{fg}) is sufficiently high, an inversion channel is formed at the front interface. Conversely, an inversion channel emerges at the back interface as the back-gate voltage (V_{bg}) increases. When both V_{fg} and V_{bg} are sufficiently high, inversion channels are created at both interfaces.

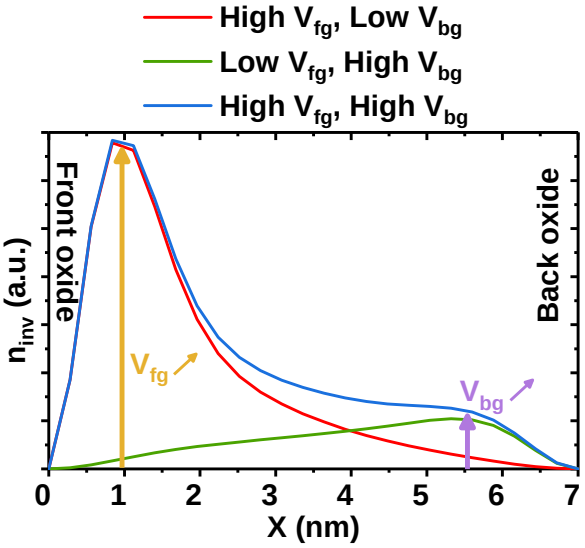

Figure 4.3: Inversion carrier density distribution (calculated with 1D Poisson equation) as a function of position x between the front gate ($x = 0\mu m$) and the back gate ($x = 7\mu m$) for two given values of V_{fg} and V_{bg}.

4.1.2 RF small signal equivalent model

The goal of this work is to use RF characterization as a complementary tool to the DC characterization. As demonstrated in chapter 2, to analyze the RF behavior of the transistor, a equivalent small signal model is used (see figure 4.4), allowing to extract the transistor parameters [Nys+21].

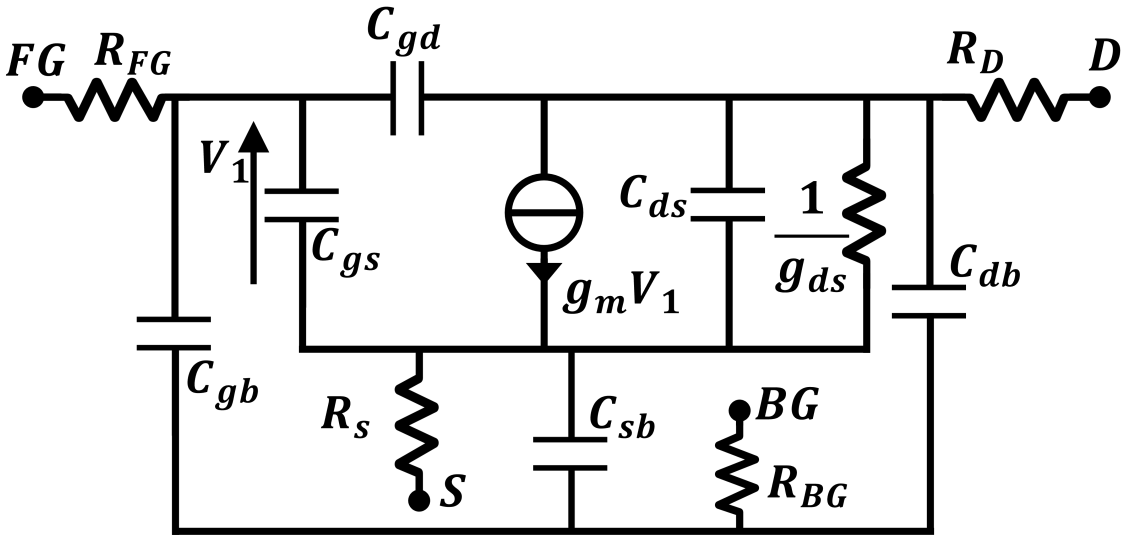

Figure 4.4: FDSOI equivalent small signal circuit. Equation of the transconductance, drain to source conductance and the total front-gate capacitance

This section mainly deals with the total front-gate capacitance (C_{gg}), the gate to drain capacitance (C_{gd}) and the drain to source conductance (g_{ds}). These three parameters are extracted with figure 4.4 using the following equations:

$$C_{\mathrm{gg}} = C_{\mathrm{gb}} + C_{\mathrm{gd}} + C_{\mathrm{gs}} = \frac{\Im(Y_{\mathrm{gg}})}{\omega} \tag{4.1}$$

$$C_{gd} = -\frac{\Im(Y_{\mathrm{gd}})}{\omega} \tag{4.2}$$

$$g_{ds} = \Re(Y_{dd}) g_m = \frac{1}{\Re\left(\frac{1}{Y_{\mathrm{dg}}} - \frac{1}{Y_{\mathrm{gd}}}\right)} \tag{4.3}$$

where $Y_{ij} = \frac{I_i}{V_j}$ with $V_k = 0$ for $k \neq j$ is the admittance parameter.

4.2 Threshold voltage extraction

The threshold voltage is a key parameter in designing circuits with CMOS transistors. Physically, this voltage corresponds to the transition from weak inversion, where the inversion charge is exponentially dependent on the gate voltage V_{GS}, to the strong inversion regime, where the inversion charge varies linearly with V_{GS} [FT11]. The geometry of the transistor induces variations in the threshold voltage: smaller transistors are more susceptible to short channel effects and Drain-Induced Barrier Lowering (DIBL) [FT11]. This transition voltage is temperature-dependent: as the temperature decreases, it shifts to higher absolute values with a sensitivity of around 0.5 to 1 mV/K [Paz+20; Bec+20]. While for bulk MOSFETs, this shift is explained by the temperature dependence of the Fermi level in the silicon channel, in Fully Depleted Silicon-On-Insulator (FDSOI) technology, it is primarily due to the Fermi-Dirac distribution [FT11]. Consequently, it is crucial to define an accurate and physically method for extracting the threshold voltage that remains valid down to deep cryogenic temperatures. In this study, we investigate the extraction of the threshold voltage for CMOS transistors fabricated using the 28 nm FDSOI UTBB technology from STMicroelectronics [Pla+12]. A thorough understanding of the variation of V_{th} with temperature is essential for accurate transistor modeling, and we explore the effect of back-gate bias in shifting the threshold voltage to lower values at cryogenic temperatures.

4.2.1 Different method comparison

There are many different methods to extract the threshold voltage with DC measurement and depending on its definition [Ort+13]. This paper focuses on the constant current method [Tsu+99] and on the second derivative technique [Won+87] because they correspond to the threshold voltage condition $C_{\text{inv}} = C_{\text{ox}}$ in FDSOI transistors, with $C_{\text{ox}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}}$ and $C_{inv} = \frac{dQ_{inv}}{d\psi_s}$ the derivative of the inversion charge with respect to the surface potential [Rud+11; Poi+05].

4.2.2 Constant current method based on EKV model

The constant-current method is often used in industry due to its straightforward application (no capacitance measurement required) and it corresponds to the capacitance definition of the threshold voltage. The threshold voltage is extracted by taking the gate voltage for which a given fixed drain current level is reached. Most of recent papers [Baz+11; BMC20] based the calculation of the constant drain current on the Enz-Krummenacher-Vittoz (EKV) compact MOSFET model. This model provides a physics-based description of the inversion charges in the MOSFET channel [EV06; Sal+03]. In this model, a

specific current is used to normalized the current. This current is named I_{spec} and calculated as follow:

$$I_{spec} = 2 \cdot n \cdot U_t^2 \cdot \mu_0 \cdot C_{ox} \cdot \frac{W}{L} \tag{4.4}$$

Where $U_t = \frac{k_b \cdot T}{q}$ is the thermodynamic voltage, μ_0 is the low field mobility, C_{ox} is the oxide capacitance per unit area and W and L are the width and length of the transistor. The low field mobility is extracted using the Y-function method [Ghi88].

n is the slope factor and is extracted with the substhreshold slope defined as [Bre79]:

$$S = \frac{dV_g}{d(log(I_d))} S = U_t \cdot ln(10) \cdot n \tag{4.5}$$

According to [EV06; EPF; Baz+11], at the transition between weak and strong inversion, the current reachs $0.608 \cdot I_{spec}$ which means:

$$I_{d,const} = 0.608 \cdot I_{spec} = 0.608 \cdot 2 \cdot n \cdot U_t^2 \cdot \mu \cdot C_{ox} \cdot \frac{W}{L} \tag{4.6}$$

Where $I_{d,const}$ is the constant current value and when the current reached this value $V_g = V_{th}$.

This method is applied on the two FDSOI transistor ($20 \times 1\mu m$ gate width and $300nm$ or $28nm$ gate length) and the following $I_{d,const}$ is obtained (see table 4.1 and table 4.2). These values suffer from the uncertainty of the determination of the different parameters that are considered in the formula.

Temperature	n	I_{spec}	$I_{d,const}$
300K	1.1	2.35 $\times 10^{-2} mA$	1.43 $\times 10^{-2} mA$
200K	1.13	1.36 $\times 10^{-2} mA$	8.27 $\times 10^{-3} mA$
100K	1.24	6.28 $\times 10^{-3} mA$	3.82 $\times 10^{-3} mA$
50K	1.42	1.96 $\times 10^{-3} mA$	1.19 $\times 10^{-3} mA$
4.2K	10.9	1.07 $\times 10^{-4} mA$	6.56 $\times 10^{-5} mA$

Table 4.1: Determination of the constant current based on the EKV model for all temperature and for device of $L = 300nm$ and $W = 20\mu m$.

Temperature	n	I_{spec}	$I_{d,const}$
300K	1.3	$2.48 \times 10^{-1} mA$	$1.51 \times 10^{-1} mA$
200K	1.5	$1.08 \times 10^{-1} mA$	$6.57 \times 10^{-2} mA$
100K	1.67	$9.49 \times 10^{-2} mA$	$5.77 \times 10^{-2} mA$
50K	1.9	$3.10 \times 10^{-2} mA$	$1.89 \times 10^{-2} mA$
4.2K	17	$1.76 \times 10^{-3} mA$	$1.07 \times 10^{-3} mA$

Table 4.2: Determination of the constant current based on the EKV model for all temperature and for device of $L = 28nm$ and $W = 20\mu m$.

The drain current in logarithm scale as a gate voltage function for the two characterized transistors is presented in figure 4.5. The crosses correspond to the extraction point of the threshold voltage.

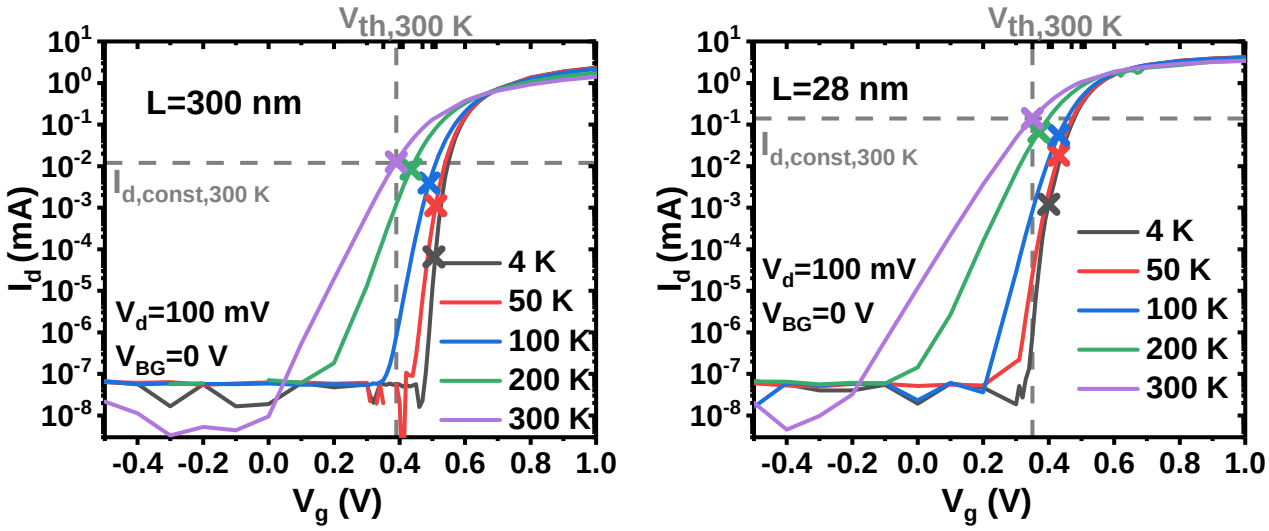

Figure 4.5: DC drain current versus gate voltage. The dotted lines correspond to the constant current value and to the threshold voltage at 300 K. The extraction points of the threshold voltage are marked with a cross. (Left) For device of $L = 300nm$ and $W = 20\mu m$. (Right) For device of $L = 28nm$ and $W = 20\mu m$.

The limits of this method include the calculation of the constant drain current $I_{\text{d,const}}$ which depends of other parameters to extract such as the slope factor and the mobility (especially at cryogenic temper-

ature). Moreover the formula (4.6) needs to be adapted at low drain voltage according to [Baz+11]. For the small device shown in Figure 4.5 (right), the curves at 4 K exhibit a lower V_{th} compared to those at 50 K or 100 K. This discrepancy arises due to subthreshold behavior, where tunneling through defects occurs [Boh+19]. Moreover, even if the value of $I_{\text{d,const},4K}$ corresponds to the capacitance condition, it has been demonstrated in [CCG23] that in short devices operating in the subthreshold regime, the drain current oscillates due to percolation effects. These oscillations impact the extraction of the threshold voltage, highlighting the limitations of the constant current method.

4.2.2.1 Second derivative method

The second derivative method consists in deriving twice the drain current with respect to the gate voltage. Nevertheless, this approach is susceptible to limitations due to mobility variation and series resistance effects, which introduce some degree of uncertainty in the threshold voltage extraction process [Rud+11]. This method is understood by considering an ideal transistor. In an ideal transistor, the drain current is equal to zero for $V_{\text{g}} < V_{\text{th}}$, and becomes proportional to V_{g} for $V_{\text{g}} > V_{\text{th}}$. Under these assumptions, the first derivative of the drain current with respect to the gate voltage is a Heaviside function $\theta(V_{\text{g}} - V_{\text{th}})$.

Therefore, the second derivative is infinite when $V_{\text{g}} = V_{\text{th}}$. With a real transistor, this second derivative will not be infinite but will reach a maximum at $V_{\text{g}} = V_{\text{th}}$, as can be seen in figure 4.6.

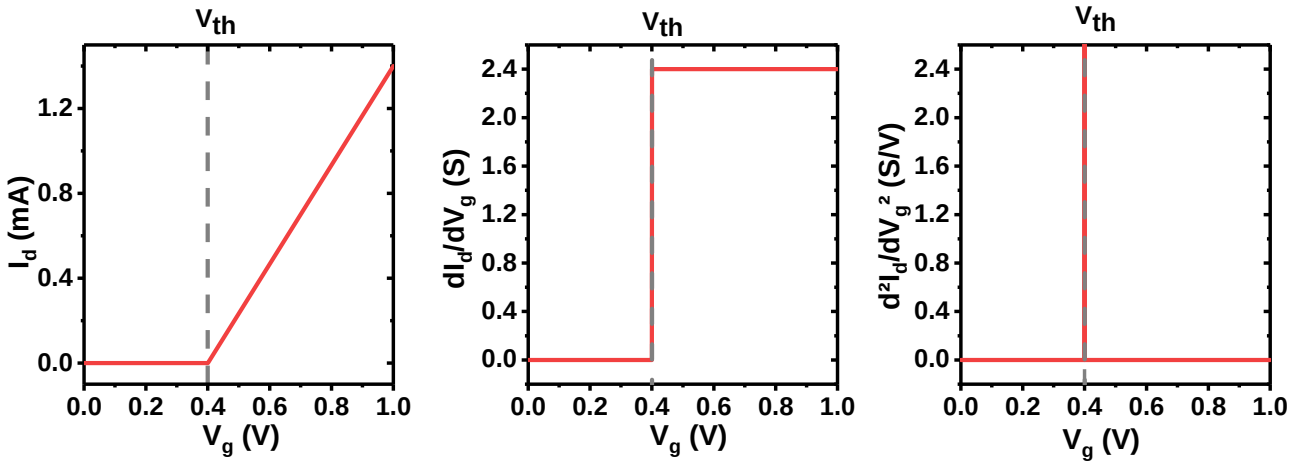

Figure 4.6: Explanation about how the threshold voltage is extracted from the second derivative method. (Left) Ideal drain current (Middle) Ideal transconductance (Right) Ideal second derivative as a function of gate voltage.

The measurement result of the drain current second derivative are presented in figure 4.7.

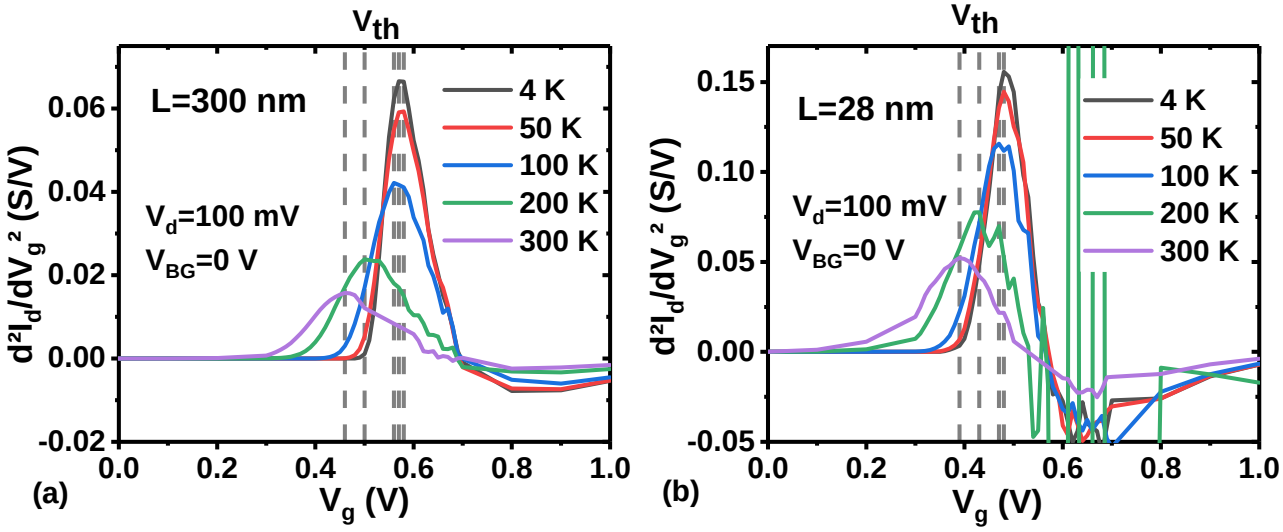

Figure 4.7: Derivative of the DC transconductance gm with respect to the gate voltage versus gate voltage. The dotted lines correspond to gate voltage when dgm/dVg is maximum (i.e. to Vth) (a) For device of $L = 300nm$ and $W = 20\mu m$. (b) For device of $L = 28nm$ and $W = 20\mu m$.

Figure 4.7 illustrates the limitations of this extraction method, particularly related to the noise, which is amplified by the second derivative. Additionally, at cryogenic temperatures, the mobility increases [BG17], and in our case, as the cryogenic prober is manual, the access resistances vary from one measurement to another, leading to uncertainty. In short-channel transistors, there are fewer carriers, and the recombination centers are less active, which can result in an inaccurate threshold voltage value. According to our measurements, the uncertainty is ± 0.01 V for the large transistor and ± 0.05 V for the small one.

4.2.2.2 Capacitance derivative method

Mathematically, the transition point between the weak inversion regime, where Q_{inv} is exponentially dependent on V_{g}, and the strong inversion regime, where Q_{inv} is linear with V_{g}, is given by the maximum of the second derivative of Q_{inv} with respect to V_{g} [Rud+11]. It is equal to the maximum of the first derivative of the gate-to-channel capacitance C_{GC} with respect to V_{g}:

$$\max_{V_{\text{g}}} \left(\frac{d^2 Q_{\text{inv}}}{dV_{\text{g}}^2} \right) = \max_{V_{\text{g}}} \left(\frac{dC_{\text{GC}}}{dV_{\text{g}}} \right) \tag{4.7}$$

RF measurements conducted with a VNA enable the direct extraction of capacitance from S-parameter measurements. This approach offers greater precision than measurements with a LCR-meter,

due to the calibration and de-embedding steps, which facilitate the removal of a greater number of parasitic elements in the case of a VNA being used. In RF measurements, this capacitance is evaluated by the gate capacitance C_{gg}, given as follows:

$$C_{gg} = C_{gd} + C_{gs} + C_{gb} = \frac{\mathrm{Im}(Y_{11})}{2\pi f} \tag{4.8}$$

where f is the frequency and Y_{11} is the input admittance on the transistor gate [Poz11] measured with the Vector Network Analyzer (VNA). The gate capacitance (C_{gg}) is mainly due to the channel capacitance (C_{gc}) contribution and increases with the inversion charge. The gate capacitance and its derivative with respect to gate voltage are presented in figure 4.8.

The limitation of this method lies in the numerical noise introduced by the first derivative. However, it offers two significant advantages over other extraction techniques: it is independent of series resistance and the transport properties of the channel carriers. Additionally, the error bars are smaller compared to those of other methodologies. The error bar is ± 0.01 V for all measured transistors and temperatures, mainly linked to the measurement voltage step. This is relatively low compared to DC methods, as shown in Figure 4.9 and Figure 4.10. In the C_{gg} measurement using RF, contributions from parasitic capacitances (such as overlap and fringing capacitances) are present. However, their variations with respect to the gate voltage are negligible compared to the deviation of the channel capacitance [Fru+21]. Therefore, even with parasitic contributions, the transition between weak and strong inversion results in a noticeable change in C_{gg} (Figure 4.8 (a) and (b)) and a precise maximum for the derived capacitance (Figure 4.8 (c) and (d)). Thus, the threshold voltage can be accurately extracted even for transistors with a very small gate area.

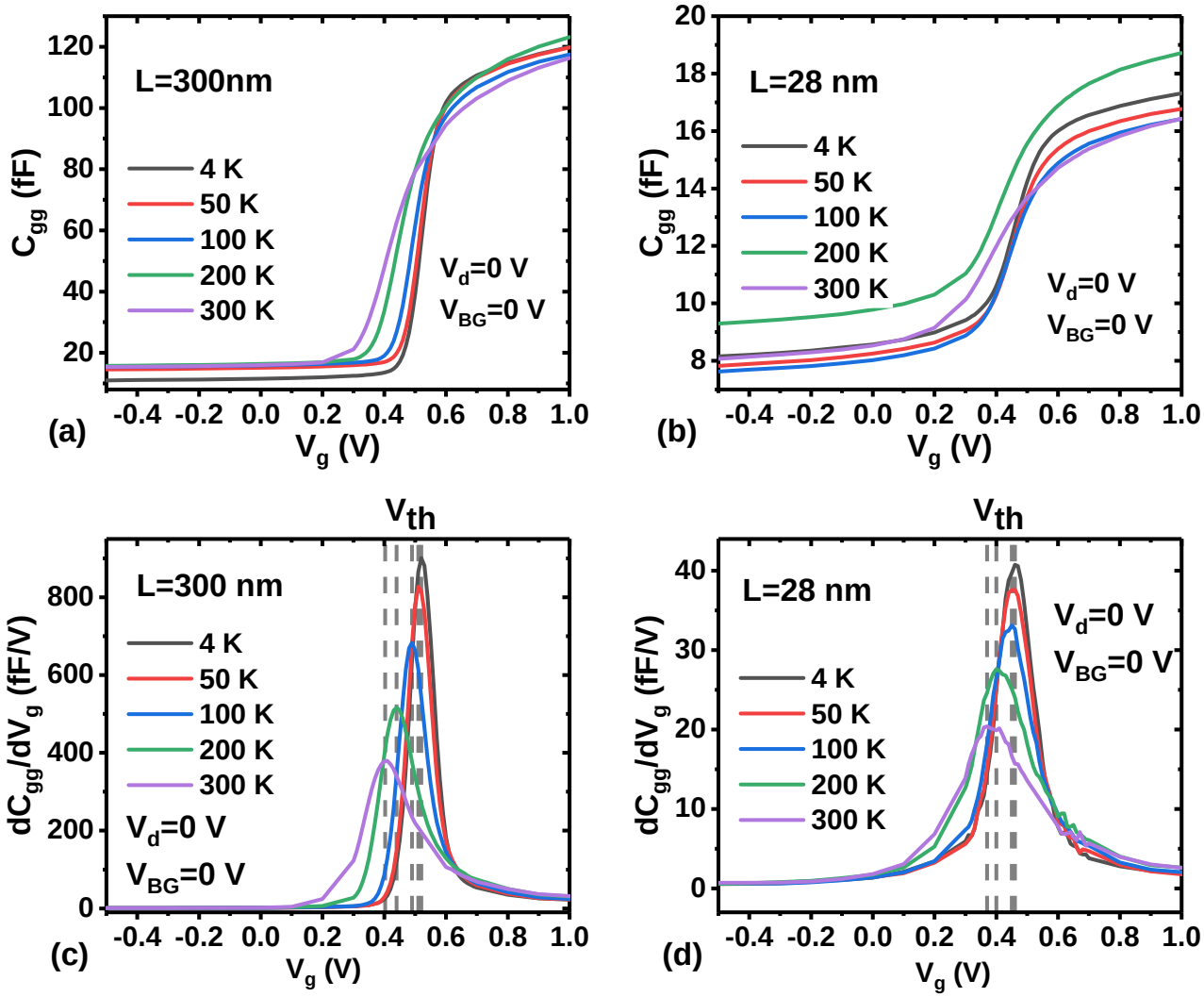

Figure 4.8: (a) and (b) Gate capacitance averaged between 1 and 5 GHz versus the gate voltage. (c) and (d) Derivative of the gate capacitance with respect to the gate voltage. The dotted lines correspond to gate voltage when dC_{gg}/dV_g is maximum (i.e. to V_{th}). (a) and (c) For device of $L = 300nm$ and $W = 20\mu m$. (b) and (d) For device of $L = 28nm$ and $W = 20\mu m$.

4.2.2.3 Comparison and conclusion

As shown in figure 4.9 and table 4.3, for relatively long devices, we see that all the methods present a similar variation of the threshold voltage with respect to the temperature decrease, differing only by a shift smaller than 70 mV. Moreover, the RF extraction method fit well with the 1D-Poisson-Schrödinger calculation based on charge distribution. The charge distribution and therefore the threshold voltage is governed by the Fermi Dirac distribution as demonstrated in chapter 1. On the other hand, for small

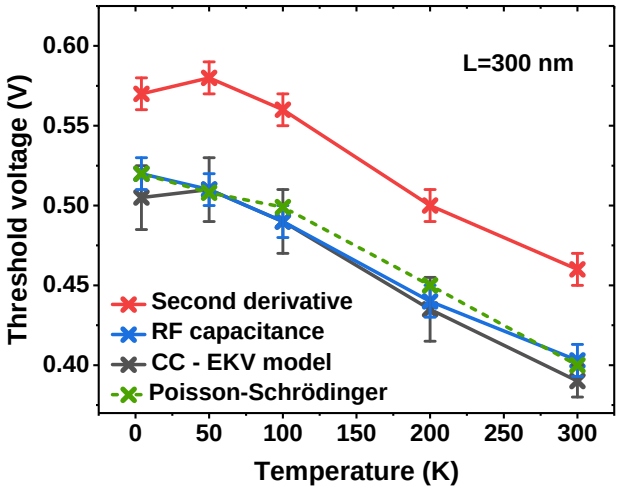

Figure 4.9: Threshold voltage extracted by different methods as a function of temperature (Vd = 100 mV and VBG = 0 V).For device of $L = 300nm$ and $W = 20\mu m$.

Temperature	CC	SD	RF capa
300K	0.37 ± 0.01 V	0.46 ± 0.01 V	0.41 ± 0.01 V
200K	0.42 ± 0.02 V	0.5 ± 0.1 V	0.44 ± 0.01 V
100K	0.47 ± 0.02 V	0.56 ± 0.01 V	0.49 ± 0.01 V
50K	0.49 ± 0.02 V	0.58 ± 0.01 V	0.51 ± 0.01 V
4.2K	0.50 ± 0.02 V	0.57 ± 0.01 V	0.52 ± 0.01 V

Table 4.3: Threshold voltage values for different extraction methods and different temperature. (CC = Constant Current method based on EKV model, SD = Second Derivative method and RF capa. = gate capacitance channel derivative method). For device of $L = 300nm$ and $W = 20\mu m$.

devices (figure 4.10 and table 4.4), the constant current method diverges from the other ones below 50 K. The second derivative and the RF capacitance methods present a similar variation.

The second derivative method leads to a higher slope which is most likely related to the mobility degradation at the interface [Rud+11]. The constant-current method yields to a lower slope mainly due to the calculation of $I_{\mathrm{d,const}}$.

The temperature sensitivity of V_{th} is 0.3–0.4 mV/K from 300 K to 100 K. Below 100 K, the thresh-

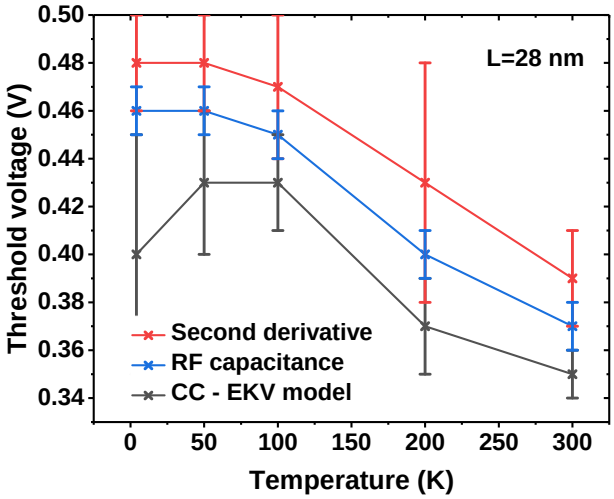

Figure 4.10: Threshold voltage extracted by different methods as a function of temperature (Vd = 100 mV and VBG = 0 V).For device of $L = 28nm$ and $W = 20\mu m$.

Temperature	CC	SD	RF capa
300K	0.32 ± 0.01 V	0.39 ± 0.02 V	0.37 ± 0.01 V
200K	0.36 ± 0.02 V	0.43 ± 0.05 V	0.4 ± 0.01 V
100K	0.39 ± 0.02 V	0.47 ± 0.03 V	0.45 ± 0.01 V
50K	0.4 ± 0.03 V	0.48 ± 0.02 V	0.46 ± 0.01 V
4.2K	0.38 ± 0.05 V	0.48 ± 0.02 V	0.46 ± 0.01 V

Table 4.4: Threshold voltage values for different extraction methods and different temperature. (CC = Constant Current method based on EKV model, SD = Second Derivative method and RF capa. = gate capacitance channel derivative method). For device of $L = 28nm$ and $W = 20\mu m$.

old voltage tends to saturate as reported for other technologies [Bec+20] (where the EKV model is used to extract the threshold voltage). As explained in chapter 1, the threshold voltage in the bulk technology is explained the Fermi potential variation at cryogenic temperature [Bec+20] whereas for FD-SOI, it is explained by the threshold surface potential variation due to the Fermi-Dirac distribution [CG22].

The shift between V_{th} values given by the different methods can be explained as RF capacitance method is purely based on a charge variation, whereas the DC ones are mediated by the current and

depends on the mobility variation.

The threshold voltage has been extracted also on PMOS transistor with the RF capacitance method and the results are presented in figure 4.11:

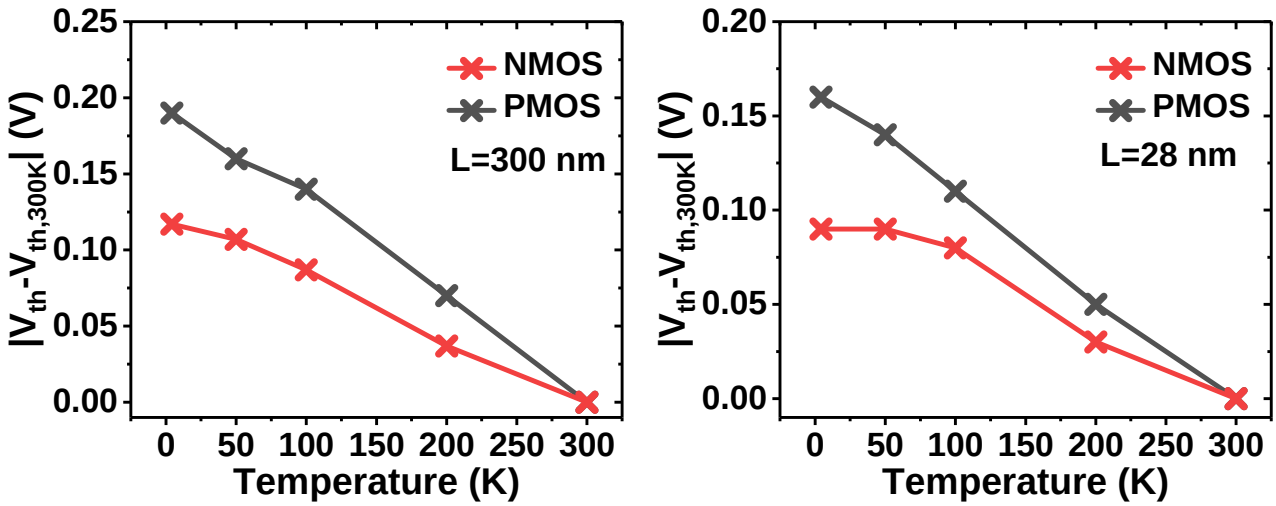

Figure 4.11: Threshold voltage values minus threshold voltage at 300K for NMOS and PMOS as a temperature function (Left) For device of $L = 300nm$ and $W = 20\mu m$. (Right) For device of $L = 28nm$ and $W = 20\mu m$.

In these curves, the PMOS threshold voltage does not saturate at cryogenic temperatures and shows a different slope compared to the NMOS. This phenomenon has been previously observed in earlier studies [Bec+20; Cas+22] and remains challenging to fully explain. In [EBJ20], an approach is suggested to fit the PMOS threshold voltage by incorporating an effective temperature dependence in the oxide capacitance. However, this hypothesis is contradicted by capacitance measurements presented in [Cas+22], where the oxide capacitance remains constant across varying temperatures. In [Cas+22], the observed threshold voltage variation is instead attributed to the saturation of the subthreshold slope at very low temperatures (typically below 100K). This behavior is effectively explained by considering a two-dimensional density of states, $N(E, \Delta E)$, with a disorder-induced exponential band tail, where ΔE represents the characteristic energy width of the band tail extension [Ghi+20].

In this subsection, we presented three distinct methodologies for extracting the threshold voltage at low temperatures. It was demonstrated that the RF extraction method is the most effective at cryogenic temperatures due to the fact that it is serie resistance independant, to its continued applicability at low temperatures, and to its suitability for use on transistors of all sizes. In the rest of the manuscript, the RF capacitance method is used to extracted the threshold voltage.

4.2.3 Back-gate voltage impact

The total gate capacitance is presented in figure 4.12 with its derivative and for different back-gate bias. Both at 300K and at 4.2K and when back-gate bias is not zero, this capacitance presents two different slopes, which respectively correspond to the apparition of the back and front channel. These apparitions are traduced on the derivative by the apparition of the two maxima when the back-gate voltage is high. At low temperatures, the increase in capacity is steeper due to the Fermi-Dirac distribution, which is sharper at low temperatures. On these curves, threshold voltage can be extracted, as for the front-gate voltage, at the maximum capacitance derivative [Rud+10].

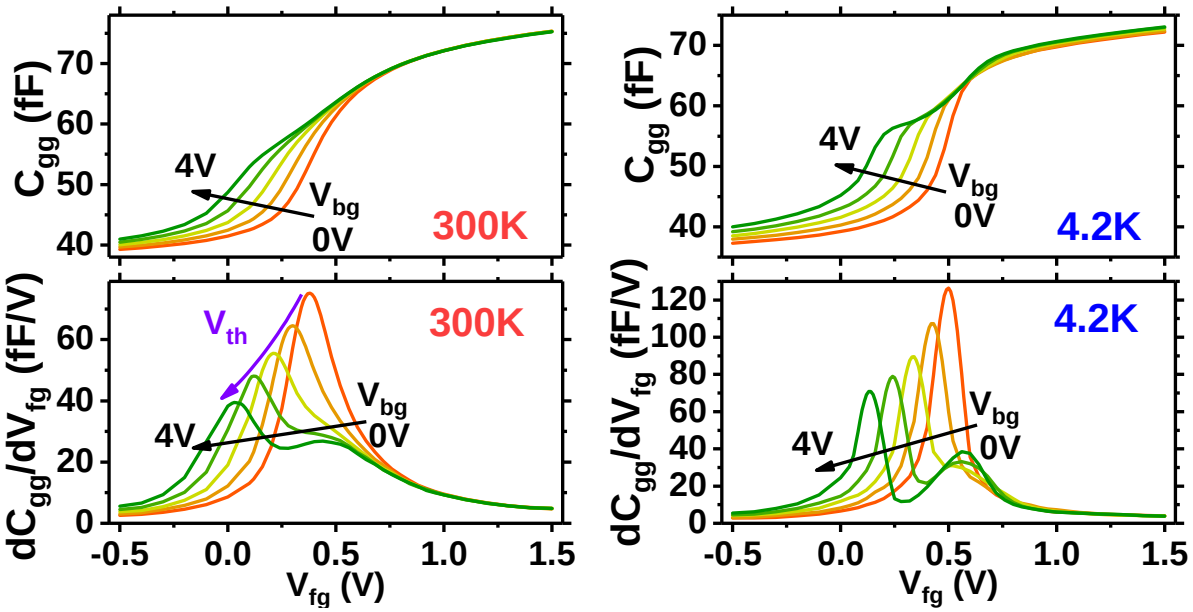

Figure 4.12: Total gate capacitance (Top) and its derivative (Bottom) as a function of Vfg at 300K (Left) and 4.2K (Right). When the capacitance derivative maximum is reached, Vfg=Vth. Extracted between 1 and 3GHz. For device of $L = 28nm$ and $W = 80\mu m$.

The threshold voltage of the N and PMOS devices as a function of back-gate voltage for different temperature is shown in figure 4.13. Both NMOS and PMOS, threshold voltages present a linear variation with back voltage independently of the temperature [CDC20].

$$V_{th} = \Delta\phi_m + \psi_{S,th} + \frac{C_b}{C_{ox}}\left(\psi_{S,th} - (V_{bg} - \phi_{fb})\right) + \frac{h^2}{8qm_{\text{conf}}t_{SI}^2} \tag{4.9}$$

where: $\Delta\phi_m$: work function difference, $\psi_{S,th}$: surface potential at threshold, C_b: bulk capacitance, C_{ox}: oxide capacitance, V_{bg}: back-gate voltage, ϕ_{fb}: flat band potential, h: Planck's constant, q: electron charge, m_{conf}: confinement effective mass, t_{SI}: silicon thickness.

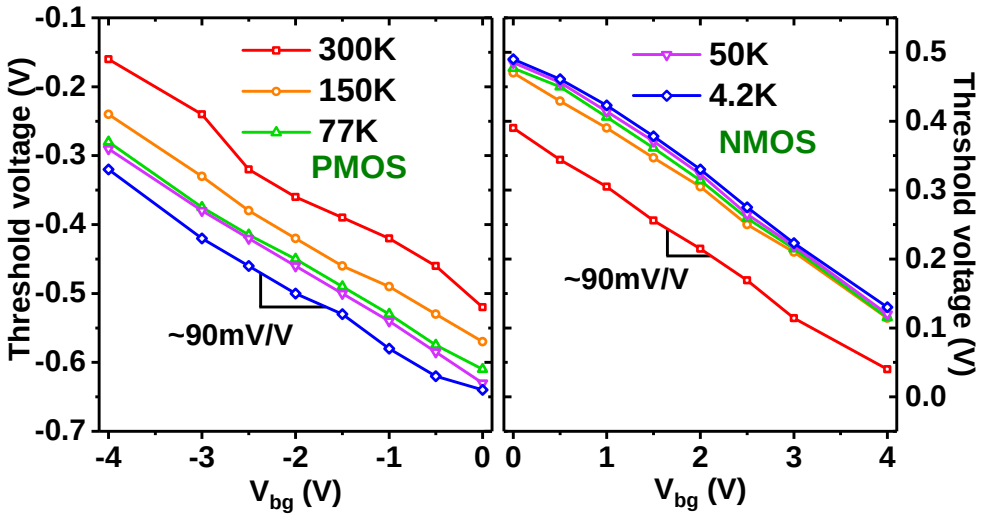

Figure 4.13: NMOS and PMOS Threshold voltages as a function of the back-gate voltage. The NMOS transistor has a 28nm gate length and 80 fingers of 1μm gate width. The PMOS transistor has a 28nm gate length and 120 fingers of 1μm gate width.

This section demonstrates that a reduction in temperature results in a shift in the threshold voltage. However, by applying a back-gate bias, at every temperature, the threshold voltage can be set to the same value as at room temperature which is one of the advantage of FDSOI technology for cryogenic applications.

4.3 RF capacitance characterization and model

In the field of transistor technology, the comprehension of capacitance behavior is employed to determine the threshold voltage, as previously demonstrated, but also the mobility.

In particular, the various transistor capacitances that constitute the small-signal AC model are crucial parameters for adapting the input and output power of an LNA. This section presents the extraction and modeling of UTBB FD-SOI transistor capacitances at zero drain voltage for temperatures ranging from 300 K to 4.2 K.

4.3.1 Capacitance description

From the measured S-parameters, we can extract the admittance Y-parameters of the transistor. Using a transistor model shown in figure 4.4 [Kil+21], we can compute the different capacitances C_{gs}, C_{gd}, C_{ds} and C_{gb} as presented in equations 4.10 to 4.12 with g, s, d and b standing for the gate, the source, the drain and the back-gate terminals respectively.

$$C_{\text{gg}} = C_{\text{gs}} + C_{\text{gd}} + C_{\text{gb}} = \frac{\text{Im}(Y_{\text{gg}})}{\omega} \tag{4.10}$$

$$C_{\text{gd}} = \frac{\text{Im}(Y_{\text{gd}})}{\omega} \tag{4.11}$$

$$C_{\text{gs}} + C_{\text{gb}} = C_{\text{gg}} - C_{\text{gd}} \tag{4.12}$$

At zero drain voltage, the transistor is symmetric. Therefore, the gate to drain capacitance C_{gd} is equal to the gate to source capacitance C_{gs}. Using this assumption and equation 4.12, we can extract the front-gate to back-gate (C_{gb}) capacitance:

$$C_{\text{gb}} = C_{\text{gg}} - 2 \cdot C_{\text{gd}} \tag{4.13}$$

In figure 4.14, we present a typical total gate capacitance C_{gg} measured as a function of the gate voltage, for a zero drain/source voltage and different temperatures ranging from 300K down to 4.2K. The presented capacitance value has been averaged where the capacitance measurement is flat with frequency (between 1.5 GHz and 6.5 GHz).

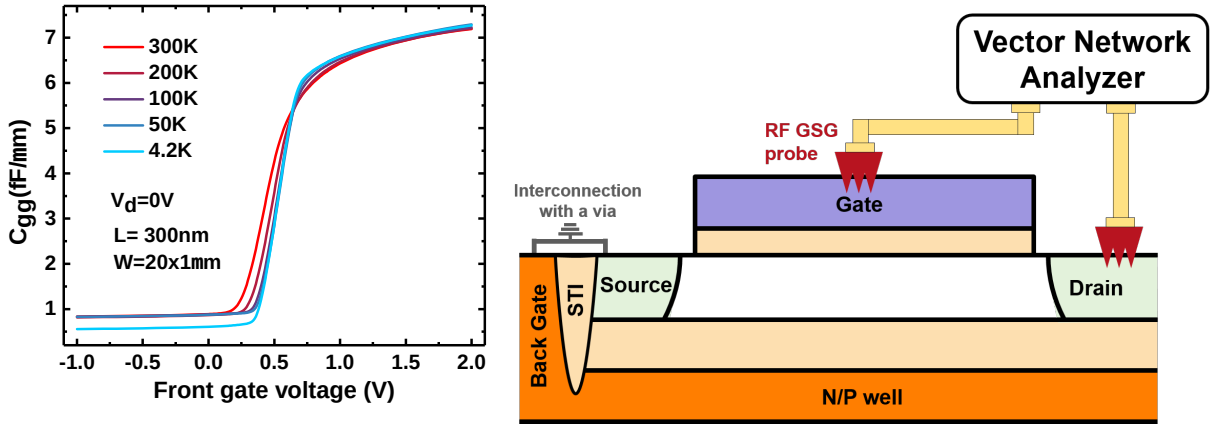

Figure 4.14: Total gate capacitance normalized by gate width as a function of gate voltage from room temperature down to cryogenic temperature and at zero drain voltage averaged from $f = 1.5GHz$ to $6.5GHz$ for gate width of $20\mu m$ and gate length of $300nm$ and measurement schematic.

On this graph, we notice the presence of a Zero Temperature Coefficient (ZTC) point at a gate voltage of 0.55 V. In FDSOI technology, this zero variation point results from the temperature behavior of the Fermi–Dirac function, which controls the sub-band carrier population [Cat+22]. The transition between depletion and inversion regime occurs at higher gate voltage when the temperature decreases in link with the Fermi-Dirac distribution which becomes sharper [FT11].

At very high inversion regime (typically above 1 V for this FD-SOI technology), the gate-to-gate capacitance remains the same regardless of the temperature. When the channel is created, this capacitance is equal to the oxide capacitance in series with an inversion capacitance in the silicon [Fru+21]. In depletion regime (below $V_g = 0$ V), all curves are merged at the same value ($C_{\text{gg}} = 8.3$ fF/μm as illustrated in Fig. 2) except the one at 4.2 K, which is noticeably lower. This effect, which is out of our measurement uncertainty, is investigated in the following section. Three samples have been tested on three different cryogenic probers. Every sample has been measured at least 3 times and the behaviour remains the same.

To analyse our measurements in depletion region, we proposed the schematic shown in figure 4.15, where C_{of} and C_{if} are the over fringe and inner fringe capacitance respectively [Fru+21].

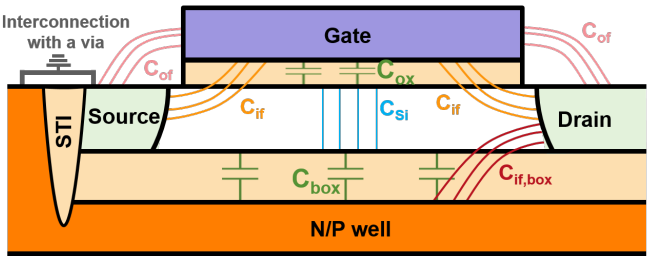

Figure 4.15: Electric field line of a FDSOI transistor in common source schematic at room temperature.

From this model, we compute the different capacitances expressed in the previous section. The inner fringe capacitance between the box and the source is short-circuited by the source to back-gate interconnection since the transistor measured are in common source configuration.

$$C_{\text{gd}} = C_{\text{of}} + C_{\text{if}} + (C_{\text{ox}} \ \ series \ \ C_{\text{Si}} \ \ series \ \ C_{\text{box}} \ \ series \ \ C_{\text{if,box}}) \tag{4.14}$$

$$C_{\text{gs}} = C_{\text{of}} + C_{\text{if}} \tag{4.15}$$

$$C_{\text{gb}} = (C_{\text{ox}} \parallel C_{\text{Si}} \ \ series \ \ C_{\text{box}}) \tag{4.16}$$

Where $C_a \ \ series \ \ C_b = \frac{C_a C_b}{C_a + C_b} = \left(\frac{1}{C_a} + \frac{1}{C_b}\right)^{-1}$.

In equation (4.14), the third term is negligible in comparison to the over and inner fringe capacitance because the impact of the inner fringe capacitance between the box and the drain is very low due to the back-gate connected to the ground (through the source access). C_{ox}, C_{Si}, and C_{box} depend linearly on the transistor gate length while C_{if} and $C_{\text{if,box}}$ have a non-linear dependence [Hib+15]. C_{of} is independent of the gate length [Hib+15].

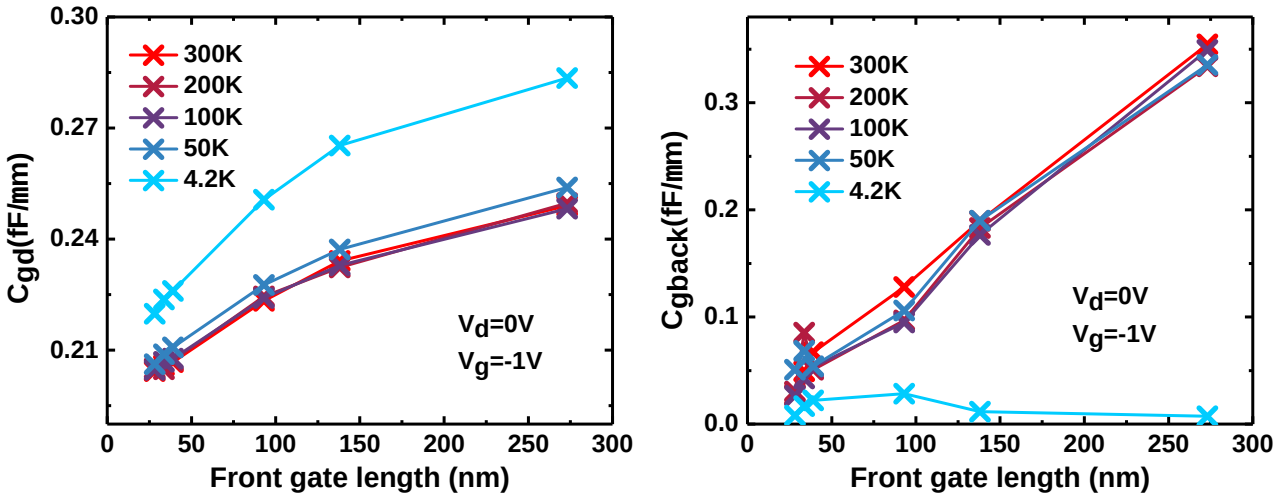

Figure 4.16: (Left) gate to drain and (Right) gate to back-gate capacitance as a function of transistor gate length for different temperature in depletion ($V_G = -1V$ and averaged from $f = 1.5GHz$ to $6.5GHz$) and at zero drain voltage.

Figure 4.16 (left) shows the gate to drain capacitance as a function of the gate length in depletion and for a zero drain voltage. As expected from equation (4.14), curves from 300K to 50K present similar values and non-linear variation with the gate length. The 4.2K curve also presents a non-linear variation but with 20% higher values than other temperature curves. Figure 4.16 (right) presents the gate to back-gate capacitance as a function of the gate length. As expected from equation 4.16, the curves from 300K to 50K have similar values and vary linearly with the gate length. On the other hand, at 4.2K, this capacitance becomes equal to zero whatever the gate lengths. We will explain this effect in detail in the next section.

4.3.2 Carrier freeze-out impact

In the N/P-well, the doping concentration is around 10^{18} cm^{-3}. At this concentration, the silicon is not degenerated and at temperature low enough (typically below $T \approx 50$ K), the Fermi level becomes smaller than the activation level [Bec+20]. The thermal energy is not high enough to ionize the dopants. Thus, the resistivity of the N/P-well increases [Bec+19].

As this freeze-out occurs, the inner fringe capacitance between the source and the back-gate is no longer short-circuited, and the third term of equation (4.14) is no longer negligible, leading to the equivalent circuit illustrated in figure 4.19. By considering the N-well resistance reaching a very high value, we can rewrite equations (4.17) and (4.18):

$$C_{\text{gs}} = C_{\text{gd}} = C_{\text{of}} + C_{\text{if}} + (C_{\text{ox}} \ \ series \ \ C_{\text{Si}} \ \ series \ \ C_{\text{box}} \ \ series \ \ C_{\text{if,box}}) \tag{4.17}$$

$$C_{\text{gb}} = 0 \tag{4.18}$$

The gate-to-drain capacitance increases due to the third term in equation (4.17) because at cryogenic temperatures, the well high resistance causes a degradation of the the back-gate connection to ground, resulting in the electric field predominantly directed towards the drain access. This phenomenon is illustrated in figure 4.17. A similar reasoning applies to the electric field between the front-gate to the back-gate, leading to the conclusion that C_{gb} becomes negligible.

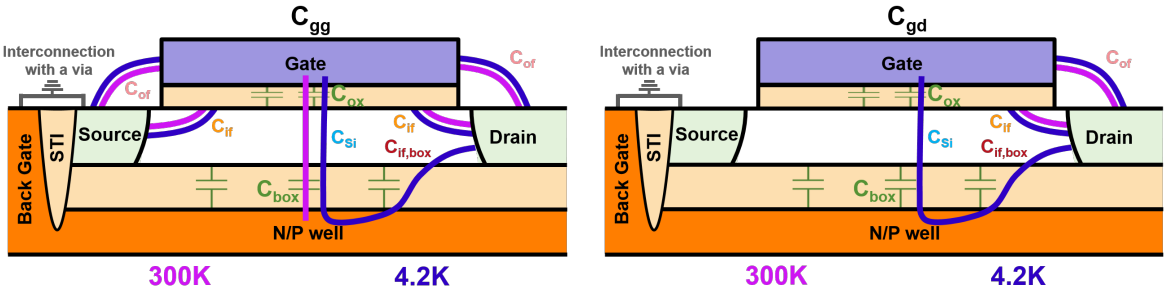

Figure 4.17: Electric field line of a FDSOI transistor in common source schematic at room temperature for (left) C_{gg} and (right) C_{gd} at room and at cryogenic temperature.

Between the freezing temperature (according to [Kit57; Bec+19], around 100 K) and 4.2 K, some of the dopants have enough energy to exceed the activation energy and become ionized. Thus, the N/P-well resistance will progressively increase. To observe this phenomenon, figure 4.18 (a and b) presents measurements of total front-gate and front-gate to drain capacitance for a 300 nm gate length LVT NMOS transistor at temperatures ranging from room temperature down to 4.2 K.

In figure 4.18 (a and b) for temperatures of 100 K and lower, we observe variations in capacitance over frequency.

When the temperature decreases, the well resistance value increases and the electric field predominantly directed towards the drain access which increases the C_{gd} value and decreases C_{gg}.

We can conclude that the N-well resistance is in parallel with the inner fringe capacitance between the box and the source. Thus, as the well resistance increases, the transition frequency (where capacitance is not flat with respect to frequency) decreases. These two graphs show that at cryogenic temperatures, accurate extraction of capacitance over the frequency is important because it can modify the measured capacitance value by up to 20%.

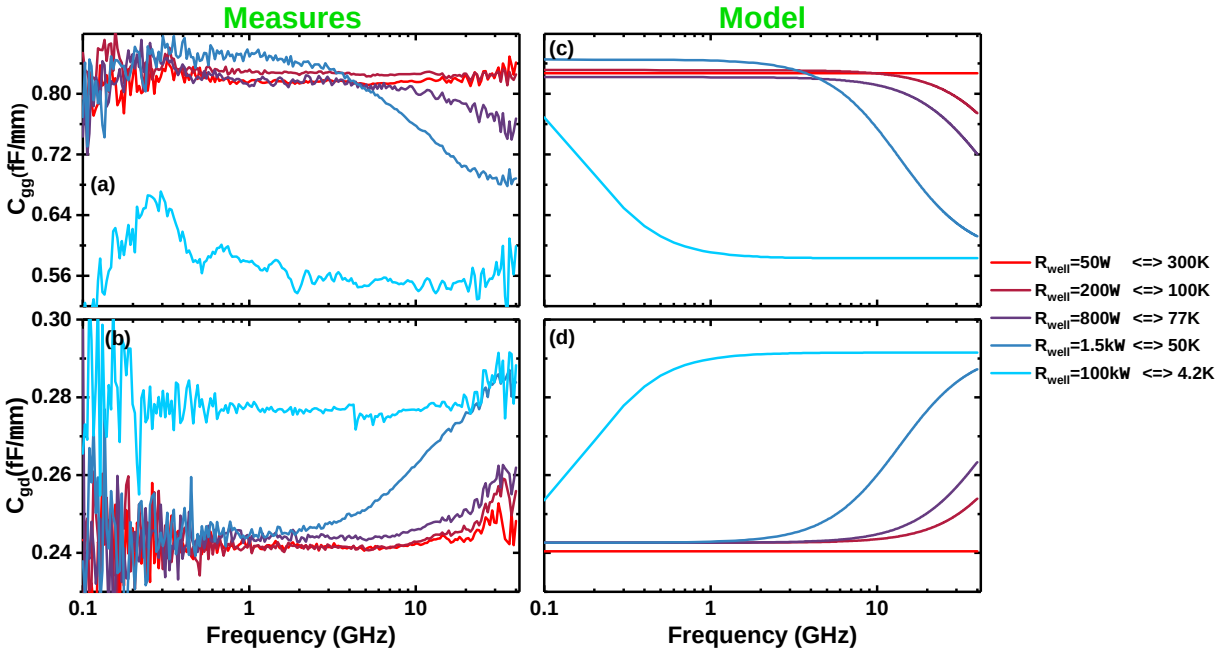

Figure 4.18: (a) Total gate and (b) gate to drain capacitance as a function of frequency from room temperature down to cryogenic temperature in depletion ($V_g = -1V$) for a zero drain voltage of a LVT NMOS transistor. (c) Total to gate and (d) gate to drain capacitance normalized by transistor width as a function of the frequency for different N-well resistance value. According to the model, the curves are for 300K, 100K, 77K, 50K and 4.2K respectively.

4.3.3 Proposed transistor capacitance model

From figure 4.15, we proposed the following RC model to simulate the frequency capacitance dependence. In this model, the N/P-well resistance is in parallel with the box to source inner fringe capacitance. Meaning that when the resistance is small (i.e. at room temperature), the inner fringe capacitance is negligible and when the resistance is high (i.e. at cryogenic temperature), the inner fringe capacitance becomes predominant.

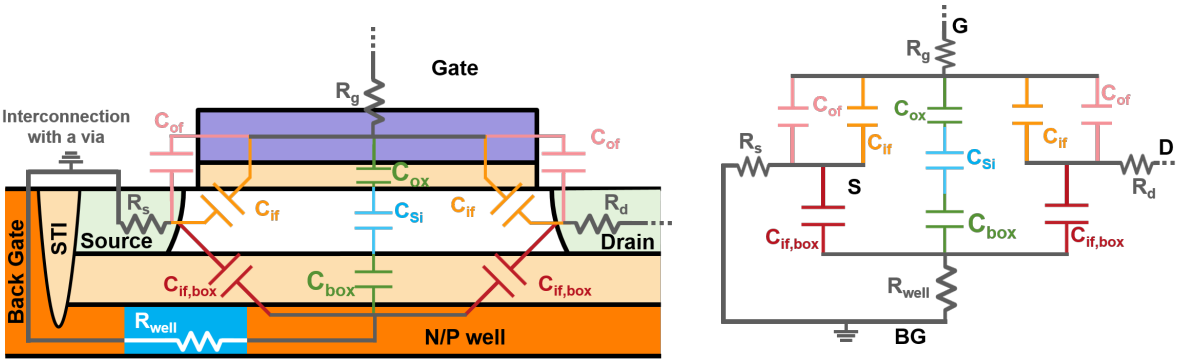

Figure 4.19: (Left) Transistor cross section with corresponding lumped elements (Right) Transistor Model proposed

The values of the different capacitances for a 300 nm gate length and 20 μm gate width transistors are shown in table 4.5. The oxide, silicon, and box capacitances have been calculated using the permittivity (ϵ_r) and thickness of the different materials as follows:

$$C = \frac{\epsilon_r \times \epsilon_0}{\text{thickness}} \quad (10)$$

The inner and over fringe capacitances have been calculated with the refined conformal mapping model from [Hib+15].

Temperature	C_{ox}	C_{si}	C_{box}	C_{of}	C_{if}	$C_{if,bow}$
300K - 4.2K	140fF	74.2fF	6.76fF	1.7fF	2.5fF	1.3fF

Table 4.5: Capacitance values for the transistor capacitance model for a 300nm gate length and a $20\mu m$ gate width. All the capacitance calculation are independent of the temperature.

By using this model in the ADS® software, we simulate the frequency dependence of the capacitance presented in figure 4.18 (c and d).

The graphs from the previous model (figure 4.18 (c and d)) show the frequency variation of the capacitance values. The starting and ending values of the capacitance are close to those measured in figure 4.18 (a and b). Moreover, as the temperature decreases, the value of the N/P-well resistance increases, and the capacitance variation trend is similar to that observed in figure 4.18 (a and b). The transition frequency shifts to lower frequencies as the N/P-well resistance increases. To observe these variations with an LCR meter (measurement around 1 MHz), the resistance value needs to be higher (at least $R_{\text{sub}} = 5\,\text{M}\Omega$ to observe variations at 1 MHz, according to the model proposed in Figure 4.19) indicating that the impact of substrate freeze-out will affect mostly high-frequency applications.

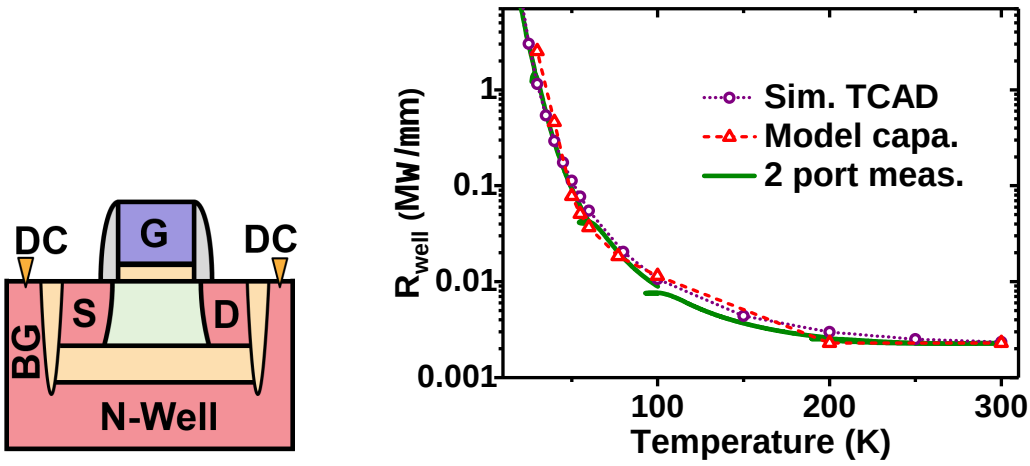

Figure 4.20: Well resistance as a function of the temperature and 2 port measurements schematic. TCAD simulation are performed on synopsis with the incomplete ionization model. Model capacitance is the fit with figure 4.19.

4.3.4 4-port RF transistors capacitance measurement

In the following study, a 4-port RF transistor has been characterized (Gate, Drain, Back-gate and substrate). Due to the limited availability of RF probes in the cryogenic prober, only 2-ports out of the total 4-ports of the transistor are connected to the RF path; and the remaining ones are connected to DC probe for biasing. As presented in appendix B, the transistor was initially measured on a room temperature prober at 300K, and the measurements were then compared to those obtained at 300K on the Lakeshore cryogenic prober with two RF probes and two DC probes. In this case, the evaluated capacitance is between the total capacitance seen between the back-gate and the ground (C_{bb}), as well as the capacitance between the front-gate and the back-gate. In order to achieve this, the two RF probes are placed on the front-gate and the back-gate, respectively, as illustrated in Figure 4.21 (Top).

The total back-gate C_{bb} (Right) and front-gate to back-gate capacitances C_{gb} (Left) as a function of the front-gate voltage are also presented in figure 4.21. The results of the front to back-gate capacitance measurement and model correspond to the behavior observed previously. In the depletion mode, the capacitance is equal to the sum of the oxide, silicon, and buried oxide capacitances, all in series. In inversion mode, the channel is formed, effectively screening the back-gate, causing all the signal from the front-gate to be directed to the drain and source. Consequently, the front to back-gate capacitance is nearly zero. At cryogenic temperatures, the capacitance value decreases due to the freezing out of the back-gate.

In order to model the total back-gate capacitance, it is necessary to consider the substrate capac-

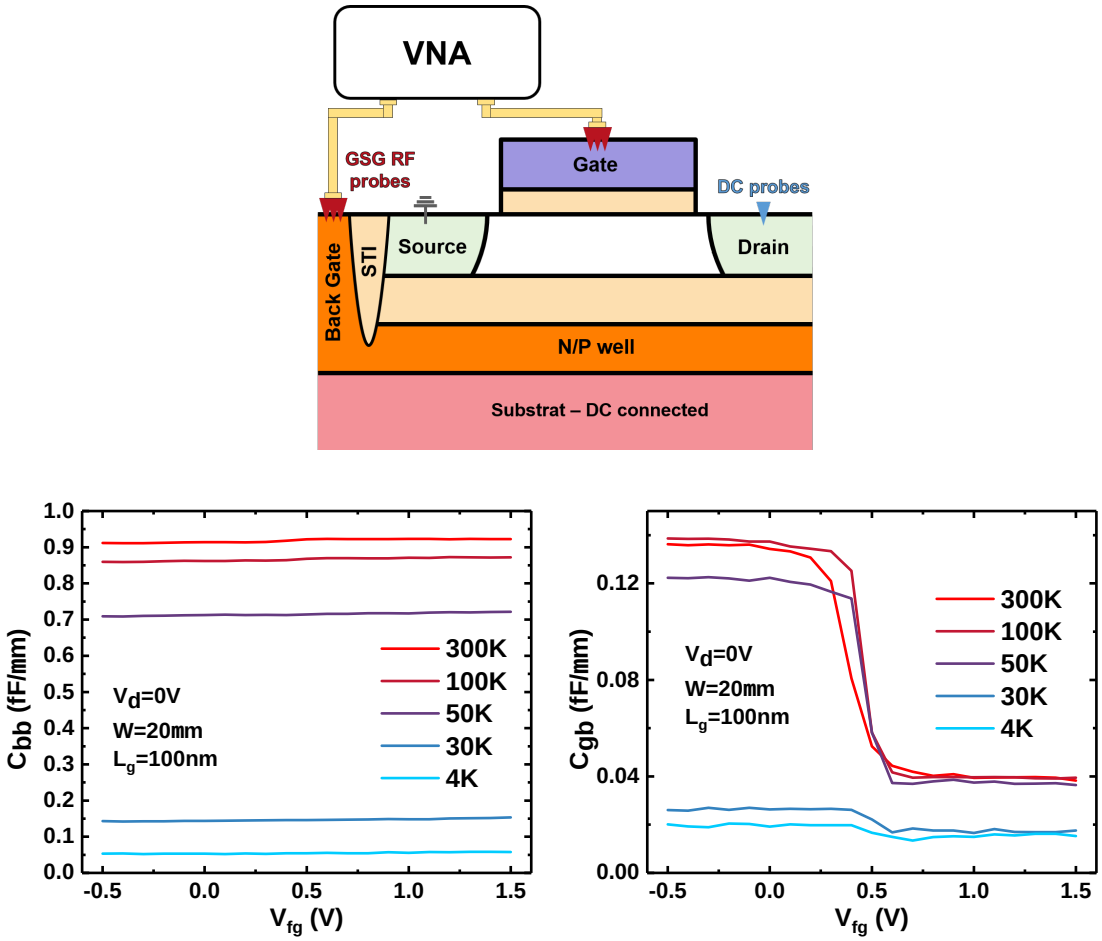

Figure 4.21: (Top) Measurement schematic with RF probe on the back-gate. (Left) Total back-gate and (Right) front-gate to back-gate capacitance normalized by gate width as a function of gate voltage from room temperature down to cryogenic temperature and at zero drain voltage averaged from $f = 1.5GHz$ to $6.5GHz$ for gate width of $20\mu m$ and gate length of $100nm$.

itance. This adds a decoupling capacitance of approximately 10 pF [Nys+21]. This value has been confirmed by 4-RF probes measurements. As the substrate is silicon doped at $10^{15}cm^{-3}$, the N-well of the back-gate and the substrate freeze at cryogenic temperature. This results in an increase in resistivity and a decrease in C_{bb}. To gain a deeper understanding of the behaviour of this capacitances, the previous model is expanded to include the capacitance between the back-gate and the substrate, as illustrated in Figure 4.22.

In order to more clearly illustrate the capacitance dependence with frequency, the capacitance in depletion as a function of frequency is presented in Figure 4.23. This graph illustrates that the total back-gate capacitance and the front to back-gate capacitance are no longer frequency-independent when the temperature is reduced. The new model allows the reproduction of the frequency dependence of the

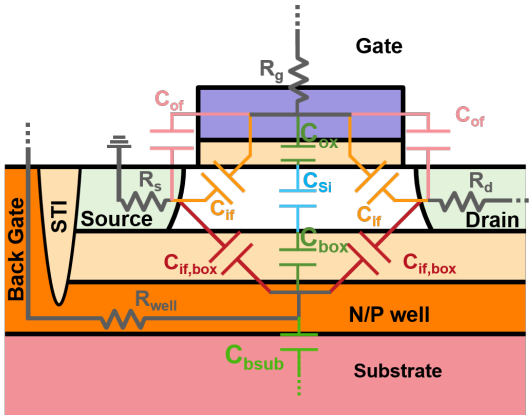

Figure 4.22: Transistor cross section with corresponding lumped elements including the substrate

different capacitances by the application of a back-gate resistance variation, as demonstrated in Figure 4.23.

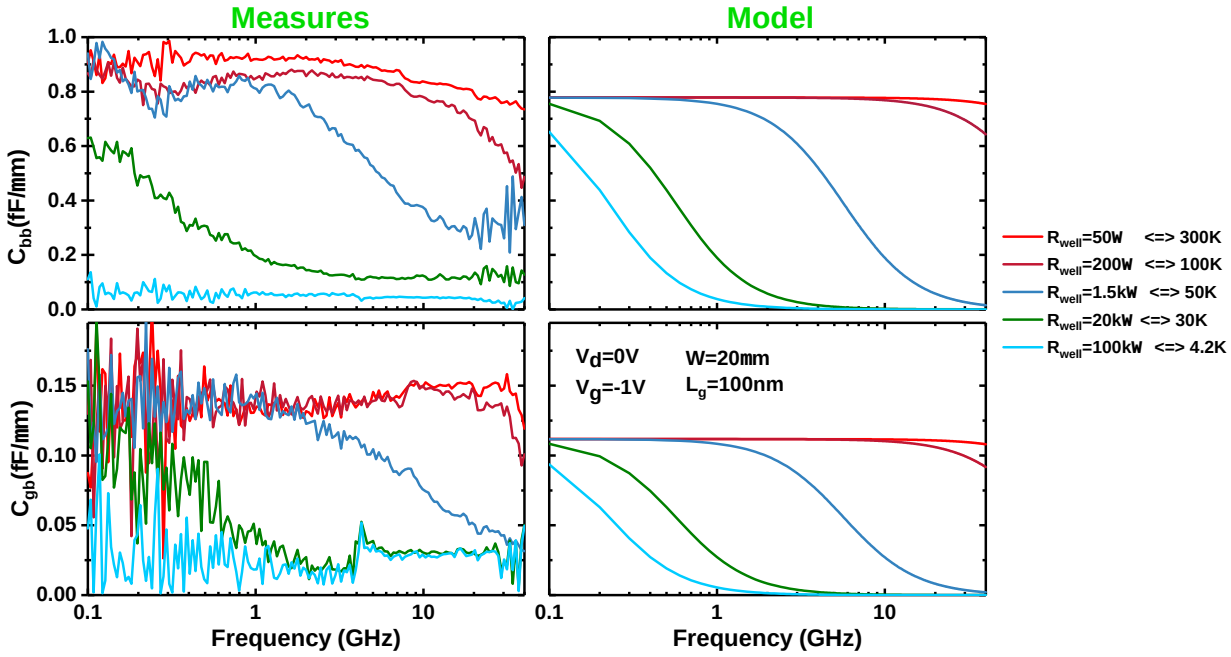

Figure 4.23: (a) Total back-gate and (b) front-gate to back-gate capacitance as a function of frequency from room temperature down to cryogenic temperature in depletion ($V_g = -1V$) for a zero drain voltage of a LVT NMOS transistor. (c) Total back-gate and (d) front-gate to back-gate capacitance normalized by transistor width as a function of the frequency for different N-well resistance value. According to the model, the curves are for 300K, 100K, 50K, 30K and 4.2K respectively.

Once more, by merely enhancing the value of the N-well resistance, we have successfully replicated the frequency dependence of the capacitance.

In this study, we have presented the extractions and the modelling of the LVT NMOS transistor capacitance at RF frequency until 40 GHz. The results of the NMOS transistor were presented, as the PMOS transistors exhibited the same behavior. These measurements revealed that when the measurement temperature reaches a critical value, the dopants in the back-gate N/P-well begin to freeze, increasing the value of the N-well resistance of the back-gate and affecting its operation, especially at high frequency. The value of the capacitances measured may vary depending on the extraction frequency.

4.4 Effective Mobility extraction

Mobility measurements are typically used to examine the scattering mechanisms in MOSFETs experienced by the carriers in the channel of the transistors. The effective mobility μ_{eff} can be evaluated using the split CV technique. In this method, the effective mobility is expressed by the following equation:

$$\mu_{\text{eff}} = \frac{L}{W}\frac{I_{\text{d}}}{Q_i V_d} = \frac{L}{W}\frac{g_{ds}}{Q_i} \tag{4.19}$$

where W and L are the transistor dimension, I_d the drain current, V_d the drain voltage, g_{ds} the drain to source conductance and Q_i the inversion charge.

The method requires the inversion charge and drain current measurements. The effective mobility accounts for Coulomb, phonon, and surface roughness scattering mechanisms [BG17]. In this section, we show how the capacitance study is used to perform the split CV method [Rom+04].

4.4.1 Inversion charge calculation

The inversion charge is expressed with the channel capacitance as:

$$Q_i(V_g) = \int_0^{V_g} C_{gc}(V)\, dV \tag{4.20}$$

where C_{gc} is the gate to channel capacitance.

For the gate to channel capacitance, we use the model proposed in figure 4.19. With this model, the total front-gate capacitance can be expressed as:

$$C_{gg}(V_g, L) = C_{gc}(V_g, L) + 2C_{if}(V_g, L) + 2C_{of}(V_g) \tag{4.21}$$

To obtain the gate to channel capacitance, first step is to subtract the total front-gate capacitance of two different dimensions of transistor. Before doing the subtraction, it is important to check that the two transistors has the same threshold voltage. The subtraction is presented in figure 4.24

As previously stated, the over-fringe capacitances are independent of the channel length, and thus do not affect the remaining capacitances after subtraction. Conversely, the inner-fringe, oxide, and inversion capacitances are dependent on the channel length and constitute the remaining capacitance, designated as C_{diff}.

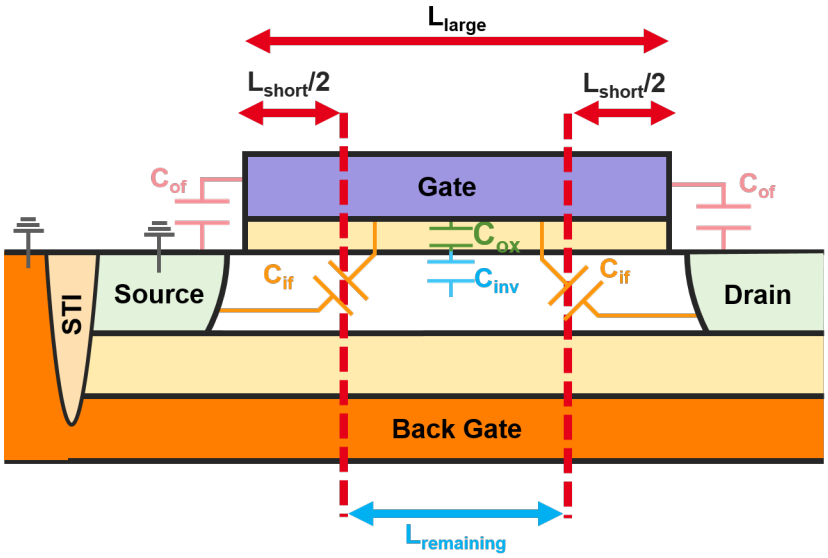

Figure 4.24: Capacitance subtraction of a large and a short transistor inspired by [Mot23].

With all the remaining capacitance, C_{diff} takes the following value :

- In depletion, when $V_{fg} << V_{th}$:

$$C_{\text{diff}}(\text{DEP}) = \frac{C_{\text{ox}} C_{\text{if,remaining}}}{C_{\text{ox}} + C_{\text{if,remaining}}} (L_{large} - L_{short}) \tag{4.22}$$

- In strong inversion, when $V_{fg} >> V_{th}$:

$$C_{\text{diff}}(\text{INV}) = C_{\text{ox}} (L_{large} - L_{short}) \tag{4.23}$$

- Between depletion and strong inversion

$$C_{\text{diff}}(V_g) = \frac{C_{\text{ox}} (C_{\text{if,remaining}} + C_{\text{inv}})}{C_{\text{ox}} + C_{\text{if,remaining}} + C_{\text{inv}}} (L_{large} - L_{short}) \tag{4.24}$$

With these three equations, we can extract the inversion capacitance without any parasitic capacitance:

$$C_{\text{inv}} = \left(\frac{1}{\frac{1}{C_{\text{diff}}(V_g)} - \frac{1}{C_{\text{diff}}(\text{INV})}} - \frac{1}{\frac{1}{C_{\text{diff}}(\text{DEP})} - \frac{1}{C_{\text{diff}}(\text{INV})}} \right) \tag{4.25}$$

We apply this method first at room temperature and on two transistors of a 20 μm gate width and 300 nm and 100 nm gate lengths. Figure 4.25 presents the total front-gate capacitance of these two transistors.

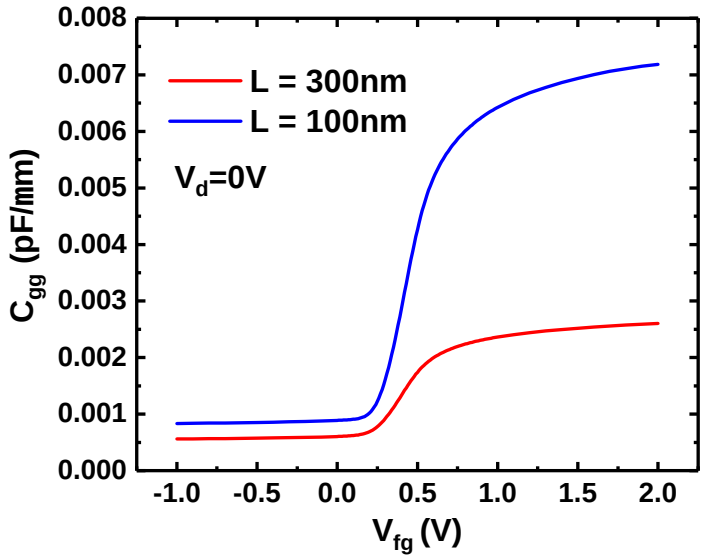

Figure 4.25: total front-gate capacitance as a function of gate voltage for two different gate length (300nm and 100nm) and a gate width of 20 $\times$ 1 μm fingers.

To evaluate this method, we compare the curves with two other methods:

- a classic split CV [Rom+04]. The channel capacitance is calculated by only subtracting the total front-gate capacitances of two transistors with different gate length. Called ”Spilt CV” on the following graphs.

- an improved split CV [Mor+21]. The channel capacitance is extracted as for split CV but with an additional step which consists to remove the capacitance in depletion to the whole curve. It is called ”*Morelle's CV*” on the following graphs.

The comparison on the channel capacitance is presented in figure 4.26.

In the case of the split capacitance voltage (CV) method, the C_{ch} value is not null in depletion due to the presence of the inner fringe capacitance. In contrast, for the *Morelle's CV* method, the value of C_{ch} is lower in the inversion mode, as a constant value of the inner fringe capacitance is removed. In inversion, the inner fringe capacitances become equal to zero when the channel is created, as stated in [Fru+21]. The method proposed allows for C_{ch} equal to zero in depletion and equal to the split CV method in inversion, which is consistent with the model proposed previously. In conclusion, regarding the different methodologies:

- The split CV method has not completely eliminated all parasitic capacitance, with some inner fringe capacitances still present in the calculated channel capacitance.

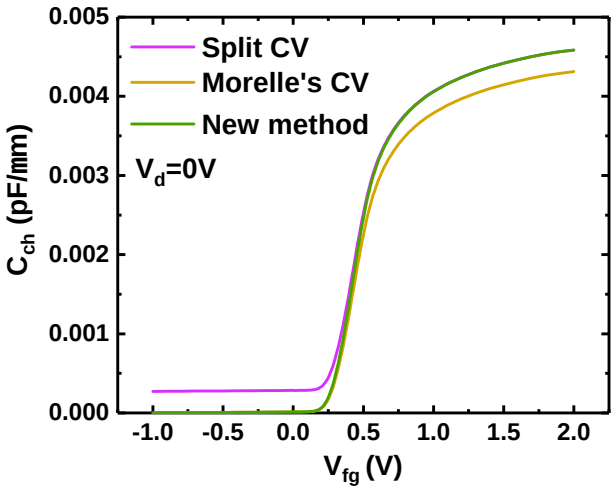

Figure 4.26: Capacitance as a function of the gate voltage. First curve correspond to the subtraction of the transistor capacitance of 300nm and 100nm gate length and a gate width of 20 $\times$ 1 μm fingers. Second curve is the extraction of the channel capacitance with the reference [Mor+21]. The last one is the channel capacitance as presented before.

- The *Morelle's CV* method has removed too much parasitic capacitance in inversion by assuming that the inner fringe capacitance affects both depletion and inversion in the same way.
- The proposed method successfully removes the parasitic capacitance by considering its differing impact on capacitance in depletion and inversion.

Once the gate to channel capacitance is expressed, the inversion charge can be calculated. Figure 4.27 presents the inversion carrier density for the three different methods discuss above.

The split-CV method results in a higher inversion carrier density that is not null in depletion due to the presence of a channel capacitance that differs from zero in depletion. The *Morelle's CV* method yields a lower inversion carrier density in comparison to the novel method.

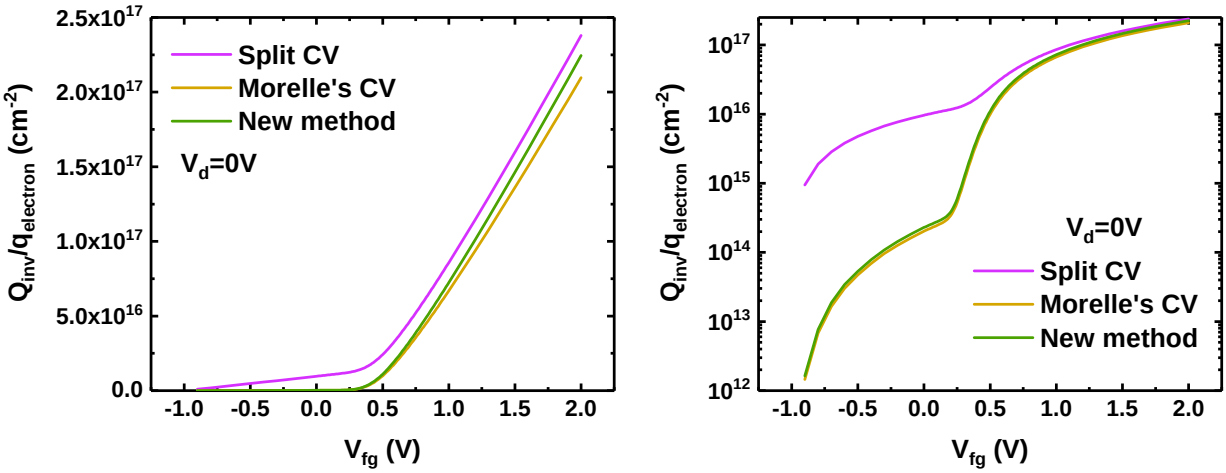

Figure 4.27: Inversion charge divided by electron charge as a function of the gate voltage in linear (Left) or in logarithm (Right) scale. Purple curve corresponds to the subtraction of the transistor capacitance of 300nm and 100nm gate length. Yellow curve is the extraction of the channel capacitance with the reference [Mor+21]. The green one is the channel capacitance as presented before.

The aforementioned methodology was applied at every temperature on the same devices as before ($L_g = 300nm - 100nm$), and the results were as follows:

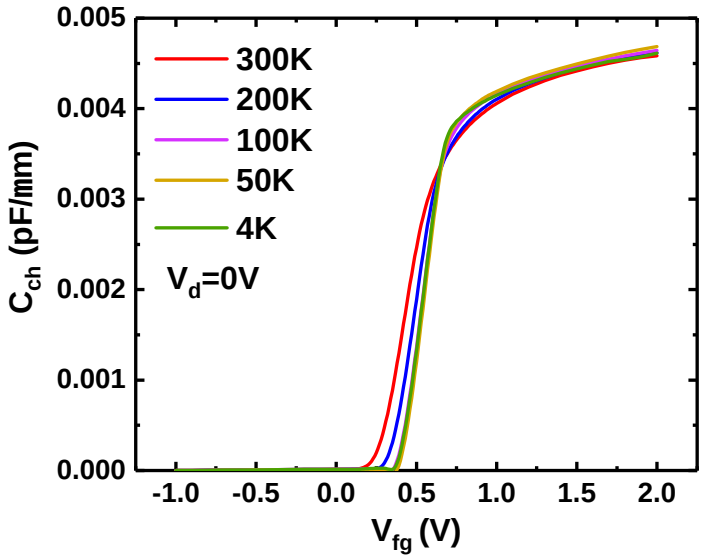

Figure 4.28: Channel capacitance measured as a function of the gate voltage from room down to cryogenic temperature.

As expected, the gate to channel capacitance exhibits identical values in depletion and inversion, regardless the temperature. The discrepancy lies in the more pronounced tilt observed at low temperatures, which is the result of an increasingly steep Fermi-Dirac distribution. The inversion carrier density in linear and logarithm scale is presented in figure 4.29.

Due to the Fermi-Dirac distribution, the inversion carrier density increases at higher gate voltage and the slope in subthreshold regime is steeper in logarithm scale when the temperature decreases.

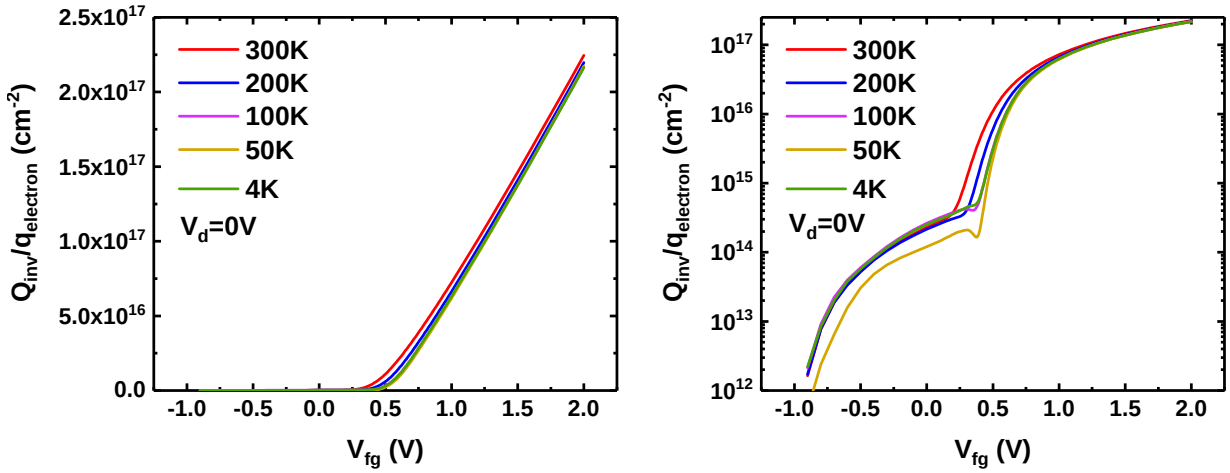

Figure 4.29: Inversion charge divided by electron charge as a function of the gate voltage in lineare (Left) or in logarithm (Right) scale from room down to cryogenic temperature.

4.4.2 Drain to source conductance correction

Since we extracted the inversion charge from the measurements, only the drain to source conductance is remaining to express the effective mobility value. As explained in chapter 2, $g_{ds,meas}$ is extracted directly with the S-parameters and suffer from different parasitics such as the access resistance. However, to calculate the effective mobility, the intrinsic drain to source conductance should be extracted. To do so, the same reasoning as for the capacitance is applied on the drain to source conductance. To remove the different parasitics that are independent from the transistor length, the following equation is used:

$$\frac{1}{g_{ds,int,L1-L2}}(V_{fg}) = \frac{1}{g_{ds,meas,L1}}(V_{fg}) - \frac{1}{g_{ds,meas,L2}}(V_{fg}) \tag{4.26}$$

where $g_{ds,int}$ is the intrinsic drain to source conductance and $g_{ds,meas}$ is the drain to source conductance measured. In our case, we applied this methodology to transistors with a gate length of 300nm and

100nm. So the intrinsic drain to source conductance is obtained for a intrinsic 200nm channel length.

Figure 4.30 (Left) presents the result of $g_{ds,meas,300nm}$, $g_{ds,meas,100nm}$ and $g_{ds,int,200nm}$ at 300K and (Right) the intrinsic drain to source conductance for different temperatures.

As shown in these graphs, the intrinsic conductance is higher than the measured one since the access resistance has been eliminated [Nys+20]. Furthermore, as the temperature decreases, the intrinsic conductance increases due to enhanced mobility at lower temperatures [Bec+19].

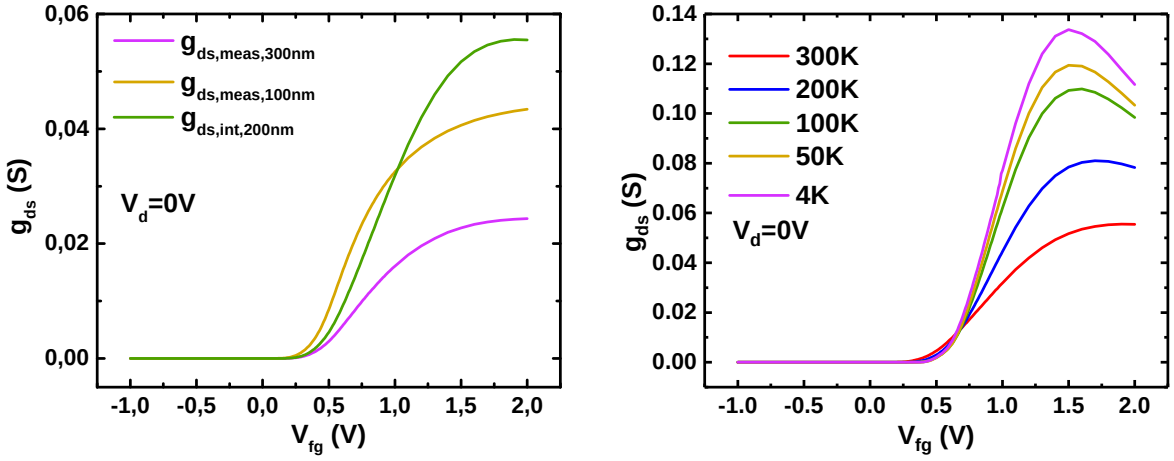

Figure 4.30: (Left) Drain to source conductance correction explanation at 300K. The transistor gate width is 20 fingers of 1 μm (Right) Drain to source conductance as a function of the gate voltage from room down to cryogenic temperature after subtraction.

4.4.3 Effective mobility

Finally, with the equation (4.19), the effective mobility is computed. The results are presented in figure 4.31 at room temperature and for the three different methods of the inversion charge calculation.

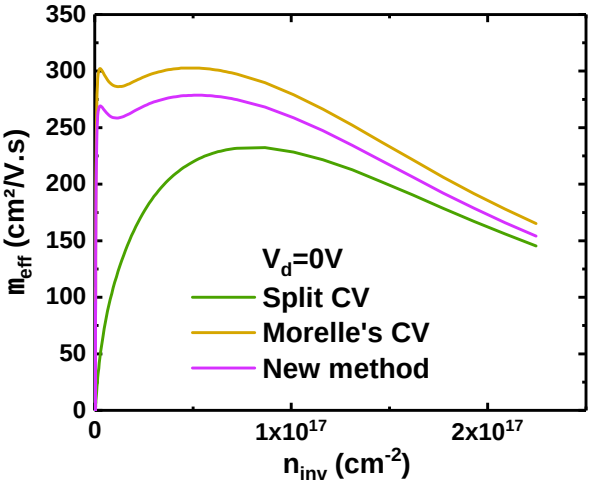

Figure 4.31: Intrinsic Mobility as a function of the inversion charge divided by the electron charge. First curve correspond to the subtraction of the transistor capacitance of 300nm and 100nm gate length. Second curve is the extraction of the channel capacitance with the reference [Mor+21]. The last one is the channel capacitance as presented before.

In our study, the split CV method is performed with RF measurement which has the advantage of computing the mobility at $V_{ds} = 0V$ but the results are similar to the mobility extracted with DC measurement presented in [Kus+16]. The split CV method tends to underestimate the mobility value because the inversion charge is too high. Conversely, the *Morelle's CV* method overestimates the mobility due to a lower inversion charge. For FD-SOI devices using the proposed method, the maximum effective mobility is found to be 278 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$. This values for FDSOI devices is consistent with other studies [Bec+19; Kus+16].

The effective mobility increases when the temperature decreases because the phonon scattering is reduced [BG17]. Surface roughness scattering has a considerable impact at high inversion charge, regardless of temperature. Additionally, Coulomb scattering can be the predominant mechanism at low charge density, particularly at low temperatures [BG17]. For this device, the effective mobility goes from 278 $\mathrm{cm}^2/V.s$ at room temperature to 771 $\mathrm{cm}^2/V.s$ at 4.2K which correspond to a multiplication by approximately 3 which is convenient with [Bec+19; BG17].

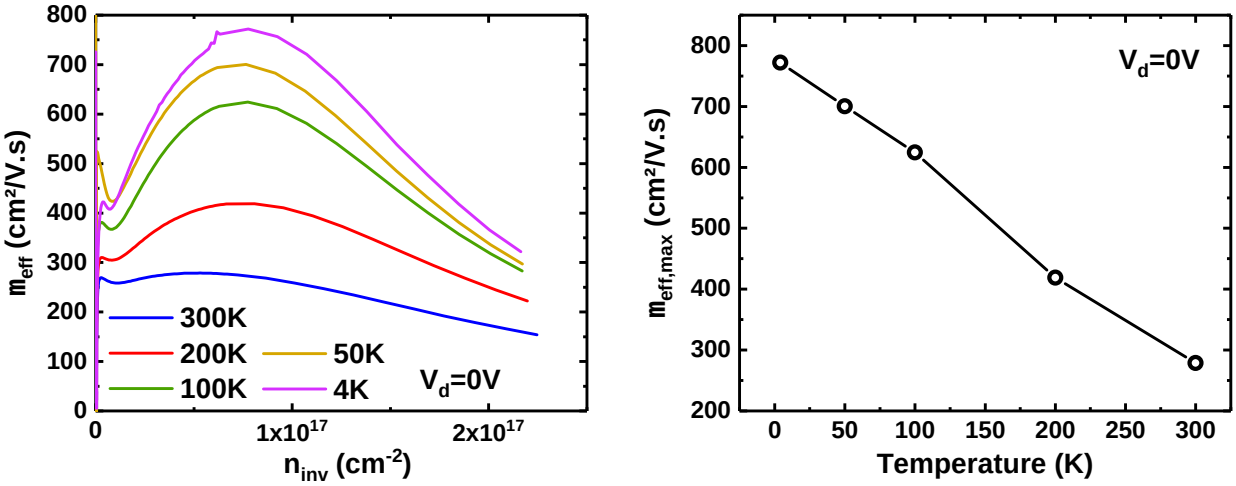

Figure 4.32: (Left) Intrinsic mobility as a function of the inversion charge divided by the electron charge from room down to cryogenic temperature. (Right) Maximum of the Intrinsic mobility as a function of the temperature.

4.5 Conclusion

This chapter has provided a detailed electrostatic analysis of FDSOI transistors from room temperature down to cryogenic temperature. We have demonstrated that as temperature decreases, the threshold voltage shifts. However, this shift can be compensated by adjusting the back-gate bias. Among the methods evaluated for threshold voltage extraction, the RF capacitance method, which relies purely on charge distribution, was found to be the most accurate, particularly for cryogenic temperatures and small device characterization.

Additionally, we showed that at low temperatures, dopant freeze-out occurs in the back-gate well, leading to an increase in well resistance. This phenomenon was observed thanks to the RF capacitance extraction using the small signal equivalent model. The analysis of capacitance was further used to refine the classical split CV mobility extraction method and demonstrated that the mobility increases at cryogenic temperature.

The next chapter will explore the effects of threshold voltage shifts and back-gate freeze-out on the performance of transistors and circuits.

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Chapter 5

RF transistor performances in 28FDSOI technology

Contents

5.1 Introduction

In the previous section, the electrostatic characteristics of FDSOI transistors were analyzed. However, since transistors are integrated into a circuit, it is essential to assess their performance under polarization.

This section is devoted to a comprehensive and rigorous characterization of transistor electrical performance across a wide range of temperatures, from room temperature down to cryogenic levels. This chapter begins by presenting the various transistor figures of merit, including the analog gain, the transition frequency, and the maximum oscillation frequency. Subsequently, the chapter addresses the self-heating effect, which can lead to a significant increase in the channel temperature and affect the device performances.

5.1.1 DC characterization

We have seen in the previous chapter that, as the temperature is lowered, the threshold voltage is shifted toward higher values, and the drain current in strong inversion is increased. Figure 5.1 presents the drain current measured as a function of the front gate voltage for different temperatures and different back-gate voltages.

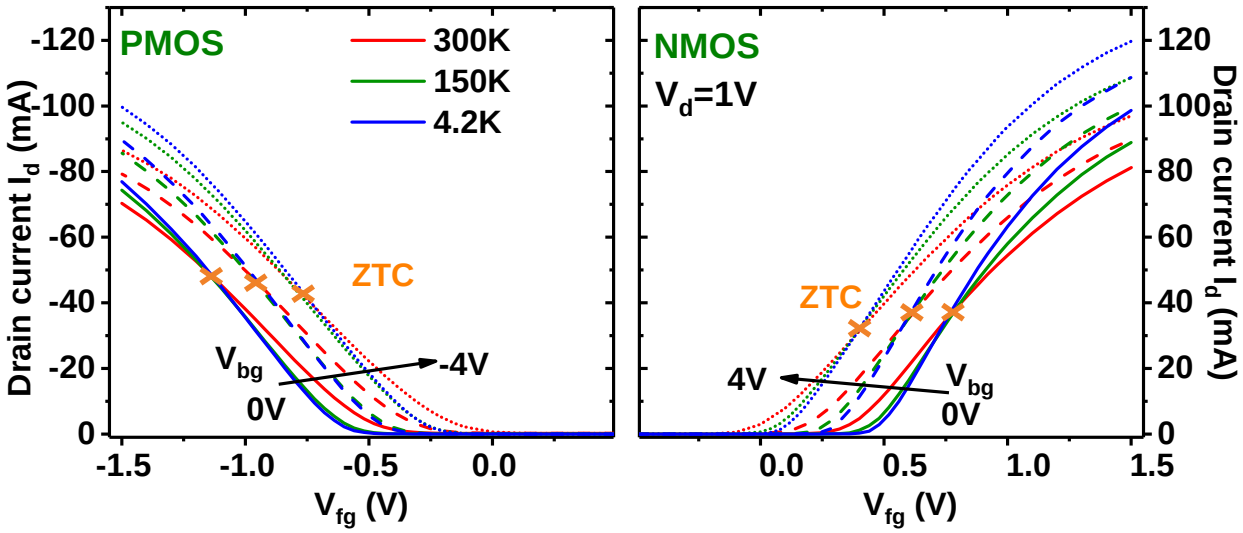

Figure 5.1: Drain current (in linear scale) as a function of the front gate voltage for different temperatures and different back-gate voltages. For a given back-gate voltage, all curves intersect at one point, the Zero Temperature Coefficient (ZTC)

On these graphs, we also notice that at each V_{bg}, the curves measured at different temperatures cross at one point, defined as Zero Temperature Coefficient (ZTC). At this particular gate bias, the drain current is independent of the temperature. This ZTC point is observed for the drain current, but also for the gate-to-channel capacitance C_{gc}. As explained in chapter 1 and in [Cat+22], this point is a consequence of the carrier population controlled by the Fermi-Dirac function.

Figure 5.2 and Formula 5.1 [Cat+22] show that the ZTC point increases linearly with the back-gate voltage, with a slope depending on the oxide, box and silicon capacitances. The same linear dependence is evidenced for NMOS and PMOS.

$$V_{\text{fg,ZTC}} = V_{\text{FB}} + \lambda k_B T + V_0 + \frac{Q_i(\lambda k_B T/q, T)}{C_{\text{ox}}} + \frac{C_b(\lambda k_B T/q + V_0 - V_{\text{bg}})}{C_{\text{ox}}} \tag{5.1}$$

where: V_{FB}: flat band voltage, k_B: Boltzmann constant, T: temperature, Q_i: inversion charge, q: electron charge, C_{ox}: oxide capacitance, $V_0 = \frac{E_g}{2}$, $C_b = \frac{1}{\left(\frac{1}{C_{\text{box}}} + \frac{1}{C_{\text{Si}}}\right)}$.

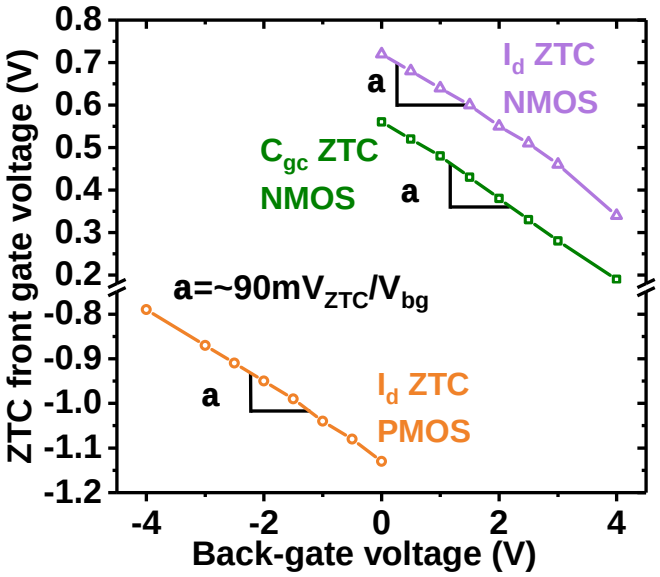

Figure 5.2: Zero Temperature Coefficient (ZTC) as a function of back-gate voltage. Identical slope for NMOS and PMOS of 90mV_{ZTC}/V_{bg}.

The slope of the ZTC voltage with respect to the back-gate bias has the same value as the slope of the threshold voltage vs. V_{bg}, which has already been presented in chapter 4. The occurrence of a of ZTC point is an interesting property that can be exploited, as presented in the following section of this chapter.

5.2 RF figure of merit extraction and calculation

This section presents three different transistor figures of merit as in [Kil+21]: the transistor gain A_v which is equal to the transconductance divided by the drain to source conductance. The transition frequency and the maximum oscillation frequency which are the frequency where the current gain is equal to 1 ($\frac{I_d}{I_g} = 1$) and the frequency where the Mason gain is equal to 1 (U=1).

5.2.1 Conductances and transistor gain

The transconductance g_m as a function of the front gate voltage is presented in figure 5.3.At both room and cryogenic temperatures, the application of back-gate bias shifts the drain current to lower front-gate voltages. Consequently, the transconductance (g_m) is also shifted to lower front-gate voltages due to the back-gate bias. The g_m maximum is higher at low temperature than at room temperature because the mobility increases when the temperature drops [Bec+19].

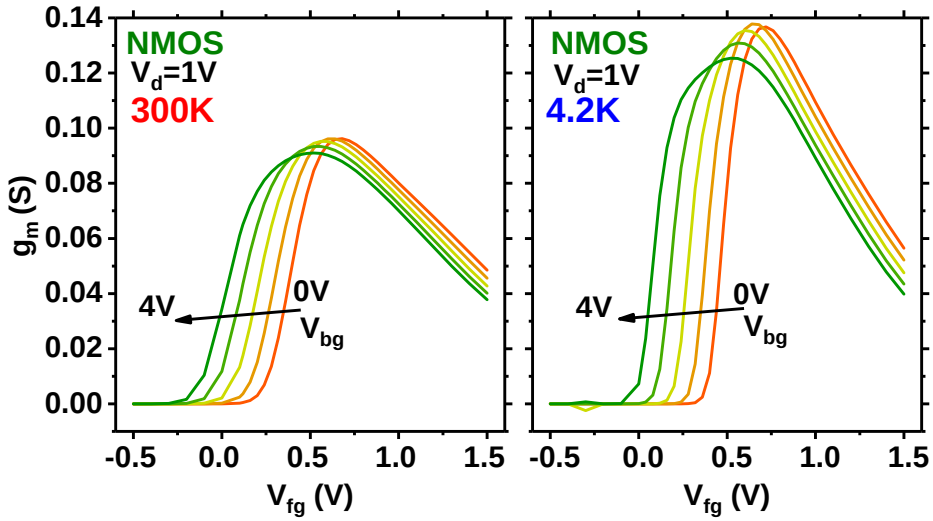

Figure 5.3: Transconductance as a function of the front gate voltage for different back-gate voltage at room temperature (Left) and at 4.2K (Right). g_m is computed by averaging data from 1 to 3GHz.

As demonstrated in [Col04] in FD-SOI, the transconductance value at high drain voltage is equal to:

$$g_m = \frac{\mu_n C_{ox} \frac{W}{L} (V_{fg} - V_{th})}{(1 + \alpha)} \tag{5.2}$$

where μ_n is the electron mobility, C_{ox} is the front oxide capacitance, W and L are the transistor gate width and length respectively, V_{th} the threshold voltage and $\alpha = \frac{C_b}{C_{ox}}$ with C_b the capacitance between the inversion channel and the ground.

As the back-gate voltage increases, the back interface becomes increasingly inverted, leading to a rise in the value of C_b and, consequently, a reduction in transconductance, as shown in the previous graph for all temperatures. However, at 4.2K, the maximum transconductance is lower at a back-gate voltage of 0V compared to $V_{bg} = 1V$. This reduction is attributed, as explained in [HDE22], to the amplified effect of surface roughness scattering at cryogenic temperatures, which lowers the channel mobility when the channel is near the front oxide interface (i.e., at $V_{bg} = 0V$). Since mobility is reduced, the transconductance decreases as well.

The drain to source conductance, measured by DC and RF technique, and normalized by total gate width, is plotted as a function of the front gate voltage in figure 5.4.

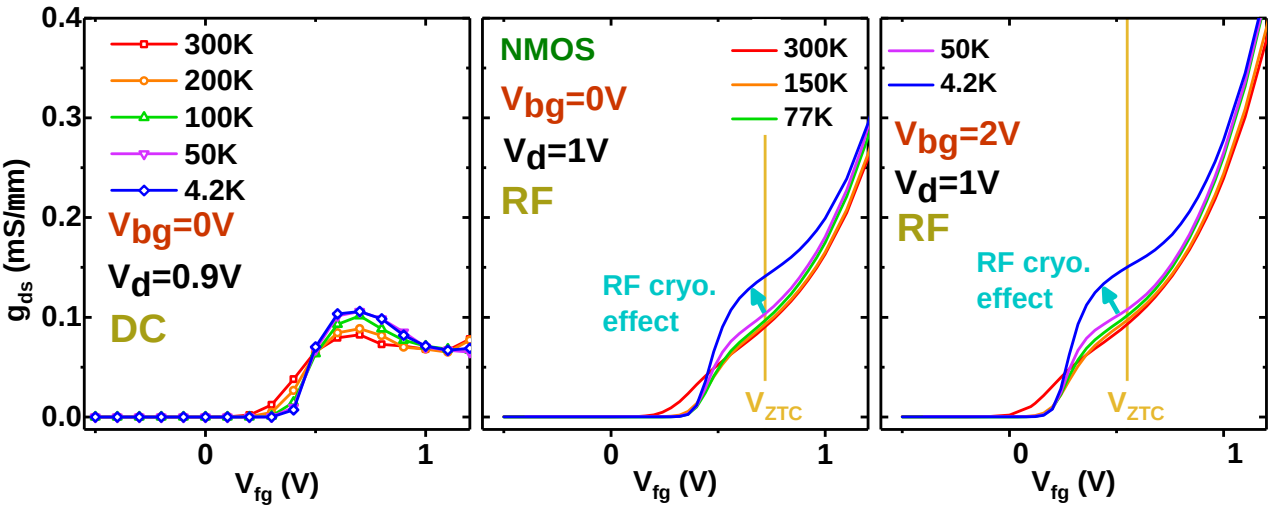

Figure 5.4: Drain to source conductance as a function of the front gate voltage. DC measurements (Left) and RF measurements (Right). RF cryogenic effect around $V_{fg=0.5V}$. Extracted between 1 and $3GHz$.

The conductance rises continuously with decreasing temperature because of the enhanced mobility. However, in the RF domain, the conductance shows a sudden bump between 50K and 4.2K. To better understand this effect, we plotted on figure 5.5 the drain to source conductance as a function of the frequency.

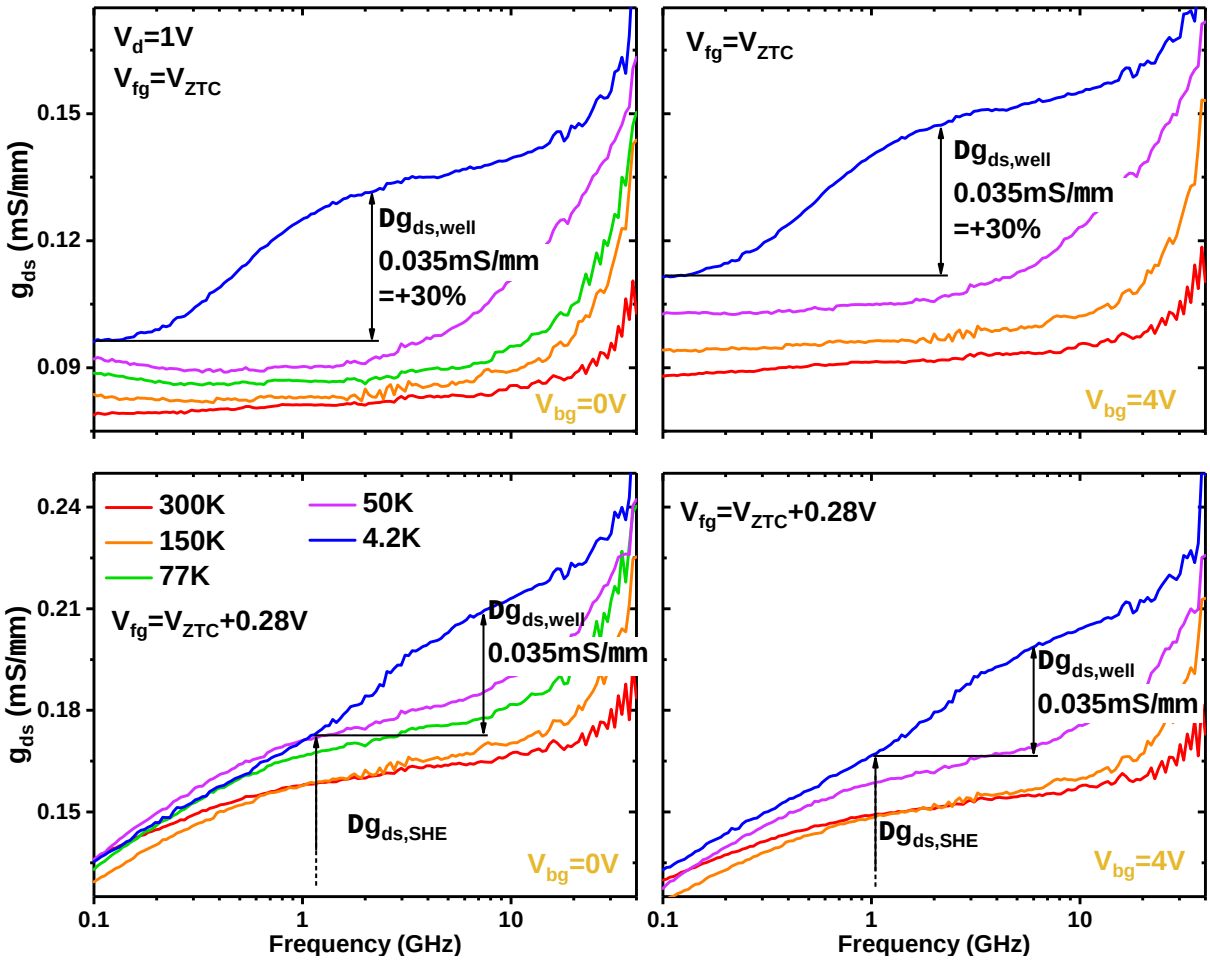

Figure 5.5: Drain to source conductance as a function of the frequency. At $V_{fg} = V_{ZTC}$, g_{ds} is independent of the Self Heating Effect (SHE) and only impact by the well.

At every temperature, the drain to source conductance frequency dependence is impacted by the Self-Heating effect as demonstrated in [Rin01; Mak+13]. This dependence can be expressed with the following equation:

$$g_{ds} \approx g_{ds,DC} + \mathrm{Re}(Z_{th}) \cdot \frac{dI_d}{dT_A} \cdot (g_{ds,DC} V_d + I_d) \tag{5.3}$$

where $g_{ds,DC}$ is the drain to source conductance in DC, Z_{th} is the frequency dependent thermal impedance.

As presented in figure 5.5 (Bottom), the self-heating effect involves a bump before 1 GHz. To see the temperature impact we removed the Self heating effect. To do so, L. Nyssens [Nys+21] suggested to extract the drain to source conductance at the ZTC voltage (observe 5.5 Top) . At this voltage, by definition, the drain current becomes independent of temperature variations ($\frac{dI_d}{dT_A} = 0$). Using equation

5.3, the drain-to-source conductance is no longer influenced by Z_{th}, meaning that the self-heating effect does not affect the g_{ds} curve. Consequently, at the ZTC voltage, only the well resistivity impacts g_{ds}, allowing it to be observed separately from the self-heating effect.

It has been previously demonstrated that the source–to-drain coupling through the well increases the drain-to-source conductance [Mak+11; Kil+03]. In [Kil+03], it was shown that the doping concentration of the well affects both the position and amplitude of this increase. Specifically, higher silicon doping levels shift the coupling effect to higher frequencies. In our case, with a well that is heavily doped (around 10^{20} cm^{-3} in 28nm FD-SOI technology), the source-to-drain coupling through the well occurs at higher frequencies and is not observed up to 40 GHz.

However, at cryogenic temperatures, as previously explained, the well suffer from dopant freeze-out, significantly reducing its active dopant concentration. In this case, the effectiveness of the ground plane is lost, and the source-to-drain coupling through the well begins to affect the drain-to-source conductance at lower frequencies. This results in a 0.035 mS/μm (30% seen at 1 GHz) $g_{\text{ds}}(f)$ rise above its DC value at 4.2 K. These effects are consistent regardless of the applied back bias.

This increase is also seen at 4.2K on Figure 5.5 (Bottom), at $V_{\text{fg}} = V_{\text{ZTC}} + 0.28V$. Since $V_{\text{fg}} \neq V_{\text{ZTC}}$, two phenomena affect $g_{\text{ds}}(f)$: self-heating effect at low frequencies (10 MHz) [Mak+13] leading to the first bump and the previously discussed well freezing effect (seen 1 GHz at 4.2 K) leading to the second bump.

In this section, we have observed the temperature dependence of both trans-conductance and drain-to-source conductance. A decrease in temperature results in an enhancement of g_m, which can be attributed to an increase in mobility. As the temperature decreases, the g_{ds} exhibits an increase, reaching a sudden peak at 4.2 kelvin due to the back-gate freeze-out effect. These two parameters have been subjected to detailed analysis because they are the two contributors to the voltage gain figure of merit (A_v).

The analog figure of merit, the voltage gain ($A_{\text{v}} = \frac{g_{\text{m}}}{g_{\text{ds}}}$) as a function of the front gate voltage is shown in figure 5.6. For the RF curves, A_v is extracted between 1 and 5 GHz, so it is impacted by the freeze out effect presented before.

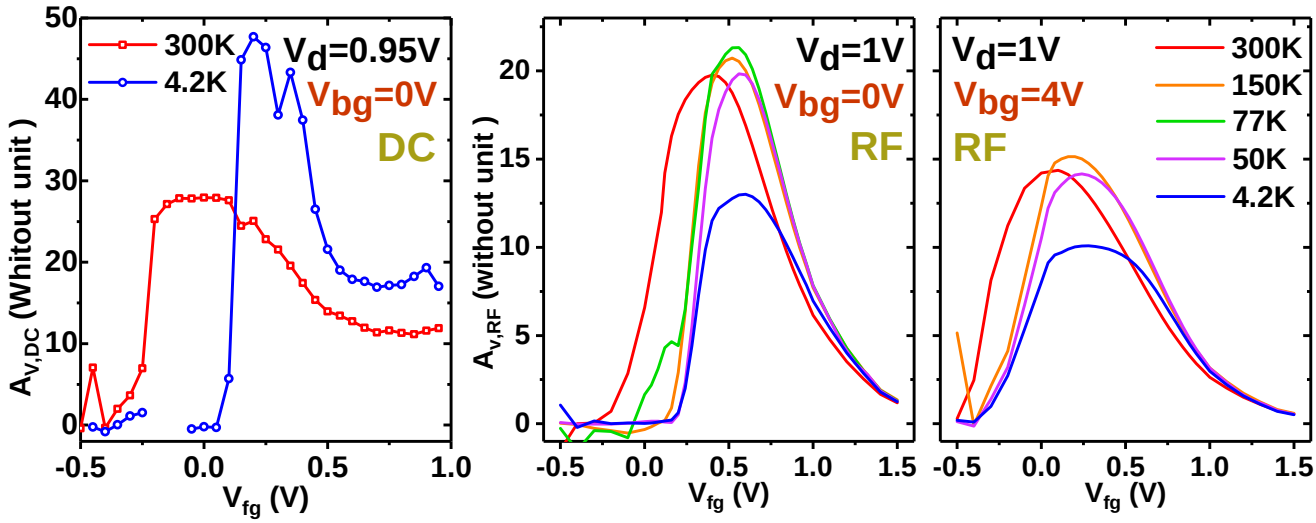

Figure 5.6: Voltage gain ($A_v(V_g) = \frac{g_m(V_g)}{g_{ds}(V_g)}$) as a function of the front gate voltage. (Left) DC measurement (right) RF measurement

In the DC measurements shown in figure 5.6 (left) the maximum voltage gain increases between 300 K and 4.2K, primarily due to enhanced carrier mobility, which increases g_m. Since the dopant freeze-out in the back-gate impacts the drain-to-source conductance around 1 GHz at 4.2K (as seen in figure 5.5), the RF voltage gain measured at high frequency has a different temperature behavior. the maximum voltage gain increases between 300 K and 77 K, primarily due to enhanced carrier mobility. However, below 77 K, the gain begins to stabilize and then decreases, a result of dopant freeze-out in the back-gate, which raises well resistance and increases the drain-to-source conductance (as shown before). At higher back-gate voltages, the maximum voltage gain measured in RF, follows a similar trend, but with lower values, consistent with the decrease in transconductance observed before with increased back bias.

In conclusion, the temperature influence on the transconductance, the drain-to-source conductance, and the voltage gain has been demonstrated. Moreover, while these parameters can be extracted from DC measurements, their temperature behavior differs at high frequencies due to back-gate dopant freeze-out. In this context, RF measurements provide critical complementary insights to DC measurements in the full device analysis.

5.2.2 Transition and maximum oscillation frequency

In this section, the RF figures of merit (transition frequency f_t and maximum oscillation frequency f_{max}) are presented as a function of temperature and as a function of back-gate voltage. f_t is extracted from the linear extrapolation of the current gain (h_{21} at 0 dB, using a fit with a fixed slope of 20 dB/dec) (figure 5.7) [Nys+20].

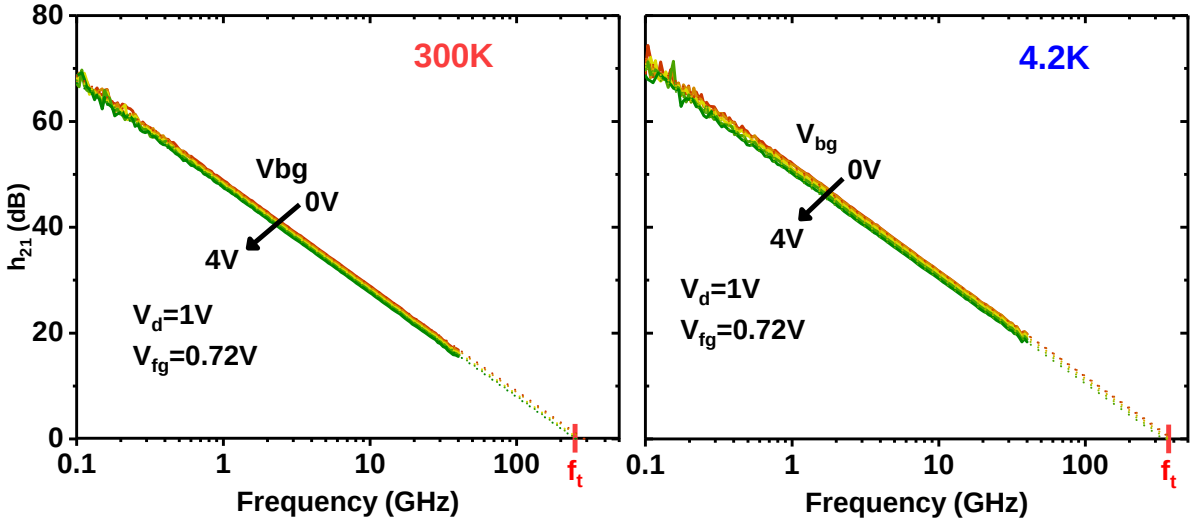

Figure 5.7: Current gain h_{21} as a function of frequency used to extract the transition frequency (f_t) at room (left) and cryogenic temperature (right). Characterized transistor is an NMOS with 28nm gate length and 80 fingers of 1μm gate width.

The extracted transition frequency is plotted as a function of V_{bg} and T in figure 5.8. We observed that the transition frequency reduces as the back-gate voltage or temperature increases (figure 5.8). The f_t increase due to temperature is similar to the results presented in [Nys+20], where 28FD-SOI technology is measured as well. This behavior is also observed in [Cha+21] in 22 nm FD-SOI technology. This trend is explained by the transconductance maximum drop with the temperature or back-gate bias increase. As for g_m, at 4.2K and $v_{bg} = 0V$ the f_t value is lower than at $v_{bg} = 1V$. This variation can be explained by the amplified effect of surface roughness scattering at cryogenic temperatures, which lowers the channel mobility when the channel is near the front oxide interface [HDE22]. f_t can be calculated with the equation $f_t = \frac{g_m}{2\pi C_{gg}}$, using the measured g_m and C_{gg}.

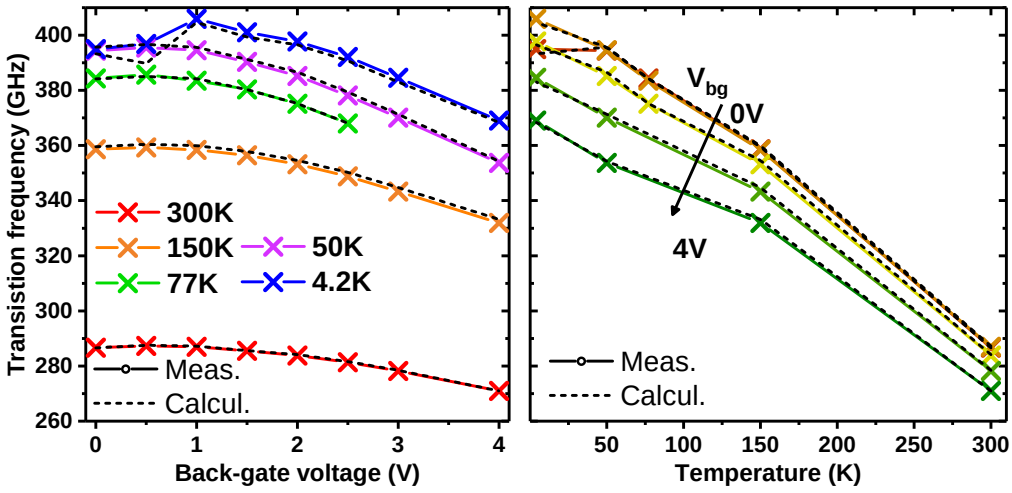

Figure 5.8: Transition frequency as a function of the back-gate voltage (left) and of the temperature (right). Calculation is performed using $f_t = \frac{g_m}{2\pi C_{gg}}$

The values of $f_{\max}$ are extracted from the linear extrapolation of Mason's gain (U with a fit at -20 dB/dec) (figure 5.9) [Nys+20], and plotted as a function of the back-gate voltage and the temperature. The maximum oscillation frequency decreases with the increasing back-gate bias, in agreement with the lower transition frequency (figure 5.10).

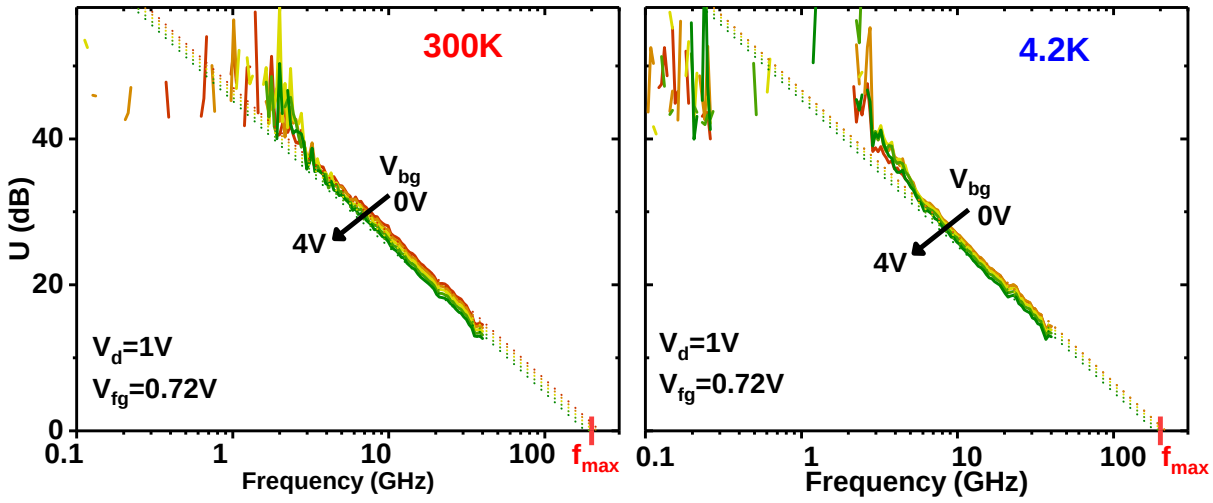

Figure 5.9: Mason gain respectively used to extract the maximum oscillation frequency (f_{max}) at room and cryogenic temperature.

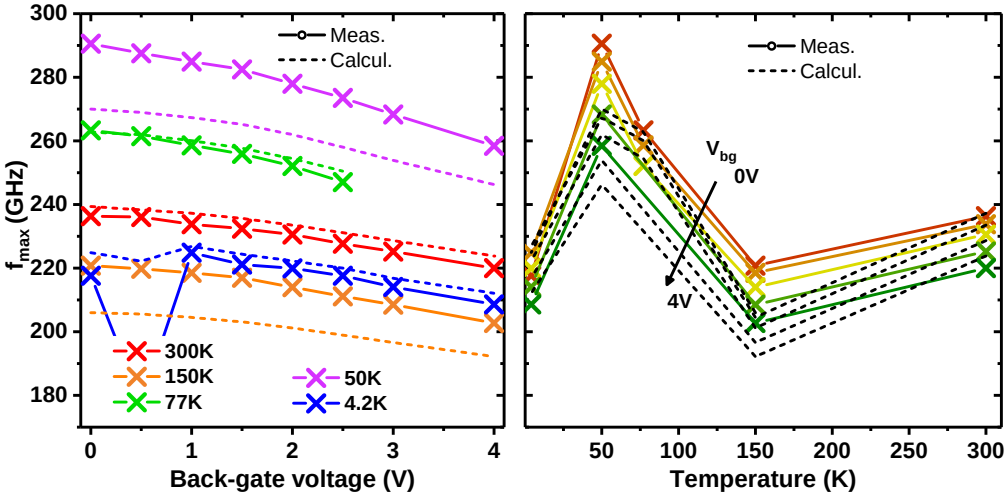

Figure 5.10: Maximum oscillation frequency as a function of the back-gate voltage (Left) and of the temperature (Right). Calculation is performed using $f_{\max} = \frac{f_t}{2\sqrt{2\pi f_t R_g C_{gd} + (R_s + R_g) g_{ds}}}$

On the other hand, the temperature dependence is not clearly evidenced due to the inaccuracy of $f_{\max}$ extraction (figure 5.10). As demonstrated in [Nys+20; Cha+21], the value of $f_{\max}$ appears to increase with a reduction in temperature. This is primarily due to an increase in transition frequency and a reduction in front gate access resistance [Nys+20]. $f_{\max}$ can also be calculated by

$$f_{\max} = \frac{f_{\mathrm{t}}}{2\sqrt{2\pi f_{\mathrm{t}} R_{\mathrm{g}} C_{\mathrm{gd}} + (R_{\mathrm{s}} + R_{\mathrm{g}}) g_{\mathrm{ds}}}}$$

.

As evidenced by the formula, the maximum oscillation frequency is dependent on the front gate access resistance. The values of R_g as a function of the temperature are extracted with Bracale's method [Bra+00]is presented in 5.11.

Since the cryogenic measurements are performed using a manual prober, both the contact quality and pad condition vary with each measurement, impacting the contact resistance and consequently the access resistance. As noted in [Pen+09], the contact resistance can fluctuate by more than 10 Ω depending on the applied force during probing. As a result, achieving consistent measurements of the front gate access resistance is challenging, with the values varying between 8 Ω and 14 Ω, corresponding to a 75% variation. This inconsistency introduces uncertainty in the extraction of f_{max}, leading to a variation of approximately 30%.

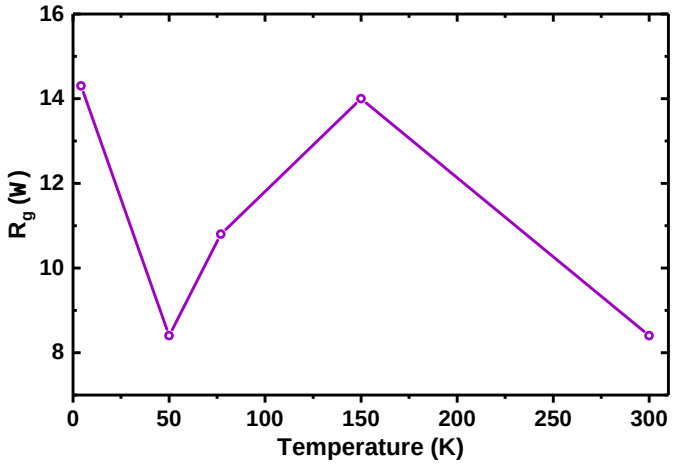

Figure 5.11: Gate access resistance as a function of the temperature. The resistance is extracted with Bracale's method [Bra+00] presented in chapter 2.

5.3 Self Heating Effect (SHE)

In FDSOI devices, the dissipation of heat generated at the drain side is impeded by the use of low thermally conductive materials, such as the buried oxide (BOX) and the thin silicon layer forming the channel. This phenomenon gives rise to significant self-heating effect (SHE), which results in a notable high channel temperature when the device is in the ON state. Such temperature increase can have a detrimental impact on device performance, resulting in reduced carrier mobility, a shift in the threshold voltage, and a deterioration in the device reliability. These challenges present significant obstacles for IC design. Although extensive experimental and theoretical studies have addressed self-heating, there is a paucity of research on self-heating at cryogenic temperatures, with a lack of experimental data in advanced technology node FDSOI devices. At low temperatures, the thermal properties of most semiconductors and metals differ significantly from those at room temperature, particularly the thermal conductivity of crystalline silicon and silicon oxide (SiO_2), which are highly temperature-dependent.

The device temperature is expressed by the following equation [Cas+22; Tri+19]:

$$T_{device} = T_A + \Delta T = T_A + R_{th}(T_A, P) \cdot V_d I_d \tag{5.4}$$

where T_A is the ambient temperature, ΔT is the temperature variation due to Self Heating Effect (SHE), P the power and R_{th} the thermal resistance which is ambient temperature and power dependent [Ber+24].

A reduction in the gate length of MOSFETs results in an increase in current and power densities, which increases the SHE. Two distinct forms of self-heating have been identified in the literature [Rin01; Mak+13]:

- **Static self heating effect** : power dissipation due to the DC bias.
- **Dynamic self heating effect** : power dissipation due to the AC signal and it affects the Y-parameters across frequencies. The phenomenon of dynamic self-heating is contingent upon the frequency of the AC signal. The poor heat dissipation caused by the buried oxide (which has a low thermal inertia) impedes the temperature to follow the AC signal at high frequencies.

In RF, the thermal response of an FD-SOI device is characterized by the thermal impedance (Z_{th}), a measurement of the temperature rise in response to power dissipation [Rin01]. This thermal impedance can be modeled as a combination of thermal resistance (R_{th}), which quantifies the device resistance to heat flow and relates the average temperature rise; and thermal capacitance (C_{th}) which accounts for the delay in temperature change due to heat storage in the materials [Mak+13]. Mathematically, Z_{th} can be expressed as a function of R_{th} and C_{th}, similar to an electrical RC network, where R_{th} controls the magnitude of the temperature rise, and C_{th} dictates the time constant, defining the speed of the thermal response to power changes. This model allows for both dynamic and static analysis of self-heating effects in FD-SOI devices [Rin01].

In RF as there is an AC signal around a given DC bias, the measurement is impacted by both static and dynamic SHE. In [Rin01], Rinaldi detailed how the Y-parameters are linked to the thermal impedance Z_{th} and he obtains the following equation:

$$Y_{ij} = Y_{ij,T} + Z_{th}\frac{\partial I_i}{\partial T_A}\left(V_g Y_{1j,T} + V_d Y_{2jT} + I_j\right) \tag{5.5}$$

Where Z_{th} is the thermal impedance, i and j correspond to the port consider for RF measurement (gate or drain for the transistor), Y_{ij} is the Y-parameters and $Y_{ij,T}$ is Y_{ij} without the dynamic self-heating.

To characterize the SHE, this section is dedicated to the extraction of the thermal impedance Z_{th}.

5.3.1 Thermal effects analysis using RF measurements

As it was demonstrated in [Rin01], the thermal impedance can be extracted from RF measurement. Dynamic self-heating varies with frequency. The self-heating results from a thermal impedance Z_{th} is expressed by [Rin01] :

$$\Delta Y_{22,\text{SHE}} = \frac{\partial I_d}{\partial T}\frac{\partial T}{\partial V_{ds}} \tag{5.6}$$

$$dT = Z_{th}\left((I_d dV_{ds}) + (V_{ds} dI_d)\right) \tag{5.7}$$

$$\frac{dT}{dV_{ds}} = Z_{th}\left(I_d + V_{ds}\frac{dI_d}{dV_{ds}}\right) = Y_{22,\text{noSHE}} \tag{5.8}$$

$$Z_{th} = \frac{\Delta Y_{22,\text{SHE}}}{\frac{\partial I_d}{\partial T}\left(I_d + V_{ds} Y_{22,\text{noSHE}}\right)} \tag{5.9}$$

$$\Leftrightarrow \begin{cases} Re(Z_{th}) = \frac{Re(\Delta Y_{22,\text{SHE}})}{\frac{\partial I_d}{\partial T}\left(I_d + V_{ds} Re(Y_{22,\text{noSHE}})\right)} = \frac{\Delta g_{ds,\text{SHE}}}{\frac{\partial I_d}{\partial T}\left(I_d + V_{ds} g_{ds,\text{noSHE}}\right)} \\ Im(Z_{th}) = \frac{Im(\Delta Y_{22,\text{SHE}})}{\frac{\partial I_d}{\partial T}\left(I_d + V_{ds} Im(Y_{22,\text{noSHE}})\right)} \end{cases} \tag{5.10}$$

where $\Delta Y_{22,\text{SHE}}$ is the drain to drain admittance variation between low frequency and high frequency (for which the dynamic self heating has disappeared), $Y_{22,\text{noSHE}}$ is the drain to drain admittance at high frequency, where the dynamic self heating has disappeared).

Figure 5.12 shows the real and imaginary part of the thermal impedance Z_{th} at room temperature as a function of the frequency. The thermal resistance R_{th} corresponds to the value of $Re(Z_{th})$ at low frequency.

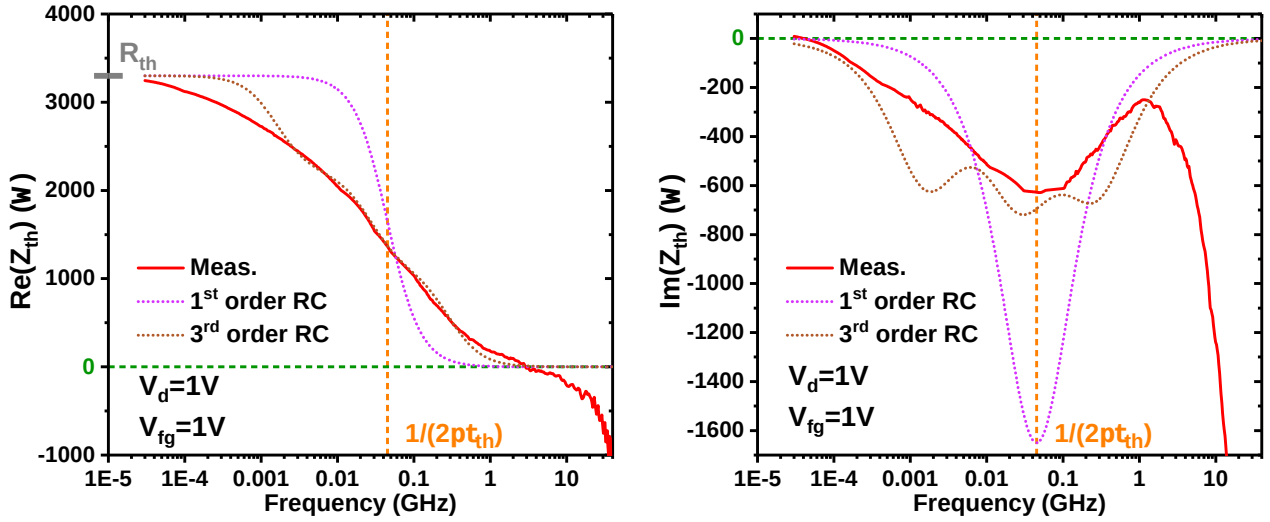

Figure 5.12: (Left) real and (right) imaginary part of thermal impedance as a function of frequency. The thermal resistance correspond to the extrapolation of the real curve at 0Hz. The thermal impedance is fitted using a 1^{st} order RC circuit or a 3^{rd} order RC

As demonstrated in [Rin01; Mak+13] and illustrated in Figure 5.12, the thermal impedance can be modeled as a first-order RC network, comprising a thermal resistance R_{th} and a thermal capacitance C_{th}. The thermal resistance R_{th} is obtained from the value of $\text{Re}(Z_{th})$ at low frequencies, yielding $R_{th} = 3.3\,\text{kK/W}$ in this case. This result aligns with previous studies, such as those presented in [Ber+24; Tri+19; Mak+13], where the thermal resistance is derived using the gate resistance thermometry technique. In FD-SOI device, the thermal resistance is higher than in bulk device [Mak+16]

due to BOX which has a low thermal conductivity [Tri+19].

The characteristic thermal frequency f_{th} can be determined by the relation $f_{th} = \frac{1}{2\pi R_{th} \times C_{th}}$, corresponding to the frequency at which the dynamic self-heating effect disappears. Consequently, the thermal time constant τ_{th} is calculated as $\tau_{th} = \frac{1}{2 \cdot \pi \cdot f_{th}}$. This constant represents the time required for the transistor channel current flow to adapt to a change at 300K. Given the first-order RC network, f_{th} is identified as the frequency at the minimum of $\mathrm{Im}(Z_{th})$. From Figure 5.12, f_{th} is determined to be $45\,\mathrm{MHz}$, resulting in $\tau_{th} = 3.5\,\mathrm{ns}$. This value is in good agreement to the one presented in [Mak+16]. Above this frequency, the impact of the dynamic self-heating is significantly reduce but always impacted by the static self-heating.

However, as can be seen on figure 5.12, due to distributed thermal spreading effects in the BOX, in the well and in the substrate [Rin01], a first-order RC network is not sufficient to fit well the thermal impedance measurement. In our case a third-order RC network allows us to fit the measurement. The measurement is fitted using ADS software. The RC networks are presented in figure 5.13:

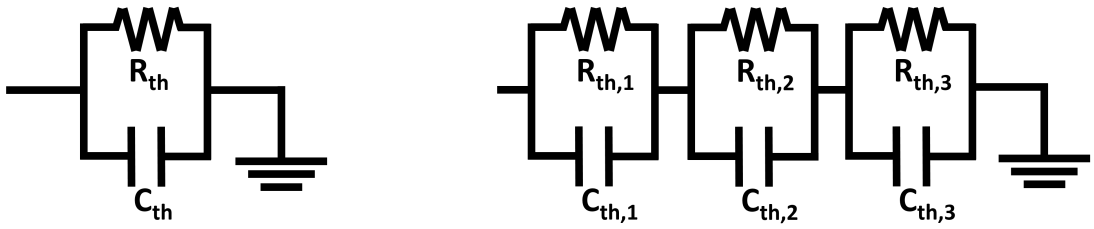

Figure 5.13: (Left) first-order RC network (right) third-order RC network used to model the thermal impedance

The value of the different thermal resistance and thermal time constant used to fit the thermal impedance in figure 5.12 are presented in table 5.1.

In the following, only the first-order RC network is considered because this network is sufficient to characterize how the device temperature rises and its ability to dissipate heat [Rin01]. Moreover, the third-order network is arbitrary fitted using ADS software and not physic behavior.

RC network	First-order	Third-order
$R_{th,1}$	$3.3kK/W$	$1.1kK/W$
$\tau_{th,1}$	$3.5ns$	$99ns$
$R_{th,2}$		$1.1kK/W$
$\tau_{th,2}$		$5.8ns$
$R_{th,3}$		$1.1kK/W$
$\tau_{th,3}$		$0.55ns$

Table 5.1: RC network parameters values

As previously explained and also discussed in [Nys+21], the drain-to-source conductance g_{ds} is impacted by the self-heating effect. The behavior of g_{ds} as a function of frequency at room temperature is presented in Figure 5.14. The relationship linking temperature variation and g_{ds} is described by the following equation:

$$g_{ds} \approx g_{ds,DC} + R_{th} \cdot \frac{dI_d}{dT_A} \cdot (g_{ds,DC} V_d + I_d) \tag{5.11}$$

As explained in [Mak+13], the variation in g_{ds} is attributed to self-heating, specifically the deactivation of dynamic self-heating at high frequencies, which leads to an increase in the drain-to-source conductance. Using the curve in figure 5.14 and equation 5.11, the real part of the thermal impedance can be expressed as:

$$\mathrm{Re}(Z_{th}) = R_{th} = \frac{g_{ds,HF} - g_{ds,DC}}{(g_{ds,DC} V_d + I_d) \cdot \frac{dI_d}{dT_A}} = \frac{\Delta g_{ds}}{(g_{ds,DC} V_d + I_d) \cdot \frac{dI_d}{dT_A}} \tag{5.12}$$

In the figure 5.14 (left), the thermal resistance is extracted as $R_{th} = 3.5\,\mathrm{kK/W}$, which is in good agreement with the value found previously. In [Jin+01], an empirical method is proposed to calculate the thermal time constant and the thermal frequency. The thermal frequency is defined as the frequency at which:

$$g_{ds} = g_{ds,DC} + \frac{\Delta g_{ds}}{3} \tag{5.13}$$

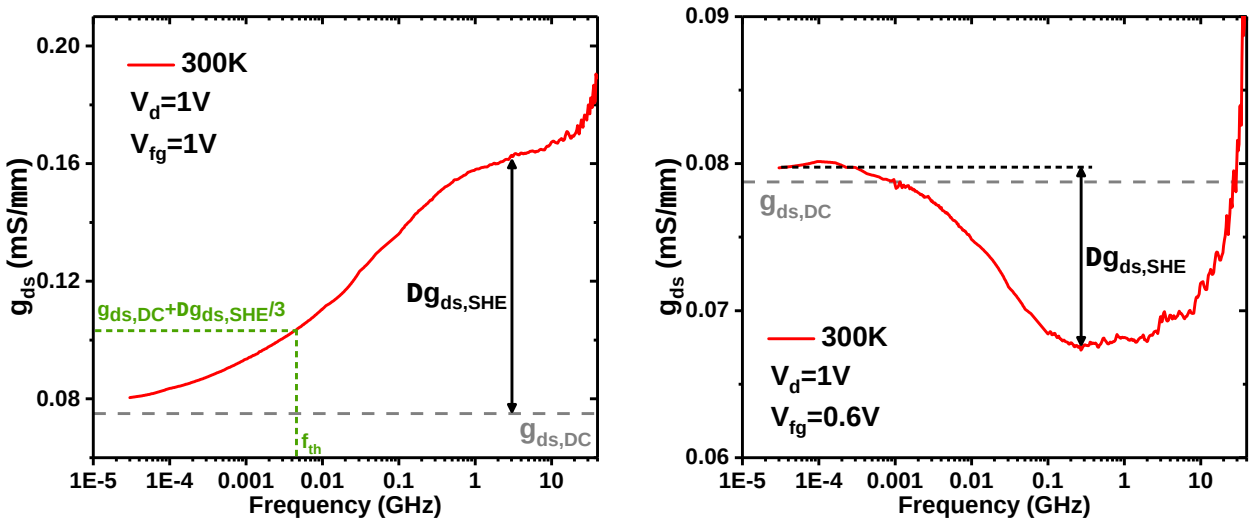

Figure 5.14: Drain-to-source conductance as a function of frequency at room temperature at (left) high and (right) low front gate voltage. The DC conductance was measured separately. The characterized transistor is an NMOS with a 28 nm gate length and 80 fingers, each with a 1 μm gate width.

Using this method, we find $\tau_{th} = 30\,\text{ns}$, which is higher than the previously determined value. The method propose in [Jin+01] is purely empirical and considers a dependence of the phenomenon as $\exp(-t/\tau_{th})$; where t is the time and when $t = \tau_{th}$, the considered parameter is divided by 3. In the RF extraction method, the method propose to extracted the thermal time constant directly on the measurement. Contrarily to [Jin+01], the RF method consider distributed thermal spreading effects in the BOX, in the well and in the substrate which can explain the difference between the two τ_{th} extracted. Moreover, [Jin+01] does not account for device geometry. However, as noted in [Mak+13], R_{th} is related to the surface area, which is used for heat dissipation, while C_{th} is related to the volume available for heat storage. Therefore, the thermal time constant is dependent on the surface-to-volume ratio, which results in a reduction of τ_{th}, a factor not considered in the method proposed by [Jin+01]. For subsequent analysis, the thermal time constant will be extracted as the frequency corresponding to the minimum of $\text{Im}(Z_{th})$.

As presented in figure 5.14 (right), the drain-to-source conductance g_{ds} decreases as the frequency increases. This behavior is due to the fact that the transistor is biased before the zero temperature coefficient (ZTC) point, where the drain current variation with respect to temperature is negative. According to equation 5.11, when dynamic self-heating deactivates, g_{ds} is expected to decrease with increasing frequency. Applying the same methodology, we find $R_{th} = 1.8\,\text{kK/W}$. As anticipated in [Tri+19], the thermal resistance value at room temperature varies slightly with power. However, it is observed in

figure 5.14 (right) that the drain-to-source conductance at high frequencies is impacted by measurement limitations, which artificially increase the value of g_{ds}, thereby reducing Δg_{ds} and consequently lowering the extracted R_{th}.

The same methodology can not be applied to the curve at 4.2K. As previously demonstrated in section 5.2.1, the well under the box freezes and the drain-to-source conductance curves are affected. Figure 5.15 presents the drain-to-source conductance as a function of frequency at cryogenic temperature. It is not possible to distinguish the impact of the self-heating and the well freeze-out on this curve. Consequently, it is not possible to extract a frequency without dynamic self-heating.

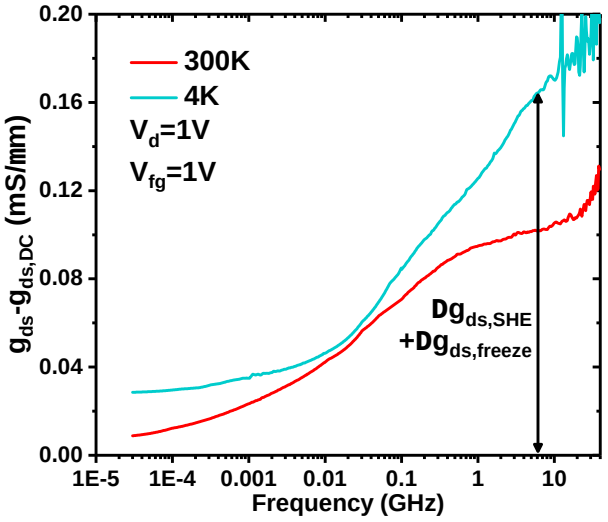

Figure 5.15: Drain to source conductance as a function of frequency at cryogenic temperature. The increase at high frequency is the sum of the self-heating effect and the back-gate freeze-out.

A methodology addresses this issue by separately analyzing the well and the self-heating effects using measurements taken at the zero temperature coefficient (ZTC) bias point [Nys+21; VRK23].

5.3.2 Zero-Temperature Coefficient

By definition, the ZTC is the front gate voltage for which the drain current is the same regardless of the temperature (i.e. $\frac{dI_d}{dT} = 0A/K$).

So as presented in [Nys+21] at this precise bias and with equation 5.11, the drain to source conductance is self heating independent and it becomes only influenced by the well effect. This impact is then removed from the curve obtained at other front gate voltages to only have the self-heating impact as presented in figure 5.16.

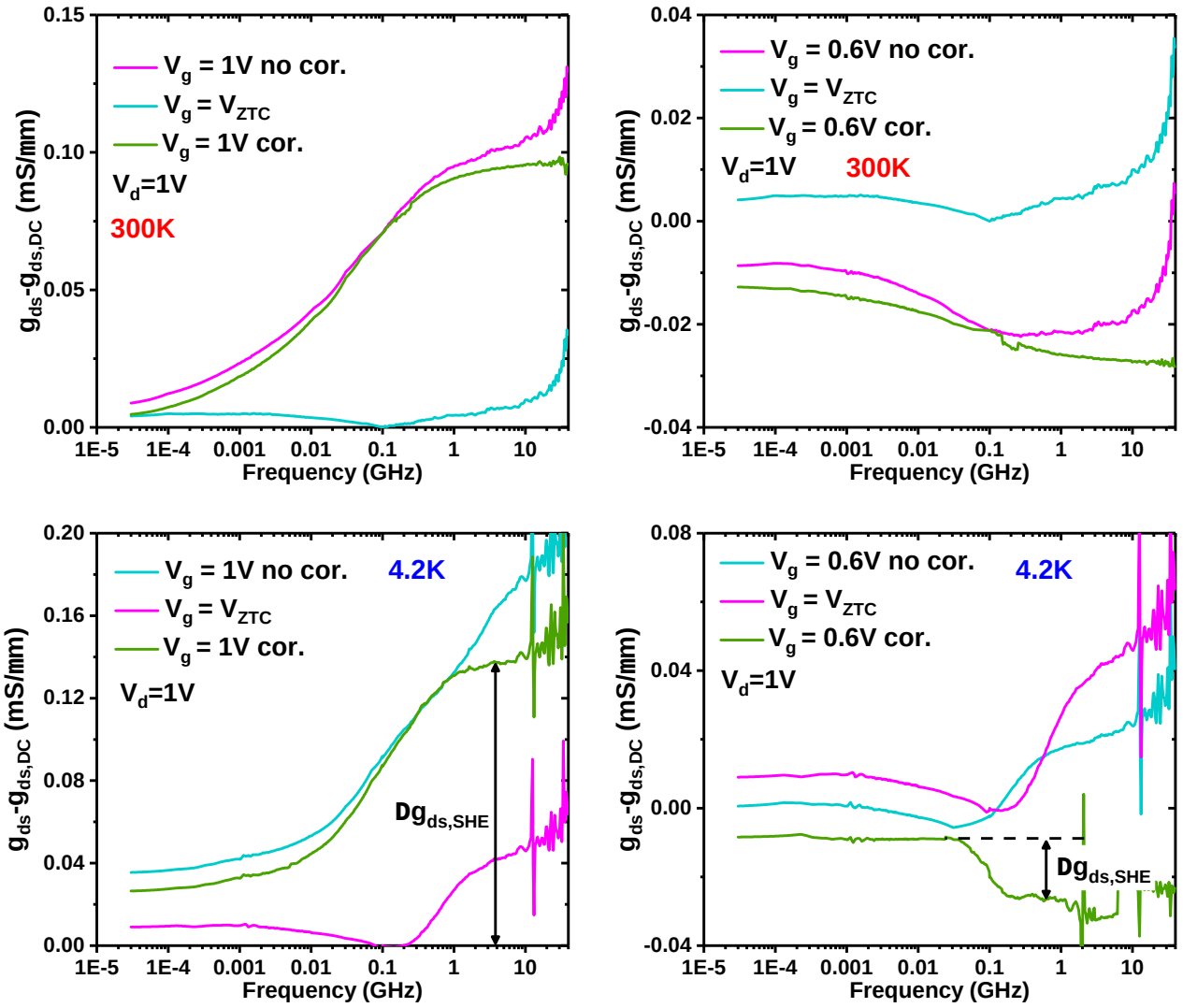

Figure 5.16: Drain to source conductance as a frequency function at cryogenic temperature with the detail of the well freeze out correction (Left) at $V_{fg} > V_{ZTC}$ and (Right) at $V_{fg} < V_{ZTC}$ at (top) room temperature and at (bottom) 4.2K.

At room temperature and a gate bias of 1 V (above the ZTC voltage), the impact of the correction is minimal. At $V_g = 0.6$ V (below the ZTC voltage), the correction eliminates the high-frequency increase in g_{ds}, resulting in a higher Δg_{ds} and an increase in the thermal resistance to 2.1 kK/W (compared to 1.8 kK/W without the correction).

At cryogenic temperatures, the correction helps remove the back-gate freeze-out effect on g_{ds} discussed in Section 5.2.1. At a gate voltage of 1 V (above the ZTC voltage), the correction reduces the variation in conductance, stabilizing it around 1 GHz when dynamic self-heating is deactivated. At

$V_g = 0.6\,\mathrm{V}$ (below the ZTC voltage), the frequency variation of drain-to-source conductance is initially positive, which is inconsistent with previous explanations since $\frac{dI_d}{dT_A} < 0$. After applying the correction, as expected, the conductance decreases as the temperature increases.

Following the application of the aforementioned correction, the thermal impedance can be computed, resulting in the graph shown in Figure 5.17.

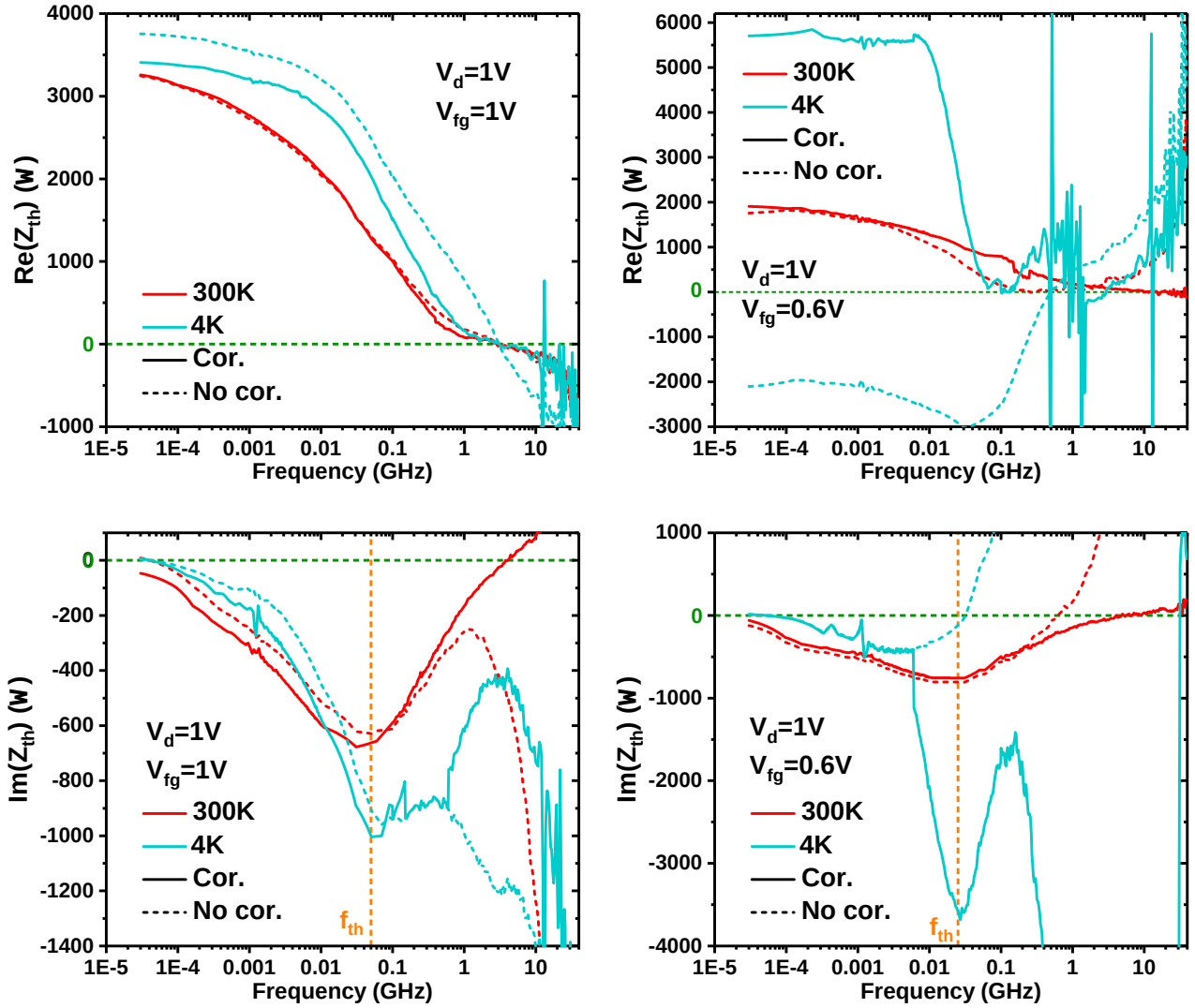

Figure 5.17: Thermal impedance (top) real and (bottom) imaginary part as a frequency function at room and cryogenic temperature with and without well freeze out correction (Left) at $V_{fg} > V_{ZTC}$ and (Right) at $V_{fg} < V_{ZTC}$

The correction has a minimal impact at room temperature but becomes significant at cryogenic temperatures, where the back-gate freeze-out behavior must be removed. At cryogenic temperatures

and a gate-to-source voltage of 1 V, the correction reduces the thermal resistance from $3.75\,\mathrm{kK/W}$ to $3.45\,\mathrm{kK/W}$ and allows the identification of $f_{th} = 48\,\mathrm{MHz}$ from the imaginary part. At a gate-to-source voltage of 0.6 V, the correction yields $R_{th} = 5.55\,\mathrm{kK/W}$ and $f_{th} = 25\,\mathrm{MHz}$.

At cryogenic temperatures, when $V_g = 1\,\mathrm{V}$, the power dissipation is higher than at $V_g = 0.6\,\mathrm{V}$, leading to a higher device temperature [Ber+24], which in turn induces a higher thermal resistance [Cas+22]. The decrease of the thermal frequency is directly link to the thermal resistance increase.

The thermal resistance is extracted from these curves at the low-frequency value of the real part of the thermal impedance. The thermal resistance values as a function of power at cryogenic temperatures, for a transistor with a 28 nm gate length and 80 fingers of 1 μm gate width, are presented in Figure 5.18. These values are compared to the thermal resistance extracted using the gate resistance thermometry technique in [Ber+24] on a different transistor with a 30 nm gate length and a single finger of 1 μm gate width.

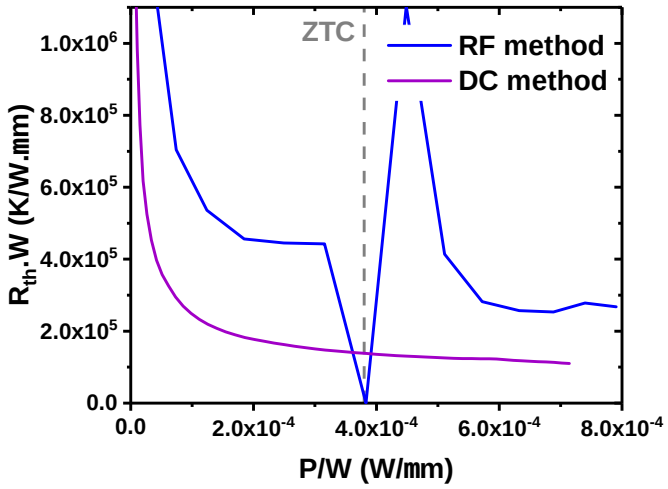

Figure 5.18: Thermal resistance as a function of power extracted at cryogenic temperatures using the RF method presented earlier, compared to the gate resistance thermometry technique from [Ber+24].

Around the ZTC voltage, the RF method shows outlying points due to two factors:

- Since the ZTC is used for correction, significant deviations from the ZTC curve are necessary.
- $\frac{dI_d}{dT_A}$ is inherently low and difficult to estimate near the ZTC point.

The thermal resistance values extracted using the RF method are compared with those obtained from the gate resistance thermometry technique in [Ber+24]. As shown in Figure 5.18, both techniques exhibit similar trends. R_{th} increases as the power decreases, particularly below 0.2 mW, where R_{th}

shows a significant rise by more than an order of magnitude. As the power increases, the device temperature rises, as demonstrated in [Ber+24]. The temperature dependence of R_{th} can be accurately described between room temperature and approximately 70 K by considering only the thermal conductivity of the gate silicon oxide [Ber+24], as the buried oxide primarily governs heat dissipation in thin-film SOI structures [Tri+19]. However, at temperatures below 70 K, the substantial increase in R_{th} is primarily attributed to the thermal conductivity of silicon [Cas+22].

The RF method exhibits a higher thermal resistance, which can be attributed to two factors. Firstly, the value of the derivative of the drain current with respect to temperature, dI_{d}/dT, has been assumed to be constant between 300K and 4.2K. However, this assumption is invalid at cryogenic temperatures[Cas+22] and it needs to be improve. Secondly, the design of the transistor differs between the DC measurement and the RF technique. In the former, the transistor has only one finger, whereas in the RF method, it has eighty fingers of 1 μm. The multiplicity of the finger increases the value of the thermal resistance due to the influence of the fingers on each other [Ber+24].

To conclude, this methodology presents good results in agreement with the literature. However there is an non-negligible uncertainty which is the way to determine $\frac{dI_d}{dT_A}$. As T_A is the device temperature we are looking for by extracting R_th, it is very complicated to correctly calculate $\frac{dI_d}{dT_A}$. In our study, $\frac{dI_d}{dT_A}$ has been determine by additional DC measurement and consider constant with the temperature which is a strong assumption needed to be improve [Cas+22].

5.4 Conclusion

In conclusion, the transistors RF figures of merits are significantly improved at low temperatures. The mobility increase at low temperature results in a higher transconductance which increase the values of the transition and maximum oscillation frequency (f_t and f_{max}). However the dopant freeze out in the back-gate well at cryogenic temperature increases the drain to source conductance at high frequency which results in an lower voltage gain. The dopant freeze out impacts the transistor performances at high frequency, so a noticeable difference exists between DC and RF performance, which cannot be overlooked. Similarly, RF measurements are affected by both the static and dynamic SHE, making it essential to complement DC measurements with RF analysis to fully understand the transistor behavior.

As demonstrated in this chapter, RF measurements provide crucial insights that are complementary to DC characterization. The high frequency transistor characterization is a necessary step to extract the small signal transistor model and to understand their frequency dependence at all interest temperature. This combination of DC and RF measurements is important for accurately characterizing and optimizing transistor behavior in cryogenic environments.

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Chapter 6

Low Noise Amplifier characterization and performance enhancement

Contents

6.1 Introduction

In the previous chapter, we presented a comprehensive characterization of FDSOI transistors, demonstrating that this technology is highly suitable for cryogenic circuits. One of its key advantages is the ability to control the threshold voltage using back-gate bias, making it a strong candidate for low-temperature applications.

It has been shown in previous works [Art+22; Nys+22; CL20] that the back-gate bias can be effectively used at room temperature to adjust both the gain and noise figure of circuits. The goal of this chapter is to extend this approach to cryogenic temperatures by characterizing a Low Noise Amplifier (LNA) and demonstrating how its performance can be enhanced through back-gate biasing of FDSOI transistors to compensate for undesired threshold voltage shifts at cryogenic temperatures.

Several LNAs have already been designed for operation at cryogenic temperatures [Lin+22; HTL24; Cag+23]. However, given the current lack of an RF cryogenic compact model, these designs often rely on various techniques to mitigate temperature-induced effects such as threshold voltage shifts. For example, *Caglar et al.* employed a 28nm CMOS bulk technology with ultra-low V_{th} devices to prevent operation in the subthreshold region at 4.2K, where threshold voltage shifts become significant.

In our case, similar to the approach in [Lin+22], we leverage FD-SOI technology to use the back-gate voltage as a mechanism to compensate for threshold voltage shifts at low temperatures. Having already demonstrated the performance of individual devices in the previous chapter, the aim here is to establish a link between those transistor-level characteristics and the overall behavior of the LNA.

The chapter is structured as follows: First, the design of the LNA is described, and its operating principles are explained. We then analyze the gain performance of the LNA from room temperature down to cryogenic temperatures, utilizing back-gate bias to enhance its gain. Following this, we present the noise figure of the LNA and investigate how the back-gate voltage influences it. Finally, we conclude by discussing how the overall performance of the LNA can be improved at cryogenic temperatures using back-gate biasing.

6.2 LNA circuit description

6.2.1 Schematic description

Measured Low Noise Amplifier (LNA) is composed of three different stages as presented in figure 6.1.

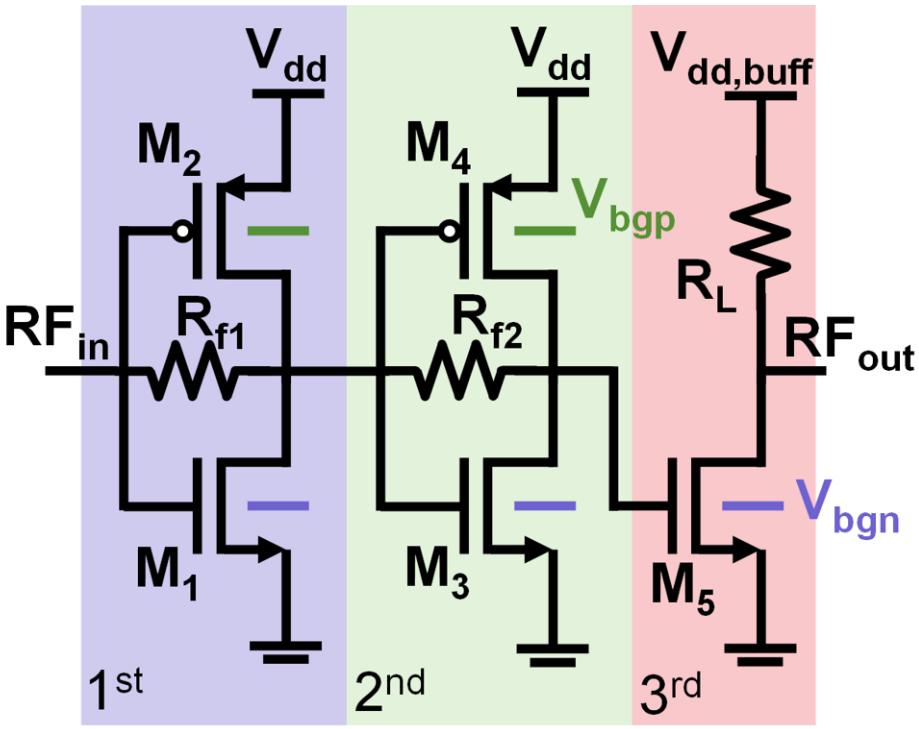

Figure 6.1: Schematic of the Low Noise Amplifier.

To simplify the optimization of cryogenic performance and to facilitate accurate measurements, the electrical design employs a dual-stage resistive-feedback inverter topology. This configuration offers the advantage of self-biasing across stages. The primary inverter stage is responsible for optimizing noise performance, while the secondary inverter stage serves to enhance the overall gain. The final stage, consisting of a Common Source (CS) amplifier, functions as an output buffer, effectively driving the 50-Ω load. The specificity of this LNA is to have access to the back-gate voltage of the NMOS and PMOS transistor which allows to control their threshold voltage.

The transistor dimensions and resistor values have been optimized to ensure that the Low-Noise Amplifier (LNA) operates effectively within a useful frequency band ranging from 2 to 8 GHz, corresponding to the signal frequencies emitted by the qubits [Le 23]. These dimensions are given in table 6.1:

Transistor	Type	L (nm)	W_{elem} (μm)	Finger nb.	W_{tot} (μm)
M_1	NMOS	28	1	80	80
M_2	PMOS	28	1	120	120
M_3	NMOS	28	1	40	40
M_4	PMOS	28	1	70	70
M_5	NMOS	28	1	40	40

Resistor	Value (Ω)
R_{f1}	450
R_{f2}	600
R_L	50

Table 6.1: (Left) Transistor dimension and (right) resistor value of the studied LNA

6.2.2 Working principle

The LNA design is based on inverter with feedback resistance. Figure 6.2 explains the principle of an inverter which correspond to the first stage of the studied LNA.

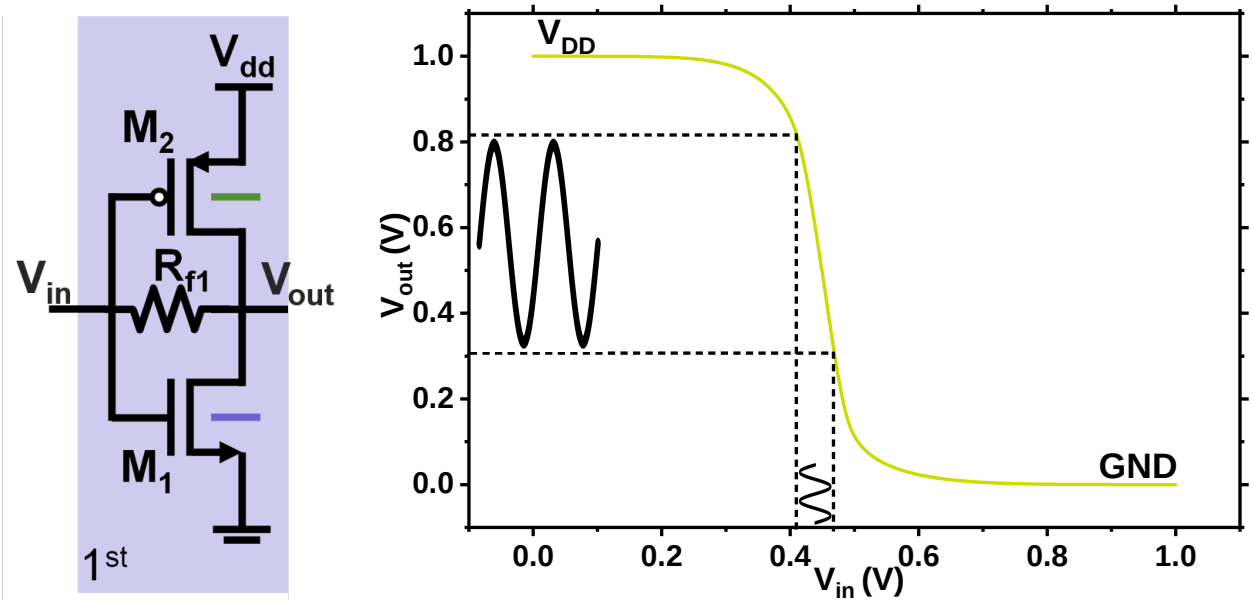

Figure 6.2: (Left) Inverter which represents the LNA first stage. (Right) Output voltage as a input voltage function of an inverter.

When the input voltage (V_{in}) is high, the PMOS transistor is OFF, and the NMOS transistor is ON, resulting in the output voltage (V_{out}) being 0V. Conversely, when V_{in} is low, the PMOS is ON, and the NMOS is OFF, so V_{out} is V_{dd}. Between these two conditions, the transistors exhibit conductance and act like a voltage divider bridge. The goal is to apply a small signal where the slope between V_{in} and V_{out} is steepest. This slope is controlled by the NMOS threshold voltage at the upper end and by V_{dd} minus the PMOS threshold voltage at the lower end. The impact of the back-gate voltage on these curves is presented in Figure 6.3.

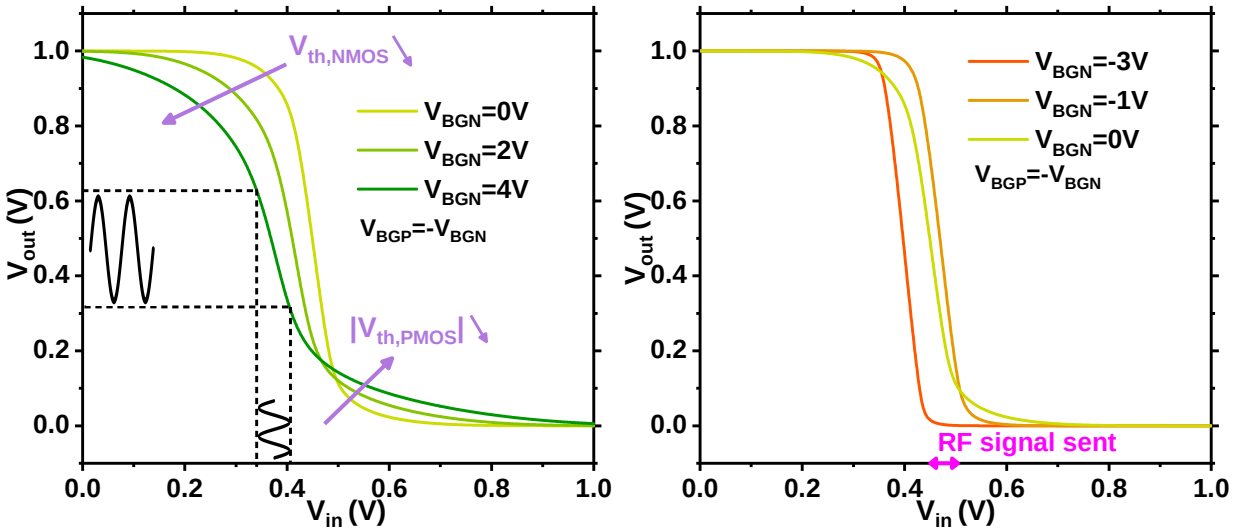

Figure 6.3: Output voltage as a input voltage function of an inverter with (left) a back bias increasing and (right) a back bias decreasing.

When the absolute value of back gate voltage decreases (figure 6.3 (Bottom right)) (i.e. the absolute value of threshold voltage increases which is the same variation when temperature drop), the slope will be steeper up to one point where the inverter becomes constrained and the slope begins to shift on Vin, the polarization is no more in the steepest part and the amplification is degraded.

6.3 LNA gain measurement

6.3.1 Temperature impact

Figure 6.4 present the LNA gain as a frequency function for 300k and 4.2K and a back-gate bias null:

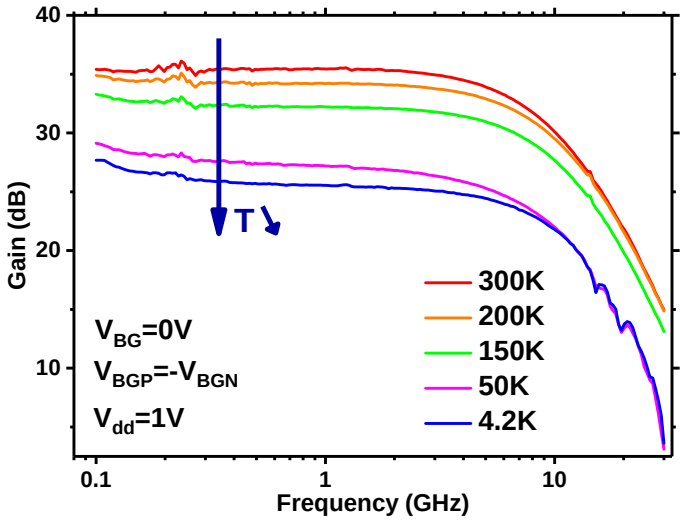

Figure 6.4: LNA gain as frequency function at room and cryogenic temperature and a back-gate voltage equal to 0.

On this graph, we see that when the temperature decreases, the LNA gain decreases. This is due to the fact that at cryogenic temperature the threshold voltage increases and the LNA becomes constraint. We are in the case of the figure 6.3 (right). Hopefully, we have a solution to compensate the threshold voltage shift, the back-gate bias.

6.3.2 Gain enhancement with back-gate bias

Figure 6.4 presents the LNA gain as a frequency function for 4.2K for different value of back-bias:

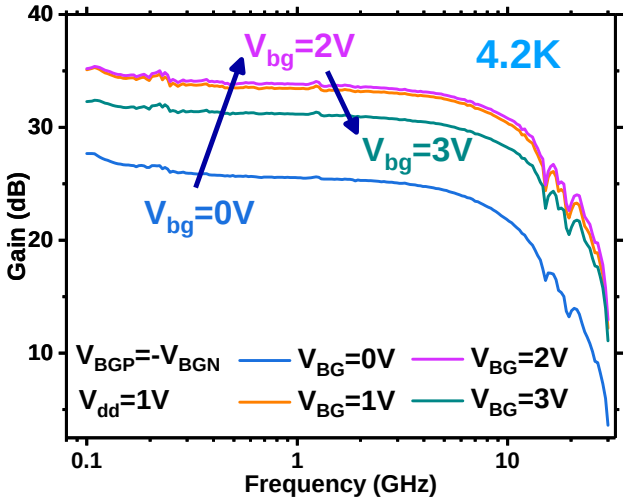

Figure 6.5: LNA gain as frequency function at cryogenic temperature and a back-gate voltage from 0 to 3V.

On this graph, we see that when the back-gate voltage increases, the gain increases and presents a maximum at a back bias of 2V. After this maximum the gain decreases when the back bias increases. Before the optimum, the LNA is constraint due to the threshold voltage shift at cryogenic temperature. When the back-gate voltage increases, the threshold voltage decreases and the inverter curves go from the red to the yellow one on the case of figure 6.3 (right). After the optimum, the slope of the inverter become lower, we go from the yellow curve to the blue curve in the case of figure 6.3 (left).

Figure 6.6 presents the gain as a function of the frequency. The cutoff frequency is not impacted by the temperature or the back-gate bias because it is mainly dependent on the transistor capacitances which present small variation with the temperature and the back-gate voltage.

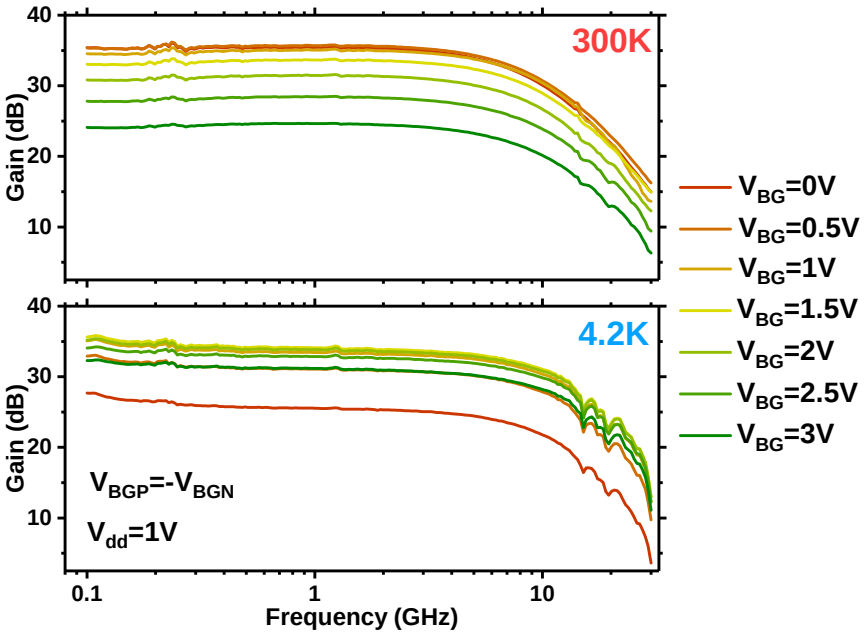

Figure 6.6: LNA gain as a function of the frequency for different V_{bg} at (top) room and (bottom) cryogenic temperatures.

On the figure, it is evident that both at 300K and 4.2K, the gain exhibits an optimum. At 300K, this optimum is reached when $V_{BG} = 0\,\mathrm{V}$, whereas at 4.2K, the optimum occurs at $V_{BG} = 1.5\,\mathrm{V}$. As the back-gate voltage approaches this optimal value, the gain increases significantly, highlighting the dependence of the gain on V_{BG} near its optimum.

Figure 6.7, presents the gain as a back bias function :

As shown in figure 6.7, the gain is modified by the temperature and by the back gate voltage. At $V_{bg} = 0V$, the gain drops of 10dB between 300K and 4.2K because the inverter are constrained. Using the 1.5V of back biasing on NMOS back bias and -1.5V on PMOS (to compensate V_{th} swing in accordance with figure 4.13 which represent the threshold voltage versus back-gate voltage), the gain can be increased of 8dB at 4.2K as shown in 6.7 (bottom). The 2 dB remaining between the maximum gain at 300K and at 4.2K is due to the increased of the drain to source conductance at 4.2K as presented in figure of drain to source conductance (see figure 5.5).

Figure 6.7 (Top) show that LNA performances can be enhance by using only NMOS (or PMOS) back bias but by using NMOS and PMOS back bias, back-gate voltage is approximately divided by two.

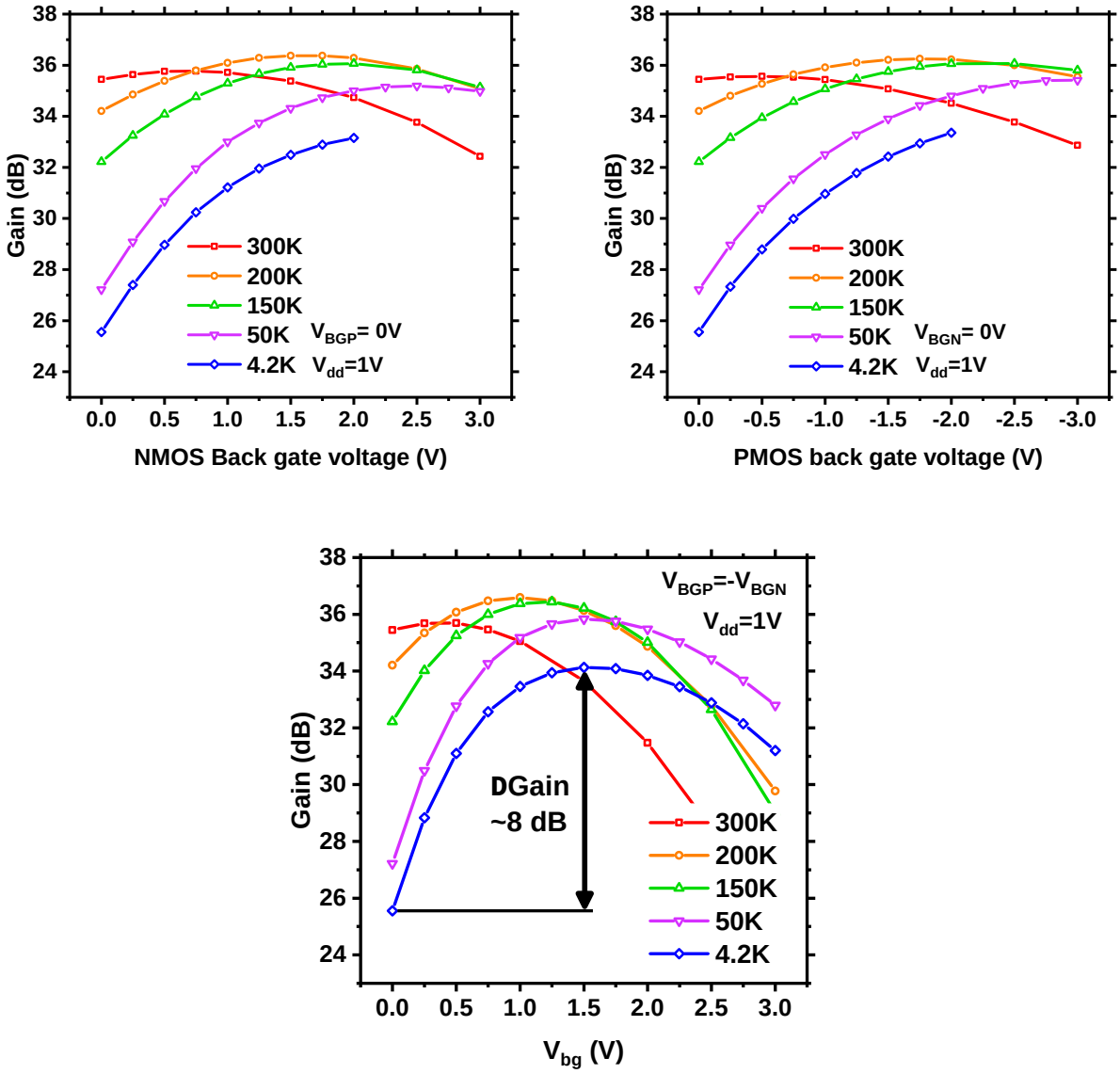

Figure 6.7: LNA gain as a function of the back-gate voltage. (Top left) Only the NMOS V_{bg} varies and $V_{bg,PMOS} = 0V$. (Top right) Only the PMOS V_{bg} varies and $V_{bg,NMOS} = 0V$. (Bottom) Both NMOS and PMOS V_{bg} vary.

Figure 6.8 present the maximum of gain as a temperature function and the back-gate voltage needed to reach this gain maximum. The gain maximum follows the same behavior as the voltage gain (see figure 5.6). The back-gate voltage needed to reach the maximum correspond to the one required to compensate for the threshold voltage shift due to temperature variation.

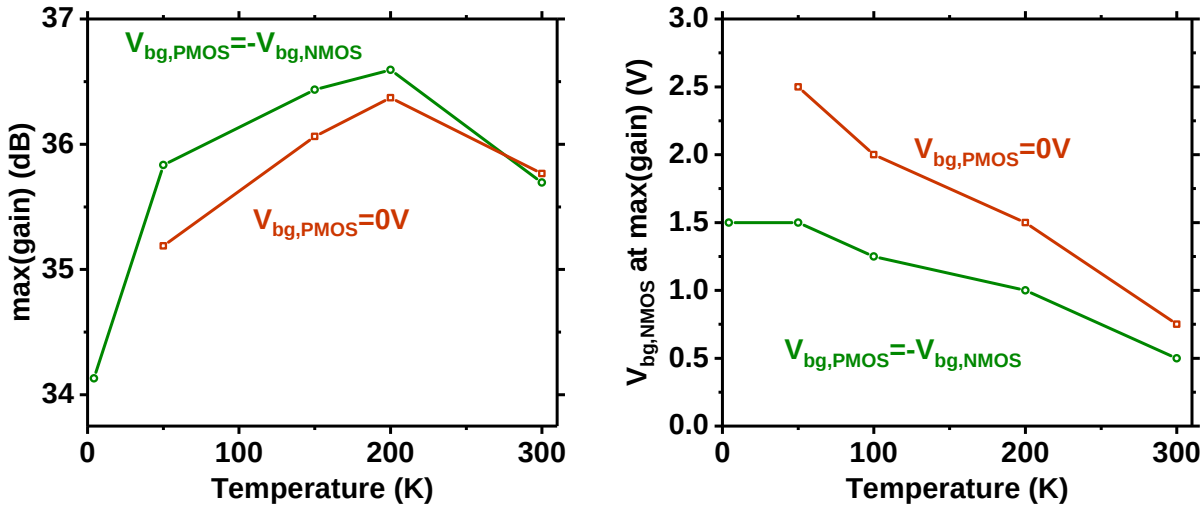

Figure 6.8: (Left) Max gain and (right) $V_{bg,NMOS}$ needed to reach this maximum as a temperature function

6.4 LNA noise measurement

While we have observed an enhancement in gain with the application of back-gate bias, another crucial figure of merit for the LNA is the Noise Figure (NF). In this section, we examine the impact of temperature on the NF and its behavior as a function of back-gate voltage.

6.4.1 Temperature impact

In this section NF is expressed in dB and is converted in equivalent noise temperature (T_{eq}) using the following formula [She+21]:

$$T_{eq} = T_0 \times (10^{\frac{NF(dB)}{10}} - 1) \tag{6.1}$$

where $T_0 = 290K$ is the standard reference temperature and $NF(dB)$ is the Noise Figure in dB. The NF of the LNA as a frequency function is plotted in figure 6.9.

From this graph, it is evident that the NF decreases as the temperature is reduced, primarily due to the reduction of thermal noise at lower temperatures, as outlined in [RE05]. As defined by [SK07], thermal noise arises in any conductor or semiconductor device and is caused by the random thermal motion of charge carriers. This type of noise is often referred to as white noise because it remains constant across all frequencies. The mean-square open-circuit voltage of thermal noise can be expressed as:

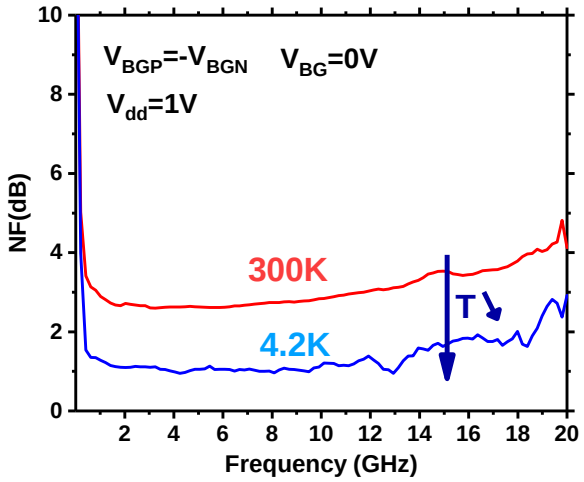

Figure 6.9: LNA noise as frequency function at room and cryogenic temperature and a back-gate voltage equal to 0.

$$\langle V_n^2 \rangle = 4 \cdot k_b \cdot T \cdot B \cdot R \tag{6.2}$$

where k_b is the Boltzmann constant, T is the temperature, B is the bandwidth in Hz, and R is the real part of the dynamic impedance $\frac{dV}{dI}$ across the terminals.

Within the useful frequency band, the NF reduces from 2.65 dB ($T_{eq} = 243.8K$) at room temperature to 1.04 dB ($T_{eq} = 78.5K$) at 4.2 K. The NF exhibits similar frequency dependence at both room and cryogenic temperature, which confirm that the noise reduction is mainly due to the reduction of the thermal noise.

6.4.2 Noise enhancement with back-gate bias

Figure 6.10 shows the NF of the LNA at cryogenic temperature as a function of frequency for different back-gate voltages.

As seen in the figure, the NF decreases as the back-gate voltage increases, reaching an optimum at $V_{bg} = 2V$. Beyond this point, the NF begins to increase. With the application of back-gate bias, the NF in the useful frequency band improves from 1.04 dB ($T_{eq} = 78.5K$) at $V_{bg} = 0V$ to 0.34 dB ($T_{eq} = 23.6K$) at $V_{bg} = 2V$. We hypothesize that the back-gate voltage enhances noise matching at both the input and output [CL20]. Figure 6.11 further illustrates the NF as a function of back-gate voltage, as well as the minimum NF across different temperatures.

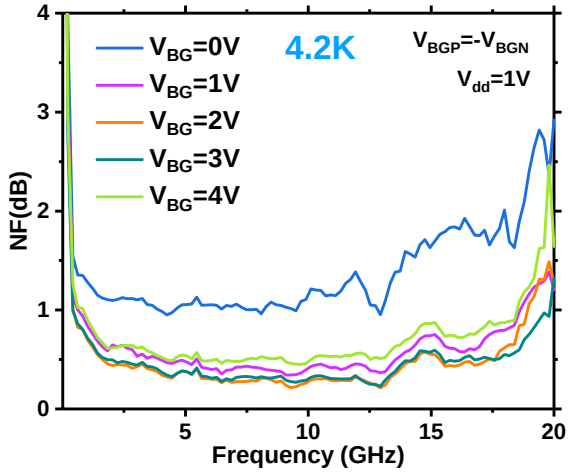

Figure 6.10: Noise figure of the LNA as a function of frequency at cryogenic temperature, with back-gate voltages ranging from 0V to 4V.

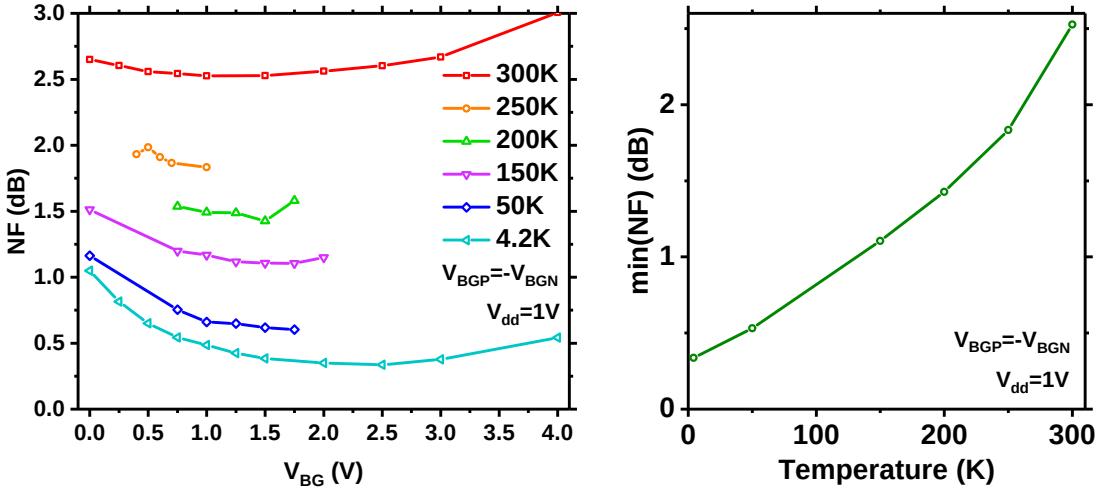

Figure 6.11: LNA noise figure as a function of (left) back-gate voltage and (right) temperature, for both NMOS and PMOS transistors. Due to measurement constraints, some temperatures present only limited back-gate bias data.

At each measured temperature, the NF exhibits a minimum value, demonstrating that the back-gate bias improves the noise performance of the LNA consistently across the temperature range. Comparing the performance with and without back-gate bias, the NF is improved by 5% at room temperature and by 0.71 dB at 4.2K.

However, the minimum noise figure of the LNA is not reached for the same back-gate as the max-

imum LNA gain. This mean that a compromise should be done between the gain and the noise figure desired.

6.5 Simultaneous gain and noise figure enhancement

To illustrate the compromise, the figure 6.12 presents the noise figure as a back-gate voltage function for 300K, 150K and 4.2K. The back ground color correspond to the gain value at the different back-gate bias.

In these graphs, it is evident that for both gain and noise figure optimization at cryogenic temperature, the back-gate voltage (V_{BG}) should be increased. Notably, a higher V_{BG} is required to optimize the noise figure compared to optimizing the gain. However, as illustrated in Figure 6.11, the noise figure varies by less than 1 dB with changes in back-gate voltage at cryogenic temperatures.

Specifically, in Figure 6.12 at 4.2K, with $V_{BG} = 2V$, the LNA reach a 0.35dB noise figure ($T_{eq} = 24.3K$) and a gain higher than 34dB. This values of noise figure is only 4% higher than the minimum noise figure at 4.2K.

In conclusion, we have proposed an LNA structure based on an inverter and analyzed its gain and noise performance. The LNA gain and noise figure are enhanced with back-gate voltage, but at different applied V_{BG}. A compromise must be made depending on whether noise or gain performance is prioritized.

While the gain and noise figure value can be expected to vary quantitatively with LNA design, the underlying physics of back bias and temperature dependence can be generalized to all design.

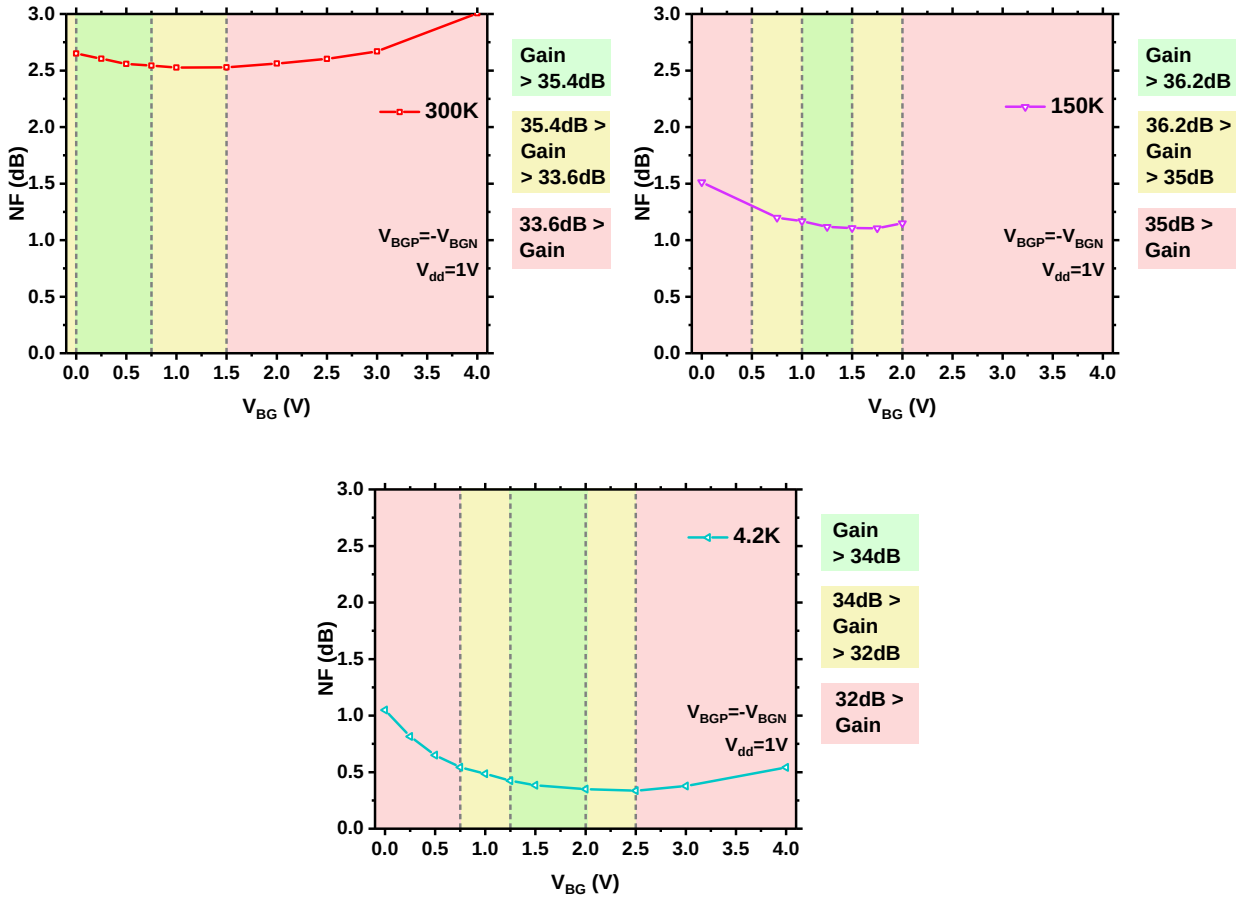

Figure 6.12: LNA noise figure as a back-gate voltage function for 300K, 150K and 4.2K. The color correspond to the different value of gain at the corresponding back-gate voltage

6.6 Conclusion

Finally, table 6.2 summarizes the effect of the temperature and of the back bias on the stand alone transistor and their impact on the LNA performances.

<table>
<tr><th></th><th colspan="2">Transistor</th><th>LNA</th></tr>
<tr><td rowspan="5">Temperature drop</td><td rowspan="2">Well freeze</td><td>g_{ds} ↗</td><td>Max gain ↘</td></tr>
<tr><td>Capa depend on frequency</td><td>No impact on cutoff frequency</td></tr>
<tr><td colspan="2">V_{th} ↗</td><td>Loss of functionality, gain ↘</td></tr>
<tr><td colspan="2">Max g_m ↗</td><td>Max gain ↗</td></tr>
<tr><td colspan="2">Thermal noise ↘</td><td>Noise figure ↘</td></tr>
<tr><td rowspan="3">V_{bg} increase</td><td colspan="2">V_{th} ↘</td><td>Recover room temperature gain</td></tr>
<tr><td colspan="2">f_t and f_{max} ↘</td><td rowspan="2"></td></tr>
<tr><td colspan="2">V_{ZTC} ↘, same as V_{th}</td></tr>
</table>

Table 6.2: Summary table of the back bias and temperature impact on the transistor characteristics and on LNA. Its enhancement depend on its design

In this table, we see that the threshold voltage shift at cryogenic temperature induce a loss of functionality and a important gain loss for the LNA. However the back-gate bias allows to reduce V_{th} and to recover room temperature gain.

In addition to show competitive performance [Puy+24], the main goal of this study is to demonstrate the advantage of using the back-gate feature of FD-SOI for designing low temperature circuit such as LNA. The other advantage of FD-SOI technology is that it is fully compatible with the silicon spin qubits technology.

This chapter has demonstrate that FD-SOI technology is promising and in the following a more exhaustive study will be performed about the noise figure characterization. These first measurement also give a feed back to the first design of LNA to improve these performance. Moreover the interest of the back-gate has been demonstrate on LNA characterization but other circuit (such as ring oscillator) can benefit of this threshold voltage reduction.

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Conclusion

General conclusion

This thesis aimed to provide a comprehensive and exhaustive RF characterization of passive and active devices, completing the studies performed in DC and offering new insights into the analysis of circuit performance at cryogenic temperatures. The work presented contributes to a deeper understanding of device behavior in such environments and some RF cryogenic measurements on both active and passive, which is essential for the optimization of cryogenic circuits.

The first step involved developing a reliable and repeatable measurement methodology from room temperature down to cryogenic conditions. This is a key phase in the RF field. Various measurement setups were compared to establish the most optimized system for the necessary RF characterizations. This groundwork ensured the precision and reproducibility required for the subsequent experiments.

In Chapter 3, passive components like inductors were studied since they play a significant role in circuit performance. They were characterized, and their temperature behavior depending on the substrate was investigated. It was found that at cryogenic temperatures, carrier freeze-out leads to a substantial increase in substrate resistivity, thereby reducing losses and enhancing inductor performance. At sufficiently low temperatures, the substrate's impact on inductor performance becomes negligible, eliminating a major source of degradation seen at higher temperatures. This could lead to new designs of passive devices oriented specifically for cryogenic temperatures.

The characterization of FDSOI transistors was then explored in detail. Through electrostatic analysis, the threshold voltage was extracted via capacitance measurements. It was observed that as temperature decreases, the threshold voltage shifts, but this shift can be compensated thanks to the back-gate bias. Additionally, this electrostatic study revealed that dopants in the back-gate well freeze below a certain temperature, significantly increasing the back-gate resistance. This parameter should be included in the transistor model for better RF capacitance extraction. This analysis also provided insights into improving mobility extraction using the classical split-CV method.

The RF performance of transistors from room temperature to cryogenic temperatures was also examined. It was observed that RF figures of merit (f_t and f_{max}) improve as the temperature decreases. The transistor voltage gain increased down to 77K. However, below 77K the freeze-out of dopants in the back-gate increase the back-gate well resistance. This increase alters the coupling between the drain-source access and the back-gate, which increases the drain-source conductance and reduces the voltage gain. In fact, this effect appears around 1 GHz, a frequency range where DC measurements fail to capture such phenomena, underscoring the importance of RF characterization for a complete understanding of transistor behavior. Additionally, the RF measurements allowed the investigation of dynamic and static self-heating effects, enabling the extraction of both the thermal resistance and the thermal time constant.

Finally, these characterizations were applied to optimize a low-noise amplifier (LNA) operating at cryogenic temperatures. As predicted by the elementary device measurements, when the temperature decreases, the transistor gain degrades, due to the shift in the threshold voltage and also below 77K due to the dopant freeze out in the back-gate. However, the noise figure improves due to the reduced thermal noise. Both the gain and noise figure can be optimized using the back-gate bias to compensate the threshold voltage shift across the temperature.

In conclusion, this work has provided reliable data and analysis in RF of devices and circuits from room temperature down to 4K. It demonstrates the importance of RF characterization to complement DC studies towards a better understanding of device physics under extreme conditions. These insights are crucial for the design and optimization of cryogenic circuits, particularly in applications requiring high performance at very low temperatures.

Future perspective

Building upon the findings of this thesis, several promising avenues for future research on RF characterization at cryogenic temperatures are suggested. These perspectives aim to extend the applicability of the methodologies developed, enhance measurement accuracy, and deepen the understanding of device and circuit performance under cryogenic conditions.

One immediate extension of this work would be to adapt the RF characterization techniques developed here to other semiconductor technologies. While this thesis has focused on a specific technology, applying these methodologies to alternative technologies, such as different types of transistors or materials like wide-band gap semiconductors, could provide valuable insights into their behavior at cryogenic temperatures.

A significant next step would involve the integration of the RF measurements into the development of a compact RF model that remains accurate down to cryogenic temperatures. Such model would

enable reliable RF simulations at these extreme temperatures, facilitating the design and optimization of circuits intended for cryogenic applications. This modeling would be crucial for the development of cryo-electronics, particularly in fields such as quantum computing and space exploration.

For passive components, further research could focus on studying their linearity at cryogenic temperatures. While this thesis explored inductors, investigating how cryogenic conditions affect the linearity of these components could help improve their performance in RF circuits, ensuring more predictable and stable operation in low-temperature environments.

Improving noise measurement techniques is another important direction. In this work, noise characterization played a role in understanding circuit behavior, but developing more reliable methods for noise measurements at cryogenic temperatures would lead to better insights into thermal and other noise sources. These improvements could yield more accurate predictions of circuit performance, particularly in sensitive cryogenic applications such as low-noise amplifiers.

Additionally, noise measurements on transistors themselves could be expanded to facilitate the incorporation of noise behavior into compact models. This would allow for the simulation of both RF performance and noise characteristics under cryogenic conditions, which is essential for designing low-noise circuits.

Another promising area is the characterization of different circuits to explore how cryogenic temperatures, particularly the effects of threshold voltage shifts and back-gate freeze-out, impact their performance. Circuits such as ring oscillators, circulators, or other complex RF components could be tested to determine how these phenomena influence their behavior, providing new insights for circuit design at cryogenic temperatures.

Finally, an ambitious future direction would be the complete RF characterization of a quantum bit (qubit) readout chain. As quantum computing progresses, understanding how the entire readout chain performs under cryogenic conditions, from the RF front-end to the digital readout, is crucial. Such work would contribute significantly to the development of efficient, scalable quantum computing systems, where low-temperature performance is critical.

In summary, these perspectives represent exciting opportunities to broaden the scope of RF characterization at cryogenic temperatures. By pursuing these research directions, the insights gained from this thesis could be extended to new technologies, models, and applications, paving the way for further advancements in cryo-electronics.

Appendix A

Complementary Inductors Measurements

This appendix complements the inductor measurements presented in Chapter 3. The characterization results for different inductors are shown.

As described in Chapter 3, different shielded inductors have been characterized. Figure A.1 shows a picture of all the measured inductors with the de-embedding Open and Short structures:

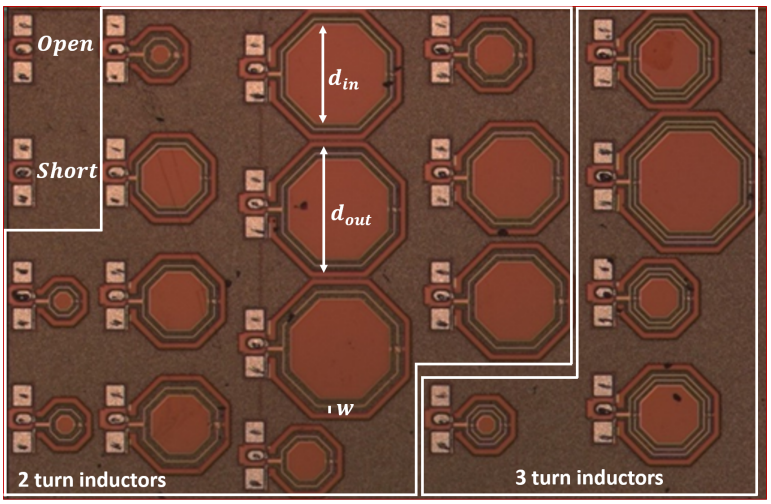

Figure A.1: Octagonal FDSOI inductors measured with two or three turns and on-wafer Open and Short structures.

We have measured 18 octagonal spiral inductors with different numbers of turns n, metal track widths w, and inner diameters d_{in}. The dimensions of the different inductors are given in Table A.1:

The measured values of the inductance at low frequency, $f = 500$ MHz, for all our two-turn inductors are presented in Figure A.2 for temperatures from 300 K down to 4.2 K. We observed that the low-frequency inductance varies linearly with d_{in} and does not depend on temperature in this range.

Number of turns n	2	3
Inner diameter d_{in}	From 79.2 μm to 396 μm	From 158 μm to 396 μm
Metal track width w	From 13.95 μm to 23 μm	13.95 μm

Table A.1: Parameters of the measured inductors. Each inductor has different dimensions within the indicated range.

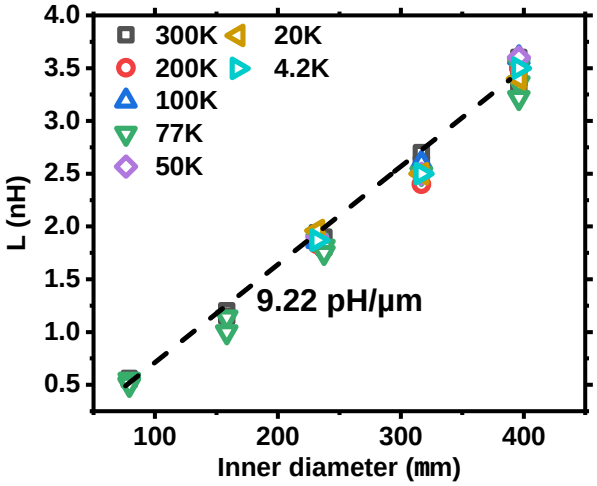

Figure A.2: Inductance L_{LF} measured for 14 two-turn inductors at low frequency (500 MHz) as a function of the inner diameter d_{in}, and for different temperatures. The low-frequency inductance varies linearly with d_{in} and is temperature-independent.

The inductance value at low frequency is expressed theoretically by the modified Wheeler formula [Moh+99; Whe28]:

$$L_{DC,theo} = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + K_2 \delta} \tag{A.1}$$

where $d_{avg} = 0.5(d_{out} + d_{in})$ is the average diameter, d_{in} and d_{out} are respectively the inner and outer diameters of the inductor (see Figure A.1), $\delta = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}$ is the fill ratio, $\mu_0 = 4\pi \times 10^{-7}$ H.m^{-1} is the magnetic permeability of free space, n is the number of turns, and K_1 and K_2 are layout-dependent coefficients, arbitrarily set to fit the curve. For the characterized octagonal inductors, $K_1 = 2.1$ and $K_2 = 3.55$ are used.

The inductance values as a function of the inner diameter are presented in Figure A.3. The error bars represent temperature variation.

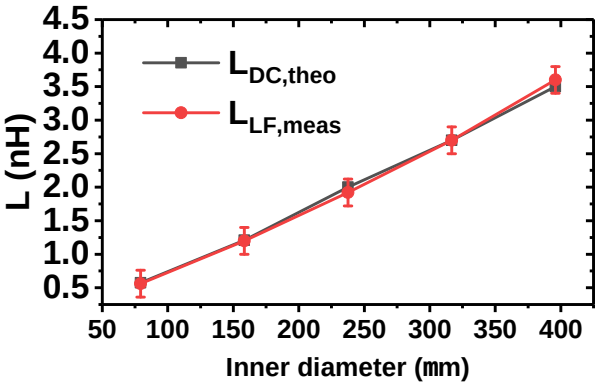

Figure A.3: Comparison between the measured inductance extracted at 500 MHz and the theoretical inductance using the modified Wheeler formula for two-turn inductors. The error bars represent temperature variation.

In this graph, we see that the modified Wheeler formula can be applied for all measurement temperatures and all inductor dimensions we have characterized.

The frequency dependence of inductance values for 3 other inductors (different from those presented in Chapter 3) is presented in Figure A.4.

The temperature behavior of the inductors is the same as the one presented in Chapter 3. The response is inductive at low frequency and then becomes capacitive at high frequency after the Self-Resonant Frequency (SRF) [BKL04]. The extrema values of the inductance L at low and high frequencies remain the same regardless of the temperature, within our measurement accuracy. The main difference appears around the self-resonant frequency. Resonance occurs at the same frequency regardless of temperature, but the inductance value increases by a factor of 3 around this frequency between 300 K and 4.2 K. This increase at low temperatures is due to the reduction of metal track resistivity at low temperatures [Pat+20].

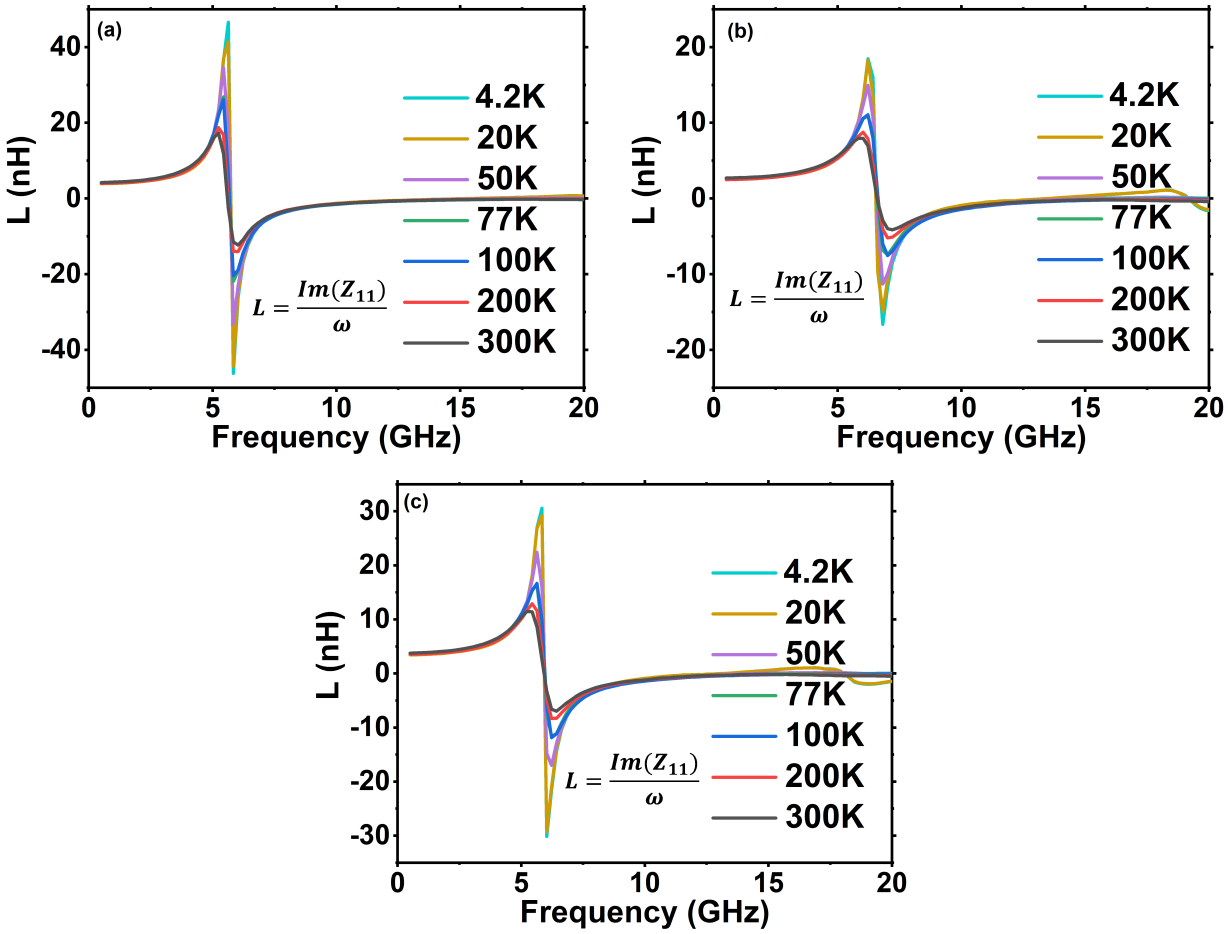

Figure A.4: Inductance L measured vs frequency for different temperatures from 300 K down to 4.2 K for three different inductors. (a) $d_{in} = 237.6$ μm, $w = 13.95$ μm, $n = 3$. (b) $d_{in} = 316.8$ μm, $w = 20$ μm, $n = 2$. (c) $d_{in} = 396$ μm, $w = 13.95$ μm, $n = 2$.

Appendix B

4 RF Pads Cryogenic Measurement

This appendix details the 4 RF ports measurement performed on the FD-SOI transistor and how it was adapted and validated on the RF cryogenic prober with only two RF probes.

B.1 Principle of Operation

In RF, to perform 4 RF pad measurements, GSGSG (Ground-Signal-Ground-Signal-Ground) probes are used. Each probe refers to 2 RF ports connected to the VNA. The principle of measuring an FD-SOI NMOS transistor is presented in Figure B.1.

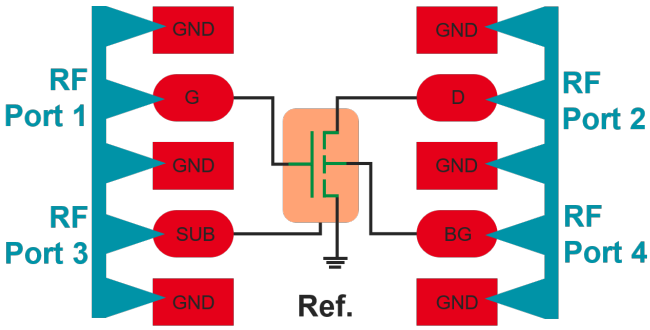

Figure B.1: Schematic of the 4 RF pads NMOS transistors. Ports 1, 2, 3, and 4 are for the gate, the drain, the substrate, and the back-gate. In the case of a 4 RF probe measurement, each pad is connected to an RF probe.

However, this configuration was not possible in the RF cryogenic prober due to the fact that the cryogenic prober is equipped with only two RF accesses facing each other. To simulate 4 RF pad measurements at cryogenic temperatures, we use 2 RF probes and 2 DC probes, performing two measurements in different configurations. The probe placement differs between configurations, as shown

in Figure B.2.

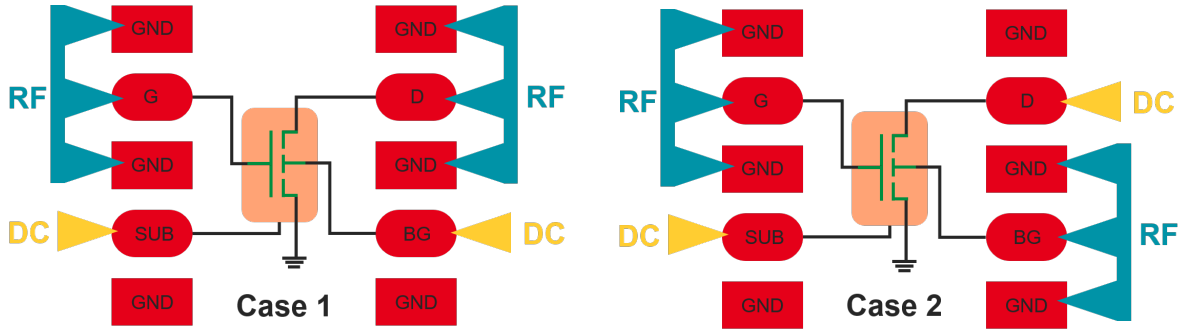

Figure B.2: Schematic of the 4 RF pads NMOS transistors. Ports 1, 2, 3, and 4 are for the gate, the drain, the substrate, and the back-gate. In the first case (left), the measurement is performed between the gate and the drain. The substrate and the back-gate are connected to a DC probe. In the second case (right), the measurement is performed between the gate and the back-gate. The substrate and the drain are connected to a DC probe.

In the first case (Figure B.2 (left)), the RF measurement is performed between the front-gate and the drain, as in a classical 2 RF port transistor measurement. This measurement was mainly used to compare with real 4 RF pad measurements and validate the measurement methodology. In the second case (Figure B.2 (right)), the RF measurement is performed between the front-gate and the back-gate. This allows the extraction of the gate-to-back-gate capacitance (C_{gb}) and the total back-gate capacitance (C_{bb}), which is not possible with a classical 2 RF port transistor measurement.

B.2 Comparison and Validation at Room Temperature

To validate this methodology, capacitances are extracted and compared between real 4 RF probe measurements and the proposed 2 RF probes and 2 DC probes configuration at room temperature. Comparisons of the total gate capacitance, gate-to-drain capacitance, and gate-to-back-gate capacitance are presented in Figure B.3.

All capacitances measured are extracted between 1 and 3 GHz and present similar variations. These three curves confirm that the measurements performed on the cryogenic prober with only 2 RF probes are accurate and provide results consistent with those from the 4 RF probe measurements.

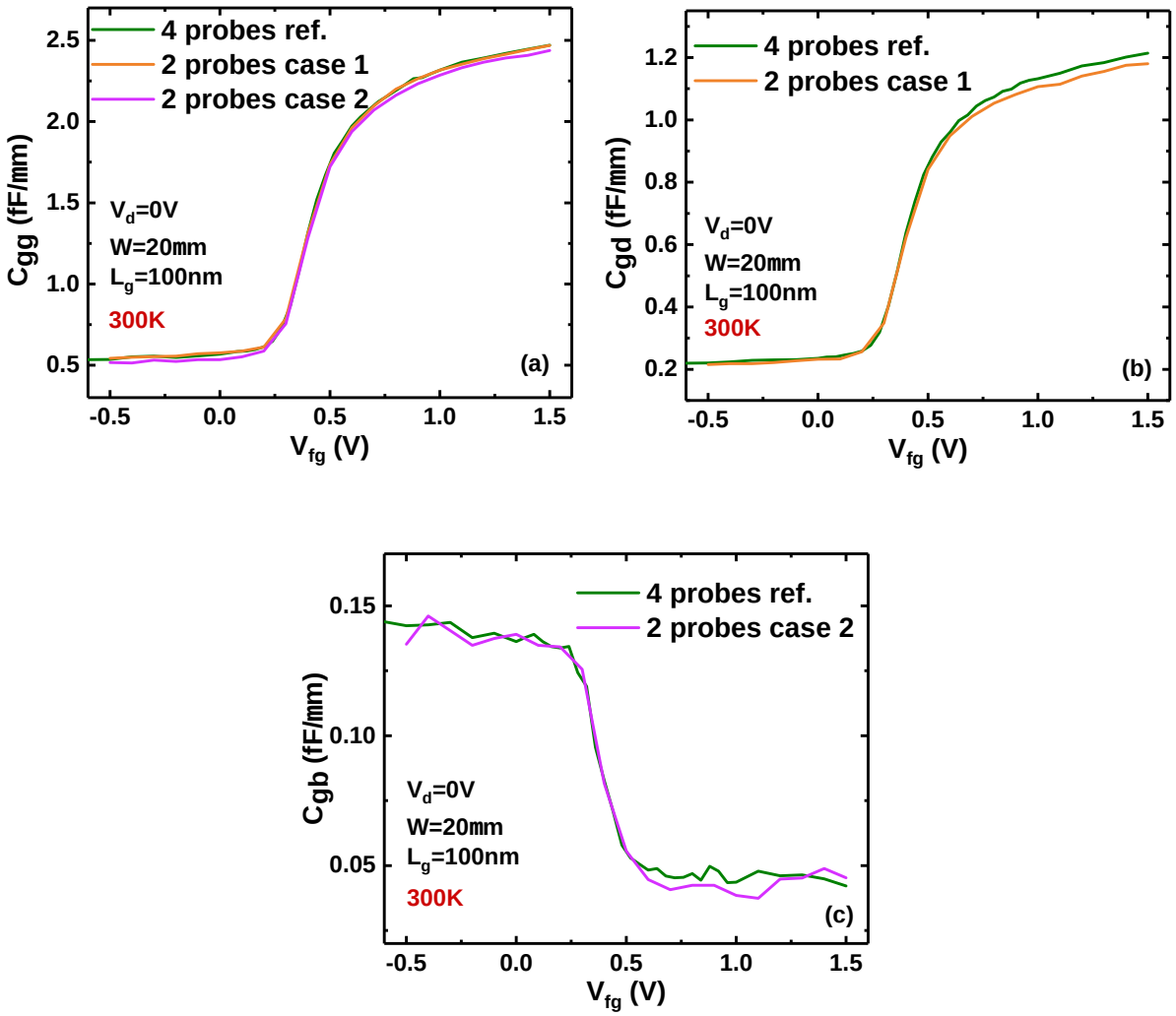

Figure B.3: (a) Total gate capacitance, (b) gate-to-drain capacitance, and (c) gate-to-back-gate capacitance as a function of gate voltage. The three curves represent the three measurements performed: first, a measurement with 4 probes on a Cascade prober; second, a measurement with 2 RF probes on the gate and drain on the Lakeshore prober; third, a measurement with 2 RF probes on the gate and back-gate on the Lakeshore prober.

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