Analysis of robustness of 650 V GaN HEMT under repetitive short-circuits

Adrien Lambert

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Analysis of the Robustness of 650 V GaN HEMTs under Repetitive Short-Circuits

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Bonne lecture

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Abstract

Since the 50's power electronics has been developed through silicon which became the largely dominant material for power semiconductors. Silicon has indeed proven a good reliability, is easy to purify and after decades of cost reduction, is very affordable. Nevertheless, after fifty years of improvement, physical limits of silicon are reached and don't match anymore with the new applications needs, like a higher operating frequency and a higher power. Wide-band gap (WBG) materials, such as diamond, gallium nitride (GaN), and silicon carbide (SiC), have emerged to address these challenges. GaN, especially in HEMT power devices, is particularly promising due to its high switching speed, excellent thermal conductivity, and potential for high-frequency operation. Despite their advantages, GaN components must demonstrate robustness and reliability, particularly against short-circuits, to be widely adopted in industries like automotive and avionic.

The study of short-circuits began a few years ago, with initial work observed in 2013. However, it remains limited in several respects. The normally-off technology of p-GaN and cascode components has been studied almost exclusively. Current studies of enhanced mode (e-mode) components based on p-GaN components have revealed that the highest voltages could only be achieved at the cost of concessions (overheated environment, increased gate resistance). To the best of our knowledge, very few, if any, papers focus on normally-on technology depletion mode (d-mode). What is more, current studies are mainly concerned with the robustness of components to a single short-circuit and the time to failure.

Rather than carrying out destructive short-circuits, which would make it much more difficult to analyse the component once it has been destroyed, it was decided to carry out repetitive, non-destructive short-circuits. Several series of successive short circuits are performed.
These short-circuits are interspersed with electrical characterizations to identify parametric variations and gain a better understanding of degradation and failure mechanisms. The study of induced damage is therefore a key point and it will contribute to the design of more short-circuits robust chips. Two suppliers of 650 V GaN components have been selected, with normally-on and normally-off components. A short-circuit test bench specifically for GaN HEMT 650 V components has therefore been developed. It consists of three parts: a power/mother board, a device/daughter board and a driver board. A sarcophagus was developed using 3D printing. It holds the component by pressure on the device board and eliminates the need to solder the components, thereby reducing the thermal stress on the device board in successive soldering/desoldering of components.

However, the task proved more arduous than expected. Despite the particular care taken with the routing and the compactness of the electronic boards, with the aim of reducing the loop inductance, the initial tests were not at all conclusive and the experimental bench needed to be greatly optimised. A SPICE simulation has been developed to help understand the parasitic phenomena. Reducing common-mode currents was of prime importance, through the use of appropriate probes or ferrite cores. Several versions of the test bench have been developed, to achieve relevant results in terms of stability and in line with what should be required by future JEDEC standards for short-circuit testing.

Different parametric and dynamic variations have been observed. In addition, components with the same structure but from different suppliers gave different results in terms of stability and robustness against short circuits. Explanatory hypotheses were formulated at the end of the thesis.

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Résumé

Depuis les années 1950, l'électronique de puissance s'est développée grâce au silicium, qui est devenu le matériau dominant pour les semi-conducteurs de puissance. Le silicium a en effet prouvé sa fiabilité, est facile à purifier et, après des décennies de réduction des coûts, est devenu très abordable. Cependant, après cinquante ans d'améliorations, les limites physiques du silicium ont été atteintes et ne répondent plus aux besoins des nouvelles applications, comme des fréquences de fonctionnement plus élevées et une puissance accrue. Les matériaux à large bande interdite (WBG), tels que le diamant, le nitrure de gallium (GaN) et le carbure de silicium (SiC), ont émergé pour relever ces défis. En dépit d'une grande vitesse de commutation et d'une conductivité thermique accrue, les composants GaN doivent démontrer leur robustesse et leur fiabilité, notamment face aux courts-circuits, pour être largement adoptés dans des secteurs tels que l'automobile et l'aéronautique.

L'étude des courts-circuits a commencé il y a quelques années avec les premiers travaux observés en 2013. Cependant, les études restent limitées à plusieurs égards. La technologie normalement bloquée des composants p-GaN et cascode a été étudiée presque exclusivement et les tensions les plus élevées n'ont pu être atteintes qu'au prix de concessions (environnement surchauffé, augmentation de la résistance de grille). La littérature est inexistante pour la technologie normalement passante. De plus, les études actuelles se concentrent principalement sur la robustesse des composants face à un unique court-circuit destructif et sur le temps avant défaillance.

Plutôt que de réaliser des courts-circuits destructifs, avec une analyse du composant d'autant plus difficile une fois celui-ci détruit, il a été décidé de réaliser des courts-circuits répétitifs et non destructifs. Ces courts-circuits sont entrecoupés de caractérisations électriques afin d'identifier les variations paramétriques et de mieux comprendre les mécanismes de dégradation et de défaillance. L'étude des dommages induits constitue donc un point clé et contribuera à la conception de puces plus robustes face aux courts-circuits. Deux fournisseurs de composants GaN de 650 V ont été sélectionnés, incluant des composants normalement passants et normalement bloqués. Un banc d'essai de courts-circuits spécifiquement conçu pour les composants GaN HEMT de 650 V a ainsi été développé. Il se compose de trois parties : une carte mère d'alimentation, une carte fille pour le composant, et une carte de commande. Un sarcophage a été conçu par impression 3D. Il maintient le composant par pression sur la carte fille et élimine la nécessité de souder les composants, réduisant ainsi les contraintes thermiques sur la carte lors des soudures et dessoudures successives.

Cependant, la tâche s'est avérée plus ardue que prévu. Malgré les soins particuliers apportés au routage et à la compacité des cartes électroniques, dans le but de réduire l'inductance de boucle, les premiers tests n'étaient pas du tout concluants. Le banc expérimental a par conséquent dû être considérablement revu et optimisé. Une simulation SPICE a été développée pour aider à mieux comprendre les phénomènes parasites. La réduction des courants de mode commun a été d'une importance primordiale, grâce à l'utilisation de sondes appropriées ou de tores de ferrites. Plusieurs versions du banc d'essai ont été conçues afin obtenir des résultats pertinents en termes de stabilité et conformité en vue des futures normes JEDEC pour les tests de courts-circuits.

Différentes variations paramétriques et dynamiques ont été observées. En outre, des composants de même structure et aux caractéristiques similaires, mais provenant de différents fournisseurs, ont donné des résultats sensiblement différents en termes de stabilité et de robustesse face aux courts-circuits. Des hypothèses explicatives ont été formulées à la fin de la thèse.

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Table of Symbols

χ: Electron affinity (eV)
Φ_m: Metal Work Function (eV)
Φ_s: Semiconductor Work Function (eV)
$\Phi_{AlGaN:}$ AlGaN Work Function (eV)
Φ_{GaN}: GaN Work Function (eV)

2DEG: two-dimensional electron gas at the AlGaN/ GaN heterojunction
C_b: polymer capacitor
C_{iss}: gate input capacitance
C_{oss}: gate output capacitance
C_{rss}: reverse transfer capacitance
C_S: Ceramic capacitor
DUT: Device Under Test
C1 : SPICE Polypropylene capacitor of 133 µF (Figure 34)
C2 : SPICE ceramic capacitor of 2 µF (Figure 34)
D-HEMT: Depletion-mode High Electron Mobility Transistor
E-HEMT: Enhancement-mode High Electron Mobility Transistor
$\vec{E}$: Electric field (V/m)
E_F: Fermi's Energy
$E_{g\ material}$: bandwidth gap of a specific material (eV)
E_{vacuum}: Vacuum Energy
ESL: Equivalent Series Inductances
ESR: Equivalent Series Resistance
ΔI: difference in short-circuit current values between off and on states
Δt: commutation time, during which the current goes from its reduced value in off-state, to its highest value in on-state
L12: SPICE parasitic Inductance of the wires connecting the HV supply and the power board (Figure 123)
$R_{GOFF:}$ Driver-controlled gate off-state resistor
$R_{GON:}$ Driver-controlled gate on-state resistor
TLF: Time Leading to Failure

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Tables of Test-Boards and Devices

The study of short-circuits on GaN HEMT is based on the use of several types of test-board. One strategy was to use a daughter board, related to the device under test and a mother board, related to power supply. Another strategy was to use one single test-board, abandoning the daughter / mother board logic. Improvements have been made on it, like reducing the parasitic inductance of the shunt connection, and therefore the power loop inductance or choosing adapted probes. Reducing common mode current has also been a key element.

However, during the 2024 study, different improvements in test-boards have been directly made. It concerns power board but also driver boards. The different version are sum up hereunder.

Name of the board in the thesis	**Year / Version**
Test-Board 202**3**	First Test-board. It is made up with: - Power Board 2023 - Daughter Board 2023
Driver Board 202**3**	First driver board, developed in 202**3**
Driver Supply Board 202**3**	First driver supply board, developed in 202**3**
Test-Board 202**4**	202**4**, single test-board (power and device in the same board), abandon of the logic mother / daughter board to minimize the size and the parasitic effect of the test-board
Driver Board 202**4**	Second driver board developed in 202**4**, with former driver from Texas Instrument replaced by a new one from Microchip
Driver Supply Board 202**4**	Second driver supply board developed 202**4**, with former DC / DC converters replaced by ones with reduced insulation capacity

Table 1: Summary of the different version of power or driver boards

The different versions of these boards do not give only two configurations. As it has been described in the Chapter 2, the Test-Board 202**3** has also been tested with Driver Board 202**4** and Driver Supply Board 202**4**.

These various combinations allow to more easily visualize the benefits of these newly designed boards. Combined with these 2024 Driver boards, the test-board 2024 gives the best results in terms of stability for short-circuit testing.

The several types of tested components and their supplier are summarized below with the Table 2.

Component	**Supplier**	**V_{th}**	**V_{GS} OFF / V_{GS} ON**	**Id**	**R_{DS_ON}**
D-mode	Supplier 1	-12.5 V	- 24 V / 0 V	10 A	250 mΩ
Batch A	*Region A of the wafer*				
Batch B	*Region B of the wafer*				
Batch C	*Region C of the wafer*				
Cascode	Supplier 1	1.8 V	- 3 V / +6 V	10 A	190 mΩ
p-GaN	Supplier 1	1.8 V	- 3 V / +6 V	15 A	120 mΩ
p-GaN Prototype	Supplier 1	1.7 V	- 3 V / +6 V	12 A	190 mΩ
p-GaN	Supplier 2	1.7 V	- 3 V / +6 V	11 A	150 mΩ

Table 2 : Different types of studied components and their main parameters

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General Introduction

In 1890, the “War of Currents” between Georges Westinghouse and Thomas Edison finally favoured alternating current (AC) over direct current (DC). The electricity network was then built accordingly, with alternating current being used to transmit electricity and the networks being organised into a hierarchy.

In this hierarchy electricity is produced from power plant with nuclear, coal, oil, or hydraulic energy. This electricity produced by turbines of these power plants is then spread over the whole territory and consumption regions through an alternative network.

To reduce power losses due to Joule effect, electricity is transported at high voltage and then lowered, thanks to successive voltage transformers as it gets closer to consumption places.

This leads to several types of network. Interconnection or main transmission networks, called energy highways between countries or for long distances, transport energy from production sites. Their voltage is 400 kV or 225 kV with reduced losses. At regional level and for voltages of 225 kV, 90 kV and 63 kV, the subtransmission network has been designed. It also supplies energy to large industrial sites. Finally, for voltages ranging from 20 kV (medium and small businesses) to 400 V (domestic applications), there is the distribution network [1] .

However, many applications require direct current or alternating current at other voltage or other frequency (50 Hz in EU, 60Hz in US as shown in Figure 1)

This is where power electronic comes in, with the use of converters which can be divided into four types:

Input & output power	Device
AC to DC	Rectifier
DC to AC	Inverter
DC to DC	DC-to-DC converters
AC to AC	AC-to-AC converters

Table 3: summary of the different converters type

Rectifiers are used for electronic devices like computers, televisions which require direct current. Inverters can be found in UPS (uninterruptible power source), traction or renewable energy systems such as photovoltaics. This converter allows to transform the stored continuous energy to an alternative signal before injecting it in the network. DC-to-DC are used to sustain a level of voltage, electronic isolation, and power factor correction [2]. AC-to-AC converters are used to change the voltage or the frequency.

To understand to what extent is power electronics present, Baliga states in [3] that at least 50% of the electricity used in the world is controlled by power devices.

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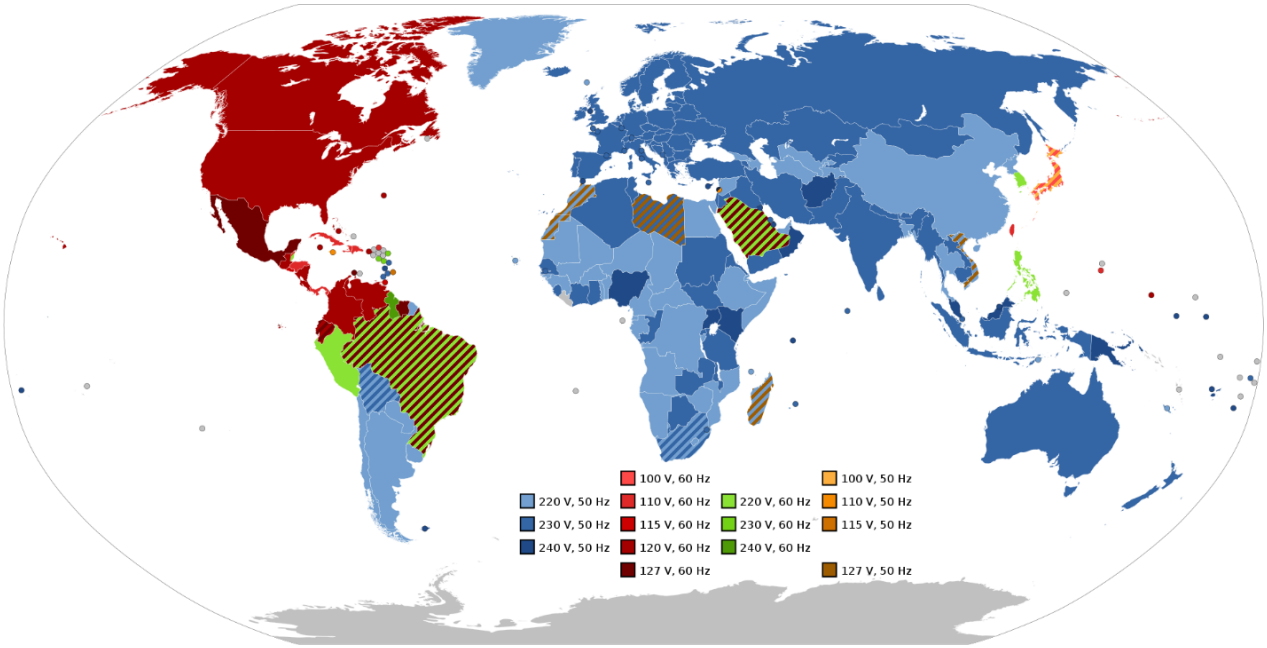

Figure 1: Nominal frequency and voltage by country (from [4])

Power electronics started at the beginning of the 20th century with the first mercury vapor rectifier. It was used to convert alternating single-phase current to direct current for DC network of subway or powering DC train engines in France or radio emitters up to the 50s [5,6].

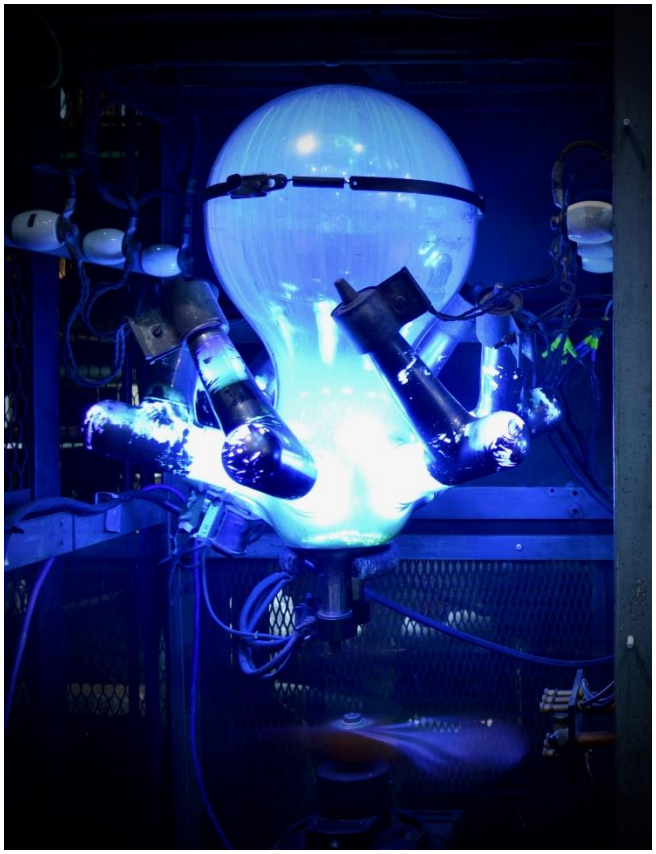

Figure 2: Illustration about a mercury vapor rectifier [7]

The advent of semiconductors materials, especially silicon, during the 60s-70s made these types of converters outdated.

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Since the 50s power electronics has been developed through germanium-based rectifiers (1952), rapidly replaced by silicon in 1955 whose band gap is wider (1.12 eV for silicon versus only 0.66 eV for Germanium [8]), to finally become the largely dominant material. Silicon has indeed proven a good reliability, is easy to purify and after decades of cost reduction, is very affordable[9].

New needs

Electric consumption is increasing and will not slow down within the next decades. The graph below indeed shows a growth of 150 % from 1990 to 2023, related in majority to Asia development. Taking into consideration that resources are limited, energy savings by reducing the losses and weight reduction need to be done.

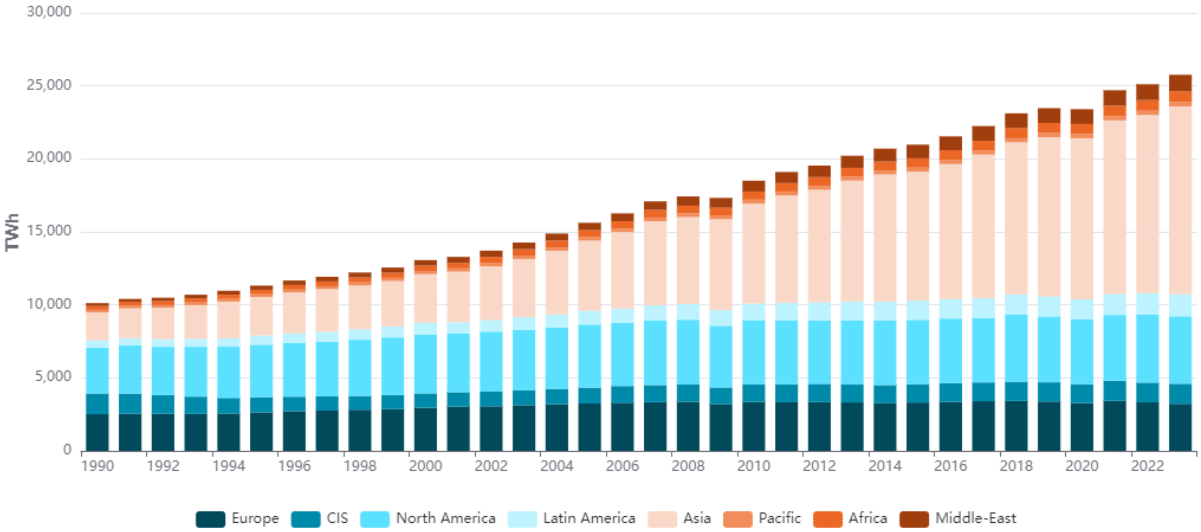

Figure 3: Graphic showing the world electric consumption [10]

This rise can also be linked to the present growing-up electrification. Numerous applications have been or are currently developed, such as smartphones or computer but also more recently like e-automotive with electric cars and ultra-fast DC chargers or all-electric aircraft.
Considering electric vehicles, for a long time it has been tried to increase the capacity of batteries. However, the solution may lie more in chargers, with increased power levels and the search for a replacement for silicon
These new modes of consumption and production are redefining current patterns and making the use of DC networks particularly relevant and the use of power electronics, in particular power converters, essential. Large band-gap materials with a gap of around 3 eV (compared with 1.12 eV for Si) could offer an alternative.

Figure 4: Illustration of new electrical applications (Photovoltaic panels, EV, Boeing 787 Dreamliner

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Besides that the emergence of decentralised renewable energy production methods such as on-shore and off-shore wind power and photovoltaic panels counteracts the previous pattern of production, transmission and consumption of electricity.

Renewable energies indeed involve decentralised production facilities, far from the original production sites. This requires the use of very high voltage converters to reduce losses due to the Joule effect. Multi-stage converters are therefore used, with stages of the order of 10 kV. However, if the Si manages to accept this voltage rating, it becomes highly resistive and therefore heats up a lot, needs to be cooled and therefore consumes energy. Hence, Si is not very well suited to this application and a new material is required.

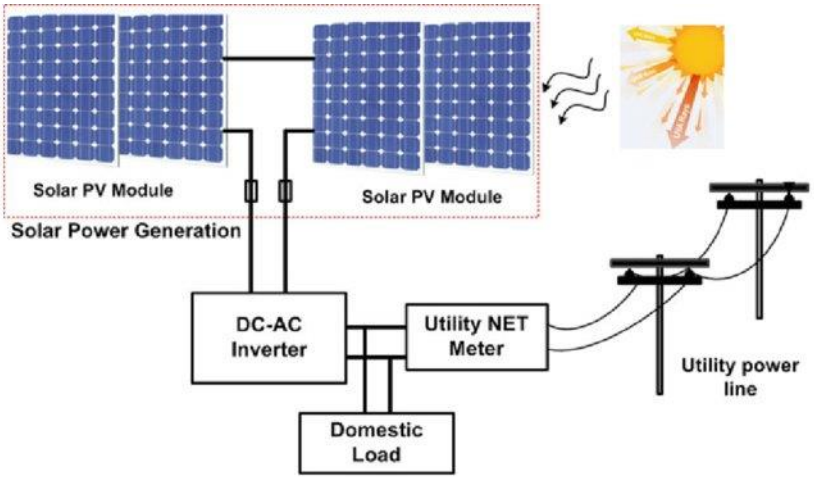

Figure 5: Illustration of the connection between PV panels and network from [11]

To address this need of improvement, two main materials have been studied. With reduced losses, higher current and voltage range and increased switching frequency, the wide band-gap materials such as gallium nitride (GaN) and Silicon Carbide (SiC) represent the solution to reach these new requirements. Particularly appreciated in RF domain with an increased frequency up to tens of Megahertz [12–14], GaN transistors are currently studied as power devices for voltage range up to 650 V, while SiC devices are rather reserved for higher voltage such as 1200 V. As reminder, Silicon MOSFET cannot excess switching frequency above several hundred of kHz [15].

With specific voltage, frequency, direct or alternating current, low voltage (<900 V) power conversion devices hence appear as a significant market and will not reduce with the years.

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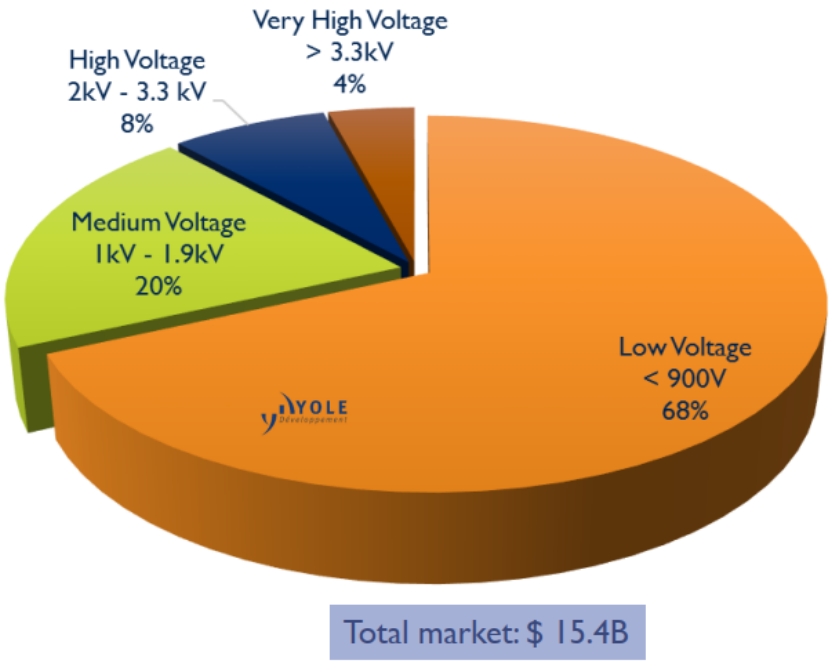

Figure 6: 2017 market for power devices in power electronics, split by voltage range [16]

Diamond, as an ultra-wide-band-gap technology, is also the subject of many research [17–19] (including the Ampère laboratory), GaN, which is faster in switching allows the device to operate at high frequencies, while SiC, whose better thermal conductivity allows greater heat dissipation and is therefore particularly suitable for high-power applications. The both following figures present characteristics of these materials. For a greater clarity, Figure 8 does not consider the exceptional performances of diamond, to focus on other materials which seem eclipsed in comparison.

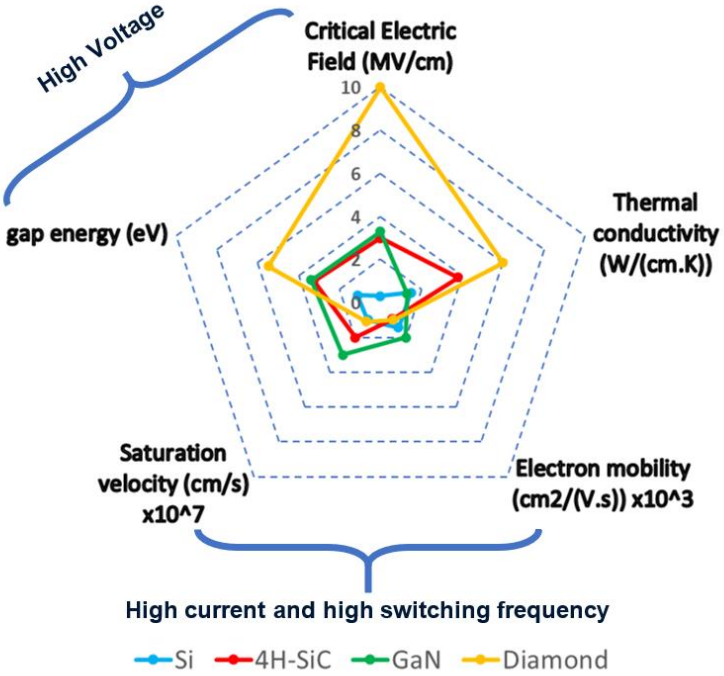

Figure 7: Star Diagram comparing Diamond, GaN, SiC et Si from [20]

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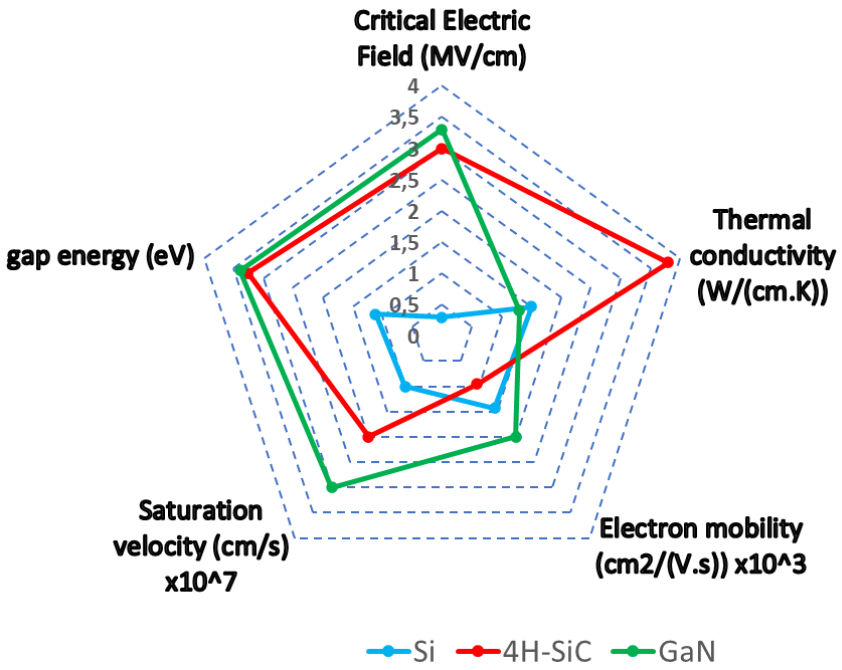

Figure 8: Star Diagram comparing GaN, SiC et Si from [20]

However, GaN-based power devices need to be improved, particularly in the domain of the robustness where several degradation and failure mechanisms are not well understood. Their commercialization at large scale necessarily goes through an improvement of these reliability aspects, highly requested by the automotive or aeronautic field.

With simultaneous high-voltage and high-current, short-circuits represent one of the most undesirable events due to the significant amount of energy to be dissipated [21,22]. This thesis will focus on the impact of short-circuit on 650 V GaN HEMT.

Chapter 1 provide basic knowledge of semiconductor to afterwards better understand the specific properties of the GaN transistor. Particular attention has been paid to understanding the physical mechanisms inherent in the operation of GaN transistors, which are often shortly described in theses. Thereafter, Chapter 1 will focus on the state-of-the-art of short-circuit on GaN power transistors. The literature is indeed very incomplete. The mechanisms of short-circuit operation and breakage are generally poorly understood, and the authors of scientific papers contradict each other. Three types of failure mechanism have been identified. Their strengths and weaknesses have been discussed in this chapter to better prepare the study of the degradation of GaN transistors under short-circuit conditions.

An innovative approach was decided upon and described in Chapter 2. The literature currently relies on destructive testing, with the major drawback that chips are difficult to analyse once they are destroyed and even more considering the colossal power to be dissipated during short-circuiting. To counter this, it was decided to work on repetitive, non-destructive tests. The literature is inexistant about the analysis of normally-on components. They are studied in this thesis in addition to normally-off p-GaN components from two separate suppliers. Between each series of short circuits, the component is characterised using a B1505A characteristic tracer and the evolution of the transistor static parameters such as the threshold voltage V_{th} or the on-state resistance R_{DS_ON} are analysed.

The impressive switching speed of GaN components means that the slightest parasitic effect is exacerbated. Several phases of optimisation of the experimental short-circuit bench were therefore carried out, and are described in Chapter 2. In parallel with this, a SPICE simulation was developed in order to gain a better understanding of the operation of the experimental bench. These analyses led to various improvements and versions of the short-circuit test bench, summarised briefly in Table 1 and detailed in Chapter 2.

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After a complex optimization of the test bench, Chapter 3 gives the final results of normally-on and normally-off components in terms of behaviour, dynamic observations and degradation following the application of repetitive short circuits. The normally-off components deliver very different behaviour and robustness under short-circuit conditions. Different variations and types of failure are observed. At the end of the chapter, some answers are given about to the increased robustness of components from the first supplier.

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1

GaN Transistors and State-of-the-Art about Short-Circuit

Chapter 1 provides basic knowledge of semiconductor to afterwards better understand the specific properties of the GaN transistor. Particular attention has been paid to understanding the physical mechanisms inherent in the operation of GaN transistors, which are often shortly described in theses. Thereafter, Chapter 1 will deal about a state-of-the-art of short-circuit on GaN power transistors. The literature is indeed very incomplete. The mechanisms of short-circuit operation and breakage are generally poorly understood, and the authors of scientific papers contradict each other. Three types of failure mechanism have been identified. Their strengths and weaknesses have been discussed in this chapter in order to better prepare the study of the degradation of GaN transistors under short-circuit conditions.

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1.1 Transistor Technology and GaN Material

1.1.1 Definition of a Semiconductor

An atom is surrounded by electrons in its various outer layers. the electrons located on the last outer layer, which have the lowest ionization energy are called the valence electrons and are eventually able to move from the valence band to the conduction band.

Figure 9 shows three types of materials. In a conductor, the conduction band and valence band overlap, so valence electrons can easily become free electrons and be in the conduction band.

In an insulator or semiconductor, on the other hand, the bands are separated. Energy must be supplied to the valence electrons to move them into the conduction band. The minimum energy required is the band gap. For a semiconductor, the gap will be small (a few eV), whereas it will be much larger for an insulator and will confer the insulator behaviour [23].

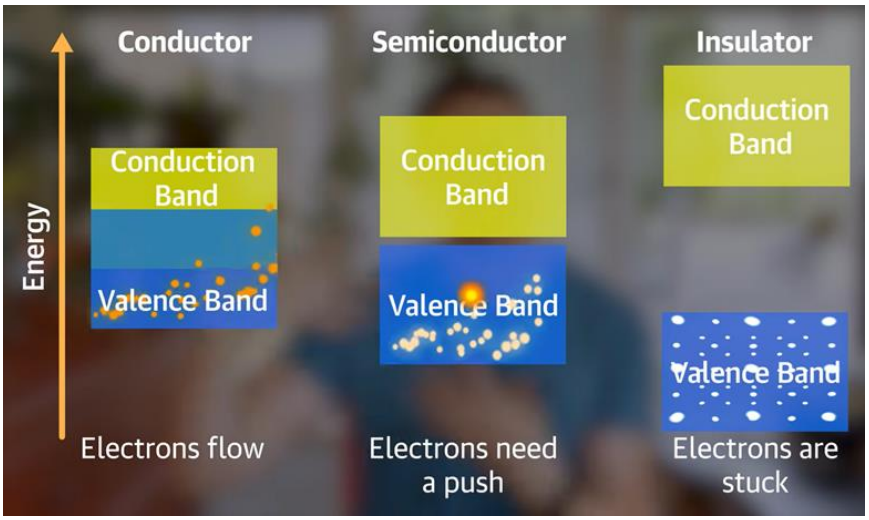

Figure 9: Energy band diagram for conductor, semiconductor and insulator according to [2]

As it is shown in figure below, a semiconductor device, depending on the control state, will be able to pass current (Figure 10-b) or not (Figure 10-a) and will therefore be either conductive or insulating.

An analogy can be made with an electrical switch, except that here, instead of human mechanical control, it will be an electrical (current or voltage) or optical control.

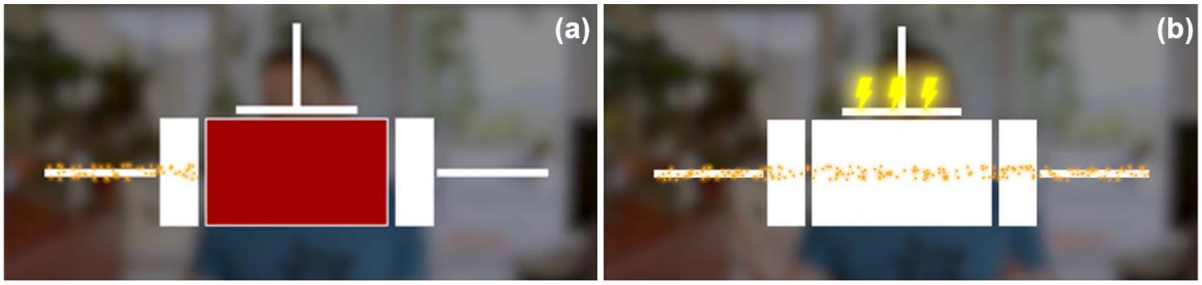

Figure 10: diagram showing the off-state (a) and on-state of a semiconductor from [2]

Semiconductor devices can be divided into two groups. Devices adapted to signal electronics, which will be used in smartphones or computers whose main function is to pass or not a logic signal (0 or 1 for the closed or open state), power semiconductors which will be found as converters for motors, solar panels, etc… It is the latter field that interests this thesis.

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Although the above-mentioned applications require electrical energy, they differ in terms of power, frequency and form (DC or AC). A conversion step is therefore required. For example, a computer operating on direct current with a voltage of the order of tens of volt will need a converter, more commonly known as a "rectifier", so that it can be connected to the 230 V alternating current domestic network. Depending on the application - low or high power, low or high frequency, different types of power semiconductors are needed, as represented in Figure 11.

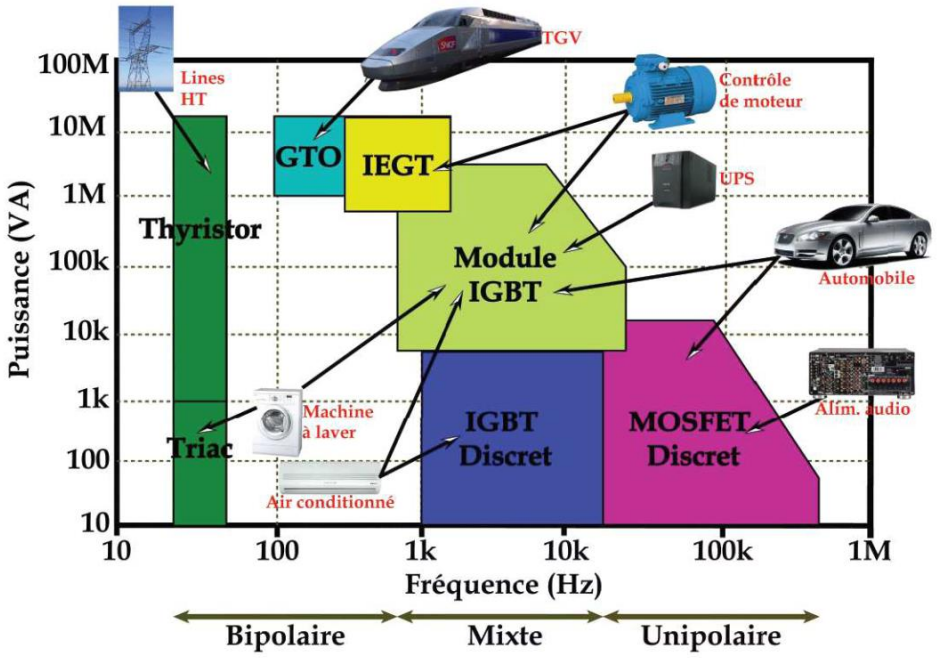

Figure 11: Illustration of the fields of application for semiconductor power components in 2005 from [2]

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1.1.2 GaN Material

GaN is one of the more promising wide band gap semiconductors for power device applications. It is made up of elements from column III of the periodic table of elements (Gallium Ga, Aluminium Al, Indium In) associated with the element nitrogen (N) in column V. These materials, GaN, AlN, InN and their alloys are commonly known as “III-N materials”.

They crystallize in two types of structure: the cubic zinc blende (ZnS) structure and the hexagonal wurtzite structure. Thanks to ionicity of the III-N bonds, the wurtzite phase is the most thermodynamically stable [24,25].

This structure is made up of two hexagonal sublattices: one with gallium atoms (Ga) and the other with nitrogen atoms (N) along the c axis as shown in Figure 12.

The structure is ideal when it is composed of regular tetrahedrons. Wurtzite crystals are stable when the criteria c / a ≤1,633 is verified [25].

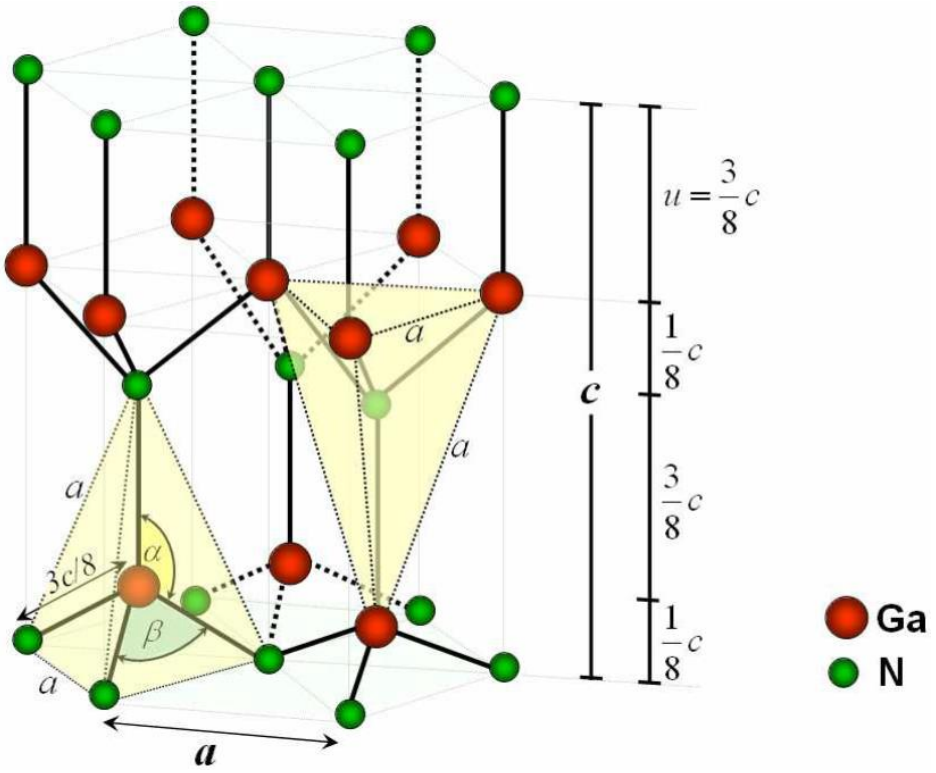

Figure 12: Ideal Gallium nitride wurtzite hexagonal structure from [25]

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1.1.3 The HEMT, a Specific transistor

1.1.3.1 Overview

The HEMT (High Electron Mobility Transistor) is a lateral field effect transistor. What sets it apart from other transistors, such as JFETs (Field Effect Transistor), MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) and others, is the presence of a two-dimensional electron gas, the 2DEG, formed at the interface of the heterojunction between two semiconductors with different band gaps. This 2DEG is characterized by a high electron mobility and the possibility to stop the conduction by cutting it enables the transistor to operate at higher frequencies than other structures. This 2DEG also has a high electron density what is suitable for power applications [20,21,24,26,27].

The heterojunction of HEMT is made up of two semiconductors with different band gaps, mainly AlGaAs/GaAs and more recently AlGaN/GaN. It is this latter pair of semiconductors that present interest for power applications.

The growth of gallium nitride can be carried out on massive GaN which nevertheless has the major disadvantage of being extremely expensive to produce without defects [20,21,28]. Other possible substrates are sapphire (Al_2O_3), silicon and silicon carbide (6H-SiC).

Regarding sapphire, if it is commonly used in the field of electroluminescent diodes because of its transparency, its low thermal conductivity makes it difficult to use as a substrate in power devices. The significant lattice mismatch with GaN as well as different thermal expansion coefficients, operating a significant curvature of the substrate, make its utilization limited with GaN HEMTS [25,27,29].

Silicon carbide, by its lattice parameter close to that of GaN, as well as its very good thermal and electrical conductivity constitutes a substrate of choice but its high cost as well as the potential appearance of cracks in the material during cooling complicate its use or reduce it to components which require a significantly high power density [25,27,29] or specific use like radar [30] .

The low cost of production of silicon wafers with the maturity of the die and its good thermal conductivity make a substrate of choice. Nevertheless the significant lattice mismatch between GaN and Si and a significant thermal expansion coefficient difference with GaN makes the presence of a buffer layer essential to reduce the possible dislocations in GaN [25,27–29].

An AlN layer is introduced between substrate and GaN layer to reduce constraints and defect. It is called the nucleation layer. Another layer, called transition layer, made up of different concentration of AlGaN with different proportion of alumina. This process allows a better growth quality [20,24].

Another layer of AlN can be found at the interface of the heterostructure AlGaN / GaN and is called spacer. This layer is made up of material with the highest gap (6.2eV). By its wide band gap, increase the discontinuity between GaN and AlGaN which improves electrons containment in the 2DEG [24].

Material	*Lattice parameter (Å)*	*Coefficient of thermal expansion (10^{-6} K^{-1})*	*Thermal conductivity (W.K-1.cm-1)*
Al_2O_3	a = 4,758 c = 12,99	Δa/a = 7,5 Δc/c = 8,5	0,5
4H-SiC	a = 3,07 c = 10,05	Δa/a = 4,2 Δc/c = 4,68	3.7
Si	a = 5,4301	3,59	1,5
GaN	a = 3,189 c = 5,18	Δa/a = 5, 59 Δc/c = 3,17	1,3

Table 4: Characteristics of the most commonly used substrates for growing GaN from [3,31–33]

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A schematic diagram of a HEMT structure is presented below, highlighting the AlGaN / GaN heterojunction. This simple schematic will be corrected and completed as the paragraph progresses.

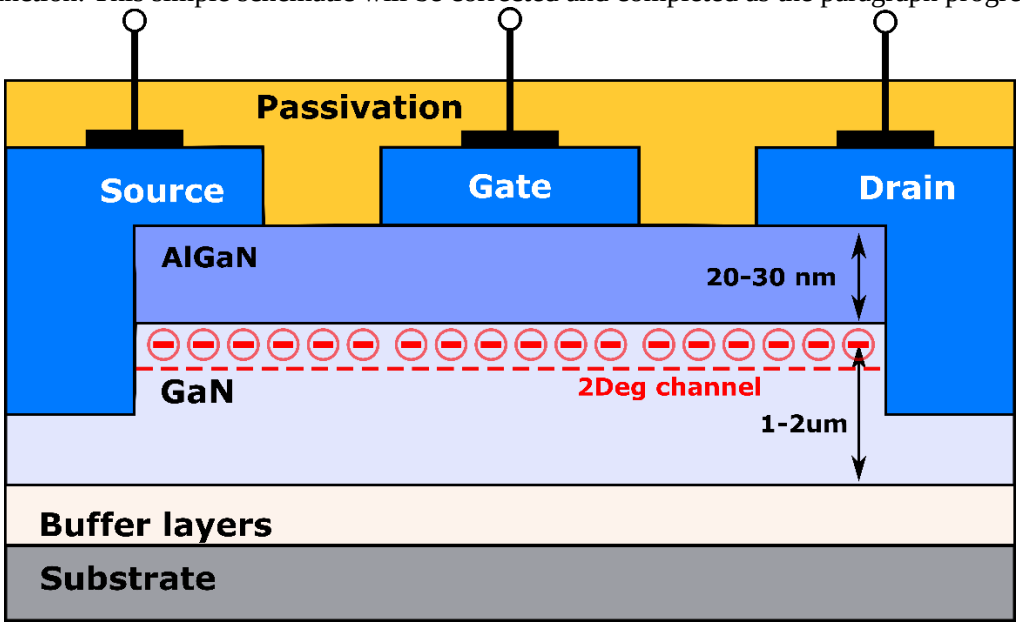

Figure 13: Diagram of a HEMT component with its 3 electrodes (Gate, Drain and Source) from [7], [18], [19]

The thickness of the AlGaN layer is of the order of tens of nanometers, from 20 nm to 30 nm, the thickness of GaN being far much larger, of the order of 1-5 µm [21,24,28].

1.1.3.2 Detailed Operation

The operation of the HEMT is based on several physical phenomena detailed below:

Polarization Displaces Electrons Within the AlGaN/ GaN Heterojunction

GaN is, in its most stable thermodynamic form, in the so-called Wurtzite or hexagonal configuration [36] , compared to the so-called cubic or zinc blende (ZnS) structure.

Nitrogen being more electronegative than gallium (3.04 for Nitrogen vs 1.81 for Gallium [24]), a dipole moment exists between these two elements, oriented from the nitrogen atom towards the gallium atom [24,36]. Therefore there is a polarization field between gallium and nitrogen, called spontaneous polarization P_{SP}. This polarization appears naturally, without constraint or stress [36]. The vector sum of all these dipole moments gives a total spontaneous polarisation [24].

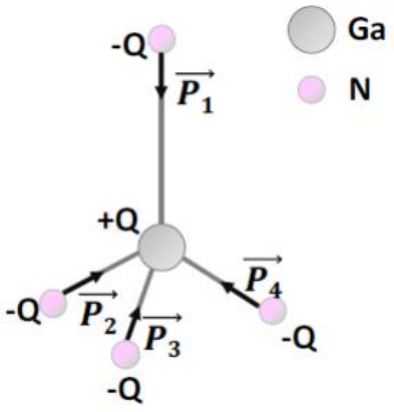

Figure 14: different dipole moments contributing to a global spontaneous polarisation in GaN [24]

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AlGaN is an alloy made up with alumina and gallium nitride. Within the hexagonal crystal, gallium atoms will be replaced by alumina atoms, which gives the following formula:

$$Al_xGa_{1-x}N$$

With x representing the percentage of aluminium.

Therefore, the lattice parameter as well as the band gap can be controlled according to parameter x. As previously mentioned with GaN, AlGaN also exhibits spontaneous polarization. In the table below are listed various parameters with in particular spontaneous polarization, for x percentage of alumina:

	GaN	**$Al_xGa_{1-x}N$**	**AlN**
a (Å)	3,189	$-0,077x + 3,189$	3,112
c (Å)	5,185	$-0,203x + 5,185$	4,982
P_{sp} (C/m^2)	-0,029	$-0,052x - 0,029$	-0,081
e_{31} (C/m^2)	-0,49	$-0,11x - 0,49$	-0,6
e_{33} (C/m^2)	0,73	$0,73x + 0,73$	1,46
C_{31} (GPa)	103	$5x + 103$	108
C_{33} (GPa)	405	$-32x + 405$	373

Table 5: List of different parameters of GaN, AlN and AlGaN according to the proportion of alumina from [25]

Heterojunction Between AlGaN and GaN

Lattice Mismatch and Piezoelectric Polarization:

Each material is characterized by its crystalline network made up of the different atoms that compose it. The lattice represents the smallest pattern of the network which, when repeated, will give the whole crystal structure of the component. Two materials therefore have different latticees. During their juxtaposition, elastic (non-permanent) or even plastic (permanent) stresses will appear.

Each crystal is characterized by constants called lattice parameters and collecting characteristic lengths or angles. a_0 appears as a key-parameter.

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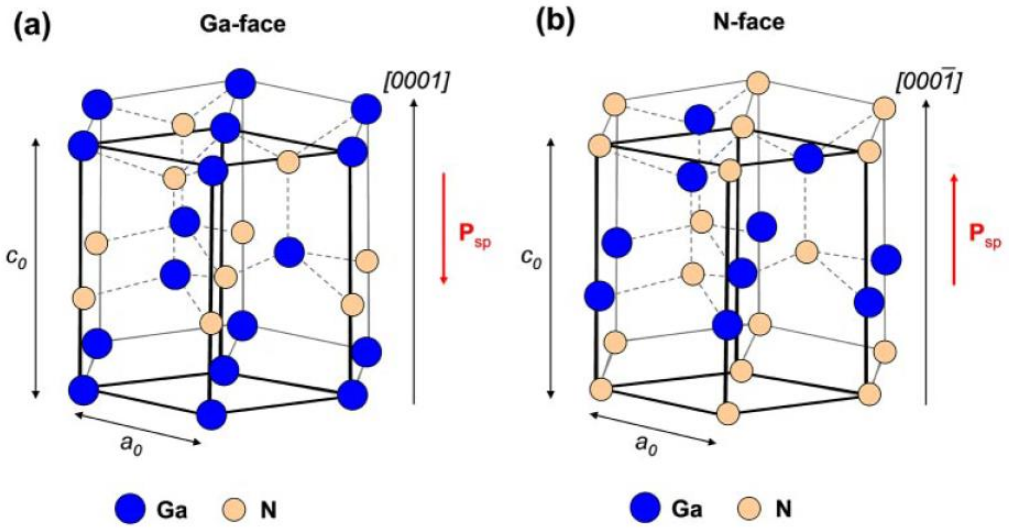

Figure 15: Representation of the GaN crystal lattice, according to gallium or nitrogen polarity from [36]

Following a heteroepitaxy where a fine material film of lattice parameter $a_{0\ \text{film material}}$ is deposited on a substrate, the substrate will impose its lattice parameter $_{a0\ \text{substrate}}$ during cooling. The lattice parameter of the deposited material thus evolves and becomes $a_{0\ \text{substrate}}$.
Two cases are then distinguished:

- $\mathbf{a_{0\ substrate} > a_{0\ film\ material}}$: the substrate tends to stretch the material film, the latter is in tension
- $\mathbf{a_{0\ substrate} < a_{0\ film\ material}}$: the substrate tends to compress the material film, the latter is in compression

AlGaN and GaN do not have the same lattice parameter, $\mathbf{a_{0GaN} > a_{0AlGaN}}$.
During deposition, the AlGaN is subjected to tensile stress, illustrated by the diagram below

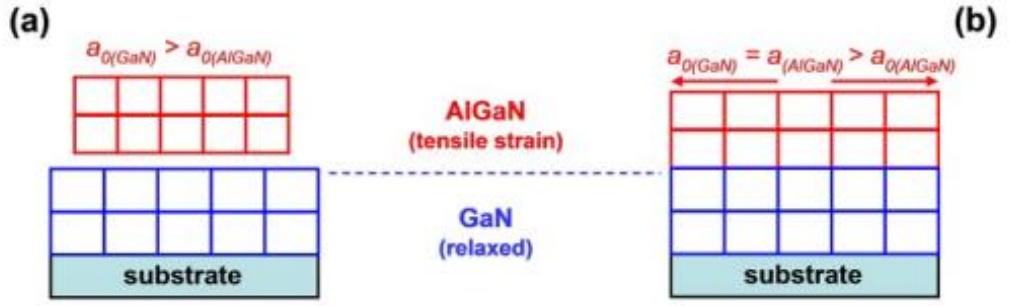

Figure 16 Illustration of the stress in tension experienced by the AlGaN deposited on GaN

These mechanical stresses will therefore reveal an additional constraint, called piezoelectric polarization.

Recall piezoelectric effect:

A physical deformation will induce an electric polarization. Charges appear on one of the faces of the crystal. This phenomenon is called electromechanical coupling. A force induces a deformation that itself induces an electrical voltage.

Pressure sensors work on that principle. Another common application is the lighter, the exerted force on the piezoelectric crystal produces an electrical voltage that will come to discharge abruptly in the form of sparks.

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There is also the reverse piezoelectric effect which is characterized by a physical deformation, induced by a voltage. It is on principle that the quartz clock works, it polarizes the quartz crystal that will vibrate at a characteristic frequency, stable and thus allow its use in watches**.**

In the case $\mathbf{a_{AlGaN} > a_{0AlGaN}}$, polarization is negative
In the case $\mathbf{a_{AlGaN} < a_{0AlGaN}}$, polarization is positive

In the case of a AlGaN/ GaN heterostructure, the piezoelectric polarization is negative, parallel to the polarization P_{SP}, towards the GaN as shown in the figure below [36].

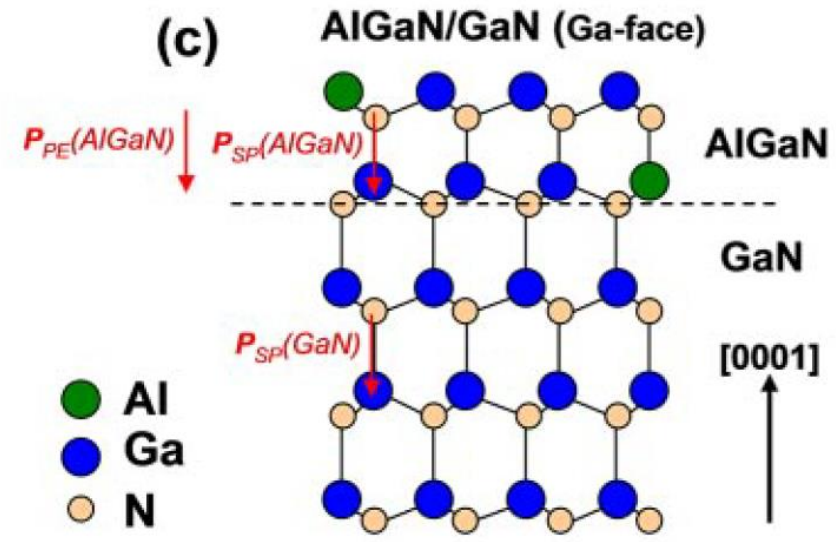

Figure 17: Representation of the different polarization vectors within the AlGaN network, based on [36]

These different polarizations within the constituent materials of the heterojunction will then induce charge densities within the AlGaN/GaN interface.

As listed in the above Table 4, $|P_{SP\ AlGaN}| > |P_{SP\ GaN}|$. With a thickness of the order of a micrometre, the GaN layer is relaxed and has reduced spontaneous polarization compared with AlGaN [24]. The quality of this GaN Layer is a determining factor to ensure a good confinement of electrons and reduce diffusion through dislocations or surface roughness [24].

Due to the tensile stress applied by GaN to AlGaN, this former presents also a spontaneous polarization The polarization seen in AlGaN is therefore higher than in GaN.
A higher charge density in AlGaN than in GaN is therefore present, which is represented in the diagram by the quantity of charges, represented by a sign "+" or "-" according to their polarity [25] .

This can be summed up as follows; in GaN, few polarization (relaxed) so low load shifting, whereas in AlGaN, many charges are shifted.

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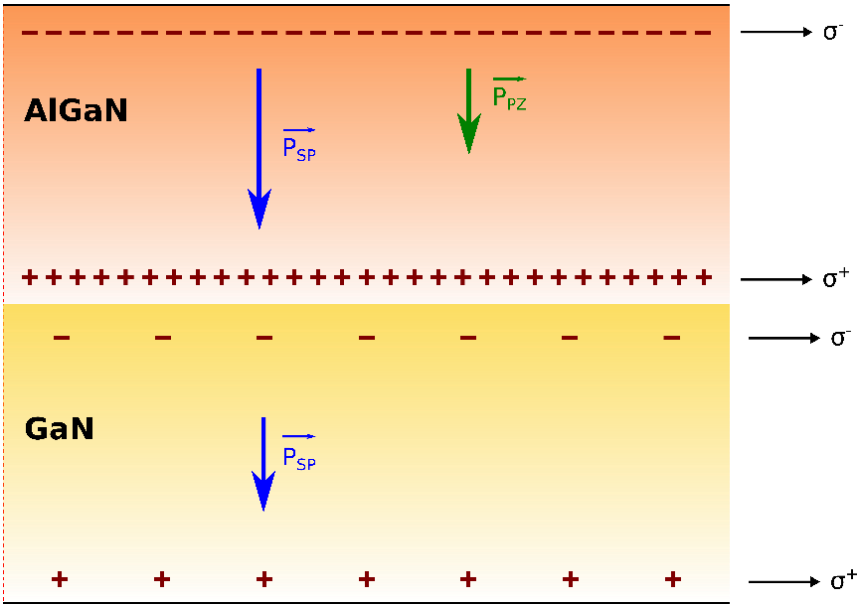

Figure 18: Illustration of charge densities due to different polarizations

In order to prevent the arrival of disruptive cations to compensate for the density of negative charges in the upper part of the AlGaN, a passivation layer is applied above the material, usually in SiN.

As a result of these different polarizations:

AlGaN is N-doped, i.e. a donor. There are therefore many free electrons. These free electrons will then be attracted by the positive charge density in the lower part of the AlGaN (the part with the highest number of "+" charges in the diagram above).

Negatives "-" charges are present in GaN near the interface and are likely to repel incoming electrons. However, this density of negative charges remains low compared with that of AlGaN, represented in the diagram by the low number of charges created in GaN [25].

The electrons are therefore attracted to the GaN, which is the first stage. However, at this stage, they are still in the AlGaN. It remains to explain how they cross the interface

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The Difference in Doping and Gap Makes the Electrons to Tilt and Confine Them in a Quantum Well

Heterostructures are characterized by Fermi level of each of the components of this heterojunction and thus by the potential barrier that will form at the various interfaces. This barrier conditions the passage of an electron or a hole from one material to another. It is determined by comparing the energy required for an electron in each material to be extracted from that material and moved infinitely away from it.

GaN HEMT is based on a specific case of semiconductors heterojunction formed by a GaN layer with an AlGaN layer. To completely understand the inherent mechanisms of heterojunction, a recap has been written in Annex 5.1
In the next paragraph, the focus will be on the involved heterojunction in GaN HEMT

HEMT GaN is indeed a specific case amid the possible different cases of heterojunction. It has the following characteristics:

- $\Phi_{AlGaN} < \Phi_{GaN}$: electrons will therefore spontaneously pass from AlGaN to GaN

In this case, the AlGaN Work Function Φ_{AlGaN} is inferior to the GaN Work Function Φ_{GaN}.

The bandgap of the AlGaN alloy is expressed by the following equation [20,25,37]:

$$E^g_{Al_xGa_{1-x}N} = xE^g_{AlN} + (1-x)E^g_{GaN} - bx(1-x)$$

Where x is the aluminium ratio, $E^g_{Al_xGa_{1-x}N}, E^g_{AlN}, E^g_{GaN}$ are the bandgap widths of $Al_xGa_{1-x}N$ alloy, AlN and GaN, and b the non-linearity term representing the deviation from the Vegard-type linear law [19], [20], [35]–[38].
b = 0.7eV is commonly used for both structures wurtzite and zinc-blende [25].
The x parameter commonly used equals to 0.3 [25,37]. As x rises, it increases spontaneous and piezoelectric polarization and so the 2DEG electrons density. But above 0.38 it causes the GaN to stress in compression. Beyond 0.5 the crystalline quality deteriorates and partial relaxation of the AlGaN layer appears. Finally, x = 0.3 is commonly used [25,37].

Material	*Eg(eV)*
GaN	3.44
AlN	6.2

Table 6: band-gap values for GaN and AlN at T = 300 K [20,24]

With the equation above and the listed values, it leads to $E_{g\ (A\ lxGa1-x)}$ = 4,41 eV and $E_{g(GaN)}$ = 3,44 eV. It finally leads to:

- $E_{g\ (AlxGa1-x)} > E_{g(GaN)}$

AlGaN is heavily N-doped, so its Fermi level is close to the conduction band. GaN is undoped, so its Fermi level is midway between the conduction and valence bands.

Before the junction, the energy levels are as follows:

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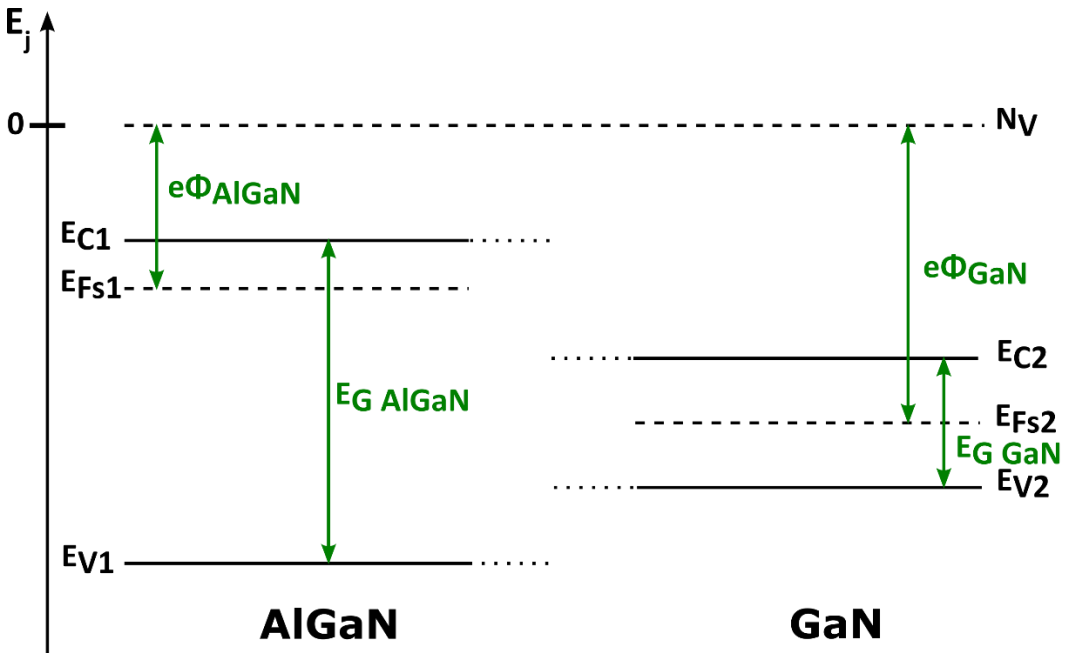

Figure 19: Band structure of the material AlGaN and GaN before junction, drawn from [3]

The electrons diffuse from AlGaN to GaN and the Fermi levels align according to Anderson's model. This adjustment is non-symmetrical, with the greatest variation in Fermi level observed in the least-doped semiconductor, in this case undoped GaN.

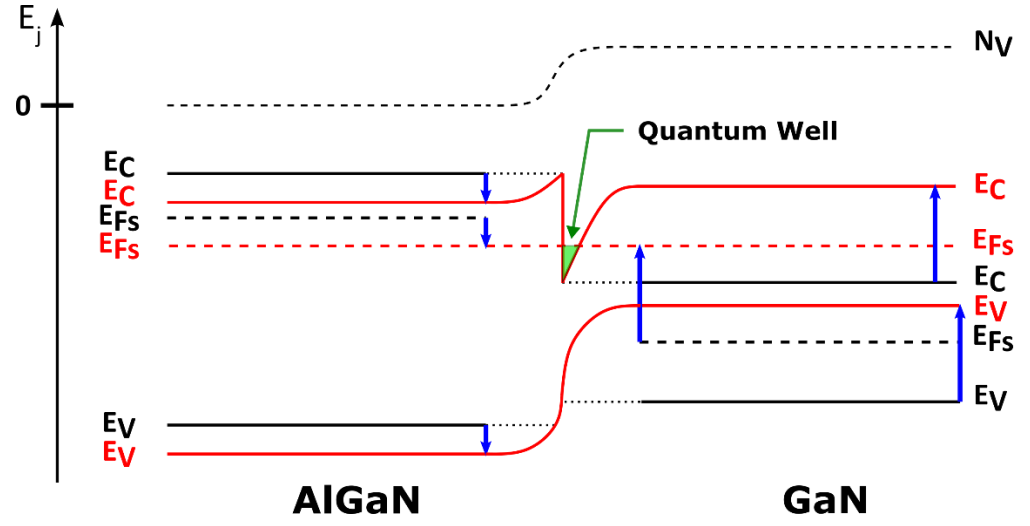

Figure 20: Band structure of the AlGaN / GaN heterojunction (black: before equilibrium, red: after) drawn from [3]

The electrons, leaving the doped region of the AlGaN, will create a depletion zone in this same material. This creates a potential barrier. GaN enters an accumulation regime.

The characteristics of the heterojunction mentioned above in Figure 20 will allow the appearance of a quantum well in which the electrons will remain confined. This cluster of confined electrons then becomes what is known as a 2-dimensional electron gas, since they can only move in a X-Y plane. This phenomenon occurs along the entire length of the heterojunction and leads to the appearance of a channel in which this 2DEG flows.

Because GaN is undoped, it contains very few impurities compared with doped AlGaN. The free electrons, normally slowed down by collisions with the impurities that gave rise to them, now find

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themselves in a quasi-pure area, confined with only electrons within the quantum well and evolving with a reduced number of collisions [41]. S.M.SZE and M.K.LEE in [8] directly linked electron mobility to reduced impurities as the mobility is inversely proportional to the total impurities concentration. Reducing the impurities reduces hence the probability of impact between carriers and impurities as ionized dopant. The formation of this 2DEG channel enables to highly increase the electron mobility, from 100 $cm^2V^{-1}s^{-1}$ in bulk GaN to 1000 - 2000 $cm^2V^{-1}s^{-1}$. The significant electron mobility of GaN HEMT comes from this phenomenon [20,25,36,42,43]. However, the GaN-Bulk can be unintentionally doped and it can be considered as a slightly n-doped semiconductor [20,26].

At this stage, it remains one unexplained phenomenon: the curvature of the AlGaN bands. Under the effect of polarisation, the conduction electrons in excess in n-doped AlGaN move toward the positive polarisation. Their departure leaves fixed positive charges. This appearance of charges will bend the energy bands as shown in the Figure 21 below.

The generated electric field, by reducing the overall electric field in the AlGaN, will then flatten the curves and give the final appearance of the figure:

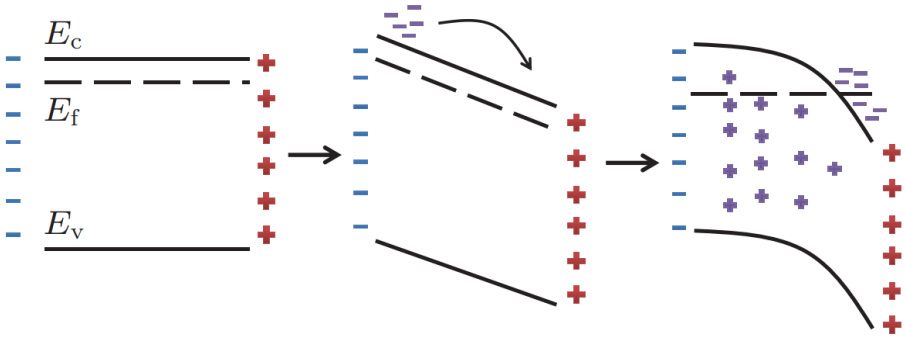

Figure 21: bending of the energetic bands in case of n-doped AlGaN [44]

After junction with GaN, the final Figure 22 is obtained:

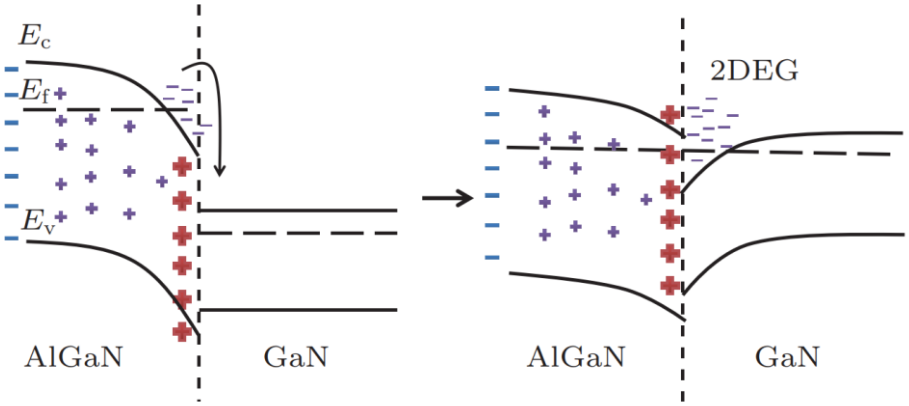

Figure 22: band-diagram of an n-doped AlGaN/GaN heterostructure, [44]

However, it remains a special situation where the AlGaN is not doped. The absence of mobile conduction electrons causes an absence of curvature and leads to the Figure 23 below.

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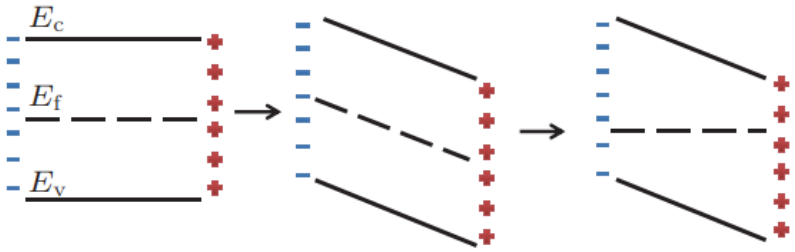

Figure 23: band-diagram of undoped AlGaN [44]

Nevertheless, this situation is not realistic. The presence of conduction electrons, particularly in the case of unintentionally doped AlGaN, come from surface-donors [44]. These electrons are then "activated" into the conductive band and move towards the GaN thanks to the polarization.

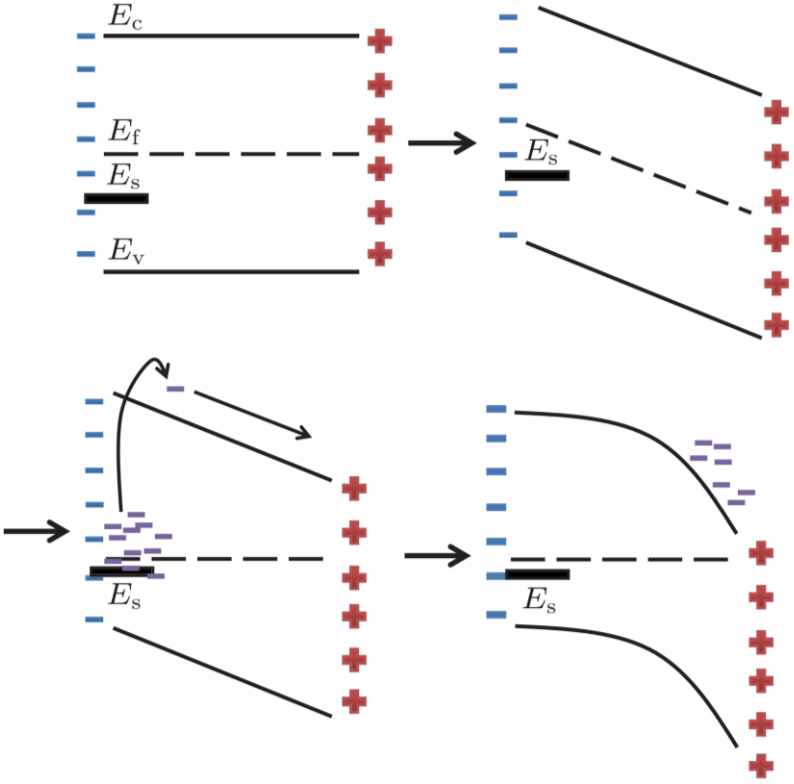

Figure 24: band-diagram of undoped AlGaN, taking into account surface-donors [44]

At the junction, these electrons switch to GaN.

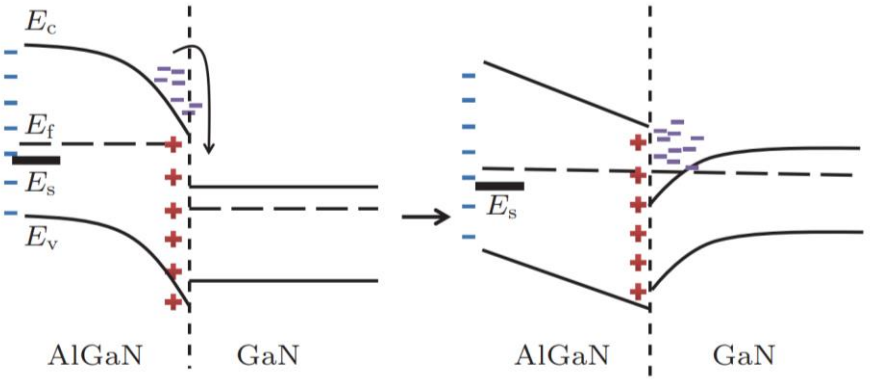

Figure 25: band-diagram illustrating the 2DEG channel formation [44]

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This last case shows that the doping of AlGaN is not necessary for the formation of the 2DEG of electrons. AlGaN is often n-doped in order to introduce additional electrons and thus increase the density of the 2DEG [45].

In conclusion, it has been seen that the formation of the 2DEG depends on several criteria. Firstly, the heterojunction of both materials, AlGaN and GaN will enable spontaneous and piezoelectric polarisations to be established, favouring the migration of electrons from AlGaN to GaN. The different work functions of these materials ($\Phi_{AlGaN} < \Phi_{GaN}$) and the distinct gaps ($Eg_{(AlGaN)} > Eg_{(GaN)}$) will respectively allow the transfer of electrons from AlGaN to GaN, and their confinement within GaN, through the formation of a quantum well. The spontaneous presence of these electrons hence gives the transistor its normally conducting nature. For this reason, various structures have been created to artificially give the transistor its normally blocked character, which is appreciated by industry.

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1.1.4 The Different Structures of GaN HEMT

The structure previously seen in Figure 13 is a "Normally-ON" or "depletion mode" structure. With no gate polarization (V_{GS} = 0 V), the 2DEG is present and the transistor conducts. The threshold voltage V_{th} is hence negative. This means that a negative voltage must be applied to the gate, below V_{th}, to stop conduction.

The main risk put forward by the current industry is the load supply of power in the event of a control fault, as the transistor remains conductive in the absence of gate polarization [24]. Non-conducting transistors for zero gate voltages are therefore preferred for security reason [15,21,28,46], and "Normally-OFF" or "enhancement mode" structures through several structures have been developed.

1.1.4.1 The Cascode Structure

Cascode technology is based on the use of a normally-OFF silicon MOSFET connected in series with the HEMT. When the MOSFET is positively polarized, for a value exceeding its threshold voltage, it switches on the Si MOSFET. The GaN HEMT, with a negative threshold voltage is already switched on as the gate is connected to the source pad of the whole component (S of the Si MOSFET in the scheme below) and the conduction between Drain D and S can be established. The transistor therefore becomes conducting. Conversely, when the MOSFET is not biased (zero gate voltage) or negative polarized, the drain voltage of the Si MOSFET starts to increase. For a sufficient value of D drain of the Si MOSFET, as $V_{D\ Si\ MOSFET}$ equals to $V_{S\ GaN\ HEMT}$, the voltage drop between $V_{S\ GaN\ HEMT}$ and $V_{G\ GaN\ HEMT}$ goes below the threshold voltage, $V_{GS\ GaN\ HEMT}$ becomes negative and blocks the GaN HEMT [20,24,47]. Finally, even if the gate control is ensured by the silicon MOSFET, whose blocking ability is around 30 V [27,48] it does not obstruct the high-voltage blocking capacity of the GaN HEMT and allows to apply a high electric field on it [20].

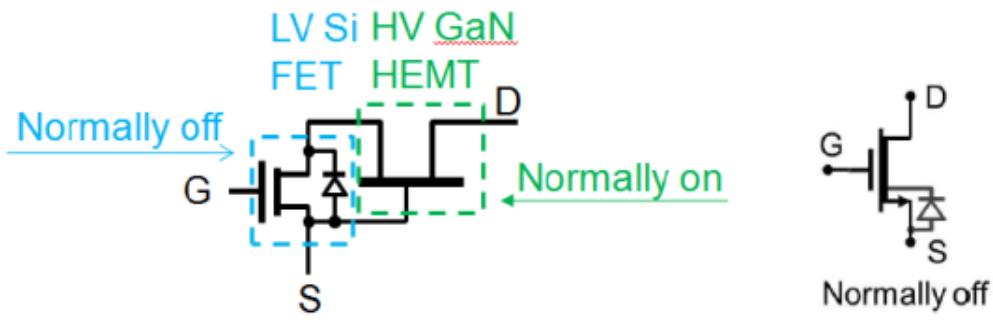

Figure 26: Diagram of a cascode structure combining a Si MOSFET and a GaN HEMT from [49]

This structure is characterized by a very good stability of the threshold voltage V_{th} [20,48,50]. The main advantage is that structure does not affect the physics of GaN HEMT and hence it reduces the possible defaults due to the production process. However, the combination with a silicon MOSFET hinders the main advantages of the HEMT. Silicon conducts heat less well than GaN, so the operating power lower. The switching frequency, which depends on the upstream MOSFET, is also reduced, whereas this is a major advantage of GaN HEMTs. Interest in this type of circuit is therefore limited. Furthermore, the connections between the MOSFET and HEMT are crucial, lead to complex packaging and may introduce parasitic inductances that can affect the component [20,51].

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1.1.4.2 The Recessed-Gate Structure

The recessed gate structure consists of etching the thin AlGaN layer to insert the gate through it. Reducing the thickness of the AlGaN at this point will locally reduce the aluminium concentration, so reduce the piezoelectric polarization, and thus interrupt the 2DEG channel. The main difficulties with this technique are the precision of the etching, which is delicate with an AlGaN layer of the order of tens of nm, and the need for uniformity. In fact, if this plasma etching is not well controlled, it will result in a threshold voltage variation, the etching depth influencing directly V_{th} [21,24,52]. Finally, the threshold voltage of the component, although positive, remains low, at around 1.5 V or below [24]. A scheme from the literature [20,27,48,53] about the concept of this recessed gate structure has been drawn in Figure 27.

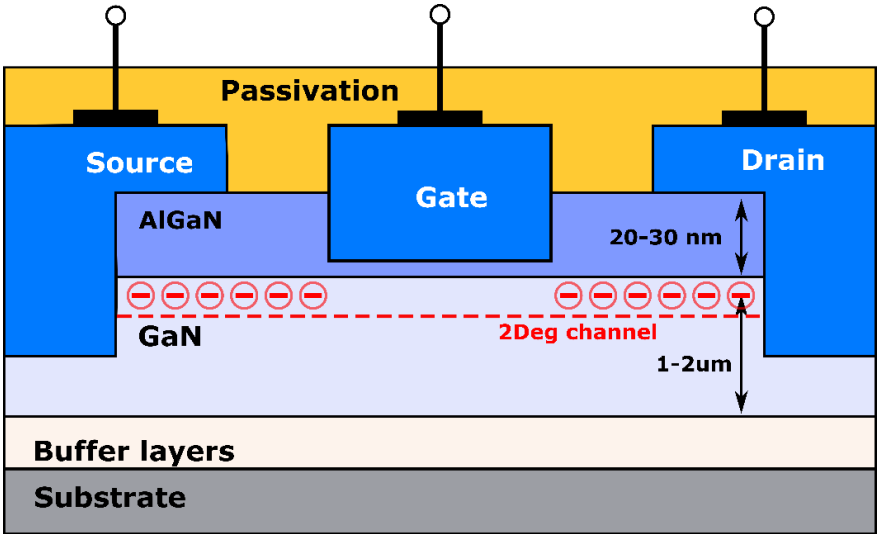

Figure 27: Diagram of a HEMT component in a recessed-gate structure

1.1.4.3 The MIS(MOS)-HEMT structure

The Schottky contact of the former structure presents a non-negligible gate leakage current, particularly during the turn-off where a reverse-bias gate leakage current is present and affects the switching [20,54].

To prevent this phenomenon, MOS and MIS-HEMT structure with an insulation layer beneath the gate have been developed. The term MOS-HEMT refers to a structure where the insulation layer is an oxide. If not, it is called MIS-HEMT. Several structures of MOS(MIS)-HEMT exist. Amid them, recessed-gate MOS(MIS)-HEMT are very close to recessed-gate HEMT unlike they have this insulation layer [21]. A scheme from the literature [20,35] about the concept of this recessed-gate MIS-HEMT structure has been drawn in Figure 28. The main drawback of this structure remains the existence of possible V_{th} instabilities through electron trapping at the insulator – AlGaN interface [20].

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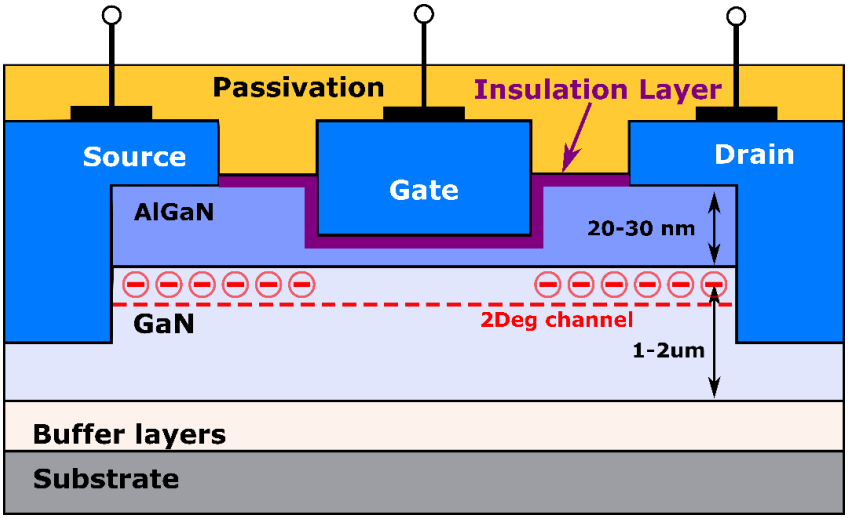

Figure 28: Diagram of a HEMT component in a MOS(MIS)-HEMT recessed-gate structure drawn from [20,35]

1.1.4.4 The Fluor-Gate Structure

Normally-off functionality can also be achieved by implanting fluorine ions under the gate. Thanks to its strong electronegativity (3.98), Fluor atoms become easily negatively charges Fluorine F^- ions. The negative charges of the fluorinated ions will then create a depletion zone and hence break the 2DEG channel [20,25,55]. The Figure 30 gives the aspect of the band-diagram in case of a presence of Fluor layer. Despite its greater simplicity compared with the recessed gate, the major disadvantage of this technique is the instability of the threshold voltage [24,25,54]. The scheme of an hybrid structure combining the MIS-HEMT structure with a Fluor implant under the gate has been drawn in Figure 29.

Figure 30 illustrates the bending of the energy bands at the interface with the layer of Fluor atoms. The fluorine ions act as negative charge and hence bend up the energetic band of GaN, depleting locally the quantum well. By applying a positive voltage on the gate, the transistor is once again able to form the 2DEG channel and to establish the conduction.

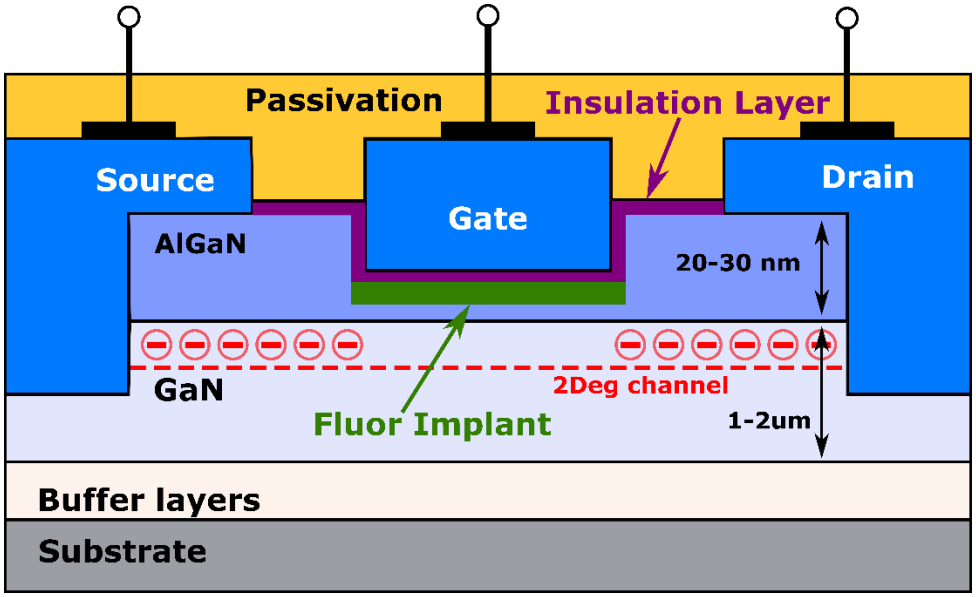

Figure 29: MIS-HEMT with a fluor gate structure drawn from [56]

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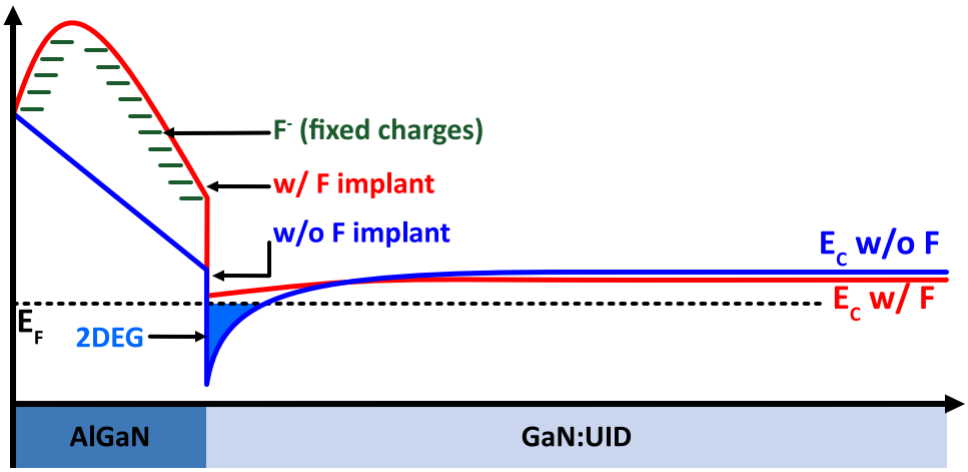

Figure 30: conduction band diagram of AlGaN/GaN heterostructure in presence of fluor layer (red) or not (blue)[20]

1.1.4.5 The p-GaN Gate Structure

Finally, there is the p-GaN gate technique. A layer of p-doped GaN is inserted between the gate and the AlGaN layer. The positively charged holes will attract the channel conduction electrons. Their departure from the channel will therefore temporarily cut it. At the same time, the positive charges of the holes in p-GaN are recombined with the displaced conduction electrons of the channel. There is therefore no longer electroneutrality in p-GaN, the negative charges dominate and, acting like electron repellents, break the 2DEG channel in an established way. This technique represents the main commercial solution but it is still being studied, in particular to make it more reliable and obtain a high threshold voltage (>2V) [25,57]. An example of a p-GaN structure, associated with a MIS-HEMT architecture has been drawn in Figure 31.

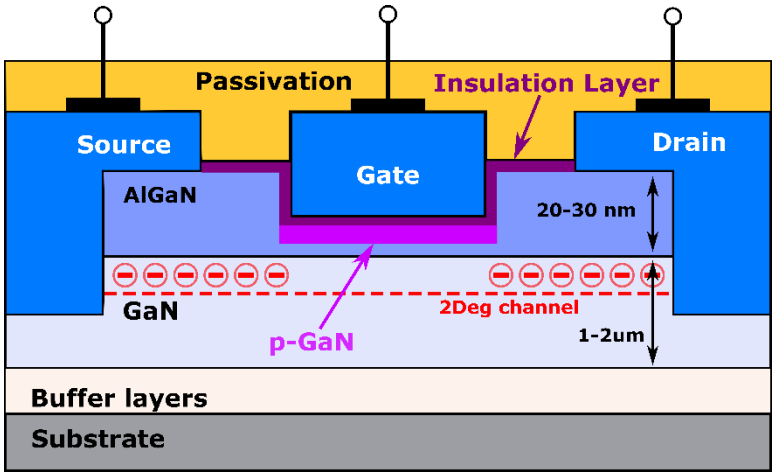

Figure 31: normally-Off GaN MIS-HEMT with a p-GaN gate drawn from [58]

Another structure, also based on the implementation of p-doped material beneath the gate has been developed. Instead of having p-GaN and a static barrier, the GIT (Gate-Injection-Transistor) structure relies on active holes injection thanks to p-AlGaN material [59–61] when a sufficient positive voltage is applied on the gate. A scheme of the structure is show in Figure 32

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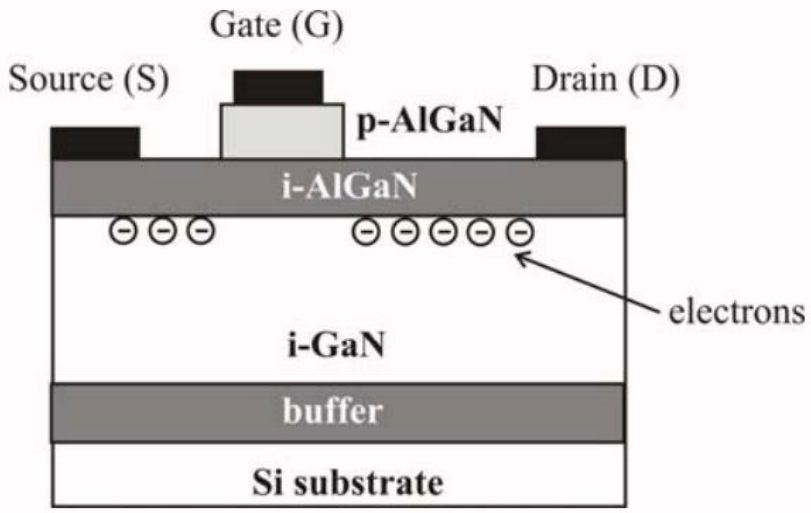

Figure 32: GIT structure from [60]

Structure	Advantages	Drawbacks	Manufacturers	Application
Fluor Gate	Easy to produce, positive threshold voltage	Limited adjustment of the threshold voltage	Mitsubishi Electric, Sumitomo Electric	RF and radar systems
p-GaN Gate	Good stability	Complex fabrication process	Transphorm, Infineon, GaN Systems	Power converters
HD-GIT	Reduced gate leakage current in comparison to p-GaN structure	Costly and complex fabrication process	Panasonic, Infineon	High power and high frequency use
Recessed Gate	Accurate control of the threshold voltage	Complex fabrication process, sensitivity of the surface	EPC, Qorvo, Wolfspeed	RF and radar systems
Cascode	Easy integration with Si MOSFET	Increased complexity, limits RF performance	GaN Systems, ON Semiconductor, Texas Instruments	Power conveters
MOS(MIS)-HEMT	Reduced leakage current	More expensive manufacturing process	Panasonic, Rohm,Fujitsu	Power converters, RF applications

Table 7: Summary about the several existing normally-off GaN Power Devices from [62–64]

1.1.4.6 The Benefit of Field Plates

In addition to the structures described above, metallic add-on, called field plates are inserted into the HEMT structure, particularly between the gate and the drain. These plates distribute the electrical charges and therefore spread the electric field, reducing its impact, particularly during the high-voltage operating. They are needed to improve the maximum voltage rating of the GaN HEMT [65].

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1.2 State-of-the-Art About Commonly Seen Problematics Related to GaN HEMT

Today, GaN is facing the same problems as the first GaAs or InP transistors [66], as M.J. Rosker has said in [67]: "While excellent performance is being shown routinely, the greatest challenge has been, and remains, achieving a high level of reliability and stability concurrently with high performance operation."

1.2.1 Threshold Voltage Variation due to Gate Leakage Current

The threshold voltage, which controls whether or not the transistor opens, appears to be a key parameter, but needs to be made more reliable and stable. Indeed, following various stresses, a non-negligible drift of its value can be observed. This variation can be attributed to various physical phenomena, such as the passage of a leakage current [68–70] but the main explanation remains the trapping/detrapping around the heterojunction [71] .

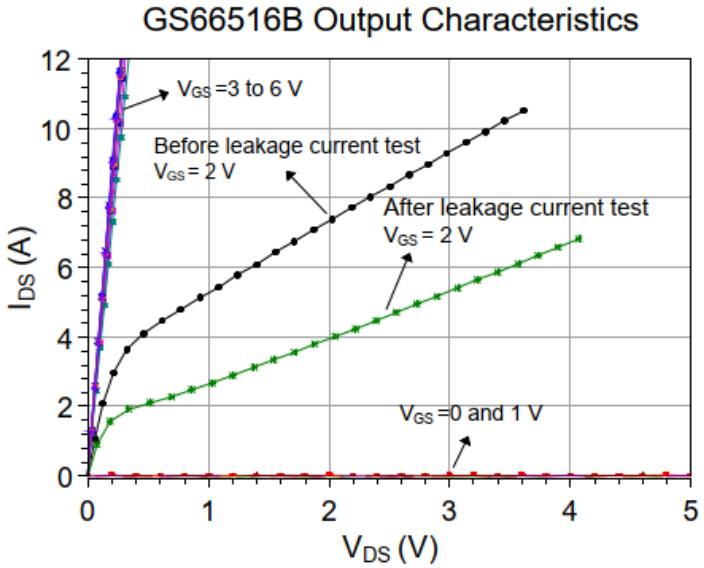

Figure 33: Output characteristic of a GaN Systems HEMT before (black curve) and after (green curve) passage of a leakage drain-source current [72]

The second physical phenomenon that can be at the origin of the variation of the threshold tension is more complex and is described in more detail in the following part. This phenomenon implies a very specific type of electron, called hot electrons [20,73].

1.2.2 Threshold Voltage Variation due to Hot Electrons

The behaviour of a transistor can be divided into three conduction states:
In the ON state, the applied gate voltage is higher than the threshold voltage, the transistor conducts. Conversely, in the OFF state the gate voltage is lower than the threshold voltage, the transistor does not conduct. Recall here that a threshold voltage V_{th} is defined in relation to a specific value of drain-source current I_{DS}. Saying that a transistor conducts or does not conduct, without attaching a current value to it, does not really make sense. Indeed, a semiconductor cannot be considered as perfectly insulating, there is always a leakage current, however it is small (about µA in the commonly found GaN HEMT). A drain-source current value has to be set from which the transistor can be considered in conduction state. The often-chosen value is I_D = 1 mA.

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There is then an intermediate state, called semi-ON, for which the gate voltage, although below the threshold voltage, is now close. The transistor is considered as a partially closed switch.
A weak current then flows through the channel (less than the 1mA value approached a few lines above), but a large electric field remains, the transistor being in reverse polarization. The conduction electrons, although in small numbers, will then be «heated» by the electric field, making them develop a significant kinetic energy. These particles are finally called «hot» electrons because of the relation $E = k_B.T$ linking energy and temperature, with k_B constant of Boltzmann.

Hot electrons occur mainly because of hard switching due to the presence of high electric field and high current together. So it could be assumed that short-circuit could create hot electrons, too [74].

In [75], A.Tajalli and M.Meneghini are interested in the link between hot electrons and threshold voltage variation. Indeed, these accelerated electrons will then have enough energy to get out the potential well in which they were previously confined and will cause impacts in the surrounding materials [66].

To verify the existence of hot electrons, electroluminescence is used. These highly energetic electrons de-excite by emitting light. These emitted photons are then captured and their analysis makes it possible to quantify the number of hot electrons [66].
In [75] both in the semi-ON and ON states, the drain – source channel is polarized below 50 V (a minimum of 50 V drain-source polarization is needed to observe the phenomenon of hot electrons, as the latter require an electric field high enough to be excited). Only the amount of electrons will differ quasi-conduction for the semi-ON state from a full conduction for the ON state.

As a consequence, hot electrons have to be considered and their impact will be carefully studied during short-circuits.

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1.3 State-of-the-art About Short-Circuit for Power GaN HEMT

1.3.1 Some Definitions about What Is a Short-Circuit

GaN components, with the wide-band gap (WBG) technology represent a new type of transistors. Their high current density is one of the most relevant points. Regardless very attractive performance like low conduction and switching losses, fast switching, high-voltage and high-temperature operation, [21,46,76–78] , robustness and reliability of GaN components keep unavoidable keys for their future commercialization and will be indispensable for a large spread in automotive or avionic industry [46,79].

Resisting against major incident operations belongs to this necessary robustness. With both concomitant high-voltage and high-current between drain and source terminals, short-circuits are considered as one of the most unwanted operations with a significant energy to dissipate through the transistor [46,78,80–82].

Figure 34 illustrates the simultaneous current and voltage high-values during a short-circuit. Short-circuits are characterized by a very fast rise of the current, well in excess of the component current rating and in less than one microsecond, then a sharp reduction of the drain current. As it has been explained above, the harmful aspect comes from the fact that during all this time drain-source bias remains at quasi-constant level, except during the switchongs where a brief voltage drop (at turn-ON) or overvoltage (at turn-OFF) can be observed.

Furthermore, one of the advantages but also difficulties of GaN components lie in the fact that the current rise slopes are extremely high. GaN Systems reported in [83] that the drain current need only 5 ns to reach 30 A at the turn-ON. With a typical parasitic inductance of 15 nH, it already leads to an overvoltage of 150 V.

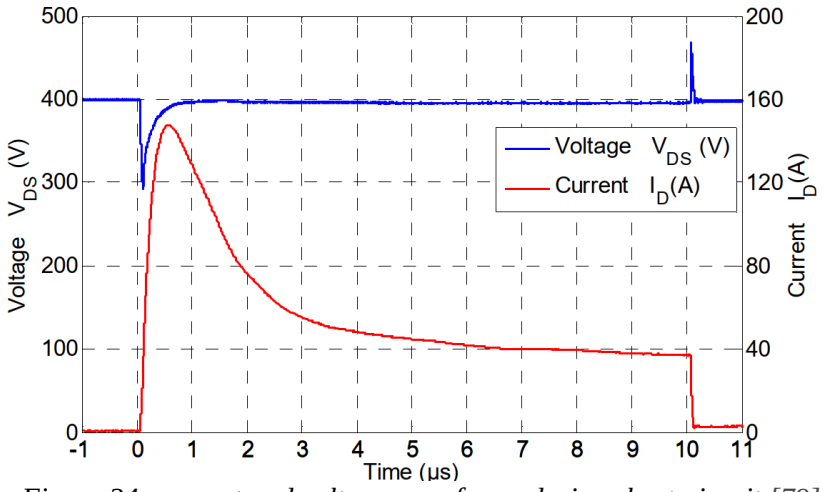

Figure 34: current and voltage waveforms during short-circuit [79]

Figure 35 below shows a typical failure with a recognizable uncontrolled drain current rise. After 460 ns it can be indeed noticed a sharp increase of the drain current value, much higher than the former value near t = 100 ns. It is also associated with a collapse of the drain voltage. These two combined effects suggest a device failure. The upstream protection opened the circuit after 70 µs, quickly disconnected the DUT from DC capacitors and thus avoiding its explosion.

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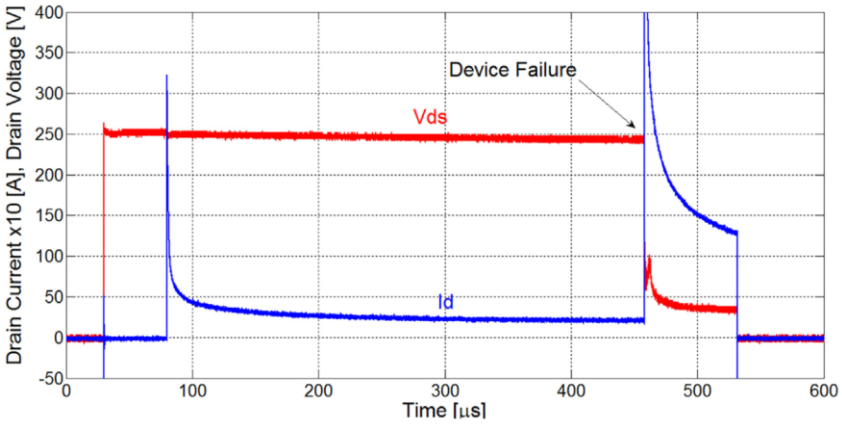

Figure 35: drain current and polarization waveforms during a destructive short circuit test applied on 650 V GaN HEMT [84]

Three types of short-circuit exist. Amid them, short-circuit type 1 and type 2 must be distinguished. The third type (type 3) is specific to component with antiparallel diode and reverse conduction [21,85].

One of the most occurring short-circuits is the type 1 [34,78]. As a consequence, the type 1 test is preferred in the industry [11], [12] and so in research papers. During the Type I test, the device is formerly gated off, hence withstands a high voltage and is switched ON. Consequently, a significant current flows through the transistor. The rise of the current is very fast, about tens of nanoseconds and then reduces due to the temperature increase. Therefore, that type of default is also called hard-switching fault. As the voltage is still present between drain and source of the device, the power dissipation is significant and thermal failure can occur. In the Figure 37, for the red graphics a fast rise of I_D is seen with a constant drain-source voltage V_{DS} which leads to a thermal failure. Reducing the drain-source current I_D with detection and protection systems in blue graph prevents the device from breaking up as shown in the Figure 34. Such solution have been patented for instance with Short-Circuit Current Limiter [46] but remain limited and present substantial drawbacks. It IS also to be mentioned that several types of failure mechanisms exist. It will be further detailed.

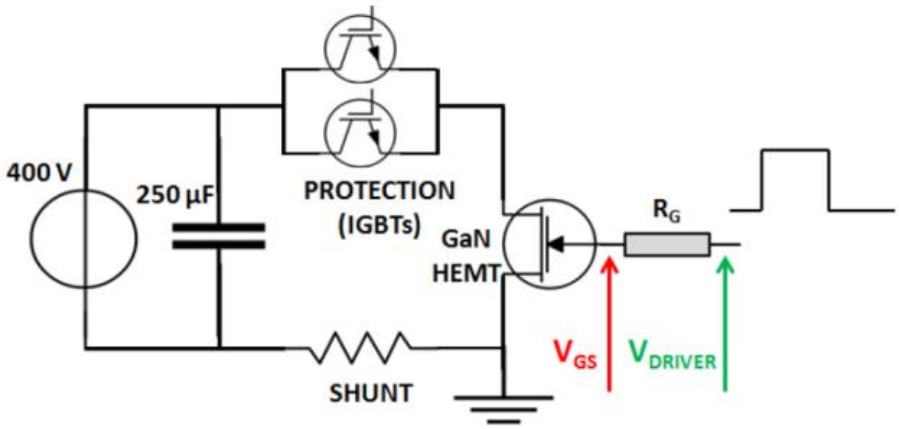

Figure 36: Schematic of a type I short-circuit test bench from [79]

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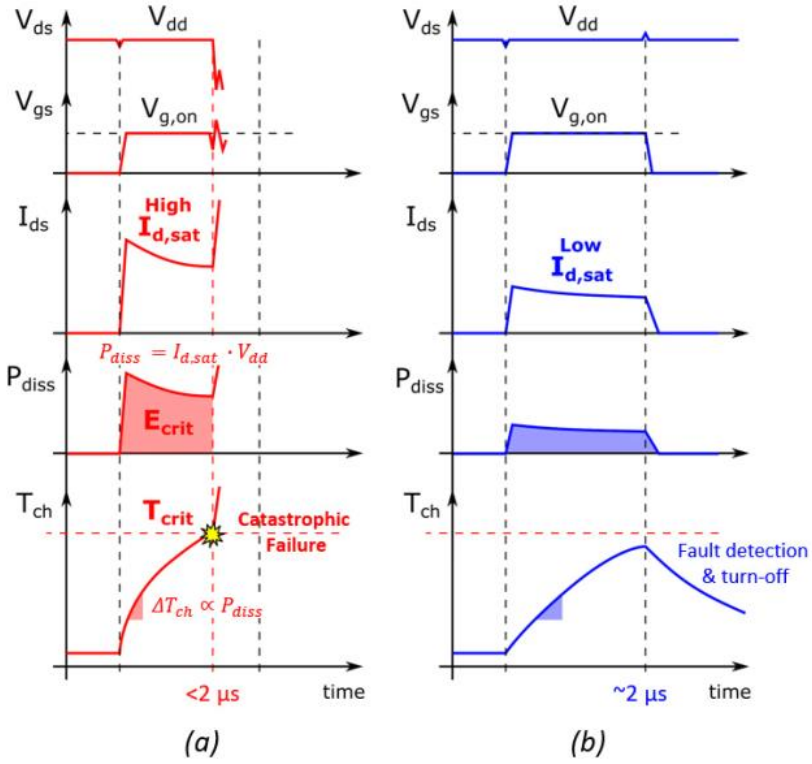

Figure 37: Schematic waveforms during short-circuit for high current and high power density (a) and lower current and power allowing the protection system to detect the fault before a too critical temperature [46]

For short circuit type II, the DUT (Device Under Test) is already gated ON before the default and conducts a current. For that reason it is called fault under load [21,35]. Considering the fact that conducting the default will increase the gate-source voltage, type II is considered more harmful than type I [21]. The initial strategy of this thesis was to work on both types. However, due to the necessary optimizations and a lack of time, only Type 1 SCs are studied in this manuscript.

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1.3.2 A Brief Historic and Contextualisation About Short-circuit

In 2013, the author of [87] predicted poor short-circuit performance of lateral GaN components compared to well-known silicon vertical IGBTs. The author of this article notably highlights an electric field ten times more important for lateral GaN than for Si IGBT during strong drain-source polarizations. Coupled with an increased current density for HEMT GaN technology, the dissipated heat power during a short circuit is significant with a possibility of tens of kilowatts to dissipate in devices of a few millimeters width. A short-circuit is linked to a very fast rise of the drain current [46]. It would be all the more destructive as, unlike Si IGBT, the current circulates in a very thin region called the 2DEG Channel (AlGaN layer of the order of nm, GaN of the order of tens nm [24]). The direct consequence would be extremely localized heating points. Added to all this a relatively bad thermal conductivity, to compare particularly with silicon carbide SiC, it is assumed that the triggering of these localized heating spots will be extremely rapid, making it all the more difficult for HEMT GaN transistors to be reliable in the face of short-circuits.

To compare, SiC components withstand a fault duration between 8 and 13 µs, on a 600 – 700 V bus [21]. According to [88,89] SiC components are able to resist to thousands of repetitive short circuits for a duration greater than 10 µs. Most of the time the failure occurs in the gate oxide.
Saturation current reduction and a rise of on-resistance are the only signs of fatigue.
For SiC components, a rising leakage gate current can also be perceived as a sign of the short-circuit and allows to prevent failure [90]. On the contrary there is none of it for GaN components [35,91].
That is why today the failure origin of GaN is not well understood, with unexplainable very fast failure about a few microseconds or even hundreds of nanoseconds or long failure with tens of microseconds).

In parallel to this harbinger of bad news, if first studies on short-circuit were observed from 2013, ten years later, the situation is rather bleak. It remains limited in several aspects. Normally-off Technology with p-GaN components and cascode has been almost exclusively studied to the detriment of normally-on technology [34,35,46,58,77,78,81,84,91–102]

In [35] some technologies have been tested, among them the normally-off HEMT as p-GaN, cascode and normally-ON HEMT. A summary is presented in Table 8. The only normally-ON HEMT which has passed the short-circuit event, with a duration of 30 µs, had a gate-bias close to its threshold voltage (semi-on state). Consequently, the failure was rather due to the high electric field than the short-circuit characteristics. For enhancement-HEMT (E-HEMT or E-mode HEMT), even if few samples withstood beyond the critical 10 µs, the majority failed before 1 µs of short-circuit events. This non-robustness of the GaN components can be linked to the considerable density of current and the significant thermal power to dissipate in a small volume.

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TABLE I
STATE-OF-THE-ART OF SC CAPABILITY

Device technology	V_{BR} (V) - I_D(A)***	V_{DC} (V)	t_{on}||t_{SC} (µs)	ΔI_D (%)	V_G (V)
GaN EHEMT [20]	200 - 3	50*	10	25	+4/0
		100	2	-	+4/0
GaN cascode [2]	600 - 20	150*	10	39	+12/0
		200*	10	-	+12/0
		<280*/**	10	-	+12/0
GaN cascode [18]	600 - 5	400	7.8	-	N/A
	600 - 16	400	7.7	-	N/A
	600 - 30	400	7	46	N/A
GaN DHEMT [19]	650 - N/A	250*	10	40	0/-15
		300	4	-	0/-15
		350	0.9	-	0/-15
		400	<0.5	-	0/-15
		400	30	-	-1.5/-15
GaN cascode [16]	600 - 18	100*	10	70	+10/0
		100	14	-	+10/0
		200	4	-	+10/0
		300	1.8	-	+10/0
GaN EHEMT [16]	600 - 16	100*	10	33	+5/-3
		150	4.5	-	+5/-3
		150*	4	-	+5/-3
		200*	2	-	+5/-3
GaN EHEMT [17]	650 - 60	400*	10	90	+5/0
		400	1.2	-	+5/0
		400*/**	500	-	+5/0
	650 - 30	270**	>800	-	+5/0
		270**	>800	-	+5/0
	650 - 22	400	~0.2	-	+5/0
		400	~0.2	-	+5/0

* Non-destructive SC results / ** Only for few parts / *** Rated values

Table 8: state-of-the-art of short-circuit capability from [35]

The extend of the studies for p-GaN components has been sum up in Figure 38. It represents the duration of the short-circuit and the applied voltage. The green dots mean the device has withstand the short-circuit while in orange it has failed. If it can be noted that devices withstand the highest voltage, it has to be mentioned this was at the price of concessions (overheated environment or increased gate resistance for instance). These adjustments, like reduced gate-source polarization, higher gate resistance or overheated environment are depicted in Figure 39 . These phenomena will be further explained below. Without such adjustment, the maximum drain-source polarization remains around 150 – 200 V. Moreover, if the performance in the short-circuit remains limited in voltage, the components break very quickly, sometimes randomly and as consequence failure mechanisms remain misunderstood. No papers are interested in technology normally-on, despite the fact it is the simpler structure (no upstream Si MOSFET as in the cascode structure or specific modification of the gate structure as in the p-GaN configuration. In addition, current studies mainly focus on the withstand of the component after a unique short-circuit and the duration before failure.

Recent study ([97]) showed a major robustness improvement, with TLF (Time Leading to Fail) around hundreds of microseconds with the concession of a low current, under a bus voltage of 400 V and a gate-source voltage of 5 V (HEMT p-GaN from GaN systems). Nevertheless, if robustness has made progress, it's not the same for fatigue strength. Components did not endure more than twenty

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short-circuits of only 20 ns [97]. It is even worse for a short-circuit duration of 1 µs, the failure arrived at the second event.

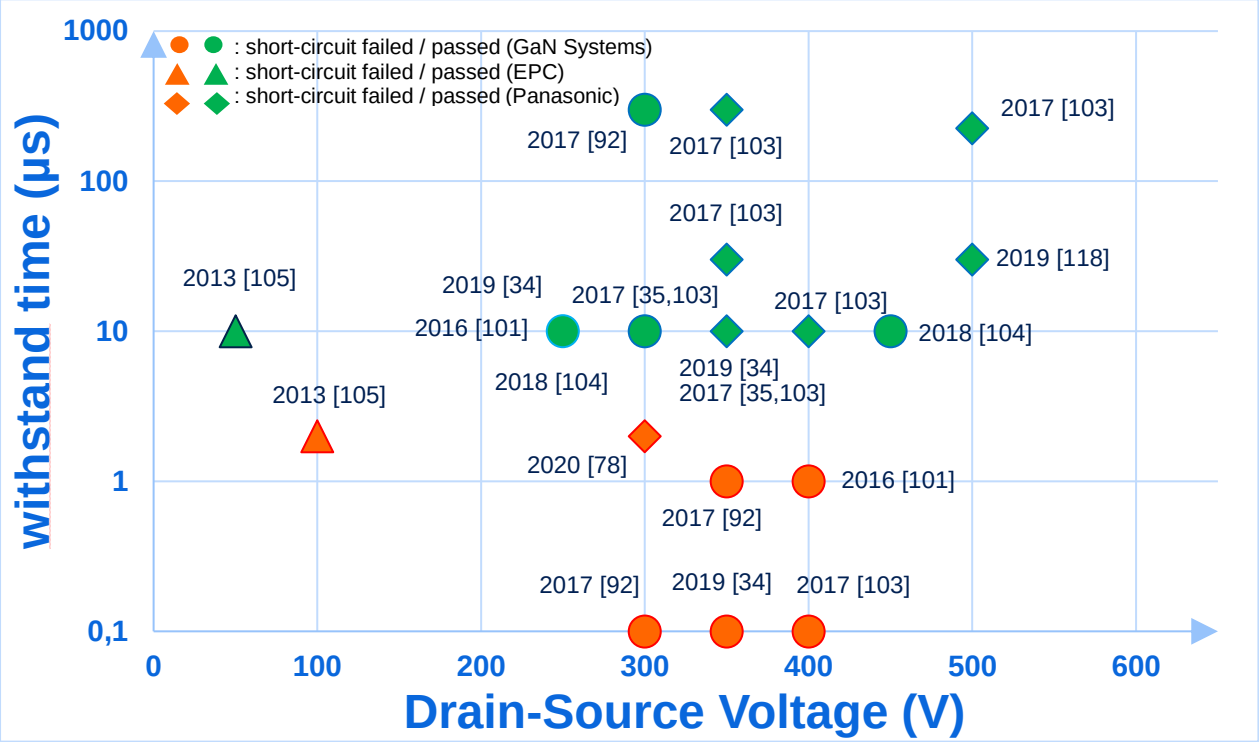

Figure 38: bibliographic state of the art about unique destructive short-circuit on p-GaN components [34,35,78,81,91,92,101,103,104]

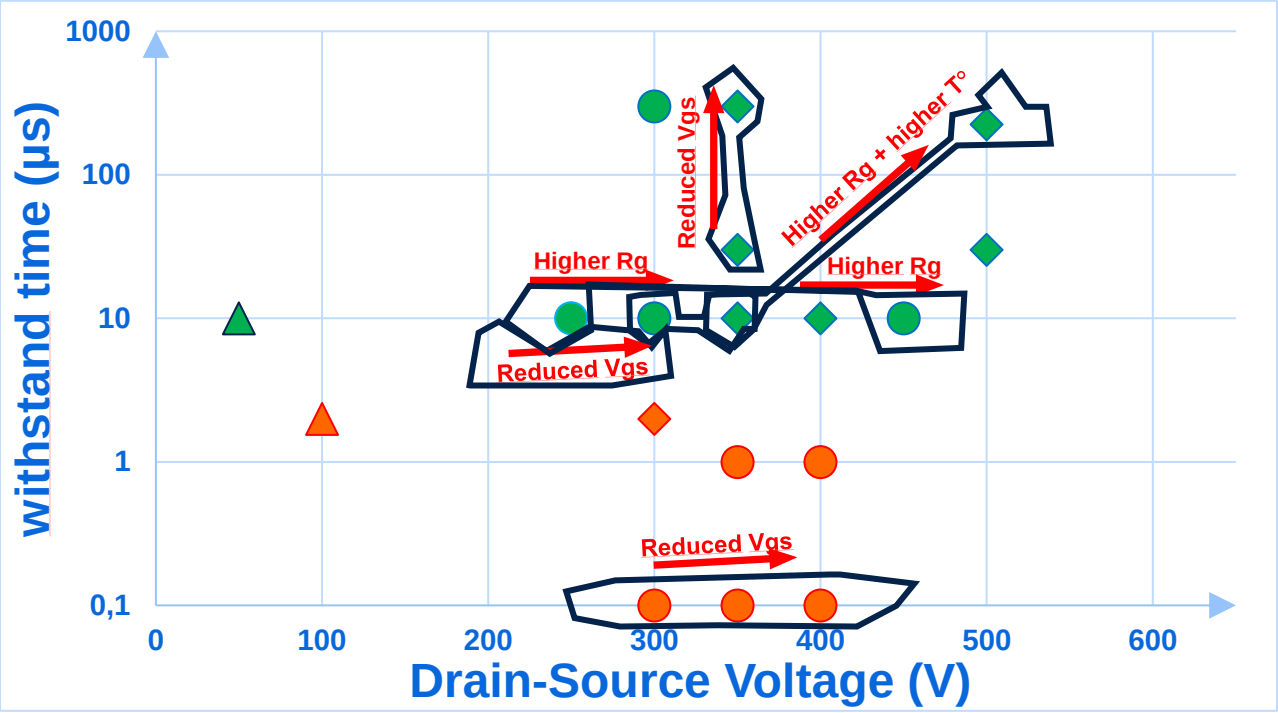

Figure 39: Representation of the concessions to increase the withstand time or the drain-source voltage

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1.3.3 Why Are Today Protection System Not Relevant?

The study of short circuits is necessarily linked to time. Under a certain voltage, the component must be able to resist for a minimum fixed duration. Considering the significant quantity of energy to dissipate, resisting a short-circuit for 100 ns is not the same as resisting for 100 µs. This withstanding duration of the device under a given voltage is hence studied. That duration, called TLF, needs to be sufficient until the protection system detects the default and turns off components before catastrophic failure [80,105].

For IGBT, this time of protection actuation is today between 6 µs and 10 µs [99] . However, it is always considered with a certain margin and conventionally set to 10 µs. Other protection systems exist, like [99] with the desaturation circuit but it appears limited and not relevant for the specific case of GaN component [106] because of the too fast commutation speed of GaN HEMT. To protect efficiently the system would indeed react in less than 300 ns [54], 300 ns [35] or 400 ns [94].

Consequently, a faster response of the protection system, linked to a drop of the required withstanding time of transistor would be an idea. However, a too fast response could lead to an erroneously activation due to switching transients and noise. In fact, under 400 V GaN components are able to switch faster than 10 ns [28,83]. In regard to the parasitic capacitance and inductance, transient currents have to be considered and could provoke an accidental actuation of the protection system. As it is explained in [46], too fast and the systems risks to activate by mistake, too slow and the device will not sustain the short-circuit and will be destroyed.

However the component withstanding time must be known very precisely [35,97], this in order to correctly design a possible protective circuit, associated with the converter where the component will be used [76] .

To evaluate the GaN HEMT robustness, criterion differ from articles. Some state that 650 V GaN components have to resist under a load of 400 V, long enough to let the protection system trigger. The resistance criterion for at least 10 µs is regularly seen [1], [7], [33]. In [105] these 10 µs are associated with a polarization of the drain-source of 80% of the nominal voltage. For [80] it is under a 400 V bias that the 650 V components must withstand 10 µs. For [46] it is under a bias equal to two-thirds of the breakdown voltage. In [103] for typical power electronic application, the requirement for the DUTs is to withstand a SC within 50% of the nominal breakdown-voltage for a duration of 10 µs.

As it has been shown in Figure 35, simultaneous high-voltage and high-current represent a significantly high thermal power to dissipate rapidly [97,105]*. This is all the more critical as this thermal power develops in the 2DEG channel, an extremely reduced volume. This logically brings the idea of thermal breakages, as the component could not dissipate the short-circuit energy quickly enough* [21,46,106,107].

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1.3.4 One of the Most Visible Phenomena of the Short-Circuit Which Yet Does Not Make Consensus, The Reduction of Drain Current:

The explanation of short-circuit failure is a complex field of study. This can be verified when, even before looking at the reasons for the breakage of a component, it is already difficult to agree on the behaviour of the transistor during short-circuits. Indeed, one of the most visible phenomena of the short-circuit, the reduction of drain current does still not make consensus,

As it has been shown in Figure 34, during a short-circuit event, drain current rises very rapidly and after a brief but high peak, starts to decrease [34,35,91,101,104]. However, there is still no consensus in the literature on this phenomenon.

1.3.4.1 Reduction of the Carrier Mobility or Saturation Mobility by Thermal Increase Can Be One of the Explanation About Drain Current Reduction

The most obvious explanation is based on the component self-heating. During the short circuit, the significant amount of energy to dissipate causes a rapid heating of the component [46], especially in the 2DEG Channel, demonstrated with the TCAD [35]. This heating, through an increase of thermal agitation, will a bit more disrupt the load carriers and thus reduce their mobility [34,58,108,109].

When looking at the p-GaN HEMT, this reduction of drain current is particularly important, and significantly higher than more mature components such as silicon IGBT and MOSFET, with a higher reduction of 30% as it is shown on the Figure 40 [58].

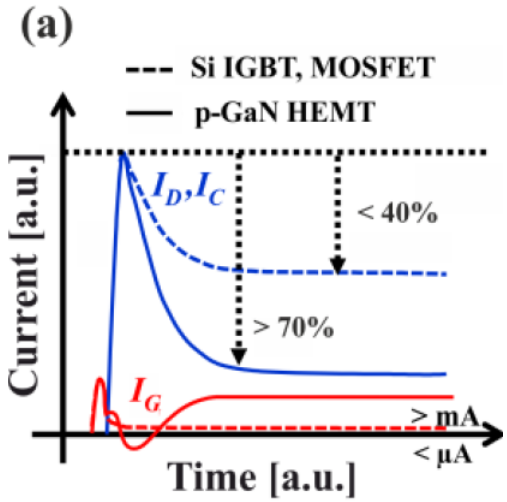

Figure 40: Gate and drain current waveforms during a short-circuit [58]

1.3.4.2 Drain Current Reduction Cannot Be Explained by the Only Reduction of Carrier Mobility

Many authors [21], [30], [31], [82], [96], [102] stated that the drain current reduction cannot be explained by the only reduction of carrier mobility. They put forward the idea of a role of V_{DS} polarisation but also of V_{GS} and more precisely of the gate in the case of enhancement Mode HEMT (p-GaN).

The authors of [34], with the Figure 41 noted that a larger bus voltage increases the drain current reduction without affecting the current slope $\frac{di}{dt}$. The same observation can be made at 25 °C or 125 °C. This drain current reduction is also observed in [104] with the Figure 42.

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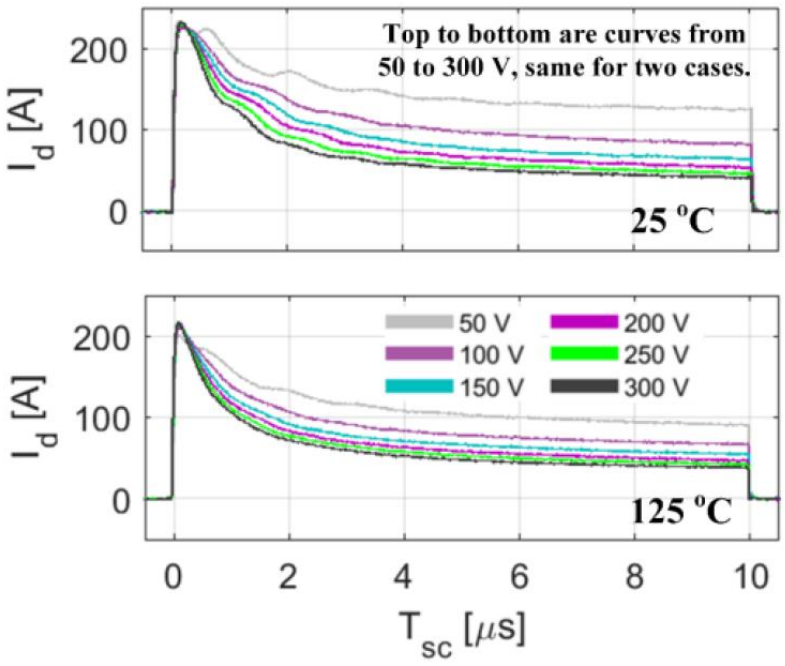

Figure 41: short-circuit experimental current waveforms for many drain - source polarizations at 25 °C and 125 °C [34]

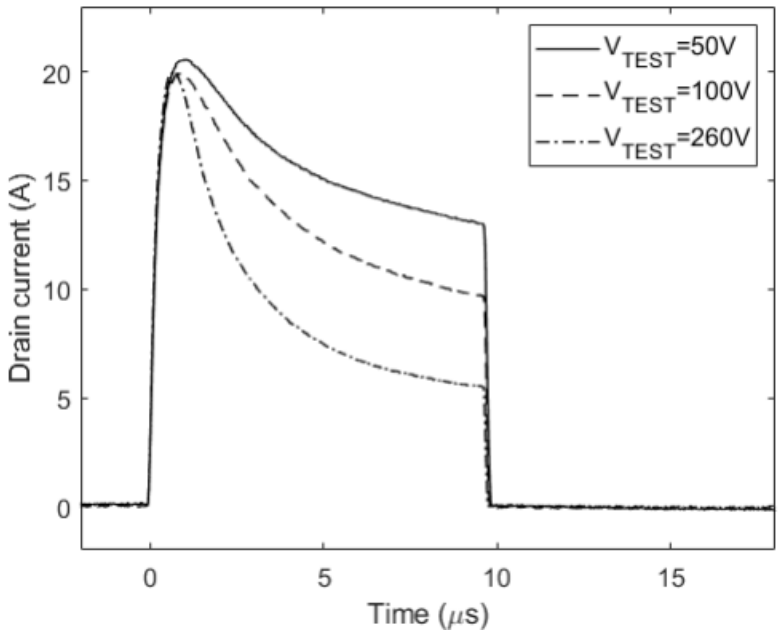

Figure 42: Measured drain current waveform during a short-circuit test [104]

In first instance, that can be easy to understand, the higher the drain-source polarization, the bigger the energy to dissipate. With a bigger energy to dissipate, the temperature will rise higher in the 2DEG channel and, according to the previous paragraph, will reduce the carrier mobility and so the drain current.

The point of [34] is they considered the gate-source polarization through the Figure 43. What can be noticed is that the rise of V_{DS} has an impact of V_{GS}. More precisely the higher V_{DS} is, the higher is the reduction of V_{GS}. This V_{GS} reduction can thereafter easily be linked to drain-current reduction.

As a consequence, gate-source polarization seems to have an impact on drain current reduction and do not let thermal aspect to solely explain that current reduction.

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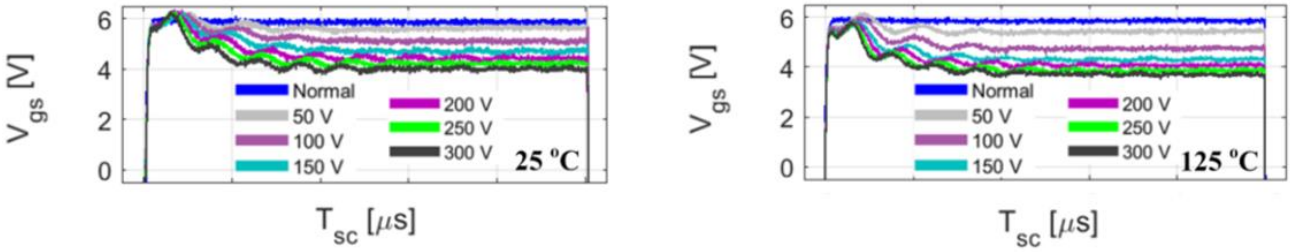

Figure 43: V_{GS} reduction based on an increase of V_{DS} from [34]

What is remarkable is that ambient temperature seems not affect the extreme values while keeping in mind that ambient temperature is different than internal temperature.

To understand how this drop of V_{GS} can exist, the authors get deeper and focused on I_G .
The behaviour of the gate current has to be distinguished depending on the structure. In the case of cascode and MIS-HEMT, two structures where the gate current has been minimized, a brief peak of gate current can be observed just after the turn-on, explained by the charge of the gate input capacitance C_{iss}. The gate current comes rapidly to zero once the capacitance is charged. For p-GaN structures, the gate current do not go to zero and keeps having a non-negligible value of tens of milliamps [35]. This assertion is the key to understand the role of I_G in the specific case of p-GaN HEMT.

In [34,35] and for p-GaN components the authors noticed an higher gate-source leakage current at 125 °C than 25 °C, with values sometimes a hundred times higher than normal.

According to [15], [24], [30]–[32], [33,] this I_G increase is caused by the high temperature of the 2DEG channel and the gate. Heating the gate occurs a rise of gate current [105,114,115], which lower V_{GS} and, by bringing it closer to V_{th}, reduces the drain current. They underlined that this phenomenon, a fast reduction of drain current, correlated with an non-negligible increase of I_G, is unique to p-GaN HEMT and was not observed in Si IGBT/MOSFET, SiC MOSFET and Cascode GaN HEMT.

Landel explained in [21] that this effect is all the more present for p-GaN component with gate based on a Schottky contact, such as components from GaN Systems among others. On gate components whose gate contact is ohmic (Panasonic for example with the HD-GIT), this effect is retrieved but in a smaller proportion, these components being designated to already let pass a gate current in normal operation.

However, Landel challenged this idea by stating in [35] that according to the simulations, the increase in gate current is not sufficient to lead to a reduction in the V_{GS} bias and consequently a decrease in drain current. The drain current would hence be mainly due to the reduction of the mobility of the carriers μ(T), decreasing with temperature [35].

Nevertheless, heat alone cannot explain this phenomenon since an increase in temperature causes a decrease in the mobility of carriers, in other words, an increase in the resistance of the gate in this case. If this increase of the channel resistance is verified for the drain current, with the consequence of the decrease of the latter, the increase of the gate current goes backwards from this explanation.

If the gate polarization has been addressed, the authors of [35,91,110] noted a reduction in the threshold voltage when the gate heats up .
« As the gate electro-thermally behaves like a pn-junction, $V_{GS(th)}$ also decreases with T_{Gate} » [35]. A reduction of the gate threshold voltage imputable to repetitive short-circuit has also be noted by the authors of [34]. With the Figure 44 a reduction is remarked after 5 consecutive short-circuits.

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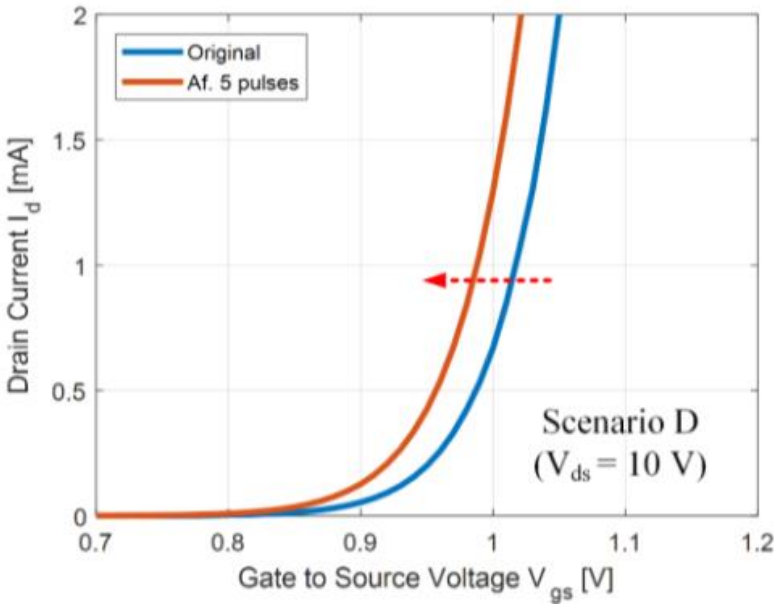

Figure 44: reduction of the gate threshold voltage after 5 consecutive short-circuits[34]

1.3.4.3 Impact of the Gate

The gate can have an impact, not only on the saturation level but also on the peak value. Sun et al. in [97] have been able to link the drain current reduction and the gate via the stress applied to it. The use of an IGBT, placed upstream of the DUT, allows polarizing the gate before starting the conduction. The longer the gate bias time, before the DUT is shorted, via the IGBT, the greater the reduction in maximum drain current.

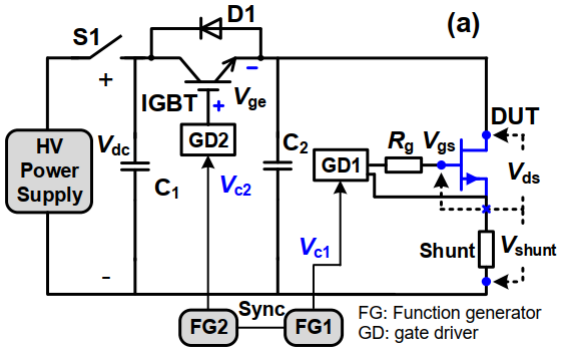

Figure 45: electrical scheme of the used test-bench in [97]

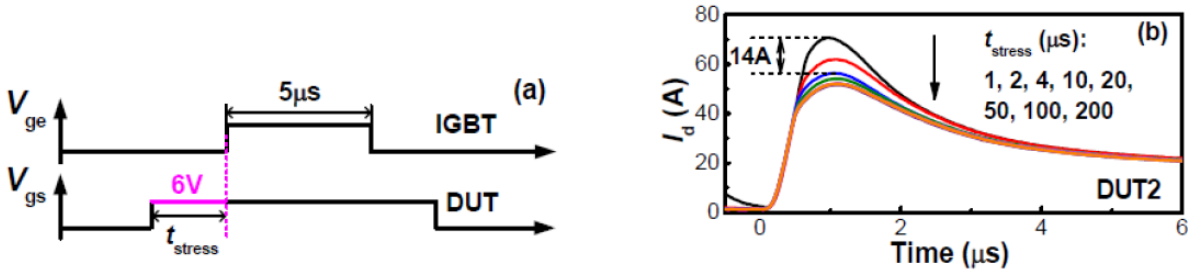

Figure 46: a) Chronograms about IGBT and DUT command, b) augmented drain current reduction under several pre-polarization duration [97]

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1.3.4.4 Specific Behaviour of the Cascode Structure During Short-circuit

Thermal agitation cannot solely explain all, particularly in the case of cascode current reduction due to thermal agitation. The cascode structure remains specific, with a particular behaviour against short-circuit. If another type of GaN component such as cascode is considered, drain current reduction effect is smaller [35]. Fernandez et al in [35] explained that in details by comparing the drain current reduction between cascode components and HEMT p-GaN. The former proved a reduction between 46% et 62% of the maximum drain current value, depending on the active, against more than 80 % for the p-GaN component.
To explain this, Fernandez et al. distinguish 4 distinct behaviour zones during the short-circuit phase, specific to the cascode structure. These four zones are called A, B, C and D.

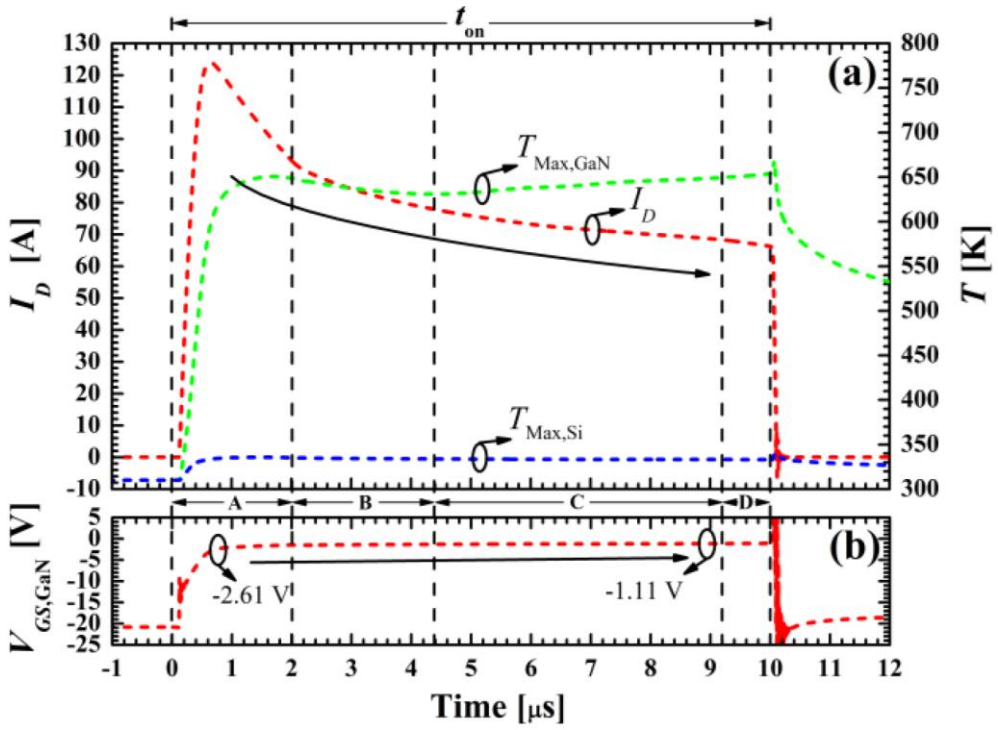

Figure 47: simulated TCAD waveforms during a cascode non-destructive Short-Circuit [35]

During phase A, the drain current and maximum temperature of both GaN and silicon (simulated) increase concomitantly until a maximum value is reached. Once the maximum silicon temperature has been reached, the drain current I_D begins to decrease rapidly thanks to the self-regulating effect in the transistor [35]. It should be noted that at this point, the GaN temperature during the test has not yet reached its maximum value which will be reached at the end of the phase D around 650 K.
During the phase B, the heat continues to diffuse along the AlGaN/GaN heterojunction to the contact metallization. This diffusion to the metal contacts is effective and allows the slope of the temperature to decrease slightly. As a result, the I_D slope is modified. However, this phase B reaches its limits once the metallization of the contacts has been reached, with a re-increase in temperature and the start of phase C.
In phase C, the authors of [35] explain that if the temperature rises again, the slope of the drain current remains the same. They explain this by the internal cascode structure. The control part, provided by the silicon MOSFET, is remote from the power part, provided by the GaN D-MODE HEMT.

Under short-circuit conditions, the Si MOSFET can be electrically reduced to its resistor $R_{DS_ON,Si}$ [116]
In this case, considering the Figure 48 and the fact that the resistance of the package is negligible in comparison to the on-resistances of the GaN HEMT and the Si-MOSFET, the following equation can be written:

$$V_{GS,GaN} = -R_{DS_ON,Si} \times I_D$$

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Hence $V_{GS,GaN}$ and I_D can be linked by the only resistance of the silicon MOSFET.
In addition, the thermal dependence of I_D through the depletion-mode HEMT is proportional to the product $\mu(T) \times (|V_{GS(th)}|-|V_{GS,GaN}|)$ [16], [43], explained by the fact that during short-circuit temperature mainly rises in the d-mode HEMT (Figure 47) and remains low in Si. As a result, $R_{(DS\ ON,Si)}$ remains almost identical. [35,116]. Finally, the authors state that they have verified experimentally that the reduction ($|V_{GS(th)}|$ is thermally less marked than that of $|V_{GS,GaN}|$). The term $|V_{GS,GaN}|$ therefore predominates in the increase of the term $(|V_{GS(th)}|-|V_{GS,GaN}|)$

The reduction of I_D by self-heating then induces a reduction of the term $|V_{GS,GaN}|$ and then increases $(|V_{GS(th)}|-|V_{GS,GaN}|)$ which tends to counteract the decrease in I_D current. For this reason, the cascode shows a less marked ΔI_D reduction than the p-GaN components. The autors of [35] called it "positive feedback"

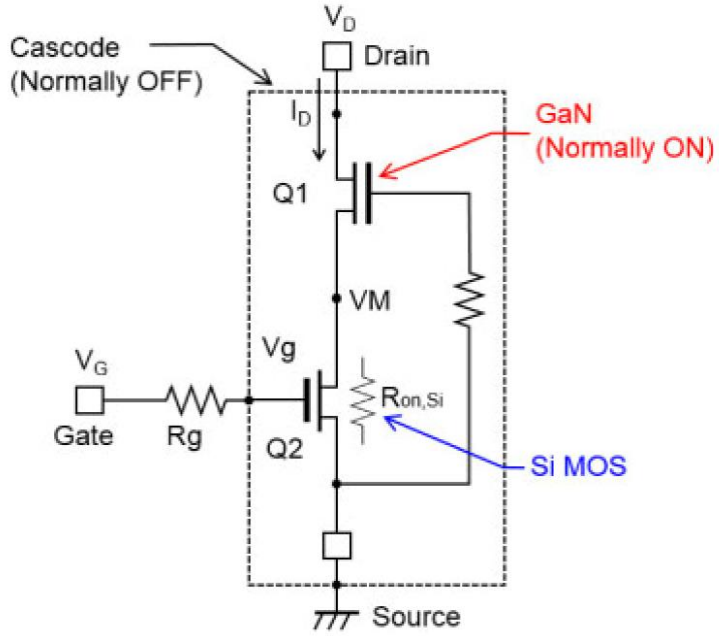

Figure 48: circuit of the GaN d-mode HEMT and Si MOSFET in the cascode structure [81]

With a different structure, $V_{GS,GaN}$ in p-GaN is associated with other equation than cascode one. As a consequence, this "positive feedback" cannot exist what explains why cascode have a lower drain current reduction and hence a lower short-circuit robustness. p-GaN HEMT, with the only thermal self-regulation of the 2DEG channel show a larger drain current reduction and hence a lower power to dissipated what can explain a better robustness to short-circuit [35].

1.3.4.5 Do the Same Mechanisms Occur During the Specific Case of Short-Circuit?

It can be questioned if it is relevant to consider that the drain-current reduction during normal conduction activates the same mechanisms during the specific case of short-circuit? On the contrary of the previous paragraphs, the authors of [105,117] underlined the reduction of drain current can more linked to charge trapping phenomenon. Indeed, in presence of high drain-source polarization, carriers are heated by the ambient electric field and are able to divert from the conduction channel and go to adjacent regions which contain a high concentration of deep traps. The loss of these carriers take part to the current collapse and hence could explain the drain current reduction [117].

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Still in [35], Fernandez et al. explain the circulation of a gate current through a MIS-HEMT, yet counterintuitive due, by definition, to the presence of an insulation below the gate. This circulation would be due to thermal aspect combined with vertical tunnelling effect [105,111]. ("In the MIS-HEMT structure, this gate contact may also be considered a dielectric-assisted Schottky contact, reducing the reverse gate leakage current by approximately four orders of magnitude" from [112])

An interesting thing to note is the behaviour of IGBT during short-circuit. The components are indeed far more mature, their robustness against short-circuit has been widely studied [85,86,93,118–121]. Paula Diaz Reigosa in [119] highlighted the fact that the gate capacitance of IGBTs could, in presence of an electric field, be associated with charge-storage mechanism and de facto a reduced carrier velocity. The phenomenon of time-varying capacitance could also lead to oscillations.

Hot-carrier and trap ionization topics need to be addressed. The authors of [116] indeed wrote "It must be observed that non-optimized GaN transistor design that considers, for example, drift region length and breakdown voltage margin, may lead to severe hot-carrier effects and trap ionization during the short-circuit event, resulting in reduced withstand. Therefore, the first consideration in improving the short-circuit endurance is to design the transistor such that premature breakdown and hot-carrier induced degradation are prevented. As a result, the device endurance becomes thermally limited."

One of the most visible phenomena during a short circuit, namely this reduction of the drain current, remains not clarified today and only accentuates the blur on short circuit phenomena in the HEMT GaN transistors. This opacity will be increased tenfold for the failure phenomena and it will be detailed below. However, this phenomenon is nonetheless important, since drain current reduction means reducing the power to be dissipated in the component and making the component more robust in face of a short-circuit.

The following part address the short-circuit failure mechanisms.

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1.3.5 Several Types of Failure Mechanisms

1.3.5.1 Thermal Failure

For cascode technology, Transphorm components have been mainly studied [35,76,77,82]. In 2016, Fernandez et al. in [35] ran some tests with cascode components, supposed from Transphorm by Mathieu LANDEL in [21]. These commercial devices were in TO-220 packaged and were designed for a maximum voltage of 600 V. These two components differ by their active area, and so the current calibre and $R_{DS\text{-}ON}$ values, 9 A and 290 mΩ for the first component, called $Cascode_{small}$. The other, called $Cascode_{Large}$ has a current calibre of 17 A and a 150 mΩ resistance.

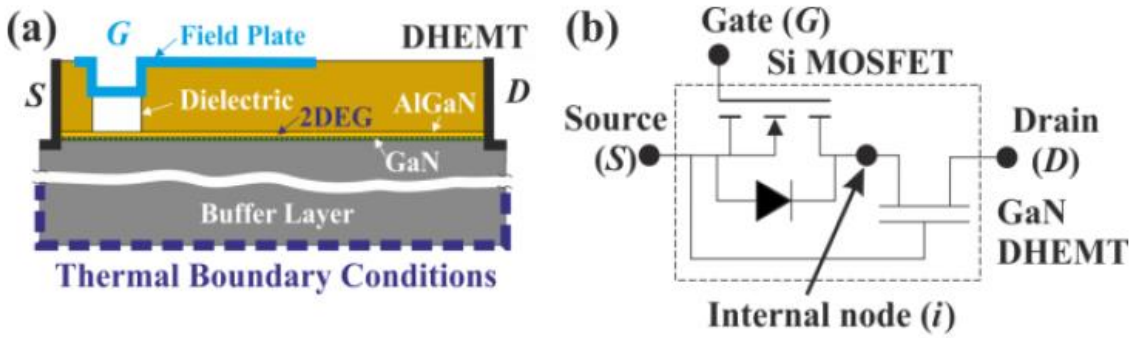

Figure 49: (a) DHEMT Structure and cascode schematic from [35]

Device turn-On and turn-Off are operated with a gate-driver through two separated branches with specific resistance R_{G_ON} and R_{G_OFF}. A 10 mΩ coaxial shunt and differential voltage probes are used to measure drain-source, gate voltage and the gate current. Gate-driver resistances have to particularly be noticed. Indeed, the authors of [35] use high value of resistance, from 50 Ω to even 270 Ω. The authors justify their choices by the fact that low $\frac{dI_D}{dt}$ and low $\frac{dV_{GS}}{dt}$ are required for the short-circuit study to reduce significant overvoltage at switching that may destroy the device. It reduces oscillations due to $L_{\sigma 2}$ and $L_{\sigma 3}$ drawn in the scheme below in Figure 17. They underline the fact that it does not affect the simultaneous high values of I_D and V_{DS} and hence does not change the short-circuit analysis. Moreover, the cascode does not suffer from these high gate resistance values, as it only affects the Si MOSFET which commands the normally-on GaN HEMT. This statement has to be faced to real operational conditions, where gate resistance will not have such value, in order to minimise the switching losses. It will be further discuss with [104].

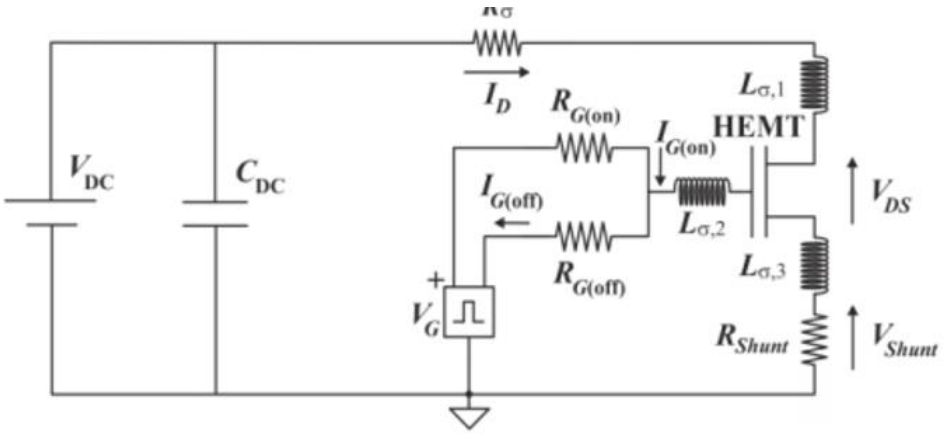

Figure 50: schematic of the SC test board

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In [35] short-circuit tests are performed from 50 V and increase with steps of 50 V until the device destruction. In parallel of destructive test, repetitive short-circuit at the specific voltage are conducted. The delay between two repetitive tests is set to 60 seconds to prevent from self-heating. The results for cascode are presented below.

Under a drain-source voltage of 100 V, the device sustains the short-circuit.

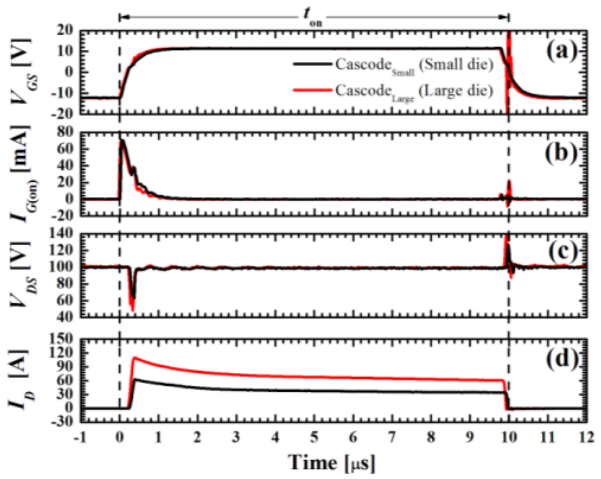

Figure 51: SC non-destructive results for Cascode$_{SMALL}$ (black line) and Cascode$_{LARGE}$ (red line) for V_{DC} = 100 V, V_G = -12 / +12 V, $R_{G(ON)}$ = $R_{G(OFF)}$ = 270 Ω (a) V_{GS}, (b) $I_{G(ON)}$, (c) V_{DS} and (d) I_D from [35]

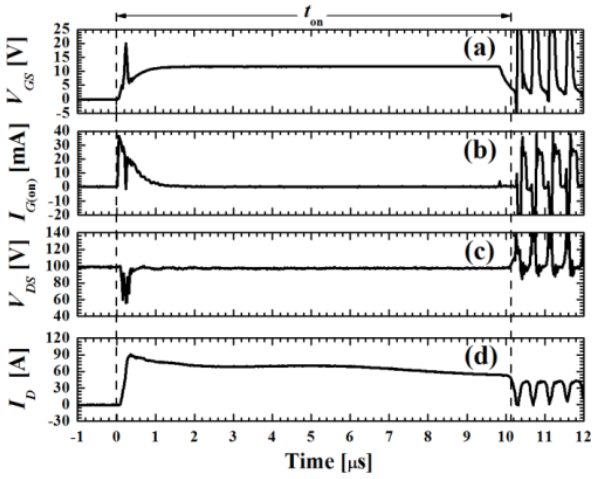

Figure 52: SC non-destructive results for Cascode$_{LARGE}$ (black line) for V_{DC} = 100 V, V_G = 0 / +12 V, $R_{G(ON)}$ = $R_{G(OFF)}$ = 270 Ω (a) V_{GS}, (b) $I_{G(ON)}$, (c) V_{DS} and (d) I_D from [35]

Considering the figures above, the quick rise of $I_{G(ON)}$ is explained by the charge of the gate input capacitance C_{iss} [35,91]. For that reason, increasing the gate resistance value affects and slows down the commutation speed of the component. A similar behaviour is retrieved for p-GaN and MIS-HEMT component with the only difference of a lower $I_{G(on)}$ peak for the former. For cascode and MIS-HEMT component, this gate current comes back to zero or nearly zero once the capacitance is charged.

This phenomena is also retrieved for p-GaN and MIS-HEMT components with the only difference that after the drain current has reached its saturation value, the gate current oscillates between positive and negative values, to finally stabilize at some tens of milliamps for the p-GaN component, depending on the drain-source DC values (Figure 57 & Figure 58). As the components are voltage controlled, the voltage drop induced by the I_G variations generates drain current oscillations.

Unsurprisingly, a higher drain current is observed for the large cascode technology (in red line) than for the small cascode technology on black line. A significant drain current reduction is noticed between both technologies during the short-circuit (ΔI_D of 45.6% and 46 % for the two respective normally-off devices). The slightly bigger reduction for cascode$_{SMALL}$ is explained by a higher dynamic resistance.

Fernandez et al. noticed the turn-off of the cascode$_{LARGE}$ is noisier than the cascode$_{SMALL}$. This phenomenon is exacerbated by a gate command of 0 / +12 V in the upper-right figure while the command was – 12 / +12 V in the upper-left figure.
The cascode sustain the SC test only up to 150 V and 200 V for the respectively Cascode$_{SMALL}$ and Cascode$_{LARGE}$. The better robustness of Cascode$_{LARGE}$ is explained by a larger active are which allows a better power dissipation. In any case the component breaks down far much before the maximum voltage.

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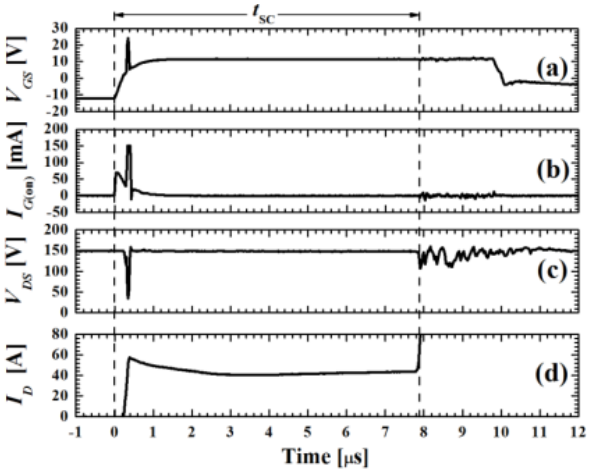

Figure 53: SC destructive results for Cascode SMALL for V_{DC} = 150 V, V_G = -12 / +12 V, $R_{G(ON)}$ = $R_{G(OFF)}$ = 270 Ω (a) V_{GS}, (b) $I_{G(ON)}$, (c) V_{DS} and (d) I_D from [35]

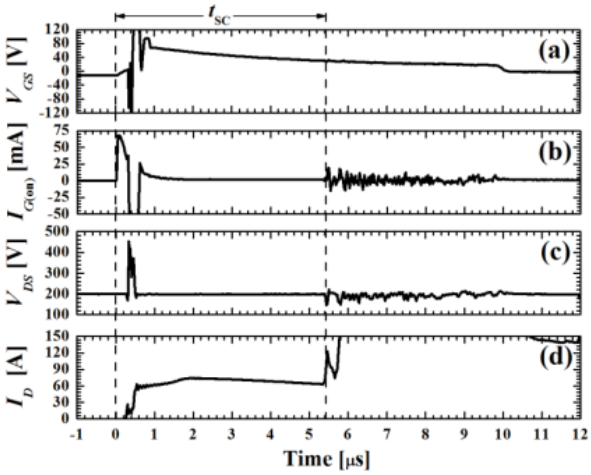

Figure 54: SC destructive results for Cascode LARGE for V_{DC} = 150 V, V_G = -12 / +12 V, $R_{G(ON)}$ = $R_{G(OFF)}$ = 270 Ω, (a) V_{GS}, (b) $I_{G(ON)}$, (c) V_{DS} and (d) I_D from [35]

For p-GaN components the waveforms are quite different with some oscillations of the gate current which induced V_{GS} oscillations and hence drain current oscillations. The drain current decrease is larger than for the cascode case.
The destruction occurs at a voltage of 400 V after 400 ns with similar waveforms at 350 V before the breakage. Fernandez et al. in [35] point out that this behaviour can be understand as the following fact: "When the device has been capable of undergoing the first 2-3 µs in SC, then it will likely pass the test" of 10 µs. It significates that the hardest period for the component is during the rise of drain current. After reaching its saturation value the drain current will decrease due to the thermal increase of the component.

For MIS-HEMT components it is quite the same, with the only major difference that for the non-destructive tests, oscillations are reduced, possibly thanks to the lower packaging parasitic inductances [35]. The breakage occurs at 350 V after 700 ns of conduction.

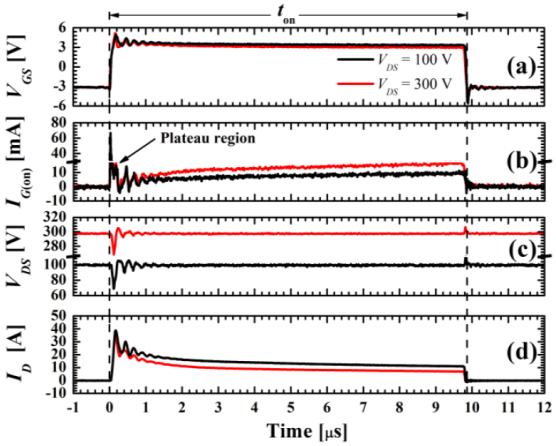

Figure 55: SC non-destructive results for a P-GaN HEMT for V_{DS} = 100 V (black line) and 300 V (red line), $I_{G(ON)}$ = 10 mA, $R_{G(ON)}$ = $R_{G(OFF)}$ = 50 Ω, (a)V_{GS}, (b)$I_{G(ON)}$, (c) V_{DS}, and (d) I_D from [35]

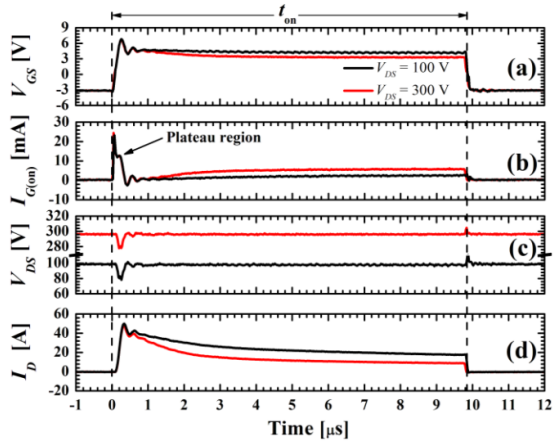

Figure 56: SC non-destructive results for a MIS-HEMT for V_{DS} = 100 V (black line) and 300 V (red line),V_{GS} = -3 / +5 V, $R_{G(ON)}$ = $R_{G(OFF)}$ = 270 Ω. (a)V_{GS}, (b)$I_{G(ON)}$, (c) V_{DS}, and (d) I_D from [35]

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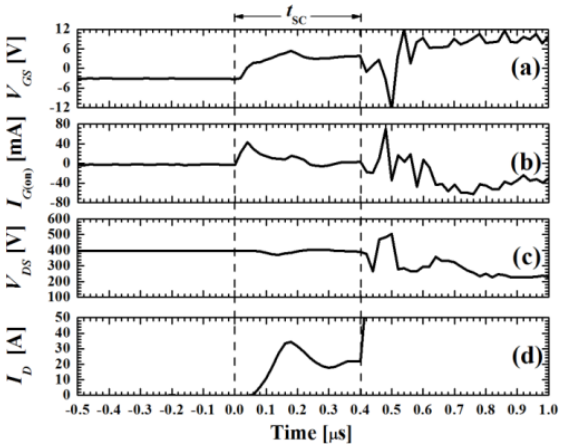

Figure 57: SC destructive results for a P-GaN HEMT for V_{DS} = 400 V, $I_{G(ON)}$ = 10 mA, $R_{G(ON)}$ = $R_{G(OFF)}$ = 50 Ω. (a) V_{GS}, (b) $I_{G(ON)}$, (c) V_{DS}, and (d) I_D

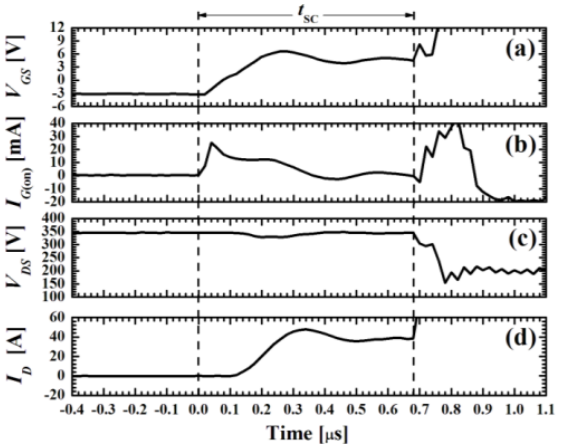

Figure 58: SC destructive results for a MIS HEMT for V_{DS} = 350 V, V_{GS} = -3 / +5 V, $R_{G(ON)}$ = $R_{G(OFF)}$ = 270 Ω. (a) V_{GS}, (b) $I_{G(ON)}$, (c) V_{DS}, and (d) I_D

From Fig. 52-53 and Fig. 56-57, it is clear that P-GaN and MIS-HEMT break down at higher DC values than cascode.

Moreover, failure occurs differently for cascode and E-HEMT components. Indeed, during the tests with the highest possible drain-source polarization (150 – 200 V for cascode, depending the small or large package), cascode break down after few microseconds (7 µs in the study). Test at 100 V and 150 V (depending on the package) were successfully conducted for during 10 µs. On the contrary if E-HEMT components (p-GaN / MISHEMT) passed the test at 350 V / 300 V, these components broke suddenly down at respectively 400 V / 350 V after only hundreds of nanoseconds of conduction. This difference of breakage let the authors of [35] to link the breakage of E-HEMT component to local effect. The author supposed the gate and field plate region, where the main adjustments have been made in comparison to cascode technology, to be the place where the failure occurs. This reasoning let them to a electro-thermal effect failure where a too high temperature lets the component becoming intrinsic. Up to a certain drain-source polarization, the component achieves to sustain the short-circuit and the developed temperature by the mechanism of electrothermal regulation but when voltage is too high, the component suddenly breaks. However, the authors of [35] mentioned that some other unknown failure mechanisms may have preceded the breakage

In parallel of this failure explanation, the authors explain the failure of cascode component as a thermal runaway.

These two different types of breakage, with long time to failure (several microseconds) versus short time to failure (hundreds of nanoseconds) can be observed in the Figure 59. For the cascode components, the critical energy, when the component breaks down, is close to the expected value. The slight lower value than expected could be explained by the fact that the component break before the end of conduction ($T_{FAILURE} < t_{ON}$). It is not the same for E-HEMT component with a highly reduced critical energy compared in comparison to slower V_{DS} tests.

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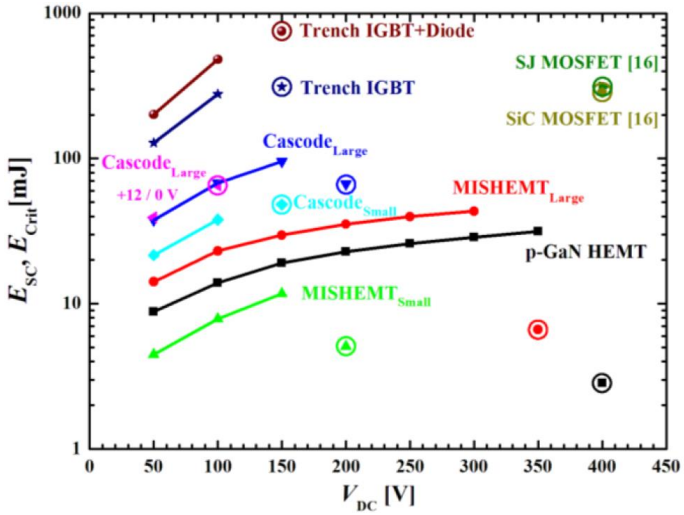

Figure 59: Dissipated and critical energies comparison for cascode components pink and blue) versus E-HEMT (red, black, green) from [35]

In line with this, the better robustness of E-HEMT exists thanks to better drain current reduction but it would be locally limited after a certain drain-source voltage level.

This study may nevertheless be questioned in the light of [104] where it has been demonstrated that higher gate resistance improve the SC robustness of p-GaN components. Indeed, in the case of p-GaN components, Riccio et al. highlighted with Figure 60 the fact that increasing the gate resistance value tends to decrease the gate current. For R_G=46 Ω, the device exhibits a gate current up to 9 mA (V_{TEST}=260 V), while for R_G=250 Ω the gate current reaches 6mA at the end of the SC pulse (V_{TEST}=300 V). This high gate current causes a significant voltage drop across the gate resistance with consequent reduction of the effective V_{GS} applied to the device. As a result, the drain current decreases. This lower drain current therefore reduces heating and de facto improves the short circuit performance of the component.

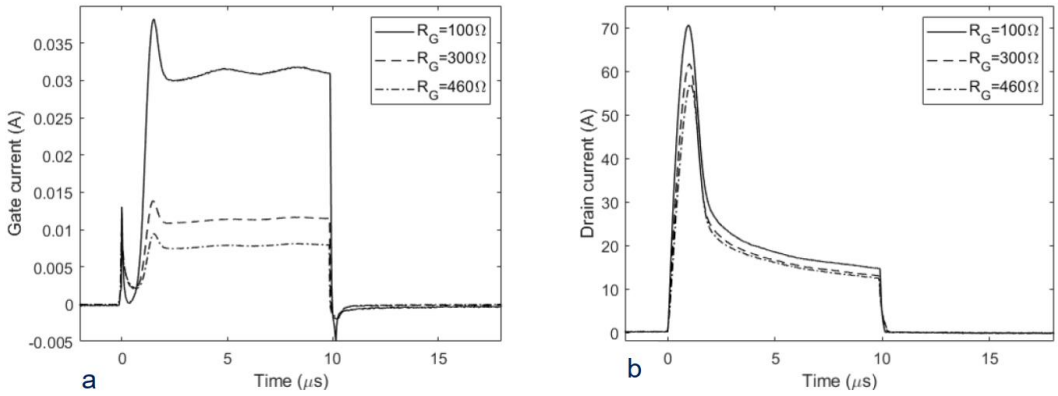

Figure 60: gate current (a) and drain current (b) waveforms during short-circuit for several values of gate resistance from [104]

Moreover letting occur theses oscillations can precisely cause failure, as it is demonstrated in [77]. These high-value oscillations of V_{GS} can result as an uncontrollable rise of drain current and causes the MOSFET failure [77]. These causes of failure are further explained.

The rise of I_G during the short-circuit for the p-GaN and MIS-HEMT is considered as a indicator of thermal failure by Fernandez et al. But the very rapid failure for p-GaN and MIS-HEMT introduces the fact that not only heating can be held responsible of failure.

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Moreover, instead of being a precursor or an indicator, I_G rise can be seen as one of factors at the origin of destruction. High leakage current at high temperature, associated with a channel threshold reduction can act in concert and lead to a thermal runaway [116]. With thermal overheating, thermomechanical stress can appear and result in a failure in the region of intermetal dielectric around the drain region [116].This assertion is reinforced by [103] where several tests at high temperature (475 K) have been made. Components sustain short-circuit during 225 µs, under 480 V and so demonstrated a better robustness. (also the case with [100], longer TLF with a temperature of 150 °C compared to room temperature, 35 µs versus 315 ns under 380 V and 160 ns under 500 V).
So, by reducing the conduction and the drain current peak during short-circuit, temperature cannot solely be considered as a failure catalyser as it was demonstrated in [7], but it is also an improvement factor of robustness.

Furthermore, in the case of p-GaN, the simulation results in [35] indicate a strong field under the gate during the breakage with short TLF and high V_{DS}. It reached its maximum at t = 200 ns. This statement is reinforced by the fact that the maximum temperature is not reached before the failure (800 ns for V_{DS} = 350 V while failure occurs at t = 400 ns for a V_{DS} = 400V).

For the case of depletion mode GaN HEMT, with, nevertheless, the non-negligible specificity of a SiC substrate and a TO-220 package, the authors of [80] also rejected thermal aspect as the main cause of failure. According to them, the temperature of the component did not exceed 150 °C at the time of failure, for both long TLF (10 µs / V_{DS} =250 V) and short TLF (0.5 µs / V_{DS} = 400 V). They also introduced the idea of charge-field phenomena with the generation of holes from impact ionization during the short-circuit. According to them this so-called premature breakdown near the gate needs therefore to be more detailed. The authors of [21,116] reinforced this idea of a premature breakdown induced by impact ionization, with the generation of new pairs of electron-holes after carriers colliding into atoms of transistor material [122,123] rather than simply thermal failure.

1.3.5.2 Failure due to Charge-Field Interaction Phenomena

In the case of [35] if Fernandez et al. were able to conduct non-destructive test at 350 V during 10 µs with p-GaN components, they faced to a very low time to failure for a slightly higher drain-source polarization (0.4 µs times under 400 V).
The authors of [92] obtained similar results, went deeper and dissociated these two types of failure (short-time failure vs long-time failure). The studied components in [92] are produced by GaN Systems, with the technology of recessed gate, with a R_{DS-ON} of 200 mΩ and a threshold voltage V_{th} of 1.53 V. The tests are performed for V_{DS} = 300 V and V_{GS} = 5V. The breakage occurs after a significant duration of conduction (308 µs), with an energy of 220 mJ. As it is commonly known the energy dissipated, and so the thermal aspect, come into play and the component dies as a result of thermal runaway. On the other hand, at 350 V, so only 50 V above the previous ones associated with a duration of conduction highly reduced due to the rapid breakage (about 700 ns), the energy, with only involved 5.3 mJ, cannot be identified as the only source of failure. As thermal aspect and energy are linked, the thermal behaviour of the device cannot solely explain the breakage.

Abatte et al. in [92] thus advance rather than the thermal aspect the idea of a trapping mechanism coupled to the electric field. In presence of voltage polarization, carriers circulate at their saturation velocity. Due to the presence of a strong electric field during the short-circuit, carriers move and thus generate a current. The generated current induces the formation of a space charge, making the electric field with the risk to finally become larger than the breakdown electric field.

The authors of [92] underline that this phenomenon of excessing the breakdown electric field is retrieved as a failure cause in other power semiconductors like diode [124] and IGBT (Insulated Gate Bipolar Transistor) [125].

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The authors of [80] confirm also the possibility of hole trap mechanism. In simulation they indeed find an important generation of holes produced by impact ionization due to hot electrons [91] circulating during the short-circuit.
These electrons, circulating in the 2DEG channel, are "heated" by the electric field and create by impact ionization many holes near the channel but also in the surrounding areas like beneath the gate.
Due to the valence band barrier of AlGaN/GaN, these holes stay in this "drift region" and start to accumulate.
The authors of [126,127] strengthened this idea of an induced gate premature breakdown due to hole generation beneath the gate region.

According to [71], [114], [116], [117], two types of failure mechanisms can be emphasized.

First, a too high electric field can be held responsible.
In depletion region like beneath the gate, positively charges holes are like N-type doping ions according to Equation 2
According to Equation 1, this accumulation of newly created holes in depletion region can enhance the positive space charge under the gate [71], [114] and influence the shape of the electric field as it is explained by the equation. The electric field will hence locally exceed the limit of the component, provoke a premature breakdown close to the gate and the breakage of the HEMT [71].
This statement is reinforced by the fact that robustness is limited to a certain voltage. At low voltage, the electric field would not be sufficient and few holes are generated but for higher drain-source polarization and so the high electric field, holes can circulate at their saturation velocity [124] and be damageable, leading to a too high and critical electric field, leading to a premature breakdown.

$$\frac{dE_x}{dx} + \frac{dE_y}{dy} = \frac{\rho}{\varepsilon}$$

Equation 1: Poisson equation linking electric filed and charge distribution with E the electric field, ρ the volume charge density and ε the permittivity

$$N_{eff} \approx N_D + \frac{J_p}{q * v_{psat}} - \frac{J_n}{q * v_{nsat}}$$

Equation 2: Relation between positive space charge Neff in the depleted region and N-doping (N_D), hole and electron current densities J_p and J_n, holes and electron saturation velocities V_{psat} and V_{nsat} from[124]

The Figure 61 illustrates this accumulation of holes below the gate which accentuates the field below it, resulting in an electrical breakdown.

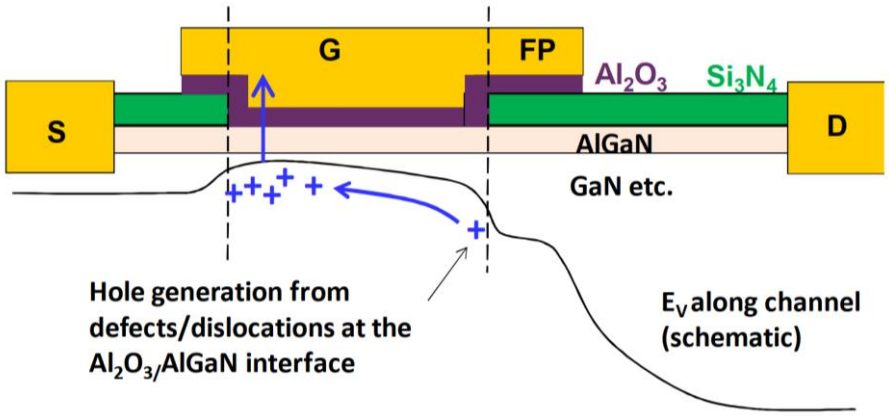

Figure 61: HEMT cross-section related to band diagram to illustrate the hole generation from [126]

Secondly a wearout of the gate after the turn-off is explained by some articles.

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The authors of [9] point out that the diffusion of stored holes after the turn-off could have an impact. The authors of [126] explain such gate wearout by the fact that the newly created holes will leak through the oxide of the gate, particularly when the device is turned-off, as the gate is negatively polarised. The formed path by holes allows then the circulation of electrons from the gate to the drain region. The Figure 62 illustrates in red the accumulation of holes beneath the gate with OBIRCH (Optical Beam Induced Resistance Change) technique.

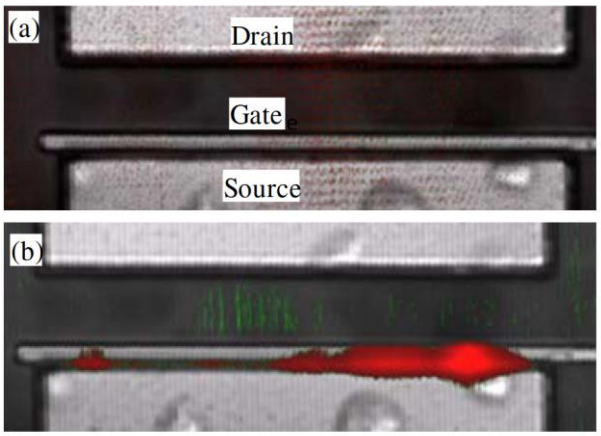

Figure 62: OBIRCH image of a fresh (a) and degraded (b) device. The red colour shows the degradation and the accumulation of holes beneath the gate from [126]

This explains the breakage as drain-gate breakage, reinforced by [91], still with the idea of a failure caused by the activation of traps, which locate the failure with a concentration of such traps on the edge of the component drain. The authors of [126] recommend hence to use thicker oxides. They mentioned that devices using silicon nitride Si_3N_4 as a gate dielectric show a far better robustness against AlGaN layer relaxation [128], inverse piezoelectric degradation [129] and an higher breakdown voltage.
[126] linked also the phenomenon with a threshold voltage shift and explicit the damages of the gate as discrete spots.

If Fernandez et al. in [35] stated that the failure is mainly related to electro-thermal effect, they pointed out also that oscillations has to be oversee. It is explained in [35] that even if the component sustains the short-circuit stress, a too excessive gate ringing could after all destroy it or the converter. In that way, it is mentioned that reducing loop inductance could improve the SC robustness

1.3.5.3 Failure due to Oscillations

In parallel with the failure mechanisms, the authors of [92] noted significant oscillations may appear on gate and drain during the short circuit. These oscillations, by creating unwanted electromagnetic interferences can lead to the breakage of the component ([93,118]). They noted that these oscillations are very similar to those occurring in short circuit IGBTs [93].
Their experimental conclusion was that oscillations are maintained due to the presence of a capacitive behaviour of the TVS diode (Transient Voltage Suppressor). These high-frequency oscillations disappear if the TVS diode is removed from the assembly or if ferrite is applied to the TVS diode. The authors conclude that these oscillations do not appear to originate from a component intrinsic mechanism such as a trapping phenomenon as it is the case for short TLF failures seen above. They conclude by saying that these oscillations are intimately linked to the presence of a capacitive driver output, something that is not very good since drivers are mostly inductive output.

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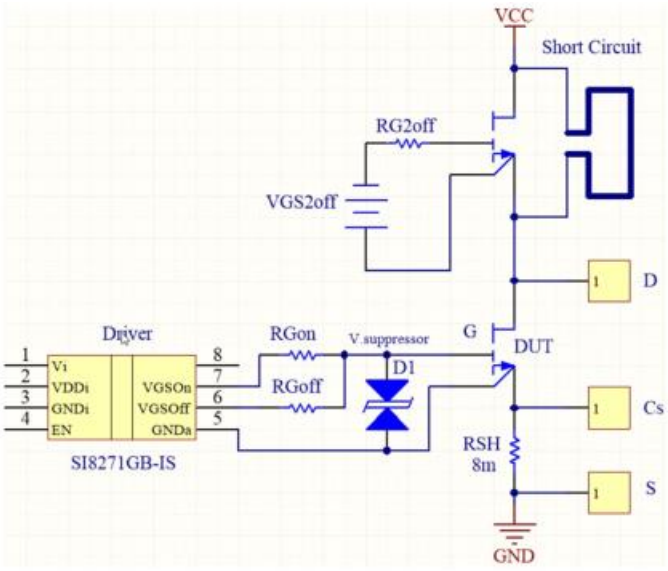

Figure 63: electrical scheme of the test-bench with the TVS diode from [92]

However, the authors of [93] noted several interesting things: the oscillations appear when the device input impedance Z_{in} (plus load circuit and parasitic element) is equal to the driver output impedance Z_{dr}. Another condition for sustained oscillation and the real part of the DUT input impedance is negative. They linked their bench with a series resonance circuit and determine the parameters of impedance which provoke oscillations

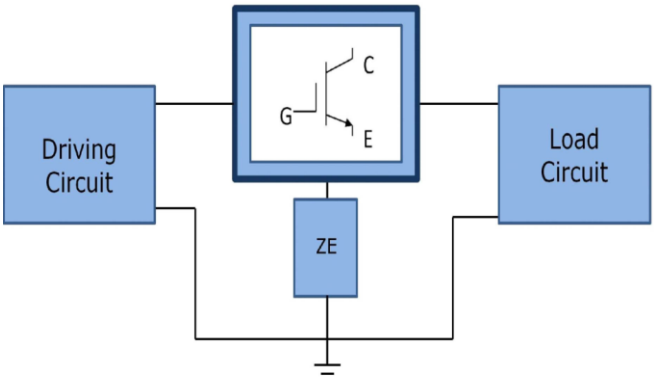

Figure 64: diagram of the real circuit with the driver, load and parasitic elements from [93]

For low-frequency instabilities (f=30 kHz), the authors linked sustained oscillations and circulating current due to injected holes from the anode/collector, creating a positive charge accumulation under the gate, resulting in the creation of a negative capacitance at the input of the IGBT. For high-frequency instabilities (f = 40 MHz), such a negative capacitance was related to the Miller capacitance of the device [130] and results in instability of the device. The authors calculated input impedance of the device. With simulation, they put on graph combinations of gate resistance R_G and gate inductance L_G for which the device suffers from HF oscillations or not. Right side of the line, the device is stable, left side of the line, undamped oscillations are present.

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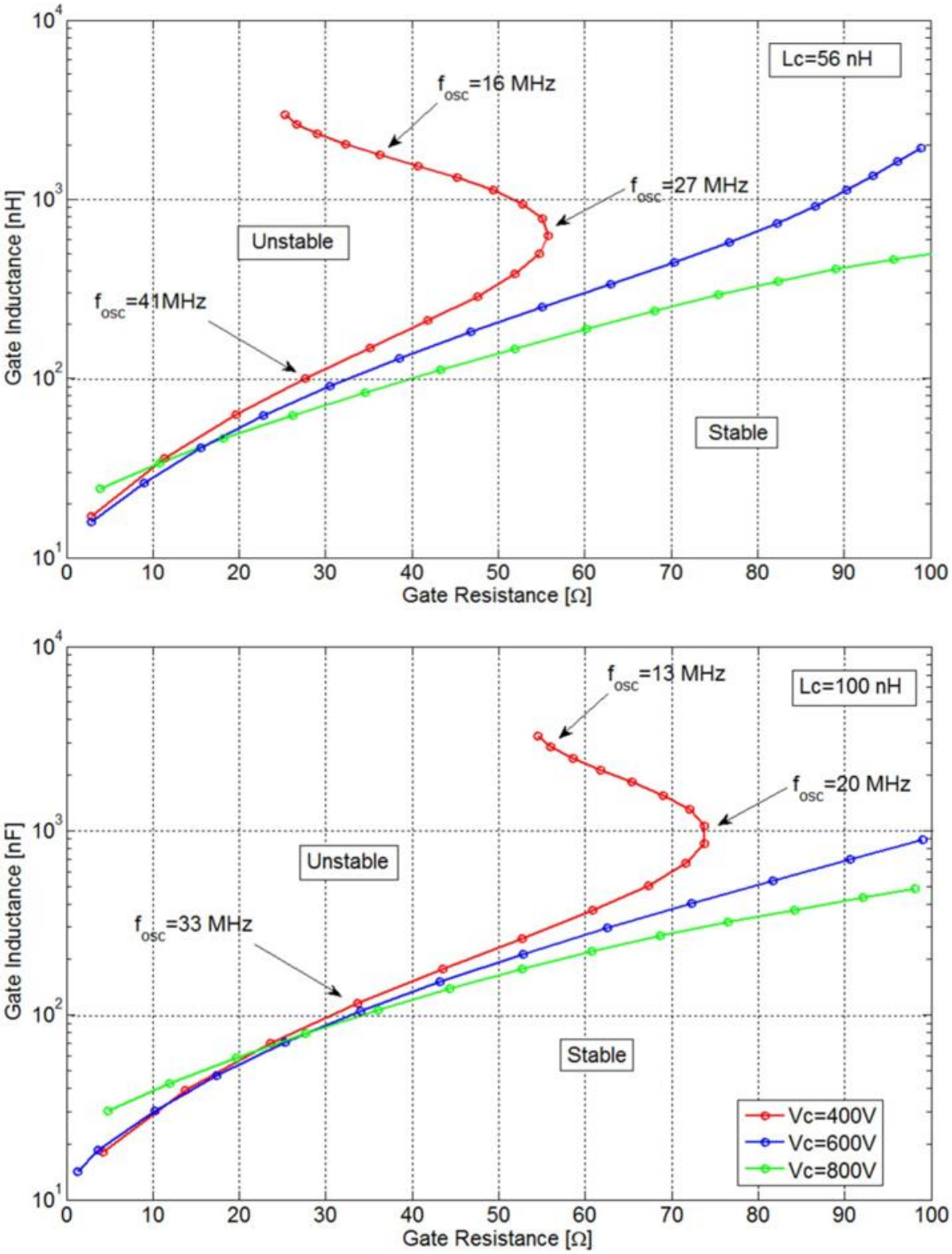

Figure 65: Stability map obtained by simulation and for V_{GE} = 10 V, V_{CE} = 400, 600 and 800 V and two stray inductances LC. The oscillation frequency is reported for some points. From [93]

The authors were able to exhibit such high-frequency variation in experiment.

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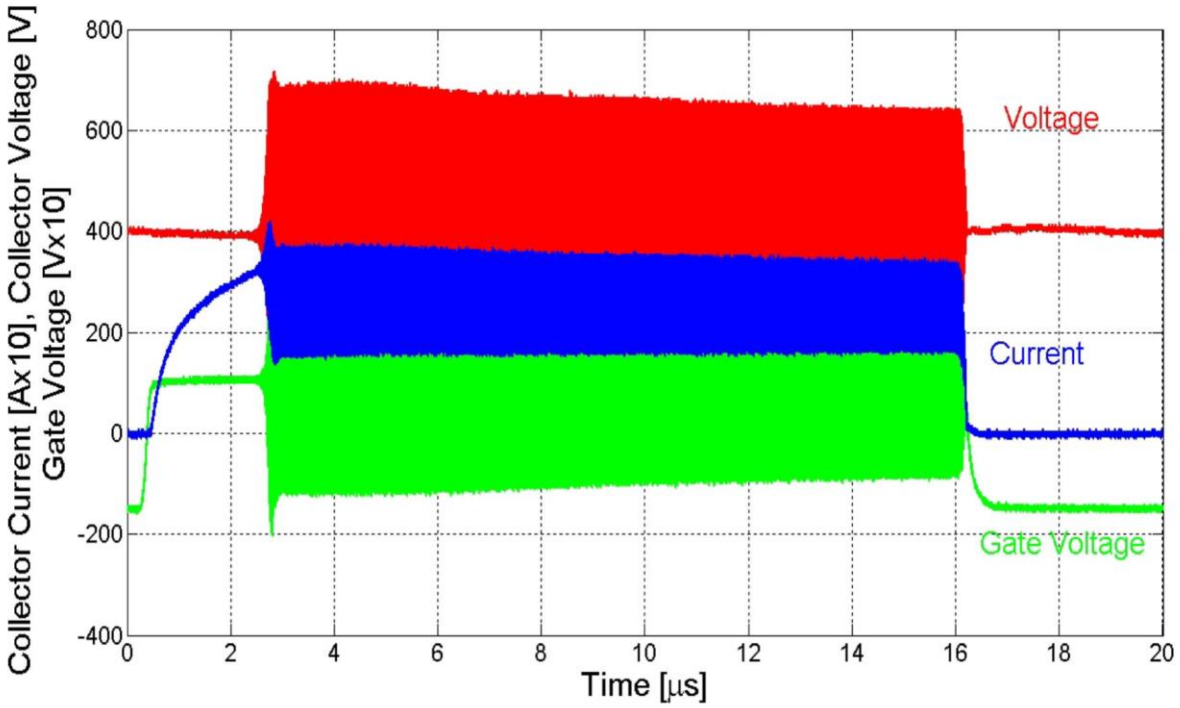

Figure 66: Measured waveforms during SC at Vge = 10 V ce = 400 V, Lg = 27 nH, Lc = 56 nH, and Rg = 10 V, from [93]

On the contrary to low-frequency oscillations, in the case of high frequency, increasing R_G from 10 Ω to 50 Ω improves the stability and reduces the oscillation (not shown in the paper).

If the problem of oscillations has been raised by [92], the authors of [77] interested of these oscillations as consequence of the component structure
This article focuses on cascode technology and shows different effects of short-circuit. Two places of failure are presented.
The origin of these oscillations is directly linked to the cascode structure and come from stray inductance of bonding wire and internal stray capacitance [50,131]. In normal operating conditions the LC tank provide only switching transients which are damped but during specific conductions like short-circuit no damping or to low damping effect from the gate resistance exist and theses oscillations become self-sustained which can lead to excess electromagnetic interference, or even worse, to a catastrophic failure.

Xue et al. from [77] shed light on two failure modes induced by SC oscillations and reveal the main cause with the help of simulation.
According to them, two phenomena exist, one from the D-HEMT process and one other from the cascode structure, in other words the link between DHEMT and Si-MOSFET. These two effects reinforce each other.

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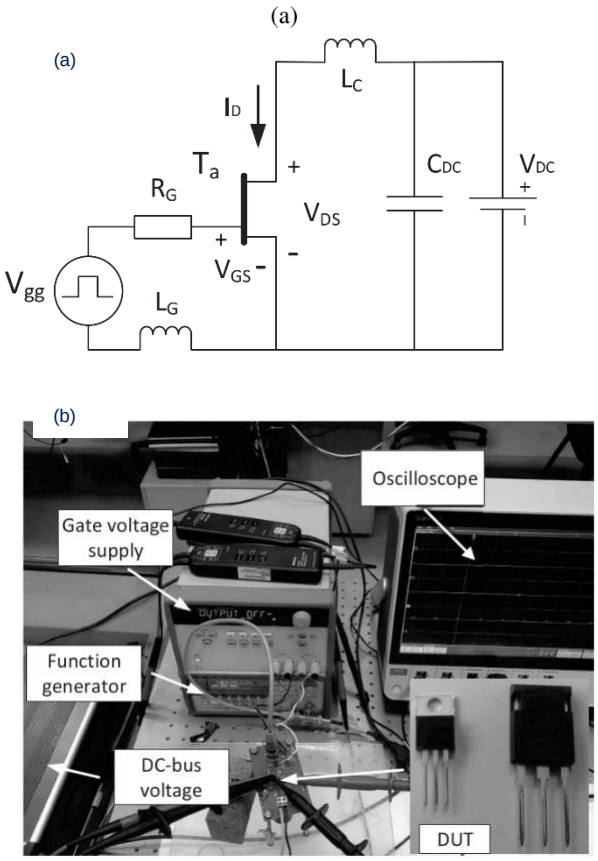

Figure 67: Short-circuit test schematic (a) and platform (b) from [77]

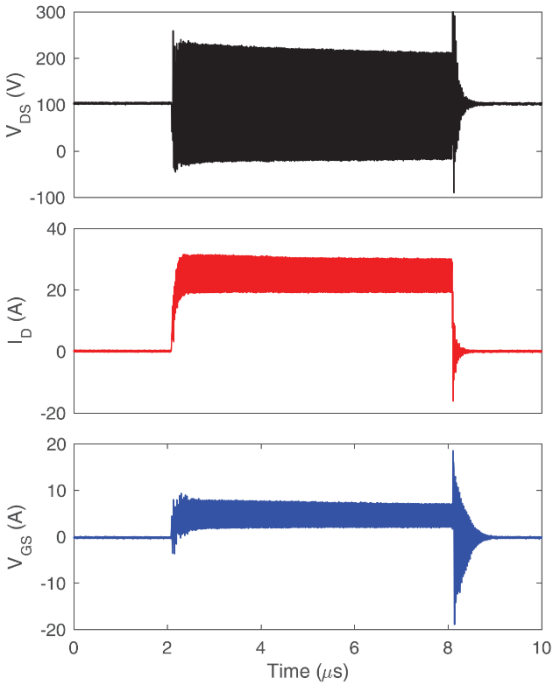

Figure 68: Short-circuit Waveforms for studied cascode from [77]

The figure above from [77] shows why the undamped oscillations can be related to short-circuit. At the turn-off, so after the period of short-circuit conduction, the oscillations attenuate rapidly, contrary to the on-period.

As seen above with [92], the authors of [77] underlines the fact that IGBT has similar current and voltage oscillations as seen in Figure 69 but according also to them, these two types of devices can not be linked for the following reasons: as similar the oscillations of these two components as they are, IGBT does not have a cascode structure and the oscillatory behaviour has been directly related to the structure according to [50,131]. Moreover, oscillation of IGBT have been mainly explained by the presence of the dynamic avalanche [77,119,120] what cannot be related to GaN HEMT components due to their unipolar nature.

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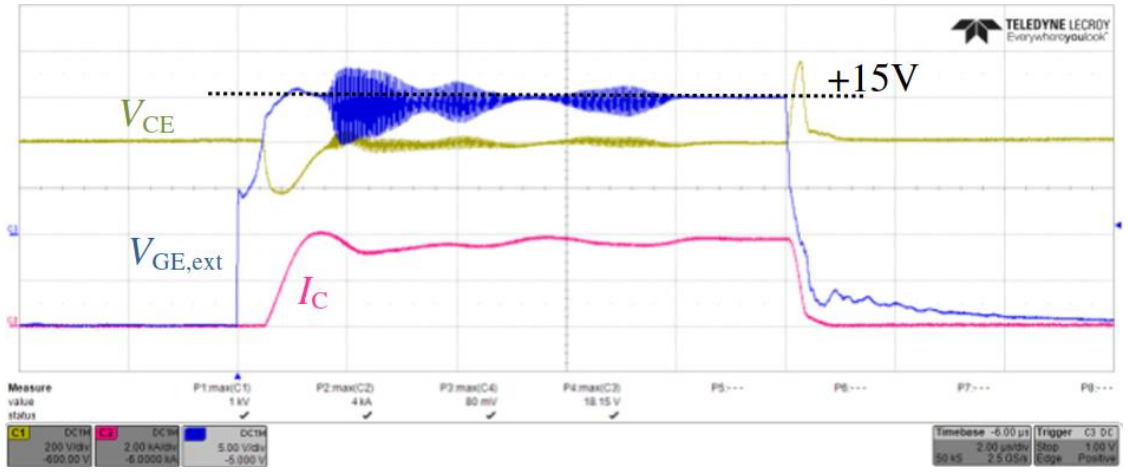

Figure 69: Gate oscillations during 800 V/10 µs short circuit of the 1.7 kV/1 kA IGBT from [132]

The authors [77] state that gate resistance R_G has no influence on short-circuit oscillation, on contrary to IGBT where it has demonstrated that gate resistance has a significant damping effect. This assertion may be reconsidered as the comparison has only been made for two values of gate resistance, 16 Ω and 80 Ω.
Moreover it has been demonstrated in [95] that R_G has a very strong damping effect in case of p-GaN component with a total suppression of oscillations for a sufficiently high value of R_G (8 Ω in the case of the study). This article also underlines the link between short-circuit oscillation and gate loop resonance.

It has to be noticed that the test-bench, reported in Figure 67, appears quite simple with a power capacitor Cdc = 390 µF. A pulse signal generated by a computer is sent to the driver which commands the gate. The two tested components, with threshold voltage of 2.1 V (cascode A) and 4 V (cascode B) were commanded by a gate function which alternated between 0 V/4.5 V for the first and 0 V/6.5 V for the second. The gate resistance value is set to 16 Ω. Nevertheless, significant high frequency oscillations appeared, more or less pronounced following the drain-source polarization.

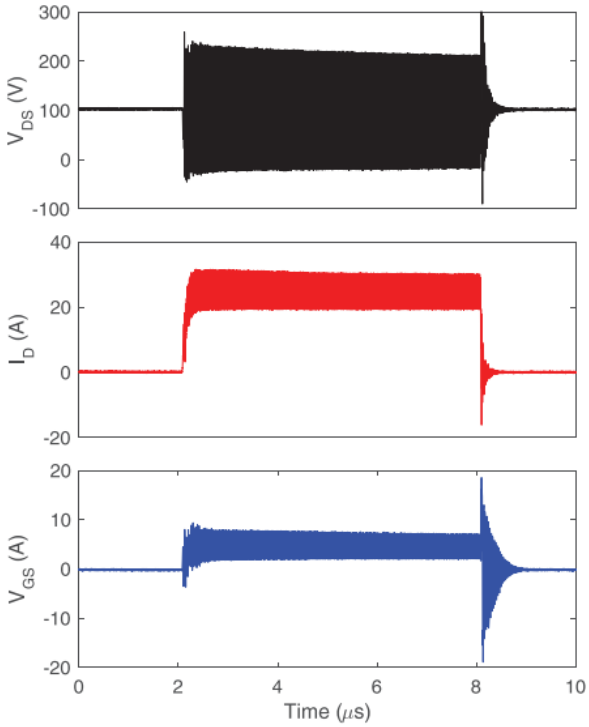

Figure 70: Short-circuit waveforms for Cascode A and Vds = 100 V and RG = 16 Ω from [77]

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Xue et al. in [77] distinguish two sources and places of oscillations:

First place, the D-HEMT: The D-HEMT is destroyed due to V_{DS} oscillations which exceed breakdown voltage. Xue et al. explain the failure by the fact that, despite a limited drain-source voltage, the oscillations reach such high-level value, more than 650 V and it overcome the breakdown voltage as shown in Figure 71. Coupled with a significant current, it leads to a too high-power dissipation, resulting in a thermal runaway. The authors identified the thermal runaway as the origin of failure thanks to the post-failure inspection of the component. It revealed large melted areas in the D-HEMT part of the whole cascode component, synonym of too high heating up. Associated with a rapid decrease of V_{DS}, as a sign of the establishment of a conductive way between drain and source, a too much power dissipation is announced by the authors as a possible origin of the failure. In fact, the D-HEMT mainly bears the voltage as the Si-MOSFET is only linked to the command. The conclusion of thermal runaway may anyway be questioned and the failure may be more related to the overcome of the breakdown voltage.

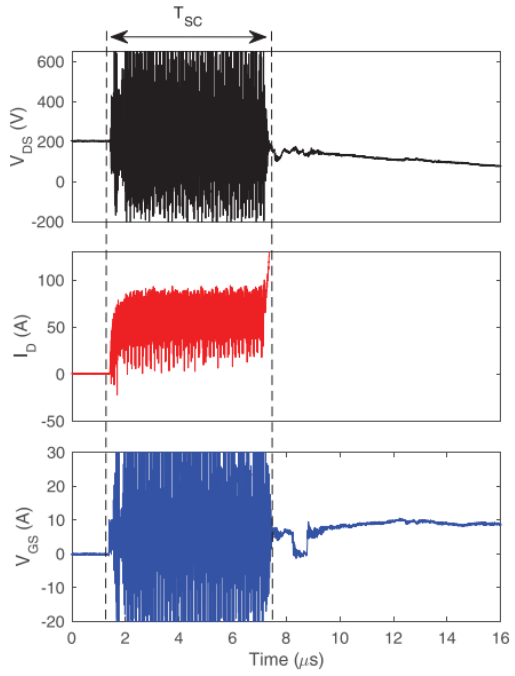

Figure 71: short-circuit failure waveforms for cascode B with V_{DS} = 200 V and Rg = 16 Ω from [77]

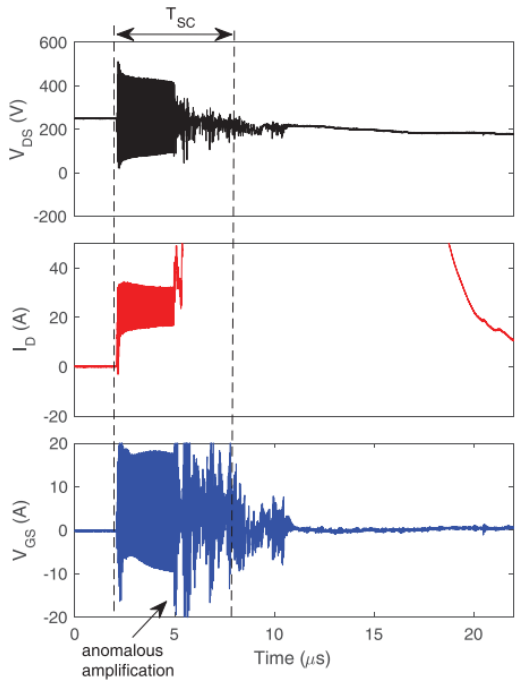

Figure 72: short-circuit failure waveforms for cascode A with V_{DS} = 250 V and Rg = 16 Ω from [77]

These oscillations come from the depletion-mode HEMT process and the wires between the Si-MOSFET and D-mode HEMT.

The authors of [77] mentioned another mode of failure, called Failure mode II in their article, represented here by the Figure 72. In this second mode, instead of a high overvoltage like in the failure seen earlier, the peak voltage on V_{DS} remains acceptable and lower than the breakdown voltage. The cause of the failure is now more at the gate level with significant oscillations of high amplitude, after only 3 µs, when the other type of breakage arrives after 7 µs of conduction. In response to this, the drain current reaches extremely high values, then provoking the component failure. Despite the fact that the oscillations were also significant in the case of the cascode B component, in this case, the authors specify that the oscillations of the V_{GS} signal seem out of control. In addition, the V_{DS} signal remains stable at a non-zero value and the component opening reveals the explosion of the Si-MOSFET. Using LTSPICE simulations, the authors conclude that the component breakage is due to too large oscillations in the V_{GS_MOSFET} signal, generating a high-power output to dissipate. This conclusion differs from the failure mechanisms associated with thermal runaway due to the existence of too high-value V_{DS}

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oscillations. In the first paragraph, the signals were relatively continuous, causing a high power to dissipate. Considering the oscillations are identified as the cause of failure, rather than thermal runaway, would it not be a dielectric break ?

The authors of [35], with the article seen above, mentioned also the gate ringing effect as a possible source of failure for cascode components. The main difference with [77] lies in the fact that in the present case the oscillations occur only at the turn-off. This makes the design of the test circuit and the reduction of interference inductances all the more sensitive. The authors of [35] considered the inductance of the package $L_{\sigma 3}$ case, between gate and source, as the source of these oscillations and thus also possibly the interaction between MOSFET and D-HEMT of the cascode.

It can be supposed the behaviour of depletion mode HEMT would differ from enhancement mode HEMT. To strengthen that, [96] has proven that adding a silicon MOSFET in series with cascode HEMT will improve its robustness. Cascode itself having already a Si-MOSFET in series, it reinforces the idea that, d-mode HEMT robustness, without any silicon MOSFET attached to it, will be far different. It hence strengthens the interest to study this type of component under short-circuit conditions.

1.4 Conclusion

The first chapter begins by highlighting the pivotal moment that power electronics is currently experiencing. After several decades of advancements in the reliability and optimization of silicon-based power devices, new technologies are emerging to address evolving global demands. These include energy conservation on a worldwide scale and increased electrification, particularly driven by the rise of electric vehicles, renewable energy sources, and significant transformations in energy distribution and electrical grid systems.

Obviously, Rome wasn't built in a day. This suggests that, despite their immense promise, wide bandgap power transistors—specifically GaN components in this thesis—are not without challenges, particularly regarding reliability and robustness. After conducting an in-depth analysis of the operation of GaN HEMTs, including the formation of the two-dimensional electron gas (2DEG) and various normally-off structures, the focus shifted to a critical evaluation of the current state of the art concerning short-circuit performance.

Several failure mechanisms have been extensively discussed. While thermal runaway initially appears to be the most obvious explanation, other physical mechanisms challenge this hypothesis, particularly in cases of a reduced failure energy. Charge-field interaction phenomena have been thoroughly analysed, as they can significantly impact the device behaviour and lead to a device failure. Additionally, impact ionization phenomena, associated with hot electrons and hole generation, must be taken into account, offering a potential explanation for component failure beyond thermal effects. A third proposed cause of failure involves potentially destructive oscillations. Potentially related to driver components, the literature has associated the concept of negative capacitance with Miller capacitance and component instability. Additional explanations for the occurrence of these short-circuit oscillations have been proposed, notably LC parasitic elements originating directly from the packaging of the cascode component and linked to the Si MOSFET driving the GaN HEMT. These oscillations can manifest in various scenarios, either during conduction or at the component's turn-off. Furthermore, oscillations affecting the V_{DS} signal, by exceeding the breakdown voltage threshold, can lead to component failure.
Particular attention must therefore be given to ringing phenomena and potentially destructive oscillations. The design strategy for the test bench will take these impacts into careful consideration.

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2

Development and Optimisation of the Experimental Short-Circuit Test Bench

An innovative approach was decided upon and described in Chapter 2. The literature currently relies on destructive testing, with the major drawback that chips are difficult to analyse once they are destroyed and even more considering the colossal power to be dissipated during short-circuiting. To counter this, it was decided to work on repetitive, non-destructive tests. The literature is inexistent about the analysis of normally-on components. They are studied in this thesis in addition to normally-off p-GaN components from two separate suppliers. Between each series of short circuits, the component is characterised using a B1505A characteristic tracer and the evolution of the transistor static parameters such as the threshold voltage V_{th} or the on-state resistance R_{DS_ON} are analysed.
The impressive switching speed of GaN components means that the slightest parasitic effect is exacerbated. Several phases of optimisation of the experimental short-circuit bench were therefore carried out, and are described in Chapter 2. In parallel with this, a SPICE simulation was developed in order to gain a better understanding of the operation of the experimental bench. These analyses led to various improvements and versions of the short-circuit test bench, summarised briefly in Table 1 and detailed in Chapter 2.

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2.1 Strategy and Design of the Test Bench

2.1.1 Overall Strategy

As it was mentioned in Chapter 1, short-circuit type I are the most-occurring short-circuit [34,78] and are therefore studied in research. This thesis will hence focus on short-circuit type I.

The current literature has mainly focused on the study of destructive short-circuits, with the major drawback of not being able to study the component once it has been destroyed. The strategy of this thesis does not focus on destructive tests but on non-destructive repetitive tests. The aim is to visualise any device drifts by means of static characterisations carried out before and after the series of short-circuits. These drifts are referred to as static. Particular attention will also be paid to any dynamic variations in the component as the various short-circuits are carried out. Static R_{DS_ON} variation will also be studied through characterisations.

2.1.2 Design of the Test Bench

In accordance with the state of the art at the beginning of the thesis, a high short-circuit current, of the order of a hundred amperes or more, can be expected with an extremely rapid rise, several tens of amperes in a few tens of nanoseconds. [21,34,35,77,94,97] as shown in Figure 73 below with a drain-source polarisation about 400 V and a maximum value of drain current about 150 A.

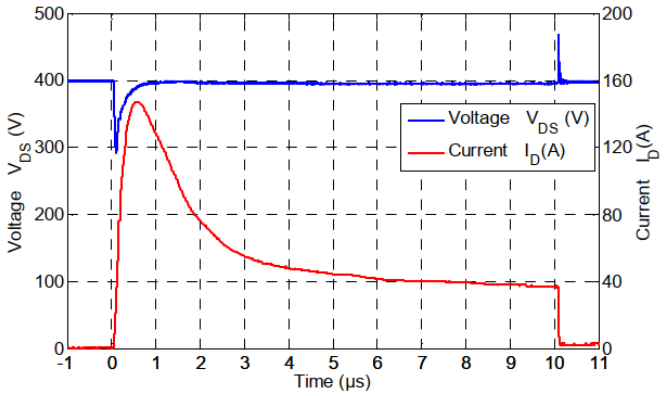

Figure 73: Drain-Source voltage and drain current during short-circuit from [21]

The functional diagram of the experimental bench is given below and the strategy for choosing components is explained in Figure 74.

In terms of the test strategy, in accordance with short-circuits type I, the component is initially blocked using a driver developed specifically for this purpose, and is then turned on by a bias applied on its gate. The normally-off components are still biased negative with a V_{GS} = -6 V signal in order to reinforce the blocked state. The applied polarisations according to the type of component and their general parameters are explained in Table 10, in page 115.

To recreate a short-circuit event, capacitors are used and connected in parallel with the component. Previously charged by the high-voltage supply when the component is gated off, they discharge in this latter when it switches to the on state. In this way, the component enforces the short-circuit current value.
The severity of the test then depends on various parameters such as the voltage delivered by the capacitors and the duration of the short-circuit or, in the present case, the number of repetitive carried out short-circuits. The inherent elements of the bench, such as parasitic inductances, can also influence the behaviour of the transistor during the short-circuit.

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When a component breaks, in most cases drain and source are short-circuited [21] which causes a very rapid increase in the current flowing through the experimental bench. To protect the bench and prevent molten material from being blown out, a simplified circuit protection is inserted. An initial schematic diagram is shown below Figure 74 with C representing the used capacitors. It will be further explained the choice of the type of capacitance

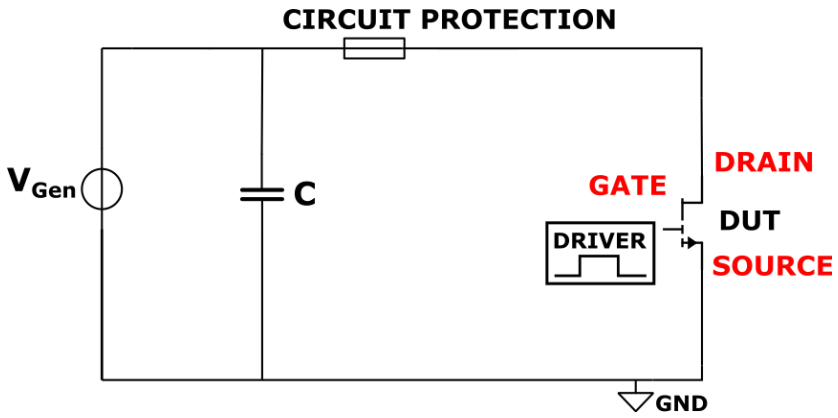

Figure 74: Layout of the test bench

2.1.2.1 Impact of Parasitic Inductances

Parasitic inductances have a particularly harmful effect. In fact, with a particularly high switching speed and the very rapid establishment, in the order of ten nanoseconds, of a short-circuit current, any parasitic inductance in the PCB power loop leads to a significant overvoltage at the component level and turns out to be deleterious.
The inductance of a switching circuit is at least of the order of a few nanohenrys [133], and in most cases exceeds ten nanohenrys [21].
It can therefore be reasonably assumed the following values, with a current variation of 400 A ($\Delta I = 400$ A). At this stage the exact value of the short-circuit current flowing through the component remains unknown, as this value depends on the component. $\Delta t = 20$ ns and a typical inductance of 20 nH is consistent, resulting in the calculation below with a phenomenal overvoltage of 400 V.

$$U_L = L\,\frac{dI}{dt} \rightarrow U_L = 400\,V$$

In addition, the power involved in a short-circuit requires the use of capacitors with a capacitance in excess of a hundred microfarads and, in addition to a non-negligible ESL (Equivalent Series Inductances), generally implies a certain amount of space and therefore an inevitable increase in the length of the tracks and de facto parasitic inductances [21].
Finally, excessive inductances, by opposing current variations, reduce the speed of switching and therefore reduce the analogy with a short-circuit event.

Consequently, particular care is taken to reduce parasitic inductances as much as possible.

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2.1.2.2 *Choice of capacitances*

Creating the situation of an extremely rapid current rise in the duration of ten nanoseconds requires the use of capacitors that quickly deliver current. Ceramic capacitors are well suited to this task, delivering a current as fast as a short-circuit current. Their major disadvantage is their relatively low capacitance (a few tens of microfarads maximum), which means that they can only be used at the start of a short-circuit. The chosen ceramic capacitor will be named C_S. A second capacitor, with a larger capacity and acting as a reservoir, is added. It is this second capacitor that will deliver the current for most of the short-circuit time. A polymer capacitor, with its high capacitance, small size and low parasitic inductance, is the capacitor of choice. This polymer capacitor will be named C_b. The different capacitors chosen and their main characteristics are summarised in the table below in Table 9. *Figure 75* illustrates the differences depending on whether only a ceramic capacitor is used (red curve) or whether this ceramic capacitor is coupled to a polymer capacitor with higher capacitance (black curve).

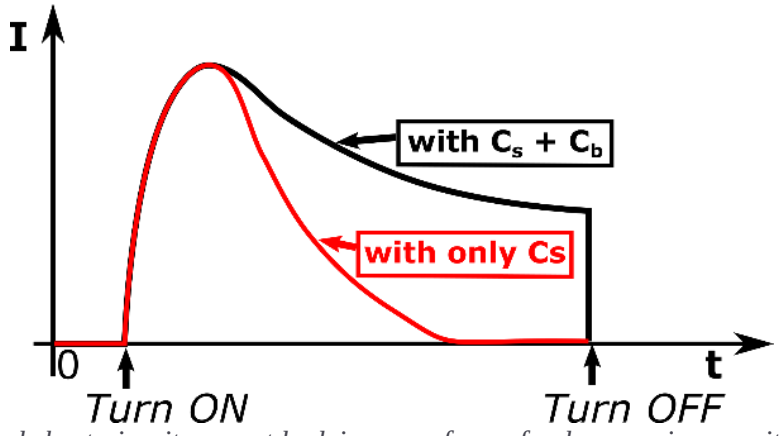

Figure 75:Typical short-circuit current look in case of use of only ceramic capacitance (red curve) and in case of use of both ceramic and polymer capacitance (black curve)

At the bench sizing stage and in the absence of any knowledge of the behaviour of components in short-circuit conditions, the various criteria are taken into account:

- A maximum short-circuit current of 400 A
- A drain – source bias of about 600 V maximum (the tested components are 650 V HEMT)
- A voltage variation tolerance at the capacitor terminals of around 5%, i.e. a maximum of 30 V.

As explained in Chapter 1, the duration of 10 µs is often referred to in the literature concerning short circuits in IGBT. This duration criterion is inherited from the study of short circuits in silicon components [21]. The target short-circuit time is therefore a maximum of ten microseconds.

This gives the following calculations:

For the ceramic capacitor C_s, supplying the first part of the short-circuit current for a relatively short time (100 ns)

$$\boldsymbol{\Delta t = 100\,ns; \Delta V = 30\,V; I = 400\,A\ ; I = Cs\,\frac{dV}{dt} \rightarrow Cs = 1.33\,\mu F}$$

For the secondary capacitor C_b, which supplies current for most of the remaining short-circuit time (around 10 µs):

$$\boldsymbol{\Delta t = 10\,\mu s\,; \Delta V = 30\,V; I = 400\,A\ ; I = Cb\,\frac{dV}{dt} \rightarrow Cb = 133\,\mu F}$$

The selected components and their characteristics are summarised in Table 9.

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2.1.2.3 Choice of Circuit Protection

A fuse is preferred to an IGBT for circuit protection. In general less protective than an IGBT because of its longer reaction time, a fuse could be much less inductive [21]. The action time of an IGBT is generally between 6 and 10 µs [99] whereas a fuse will react according to the product I^2t with a time scale of the order of milliseconds (cf datasheet of the chosen component is in appendix). Circuit protection can therefore be delayed or triggered unexpectedly. Nevertheless, the typical parasitic inductances of an IGBT on the current market, in particular Infineon technology, are of the order of several tens of nanohenrys.

The need to reduce parasitic inductances therefore leaves no choice as to the use of the fuse. On the other hand, the fuse must be able to pass the short-circuit current while opening the circuit in the event of a component fault, synonymous with a current surge of in excess of 500 A.

In order to reduce the inductance caused by the addition of the fuse as much as possible, an SMD (Surface Mounted Device) type assembly is chosen. The datasheet of the chosen fuse with I^2t curve is in the appendix.

2.1.2.4 Current Sensing

Short-circuit rating appears to be a key element. Although manufacturers specify the current calliper of component, no information is provided on the short-circuit current that the DUT enforces. Such a measure requires a wide bandwidth. As shown in the Figure 73, two dynamics can be observed, with a very rapid rise in current, on the order of ten nanoseconds, then a stabilization of the current with, in some cases, little variation, and finally a very rapid rise if the component is destroyed [92].

The low bandwidth is therefore close to zero, while the high bandwidth is well above MHz and even approaching GHz.
Various measurement techniques are classically envisaged and are detailed below.

Active current probes, otherwise known as Hall effect probes, although they can have bandwidths of up to 120 MHz, are limited in terms of maximum current (30 A at Tektronix probe, ref TCP0030A).

Current transformers or measuring toroid can be used. Their principle is based on Faraday's law and magnetic induction. They consist of a magnetic circuit, in this case a ferrite toroid, through which the conductor passes, the primary circuit as shown in Figure 76. Another conductor is wound around the core and acts as the secondary circuit.
When a current flows through the primary conductor, a magnetic field is generated in the toroid. This magnetic field $\vec{B}$ will then induce a current in the secondary circuit. By knowing the number of turns made around the toroid, and with the measurement of the secondary current, the value of the primary current I can be found.
Although this technique can be used to measure relatively high currents of the order of several hundred amperes at frequencies of up to tens of kilohertz or even up to 200 MHz for low currents in the range of hundreds of milliamps [134], its main drawback is that it cannot measure DC currents. This technique is therefore not suitable for short-circuit conduction.

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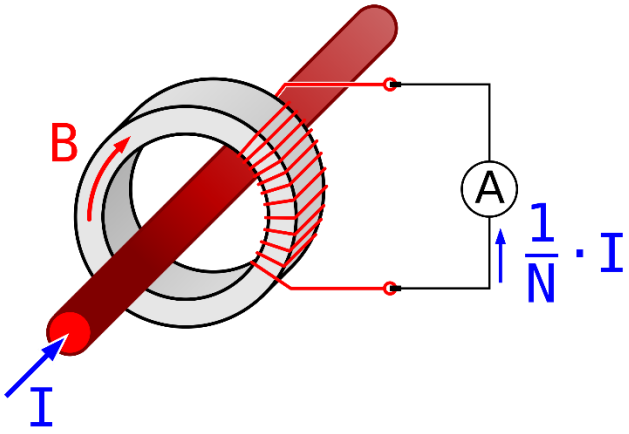

Figure 76: current measurement toroid

Rogowski toroid models do not use a magnetic circuit and are based on the use of non-magnetic sensors. The output signal is proportional to the time derivative of the primary current. As a result, they are not suitable for DC currents. In addition, they have a lower bandwidth, of the order of ten megahertz [134,135].

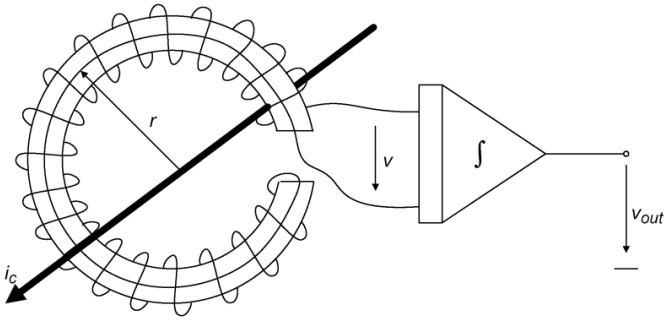

Figure 77: A Rogowski coil with a non-magnetic core material. An integrator is needed to obtain a signal proportional to the primary current from the induced voltage, from [136]

Shunt resistors are based on the principle of inserting a small resistor into the circuit and then measuring the voltage at its terminals. This resistor is usually made of a copper, manganese and nickel alloy called manganin [137–139], which gives it a very low variation in resistance as a function of temperature. The physical structure with the used materials is shown in *Figure 78*. It can be used for currents ranging from tens of mA to kA. As the resistance of the shunt is precisely known, measuring the voltage drop across the shunt gives a precise value for the current flowing through it. The shunt could have the advantage of a wide bandwidth.

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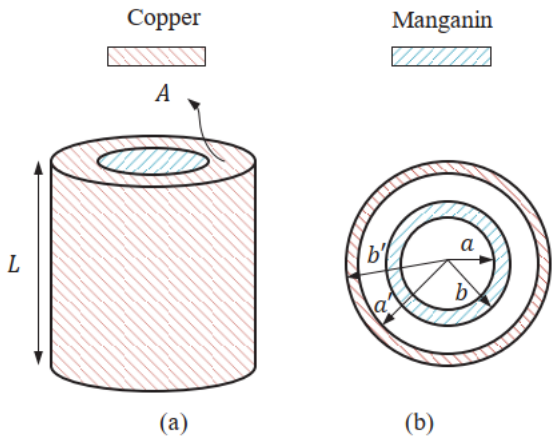

Figure 78: Physical structure of a coaxial shunt resistor, side view (a-left) and cross-sectional view (b-right) from [139]

A. Kohler in [140] nevertheless raises the problem of possible disturbances due to magnetic coupling induced by the source. He also points out that this mutual inductance increases with frequency. He therefore recommends using twisted or coaxial connections and keeping the measuring equipment away from the source.

Different shunt structures exist. Shunts with nut tightening as shown in Figure 79 have the disadvantage of having poorly defined contact resistances. Coupled with the nature of the conductor and possible corrosion, this represents a non-negligible measurement error [140].

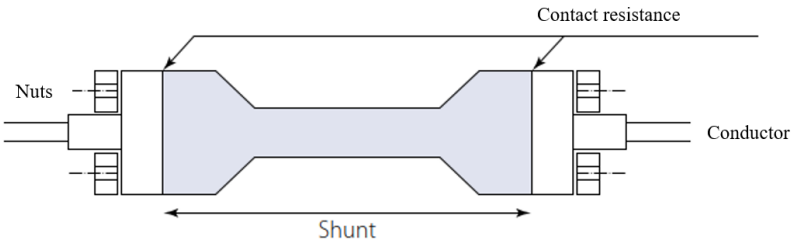

Figure 79: Assembly of an industrial shunt from [140]

Other structures can also lead to poor current distribution, resulting in measurement errors, as in the structure below in Figure 80.

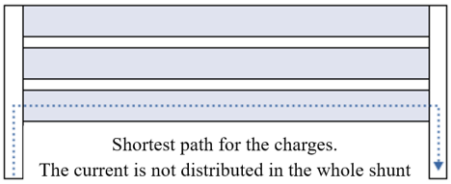

Figure 80: 3-blade structure of a shunt from [140]

Shunts with a coaxial structure reduce these possible measurement errors. However, as it will be seen later when optimizing the bench, they are not free from faults, due to their non-negligible parasitic inductance and the radiated field.

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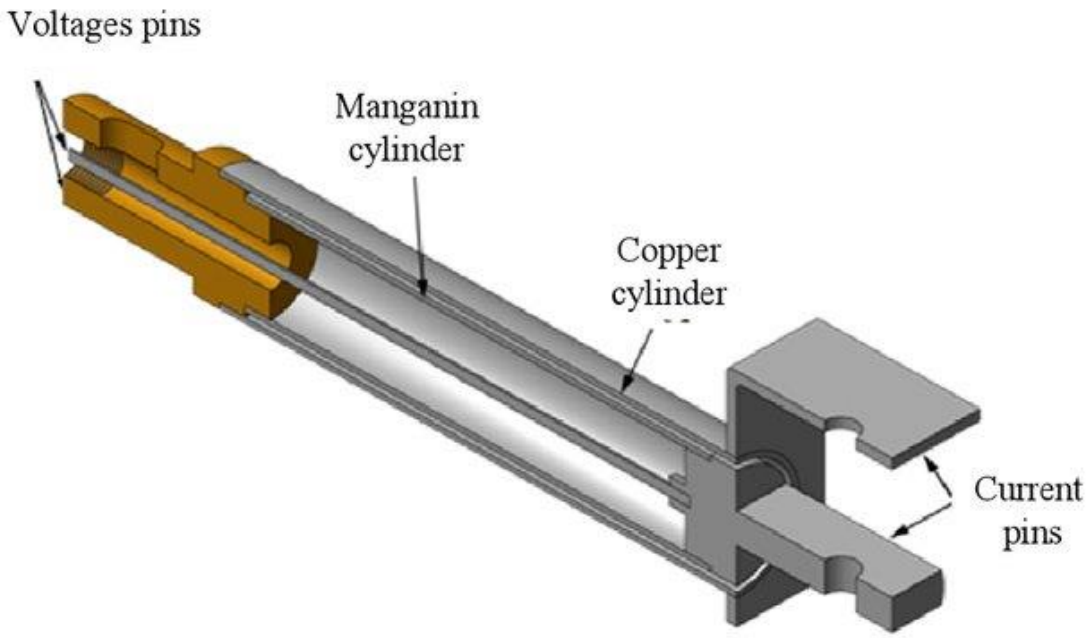


Figure 81: coaxial shunt structure from [141]

Compared with the various techniques available, and given the very fast switching of GaN components, the choice of current measurement device is based on shunt resistors.

All the hypothesis and calculations lead to the following table of components:

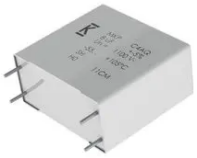
Type of component	Type of component	Main parameters	Supplier	Ref. supplier
	Ceramic capacitor	$V_{Pk,\,max}$ = 650 V C_{nom} = 2 µ F ESR = 5 mΩ ESL = 3 nH	TDK	B58035U5205M052
	Polymer capacitor	$V_{Pk,\,max}$ = 650 V C_{nom} = 130 µ F ESR = 2 mΩ ESL = 19 nH	KEMET	C4AQCEW6130A3BJ
	Ceramic Fuse	ESR = 2 mΩ ESL : not specified	BOURNS	SF-2923HC20C-2
	Current Viewing Resistors	R = 10 mΩ Bandwidth : up to several GHz	T&M Research	SDN-414-01

Table 9: chosen components and their characteristics

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The block diagram of the experimental test bench is structured as shown in the Figure 82 below.

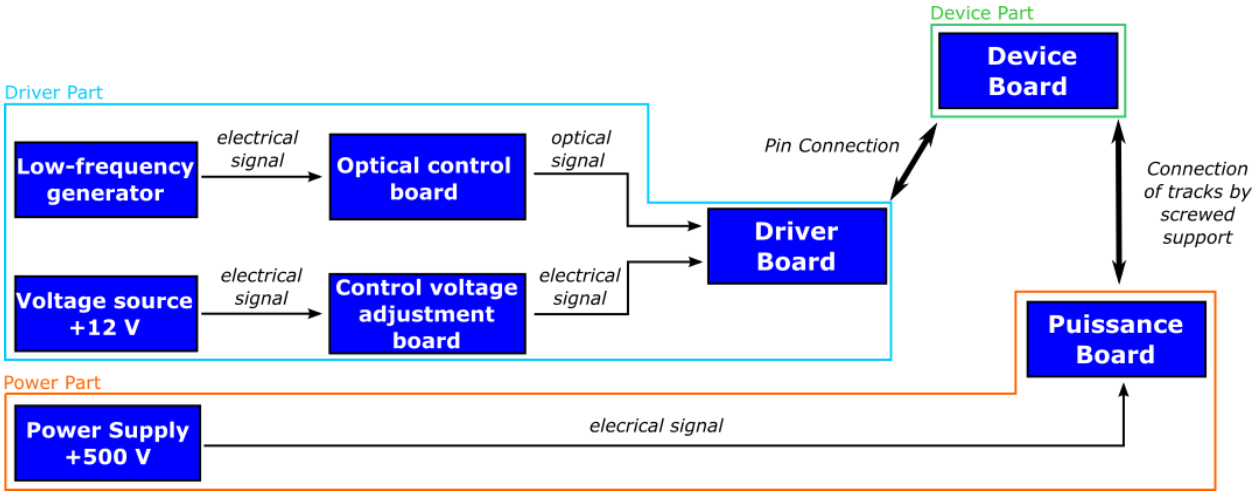

Figure 82: block diagram about the test bench

2.1.2.5 Daughter Board and Mother Board

The test strategy includes static electrical characteristics on a power device analyser, type B1505A from Keysight. The test bench consists of three key elements: the power mother board with capacitors, fuse, and current measurement shunt, the "device" daughter board with the transistor encapsulated in its sarcophagus, and the driver section for -24 V / 0 V or -3 V / + 6 V control.

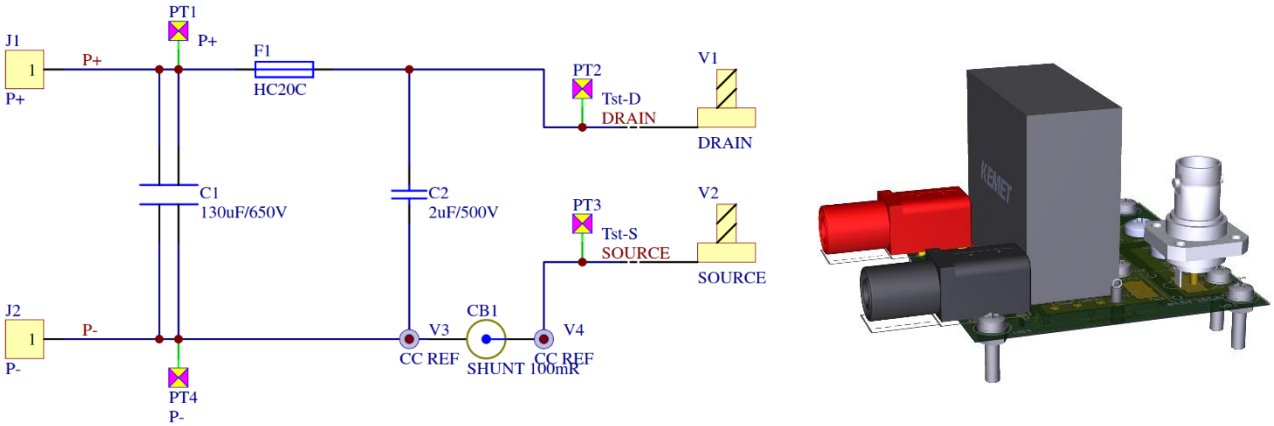

Figure 83: electrical scheme of the Mother Board and its 3D view

The Figure 83 shows the electrical scheme and the 3D-view of the power mother board. At left can be seen the red and black connection to HV-supply. The massive grey block is the polymer capacitor, and closer to the daughter board than this latter. Hence the significant inductance of the polymer capacitor does not affect loop inductance. As the shunt has a vertical structure, a connection to it can be seen in the power board. The two screws enable to attach the power board to the daughter board, presented in Figure 84.

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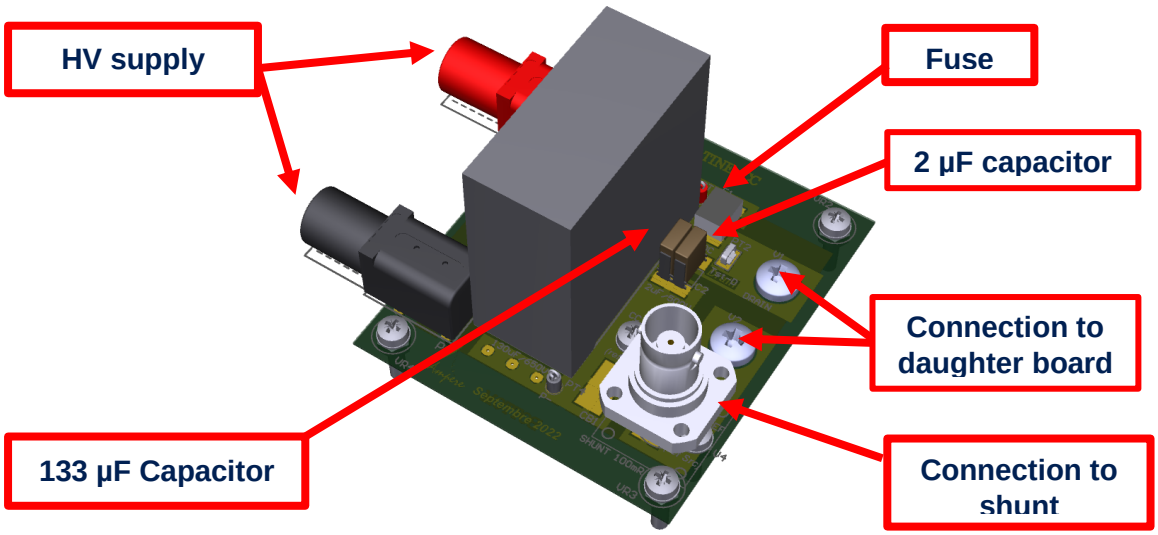

Figure 84: 3D view of the power board 2023 and its component

To reduce component handling, which could affect these electrical properties, the daughter board has been designed to be easily connected to the Keysight B1505A characteristic tracer. Figure 85 shows the daughter board and in the middle of it the sarcophagus. A small board (in light green in the figure below) enables the connection to power board with screws. These screws can be used to connect the daughter board to the characteristic tracer.

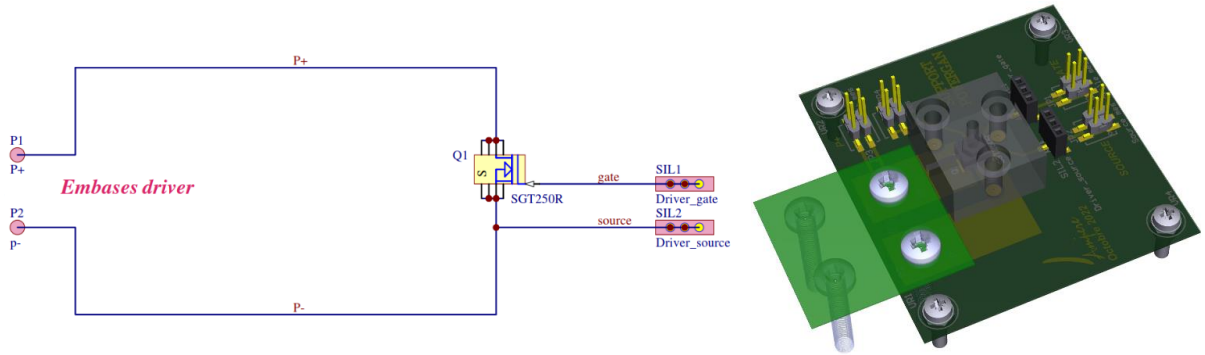

Figure 85: electrical scheme of the daughter board 2023 and its 3D view

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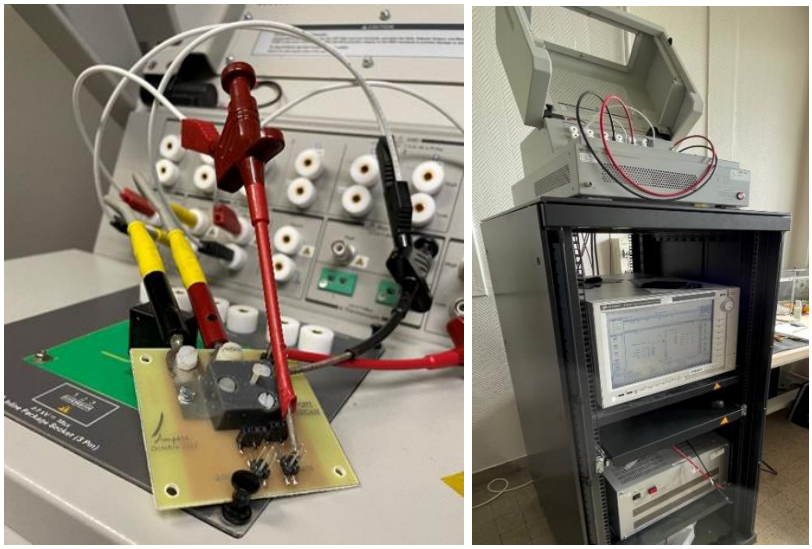

Figure 86: daughter board and its sarcophagus during a sequence of measurement at B1505A (left) and the B1505A (right)

In addition, to avoid soldering/unsoldering of components on this daughter board, and thus cause significant thermal stress, a 3D-printed sarcophagus was designed to maintain the component and ensure pressure conduction [142].

This sarcophagus was firstly drawn in a computer aided design (CAD) software. Many precautions has been taken like the use of a reduced margin (0.1 mm) which is the maximal range of precision of 3D printing. The chosen 3D printing technique was the stereolithography (SLA) in regards to its higher operating temperature and tensile strength. Thanks to a greater printing precision and getting smoother surface, this technique guarantees a better fit to the transistor dimension.

Considering the fact that the material has to be resistant to the maximum temperature outside of the transistor, rigid with a tensile strength of the order of tens of MPa, the material “Tough 2000” from Formlabs appears as the most relevant.

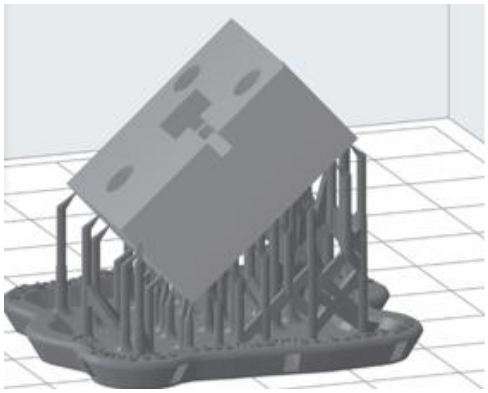

Figure 87: 3D printed sarcophagus (view from the 3D printing software)

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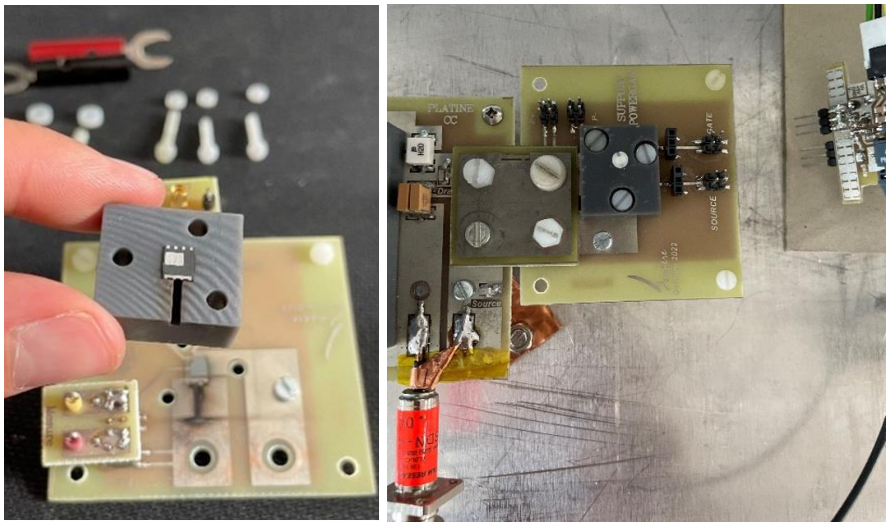

Figure 88: printed sarcophagus (bottom view, left) and mounted on the daughter board (right)

During the experiment, similar electrical characterizations with a brazed component ensured that the sarcophagus did not interfere with the component electrical properties [142]. Figure 90 shows a brazed component on a specific daughter board. A small board is also used to connect the probes to the daughter board. A comparison has been conducted between pressed and brazed normally-on devices in Figure 89. It shows no significant variation between pressed or brazed device. The only seen varaition is due to the dispersion of devices. The use of sarcophagus is therefore validate.

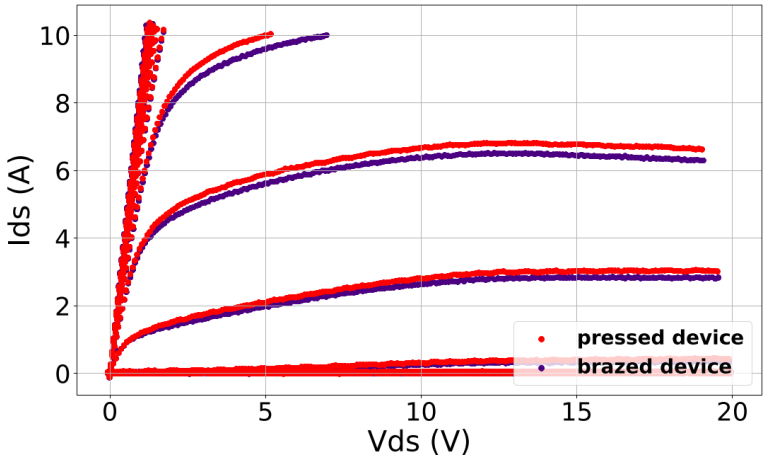

Figure 89: Comparison of eletric conduction between pressed and brazed devices

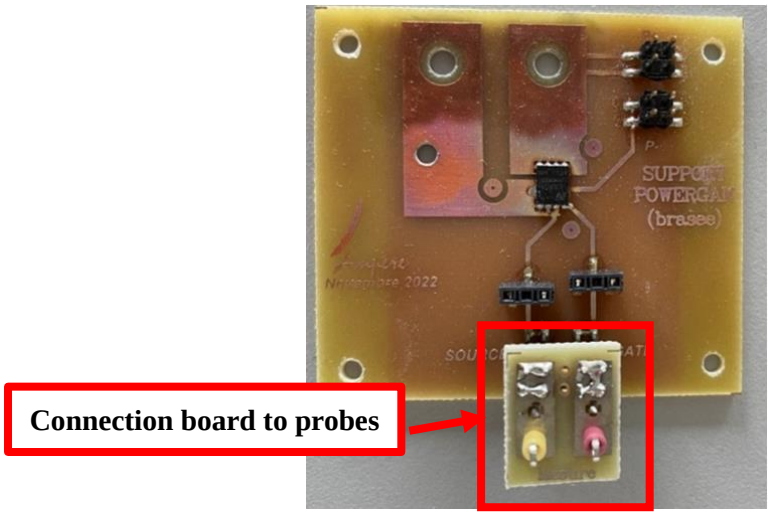

Figure 90: brazed component on a specific daughter board

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The final strategic scheme of the test-bench can be resumed as below in Figure 91.

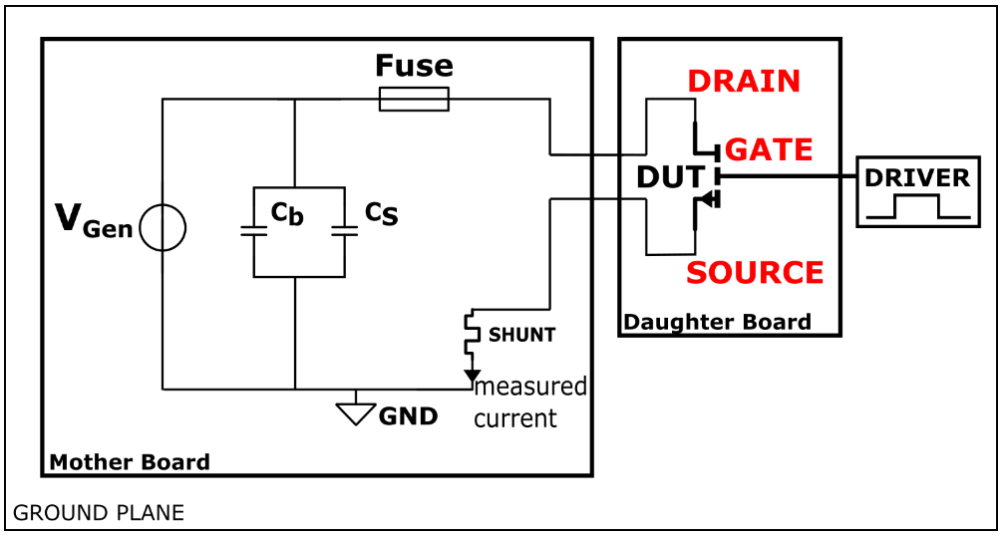

Figure 91: final strategic scheme of the test bench

The first experimental version of the test-bench and its main components are shown below in Figure 92 and in Figure 93. In Figure 92 the main elements can be seen as the driver power supply, the power / mother board, attached to the daughter board. The driver is connected to the daughter board. A eight-channel oscilloscope is used to display the various curves.

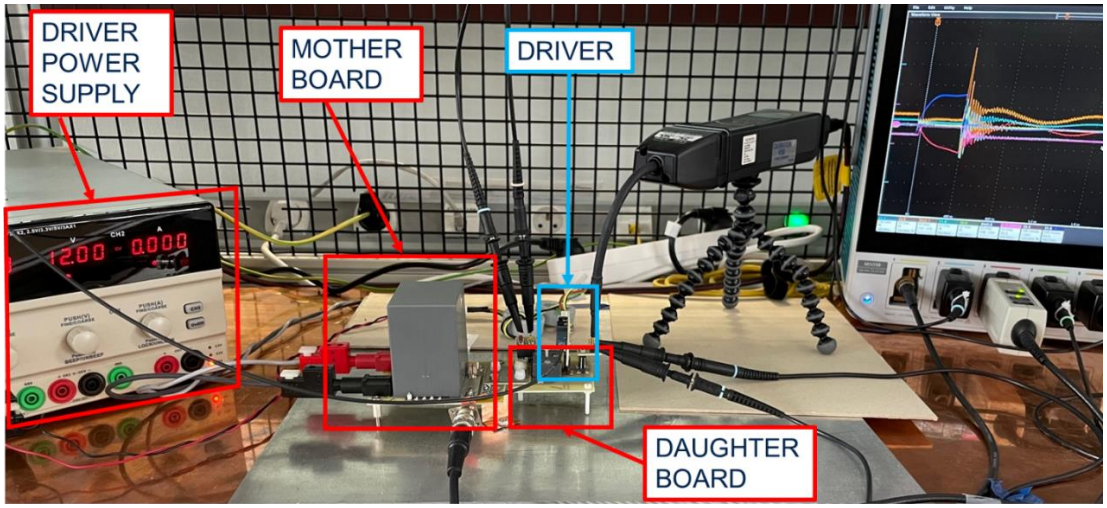

Figure 92: large experimental view of the first short-circuit test bench 2023

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Figure 93 zooms in on the daughter board, bolted to the power section. It shows the sarcophagus in grey and its three screws, as well as the driver near the component trapped under the sarcophagus.

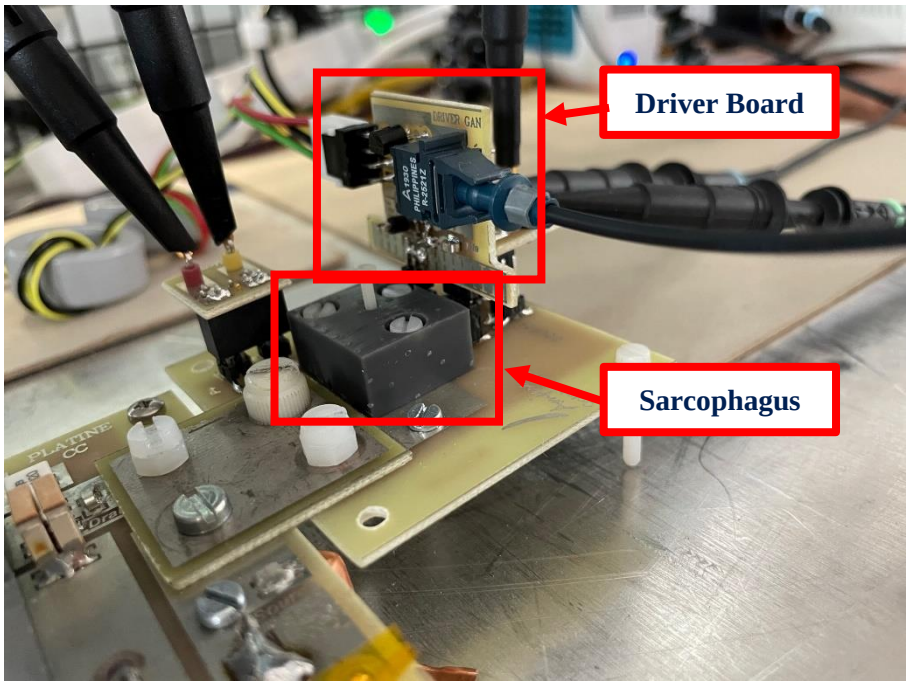

Figure 93: zoom on daughter board 2023 with screwed sarcophagus on it

2.1.2.6 Driver

A driver has been specifically developed for the test bench. It consists of two parts: the driver power supply board and the driver board as shown in Figure 94. The first board, as its name suggests, is used to adjust the ON and OFF control voltages applied to the gate of the component.
By means of vertical connectors, the driver is plugged in as close as possible to the component, as can be seen on the photographs.

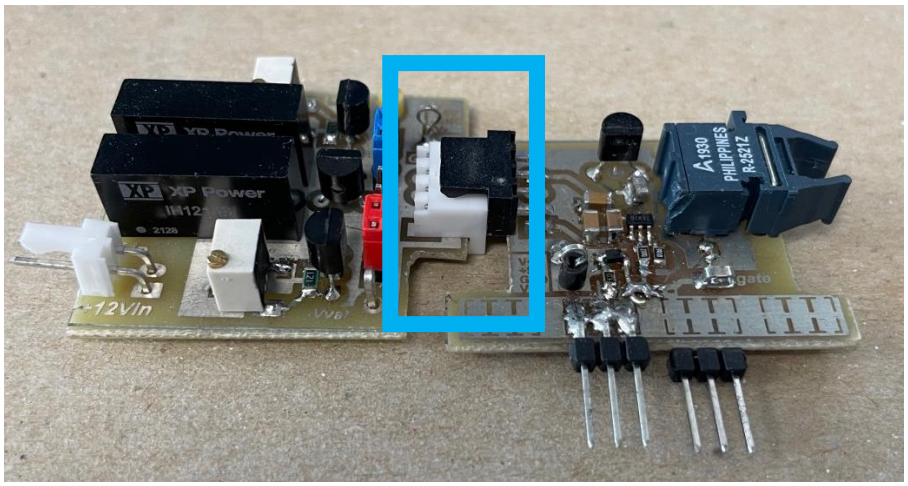

Figure 94: the two boards that build the driver 2023 (driver power supply: left, driver board: right)

Figure 94 shows a white connector (in blue square) between the driver power supply and the driver board. This connector allows the power supply to be moved away from the driver, if required. This connector also allows to be replaced by wires, enabling the use of ferrite cores for signal stabilization.

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The logic signal is transmitted via an optical fibre, arriving on one side of the driver board, while the gate bias levels are linked to the other side of the driver board.

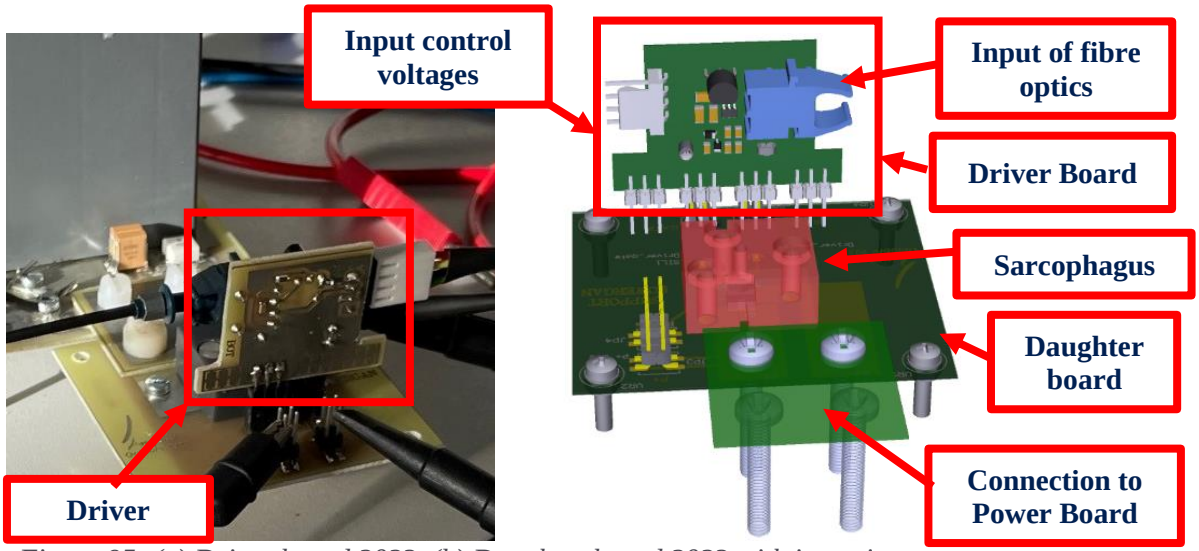

Figure 95: (a) Driver board 2023, (b) Daughter board 2023 with its main components

The driver power supply board consists of DC/DC converters for voltage stabilisation and potentiometers for adjusting the bias voltages applied to the gate of the component under test. Jumpers can be interchanged to adjust voltage levels between an adjustable potentiometer voltage and ground. This is particularly relevant when normally-on components are driven with control voltage levels of -24 V and 0 V respectively.

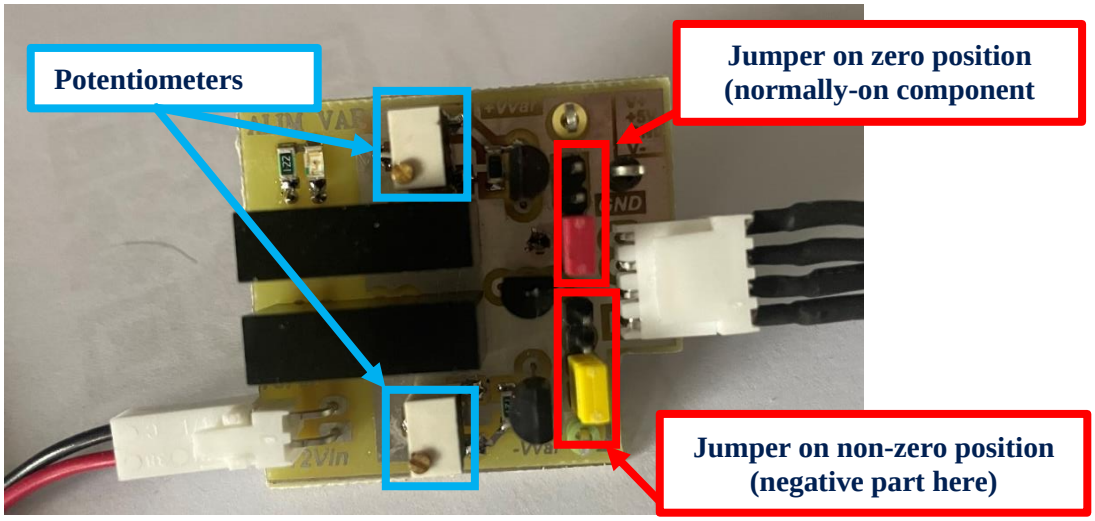

Figure 96: View of the driver power supply board 2023 and its components

General

Efficiency	• See table
Isolation Voltage	• 1000 VDC[2]
Isolation Resistance	• 10^9 Ω
Isolation Capacitance	• 60 pF typical

Input Voltage	No Load Input Current	Output Voltage	Output Current	Efficiency	Model Number[1,2]
12 VDC	20 mA	±3.3 V	±200 mA	67%	IH1203S
	20 mA	±5.0 V	±200 mA	75%	IH1205S
	20 mA	±9.0 V	±111 mA	77%	IH1209S
	20 mA	±12.0 V	±84 mA	82%	IH1212S
	20 mA	±15.0 V	±66 mA	82%	IH1215S
	20 mA	±24.0 V	±42 mA	82%	IH1224S

Figure 97: main parameters of used DC/DC converters

The second board, on the other hand, the driver board, aims to manage the control with the input of the logic control of an optocoupler, connected to the logic signal generator via an optical fibre.

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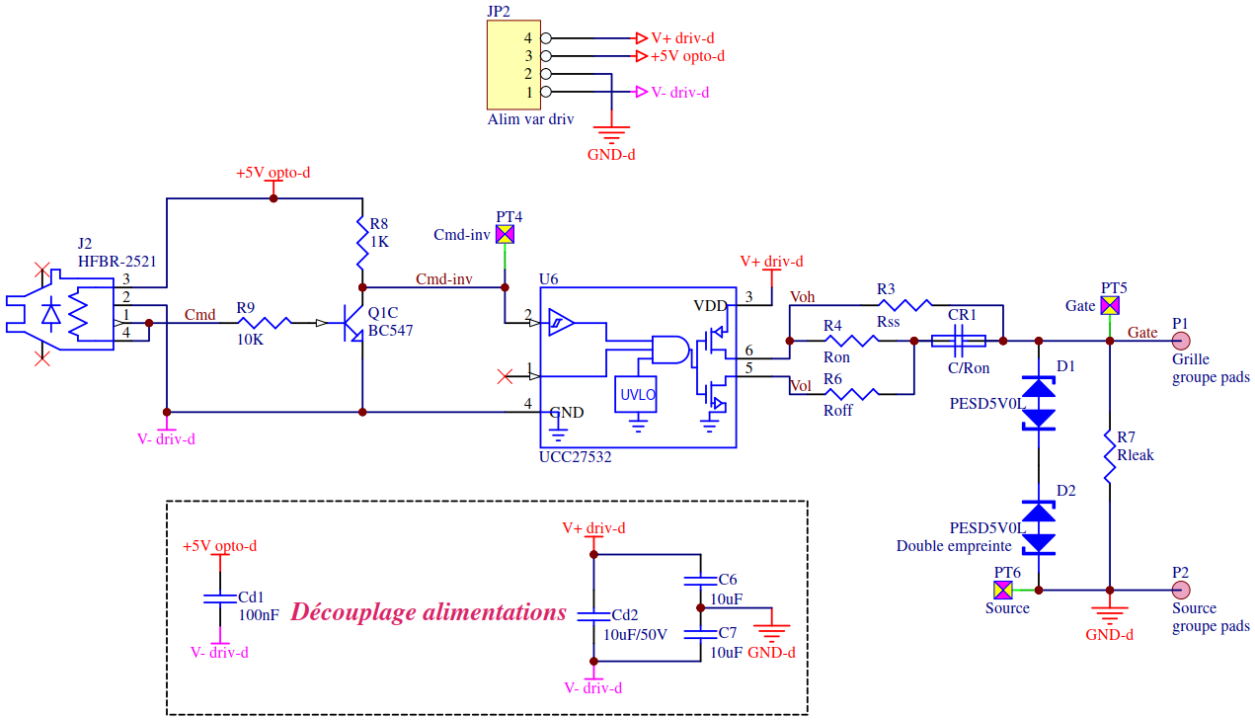

Figure 98: electrical scheme of the driver power supply board

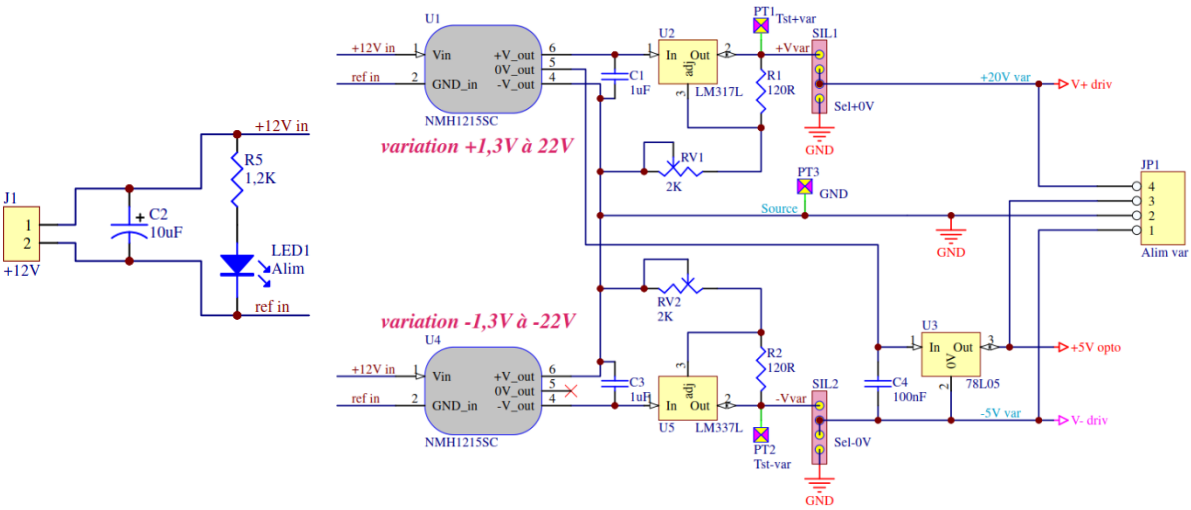

Figure 99: electrical scheme of command driver board

The arbitrary function generator used comes from Tektronix and is shown in *Figure 100* below.

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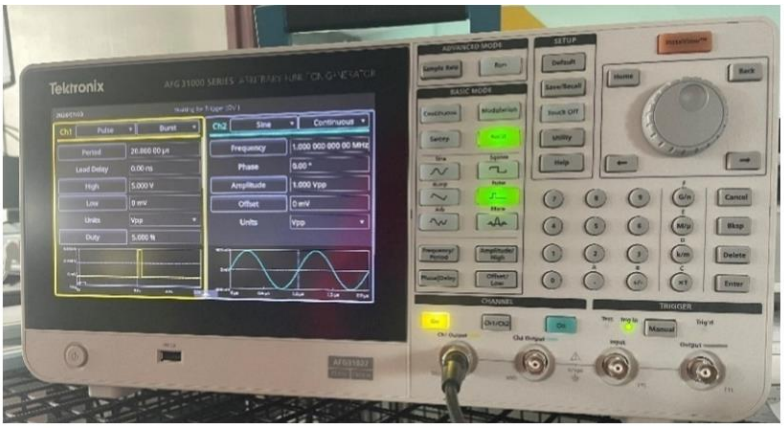

Figure 100: Arbitrary function generator AFG31000 Series

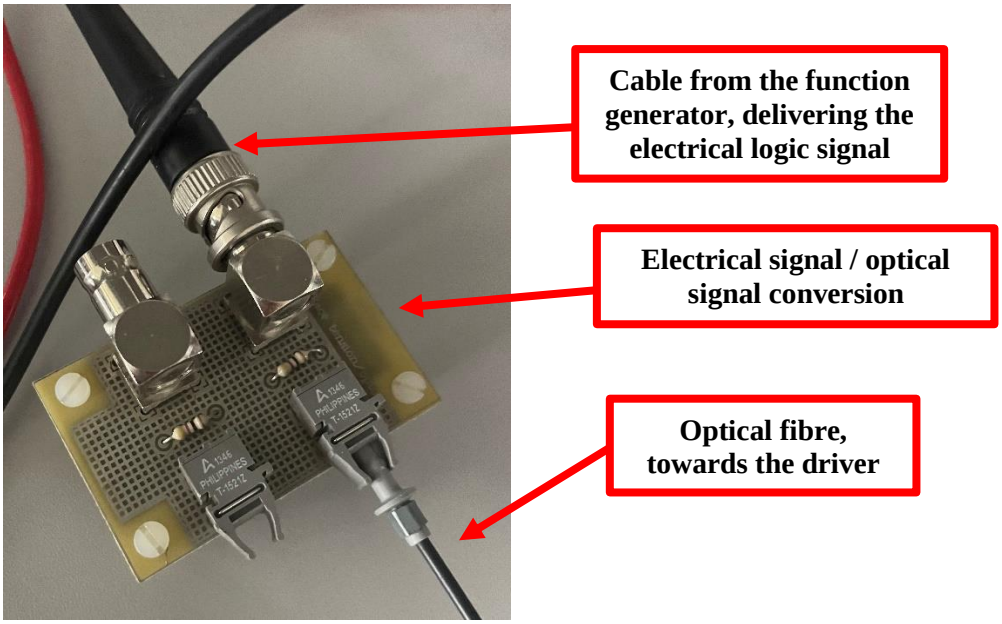

Figure 101: Photography of the optical control board

2.1.2.7 Tested components

Normally-on components, MIS-HEMT technology (insulated gate HEMT [35]) and normally-off (Cascode and p- GaN [21]) components are chosen. The advantage of cascode technology is that the GaN part is identical to its normally-on part, enabling comparisons to be made about failure mechanisms. P-GaN technology is chosen as this structure seems to be preferred in the current industrial development. All components are packaged in QFN 5x6.

Component	Supplier	V_{th}	V_{GS} OFF / V_{GS} ON	Id	R_{DS_ON}
D-mode	Supplier 1	-12.5 V	- 24 V / 0 V	10 A	250 mΩ
Cascode	Supplier 1	1.8 V	- 3 V / +6 V	10 A	190 mΩ
p-GaN	Supplier 1	1.8 V	- 3 V / +6 V	15 A	120 mΩ
p-GaN Prototype	Supplier 1	1.7 V	- 3 V / +6 V	12 A	190 mΩ
p-GaN	Supplier 2	1.7 V	- 3 V / +6 V	11 A	150 mΩ

Table 10: Different types of studied components and their main parameters

Different daughter boards have been designed, relative to the footprint of the components.

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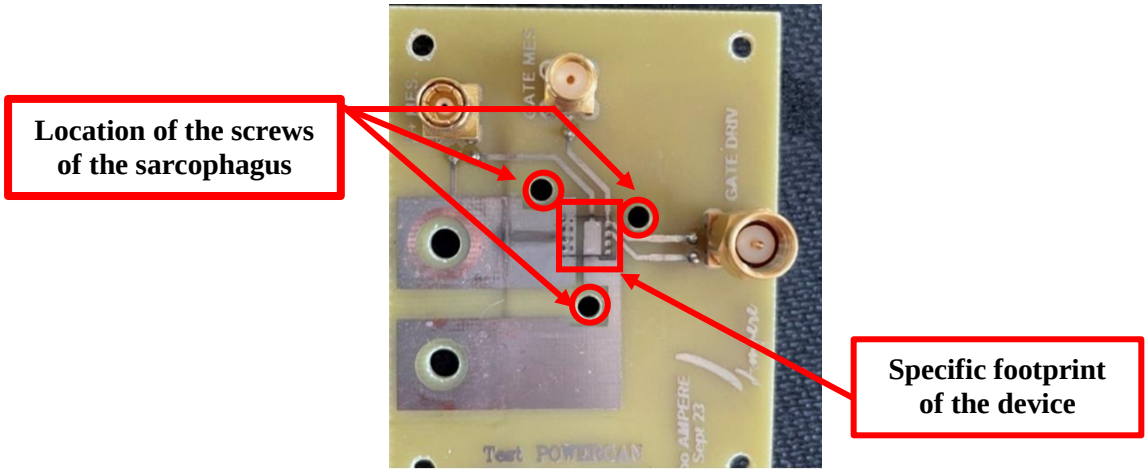

Figure 102: 2023 daughter board with a specific footprint

2.1.2.8 Test Strategy and Characterization Sequence

Various types of tests and measurements can be carried out using the KEYSIGHT B1505A. These include:

- Measurement of threshold voltage V_{th}
- Measurement of on-state resistance R_{DS_ON}

The repeatability and reliability of these measurements have been carefully studied, in particular to avoid measurement hysteresis problems relating to GaN and carriers trapping/detrapping phenomena [143]. Therefore, each initial characterization sequence was performed using the Triple-Sens reset protocol [142]. The V_{th} and R_{DS_ON} measurements were also repeated five times consecutively to ensure that the results were stable. Other complementary measurements were carried out, with increased repetition. This gave the same results in terms of stability and therefore validated the measurement sequence. This ensured that the results are not biased by an erroneous first measurement. Finally, to ensure that the parametric variations observed were indeed the result of the short-circuit application, witness components, known as ‘Golden Devices’, were used.

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2.2 Initial Tests and Optimisation of the Bench for Normally-ON Components

The first tests are carried out on the normally-ON components. A gradual increase in voltage is applied to ensure that all the components and the test bench are working properly.

2.2.1 First Tests and First Problems

Particular care has been taken to reduce parasitic inductances in advance. This involves careful routing and optimised compactness, as well as surface-mounted components with reduced ESL. Despite this, the first short-circuits caused significant disturbance and the bench had to be adjusted.

The first short-circuit was conducted for drain-source voltage V_{DS} of 10 V. Non-negligible overvoltage is observed at turn-off on V_{GS} and V_{DS} signals as shown in Figure 103 . For V_{DS} = 50 V, the signals oscillate at the risk of damaging the component at turn-off or even causing it to break. It is even worse for V_{DS} = 75 V. Solutions therefore had to be found and are further detailed.

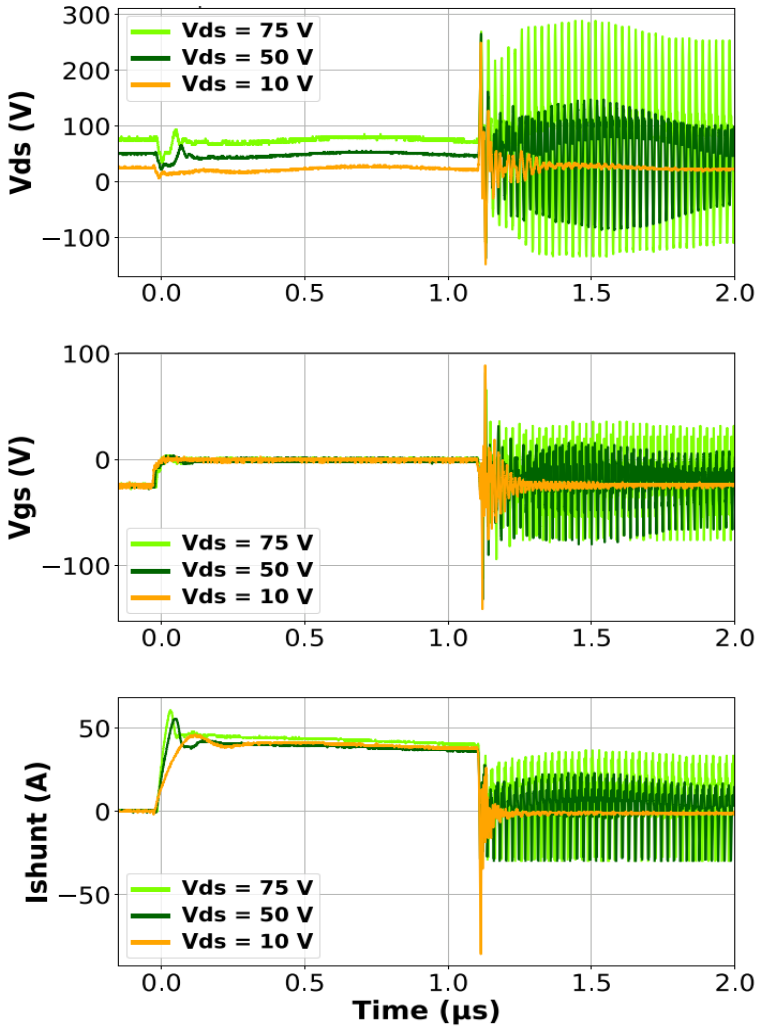

Figure 103: V_{DS}, V_{GS} and I_{SHUNT} measured signals during first short-circuits and an increasing drain - source polarization on test-bench 2023

The first component failures appear with the uncapping of the component, as shown in Figure 104. The power is therefore sufficient to tear off the package due to thermo-mechanical expansion. The presence of the intact fuse reduces the probability of a drain current runaway. At this stage, gate failure appears more likely. However, it is not possible to conclude whether the failure is due to the apparently unstable

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operation of the test bench or whether the component is not sufficiently robust to withstand successive short-circuits and has finally broken.

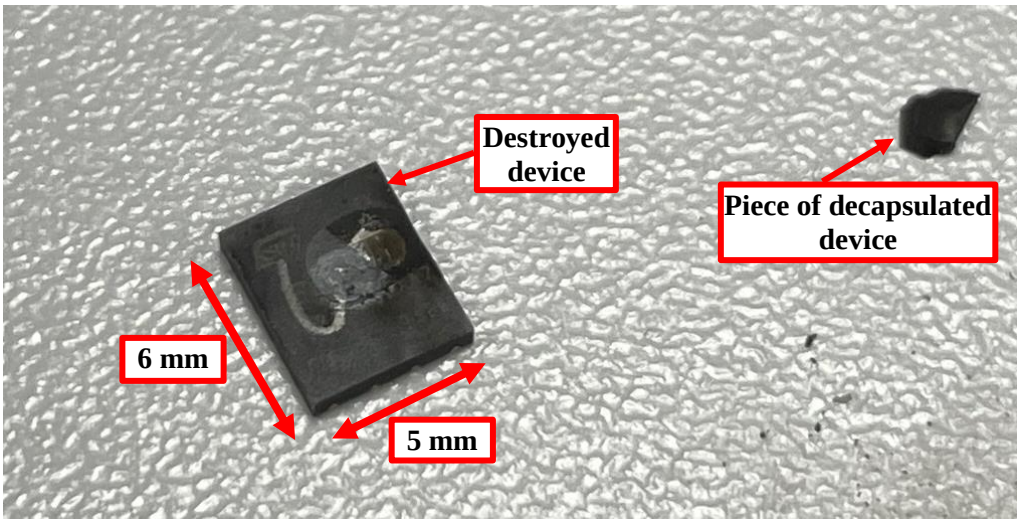

Figure 104: Photography of a destroyed component after a breakage for V_{DS} = 75 V and t_ON = 1µs

As the bench is functional, there are no routing problems and the layout in Figure 74 is therefore correctly executed. On the other hand, the fact that disturbances are present as soon as the drain-source polarisation is increased even slightly led to carry out a SPICE simulation.

At the same time, initial adjustments were made by changing the R_{GOFF} resistor from 9.1 Ω to 20 Ω. For future tests, it was decided to keep the drain-source bias low, with V_{DS} = 10 V, in order to reduce the risk of component breakage. Figure 105 shows the configuration with R_{GOFF} = 9.1 Ω (purple curve) or with R_{GOFF} = 20 Ω (red curve).

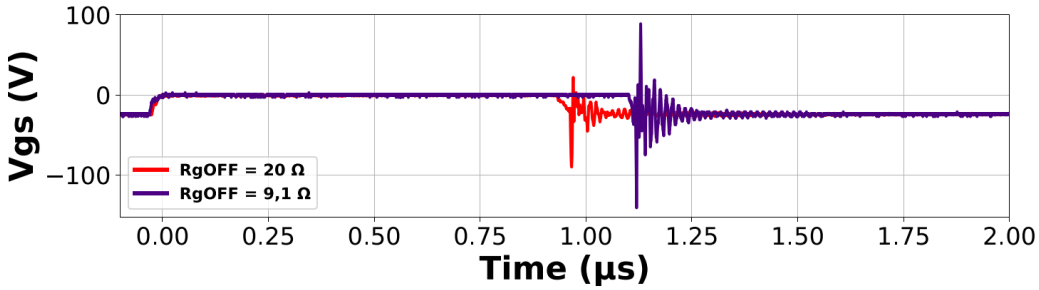

Figure 105: Comparison of the V_{GS} signal for two R_{GOFF} resistor values

As it can be seen in Figure 105, this increase in the R_{GOFF} resistor gives encouraging signs with the significant reduction in the overvoltage at turn OFF of the V_{GS} signal. However, the disturbances remain unacceptable for the V_{GS} signal, with a peak close to -100 V at turn OFF on the gate, and the gate resistance cannot be increased indefinitely. The duration of the short-circuit is different between the two tests, it will be solved with the 2024 driver.

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2.2.2 Development of the SPICE Simulation

2.2.2.1 Model of the Test Bench

For greater clarity, the general diagram of the experimental bench is shown below and annotated with colours defining the blocks whose modelling is detailed below.

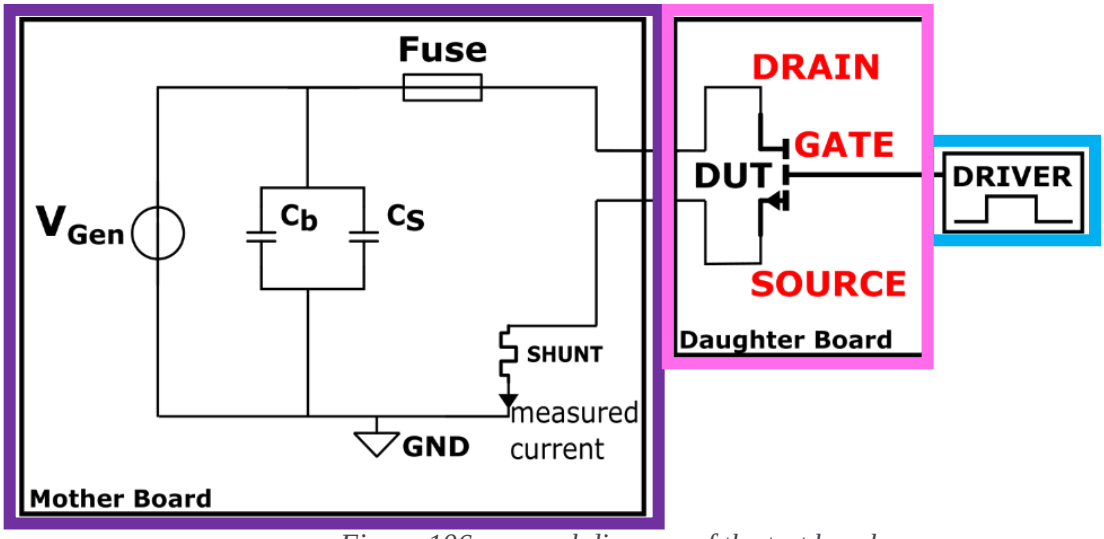

Figure 106: general diagram of the test bench

The power section is first simulated using SPICE.

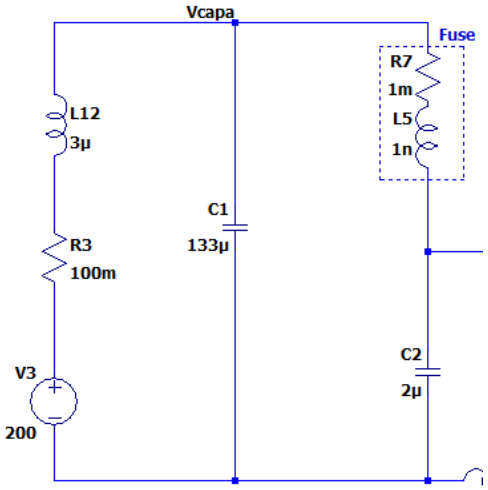

Figure 107: Power side of the SPICE simulation of the test bench

The two capacitors C1 and C2, of 133 µF and 2 µF respectively, are inserted as well as their ESR (Equivalent Series Resistance) in accordance with the datasheet. The fuse is modelled as a low resistance with a parasitic inductance reduced to 1 nH, not mentionned by the supplier but judged to be of this order due to the SMD mounting of the fuse.
L12 represents the parasitic inductance of the wires connecting the high-voltage supply to the test board.

A SPICE model of the shunt was also developed, consisting of inductors and a 10 mΩ resistor.

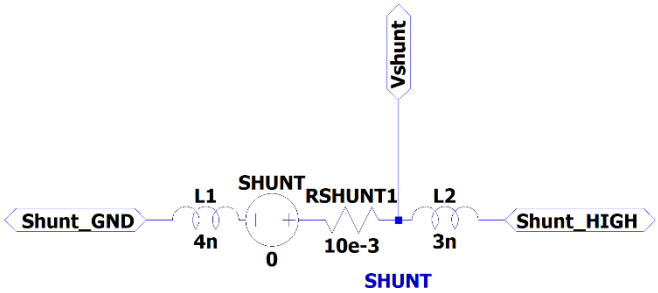

Figure 108: shunt SPICE model from discussion with Dr. Dominique Tournier in Lab. Ampere

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The connections from the power board to the daughter board were modelled by resistors and the conduction paths by parasitic inductances. The HEMT model is inserted into the SPICE simulation, with Dp, Sp and Gp representing the drain, source and gate of the component.

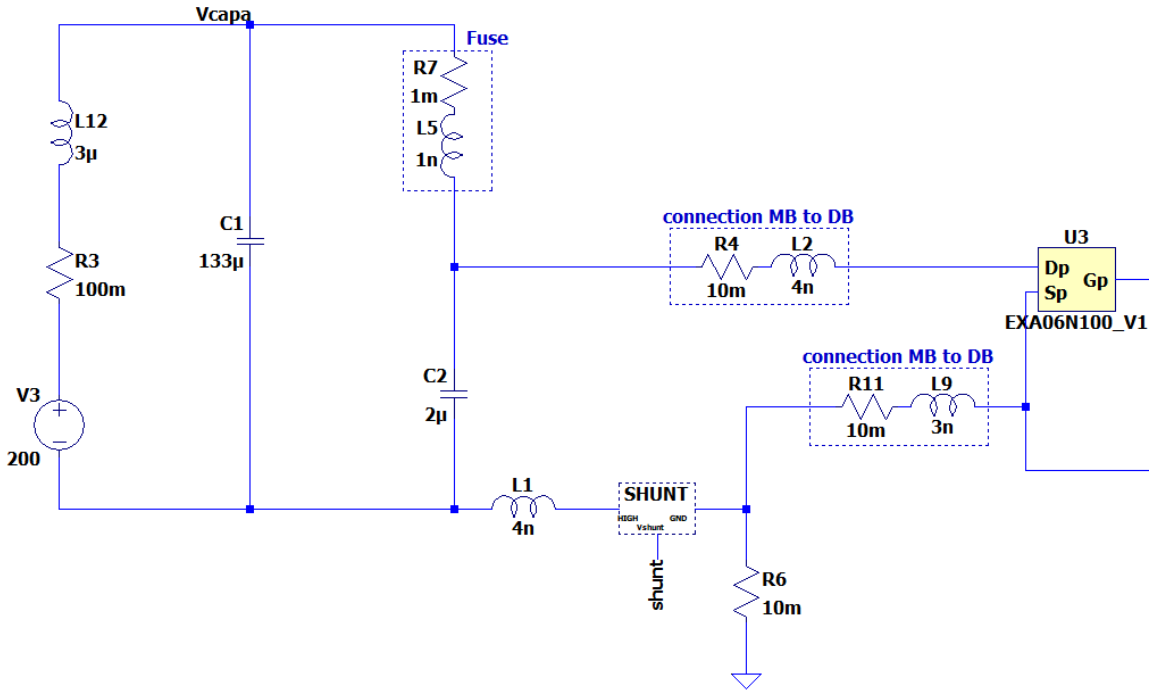

Figure 109: SPICE simulation of the test bench

Finally, the driver part is modelled using MOSFET models with characteristics as close as possible to those given in the datasheet for the driver used, reference ucc27532.

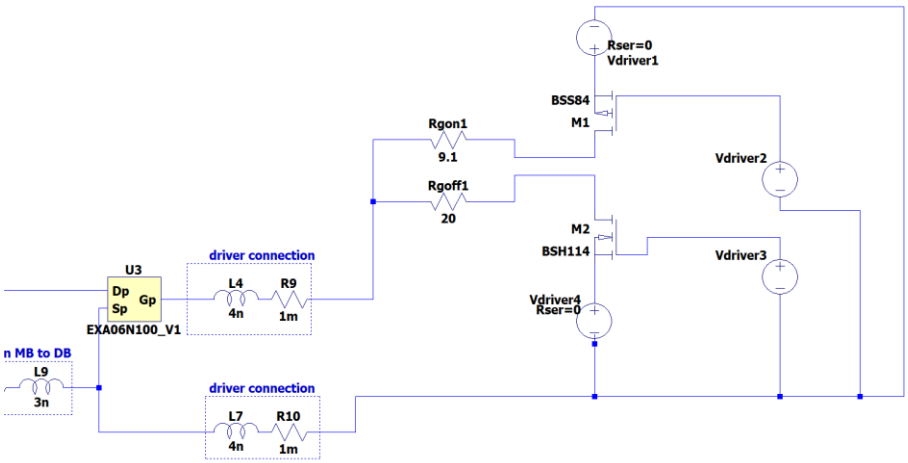

Figure 110: SPICE simulation of the driver part

This leads to the following general SPICE simulation scheme shown in Figure 111. However, this simulation will be improved later. Other values, particularly for parasitic inductance will be changed. These changes are described further below.

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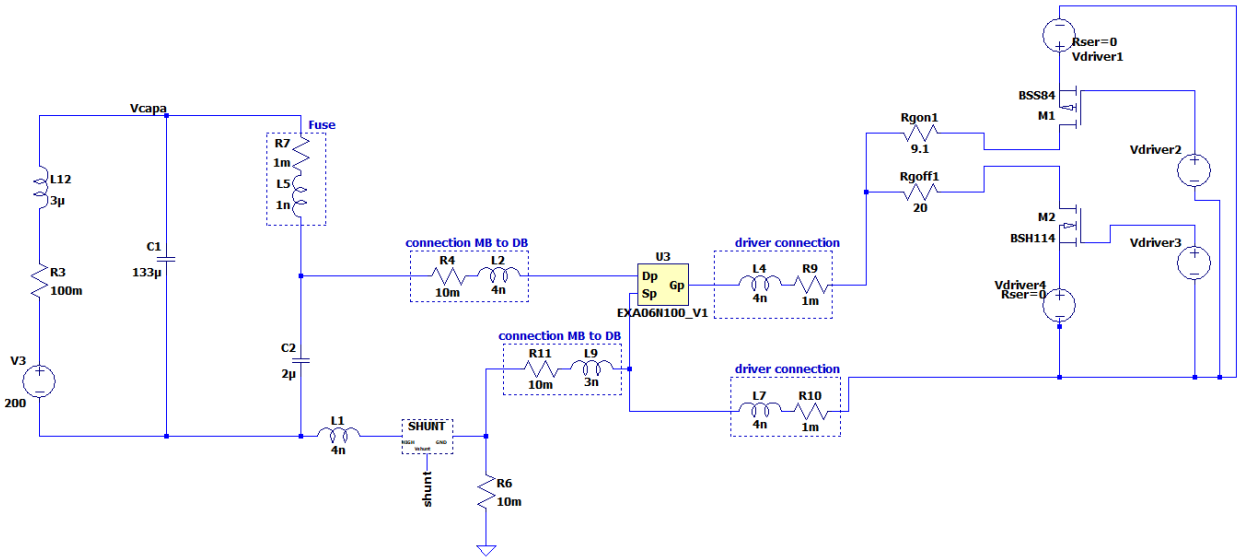

Figure 111: SPICE model of the whole test bench

2.2.2.2 SPICE Model of Passive Probes

Given the apparent disturbances, it is fair to wonder about the contribution of probes.
There are various probe models. In his thesis [134], K. Mbaitelbe uses the diagram shown below, including the values used to model the scope input, which will be reused in this thesis

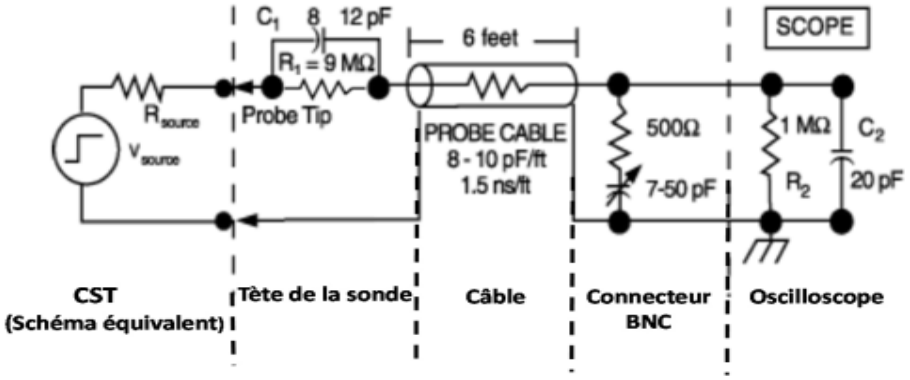

Figure 112: probe model from [134]

Ammous et al. in [144] go into a little more detail about the model used to simulate the impacts of the cable linking the probe to the oscilloscope. They use resistive, inductive and capacitive blocks as shown in the Figure 113 below.

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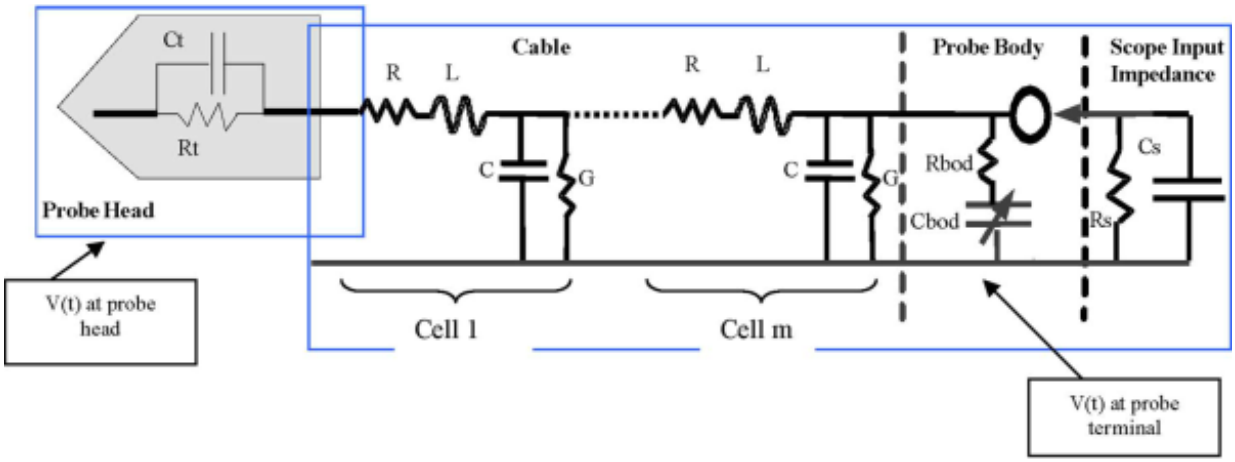

Figure 113: model of voltage probe from [19]

The authors of [144] specify in the table below the data they will use to model the Tektronix probe. The model of passive probe used, although different, is not fundamentally different and remains similar. As the values were not supplied by the supplier for the model of probe used in the manipulation, it was decided to use these values as a basis, as they were deemed to be consistent.

Parameters / Probe type	R1	C1	G1	L1	M : cells number	Models Parameters at Head or Body Probe	
Current Probe: Coaxial wire	0.0025m Ω	100pF	9ns	200nH	6	Shunt model : Rs=25m Ω Ls=1p H Cs=6.6µ F	
Voltage probe P6139A (TEKTRONIX)	260 Ω	38p F	1.5n S	540n H	14	-Body probe model: C_{bod}=12.6pF, R_{bod}=180Ω, - Head probe model: Rt=9M Ω, Ct=8p F	

Table 11: physical values of probes

Joao Soares de Oliveira in [72] uses the values in the table below to model the transmission elements relating to the cable linking the probe to the oscilloscope.

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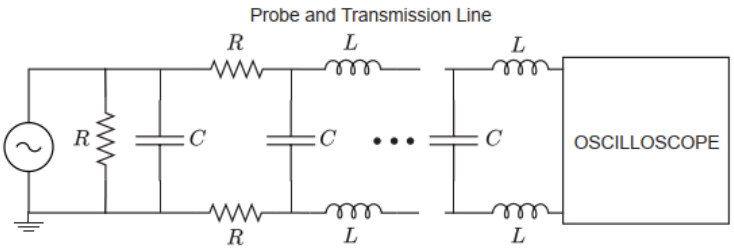

Figure 114: Transmission line model from [72]

Variable	Value	Unit	Description
C_{probe}	10	pF	Input Capacitor
R_{probe}	9	MΩ	Input Resistor
R_{cable}	150	Ω	Distributed Resistors
L_{cable}	237	nH	Distributed Inductors
C_{cable}	95	pF	Distributed Capacitors

Figure 115: used parameters for transmission line in passive probe model, from [72]

Using the various elements seen above, i.e. the line transmission elements, the probe head, the BNC connector and the oscilloscope impedance, the following scheme is designed below:

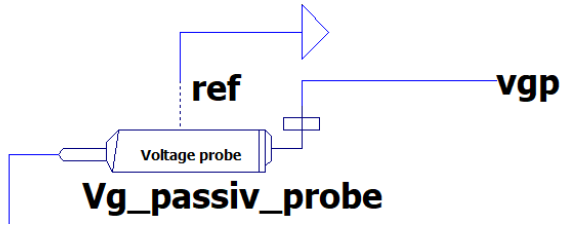

Figure 116: SPICE model of the passive probe with its components

The values of the various components making up the probe, chosen on the basis of the bibliographic data selected above, are explained in Figure 117.

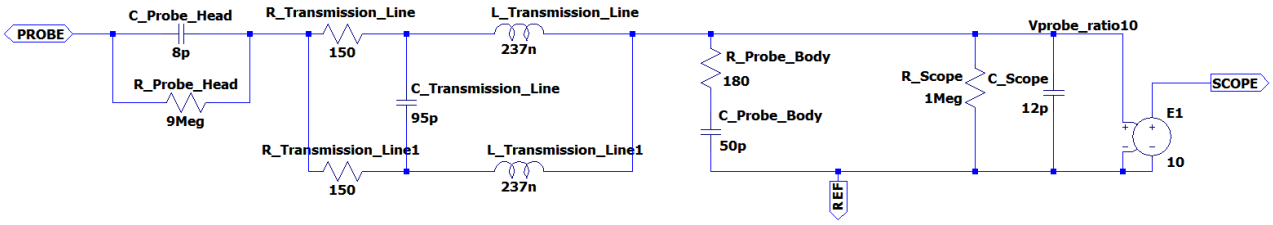

Figure 117: SPICE model of the passive probe Tektronix TPP0500 with its components

2.2.2.3 Observations of the V_{GS} Signal in Simulation

The simulation provides direct access to the gate of the device and source signals, without using probes, which is impossible in the real world. The probe model developed allows us to put in parallel what the oscilloscope would have given in reality. In Figure 118 while the pink signal, taken at the die terminals, shows only slight overvoltage, not exceeding +/- 10 V, the blue signal, taken at the output of the passive probe, is quite different, with more marked oscillations and overvoltage exceeding +40/-60 V. The model of device used in this simulation comes from the first supplier.

This reinforces the idea of taking particular care with the measurements and the equipment chosen. In particular, this will allow to put forward the idea of probe change. Those aspects will be investigated a little further on, in particular with the use of differential and optically isolated differential probes.

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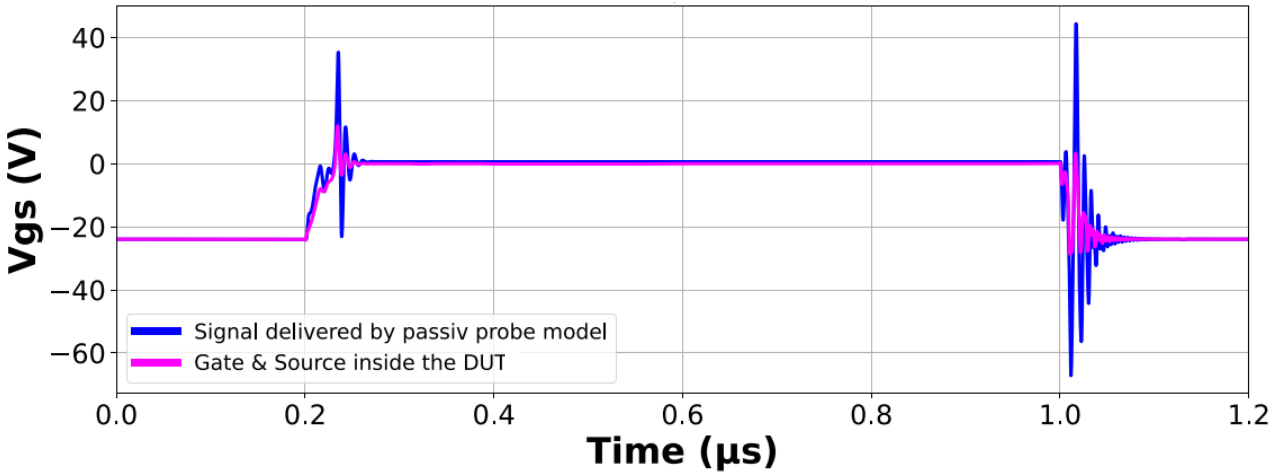

Figure 118: comparison of simulated V_{GS} signals from a passive probe (blue) or taken directly from the component terminals (pink)

In Figure 119, the turn-off section is zoomed in to show the differences between the V_{GS} signal measured at the component terminals and that measured using a passive probe.

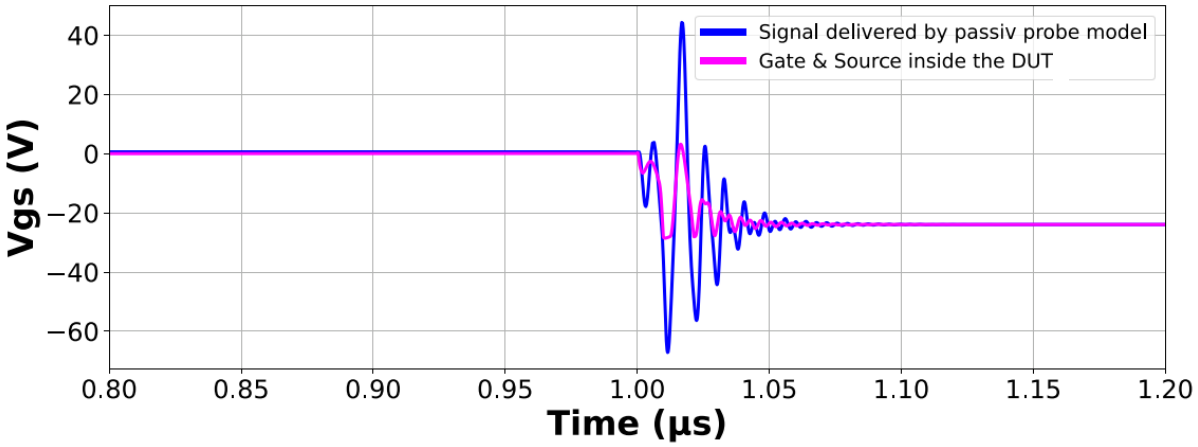

Figure 119: comparison of simulated V_{GS} signals from a passive probe (blue) or taken directly from the component terminals (pink) with a zoom during turn-off

These simulation results questioned the analysis of the signals observed via the probes. By means of this simulation, it can be stated that the signals observed at the output of passive probes do not necessarily describe what the component actually endures and therefore constitute a disturbance in themselves. Two questions remain unanswered at this stage and will be addressed experimentally. Are the signals observed by the probes really those experienced by the component? The accuracy of the signals observed by the probes can be legitimately questioned even if the probes do not artificially distort the signals.
To this end, a comparison of the various probes available has been carried out below.

The second question is whether the probes contribute to the disturbance. Does the probe produce a distorted signal or is it the probe that causes the disturbance and affect the behaviour of the component? To answer that, a experimental comparison was made with either all the probes connected, or only a single probe connected to a reference signal, to see whether or not their presence affects the operation of the bench.
The influence of probes at the experimental level is hence studied.

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2.2.3 Experimental Study on Impact of Probes

Given the uncertainties surrounding operation, and the simulation results demonstrating the impact of the measurement probes, various analyses have been carried out regarding the relevance of the probes used and their criticality.

The measurements are initially carried out with the probe reference attached to the probes themselves. Different configurations will be studied, with passive and active probes

2.2.3.1 Do Probes Cause Disturbances?

To study whether the presence of the probes alone causes disturbance, it has been decided to compare two configurations. The first situation consists of measuring with all the probes connected (*Figure 120* left - a). The second was to remove all the passive probes, with the exception of one, which was left connected to a reference signal allowing comparison between the two configurations (*Figure 120* right - b). The results about disturbances at turn-off are shown in Figure 121 below.

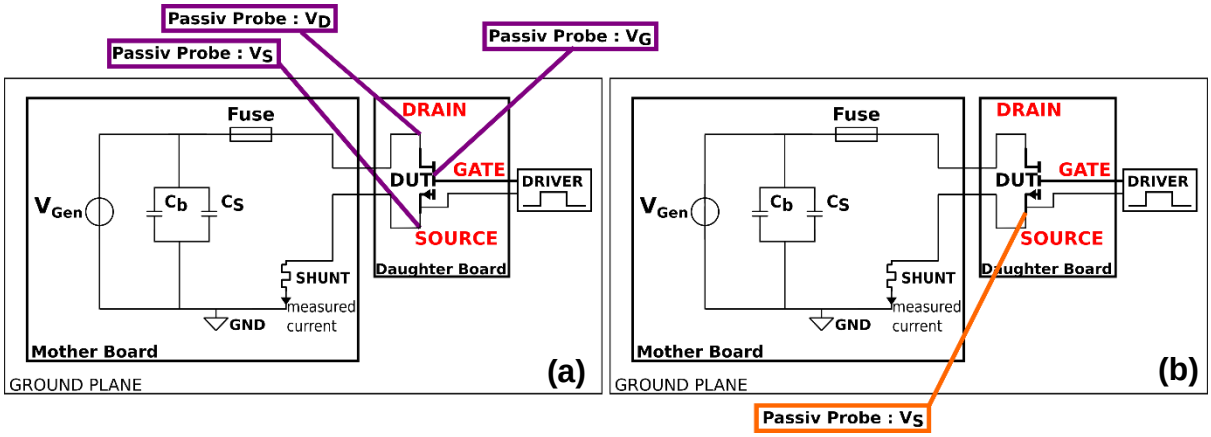

Figure 120: Two configurations of measurement, with all passive probes connected (left - a) and with only one connected to reference signal (right - b)

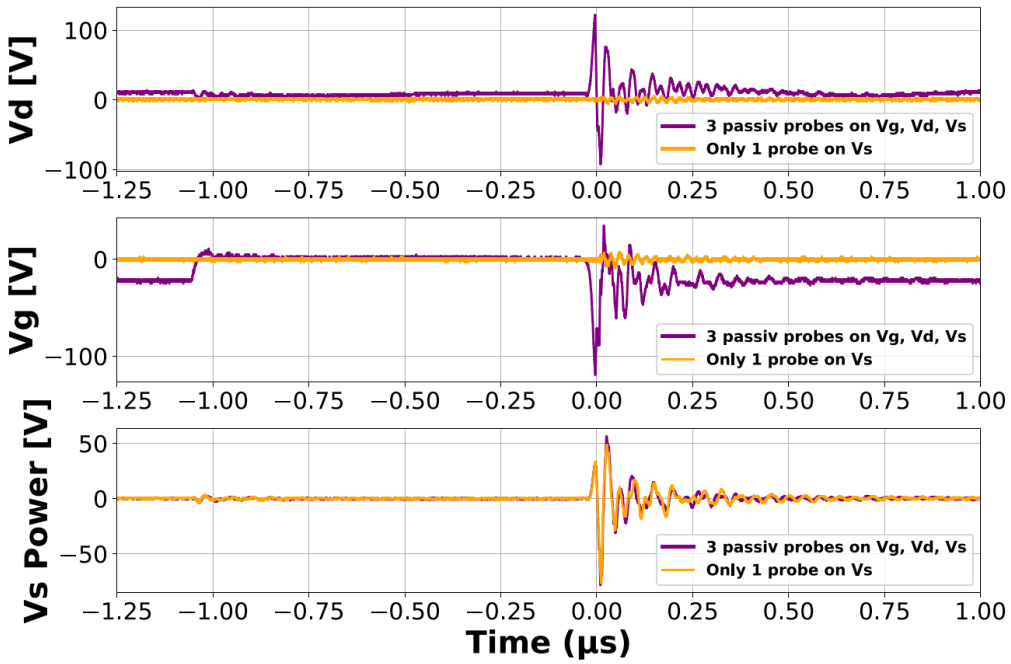

Figure 121: comparison of the Vs signal with or without the presence of all the probes

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It can be seen in the Figure 121 that the Vs signal, taken as a reference, is invariant whether all the probes measuring V_G, V_D and V_S are connected to the bench or only the one measuring Vs is present. Consequently, it can be deduced that the presence or absence of a passive probe (measuring V_G and V_D) has no significant impact and therefore that the passive probes cannot be the cause of the disturbances observed. Their relation to common-mode currents nevertheless remains concerning. It will be further studied, in particular by comparing differential probes and optically isolated differential probes [22].

Nevertheless, this configuration allows to realise that, contrary to all expectations, the potential Vs is not really stable, particularly during switching. During the first measurements, the V_{GS} and V_{DS} signal references were taken via the reference clamp attached to the probes and not via a specific measurement of the V_S potential, for example by means of a third passive probe.
It will be seen later that measuring the V_S signal via this reference clamp, rather than using a dedicated passive probe, is not insignificant.

The strong variation in the V_S signal also suggests the possible presence of common mode current.
A common mode current is a type of disturbance where current flows simultaneously on all conductors of a cable or circuit, often induced by electromagnetic interference (EMI) due to switching of devices or parasites. Unlike differential currents, which flow in opposite directions on conductors, common-mode currents flow in the same direction on all conductors in relation to earth. Common mode currents are often source of noise and disturbance in communication systems and sensitive electronic circuits[145–150].
It confirms the importance of carefully choosing the probes used in order to minimise the differences between the signals measured and the signals actually seen by the component, as the simulation study illustrated.

In view of the wide variation in the potential Vs, a connection to a large ground plane was studied, with the advantage that in theory it would be easier to stabilise the ground voltage rather than just bringing back the ground via the oscilloscope. The connection to this ground plane is made via a copper strip, as shown in the Figure 122.

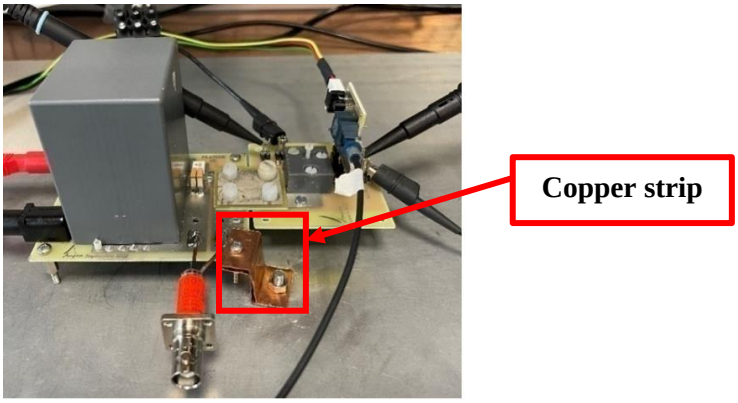

Figure 122: connection to the ground plan via a copper strip

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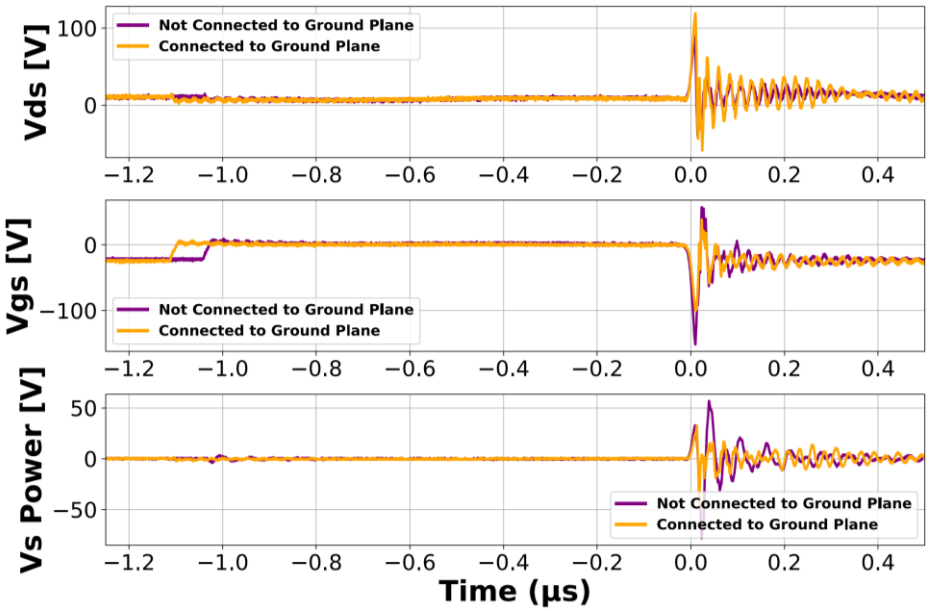

Figure 123: Impact of connecting (or not) the board to a ground plane

Figure 123 and Figure 124 show the results of this comparison with the V_{DS}, V_{GS} and Vs signals measured using passive probes. It can be seen here that the Vs potential is slightly stabilised, with a reduction in the amplitude of the oscillations once the first peak is reached and a lower amplitude for the first oscillations of the V_{GS} signal. Nevertheless, the V_G and V_D signals remain disturbed even though V_{DS} reaches only 10 V.

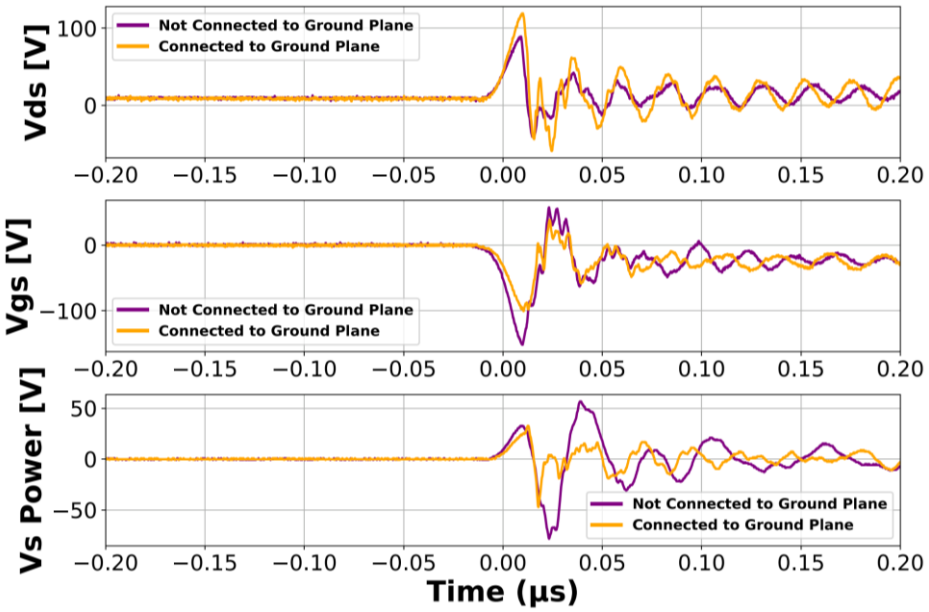

Figure 124: Zoom on Turn-OFF

Connecting to the ground plan is therefore not a sufficient solution. Other solutions need to be found. The solutions to be sought may lie in the measurement probes.

Figure 121 shows that it is necessary to have an accurate measurement of the V_S potential. In parallel with the use of two passive probes, it was decided to study the use of differential probes. Two active differential probes were studied, one with optical isolation. These probes have interesting common-mode current rejection ratios, particularly the optically isolated probe, reference IsoVu TIVH05.

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2.2.3.2 Comparison of Different Types of Probe

2.2.3.2.1 The Use of Passive Probes:

As explained before, the attention is now turned to the method of measurement. First it has been looked at the extent to which measuring with passive probes can be critical. These passive probes can hence be compared to active differential probes, whether optically isolated or not.

The first measurements carried out during the test of the experimental bench were made as follows: the probe is connected to the hot point, V_D or V_G in our case, and the reference is taken using the alligator clip (ground voltage) attached to the source potential.
The impact of this configuration is questionable, as the probe reference loop may have an impact on the measurements. The Rohde & Schwarz supplier website highlights this phenomenon by recommending that the reference of the signal has to be measured as close as possible to the passive probe to avoid parasitic oscillations, as shown in the Figure 125 below.

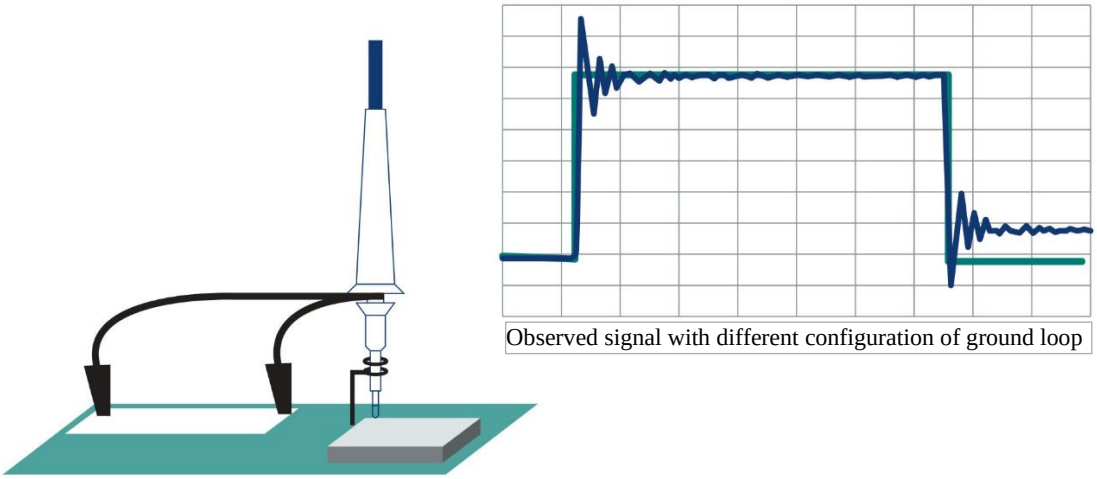

Figure 125: Three configurations of ground loop and impact on measurements of switching signals, from [151]

Tektronix also specifies this in [152]. A ground wire that is too long will increase the parasitic inductance and therefore risk causing oscillations and overvoltage, and therefore degrading the measured signals, as shown in Figure 126 .

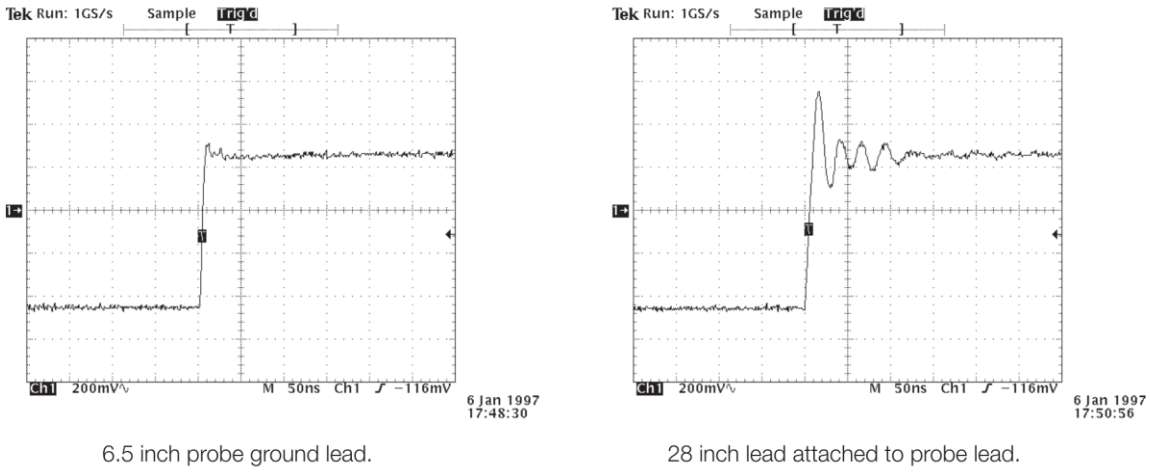

Figure 126: comparison for an extended (or not) length of the probe ground lead. The extended length causes ringing to appear on pulses from [152]

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At the experimental level, and with regard to the recommendations as explained in particular by Rohde & Schwarz, the source measurement is carried out as close to the signal as possible for both V_{DS} and V_{GS}, with measurement points at a short distance from the V_D and V_G measurement points as shown in Figure 127.

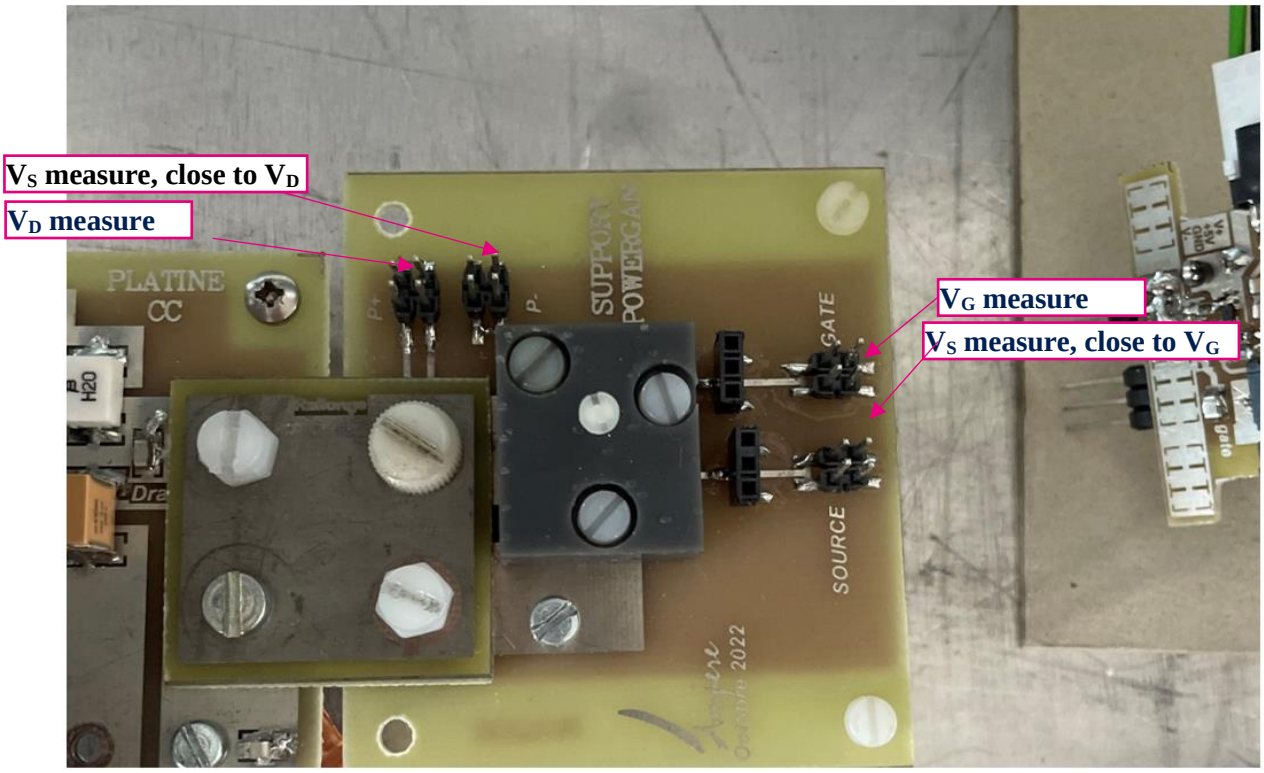

Figure 127: short distance for V_D and V_G measurements and their reference

Despite this, the fact that the V_S reference potential is measured as closely as possible to the measured signal does not prevent disturbances, as it has been seen above.
The impact of the reference loop attached to the probe is now studied.

In that present case, the circuit operates correctly at low V_{DS} voltages but oscillates catastrophically at higher voltages. It points out electromagnetic disturbances, at least of the electrostatic coupling type, linked to the increase in V_{DS} voltage.

Similar effects to those obtained experimentally can be found in the literature, for example undesirable switching as seen in Figure 128.

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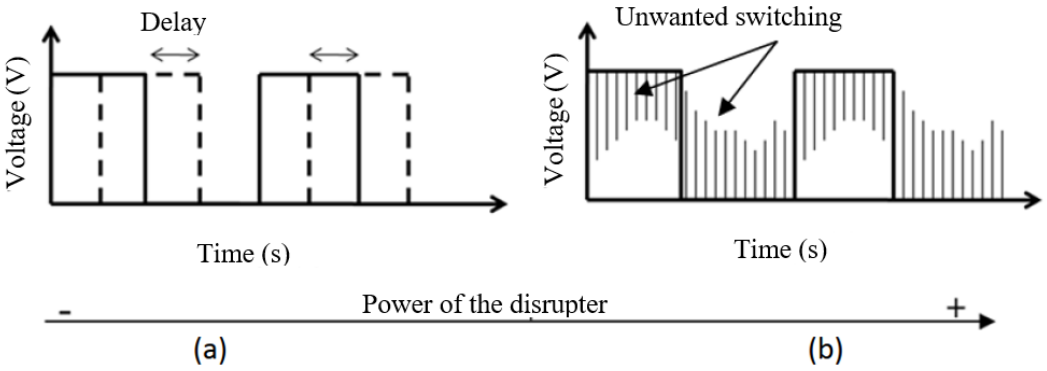

Figure 128: (a) Dynamic errors, appearance of delays, (b) Static errors, unwanted switching, from [153]

In [154], the authors observed disturbances similar to those observed experimentally at turn-OFF, with marked high-frequency oscillations. They also suggest a link with capacity, which will be discussed later in the thesis.

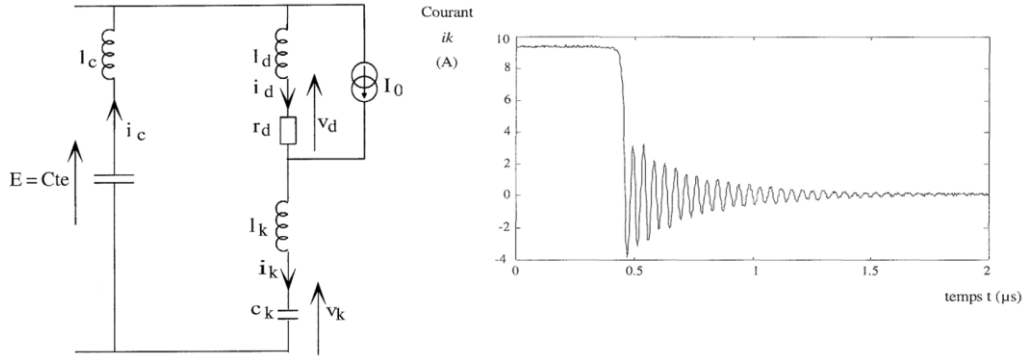

Figure 129: disruptive oscillations in the I_K current observed at the turn-off of a MOSFET transistor, from [154]

In normal operation, an electronic circuit will emit radiation, in particular via the PCB tracks or via the circuit components. Although this electromagnetic radiation is of low power, it can nevertheless alter signals and should therefore be taken into particular consideration. Once the wave has been emitted, it will couple to a circuit and disturb it [153].

In addition, connecting the reference legs of the probes at different points in the circuit is not trivial and amounts to short-circuiting this part of the circuit by connecting all these points to the oscilloscope ground.
The impact of the loop is non-negligible in terms of stability.

Two types of measurement are then carried out, the first with the reference attached to the passive V_{DS} probe, the second without. The V_{DS} signal is then measured using two passive probes and a MATH signal subtracting the measured V_D and V_S signals one from each other. The way in which the V_{GS} signal is measured is not changed, in order to see if the change in V_{DS} measurement configurations can alter the V_{GS} signal.
The study of the impact of this reference leg on signal disturbance was also analysed during the study of normally-off components. The optimisation of the test bench made it easier to identify the disturbing effects from probes. The results presented below are those relating to this study of normally-off components, with in particular the major advantage of using an optically isolated differential probe for V_{GS} measurement.

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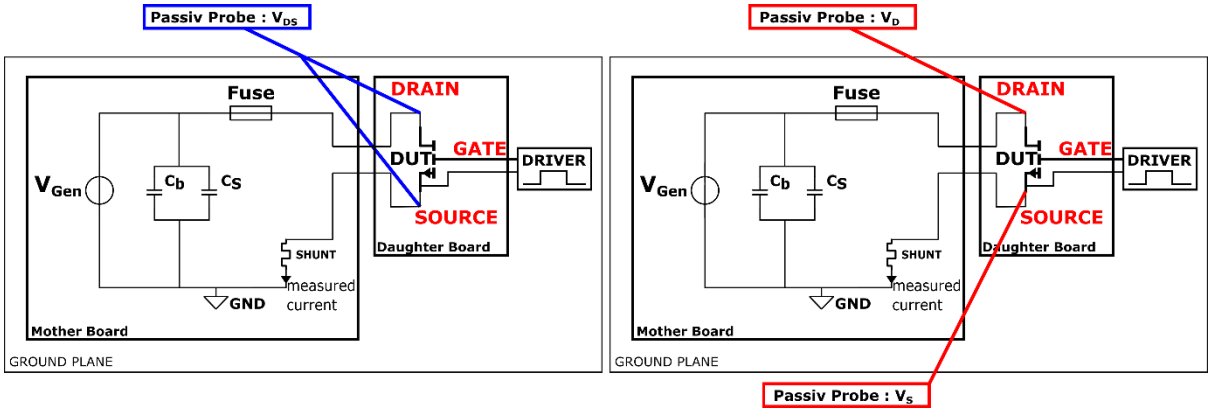

Figure 130: scheme of the two configurations of measurement

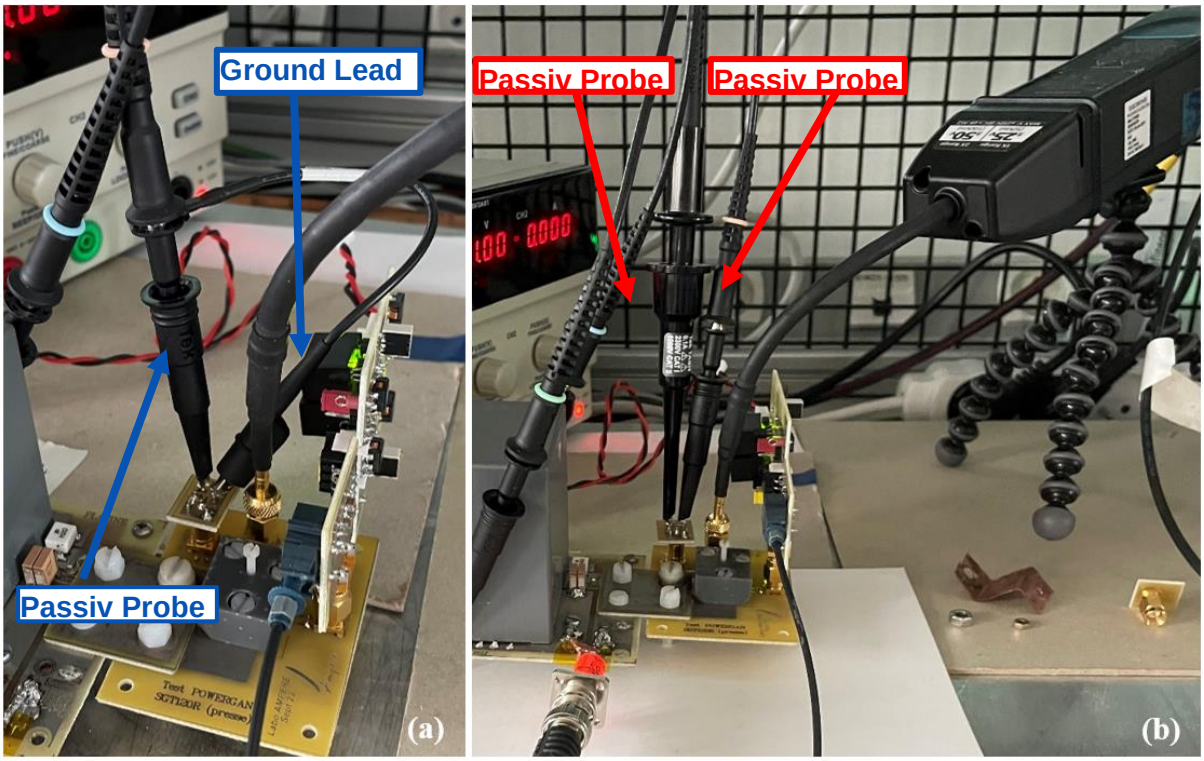

Figure 131: (a) passive probe with its ground lead, (b), two passive probes measuring V_D and V_S

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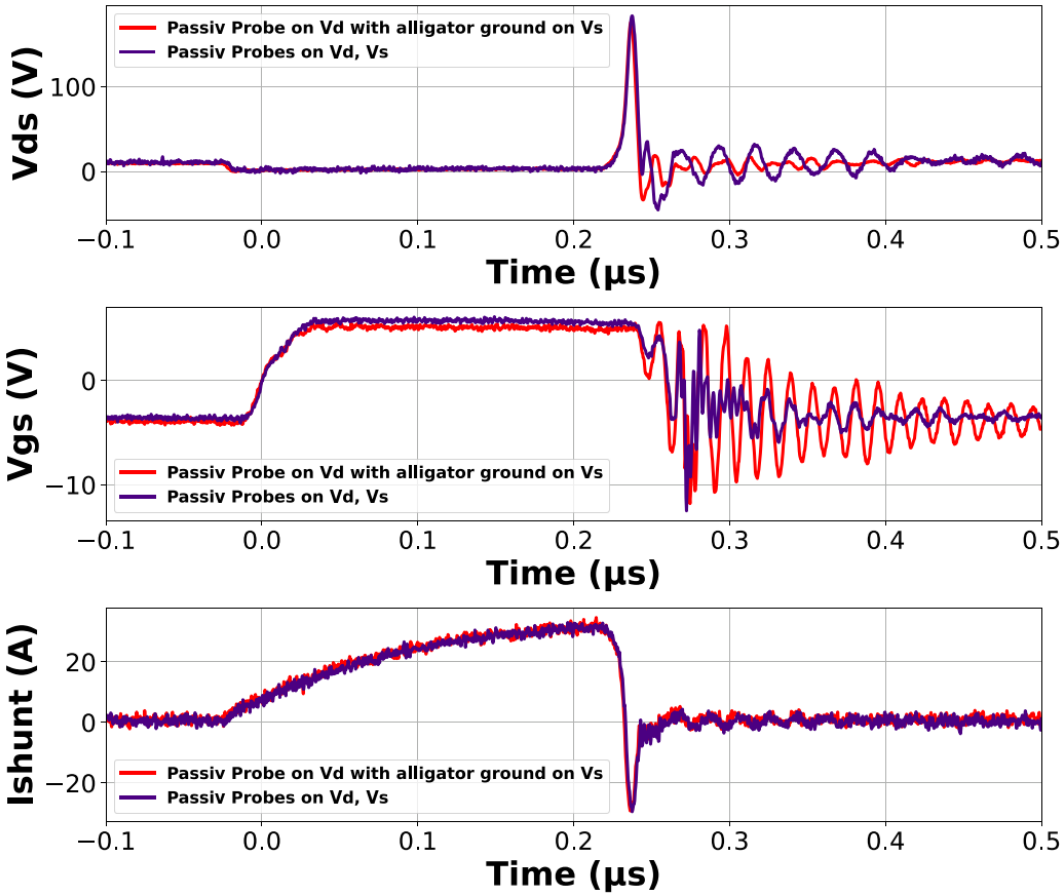

Figure 132: Impact of the ground lead on measurement

The Figure 132 shows the impact of the reference attached or not to the passive V_D probe. Whether the V_{DS} signal is measured with the reference tab attached to the measurement probe or via two passive probes (*Figure 130*) does not strongly change the shape of the V_{DS} signal. On the other hand, it can be seen to what extent the V_{GS} signal is clearly affected, with the appearance of ringing phenomena that are not negligible when the V_{DS} is measured using a probe with a ground lead attached to it.
In the end, it can be argued that it is the radiation caused by the grounding loop of the probe measuring the V_{DS} signal that degrades the V_{GS} signal, which remains unchanged in terms of measurement equipment. This type of disturbance can naturally be linked to common mode current.

In conclusion, current supplier recommendations are not applicable to GaN components. Not only must the length of the reference measurement wires be reduced as much as possible, but in the present case of study of GaN components, with their very high switching speeds, this reference wire must even be eliminated. The V_{GS} and V_{DS} signals can therefore only be measured by using a passive probe to their reference. Tektronix has well understood it for high voltage measurements. Similar protocol could be relevant in low voltage measurement with GaN devices.

Different measurement probes are then possible; coupling two passive probes and producing a MATH signal on the oscilloscope as was done in the previous test, proving the deleterious nature of the passive probe's ground lead. The other solution is to use a differential probe, which will be explained below.

2.2.3.2.2 The Use of Differential Probes

As previously stated, the rapidity of component switching and the disturbances visible on the short-circuit bench are such that this leads towards the use of differential probes, with increased common-

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mode rejection capabilities compared with simple passive probes. In general, differential probes also exhibit lower input capacitances.

Two differential probes are studied here. Firstly, a Tektronix high-voltage differential probe, part number THDP0100, and an optically isolated differential probe (IsoVu), also from Tektronix, part number TIVH05.

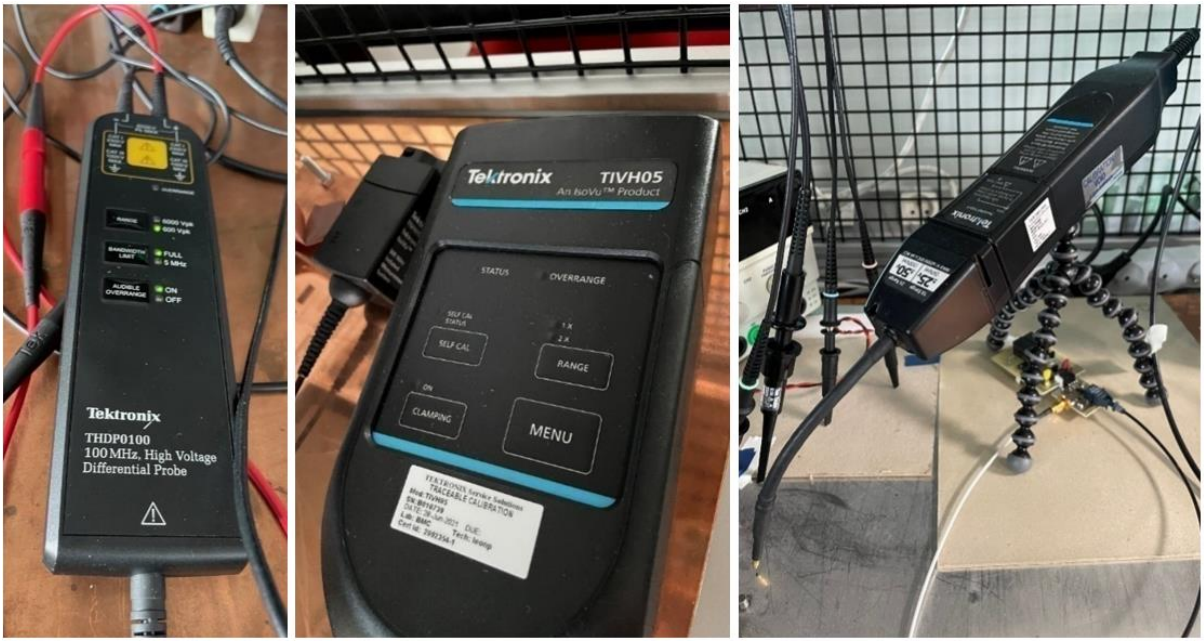

Figure 133: Differential probe (left) and IsoVu probe (middle and right)

The common mode rejection ratio (CMRR) is 26 dB for the THDP0100 differential probe, and around 100 dB for the optically isolated differential probe.

However the limit of the differential probe is its bandwidth of only 100 MHz. In comparison, the Isovu differential probe has a higher bandwidth, up to 500 MHz. Moreover the main advantage of the IsoVu probe is its high level of galvanic isolation (optical isolation). This ensures that, during measurement, the DUT remains totally isolated from the oscilloscope, which greatly helps to reduce common-mode current flow. [155]. Different connectors are available for the IsoVu probe depending on the voltage range to be measured, as shown in the Figure 134.

Type of Probe	**Reference**	**Bandwith**	**Attenuation (CMRR at 100 MHz)**	**Maximum Voltage**
Passiv Probe	TPP0500B	500 MHz	0 dB	300 V
Differential Probe	THDP0100	100 MHz	26 dB	6 kV
IsoVu Differential Probe	TIVH05	500 MHz	100 dB	5 kV (depends on the top sensor)

Table 12: Different types of compared probes

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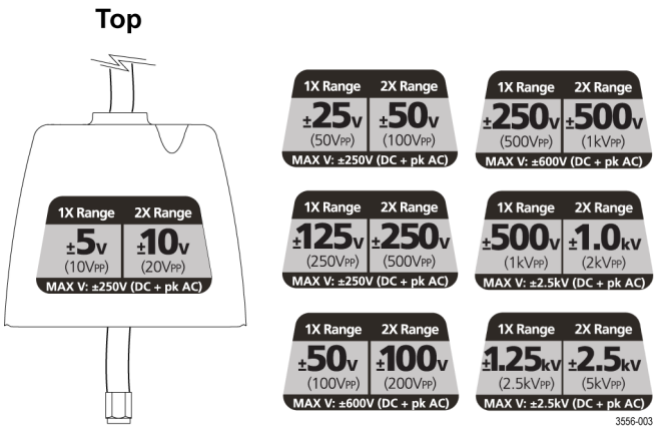

Figure 134: Various top sensor for IsoVu probe

As the IsoVu probe connectors are specific to the SMA standard, adaptors have been made. On future boards, the connectors will be directly integrated in SMA for probes and MMCX for the driver connection.

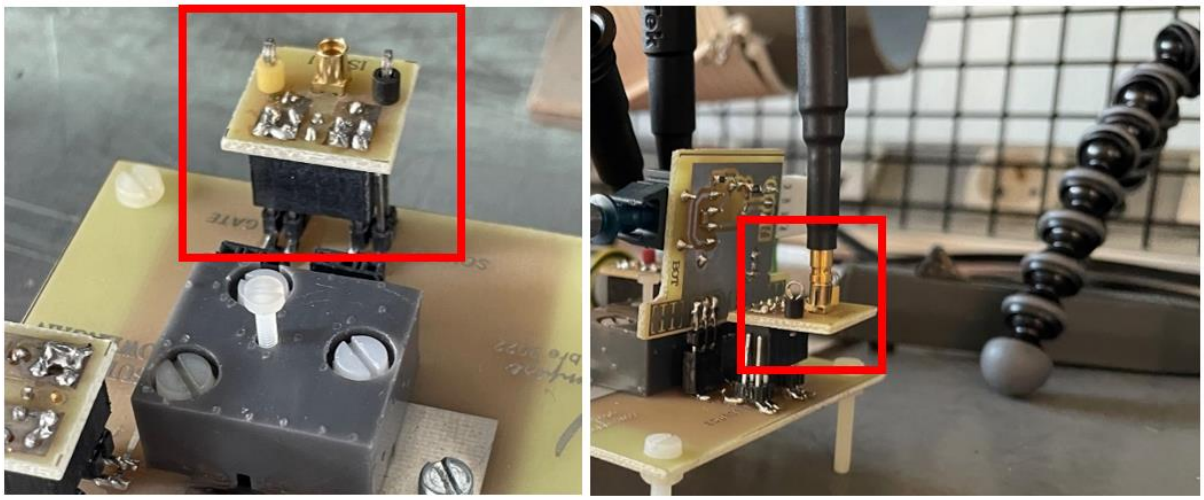

Figure 135: Details of SMA adaptor

Given the voltage levels to be respected, the V_{GS} signal is considered the most critical. On normally-on components, the limits of V_{GS} signal cannot go below -50 V. In previous tests, the oscillations were of such amplitude that they were close to -100 V, which is unthinkable for such a signal. In addition, the V_{GS} signal controls the transistor, making all the more critical. It was therefore decided to compare the different probes on this signal.
The results are unambiguous but do not go in the same direction as it might have been expected.

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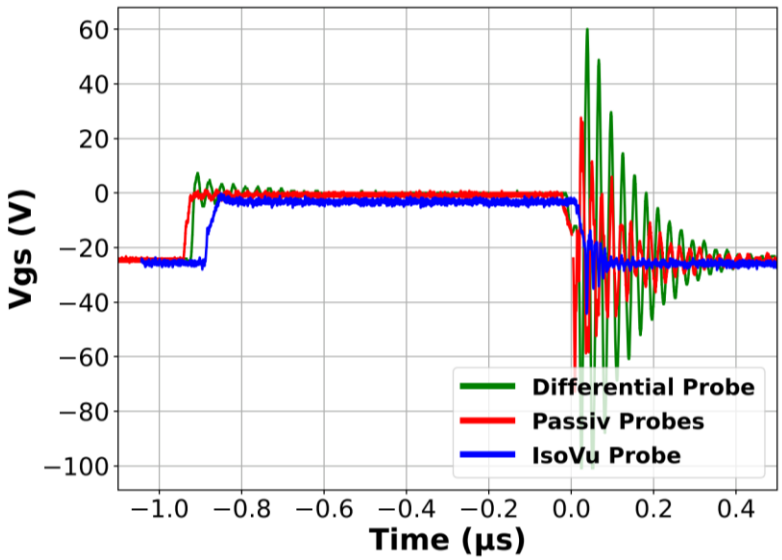

Figure 136: Comparison of V_{GS} signals measured with different type of probes

As it can be seen in Figure 136, the differential probe is far from being better than the combination of passive probes. It is even the worst configuration. This can be explained by the electronic box that manages the differentiation of the two measurements. Electromagnetic disturbances would therefore have an impact on this box and therefore on the measurements. If the differential probe has a non-negligible CMRR, the needed electronic box adds a lot. Hence it makes the use of this probe irrelevant. In contrast, the IsoVu probe, with its increased ability to reject common modes, delivers the most stable form of signal. It is the probe of choice for measuring the V_{GS} signal.

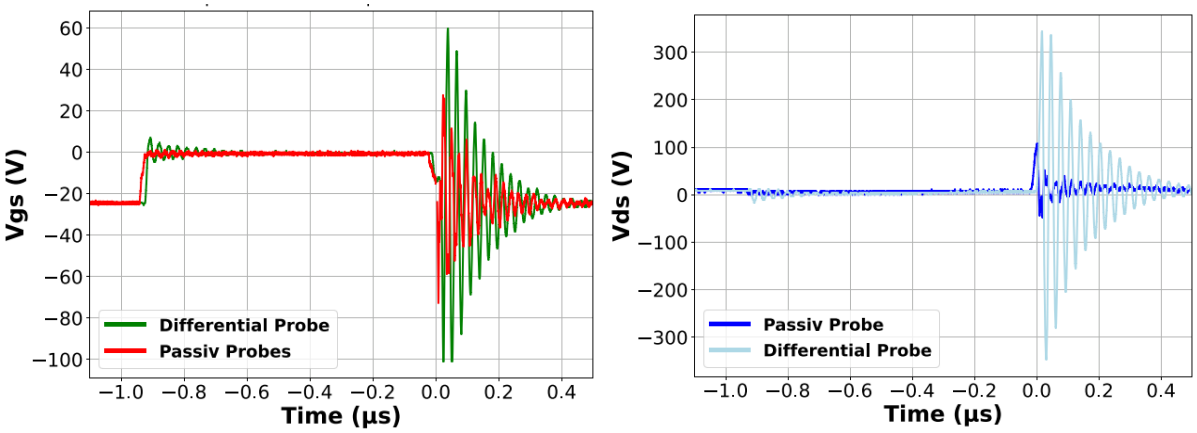

Figure 137: Comparison between differential probes and passive probes for V_{GS} (left) and also V_{DS} (right)

Measurements are now repeated on both the V_{GS} signal and the V_{DS} signal. As only one IsoVu probe is available and is now assigned to measure V_{GS}, its comparison is not carried out here. The V_{DS} signal is measured using either two passive probes and a MATH, or a differential probe.
If the use of the differential probe on the V_{GS} signal already showed little interest with the comparison in Figure 136, the measurement of the V_{DS} signal in Figure 137 is sufficiently eloquent as to the impossibility of using this type of probe on the short-circuit bench, given the amplitude and oscillations observed.
As a result, the probe strategy is now as follows:

Signal	**Type of probes**
V_{GS}	IsoVu probe
V_{DS}	Two passiv probes and a math function from oscilloscope

Table 13: probe strategy after comparison of active and passive probes

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2.2.4 Last Optimization: Current Sensing

Although the shunt is the solution of choice for measuring short-circuit current, it is not without its shortcomings, particularly in terms of parasitic inductance.
In parallel with the optimisation of the probes, a discussion was held on the possible optimisation of the shunt. The discussion focused on two aspects. The first aspect is to find out whether there is a preferable position for the shunt ground, on the device side or on the power source side. The second is to reduce the loop inductance of the shunt as much as possible, using copper tape and capton-type insulating tape. There are five possible configurations, summarised in the table below.

Type of configuration	Technical choices	Measured signal
Config. 1	Shunt mass side of Power source ground	I_D - I_{CM}
Config. 2	Shunt mass side of device	I_D
Config. 3	No shunt	-
Config. 4	Optimized shunt, mass side of power source	I_D - I_{CM}
Config. 5	Optimized shunt, mass side of device	I_D

Table 14: different configurations to optimize current sensing

Configurations 1 and 2 differ only in the position of the shunt ground and are explained in *Table 15*. Configurations 4 and 5 adopt the same strategy, but use a shunt with reduced parasitic inductance. Configuration 3 is unique in that it tests without the soldered shunt, a wire replacing it.
It has to be noted in configurations 1 and 4, as the cooper tape is screwed before the shunt. As a consequence, the measured signal is restricted to the short-current minus the value of the common mode current. In configurations 2 and 5, the shunt tape is screwed after the shunt. The measured signal is hence the total short-circuit current the device undergoes.

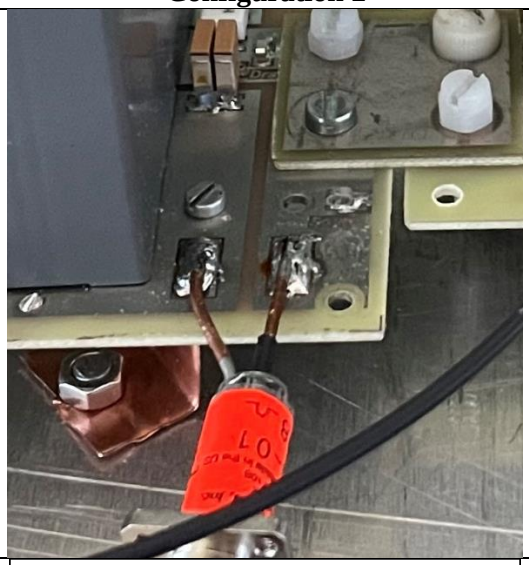
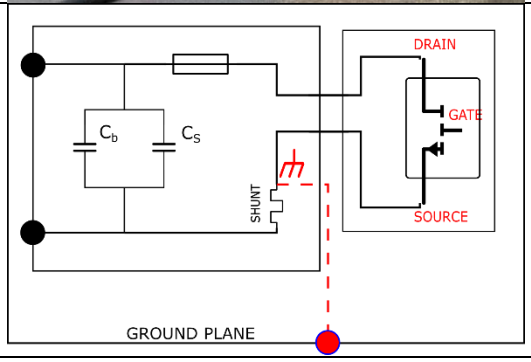
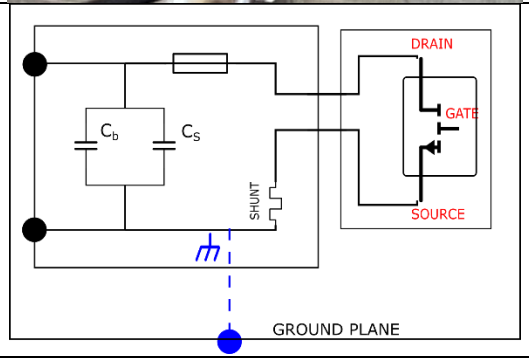
Configuration 1	Configuration 2
	
	

Table 15: Configurations 1 and 2 with their electrical scheme

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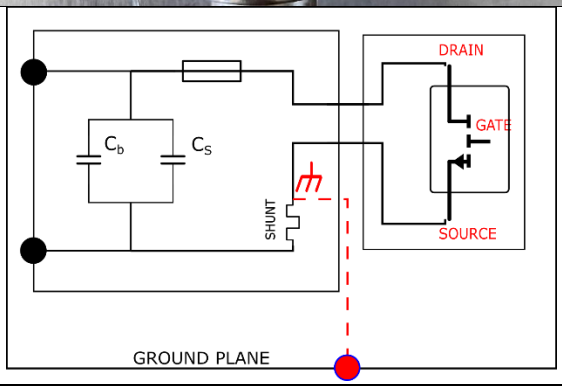
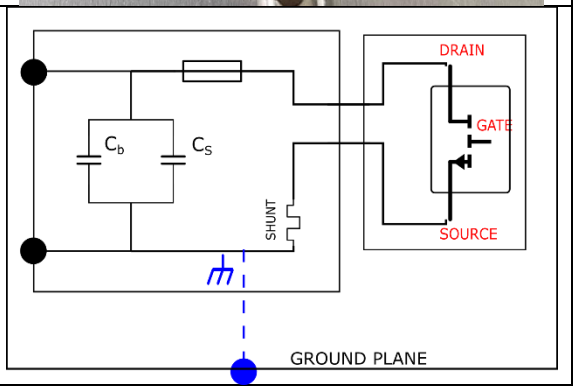
Configuration 4	Configuration 5
	

Table 16: Configurations 4 and 5 with their electrical scheme

The different possible configurations give the results shown in Figure 138
For better readability, the turn-off zone is zoomed on Figure 139. Measurements were taken at this point using passive probes for the V_{DS} signal and the IsoVu probe for the V_{GS} signal. The difference in terms of conduction duration was due to the driver, it has been corrected with the 2024 version of driver.

It can be noticed that the direction of the shunt has little influence on the overvoltage seen by the V_{DS} signal. No difference can be made between dark green versus light green curves or red versus purple curves. Consequently, positioning the shunt ground on the device side or the power source ground side has little impact. On the other hand, reducing the loop formed by the shunt legs reduces the overvoltage of the V_{DS} signal by 50 V.
The case without the shunt, due to the absence of any apparent inductance linked to this element
The V_{GS} signal, on the other hand, remains invariant, which confirms that adding or removing the shunt only affects the parasitic inductances of the power loop and therefore the overvoltage on the V_{DS} signal. For this reason, optimisations on the probes were carried out afterwards, as described above.

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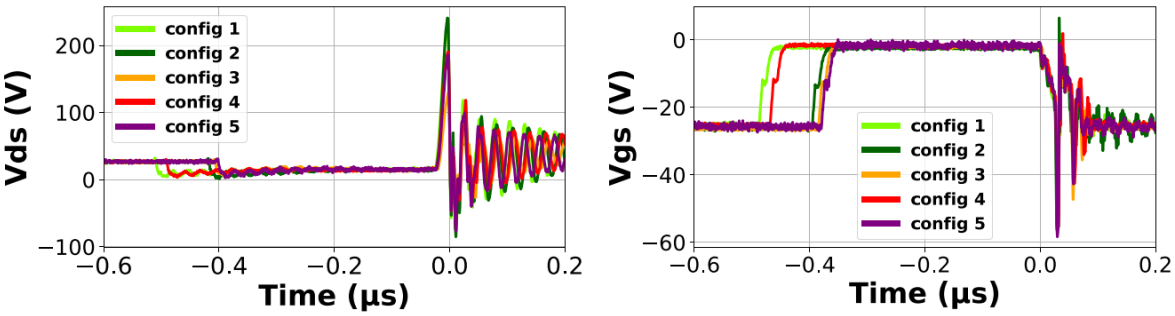

Figure 138: V_{DS} (left) and V_{GS} (right) switching voltages for different configurations of the shunt.

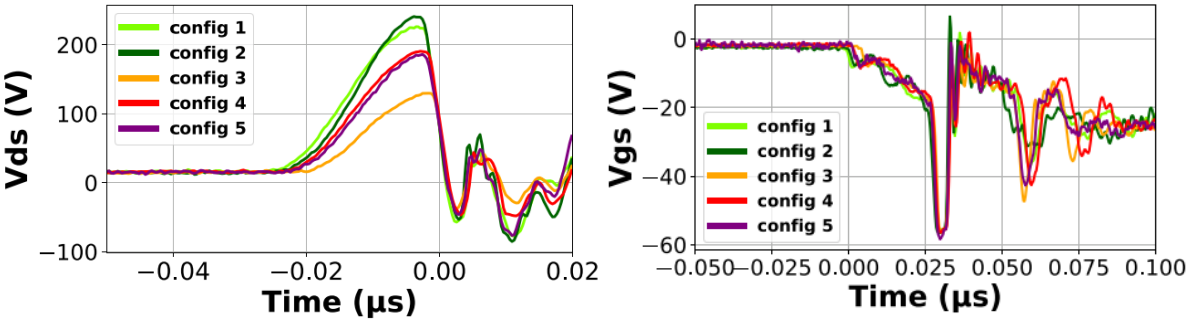

Figure 139: zoom on turn-off for V_{DS} (left) and V_{GS} (right) signals

The absence of impact on the direction of connection of the shunt and therefore of its ground was tested again later, for much larger drain-source polarisations, as shown below Figure 140 with a drain-source polarization of 200 V. It gives the same conclusion as V_{GS} and V_{DS} are stable, particularly during the turn-off and the position of the ground of the shunt does not have any relevant impact.

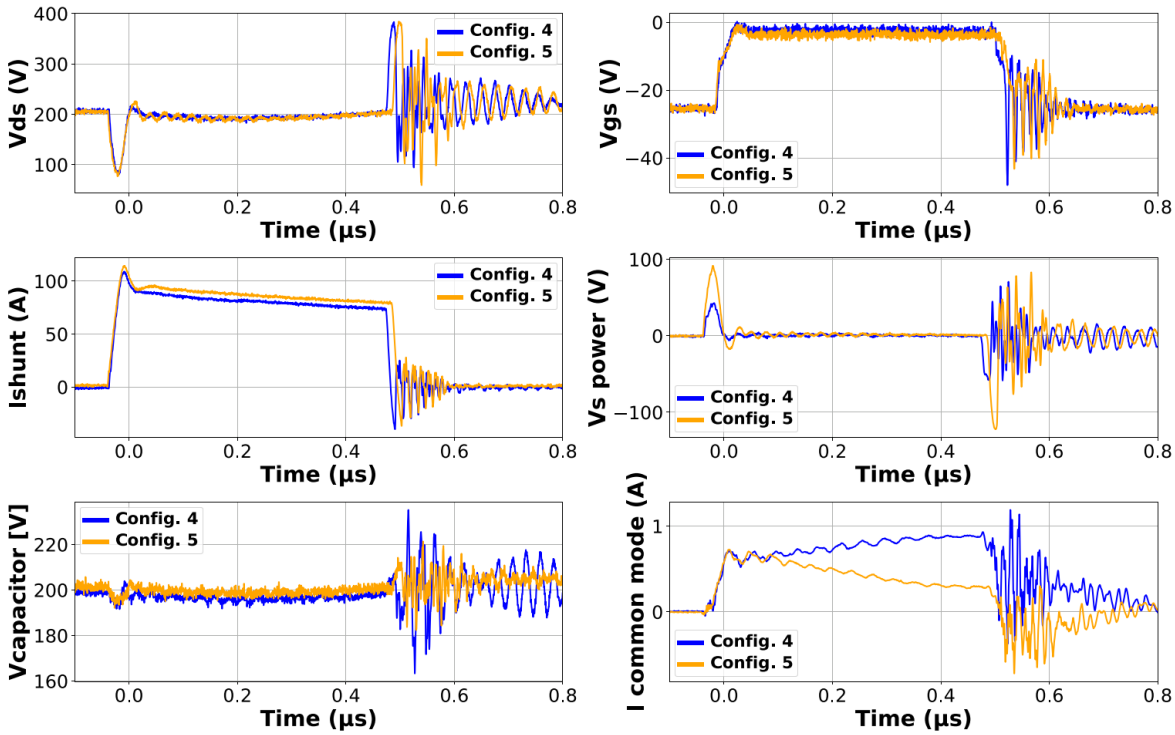

Figure 140: Comparison of the impact of configurations 4 and 5 for a, increased V_{DS} = 200 V

The various optimization with the implementation of measurements disturbing the experimental bench as little as possible and delivering signals as close as possible to what the component actually sees, coupled with the reduction of the parasitic inductance of the shunt, have enabled the experimental bench to be stabilised and have made it possible to gradually increase the voltages and to carry out non-

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destructive repetitive short-circuits for a drain-source bias of 200 V. The shunt configuration number 5 has been kept. Other tests become able to be conducted such as test for a V_{DS} = 300 V (Figure 141) and for an increased conduction time (Figure 142) . A progressive rise in V_{DS} voltage can be seen in Figure 141 up to a successful test for V_{DS} = 300 V. The Figure 142 shows the increase of conduction time with a breakage of the device for a test duration of 1 µs. The different types of breakage and theirs analyse are explained in the last chapter.

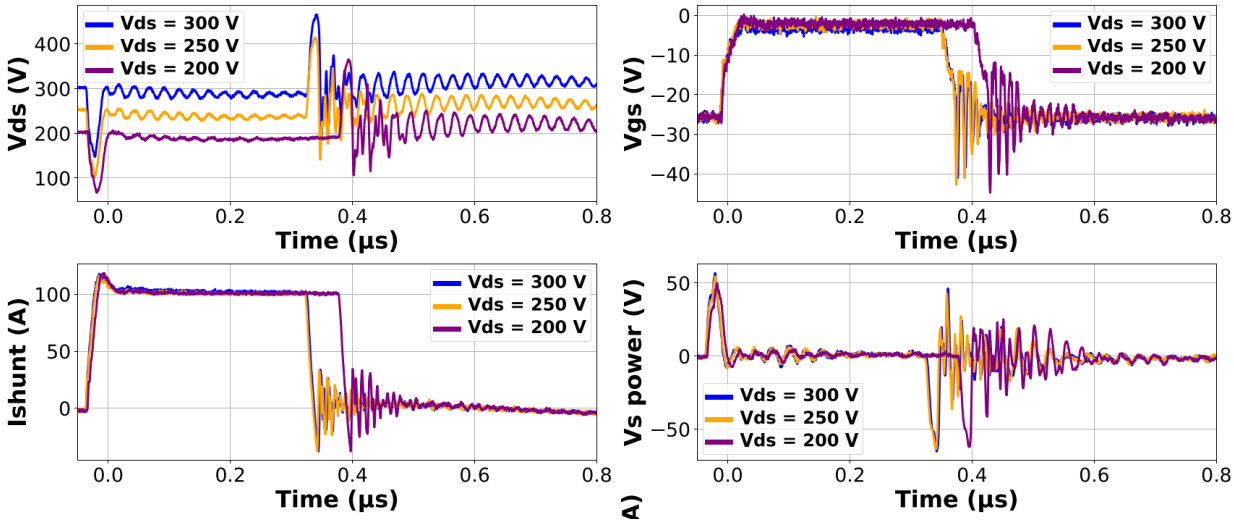

Figure 141: waveforms for an increased V_{DS} up to 300 V

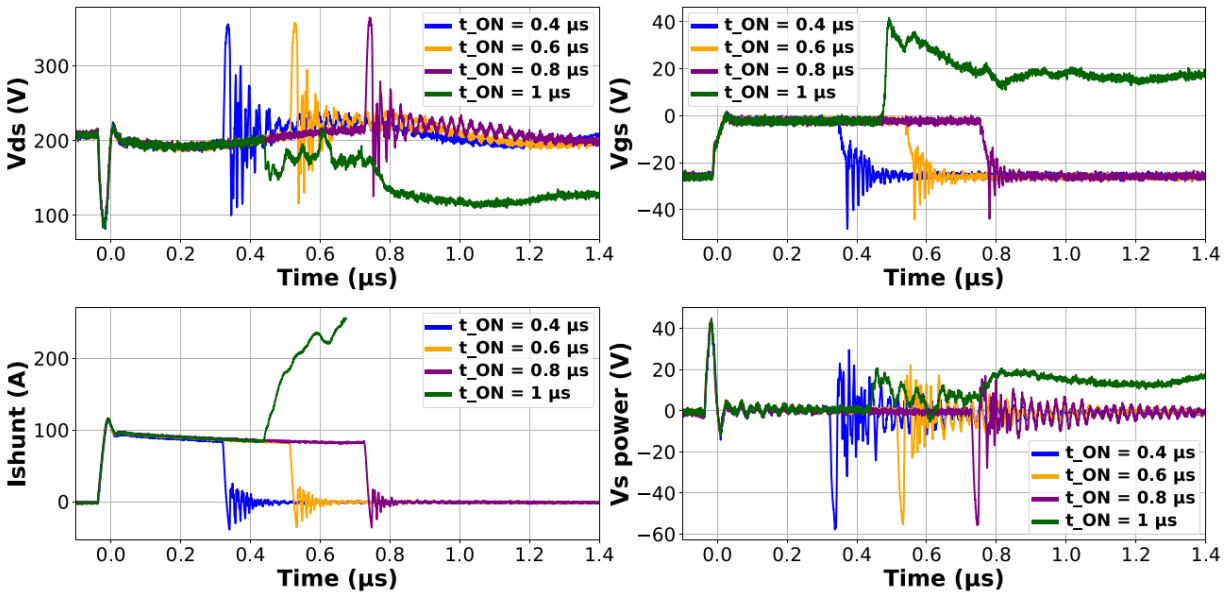

Figure 142: waveforms for an increased time of conduction and finally the breakage of the device

Thanks to appropriate measurement methods and probes, coupled to a reduction of shunt parasitic inductance, the bench has been optimised and the study of the first components, i.e. the normally-on components, can begin with the set-up of repetitive short-circuit cycles interspersed with characterisation at the B1505A.
The study was then extended to normally-off components, consisting of p-GaN structures from two different suppliers.

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2.3 Optimisation of the Test bench for Normally-Off Components

2.3.1 First Tests, and All Over Again

As it has been said in the first part, there are three normally-off components to be studied, summarized in *Table 17*. The cascode components come from the same supplier (supplier 1) as the normally-on (d-mode) components and the p-GaN.

Component	Supplier	V_{th}	V_{GS} OFF / V_{GS} ON	Id	R_{DS}_ON
Cascode	Supplier 1	1.8 V	- 3 V / +6 V	10 A	190 mΩ
p-GaN	Supplier 1	1.8 V	- 3 V / +6 V	15 A	120 mΩ
p-GaN	Supplier 2	1.7 V	- 3 V / +6 V	11 A	150 mΩ

Table 17: main properties of the three tested normally-off components

2.3.1.1 First Tests on Cascode Components

The footprint is identical for the d-mode component studied before or the cascode component. The initial daughter board is therefore retained, with only the voltage levels applied to the device gate being changed as explained in Table 17. Tests for V_{DS} = 100 V and V_{DS} = 200 V are carried out and give the results shown in Figure 143 below.

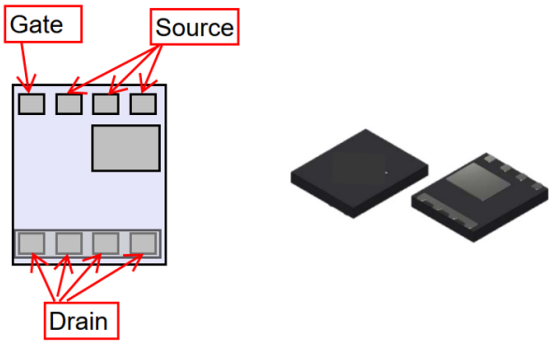

Figure 143: Footprint of the cascode device

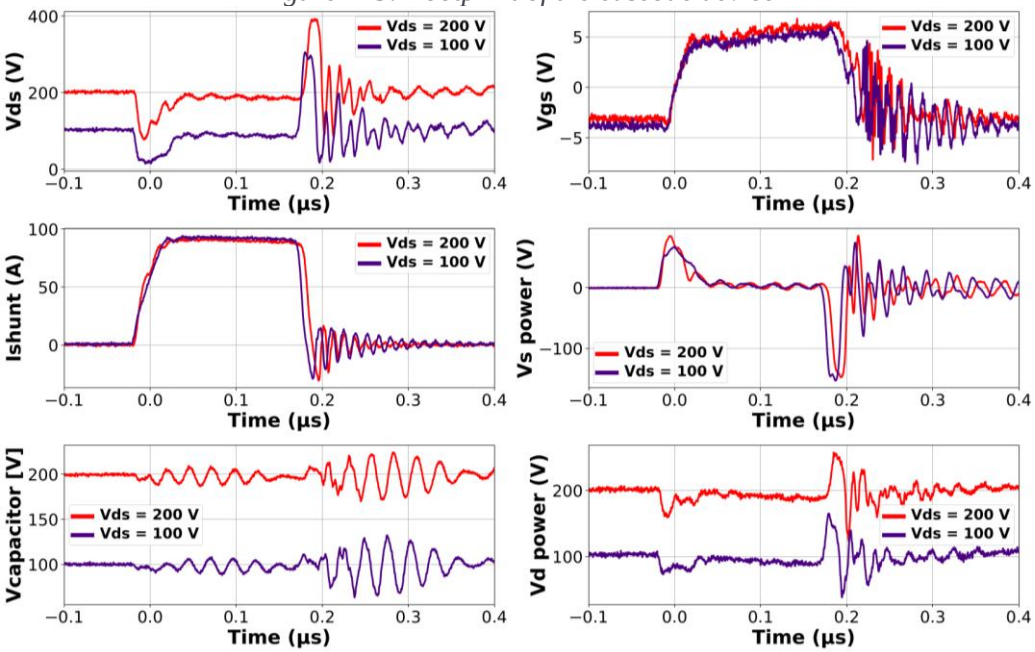

Figure 144: firsts tests on cascode components, on Test-Board 2023

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For both V_{DS} = 100 V and V_{DS} = 200 V, the signals are stable. The V_{GS} signal shows an area of disturbance at the turn-off, but at this stage the signals are considered to be acceptable and repeat tests are conceivable.

The tests continued with p-GaN components from suppliers 1 and 2.

2.3.1.2 Tests on p-GaN Components

2.3.1.2.1 Supplier 1

For the first supplier, identical to the cascode and normally-on devices, initial tests for V_{DS} = 100 V and V_{DS} = 200 V give the results shown in Figure 144 below. As with the cascode components, there are non-negligible overvoltage on the V_{DS} and V_{GS} signals. The V_{GS} signal is disturbed to a non-negligible extent during the turn-off, although this does not prevent the repeatability of the short-circuit tests as shown in Figure 145 and Figure 146. It will be seen later that the p-GaN components from the second supplier do not behave in the same way at this point.

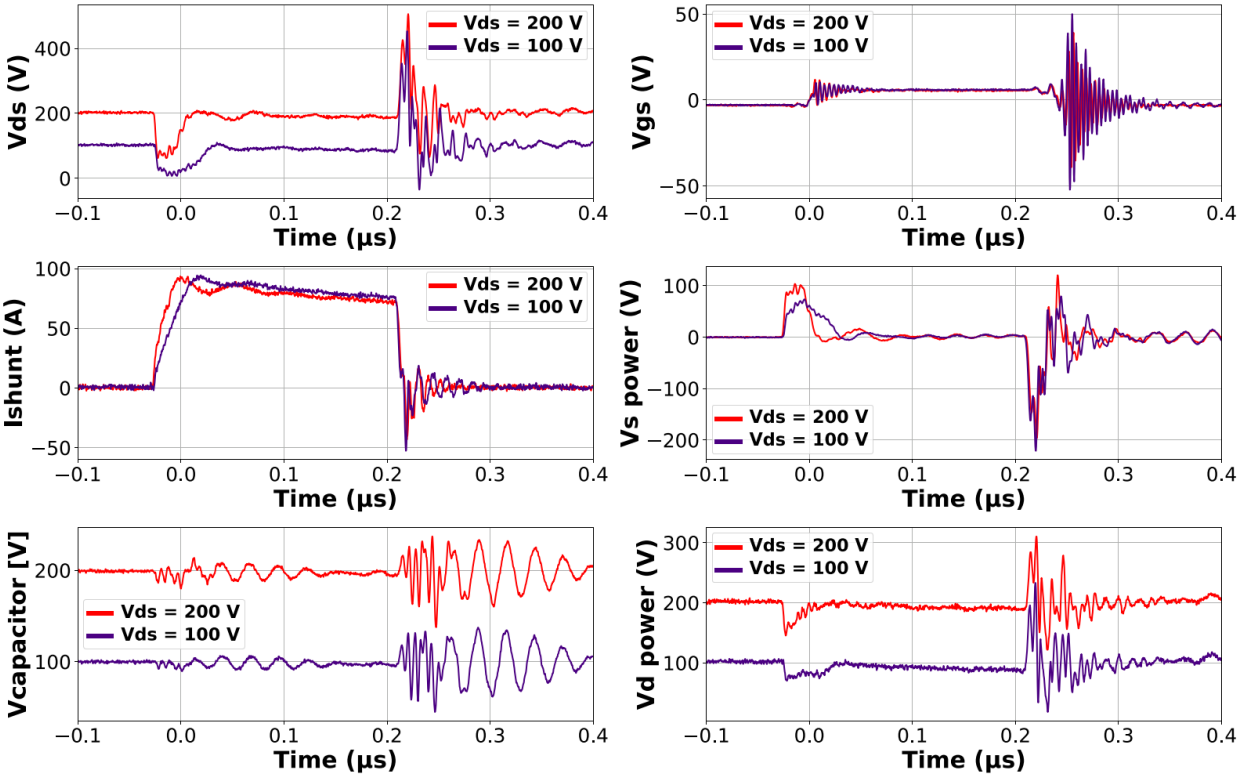

Figure 145: Waveforms for p-GaN component from supplier 1, on Test-Board 2023

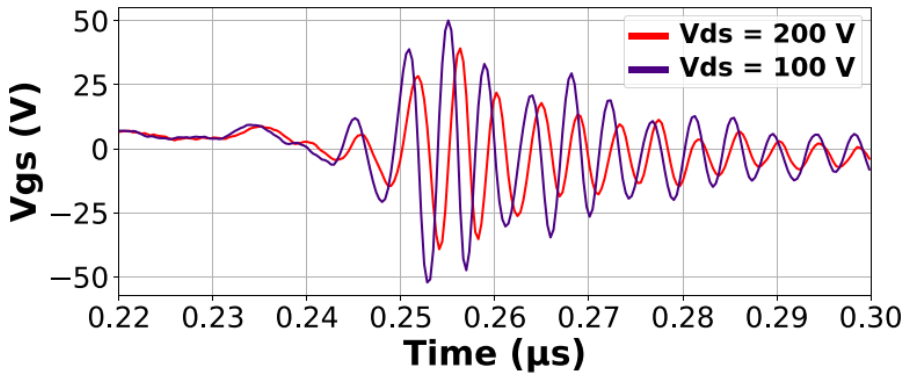

Figure 146: zoom on V_{GS} turn-off for p-GaN component from supplier 1 on 2023 test-board

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2.3.1.2.2 *Supplier 2*

With regard to the p-GaN components from the second supplier, although the tests for polarisations V_{DS} = 100 V gave signals similar to those from supplier 1 as it is shown in Figure 147, for higher polarisations, such as V_{DS} = 200 V (Figure 148), the disturbances in the V_{GS} signal were such that they prevented normal operation of the component, preventing it from stopping driving and eventually causing it to break. Oscillations and overvoltage are particularly noticeable on the V_{DS} (V_{DS} > 650 V) and V_{GS} signals, with values well above the acceptable limits specified by the supplier.

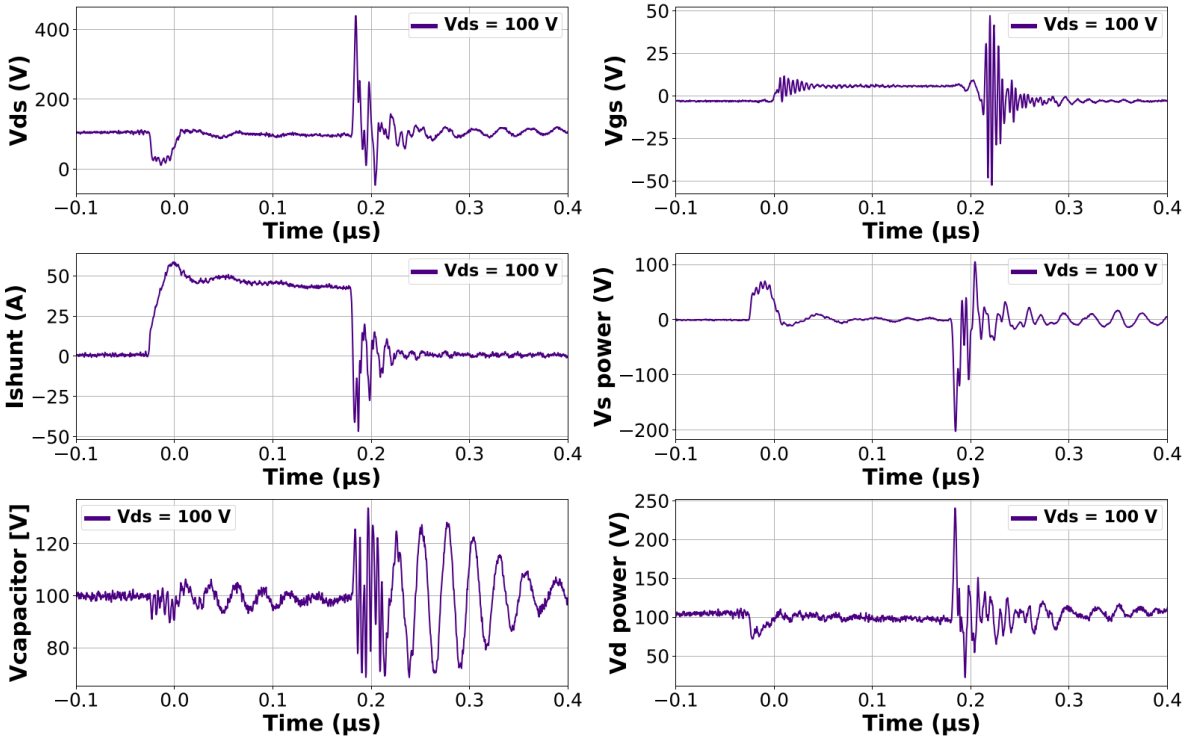

Figure 147: Tests on V_{DS} = 100 V for p-GaN components from supplier 2

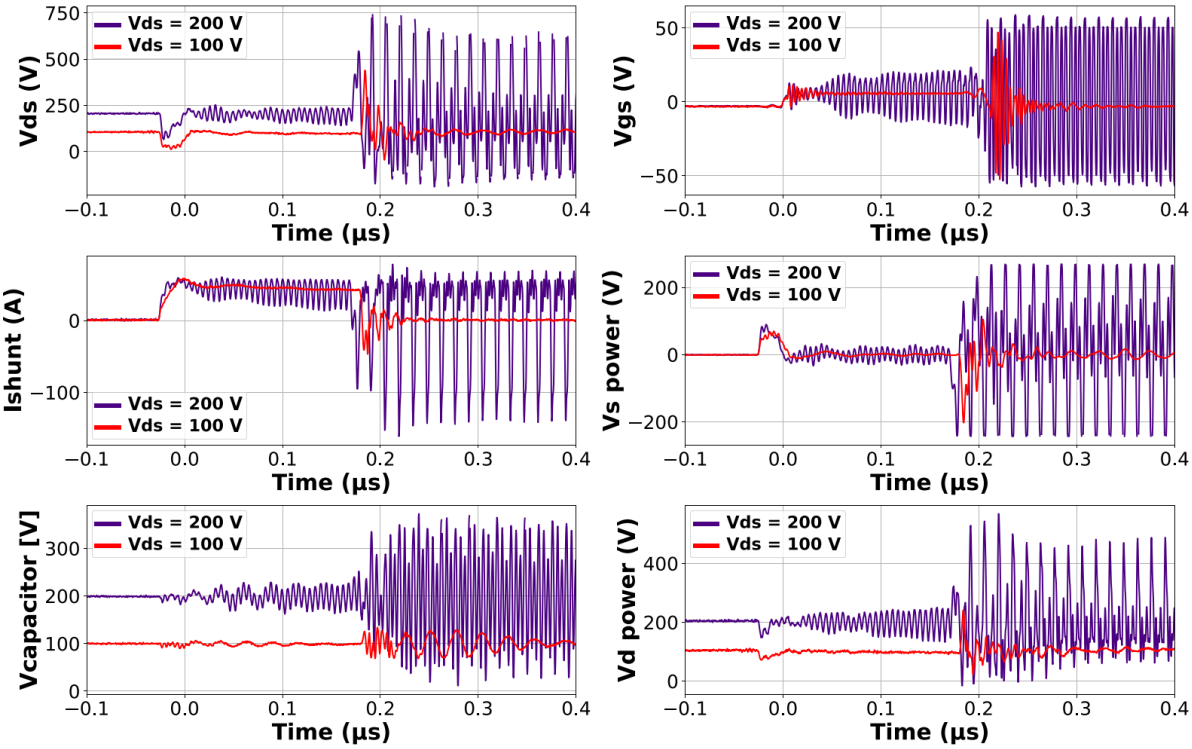

Figure 148: Tests on V_{DS} = 200 V for p-GaN components from supplier 2

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2.3.2 A New and Necessary Optimisation of the Bench

2.3.2.1 Impact of the Gate Resistance

Destructive oscillations mainly occur during the turn-off. For this reason, it was decided to study the impact of the R_{GOFF} turn-off gate resistor as it has been studied in literature for instance with [77,95]. The supplier recommends for normal switching the use of a low gate resistor, with a value of 1 to 2 Ω. This statement may be questioned in our study, given that the short-circuit is a very specific case. This is nevertheless studied in what follows with the replacement of R_{GOFF}, initially at 20 Ω, to now 2 Ω. Two comparisons are made, first for V_{DS} = 100 V and then V_{DS} = 200 V.

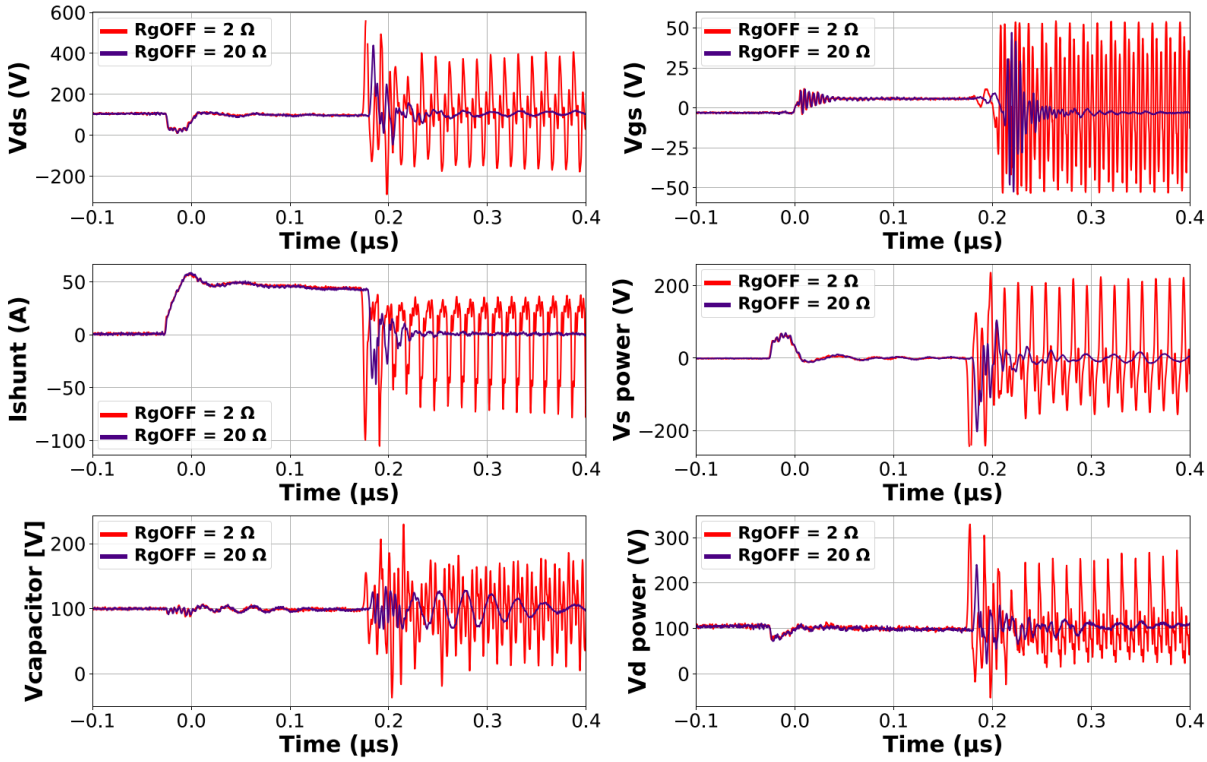

Figure 149: Comparison for two different values of R_{GOFF}: 2 Ω and 20 Ω at V_{DS} = 100 V, on Test-Board 2023

For R_{GOFF} = 2 Ω, OFF switching is impossible from V_{DS} = 100 V. Setting a lower gate resistance, as it might be expected, does not seem to improve matters, and in fact makes them worse as it can be observed in Figure 149, since for V_{DS} = 100 V, the previous signals were relatively stable. The tests are nevertheless extended to V_{DS} = 200 V in Figure 150 and give results in the same direction as the previous tests at V_{DS} = 100 V. For R_{GOFF} = 2 Ω, the behaviour is erratic from the start of conduction. Reducing the gate resistance R_{GOFF} is therefore not relevant. It is therefore necessary to study whether increasing it will stabilise the behaviour of the component.

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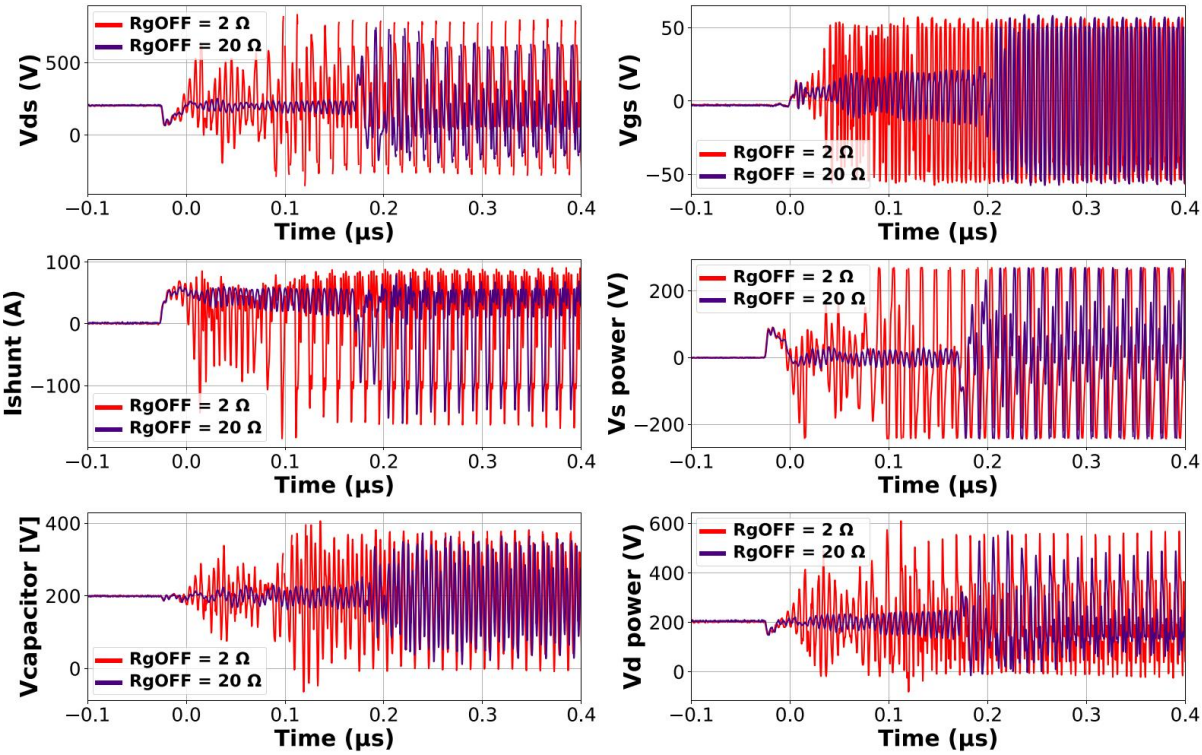

Figure 150: Comparison for two different values of R_{GOFF}: 2 Ω and 20 Ω at V_{DS} = 200 V

It was therefore decided this time to increase the value of R_{GOFF} to 30 Ω, with the same test logic for V_{DS} = 100 V (Figure 151) and V_{DS} = 200 V (Figure 152).

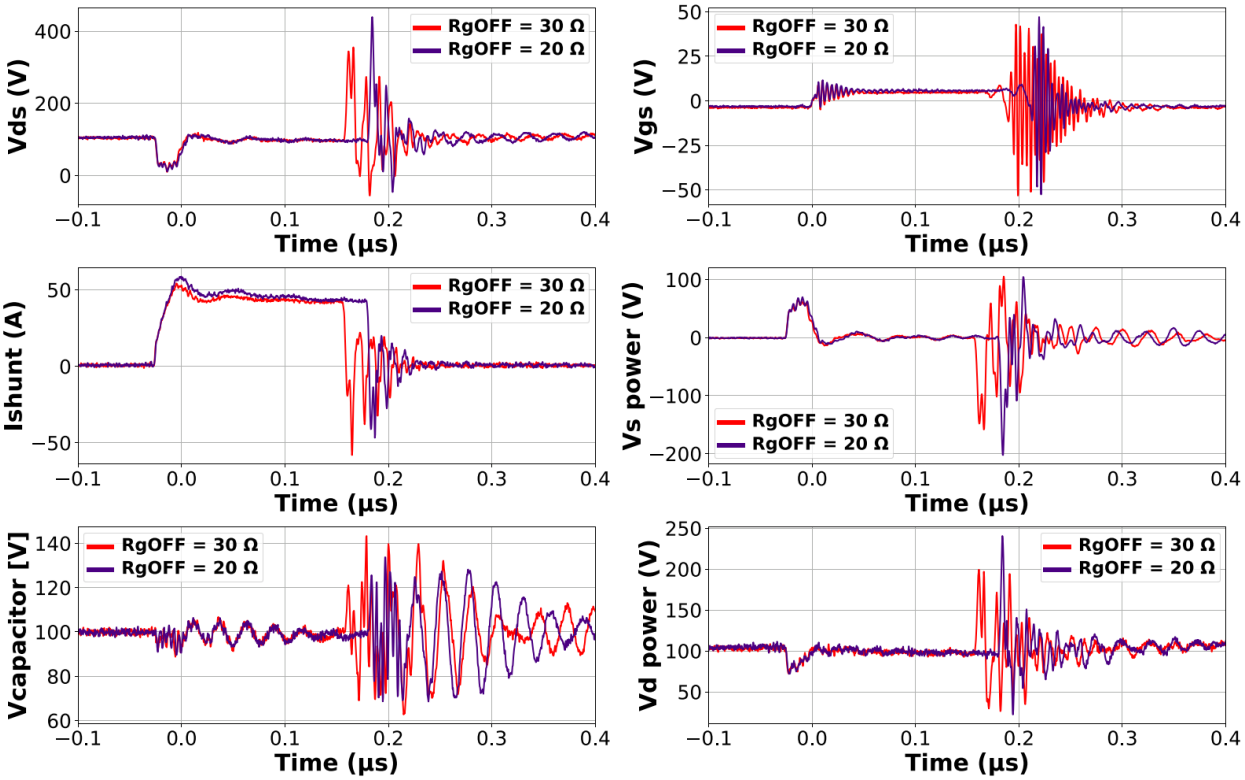

Figure 151: Comparison for two different values of R_{GOFF}: 20 Ω and 30 Ω at V_{DS} = 100 V

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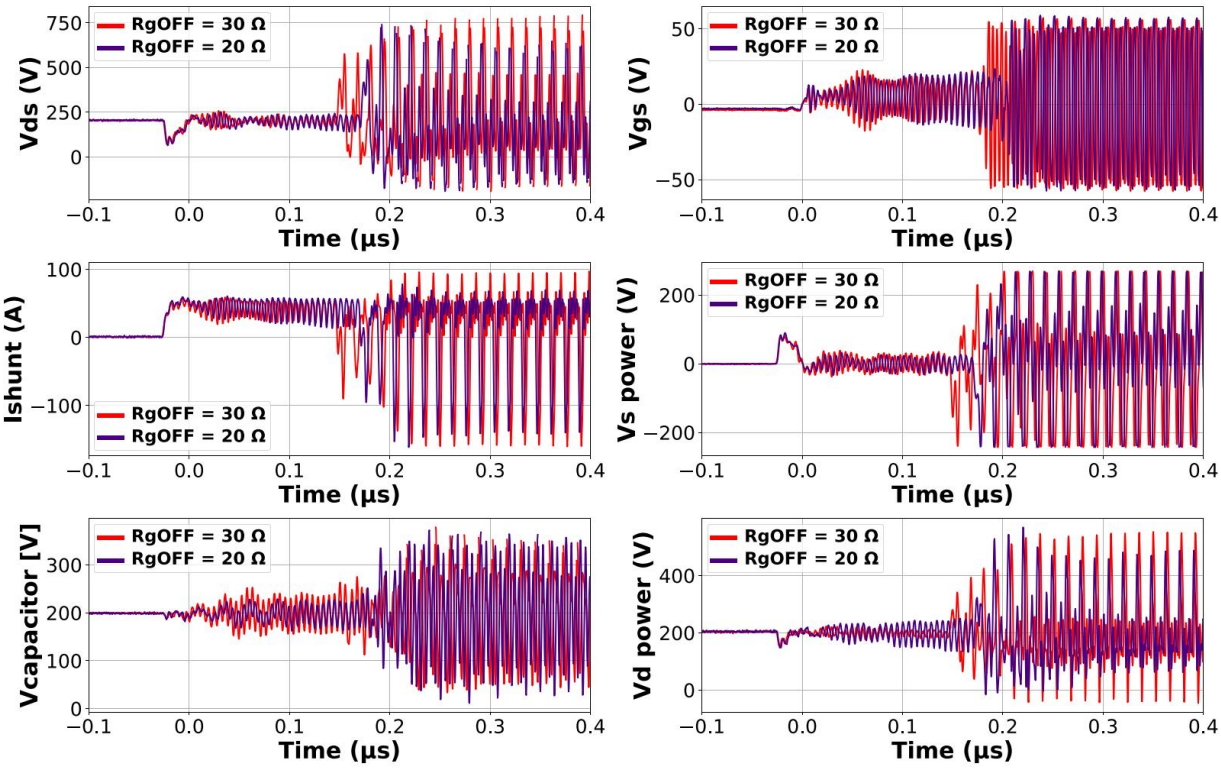

Figure 152: Comparison for two different values of R_{GOFF}: 20 Ω and 30 Ω at V_{DS} = 200 V

Increasing R_{GOFF} to a value of 30 Ω has no clear impact. The V_{DS} and V_{GS} signals show non-negligible oscillations during the conduction phase, which become totally chaotic when the component is turned off. V_{DS} overvoltage exceed the limit of the device, with a measured V_{DS} signal above 650 V. The measured signal V_{GS} greatly exceeds the limits specified by the supplier. At this stage, it is impossible to carry out repetitive short-circuit tests. As suppliers only use low resistance values, it was decided that this resistance value could not be increased indefinitely. As a result, the study and optimisation of the bench were turned towards other areas of research.

The last test at R_{GOFF} = 30 Ω proved critical. In fact, the device broke, as shown in Figure 153. Faced with the runaway state of the component and its inability to turn off the conduction, it finally broke with a rapid uncontrolled increase in current after 1.5 µs, as shown in the Figure 153.

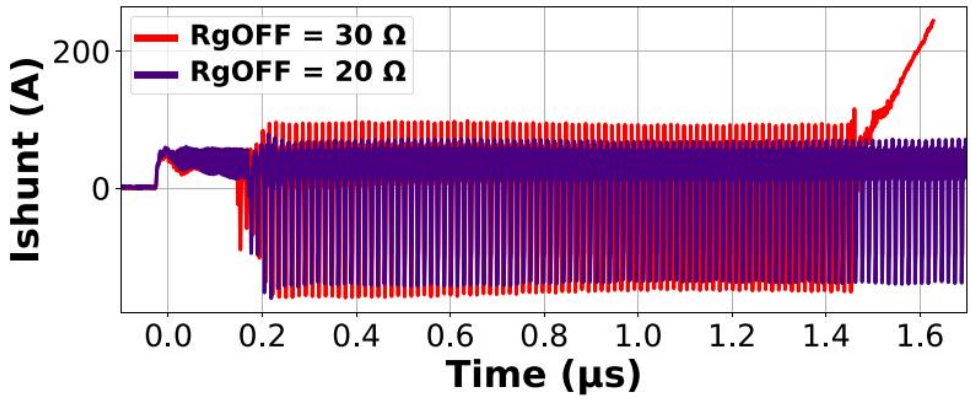

Figure 153: breakage of the component during the last test with R_{GOFF} = 30 Ω

Given this lack of understanding, it was decided to use simulation once again.

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2.3.3 Back to Simulation with Increased Loop Inductance

The simulation developed previously for the normally-on components is taken back. In the absence of technical data on the components about the IsoVu probe, it was decided to keep the passive probe models in the simulation, including for the acquisition of the V_{GS} signal. The first experimental tests resulted in the driver breaking, which is annoying because repairing or changing it is quite time-consuming. To counter this, a Transient-Voltage-Suppressor (TVS) diode was added to protect the driver from excessive overvoltage, above 24 V. The SPICE model for this component was not available, but a model for a similar component (Littelfuse SMDJ33CA) was found and added to the simulation. At this stage, there are no further changes.

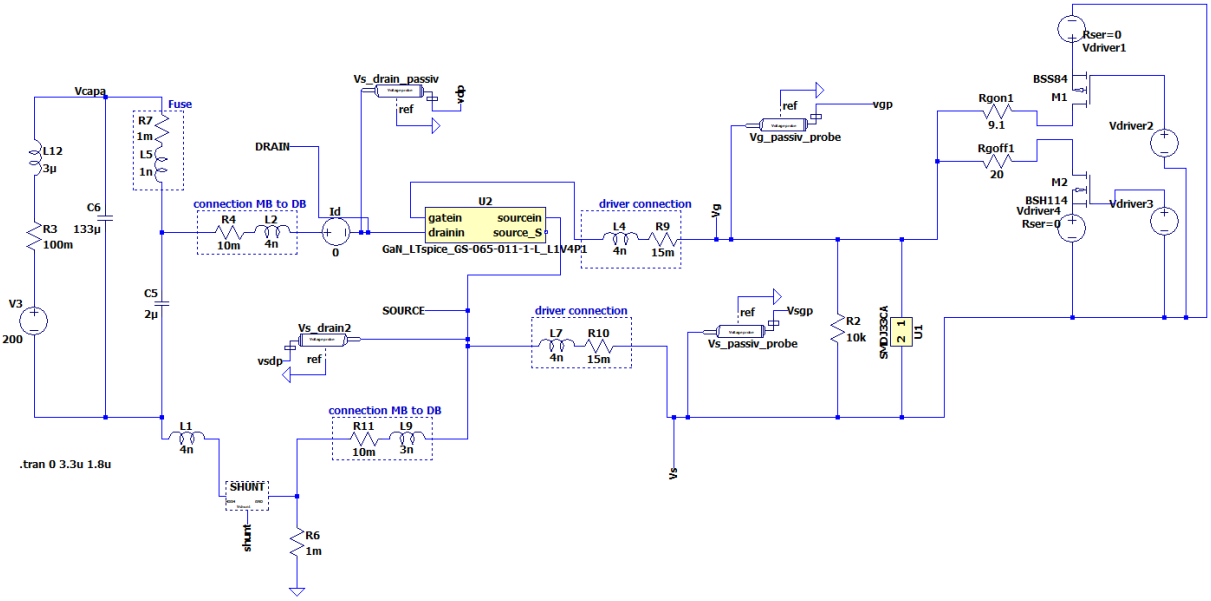

Figure 154: SPICE Simulation with same parasitic inductance as before for normally-on components

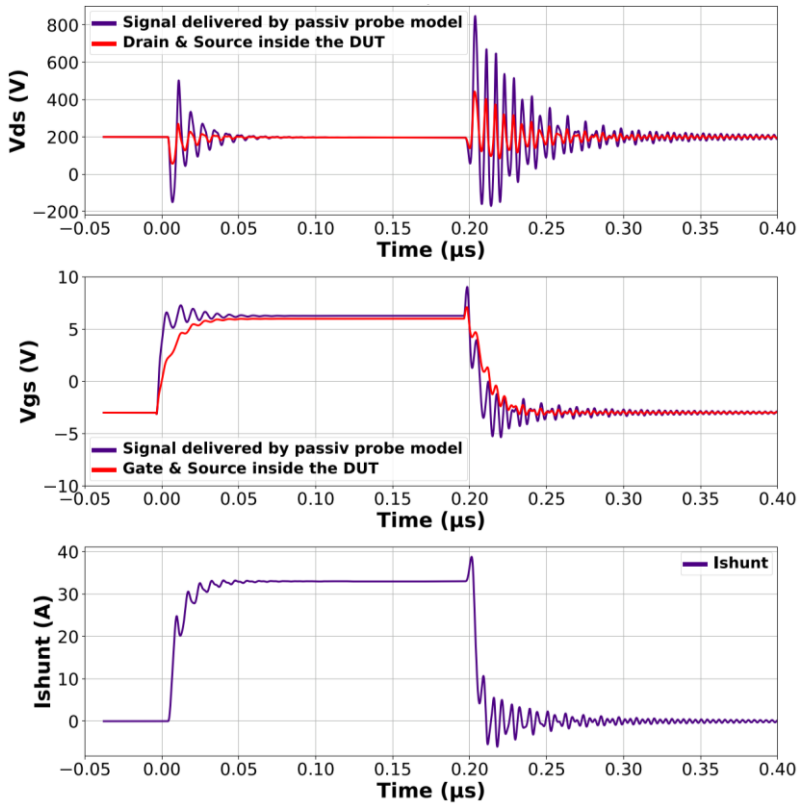

Figure 155: Simulated Waveforms V_{GS},V_{DS} and I_{SHUNT}

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The signals are acquired in two distinct ways, directly inside the device with drain, gate and source electrodes or with the help of a simulated probe. The signals are compared in Figure 155.
Although there are non-negligible oscillations at the turn-off after 0.20 µs of conduction in the Figure 155, they are nonetheless out of all proportion to those observed experimentally. At this stage, the simulation gives V_{GS} signal not dangerous for the device and needs to be improved.
The first improvement concerns the dimensioning of the parasitic inductance of the power loop. In the light of [156–158], an adjusted parasitic track inductance value of 10 nH/cm is considered preferable to what had been done previously. By means of the track length measurements reassembled in Figure 156 below, the evaluation of the parasitic inductances of the tracks is significantly increased.

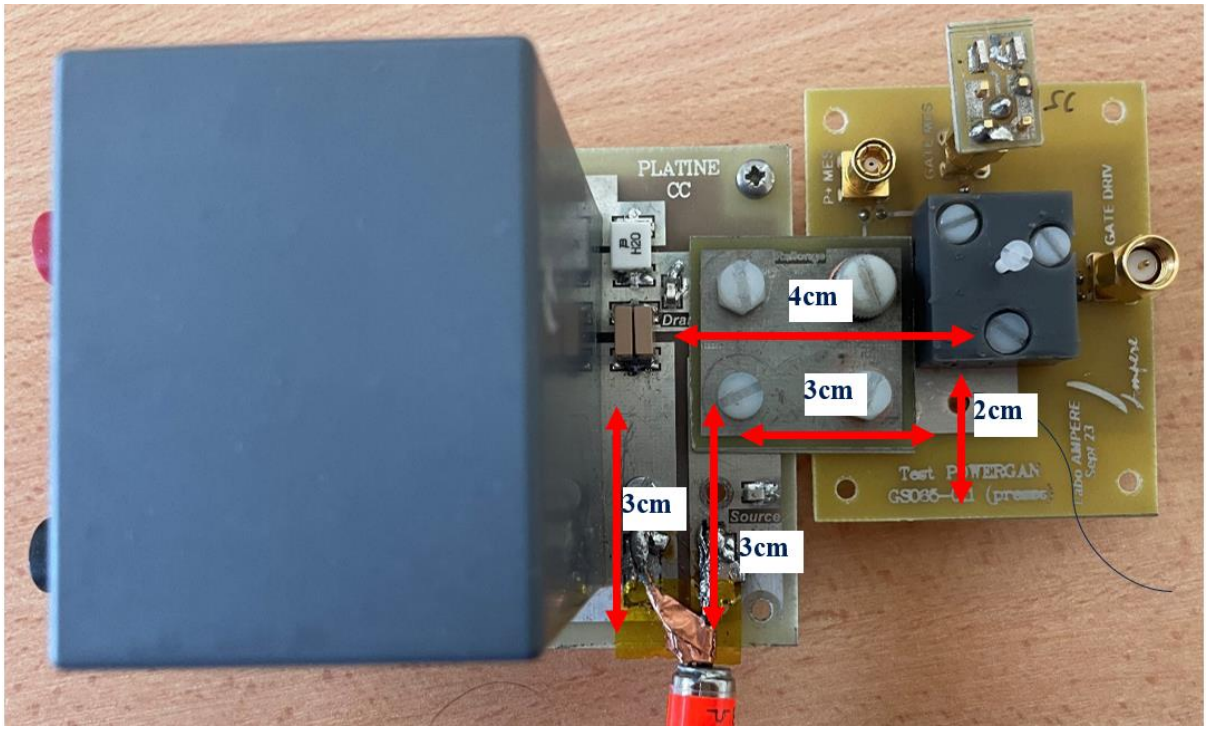

Figure 156: measurements of the length of track on PCB

The simulation is therefore modified to give Figure 157.

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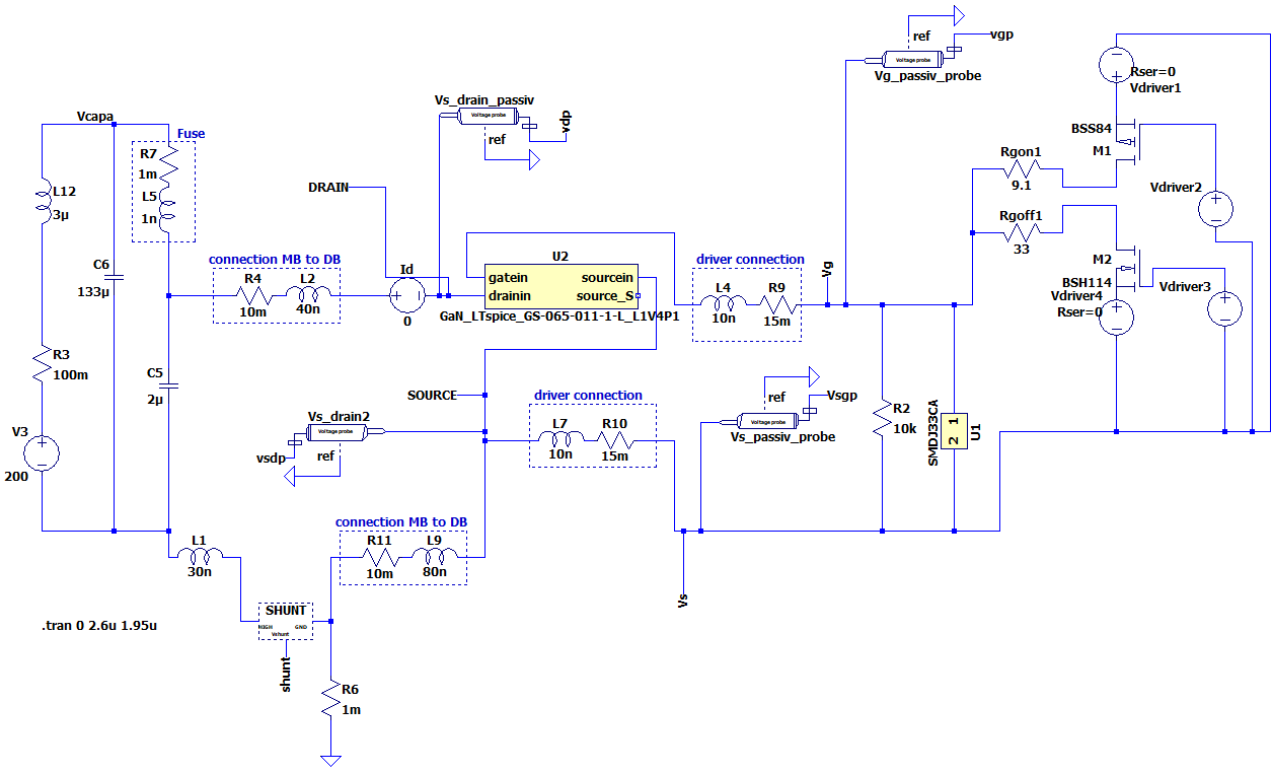

Figure 157: SPICE Simulation with increased parasitic inductances

Increasing the track inductances gives the results below. Although oscillations of greater amplitude are visualised, the chaotic aspect seen experimentally is not found.

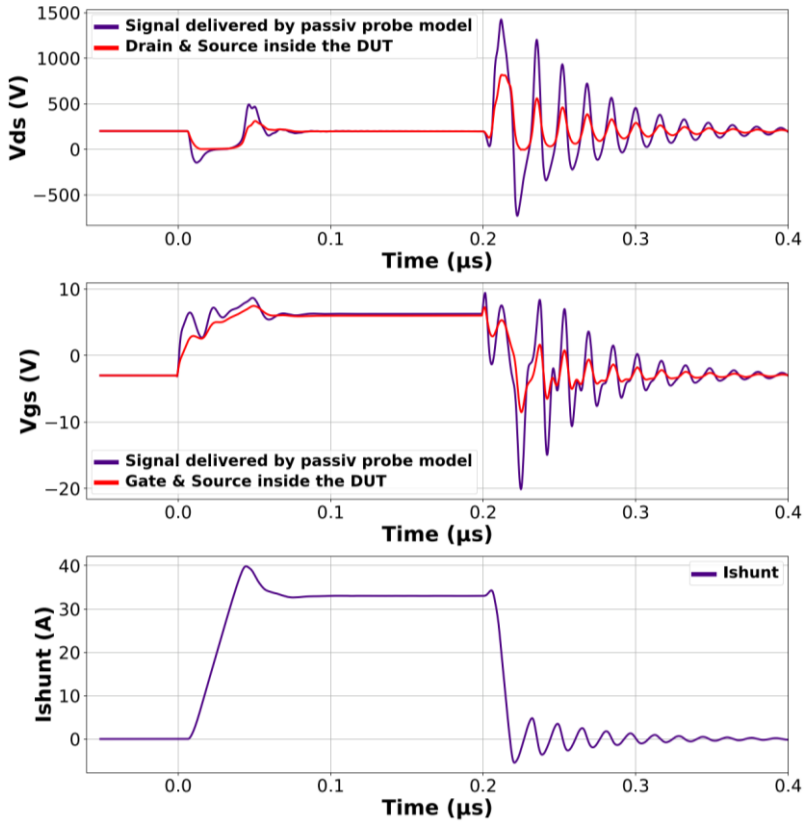

Figure 158: simulated waveforms for increased inductance in the power loop

It was therefore decided to look at the impact of possible common mode currents.

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2.3.4 Inductances Alone Cannot Explain the Behaviour of the Bench

Common mode currents are studied. A current probe from Tektronix with reference TCP0030A was used (Figure 159 and Figure 160).

Figure 159: current probe used to measure common mode current

An initial common mode current measurement is taken on the coaxial cable linking the shunt to channel 6 of the oscilloscope.

Figure 160: Photography of the test bench with the current probe on the coaxial cable

These measurements were carried out on the various normally-off components and gave the results shown on the Figure 161 for cascode components below. The common mode current measured remains close to zero when V_{DS} = 100 V, whereas for V_{DS} = 200 V, a current in excess of 500 mA is measured.

For the p-GaN component from supplier 1, there is no difference depending on the polarisation level in Figure 162, with the current measured also exceeding 500 mA. For the p-GaN component from the second supplier, with the highest level of disturbance, the common mode current is also non-negligible, of the order of 400 mA, and shows in Figure 163 the same chaotic oscillations as the V_{GS} and V_{DS} signals have. This chaotic oscillation does not exist for a V_{DS} = 100 V.

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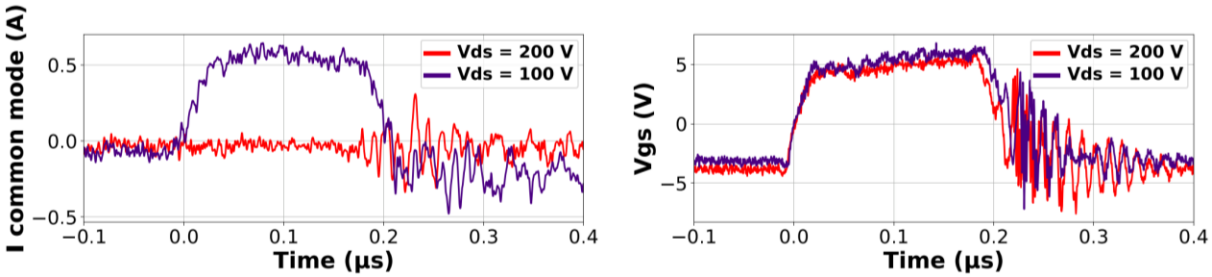

Figure 161: Measurement of common mode current for cascode component, for V_{DS} = 100 V and V_{DS} = 200 V

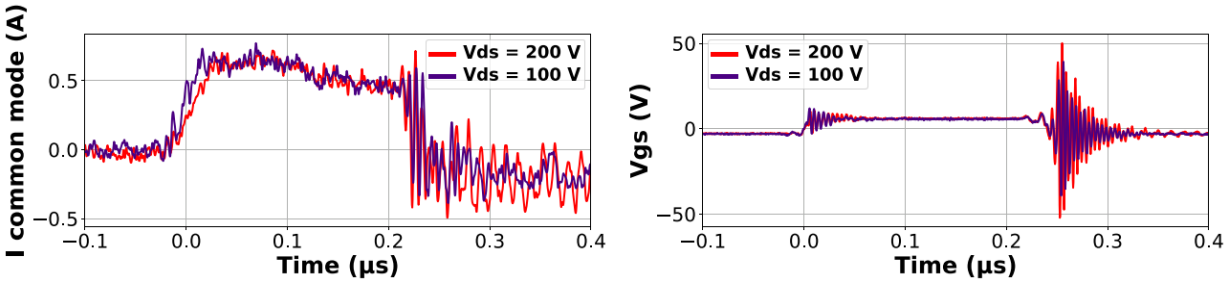

Figure 162: Measurement of common mode current for p-GaN component from supplier 1, for V_{DS} = 100 V and V_{DS} = 200 V

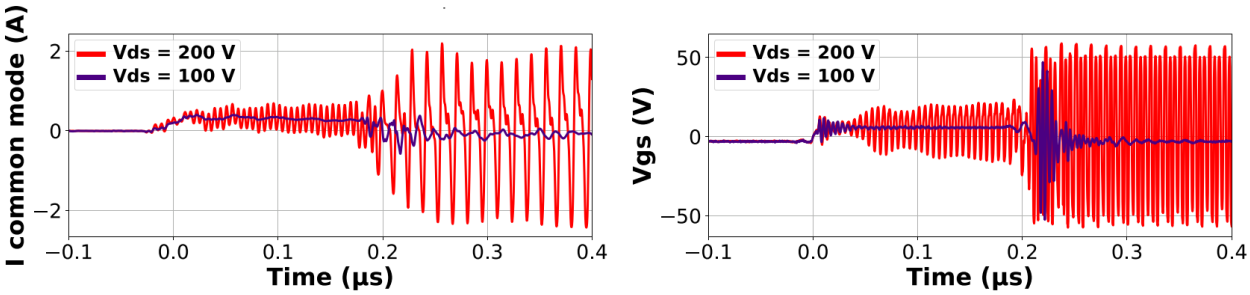

Figure 163: Measurement of common mode current for p-GaN component from supplier 2, for V_{DS} = 100 V and V_{DS} = 200 V

The authors [149,159–162] model common mode currents through parasitic capacitances between the PCB tracks and the ground plane. These capacitances have values ranging from ten picrofarad to several hundred picofarad.

A parasitic capacitor is added to the source part in Figure 164. With a value of 20 pF, similar oscillations to those seen experimentally on the V_{GS}, V_{DS} and I_{SHUNT} signals have been seen in Figure 165. However, the frequency of these simulated oscillations remains lower than those seen experimentally. The results of this improved simulation are judged as acceptable, except the overvoltage peak V_{DS} of around 4 kV. These results will be further discussed and led to other adjustments.

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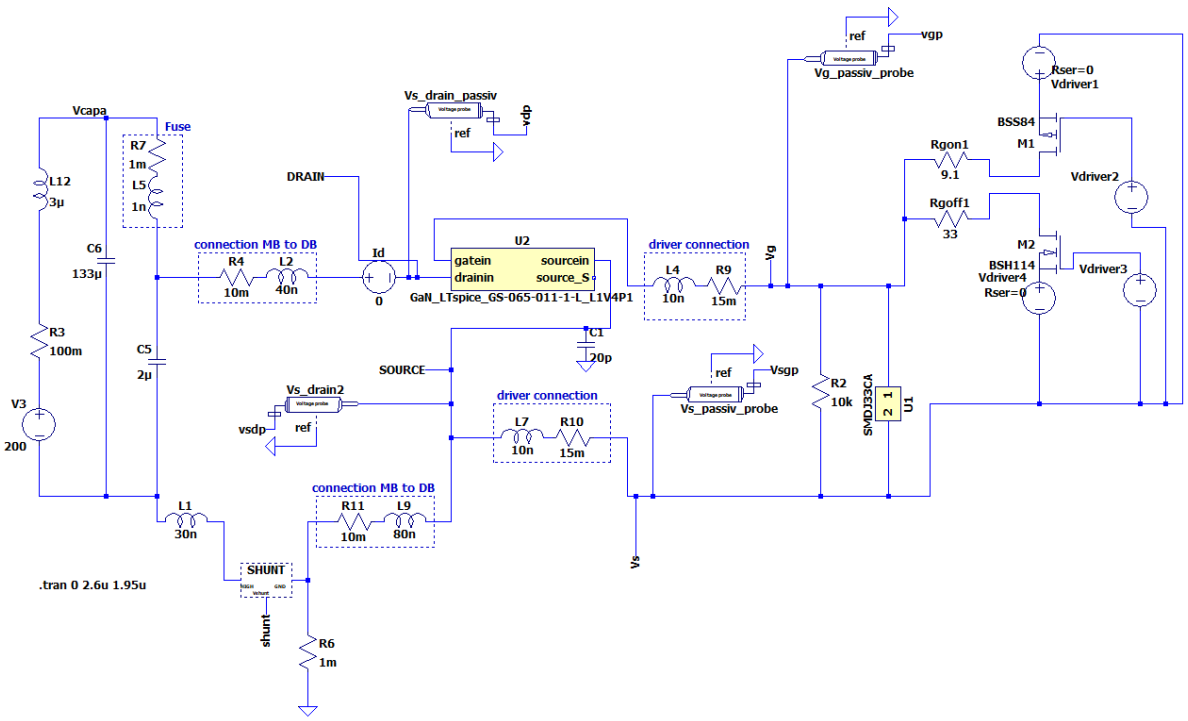

Figure 164: SPICE schematic with increased parasitic inductances and common mode capacitance on Source circuit

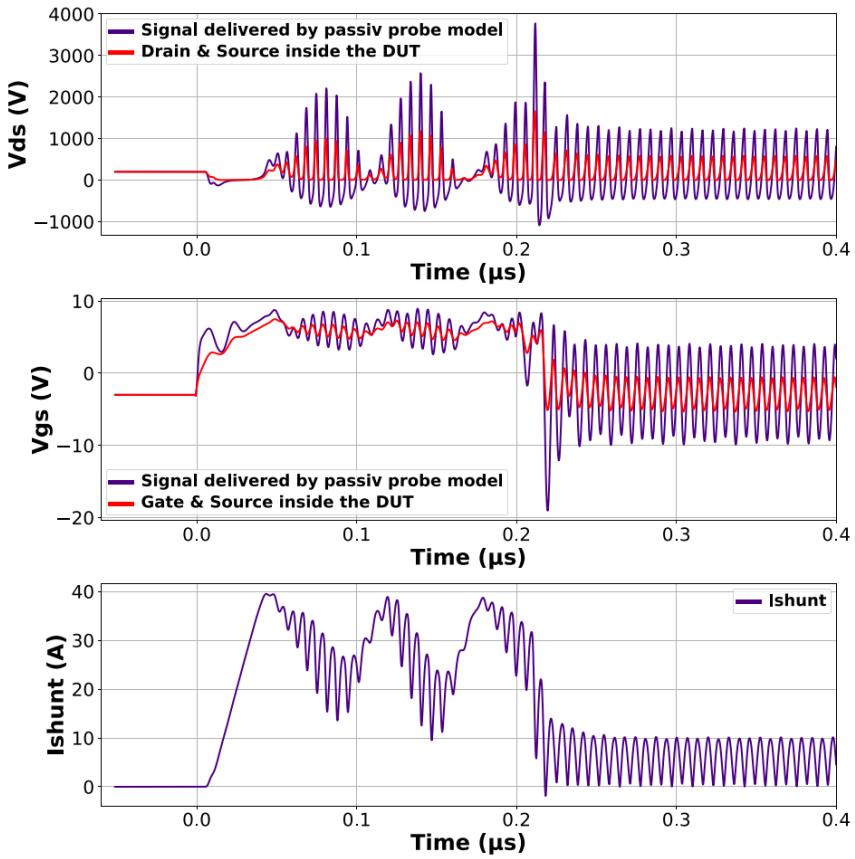

Figure 165: simulated waveforms for increased inductance in the power loop and common mode impact

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It therefore seems legitimate to ask whether the addition of this common-mode capacitance can have an impact at other points in the circuit. At this stage, it is assumed that the signal with the greatest impact, and the most important for the component, is the V_{GS} signal. It is therefore investigated whether the common mode currents do not have an impact via the driver. This is studied in simulation below, then experimentally.

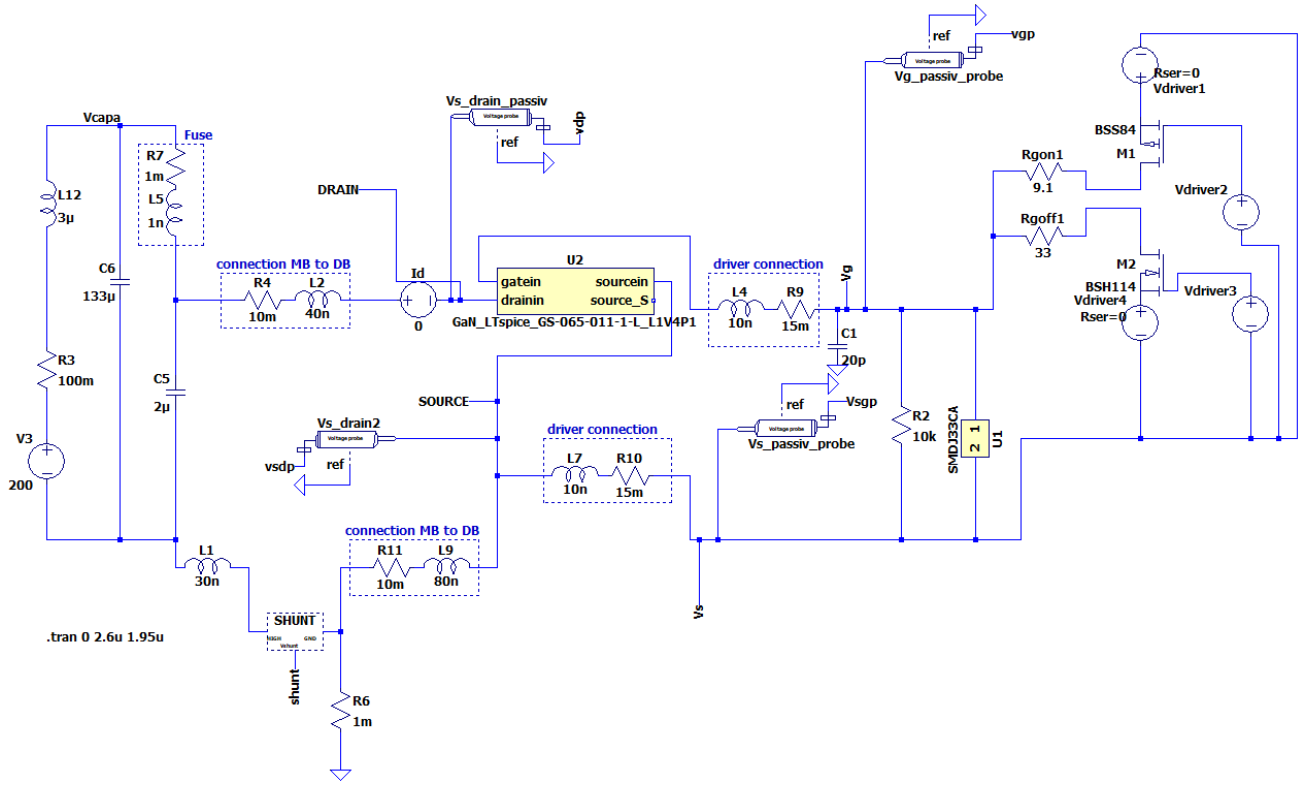

Figure 166: SPICE schematic with increased parasitic inductances and common mode capacitance on Source circuit

Figure 167 shows that adding a 20 pF parasitic capacitor on the gate side produces oscillations even more similar to those observed experimentally, except the value of overvoltage for V_{DS} signal. Optimisation of the experimental bench therefore involves the treatment of these common-mode currents.

Given that the greatest impact of this parasitic capacitance was seen at the gate in simulation, it was decided to measure the common-mode currents in this region this time.

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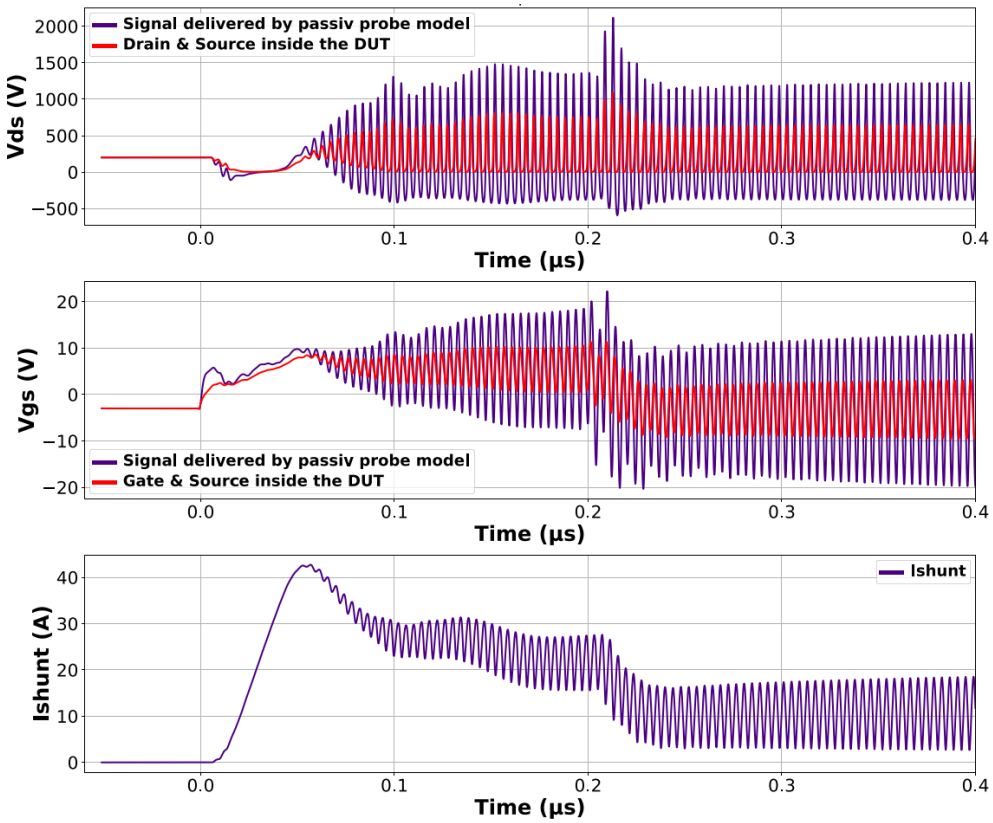

Figure 167: SPICE waveforms with increased parasitic inductances and common mode capacitance on gate

In addition, the simulation confirms that even for resistor values different from those tested experimentally, the latter have little impact. Both for R_{GOFF} = 100 Ω and for low values of R_{GON} (1 Ω) or high values (25 Ω, beyond which the fast character of the short-circuit is lost, with a much slower rise in current than during a true short-circuit), the destructive oscillations remain as it is shown in Table *18*.

R_{GON} (Ω)	R_{GOFF} (Ω)	Status
9.1	20	***Non-ok***
9.1	33	***Non-ok***
9.1	100	***Non-ok***
1	2	***Non-ok***
1	20	***Non-ok***
1	33	***Non-ok***
1	100	***Non-ok***
25	2	***Non-ok***
25	20	***Non-ok***
25	33	***Non-ok***
25	100	***Non-ok***

Table 18: Different values of Gate Resistance tested in Simulation and the conclusion about the presence of an impact or not

Also, in order to protect the driver, a TVS had been inserted in the control circuit. In the light of [95], it is reasonable to wonder whether the addition of this component can be held responsible for the chaotic behaviour seen so far. The simulation developed above indicates that there is no impact depending on whether the TVS diode is present or not. These results will be confirmed experimentally.

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2.3.5 Measurement and Reduction of Common Mode Currents

Because of their high magnetic permeability, ferrite cores are ideal for reducing common-mode currents. They can therefore be easily magnetised and concentrate magnetic fields. Ferrite cores are recognised as being particularly effective in treating high-frequency disturbances, particularly common-mode currents, thereby reducing electrical noise without altering the signals. Their use is fairly simple, since they can be added around existing cables or wires, without complex modifications to the electronic circuit or the addition of expensive electronic components [145,147,163].

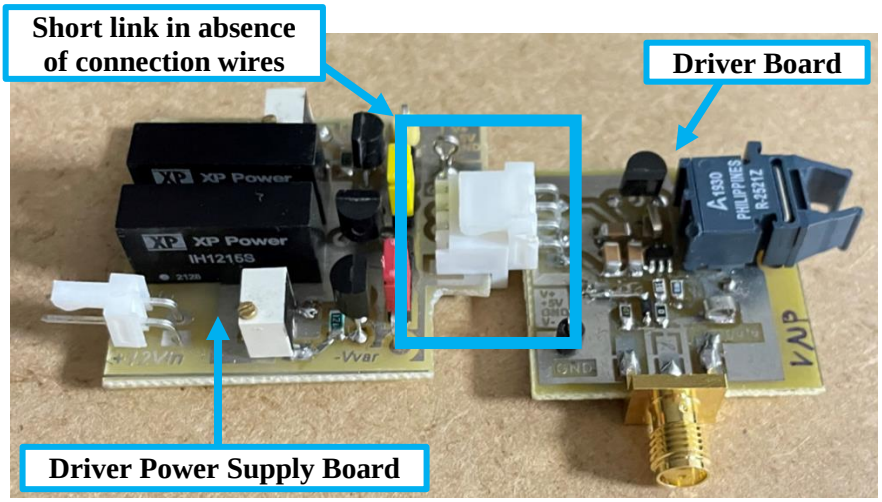

Figure 168: Driver part with the power supply (left) and the command (right)

Again using the current probe, a measurement is carried out on the wires connecting the driver power supply board and the driver board.

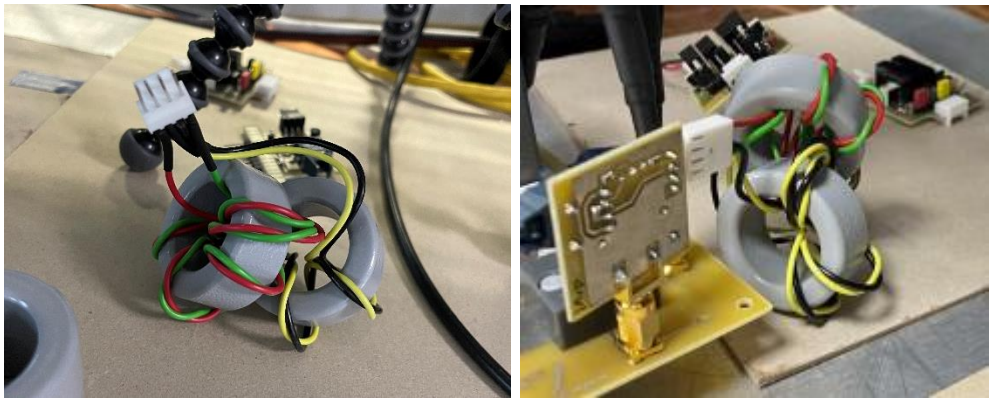

Figure 169: Two ferrite chokes interlaced with driver wires (left) and connected to the driver board (right)

Double or even quintuple looping of the wires around the ferrite cores is studied.
Various configurations were tested, but the only one giving satisfactory results was the one linking together the two V_{High} drive and V_{Low} drive wires (red and green in Figure 169) and the ground and V+ optocoupler wires (yellow and black in the photography). The results are shown in Figure 170 and Figure 171 below.

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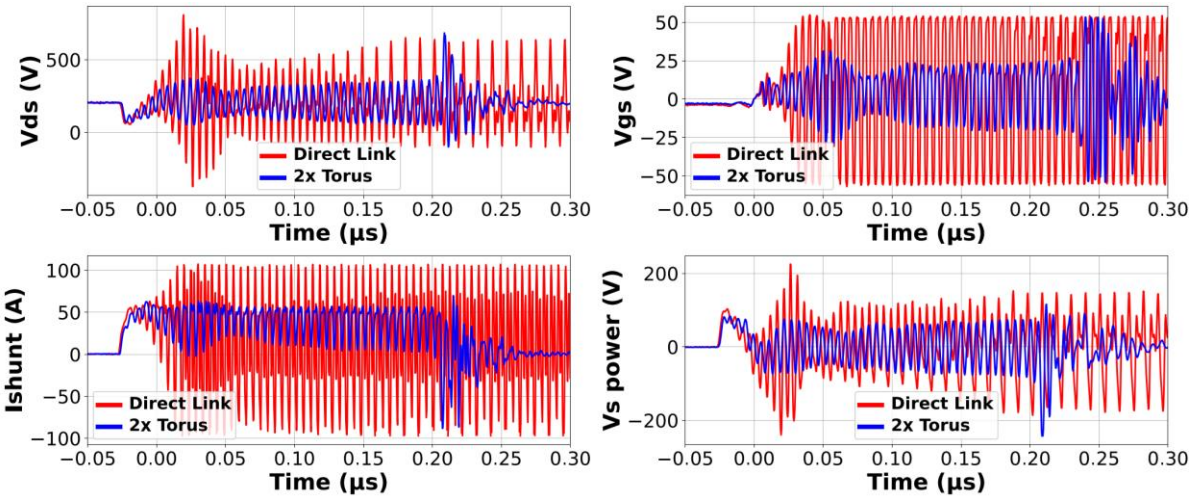

Figure 170: Experimental signals V_{GS}, V_{DS}, I_{SHUNT} and $V_{S,POWER}$ after the adding ferrite chokes

Figure 170 compares the V_{GS}, V_{DS}, I_{SHUNT} and $V_{S,POWER}$ signals before and after the addition of the ferrite cores between the driver power supply board and the driver board. Although the signals remain disturbed, it is easy to note a significant reduction in the amplitude of the signal oscillations. Measurement of the common-mode currents between the two boards in Figure 171 gives the same conclusion. These initial encouraging results point the way to further tests with increased looping of the wires through the ferrite cores.

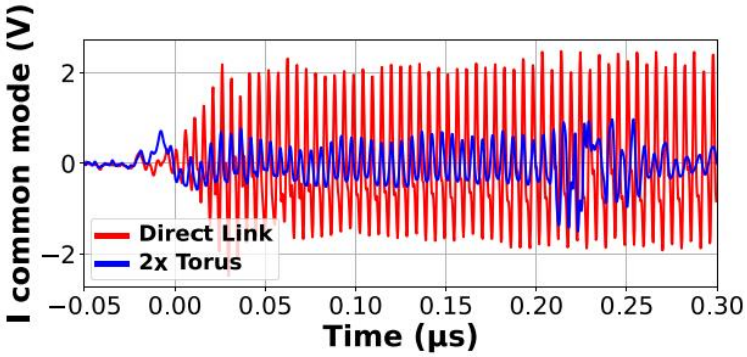

Figure 171: Experimental acquisition of the common mode current between driver power supply board and driver board

The cables are now looped five times around the ferrite cores, rather than twice. The results are shown in Figure 172 and in Figure 173 below.

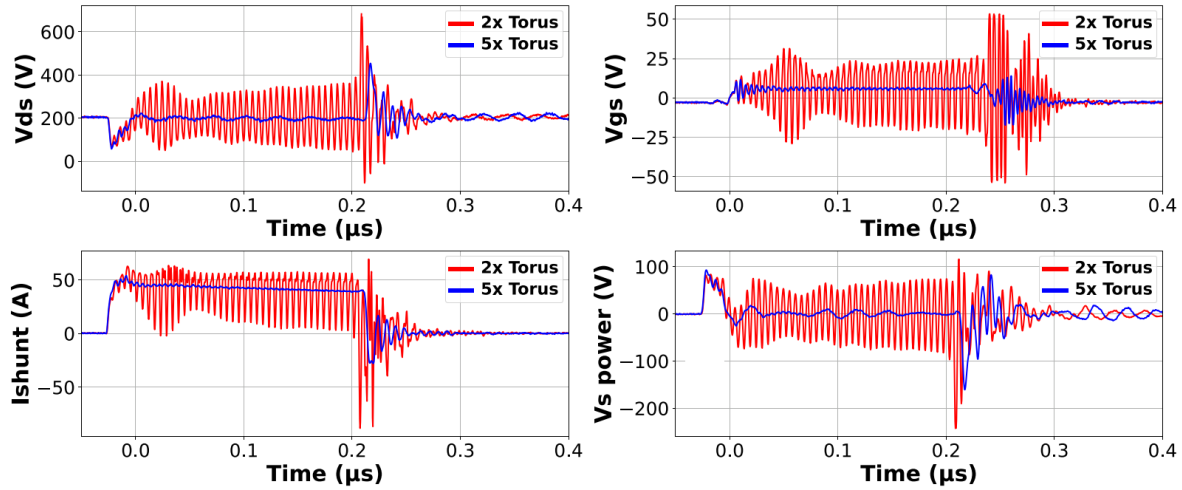

Figure 172: Experimental signals V_{GS}, V_{DS}, I_{SHUNT} and $V_{S,POWER}$ with cables looped 5 times around ferrite chokes

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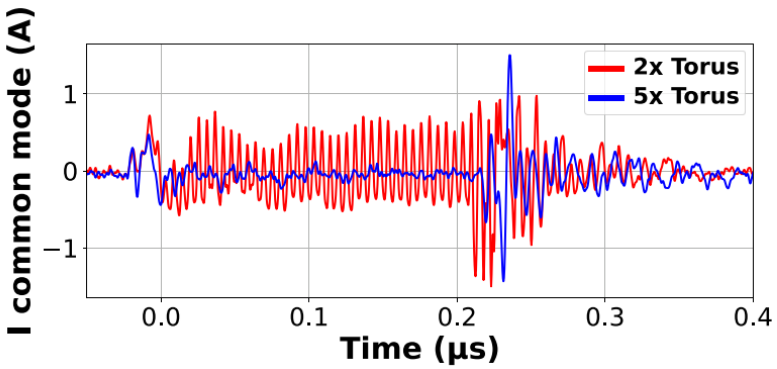

Figure 173: Experimental acquisition of the common mode current between driver power supply board and driver board with cables looped 5 times around ferrite chokes

Looping through the ferrite cores five times gave the most stable results. The oscillations of the V_{GS}, V_{DS}, I_{SHUNT} and $V_{S,POWER}$ signals have been greatly reduced and the common-mode current flow between the driver power supply board and the driver board greatly reduced.

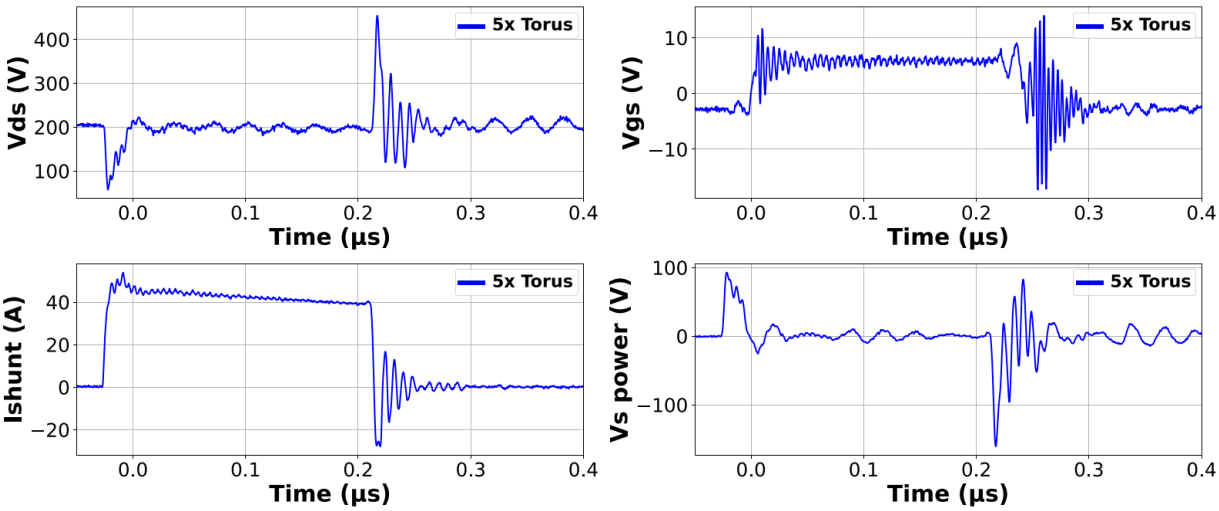

Figure 174: optimized signals with five times looped cables through ferrite cores

Optimisation of the bench, by means of simulation and experimental reduction of common mode currents, has therefore made it possible to significantly reduce disturbances. Repetitive, non-destructive short-circuit tests for V_{DS} = 200 V can now begin, as shown in Figure 175.
At this stage, the three types of component (cascode, p-GaN from suppliers 1 and 2) are operating stably on the experimental 2023 bench. The repetitive tests and electrical characterisations can therefore begin. The results are presented later in Chapter 3.

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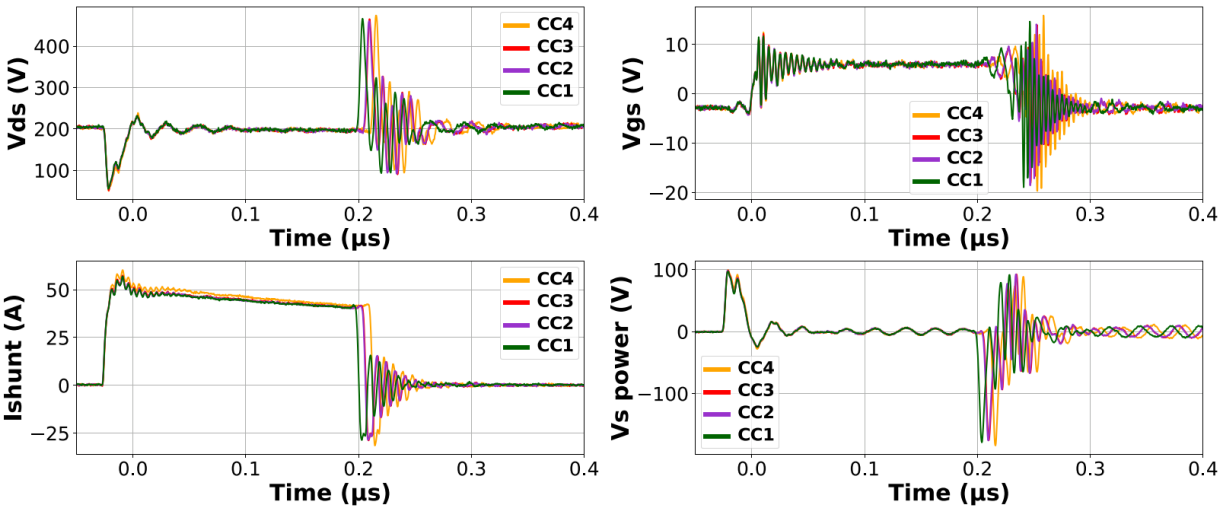

Figure 175: a series of repetitive short-circuits
(CCX mentioned in the caption with X the number of the short-circuit)

Table 19 shows how beneficial the bench optimisation was for the V_{GS} signal from the second supplier's p-GaN component. This before/after optimisation comparison is carried out for cases with a minimum of stability and is therefore limited to V_{DS} = 100 V, the V_{DS} = 200 V case being inoperable before optimisation. Results are shown in Figure 177.

	Max V_{GS} (V)	**Min V_{GS} (V)**
Before optim.	47.06	-52.53
After optim.	20.57	-23.48
Reduction	**56%**	**55%**

Table 19: Results of the p-GaN component from supplier 2 after optimization of the test bench, for V_{DS} = 100 V

Following this optimisation, the bench was re-tested on p-GaN components from the first supplier. Although these components already had stable and reproducible behaviour, the bench optimisation improved the signals for these components too. As can be seen in Figure 176, the V_{DS} signal remains broadly similar, except for a slight reduction in the overvoltage at turn-off. The most remarkable improvement is found in the V_{GS} signal, with a sharp reduction in oscillations and overvoltage during turn-off. The quantification of this optimisation of bench operation for p-GaN components from the first supplier is explained below in Table 20.
Prototypes from the same supplier were also tested and also showed stable operation.

	Max V_{GS} (V)	**Min V_{GS} (V)**
Before optim.	39.18	-39.23
After optim.	10.84	-13.52
Reduction	**72 %**	**66%**

Table 20: Results of the p-GaN component from supplier 1 after optimization of the test bench, for V_{DS} = 200 V

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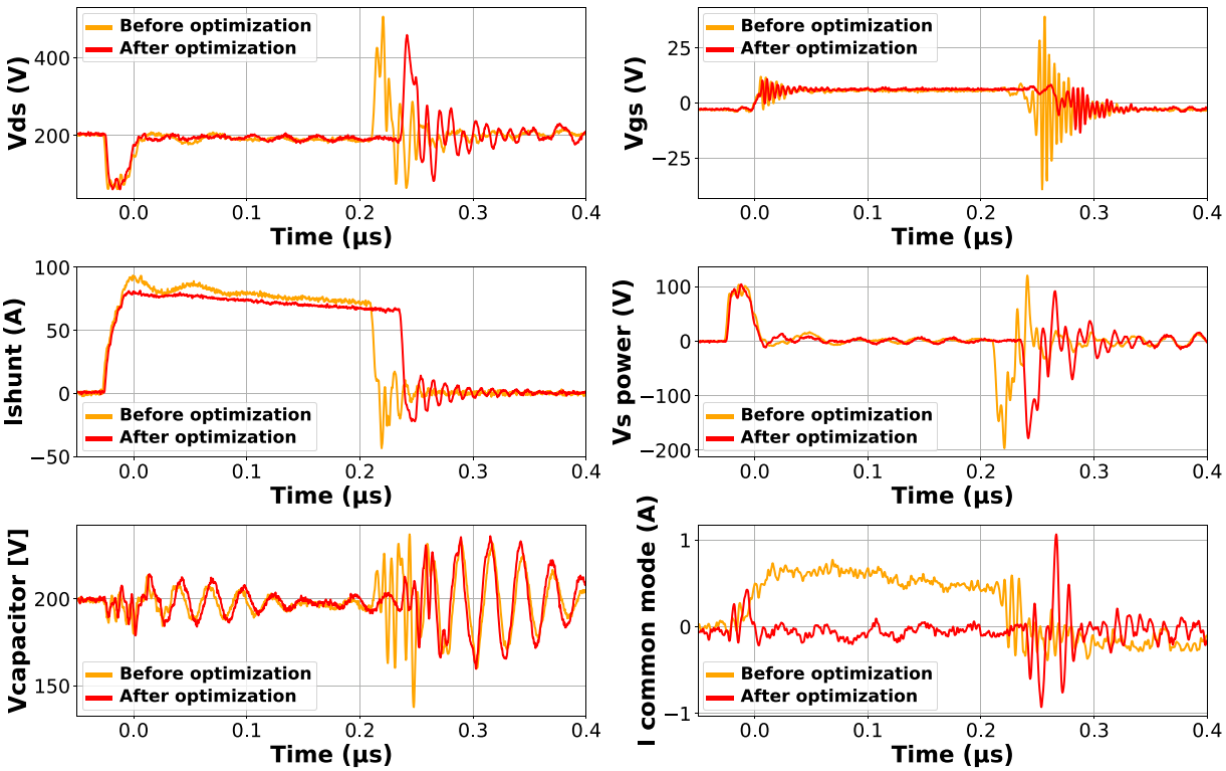

Figure 176: Experimental signals of the p-GaN component from supplier 1 before and after optimization of the test bench, for V_{DS} = 200 V

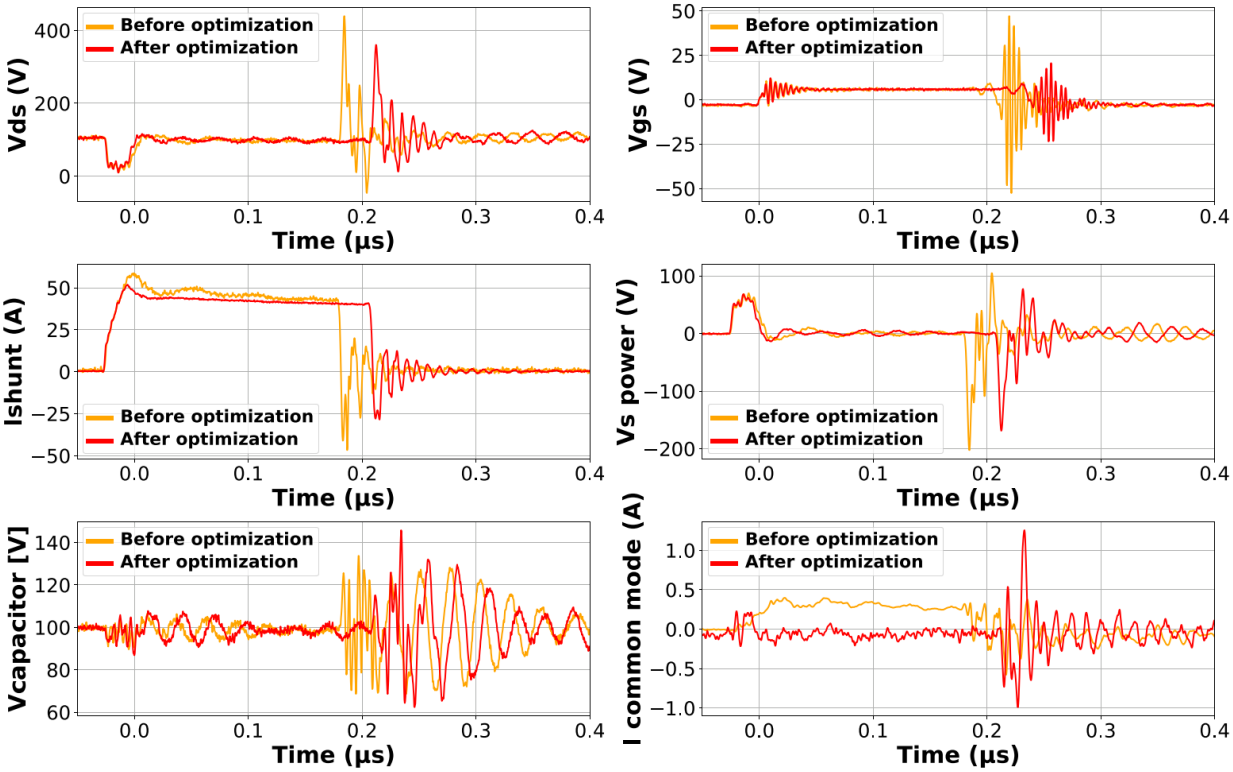

Figure 177: Experimental signals of the p-GaN component from supplier 2 before and after optimization of the test bench, for V_{DS} = 100 V, on Test-Board 2023

Optimising the bench was not an easy task, as many parameters can influence the behaviour of the bench. It has also been shown that the presence of the measurement probe can be detrimental to the correct operation of the bench. This is explained below.

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2.3.6 The Difficulty of Using a Current Probe on the Bench

During measurement reproducibility tests, it was possible to demonstrate the impact of the current active probe.

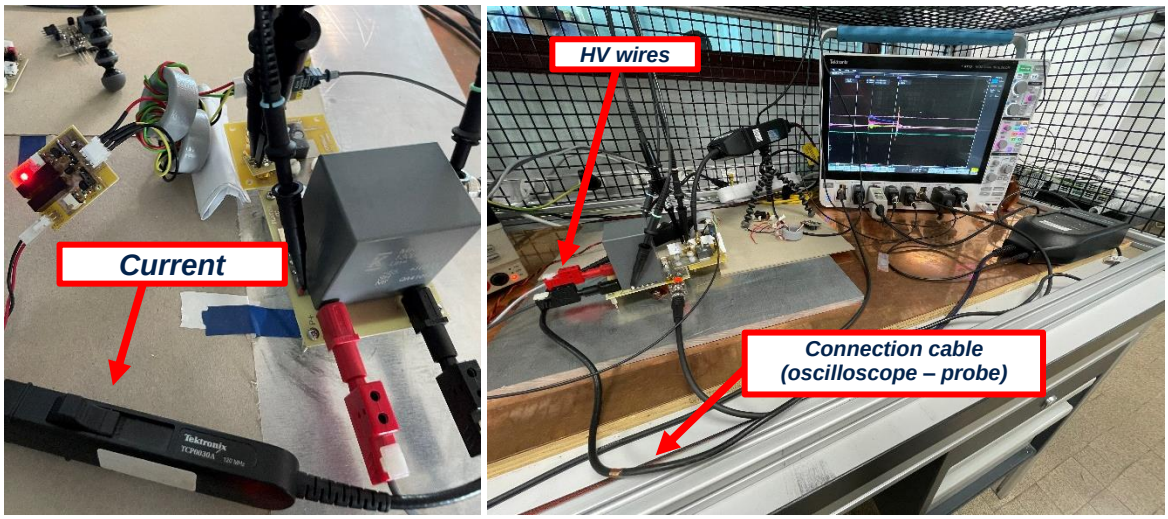

Figure 178: current probe and its connection cable to the oscilloscope

Various cases have been observed. Whether the current probe connection cable runs above or below the high-voltage supply cables is not trivial and it gives contrasted waveforms. The red curve depicts the situation when the probe cable runs below the HV supply. Sharp disturbances can be observed with parasitic oscillations during the conduction. A slight move of this cable changed a lot the waveforms with not only reduced oscillations during the conduction but also exacerbated oscillation few hundreds of nanoseconds before the turn-off. Disconnecting the probe from the oscilloscope but leaving it on the bench is not without consequences either, as shown in Figure 179 with the orange curve. The stable case (in light green), with the probe connection cable passing over the high-voltage cables, remains reproducible and gives the same conclusions as the *Figure 179* below. Nevertheless, it has been decided to remove this current probe from the experimental bench from now on, to limit the risk of disturbance.

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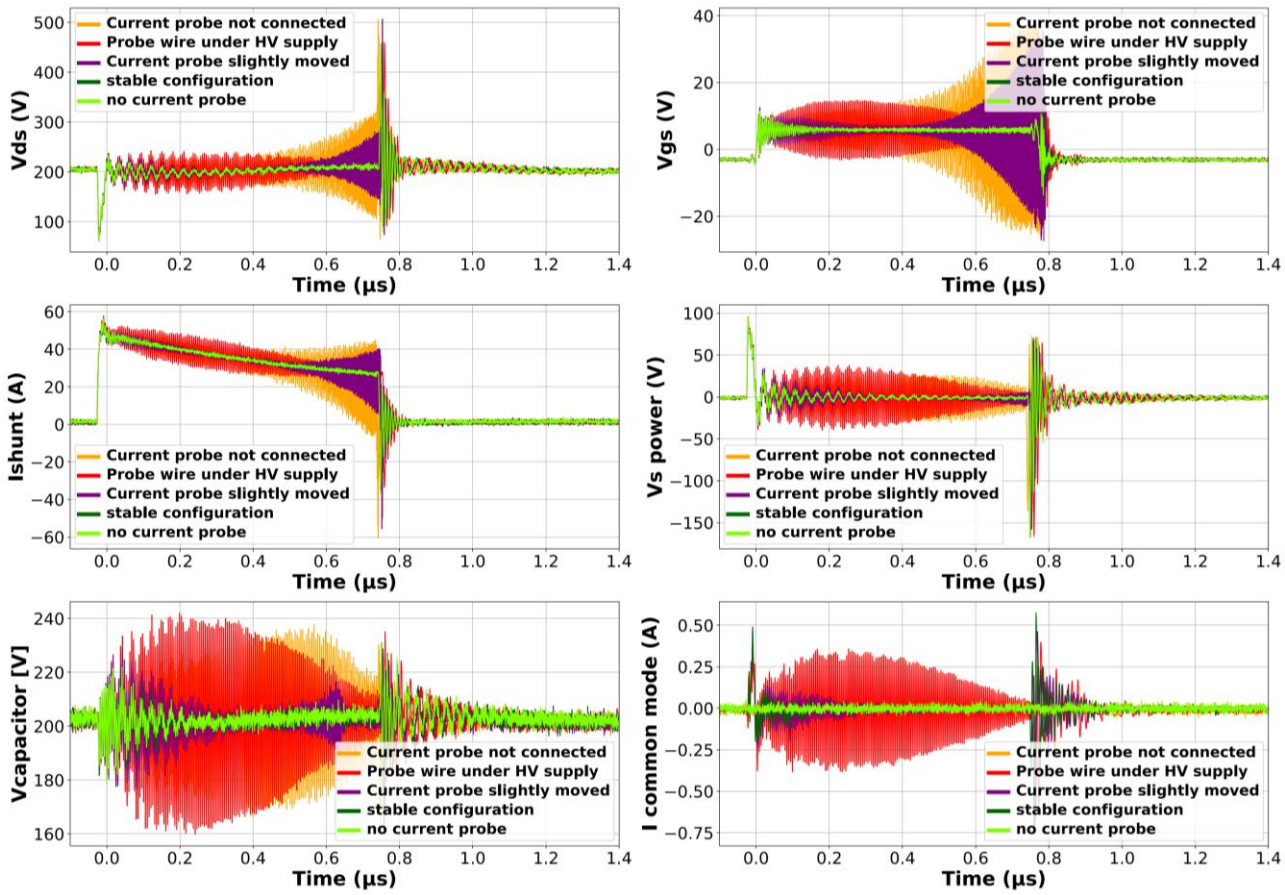

Figure 179: Impact of the current probe on the stability of the test bench

2.3.7 Impact of the New Driver (2024 Version) and its DC/DC Converters

In parallel with the development of a new version of the test board, a new version of the driver assembly is being studied. Discussions within the laboratory have highlighted the potential impact of the DC/DC converters used in the driver power supply board, as well as their insulation capacitance.
At this stage, the use of DC/DC converters with a lower insulation capacity has only been preferred on other experimental benches in the laboratory.
The converters initially used, from the supplier XPPpower, reference IH12151S, have an insulation capacity of 60 pF. The new converters chosen here, from supplier muRata, part number MGJ2D121515BSC, have an insulation capacity reduced to just 3 pF. The datasheets are provided in the appendix. These converters also have the advantage of short-circuit protection, which reduces the risk of destruction if the device breaks.
The two versions of driver power supply board with the specific converters are shown below in Figure *180*.

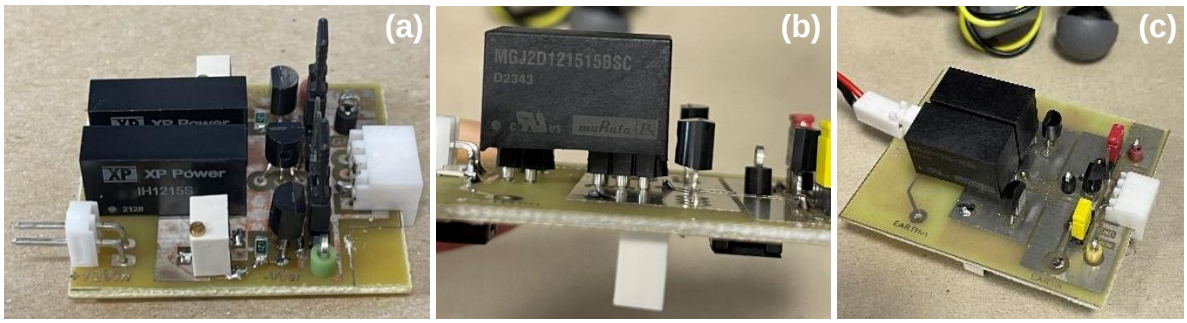

Figure 180: 2023 (a) and 2024 (b & c) versions of driver power supply board

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At the same time, and out of concern for supply lead times, the driver reference has also been changed.

The initial driver from Texas Instruments, part number UCC27531, has been replaced by a driver from Microchip, part number TC4431. No improvements are expected from this driver change, which is purely due to delivery time constraints. To ensure that there is no impact, it is ensured that the different versions (2023 or 2024) of the power supply board or driver board are interchangeable in order to isolate any changes.

The different configurations tested and their abbreviations are summarised in *Table 21* below. The last line of the table concerns the configuration without ferrite cores, which have proved their effectiveness during previous optimisations.

Type of test configuration	Version of driver power supply board	Version of driver board
D.S23 + D23	2023	2023
D.S24 + D23	2024	2023
D.S23 + D24	2023	2024
D.S24 + D24	2024	2024
D.S24 + D24 direct link	2024 (without cores)	2024

Table 21: The different configurations of tested driver and their abbreviations

A number of observations were made with the *Figure 181*. The first is that the full 2024 driver configuration is the most stable. By changing both the driver power supply board and the driver board, it was possible to reduce overvoltage of V_{DS} signals during the turn-off by around a hundred volts. Unwelcome oscillations on the V_{GS} signal are also significantly reduced compared with the 2023 configuration, both at turn-on and turn-off.

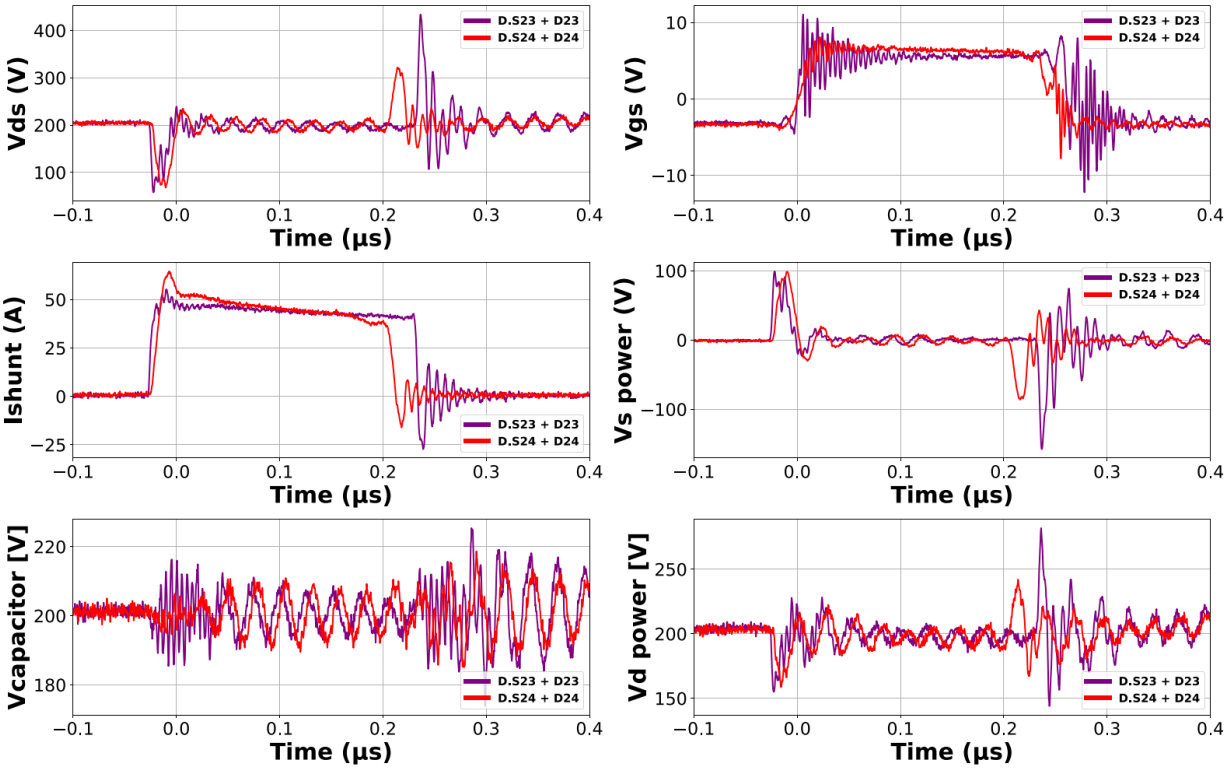

Figure 181: Experimental signals of the p-GaN component from supplier 2 for two versions of driver power supply board and driver board (2023 versus 2024) on 2023 test-board

Another observation is that with this configuration, the addition of ferrite cores is no longer essential. There is no difference in the yellow and green curves shown in Figure 182.

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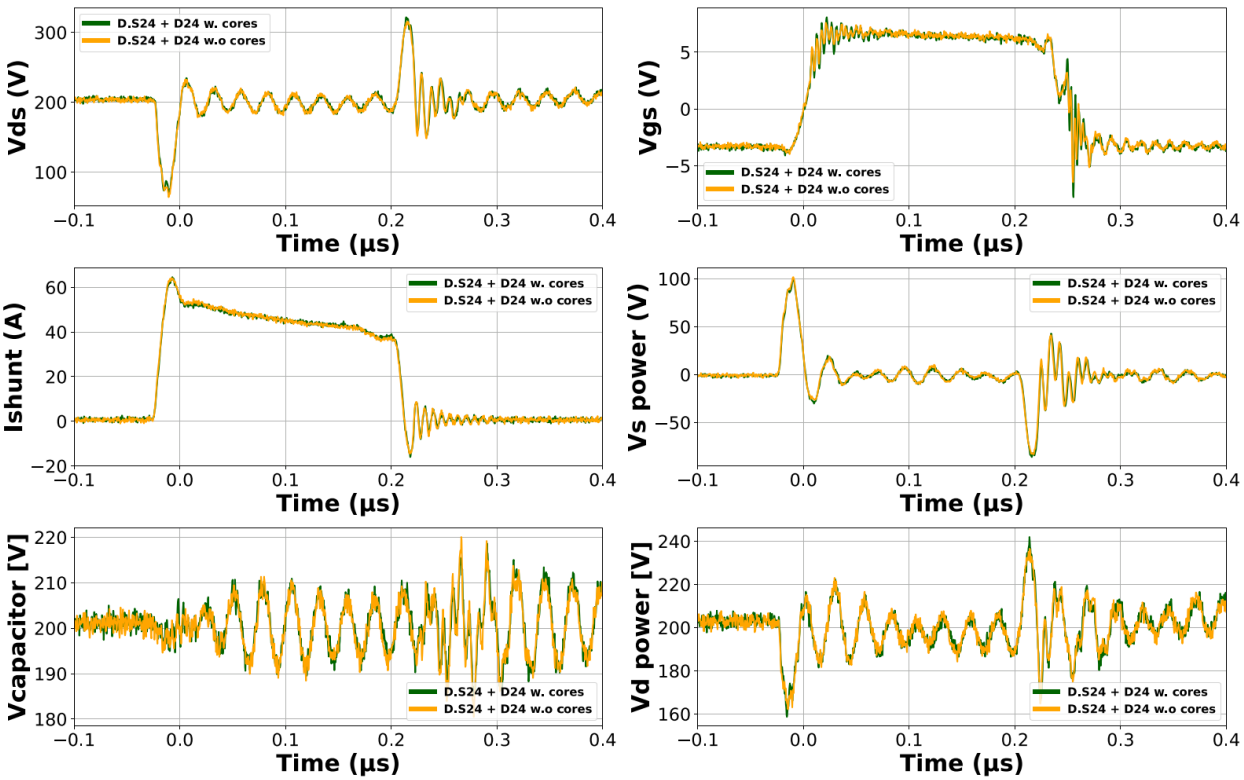

Figure 182: Experimental signals of the p-GaN component from supplier 2 with or without ferrite cores attached to 2024 driver board

Finally, it is the complete 2024 assembly that stabilises the operation of the test bench with the components from supplier 2. The *Figure 183* below illustrates the crossed cases, with the driver 2023 power supply board coupled to the driver 2024, or conversely the driver 2024 power supply board coupled to the driver 2023. These tests show that this crossover does not stabilise the operation of the bench.

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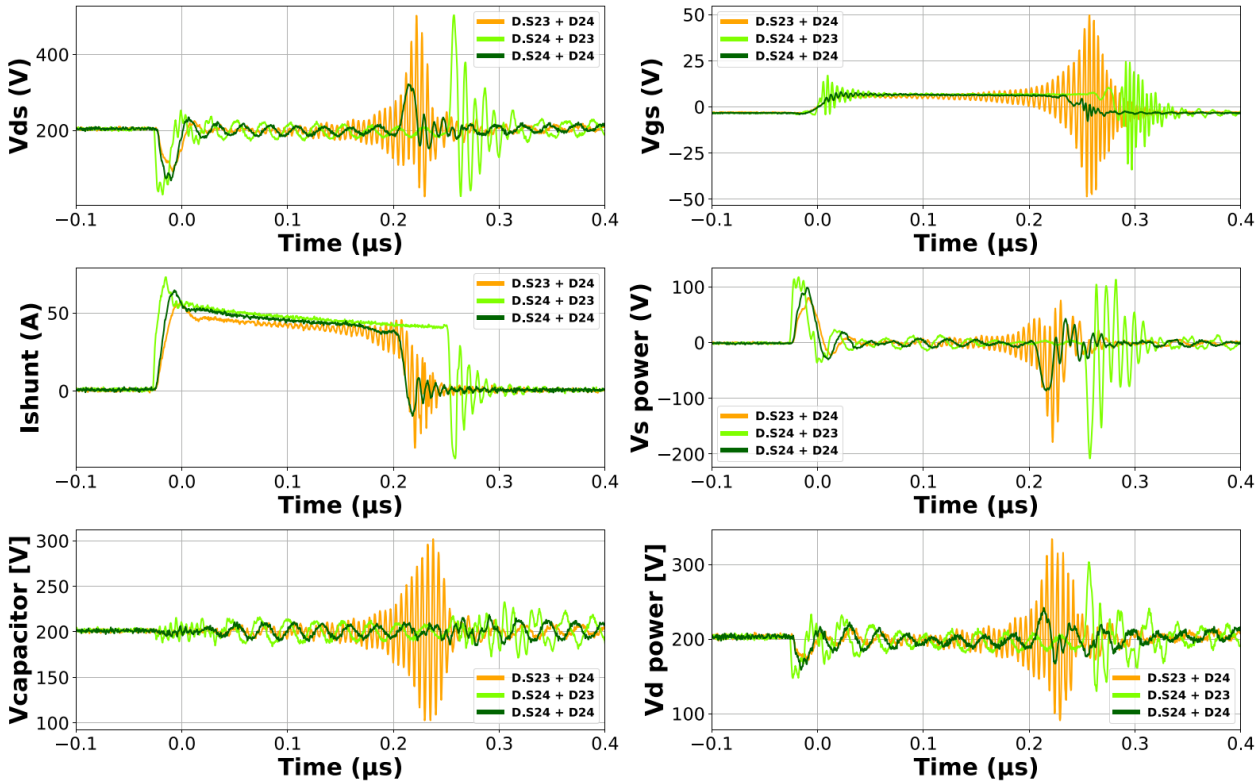

Figure 183: Experimental signals of the p-GaN component from supplier 2 with crossed configurations (2023 and 2024)

Using converters with a lower isolation capacity is therefore not enough, as can be seen from the D.S23 + D24 configuration. Just as changing only the driver is not enough, as can be seen from the D.S23 + D24 configuration, whose results are also not very stable.
While the benefit of the new 2024 converters can be attributed to their lower isolation capacity, the benefit of the new 2024 driver can be explained by its lower switching speed. This slower switching speed, observed on the rising edges of the various signals, remains relative, however, at 15 ns compared with 25 ns.

This new configuration of the driver power supply board and driver board assembly enables the following reductions in overvoltage to be achieved as shown in Table 22 below.

	Max $V_{DS,HIGH}$ (V)	**Max $V_{GS,HIGH\ (+6V)}$ (V)**	**Min $V_{GS,LOW\ (-3V)}$ (V)**	**Min $V_{S,POWER}$ (V)**
2023 Version of Driver (D.S23 + D23)	434	11	-12	-157
2024 Version of Driver D.S24 + D24 direct link	322	8	-8	-86
Reduction	**26%**	**27%**	**33%**	**45%**

Table 22: Results of the p-GaN component from supplier 2 for two versions of driver, for V_{DS} = 200 V

Similar tests have been conducted for the components from supplier 1 and it gave the same results as shown in Figure 184 and in Table 23 .

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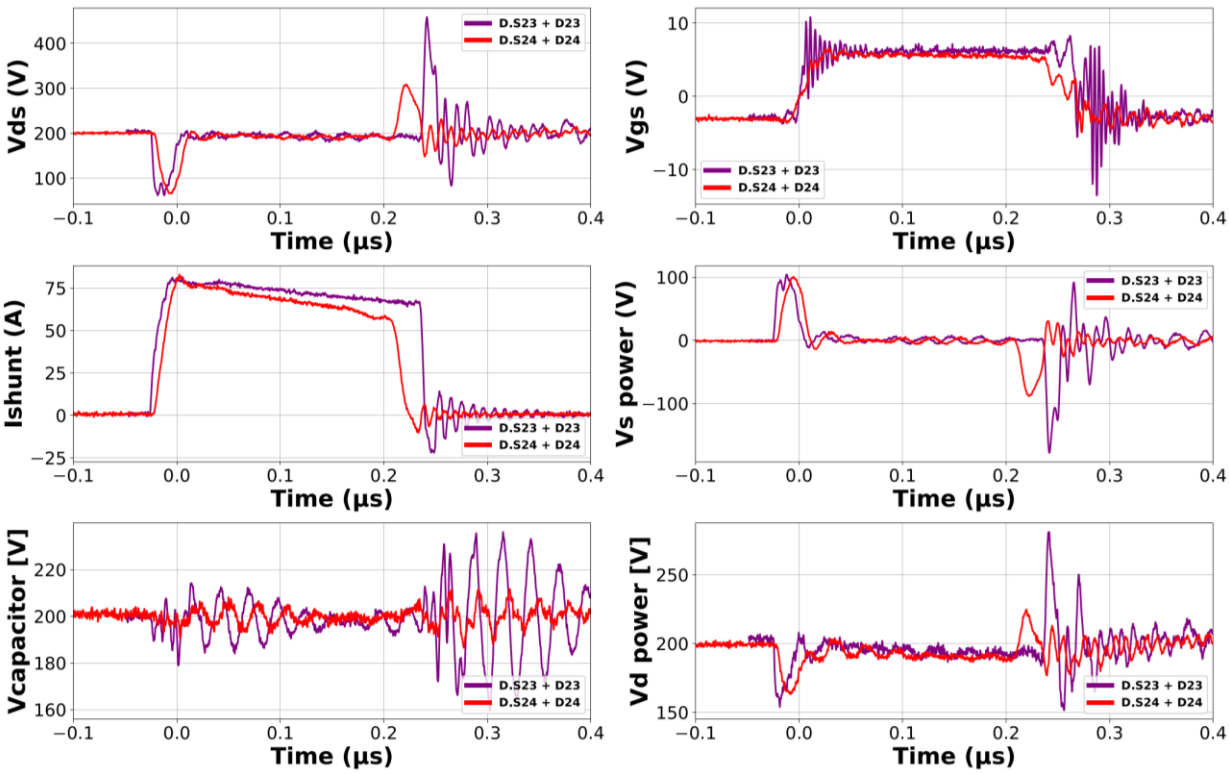

Figure 184: Experimental signals of the p-GaN component from the first supplier for two versions of driver power supply board and driver board (2023 versus 2024)

	Max $V_{DS,HIGH}$ (V)	Max $V_{GS,HIGH\ (+6V)}$ (V)	Min $V_{GS,LOW\ (-3V)}$ (V)	Min $V_{S,POWER}$ (V)
2023 Version of Driver (D.S23 + D23)	458	11	-14	-178
2024 Version of Driver D.S24 + D24 direct link	308	6.5	-5	-88
Reduction	**33%**	**41%**	**64%**	**51%**

Table 23: Results of the p-GaN component from supplier 2 for two versions of driver, for V_{DS} = 200 V

This new version of driver, formed by the power supply board 2024 and the driver board 2024, enables not only to reduce oscillation on component from supplier 2 but also to reduce overvoltage on V_{DS} and V_{GS} signals for components from both suppliers as shown in Figure 183 and Figure 184.

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2.4 Test-Board 2024

2.4.1 New Strategy

On the strength of the tests and optimisation of the experimental bench for normally-off components, it was decided to design a new board to further reduce the visible disturbances on the V_{GS} and V_{DS} signals. Parasitic inductances are a critical parameter. To minimise these as much as possible, it was decided to give-up the mother-board/daughter-board strategy and return to single-board operation. The major advantage of mother-board/daughter-board logic was the ability to test components with different footprints. This is no longer possible with the single board strategy. Nevertheless, the p-GaN components from the two suppliers have a very similar footprint, so this latest study focuses on these components.

The board layout is different, with track lengths reduced as much as possible. The component sarcophagus is now under the board in order to minimise track lengths, as shown in Figure 185(c).
A vertical shunt is preferred because its connection to the board results in less loop inductance.

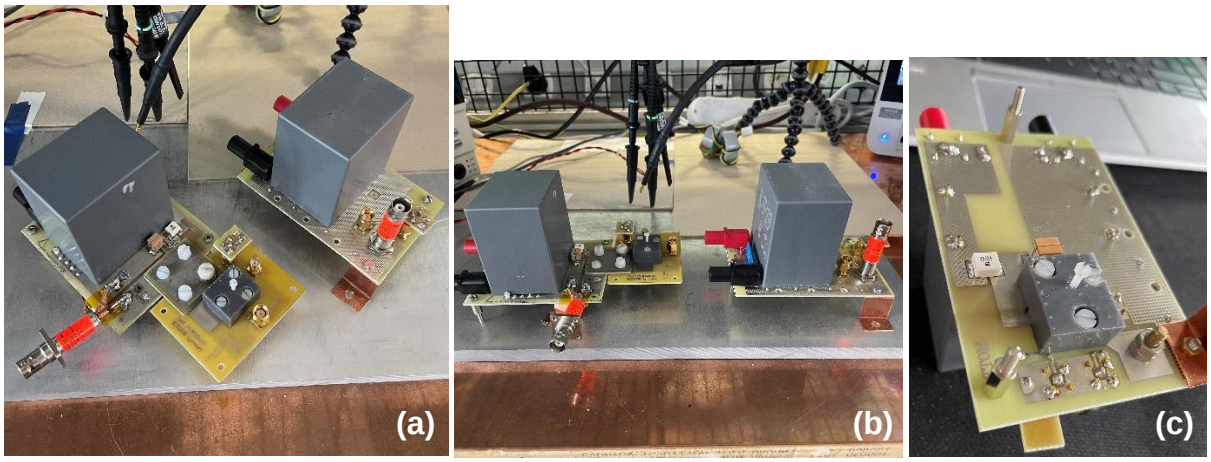

Figure 185 (a & b): 2023 Test-Board (left) and 2024 Test-Board (right);
(c): underside of the 2024 Test-Board with the sarcophagus

2.4.2 A Board Supposed to Work Better... but Does not Work as Well !

The first tests were carried out with the old driver configuration, i.e. the "2023" reference material with looping through the ferrite cores. As a reminder, this configuration was used to stabilise the 2023 version of the experimental bench. While the bench operates stably at V_{DS} = 100 V, as shown in Figure 186, the situation is different at V_{DS} = 150 V, as shown in Figure 187 in red, where V_{GS} and V_{DS} present so much oscillation that the component cannot operate properly .
The fact that the signals are stable indicates that there are no routing problems; the test-bench works but is parasitized.

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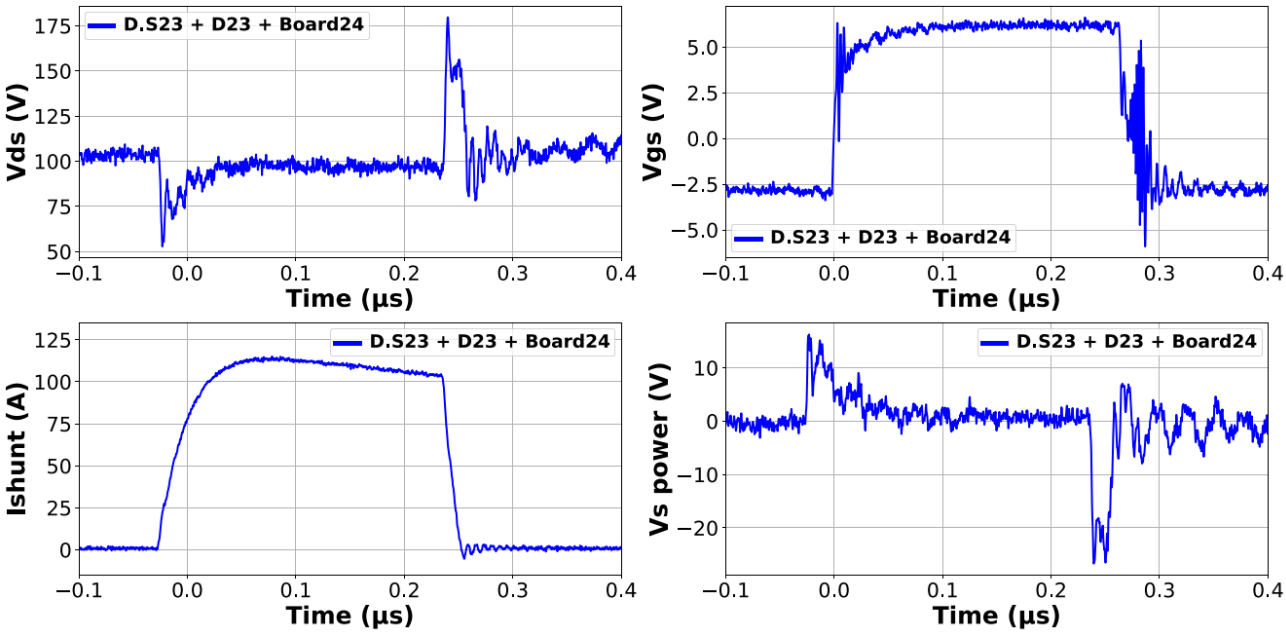

Figure 186: Experimental waveforms for the first conducted for V_{DS} = 100 V and with the 2023 driver configuration

It was therefore decided to use the driver in its 2024 configuration. The driver power supply board and the driver board are directly linked as it was previously conducted. The signals are not improved and are even disturbed from V_{DS} = 100 V in purple in Figure 187. In view of this and in an attempt to improve, it was decided to add ferrite cores to driver 2024, as it has been done for configuration 2023 but which no longer seemed necessary.
This configuration gives some stabilised results, in green in Figure 187. However, it becomes totally chaotic again as soon as V_{DS} reaches 200 V, as shown in Figure 188.

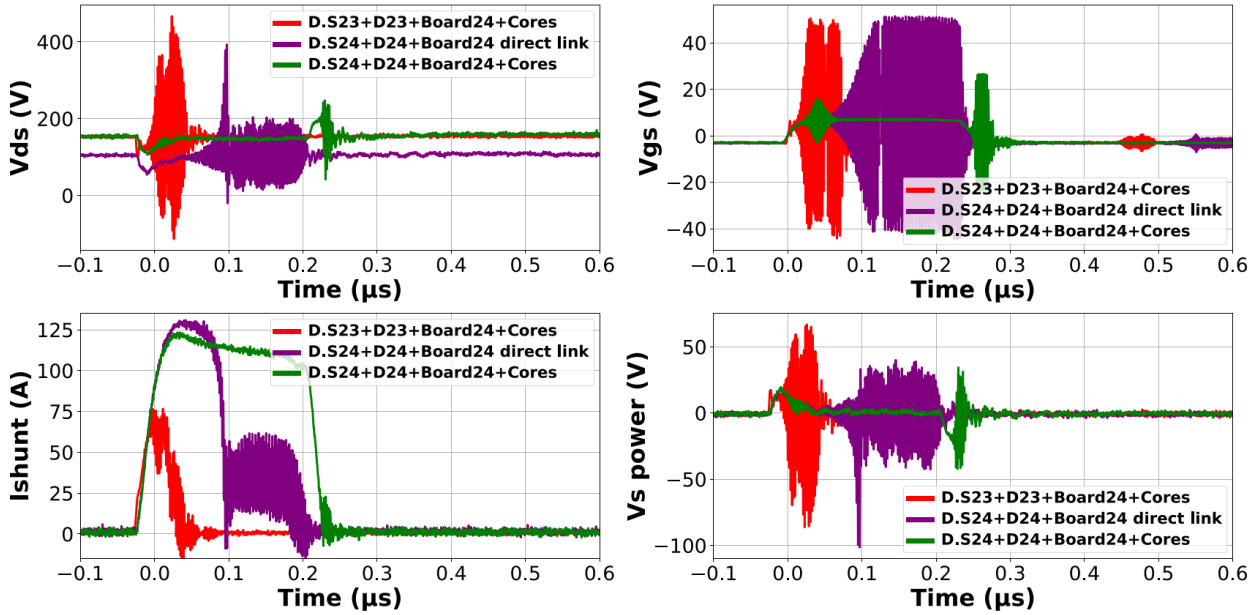

Figure 187: Experimental waveforms for different driver configuration

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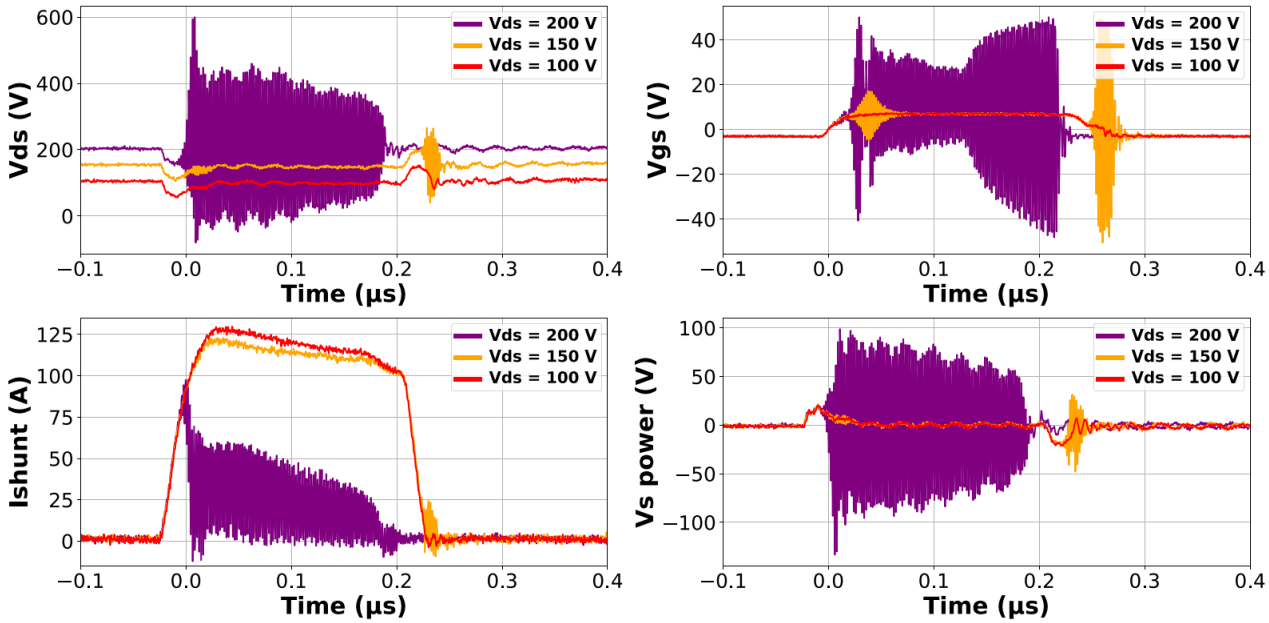

Figure 188: Experimental waveforms with cores added to 2024 driver configuration for an increased V_{DS}

Despite the difficulties in operating this board at V_{DS} voltages in excess of one hundred volts, it seems very interesting to succeed in stabilising it. Indeed, the comparison for V_{DS} = 100 V in Figure 189 shows that the new design has greatly reduced the overvoltage of the V_{DS} signal, the voltage drop at turn-on is much reduced compared with the 2023 board and the V_{GS} signal is also much less parasitic, with no oscillations and virtually no overvoltage.

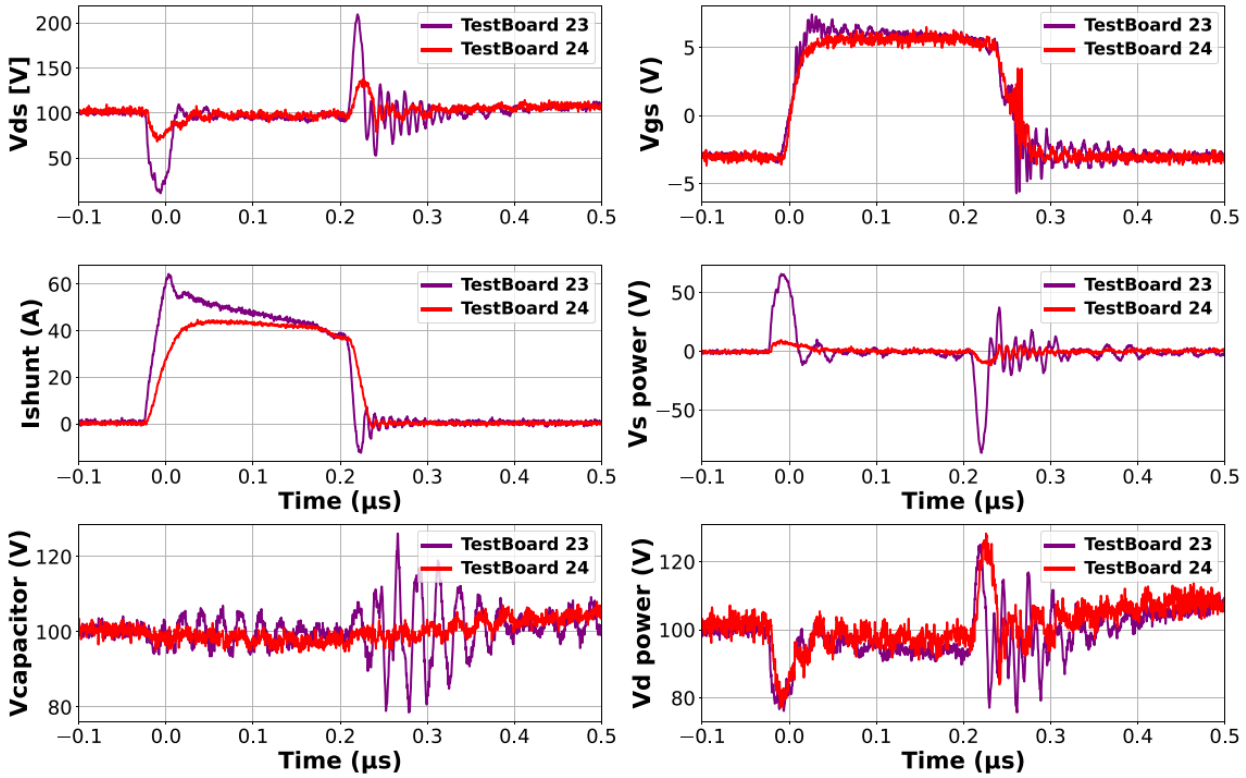

Figure 189: Comparison of the two versions of test-board 2023 and 2024

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2.4.3 Various Optimisations, Successful to a Certain Extent

The fact that the Test-board 2024 works perfectly for V_{DS} = 100 V signals but is extremely disturbed for a higher drain-source bias suggests the presence of electrostatic coupling.

2.4.3.1 Driver Shielding

Given the shape of the signals, it seems likely that it is the disturbance of the V_{GS} signal that causes this erratic behaviour. A first attempt at a solution was therefore to shield the driver. The driver board was wrapped in capton scotch to avoid potential short circuits, then covered with copper foil, connected to ground.

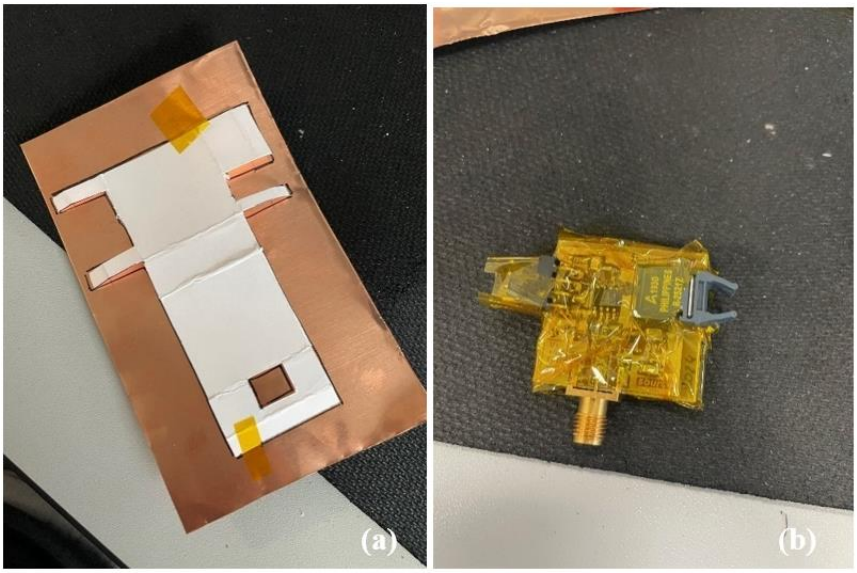

Figure 190: Pattern of the driver on the copper sheet (left) and wrapping of the driver board in capton scotch

Shielding the driver makes no difference, the signals remain very noisy and the bench is inoperable at V_{DS} voltages in excess of 150 V.

At this stage, several things have been tried, with the removal of all the probes apart from the one measuring the V_{GS} signal, and the removal of the shunt whose presence, as it has been seen a little earlier, is not without impact. These attempts at optimisation, as well as the shielding of the driver, did not produce any interesting results.

2.4.3.2 Increase the Distance of the Driver Unit

An attempt was also made to move the driver board further away, because of possible electromagnetic coupling with the power section. Two positions were studied, with the entire driver board placed either on the left-hand side of the bench, above the driver power supply (Figure 191-b), or on the right-hand side, towards the oscilloscope (Figure 191-c). These positions, shown in Figure 191, are compared with the initial position (Figure 191-a) where the driver board is plugged directly into the test board, without any connection wires and as close as possible to the component.

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Figure 191: Various driver positions away from the power section (a): initial position, (b) top left position,(c) position on the right

The Figure 192 compares the results of the different locations. In order to avoid any possible disturbance and to reduce the parasitic inductances potentially affecting the operation of the test bench, the shunt was disconnected and replaced by a bolt and screw assembly in order to connect the two planes of the test board. Figure 192 shows that none of the three positions gives stable V_{DS} or V_{GS} signals.
The initial situation (*Figure 191*-a) is represented by the purple curve. The other two positions (*Figure 191*-b and *Figure 191*-c) are represented by the orange and red curves. These last two positions give distinct results compared with the initial case, but not satisfactory results. For both the orange and red curves, the turn-off disturbances after 200 ns of conduction, are far too great for the device. Repetitive tests at higher V_{DS} voltages are out of the question at this stage, and other optimisations need to be found.

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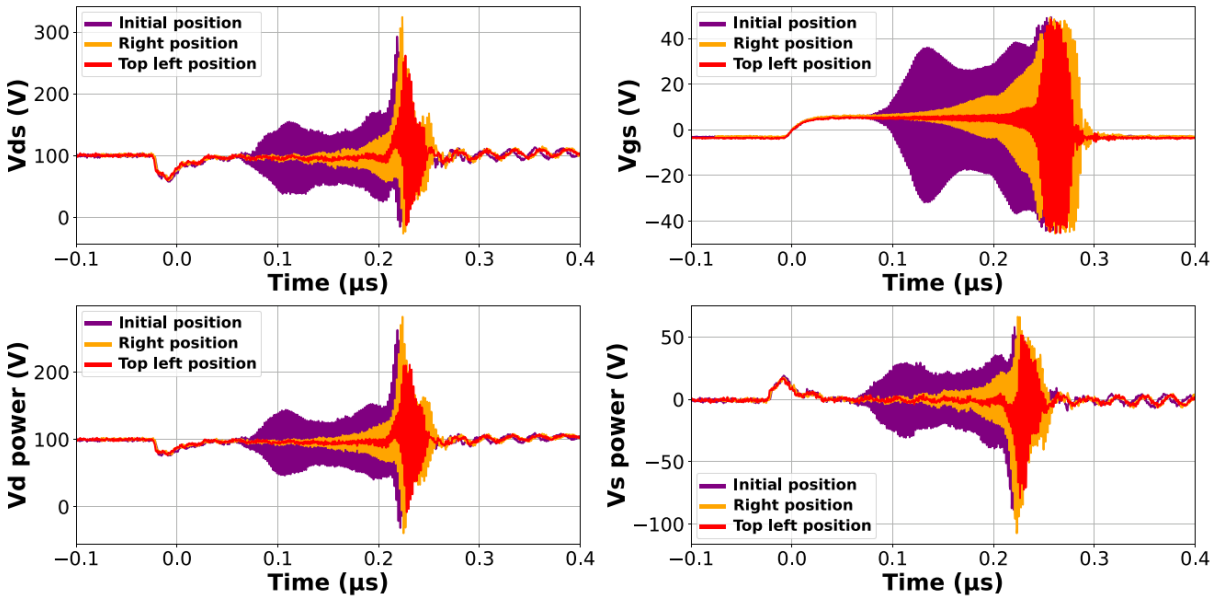

Figure 192: comparison of different locations of driver

2.4.3.3 *Separation of $V_{S,KELVIN}$ et $V_{S,POWER}$ Potentials*

After several weeks of testing, and the switchover to the functional 2023 Test-Board for tests at V_{DS} = 200 V or even V_{DS} = 300 V, as explained later in Chapter 3, two other optimisations on Test-Board 2024 were considered. Initially, when the board was designed, it was decided to combine the $V_{S,KELVIN}$ and $V_{S,POWER}$ potentials. Given the apparent disturbance of the V_{GS} signal, and the possibility of electrostatic coupling, it was decided to separate these two potentials in order to isolate the V_{GS} signal from any power-related disturbance, as shown in Figure 193.

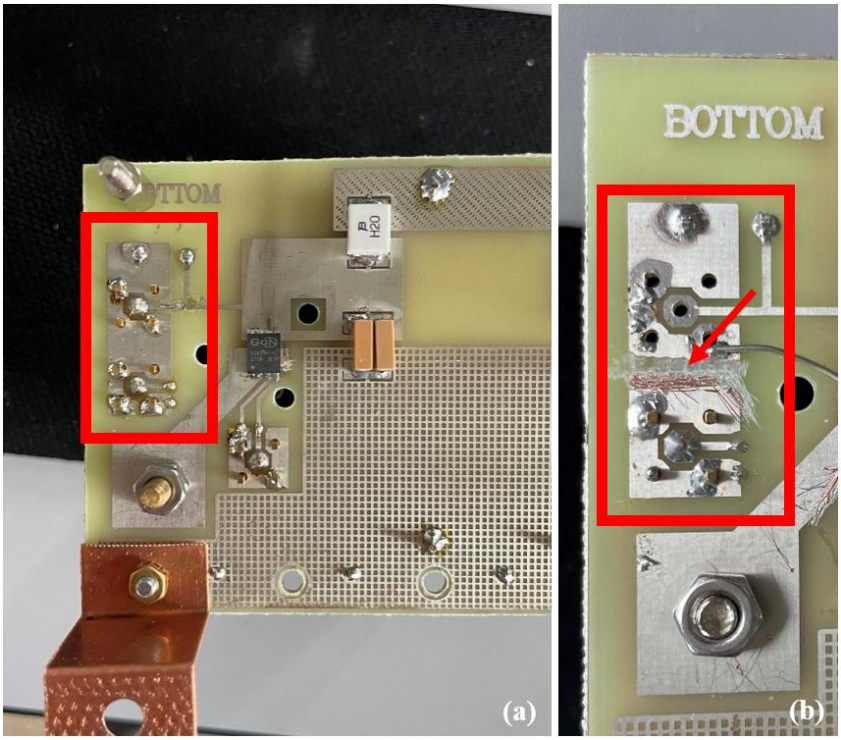

Figure 193: separation of the two potentials $V_{S,KELVIN}$ and $V_{S,POWER}$. (a): together, (b) separated potentials

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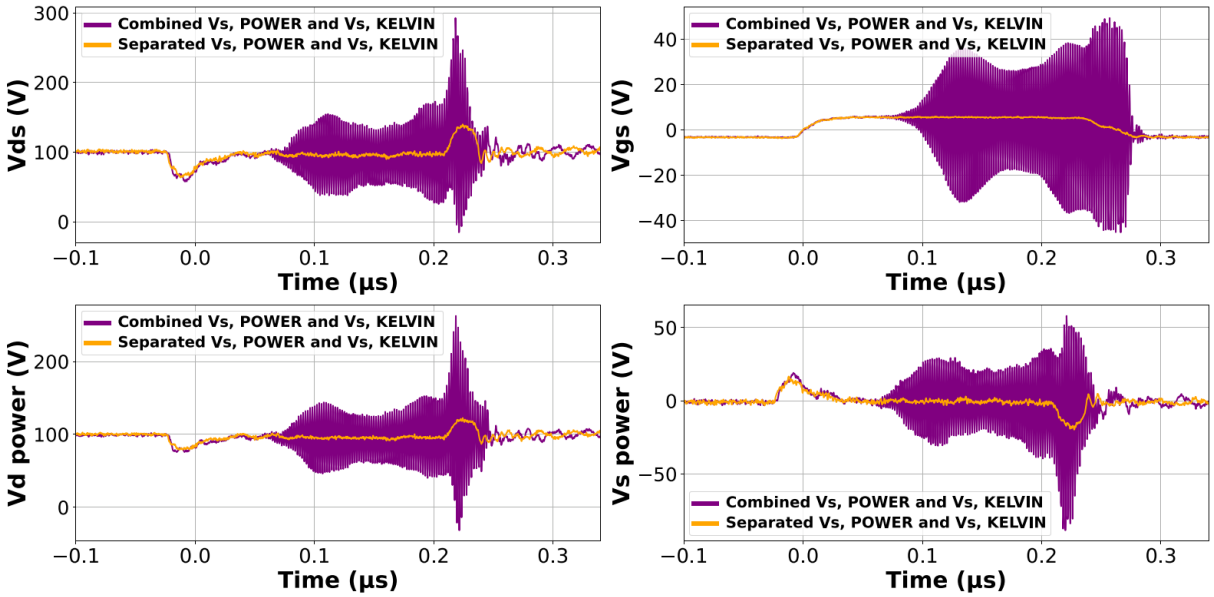

Figure 194:Experimental comparison for combined or separated potentials $V_{S,KELVIN}$ and $V_{S,POWER}$

Figure 194 illustrates these results with a comparison for combined or separated V_S potentials at V_{DS} = 100 V. The comparison with the first results when the potentials $V_{S,POWER}$ and $V_{S,KELVIN}$ were combined is unequivocal. With separated V_S potentials, the experimental waveforms are stable. V_S potentials do indeed need to be separated. Thanks to this new optimisation, it has been decided to wonder if the results of Figure 194 are still valid at a higher value of V_{DS}. Figure 195 illustrates the test with a drain – source voltage V_{DS} from 100 V to 200 V. Signals are perfectly stable up to V_{DS} = 150 V. Nevertheless, the turn-off seems to be a little bit disturbed. This disturbance increased for the second test conducted at V_{DS} = 200 V (violet curve in Figure 195) and hence need to be taken into account. Moreover, these results are still difficult to validate because of their complicated reproducibility. The solution will ultimately lie elsewhere, and is described below.

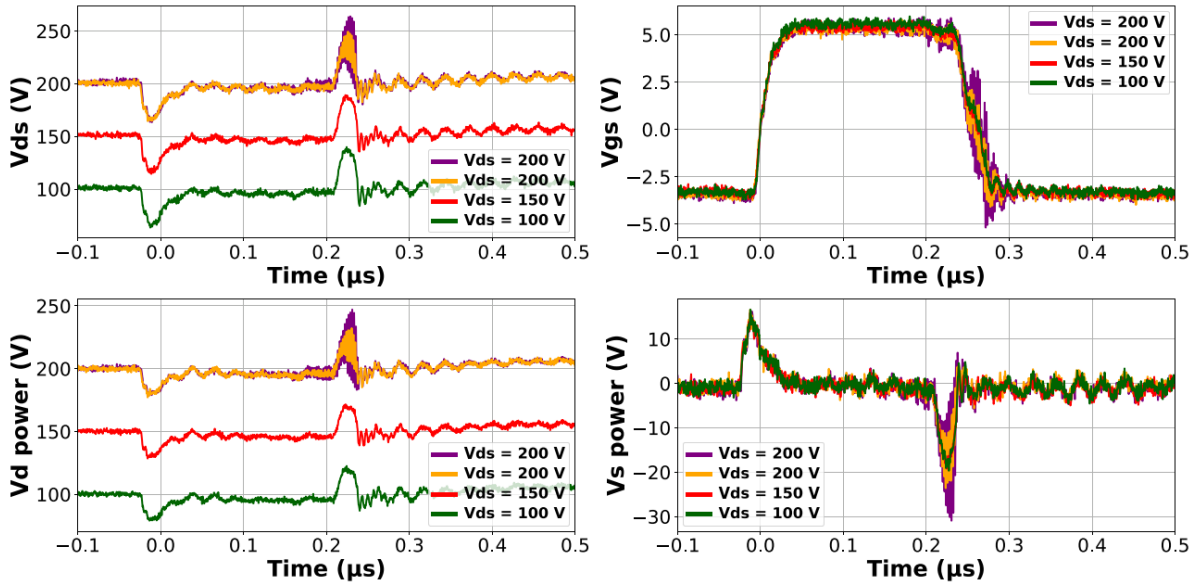

Figure 195: experimental waveforms after the separation of $V_{S,\,KELVIN}$ and $V_{S,\,POWER}$ potentials

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2.4.3.4 Impact of the Electromagnetic Coupling

The final solution was found by acting not on the driver directly, but on the driver's power supply board housing the DC/DC converters. By rotating the board on its screw axis, the impact of the electromagnetic radiation can be clearly seen. The remote position of the driver power supply board, which will be called position 2, gives extremely stable results, in contrast to the close position, which will be called position 1, which gives disturbed results in the same way as those obtained previously during unsuccessful optimisation attempts.

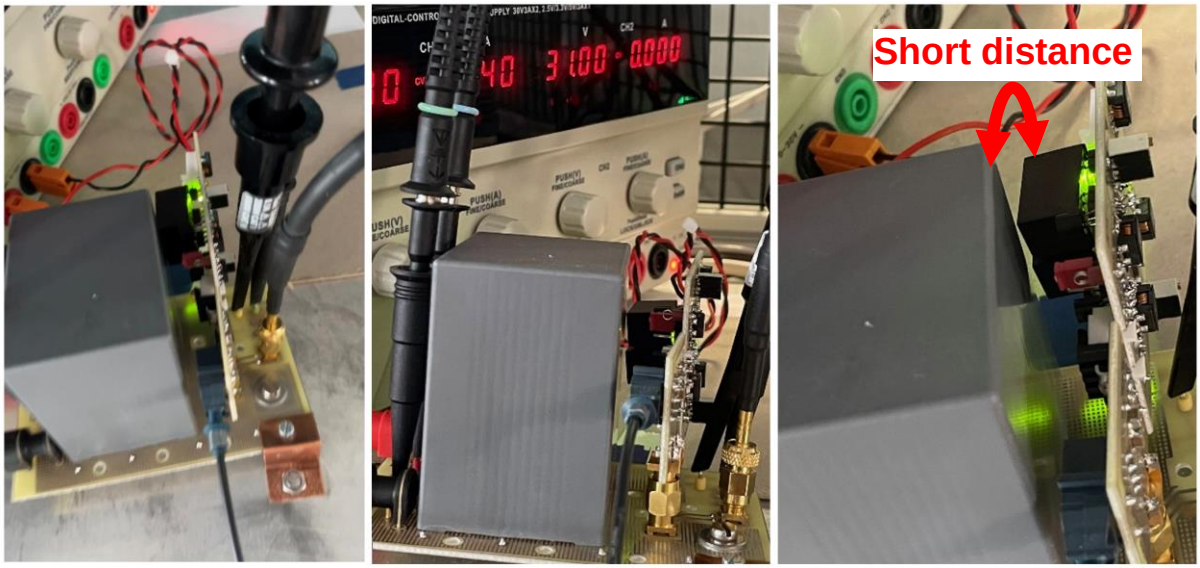

Figure 196: Driver Board in position 1 (close to power capacitor)

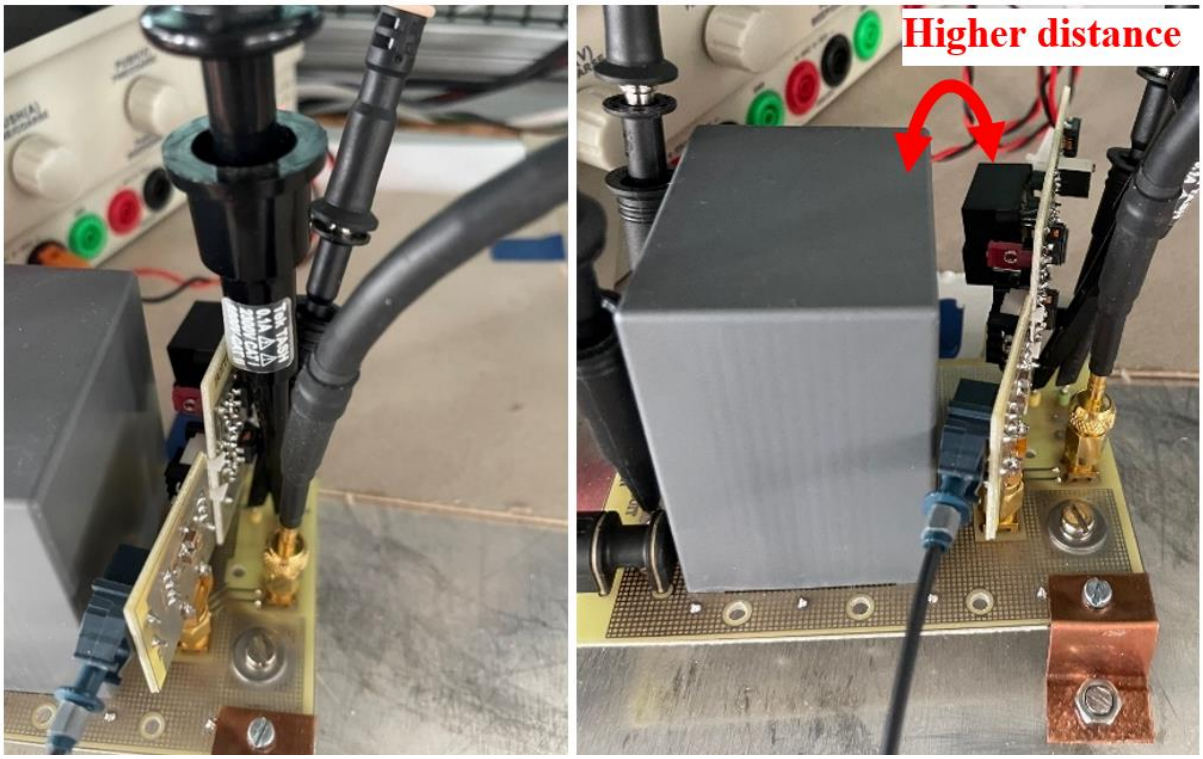

Figure 197: Driver Board in position 2 (remote DC / DC converters from power capacitor)

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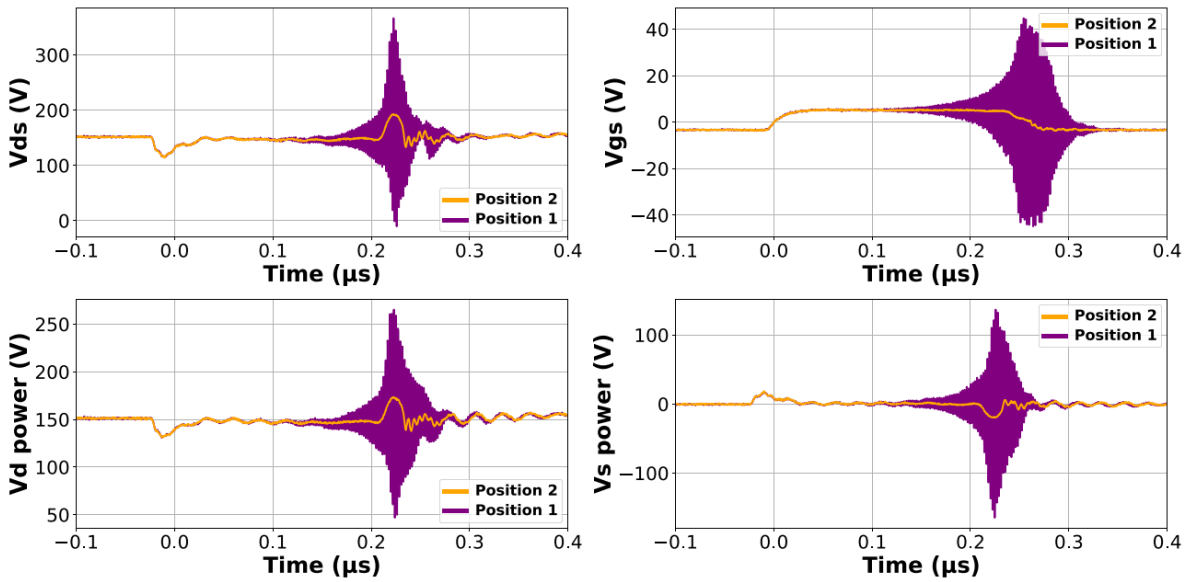

Figure 198: Experimental waveforms to compare the impact of the position of the driver for V_{DS} = 150 V

The results in Figure 198 mark a turning point, since for the first time the signals are stable and show no disturbance at V_{DS} = 150 V.
Given these results and the reduced risk of breakage, it was decided to test for V_{DS} = 200V.
Figure 199 shows the good stability of the signals following the correction applied. The tests were carried out on three separate days to ensure good repeatability.
The variation in the V_{GS} signal for tests CC1 and CC4 is due to an initial wrong calibration of the IsoVu probe.
The effort to reduce the loop inductance by reducing the size of the Test-Board was not enough. It has been seen that it was very important to consider the common mode current and the position of the driver, separating the $V_{S,\,POWER}$ and $V_{S,\,KELVIN}$.

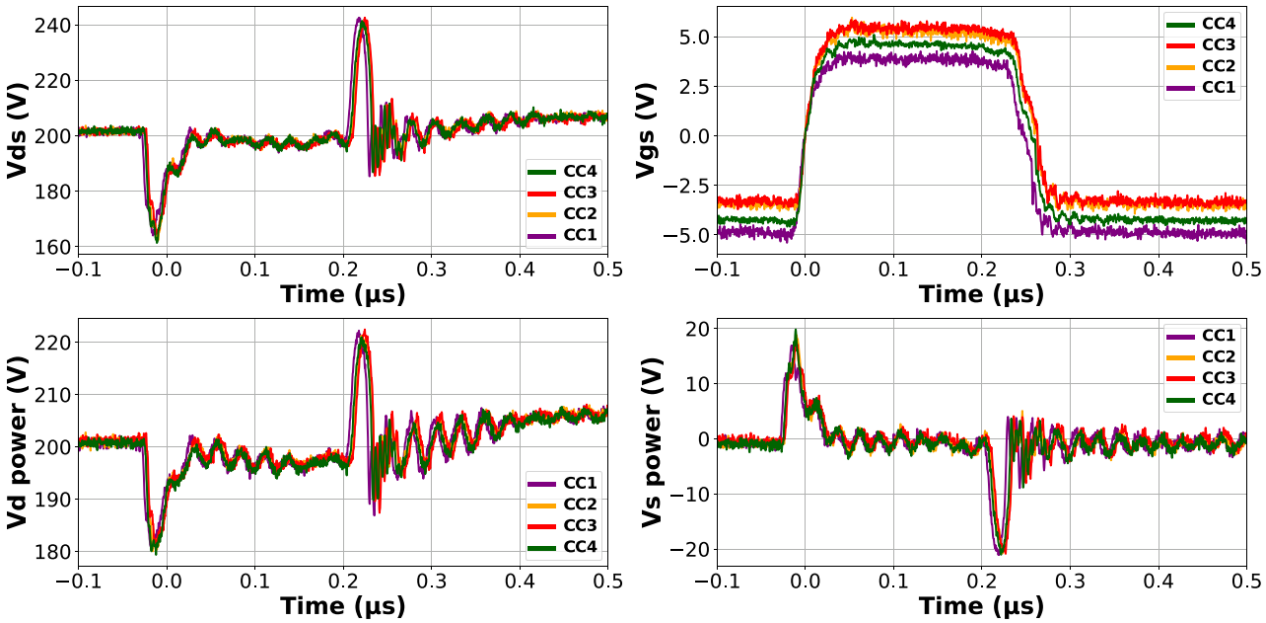

Figure 199: Repetitive short-circuits for the stabilized 2024 test-bench for V_{DS} = 200 V

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The stabilisation of the test bench enables a comparison to be made with Test-Board 2023, and Figure 200 shows the superior performance of the 2024 version (see *Table 24*). The Test-Board 2024 curve shown below is produced in its most stable configuration, i.e. without the shunt, with a bolt in its place. The voltage drop at turn-ON is greatly reduced here compared with the results for Test Board 2023. This is in line with future JEDEC standards for short-circuit testing. This reduction at V_{DS} is mainly due to the stabilisation of the $V_{S,\,POWER}$ potential. The $V_{D,\,POWER}$ potential is virtually unchanged. The V_{GS} signal is also greatly stabilised, with non-existent oscillations and extremely reduced overvoltage, similar to what was seen when operating at V_{DS} = 100 V. This suggests a maximum test voltage V_{DS} greater than the 200 V. These tests are completed further down by an increase in conduction time from 200 ns to 1000 ns.

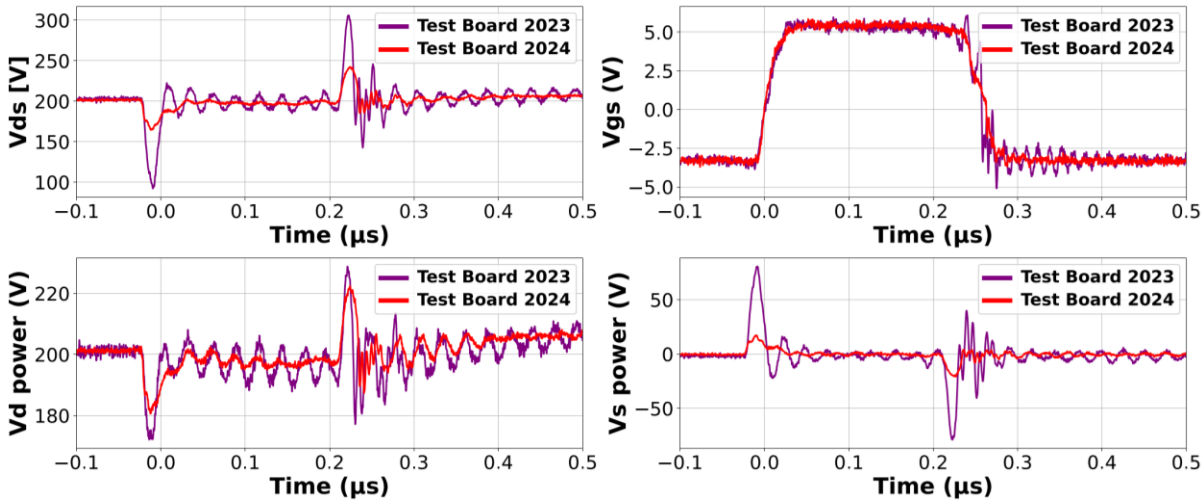

Figure 200: Comparison of experimental waveforms between 2023 and 2024 test-boards both with the 2024 driver version and p-GaN component from supplier 2

Position 2, with as steep an angle as possible between the polypropylene capacitor and the DC/DC converters, gives very satisfactory results. However, given the fact that moving the power supply board further away from the driver stabilises the experimental bench, it seems wise to test whether moving it further away from the driver improves the operation of the bench.
At this stage, the distance between the power supply board and driver board had been studied. However, the $V_{S,\,POWER}$ and $V_{S,\,KELVIN}$ potentials had not yet been separated and the fog surrounding the operation of the new board had not yet been dissipated. A test was therefore carried out on the distance between the driver and the board. The impact of the position of the driver could be studied in relation to a situation that had now stabilised, to see whether the increased distance from the driver stabilised the operation of the bench a little more or whether, on the contrary, the added length of wire proved deleterious.

	Max V_{DS} (V)	**Min V_{DS} (V)**	**Max V_S (V)**	**Min V_S (V)**
Test-Board 2023 + driver 2024	306	92	80	-78
Test-Board 2024 + driver 2024	242	164	17	-20
Reduction	**21%**	**78%**	**79%**	**73%**

Table 24: Results of the p-GaN component from supplier 2 after optimization of the test bench, for V_{DS} = 200 V

These results shown in Table 24 above are with the 2024 driver. If the comparison is focused on the first stabilized tests with the 2023 driver, the final results of this long-term optimization is even better as it is shown in Table 25 below.

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	Max V_{DS} (V)	Min V_{DS} (V)	Max V_S (V)	Min V_S (V)
Test-Board 2023 + driver 2023	432	57	96	-163
Test-Board 2024 + driver 2024	242	164	17	-20
Reduction	**44%**	**188%**	**82%**	**88%**

Table 25: Results of the p-GaN component from supplier 2 after optimization of the test bench, for V_{DS} = 200 V

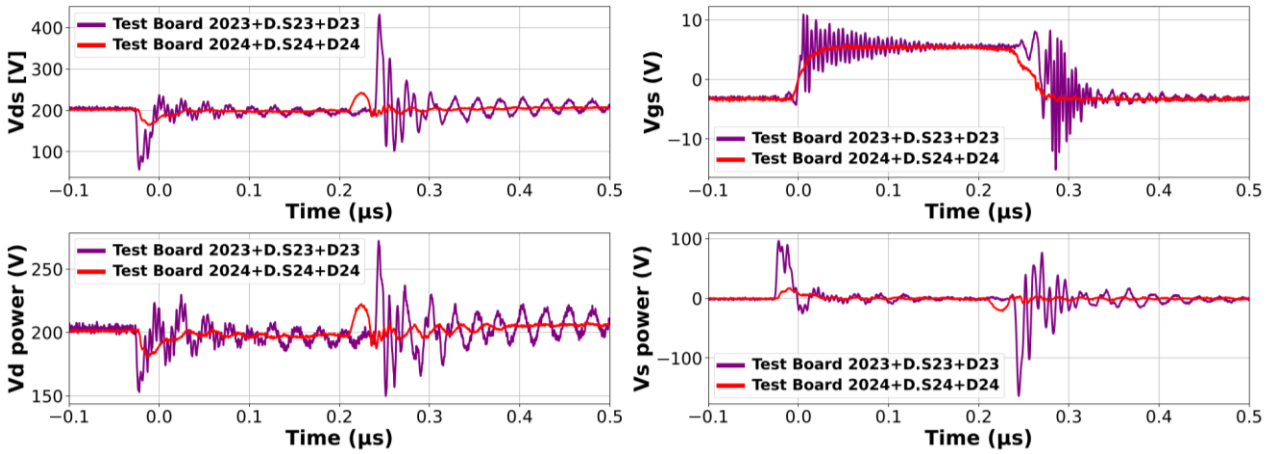

Figure 201: Comparison of experimental waveforms between 2023 and 2024 configurations (Test boards and driver boards)

As it can be seen in Figure 201, the difference between the signals from the first stabilised configuration, i.e. test board, driver board and driver power supply board from 2023, and the last signals from the 2024 configuration, i.e. test board, driver board and driver power supply board from 2024, are extremely different. The overvoltage of the various signals has been greatly reduced, as shown in more detail in Table 25. Oscillations have also become non-existent in the 2024 version. This long-term optimisation will therefore make it possible to carry out repetitive short circuits on normally-off p-GaN devices.

To confirm the previous results and gain a better understanding of the optimisations carried out, a test with the remote control was again carried out. Stabilising the operation of the test bench will allow to better visualise and understand any disturbances, or not, inherent in this remote control.

2.4.3.5 Increase the Distance of the Driver (Again)

Two positions were therefore compared, with Figure 202 (a) the stable position identified previously following the impact of the electromagnetic coupling, i.e. the driver board screwed onto the test board at a sufficient angle, and (b) a position away from the driver. Female/female adapters and a cable (50 cm length) with male connectors are used.

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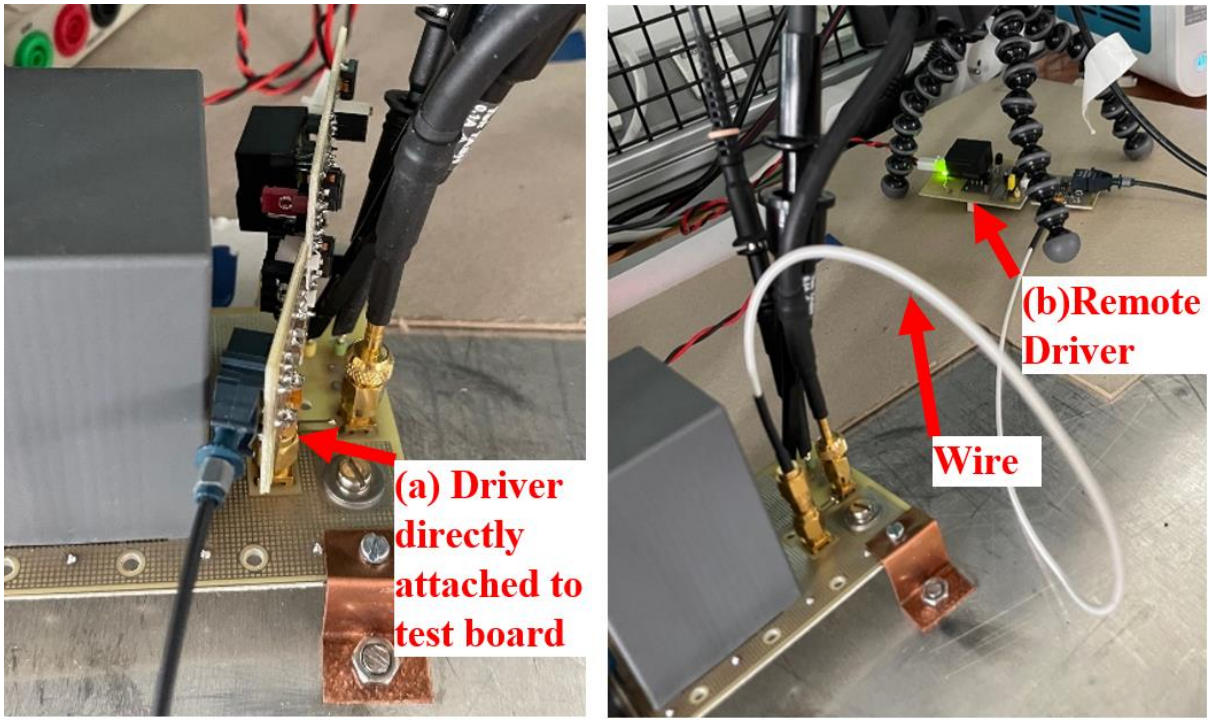

Figure 202: two studied positions of the drive, (a) directly mounted on the test board, (b) remote from test board

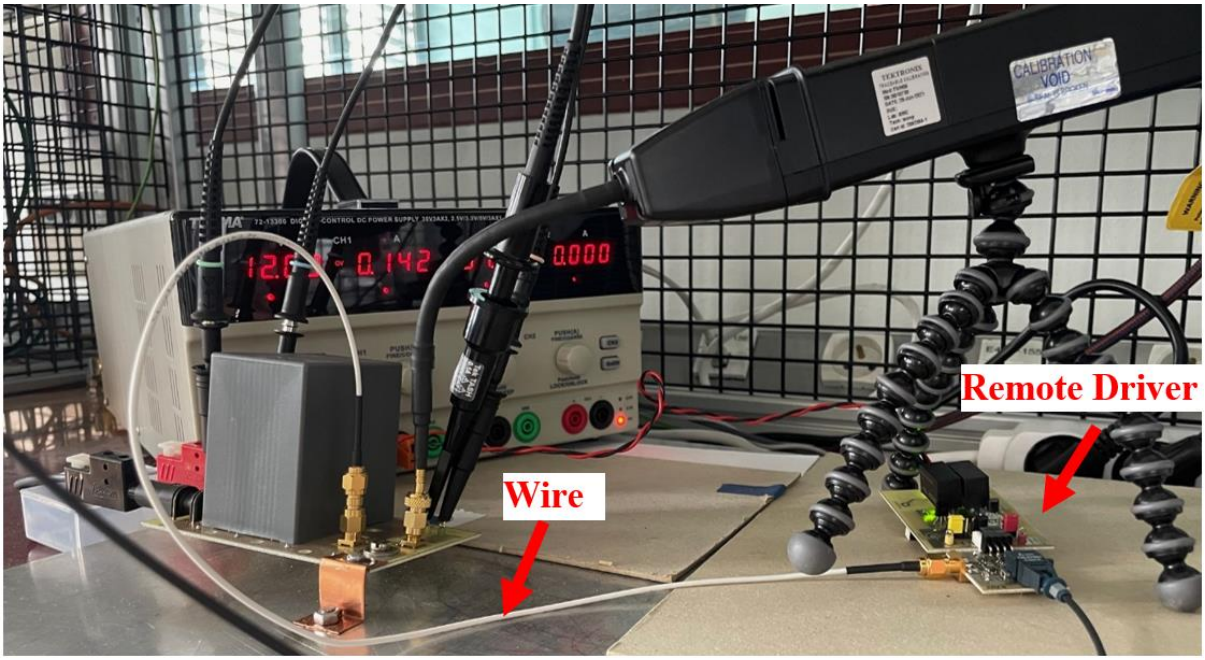

Figure 203: other view of the remote driver configuration

As it can be seen from the graphs below, the curves remain unchanged. For a drain-source bias of 200 V, the V_{DS} and V_{GS} signals are identical. Positions (a) and (b) are no more deleterious than the other, the purple and red curves overlap almost perfectly. This is an important point, as one might have feared the appearance of disturbances by adding a considerable length of wire between the driver and its connector on the test board. The inductance on the gate L_G has therefore no impact on the stabilization of the bench.

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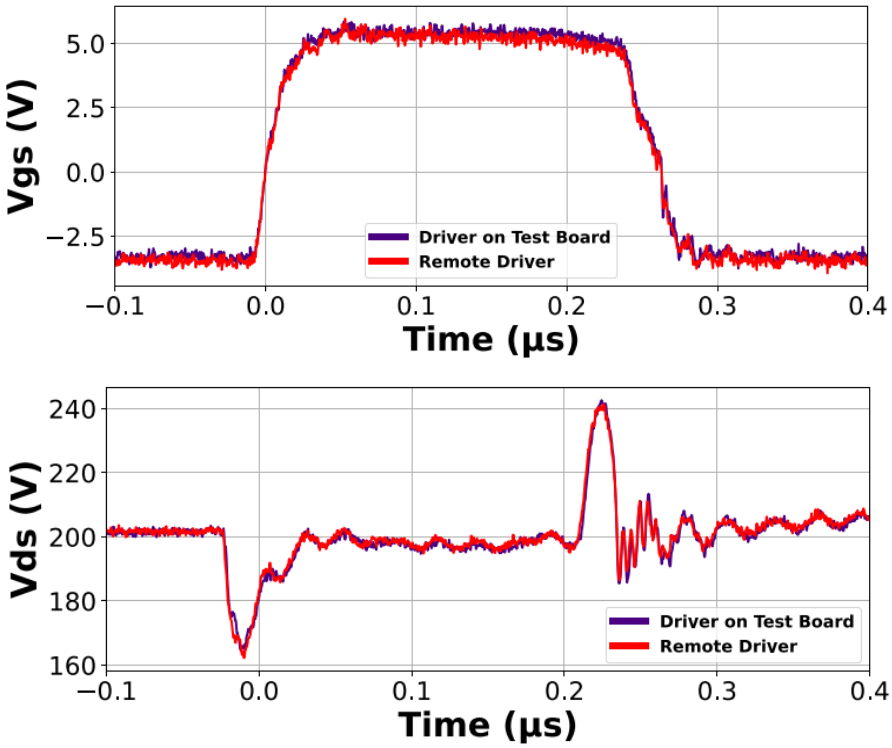

Figure 204: V_{DS} and V_{GS} signals for two different driver positions

Now that operation has stabilised, the study can move forward in two areas of research: increasing the conduction time and increasing the drain-source bias, in order to see whether the stabilisation of bench operation observed is invariant to these two areas of study.
In terms of conduction time, the short-circuit time is extended to one microsecond, compared with the two hundred nanoseconds used previously.

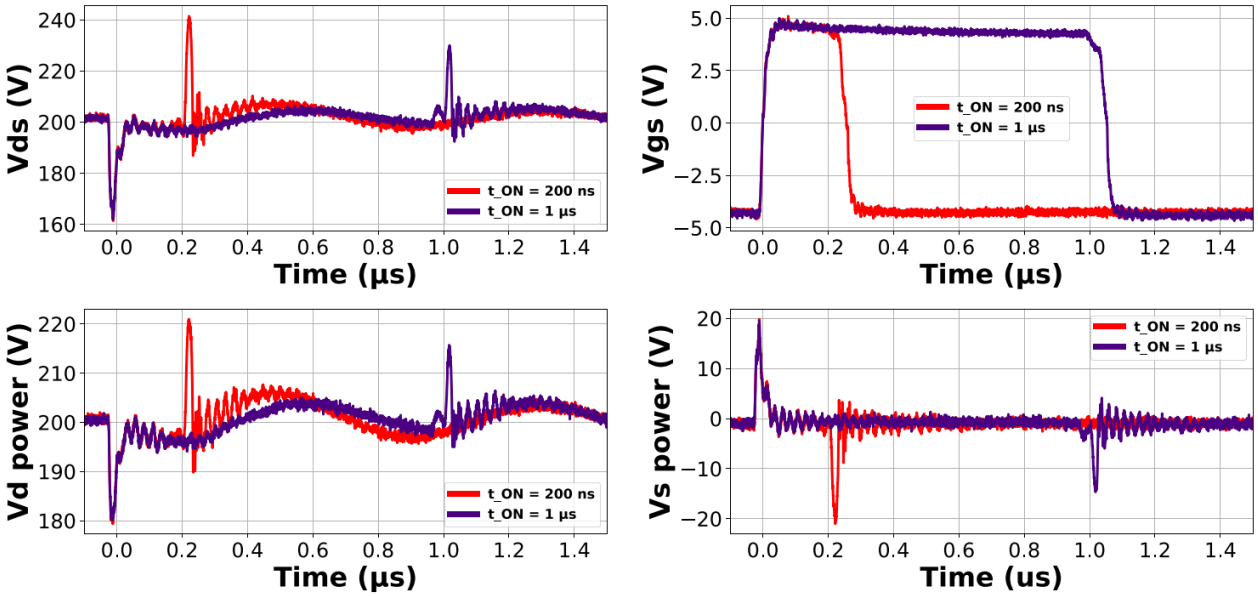

Figure 205: Experimental waveforms for an increased short-circuit time

Figure 205 above shows the various V_{DS} and V_{GS} signals and the V_D and $V_{S,POWER}$ potentials measured separately by two passive probes. Figure 205 shows the absence of instabilities following the increase in conduction time. This question was worth asking because the test board 2023, for drain-source voltages V_{DS} = 300 V, showed non-negligible oscillations in the V_{GS} signal, which increased with conduction time.

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Since increasing the conduction time did not reveal any anomalies, it was decided to work on the second aspect of the study, i.e. increasing the V_{DS} voltage with the idea of reaching 300 V, the maximum voltage at which the 2023 board can be used for components from supplier 2.

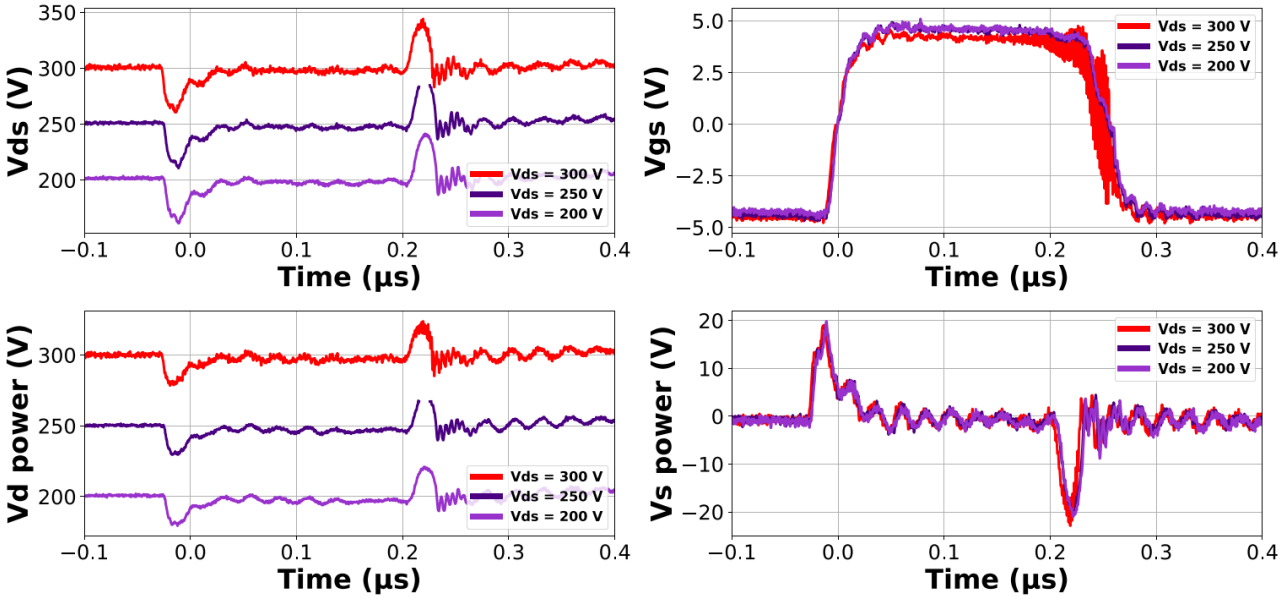

Figure 206: Experimental waveforms for an increased polarization V_{DS} up to 300 V

Figure 206 shows stable and repeatable operation of the test bench up to at least V_{DS} = 300 V. Nevertheless, the $V_{S,POWER}$ and V_{GS} signals show a slight degradation at turn-off. These disturbances can be linked to the two signals. Zooming in at turn-off, Figure 207 shows disturbances of amplitude 6 V on the $V_{S,POWER}$ signal. The same amplitude value is found for the disturbance visible on the V_{GS} signal.

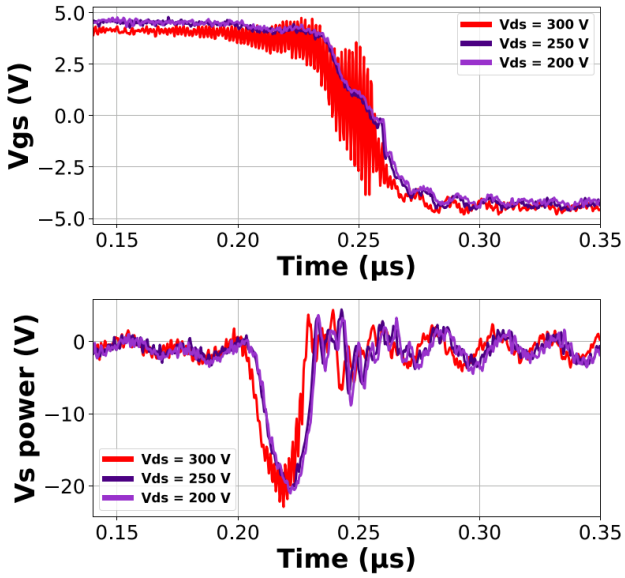

Figure 207: zoom of V_{GS} and $V_{S,POWER}$ signals during turn-off

This leads to the following conclusion: if the disturbances have been eliminated for V_{DS} = 200 V, they tend to reappear for V_{DS} = 300 V. The physical distance between the driver and its power supply board is therefore not sufficient. There are two possibilities: changing the wire connection to a larger cable, or shielding the driver and its power supply board. Adding cores in a similar way to what was done when optimising the 2023 board is also a possibility. It will be seen in the last chapter that the capacitance C_{OSS} can be a key element to stabilize the component under short-circuit and increase its robustness.

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2.5 Conclusion

Achieving repetitive, non-destructive short circuits on GaN power devices was a challenging task. Numerous optimizations were required, including the use of specific measurement probes, the reduction of parasitic inductances in the power loop, addressing common-mode currents in the driver, and implementing protections against electromagnetic interference from the power section. SPICE simulations proved invaluable for analysing, anticipating, and understanding the physical phenomena inherent to the operation of the short-circuit test bench.

This work led to the development and optimization of the first experimental bench tailored for both normally-on and normally-off components. It enables repetitive short-circuit tests at sufficiently high drain-source polarization, accounting for the voltage rating of the components and their behaviour under short-circuit conditions. The results and implications of this study are presented in detail in the following chapter.

Building on these conclusions, a second experimental test bench (cf Table 1) was developed, moving away from the motherboard-daughterboard configuration. The short-circuit performance, particularly regarding the V_{DS} voltage drop and the stability of the V_{DS} and V_{GS} signals—already improved with the first test bench—was further enhanced through the optimization of this second design.

The optimization of the various short-circuit test benches required considerable effort and time but ultimately resulted in highly stabilized signals and a significant reduction in oscillations and overvoltage. This extensive improvement now allows for repetitive short-circuit tests, detailed in Chapter 3, to be performed with greater confidence and a deeper understanding of the underlying physical mechanisms.

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3

Results

After a complex optimization of the test bench, Chapter 3 gives the final results of normally-on and normally-off components in terms of behaviour, dynamic observations and degradation following the application of repetitive short circuits. The normally-off components deliver very different behaviour and robustness under short-circuit conditions, despite relatively similar structures. Different variations and types of failure are observed. At the end of the chapter, some answers are given about the increased robustness of components from the first supplier.

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3.1 Normally-On Components

3.1.1 Tests and Behaviour of Normally-On Components

The first phase of optimization of the experimental bench enabled to carry out repetitive and non-destructive short-circuits on HEMT GaN, normally-on components. The DUT used here come from the first supplier (see Table 10) and are depletion-mode type, abbreviated d-mode.

Three batches of normally-on components are studied. They all come from the same first supplier. These three batches, named A, B and C, differ only in their location on the wafer and will be studied in turn. Significant differences were noted between the different batches of components studied.

To identify the limits of the devices under test and define an appropriate short-circuit series, various tests are carried out, including a progressive increase in V_{DS} by 25 V step. The idea is to work with a drain-source polarization that is sufficiently high in relation to the voltage rating of the device, but still able to perform several non-destructive repetitive short-circuits. This logic of repeatability means that the tests will not be carried out at the maximum short-circuit voltage of the device, but below it, in order to maintain a certain margin and to be able to have a significant number of tests and a consequent amount of energy between each electrical characterization. In parallel with these tests, the conduction time is increased.

3.1.1.1 Batch A

Initial tests (2023 Test-Board and 2023 driver) with a gradual increase in voltage are carried out, as shown in Figure 208. The DUT undergoes an initial short-circuit at V_{DS} = 25 V, then the V_{DS} voltage is increased in 25 V steps as successive short-circuits are conducted.

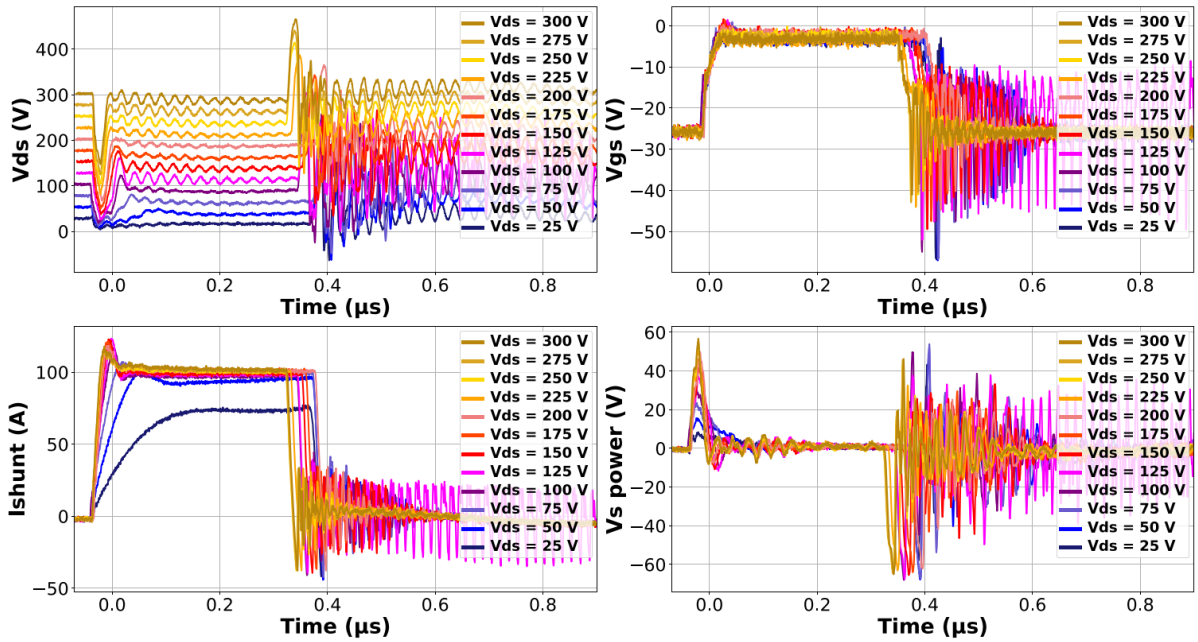

Figure 208: Experimental rise in voltage for a normally-on component, from V_{DS} = 25 V up to V_{DS} = 300 V on 2023 Test-Board with 2023 driver

Figure 208 shows a number of observations. Firstly, the maximum applied voltage recorded is 300 V. Beyond that, the component breaks. The component tested in Figure 208 breaks at V_{DS} = 325 V. The damage observed visually on the test-board is significant and is shown in Figure 209 (a & b): the drain side of the test board track shows signs of burning, and the device is completely uncapped on the upper part, as shown in Figure 209(c).

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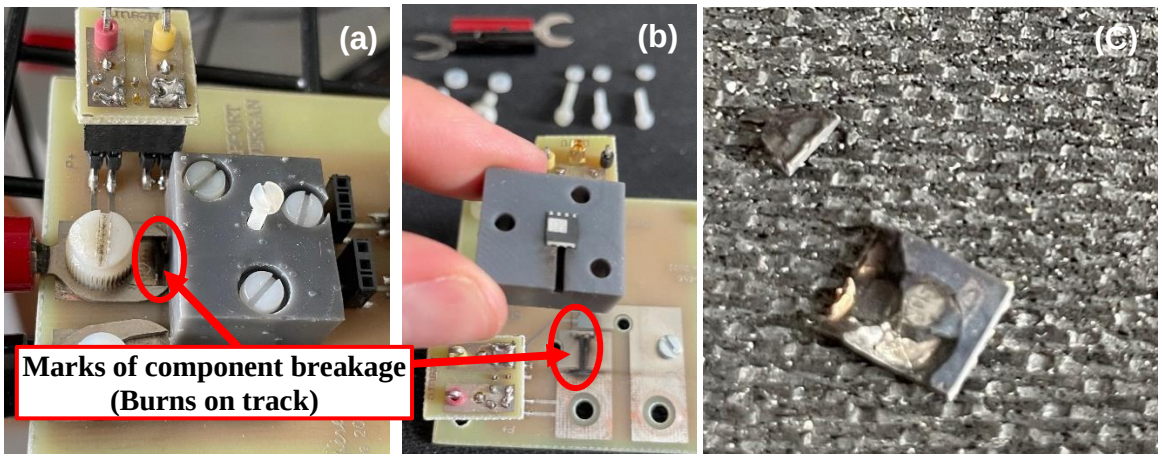

Figure 209: Results of component breakage on test board (a & b) and image of the decapsulated component (c) for V_{DS} = 325 V

The shape of the signals at V_{DS} = 300 V in Figure 208 should be considered with caution, especially in terms of overvoltage. In error, at that time, the probes used to measure the V_{DS} signal were simple passive x10 probes from Tektronix, part no. TPP0500, with a maximum operating voltage of just 300 V. This V_{DS} measurement probe will be replaced at a later date, as will be explained later in this chapter.

Figure 208 and Table 26 show that V_{DS} overvoltage are stable and do not depend on the applied V_{DS} voltage. In line with the values in Table 26, overvoltage is similar for all V_{DS} voltages, around 170 V.

V_{DS} (V)	25	50	75	100	125	150	175	200	225	250	275	300
Max V_{DS} (V)	185	234	254	280	304	321	343	365	387	415	441	466
Overvoltage (V)	**160**	**184**	**179**	**180**	**179**	**171**	**168**	**165**	**162**	**165**	**166**	**166**

Table 26: Recorded overvoltage during a rise in voltage V_{DS}

While overvoltage is stable according to the V_{DS} voltage applied, it nevertheless appears that some V_{DS} voltages are more deleterious than others. Indeed, Figure 208 shows that the oscillations in the V_{GS} signal present at turn-off diminish with increasing V_{DS} voltage. These oscillations are particularly attenuated from V_{DS} = 175 V and even more so from V_{DS} = 225 V onwards.
On the other hand, these oscillations are exacerbated and become undamped at V_{DS} = 125 V.

This is particularly apparent in Figure 210, where the V_{DS}, V_{GS}, I_{SHUNT} and $V_{S,POWER}$ signals are plotted for three distinct polarizations: V_{DS} = 100 V; V_{DS} = 125 V; V_{DS} = 300 V. Compared to V_{DS} = 300 V, V_{DS} = 100 V and V_{DS} = 125 V are particularly noisy as shown in Figure 210. While remaining at voltages that do not cause component breakage, it can be seen that the component behaves differently at different voltage levels.
This is also the case for some components in Batch B. On the other hand, it should be noted that some components do not exhibit this signal degradation.

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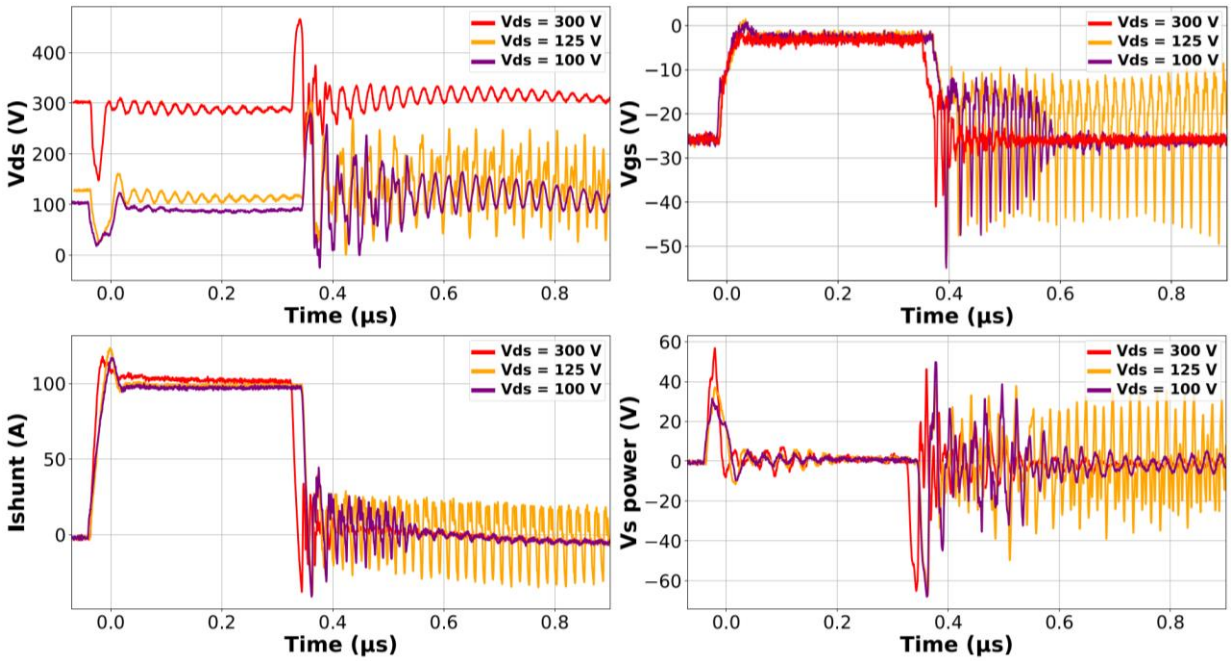

Figure 210: Experimental waveforms for V_{DS} = 100 V and V_{DS} = 125 V, compared to V_{DS} = 300 V on 2023 Test-Board with 2023 driver

According to the results of the *Figure 208*, the rise in voltage enables to decide on the voltage level selected for the series of repetitive, non-destructive short-circuits. Compared to this maximum voltage V_{DS} = 325 V, it is chosen to carry out the sequence of repetitive short-circuits at a voltage set at V_{DS} = 200 V, this drain-source polarization level being considered reduced compared to the maximum level of 325 V, but sufficient to carry out relevant short-circuit tests, notably in terms of power and energy developed. It is worth mentioning here that the peak power during breakage of DUT is around 33 kW, to be compared with the maximum power of a motorcycle for a young licensee, located at 35 kW. On a relatively small element (5x6 mm), the power dissipated therefore appears huge.

The impact of these repetitive short-circuits on the DUT is detailed in the last chapter. At the same time, tests were carried out on components from other batches.

3.1.1.2 Batch B

Similar to the tests carried out on components from batch A, a gradual voltage rise up to V_{DS} = 200 V is carried out for components from batch B in Figure 211. The tests were also conducted with the same configuration, with the 2023 Test-Board and 2023 Driver and Driver Supply Boards. Although a few slight oscillations can be observed, which are rapidly attenuated at turn-on, the turn-off seems much more disturbed and is therefore of particular interest because of possible difficulties in stopping the conduction of the component. The conclusions are similar to those reached for components from batch A, with undamped oscillations at V_{DS} = 150 V and reduced disturbances beyond that, particularly for component 3B in Figure 211.

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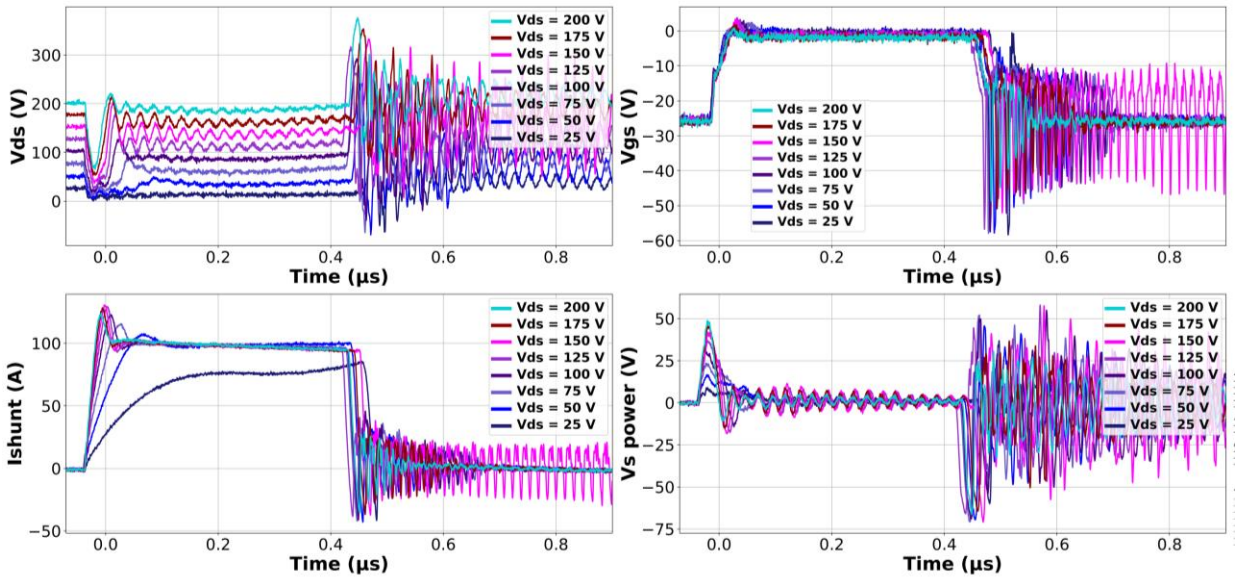

Figure 211: Experimental rise in voltage for a normally-on component, from V_{DS} = 25 V to V_{DS} = 200 V on 2023 Test-Board with 2023 driver

The previous observation becomes even clearer if the voltages V_{DS} = 100 V, V_{DS} = 150 V and V_{DS} = 200 V are isolated on the same graph, as shown in Figure 212. While oscillations are visible at turn-off for V_{DS} = 100 V, they become undamped for V_{DS} = 150 V. On the other hand, these oscillations are strongly attenuated from V_{DS} = 200 V. As seen previously, components do not behave identically according to the V_{DS} voltage level applied.

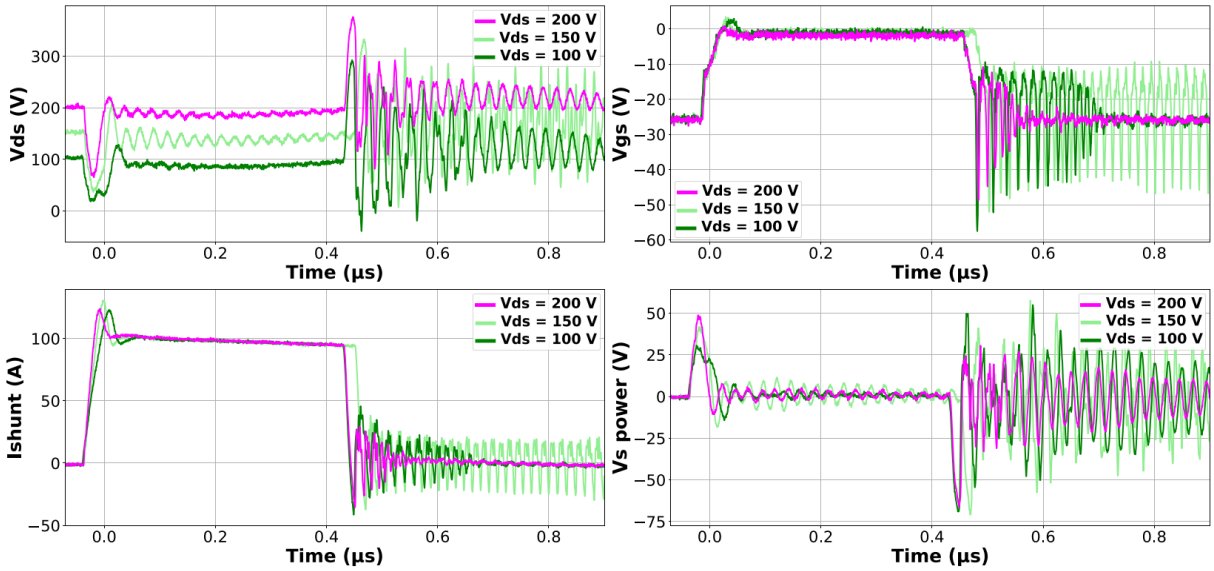

Figure 212: Experimental waveforms for V_{DS} = 100 V and V_{DS} = 150 V, compared to V_{DS} = 200 V on 2023 Test-Board with 2023 driver

With respect to Batch A, it could be noticed a small decay of the short-circuit current for devices of Batch B. This could be explained by an electrothermal coupling.
Tests were carried out on other components from the same batch, with the same results. It was then decided to move on to the third batch to study their behaviour and determine whether or not there were any differences between each batch of the same wafer.
Another possible explanation on the reduction of the perturbation for higher V_{DS} could be a reduction of the capacitance values C_{DS} and C_{GD}.

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3.1.1.3 Batch C

The study of Batch C components reveals some unexpected findings. The latest repetitive tests on Batch B components, detailed above in 3.1.1.2, were carried out at a conduction time of 800 ns. In view of the fact that these tests would be repetitive and non-destructive before a certain number of iterations, it was decided to carry out the tests on the components of batch C with the same conduction time, i.e. 800 ns. Figure 213 illustrates just how inappropriate this strategy is for batch C devices. In addition to a steeper V_{DS} voltage drop than the components in Batch B, the components in Batch C are unable to withstand the 800 ns conduction time and break prematurely.

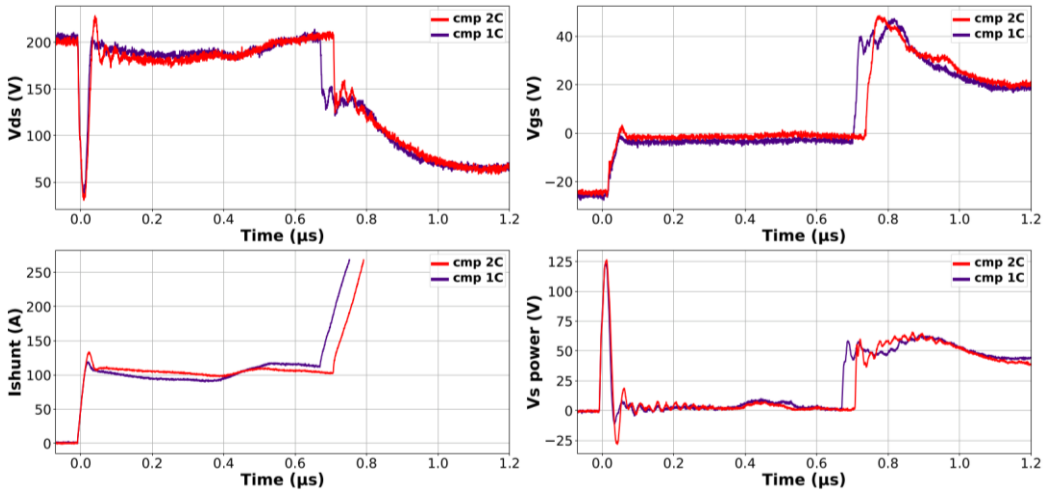

Figure 213: Experimental waveforms for single short-circuit on normally-on component from batch C, with V_{DS} = 200 V and t_{ON} = 800 ns on 2023 Test-Board with 2023 driver

As a result, the short-circuit sequence is modified and the conduction time reduced to 200 ns. Repetitive tests are carried out, as shown in Figure 214.

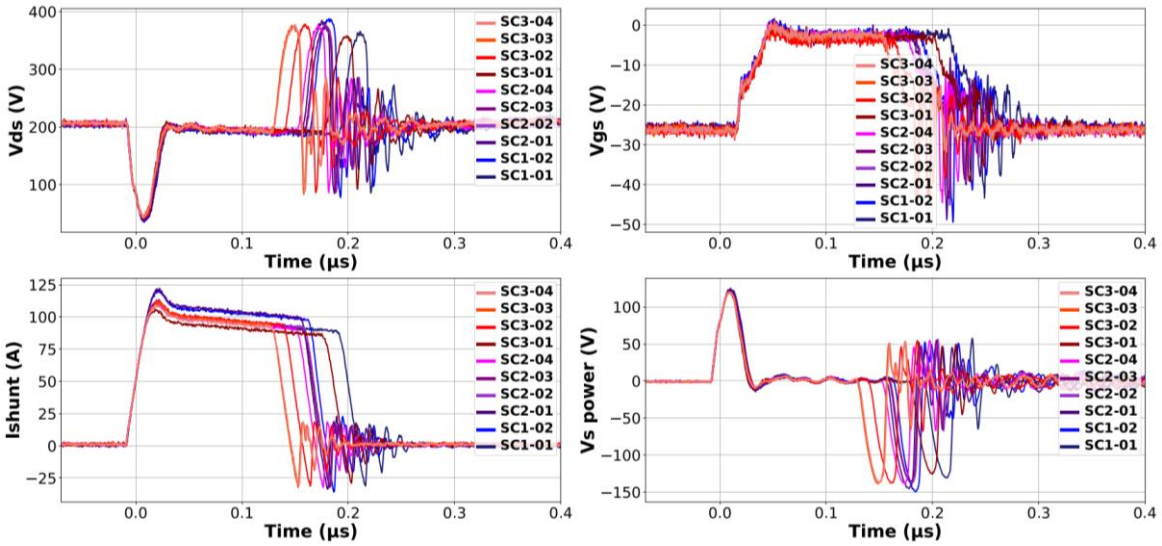

Figure 214: Experimental waveforms for repetitive short-circuit with V_{DS} = 200 V for component 3C on 2023 Test-Board with 2023 driver

Given the lesser robustness of these components, compared with batch B, the study of parametric variations will not be particularly developed. In addition to the normally-on components in batches A and B, the rest of the study will continue with p-GaN normally-off components.

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3.1.2 Dynamic Observations during Repetitive Short-Circuit

Repetitive, non-destructive testing is mainly carried out on components from Batch B, since components from Batch A were used for testbench optimization, and components from Batch C showed little robustness.

After the gradual voltage ramp-up performed in Figure 211, repetitive tests at V_{DS} = 200 V are performed on components from Batch B. Figure 215 shows a series of successive short-circuits on component reference 3B. the reference 3B means it is the third component from the batch B. While the signals in Figure 215 appear stable, a slight increase in the saturation level of the short-circuit current can be noted. Zooming in on the short-circuit current measured by the shunt in Figure 216 demonstrates this increase of several amperes with each successive short-circuit. The other signals V_{DS}, V_{GS} and $V_{S,POWER}$ remain stable. The variation of short-circuit duration between several test has the same origin as explained in 2.2.1

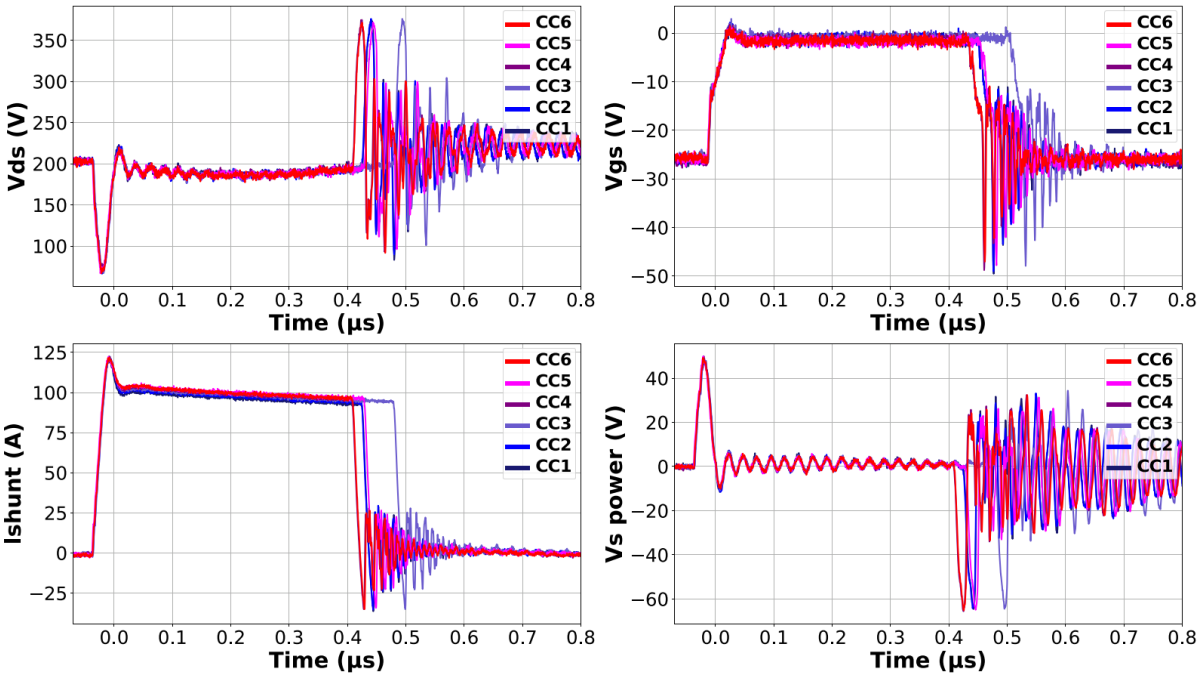

Figure 215: Experimental waveforms for repetitive short-circuit with V_{DS} = 200 V

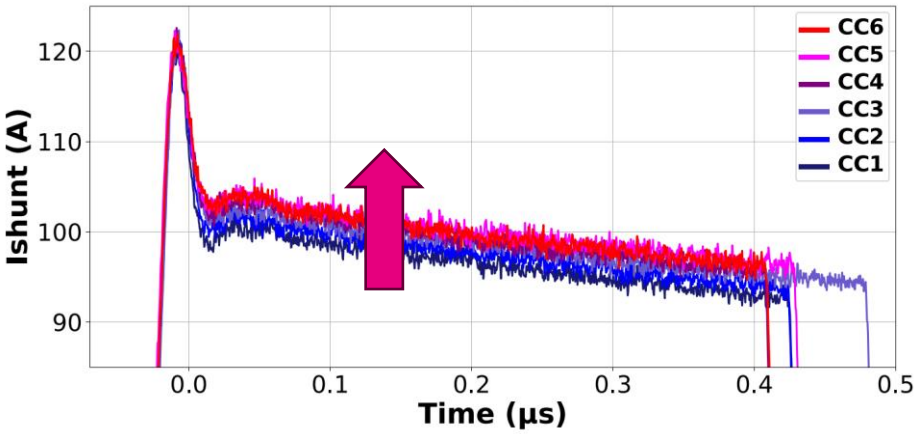

Figure 216: Zoom on I_{SHUNT} and its variation as repetitive short-circuits are conducted

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Interspersed with electrical characterizations at the B1505, further short-circuit series were carried out on component 3B, revealing the same trend in short-circuit current saturation level as successive short-circuits.

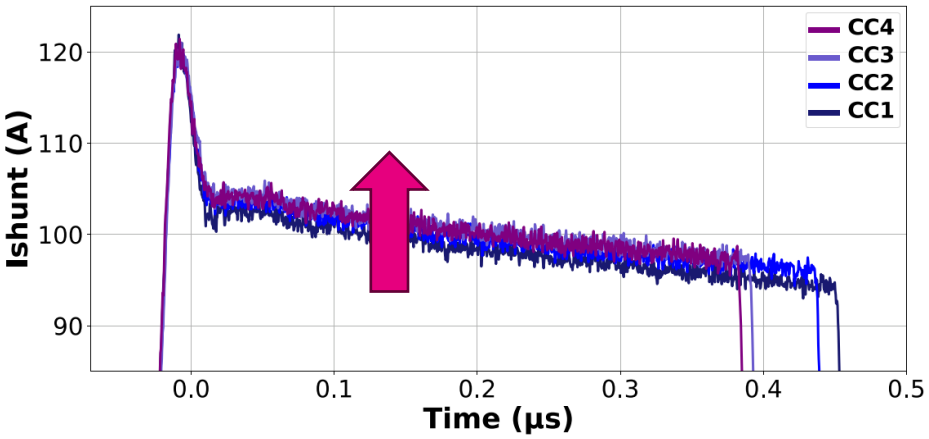

Figure 217: Little increase in the saturation level of the short-circuit current for component 3B

To consolidate these results, tests were carried out again under the same conditions, on the same component, four days later.
On the same day, three successive short-circuit sequences were carried out. Each series was separated by two hours, and each short-circuit was spaced five minutes apart to prevent the DUT from overheating.
As seen previously in Figure 216 and Figure 217, the saturation level of the short-circuit current increases as the tests progress on the three graphs in Figure 218. It can also be seen an increase of the short-circuit duration. It does not come from the device itself but it is rather due to the driver which is sufficiently inaccurate or the duration of short-circuit. This will be rectified with the 2024 version of the driver.

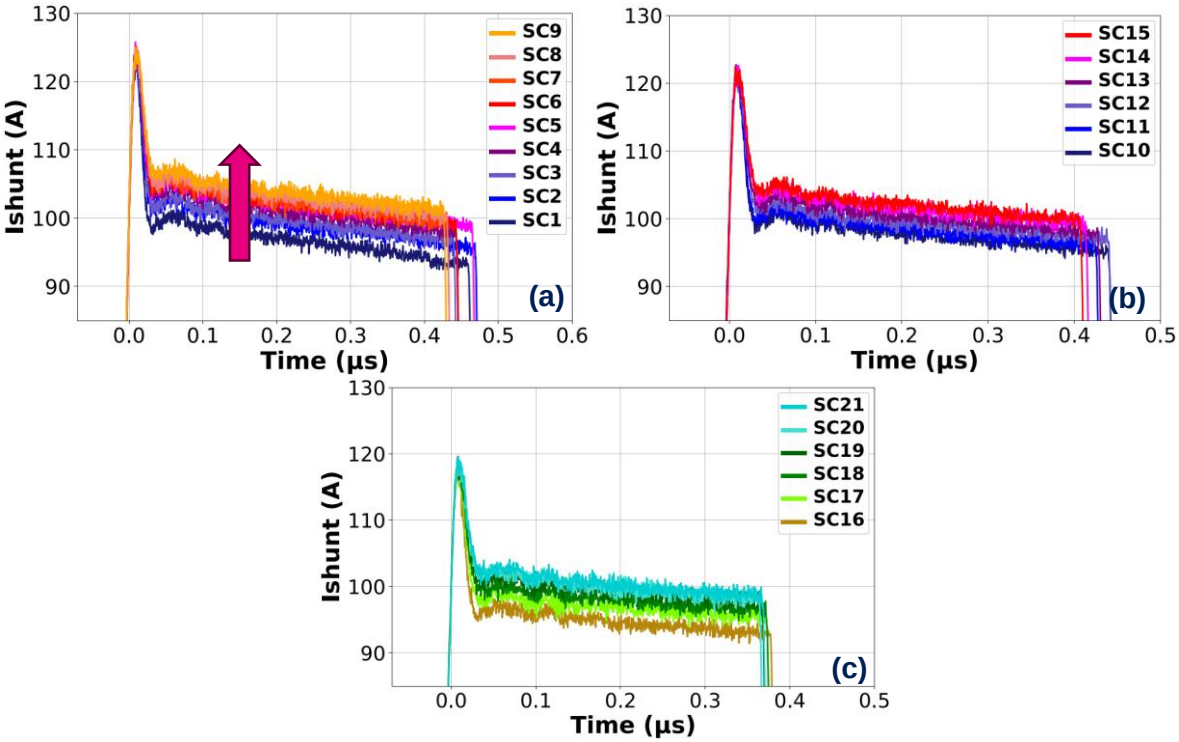

Figure 218: Increase in the saturation level of the short-circuit current for component 3B, for each series of short-circuit (a,b,c), interspersed with characterizations

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The second observation is that this variation is not immutable over time. *Figure 219* shows the first and last short-circuits in each series (a), (b), (c) from *Figure 218*. Series (a) includes short circuits 1 to 9. The second series includes short circuits 10 to 15, and the last series includes short circuits 16 to 21. While the variation observed is always in the direction of an increase in the saturation level of the short-circuit current, the first tests in each series do not start with the same short-circuit current value. What is more, the saturation level of the next series is not necessarily the same as that of the previous short-circuit series. This variation in the saturation level of the short-circuit current is therefore not permanent since, for example, the saturation level of the current of short-circuit 16, the start of the third series, is lower than that of short-circuit 1 or 10.

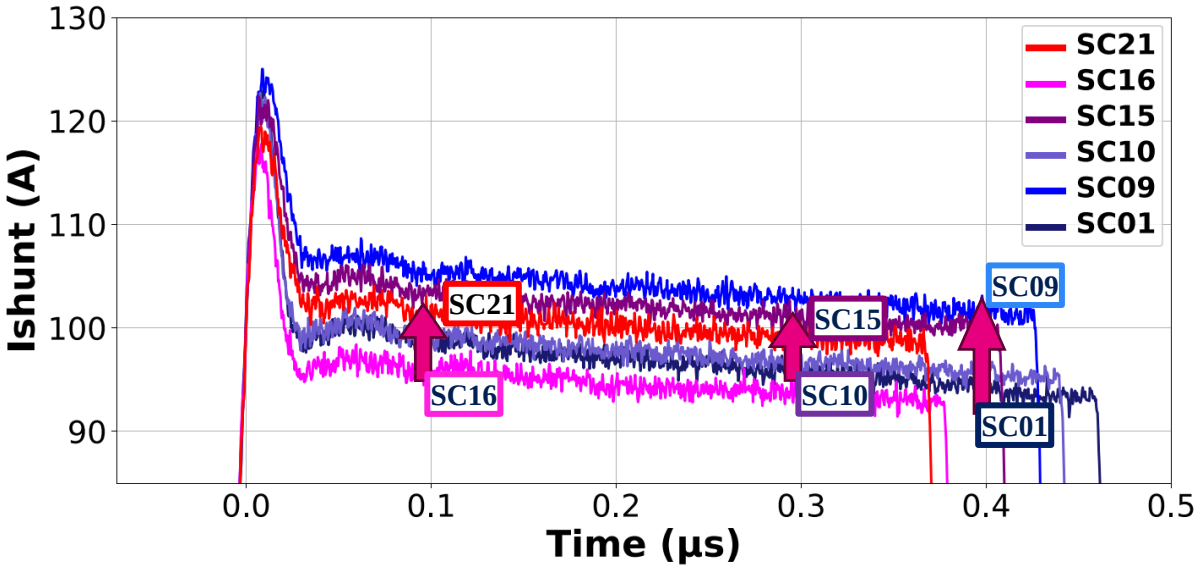

Figure 219: zoom on I_{SHUNT} during first and last short-circuit for each of three sequences

The following day, tests under identical conditions were carried out, giving the same conclusions as shown in Figure 220 where an increase in the saturation level of the short-circuit current is noted as the short-circuits increase from SC01 (first short-circuit of the series) to SC12 (12th and last short-circuit of the series).

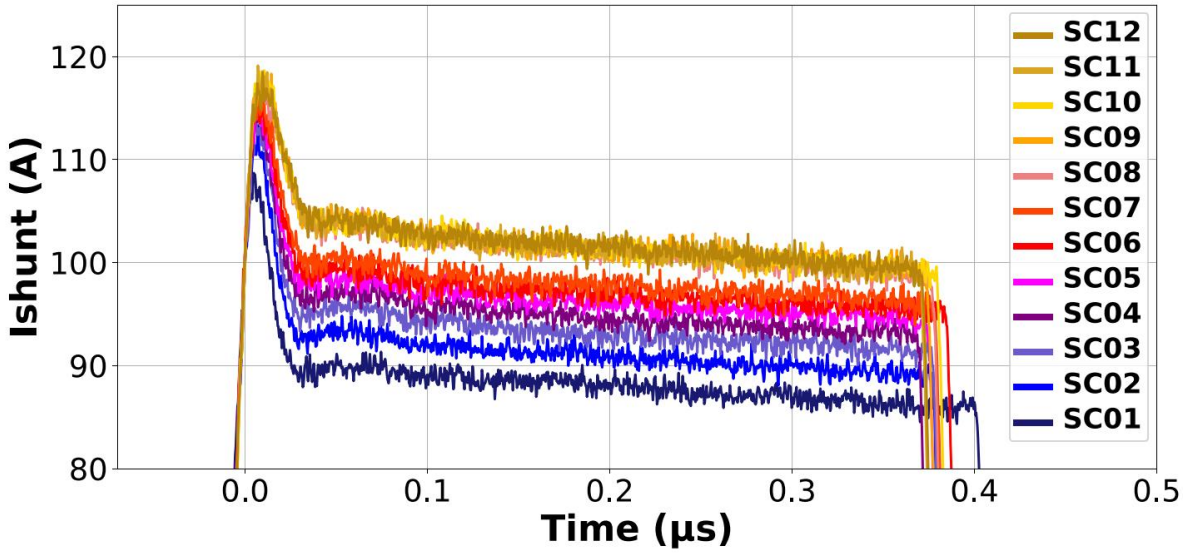

Figure 220: Increase in the saturation level of the short-circuit current for component 3B

This type of behaviour is also observed on other components with for example the component 5B. The first short-circuits carried out do not show a variation similar to that observed previously.

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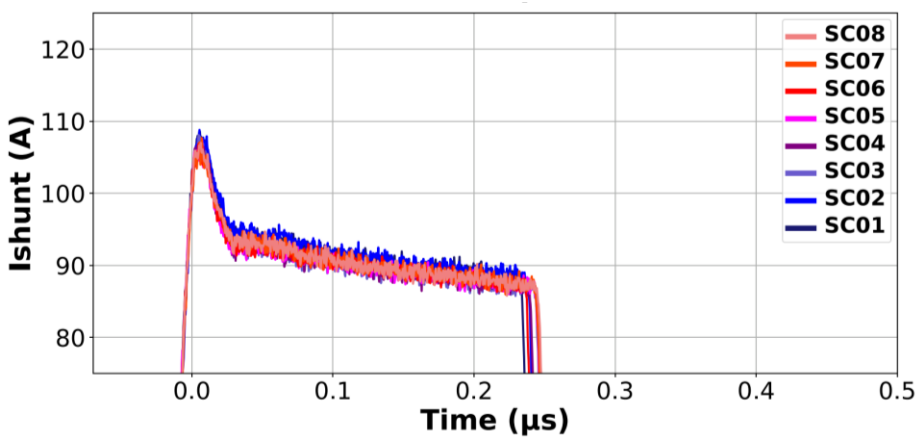

Figure 221: No variation in the saturation level of the short-circuit current (first series)

On the other hand, in *Figure 222*, the next two series, again on component 5B, referenced SC0X-2 and SC0X-3, with X the number of each short-circuit, 2 and 3 meaning series 2 or series 3, show a saturation short-circuit current trend similar to that seen previously with component 3B.

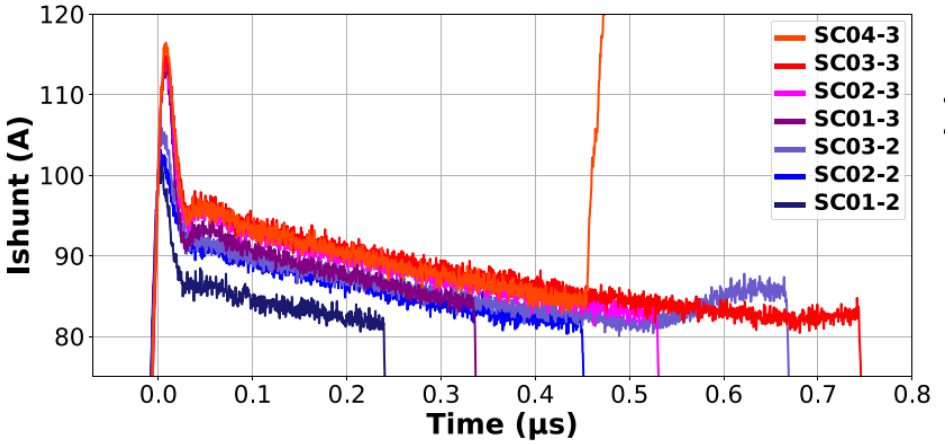

Figure 222: Increase in the saturation level of the short-circuit current and suspicious rise of I_{SHUNT} few short-circuits before breakage for component 5B

The duration of short-circuit was experimentally increased between each test, from 200 ns to 800 ns of conduction. Given the shape of the SC03-2 short-circuit current, with an increase in current shortly before the end of conduction (after 550 ns in the Figure 222), a characterization was carried out to see if the component was close to failure, but no particularly alarming signs were detected. The parametric variations observed, in particular that of the threshold voltage V_{th}, are detailed below.
On the other hand, the short-circuit current increases at 0.7 µs conduction for SC03-3, the last short-circuit before SC04-3, which will be fatal for component 5B.
This type of precursor break behaviour can be found in other components, such as component 12B in Figure 223 or component 13B in Figure 224. In the *Figure 223* the duration of short-circuit has also been experimentally increased to see potential effects and to consider the robustness of the device in terms of short-circuit duration.

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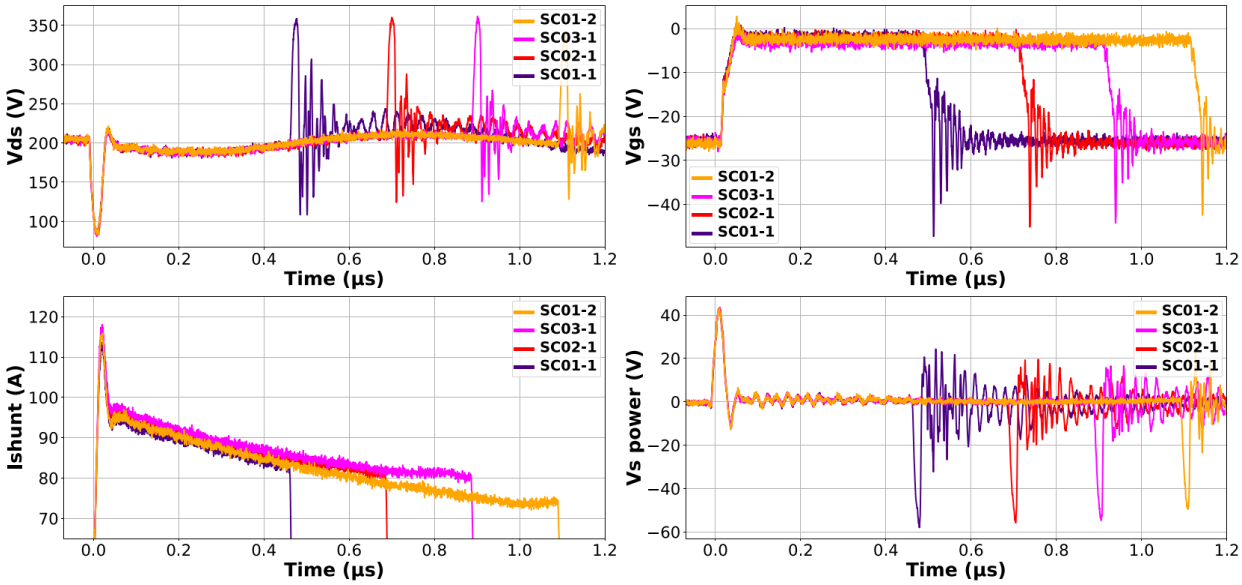

Figure 223: Increase in the saturation level of the short-circuit current and suspicious rise of I_{SHUNT}, one short-circuit before breakage of component 12B

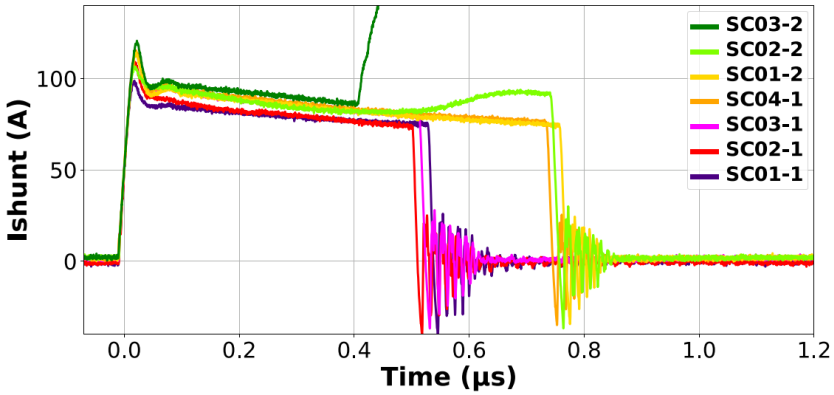

Figure 224: Increase in the saturation level of the short-circuit current and suspicious rise of I_{SHUNT} few short-circuits before breakage for component 13B

However, not all components seem to be affected by this sudden increase in current conduction, a precursor to breakage, as in the case of component 14B, which probably breaks due to the accumulation of short-circuits, but without any warning signs. On the other hand, the progressive increase in the saturation level of the short-circuit current remains verified, as shown in Figure 225. Within the same series of short-circuits, an increase in the saturation level of the I_{shunt} current can be observed with each successive short-circuit.

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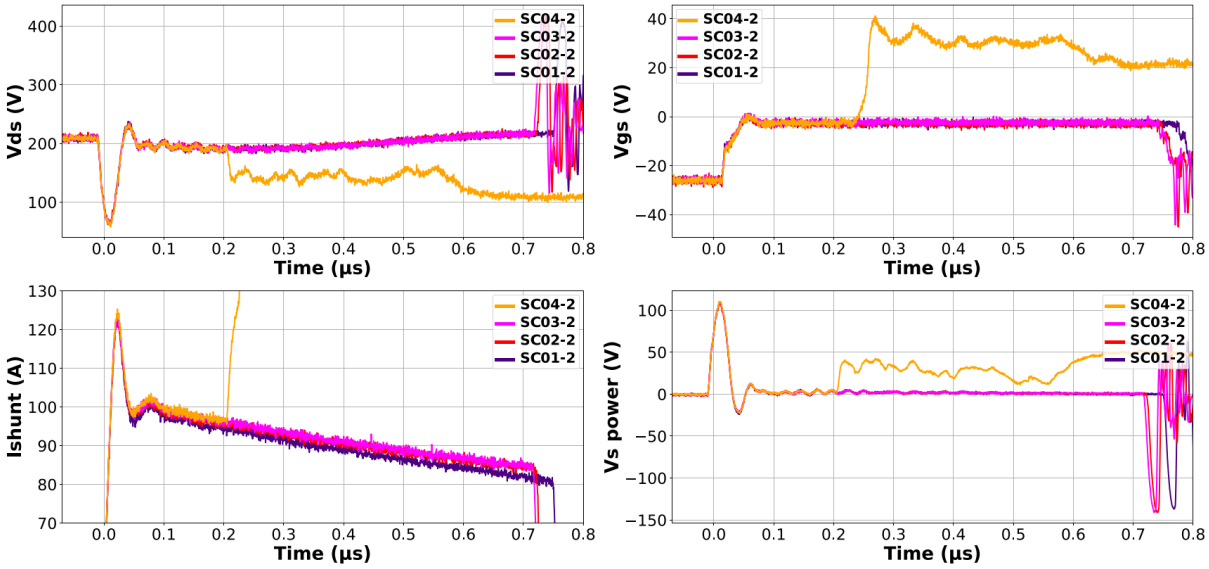

Figure 225: Experimental waveforms for repetitive short-circuit with V_{DS} = 200 V without any warning sign before breakage of the component 14B

The study of three distinct batches of normally-on components from the same wafer has yielded a number of conclusions. Firstly, the location of the chips on the wafer could have a critical impact on short-circuit robustness, as demonstrated by the premature failure of components in batch C, compared with batches A and B, each capable of withstanding several short-circuits of 800 ns conduction. In parallel with this initial conclusion, dynamic variations were observed, with the saturation level of the short-circuit current rising with each successive test. A suspicious increase in short-circuit current, potentially heralding imminent failure, was also observed on several components, although not systematically. These drift in the saturation level could be explained by some trapping that act on the internal polarisation of the device.

In addition to these dynamic observations, parametric variations are studied in greater detail below.

3.1.3 Aging Degradation After Repetitive Short-Circuits

The study of parametric variations, initiated on Batch A components, yielded interesting results, in particular the variation in threshold voltage V_{th} shown in Figure 226. This figure shows the variation in threshold voltage V_{th} before and after the application of short-circuits. The variation is represented in values (a) or in percentage deviation from the initial value of V_{th} (b) measured before the application of any short-circuit. This initial measure of V_{th} is carried out with the reinitialization protocol Triple-Sense [142]. This provides a reliable initial measure which can be compared to other measurements conducted after the application of short-circuits. Both graphs are plotted as a function of accumulated energy over successive short-circuits.

Nevertheless, the necessary optimizations carried out during the course of the A-component study deliver tests under conditions that are not very similar. For this reason, and considering the need of reproducibility between tests, the analysis of any parametric variations is mainly carried out on batch B components. Due to their low robustness, batch C components are not studied in this section.

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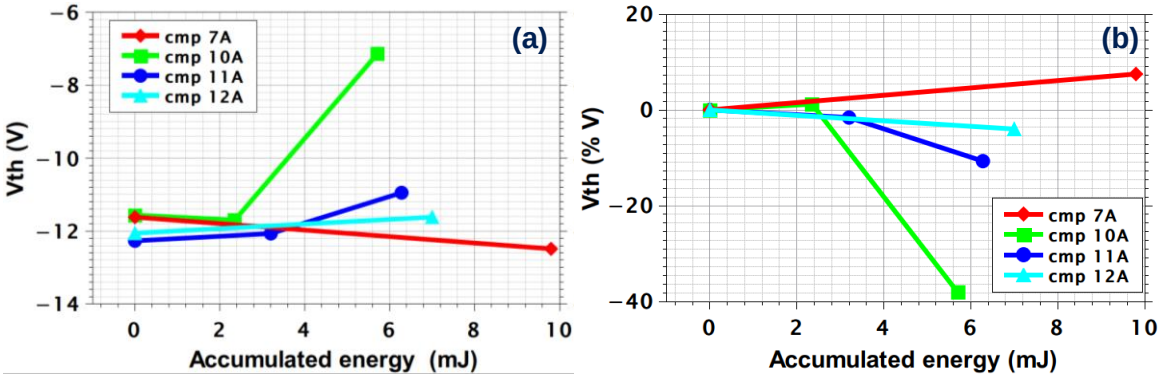

Figure 226: V_{th} variation in value (a) and in percentage (b) after repetitive short-circuits for DUT from Batch A (cf Table 1)

The bench optimization described in Chapter 2 enables to carry out repetitive, non-destructive short-circuits. B1505 characterizations are performed before and after each series of short-circuits.

The test sequence is based on the following criteria, explained in Table 27 below.
For some components, such as 17B and 18B, the conduction time is extended to 800 ns. On the other hand, the number of short-circuits in the series will be reduced, to guard against the possibility of component breakage before characterization with B1505.

V_{GS}	V_{DS}	Conduction Time
-24 V / 0 V	200 V	300 – 400 ns

Table 27: Repetitive Short-Circuit characteristics applied on DUT from batch B

Figure 227 and Figure 228 show the results in terms of threshold voltage variation, respectively as a value or percentage compared to the initial value. A general trend can be observed with the reduction in threshold voltage, with the latter dropping further into the negative range. For some components, this variation exceeds 10%, notably component 13.

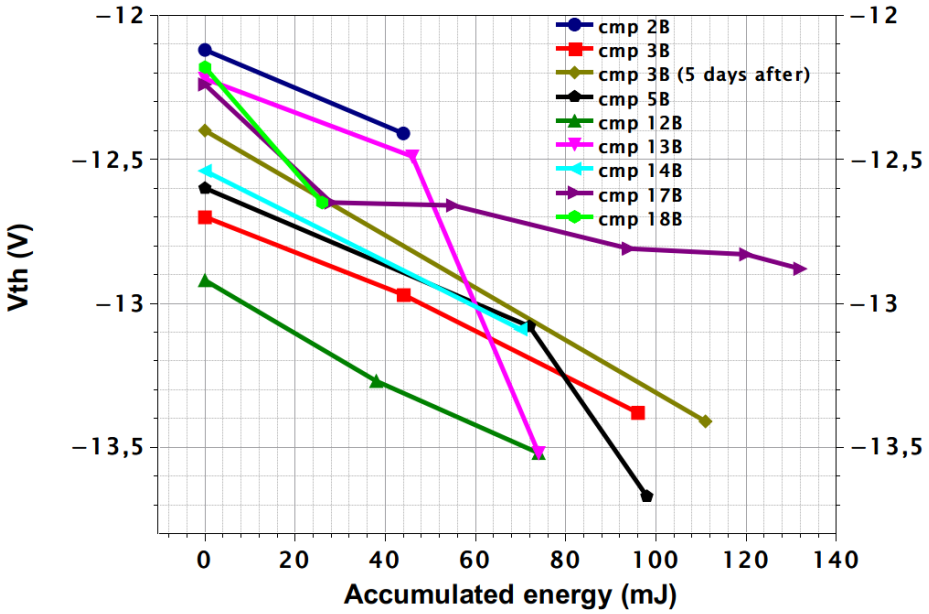

Figure 227: V_{th} variation in value after repetitive short-circuits for DUT from Batch B

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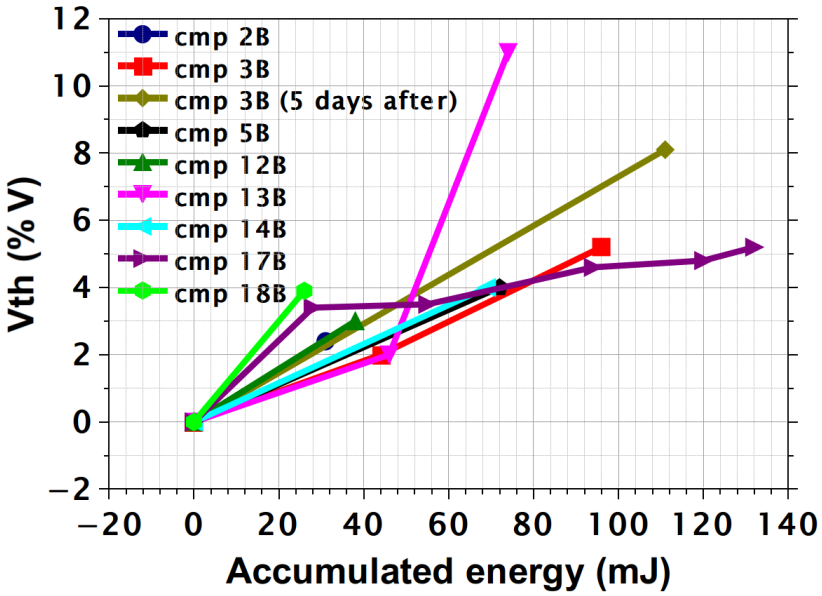

Figure 228: V_{th} variation in percentage after repetitive short-circuits for DUT from Batch B

This reduction in voltage V_{th} can therefore be interpreted as the component ability to conduct "sooner" than initially expected. This is in line with the increase in the saturation level of the short-circuit current seen previously.

This could confirm a trapping phenomenon.

This variation in threshold voltage V_{th} can also be linked to hot electrons. Indeed, the application of a drain-source bias during the presence of current flow constitutes a prime situation for the presence of this very particular type of electron, as explained in Chapter 1, figure 46, with, in particular, a tunnelling effect, enhanced by temperature, as explained in [75].

Another possible explanation is that hot electrons create trap states in or near the gate region. Trap states are energy levels in the material band gap energy where charges can be captured and immobilized. These trap states capture the surrounding positive charges. Indeed, hot electrons, having a higher kinetic energy than usual, can interact with the crystal lattice of the semiconductor material, GaN in this case, or with the dielectric, creating structural defects. These positive charges, which previously contributed to the channel cut-off and blocked appearance, are now reduced in number. The positive charges trapped in the trap states then create a local electric field that opposes the electric field of the gate. This in turn reduces the threshold voltage [164–167]

In view of these parametric variations, a link can be made between the impact of repetitive short-circuits and the variation in threshold voltage V_{th}. This suggests that physical aging mechanisms are occurring within the gate. Similar analyses will be carried out on normally-off components in the second part. In the final part of Chapter 3, different types of breakage will be explained as devices do not always break in the same way. The hypothesis of the superior robustness of the normally-off components of supplier 1 will also be discussed.

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3.2 Normally-OFF Components

Once the necessary optimization of the test bench for normally-off components has been completed, repetitive tests can begin. In the same way as for normally-on components, uncertainty about conduction time limits and drain-source polarization means that the first step is to carry out preliminary tests in order to better define the limits of the components.

In addition to the obvious differences in stability between components from supplier 1 and those from supplier 2, the latter will demonstrate less robustness and more marked limits, particularly in terms of maximum drain-source polarization. Finally, parametric variations will be studied, following the same logic as for normally-on components. The first step is to study the behaviour of p-GaN components at longer conduction times.

3.2.1 Test and Behaviour of Normally-Off Components for Increased Conduction Time

At this stage, the maximum conduction time of the p-GaN components is unknown. A gradual increase in conduction time is therefore performed. The results are shown in Figure 229. As seen in the bibliography in Chapter 1, this figure shows a significant self-reduction in short-circuit current. With a maximum value of 80 A at the turn-on peak, the short-circuit current decreases inexorably to a reduced value of 18 amperes after 6 µs of conduction.
This increase in conduction time causes no disturbance, and signals remain stable over time. Tests have even been carried out for conduction times of up to 10 µs, as shown in Figure 230.

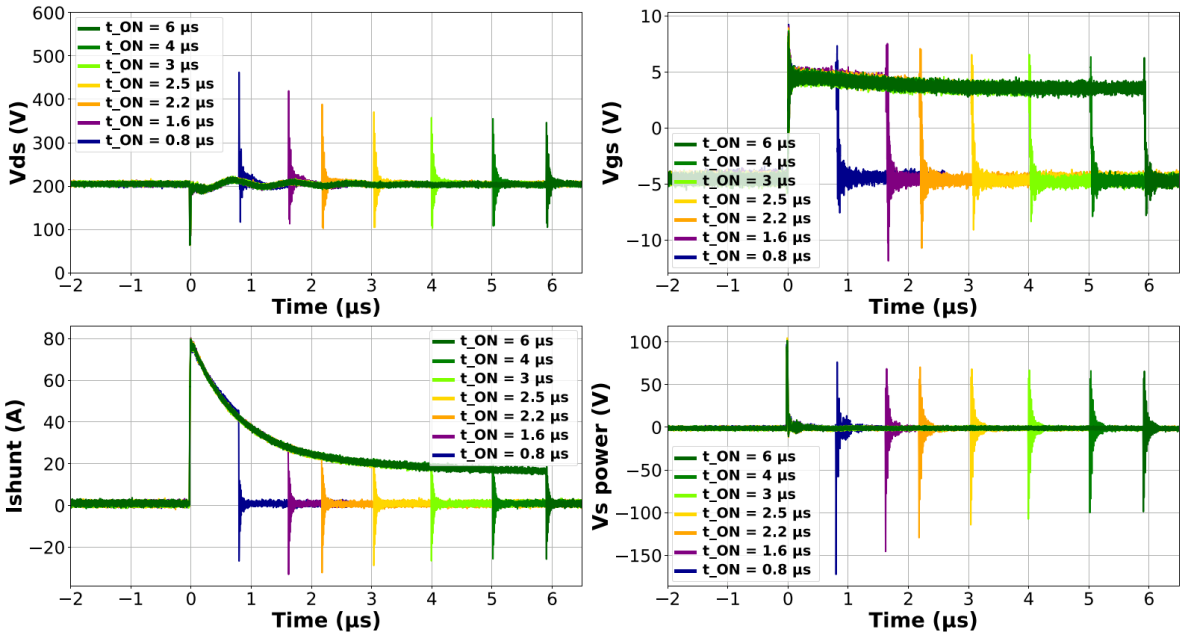

Figure 229: Experimental waveforms for an increased conduction time and repetitive short-circuit with V_{DS} = 200 V applied to p-GaN component from supplier 1 (cf Table 1)

The first comment is that for longer short-circuit times, a clear decay of the saturation current is observed and could be explained by overheating.
Two short-circuit current reduction dynamics can be observed. Up to 2 µs, reduction is very rapid, with a reduction of 60 A during this duration. Beyond 2 µs, on the other hand, the reduction is much slower, with only 2 A less short-circuit current despite 8 µs of conduction.

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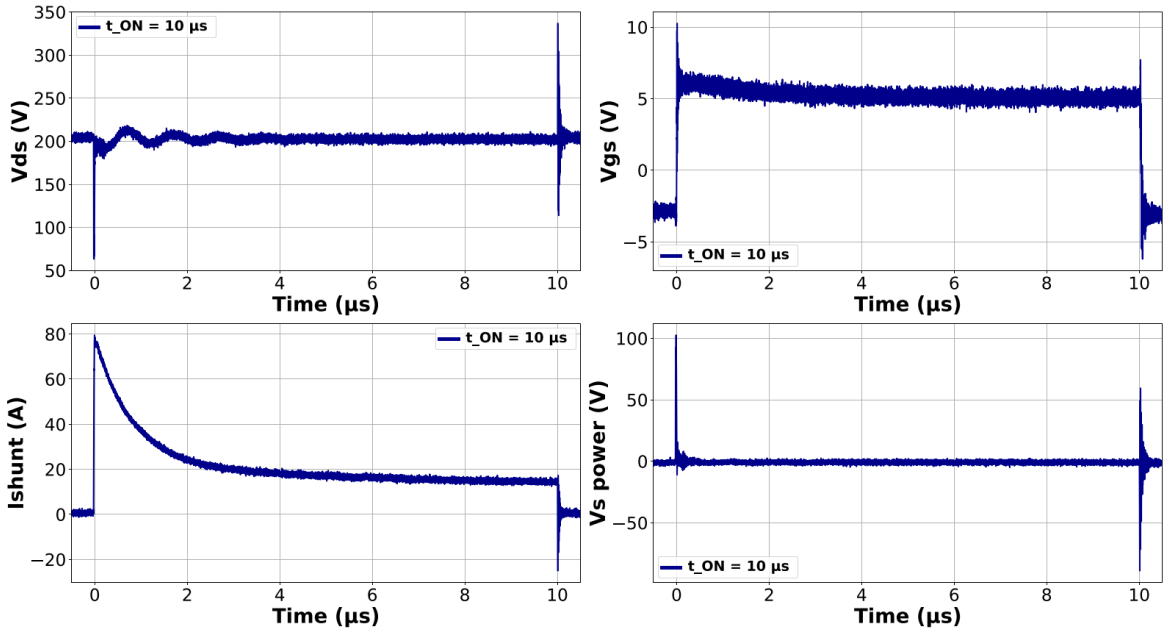

Figure 230: Experimental auto-reduction of the short-circuit current with V_{DS} = 200 V and t_{ON} = 10 µs for p-GaN component from supplier 1

Similar tests were carried out on the p-GaN components of supplier 2, yielding the same conclusions, the only difference being a lower saturation level for supplier 2 components, due to a lower nominal current rating. The tests carried out on component 11 (supplier 2) were performed on test-board 2023 with driver 2023 (see table of test-boards). The waveforms of this device are in gold in Figure 231 The new 2024 driver, still associated with this 2023 test-board, will nevertheless significantly reduce disturbances, for example when studying component 18 (supplier 2), shown in purple in Figure 231. In fact, in Figure 231 a sharp reduction of the disturbance can be seen in the purple waveforms depicting the behaviour with the 2024 driver version, in comparison to the gold waveforms which depict the 2023 driver version.

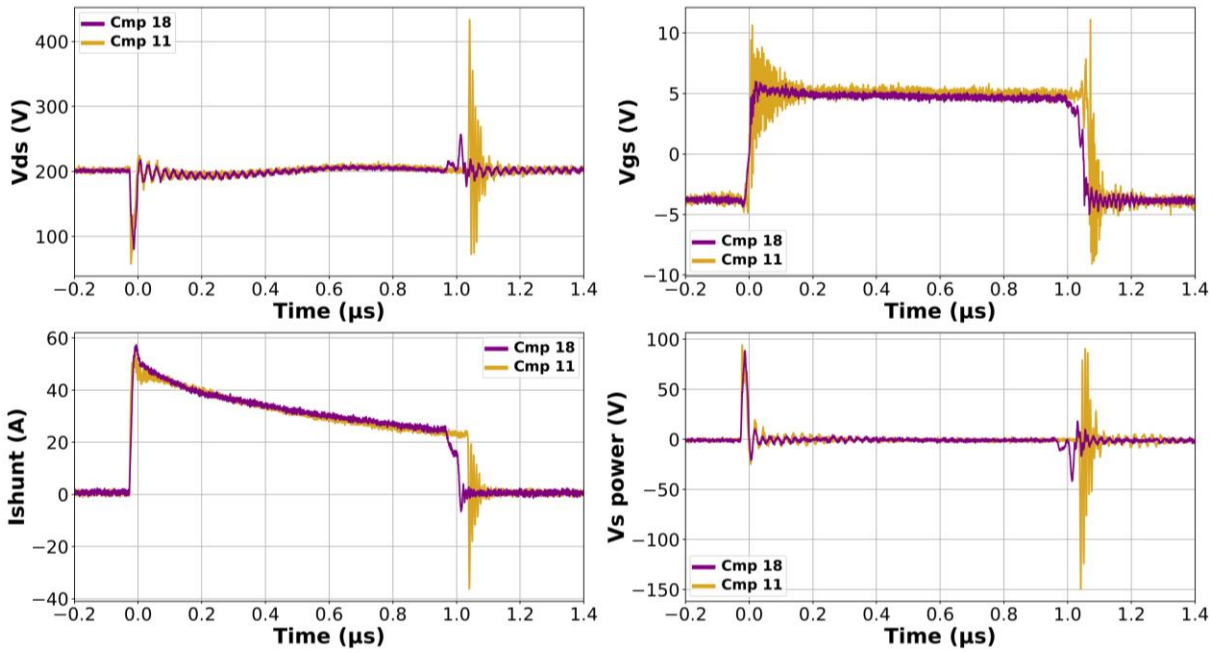

Figure 231: Experimental waveforms for short-circuit with V_{DS} = 200 V and t_{ON} = 1 µs for p-GaN component from supplier 2 on test-board 2023 with two versions of driver (gold: 2023 version and purple: 2024 version)

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Tests were also carried out on Supplier 1 prototypes, giving similar results to those of the qualified components from the same supplier previously used for testing. The results for these three components are compared in *Figure 232*. It shows a very similar short-circuit current pattern for the components from supplier 1, whether prototype or qualified product. Supplier 2 components show a noisier V_{GS} signal at turn-off, and a lower short-circuit current saturation level, the latter due to the lower current rating.

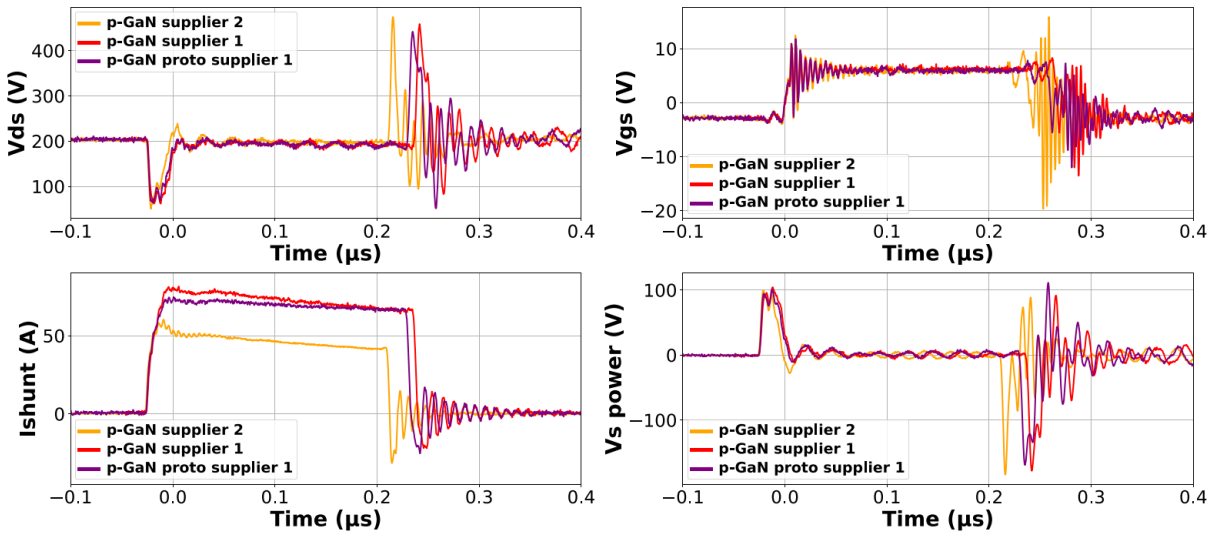

Figure 232: Experimental waveforms for p-GaN component from supplier 1 (qualified and prototype) and from supplier 2 on test-board 2023 with 2023 driver

P-GaN components thus appear to be able to withstand much longer conduction times than normally-on components. As explained in Chapter 1, this increased robustness can be explained by the significant self-reduction of the short-circuit current, as illustrated in Figure 229, Figure 230, Figure 231 and Figure 232. The self-reduction could be explained by an overheating phenomenon. Once the temporal aspect had been studied, it was decided to turn attention to the voltage limits of p-GaN components.

3.2.2 Limits in Voltage

3.2.2.1 Supplier 1

In line with the experimental testbench optimization carried out, the p-GaN components of both suppliers are stable at V_{DS} = 200 V for conduction times of up to ten microseconds, as seen in Figure 229 and Figure 230.
In view of this, a gradual voltage increase is carried out to test the limits of the components.

The V_{DS} voltage is gradually increased until the component breaks down.
Figure 233 illustrates this voltage rise with component failure at a maximum voltage of 400 V. These tests are performed on test board 2023.
In *Figure 233* the component breaks after only 400 ns of conduction, whereas it had managed to hold out for 2 µs of conduction at V_{DS} = 350 V. It can therefore be stated that this failure cannot be directly linked to energy aspects, since for a higher energy (26 mJ), with 2 µs conduction and a drain-source bias V_{DS} = 350 V, the component holds the short-circuit. On the contrary, for a drain-source polarization V_{DS} = 400 V, the device broke for a reduced energy (10 mJ)

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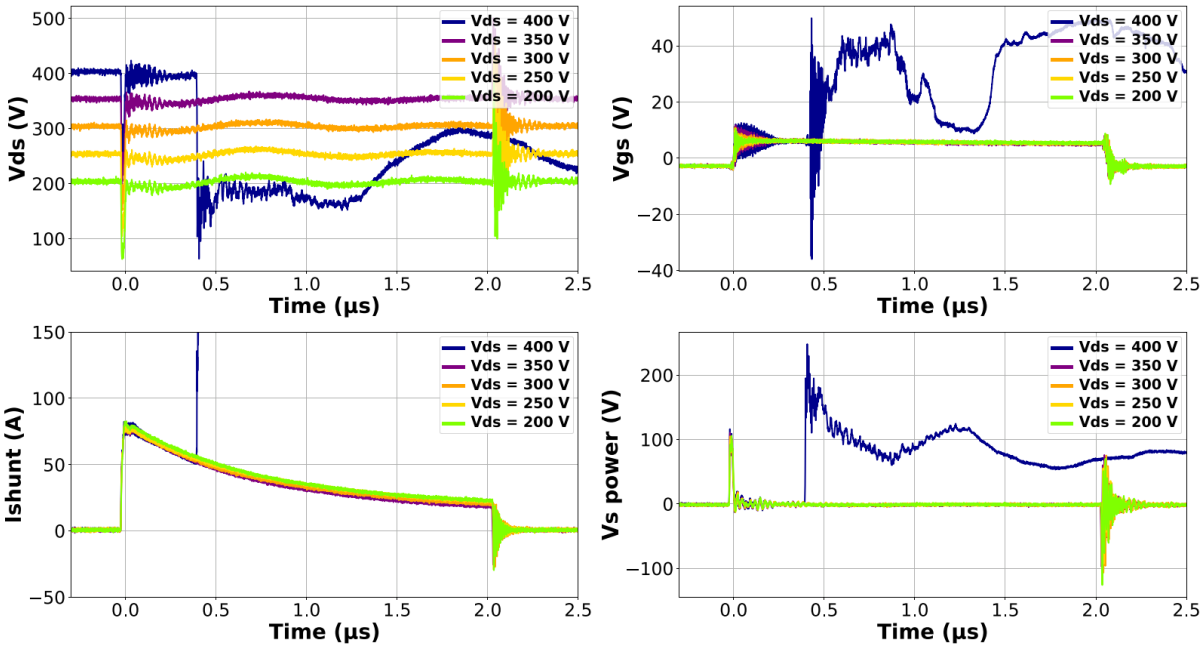

Figure 233: Experimental waveforms during a progressive rise in voltage for a p-GaN component from supplier 1

An interesting fact to note in *Figure 233* is the progressive degradation of the V_{GS} signal at the turn-on, as the drain-source polarization increases. Analysis of the origin of this phenomenon has not been studied in depth, and the open question is whether there is an effect of the experimental bench or of the DUT itself.

In general, Supplier 1 components are able to withstand several repetitive short circuits at V_{DS} = 300 V. As shown in *Figure 234*, for example, the DUT, after a gradual ramp-up in 50 V steps, undergoes no less than 10 short-circuits at V_{DS} = 300 V and a conduction time of 1 µs, without flinching. These tests were carried out on the 2023 test-board, with the 2024 driver reducing V_{DS} and V_{GS} signal overvoltage to its minimum.

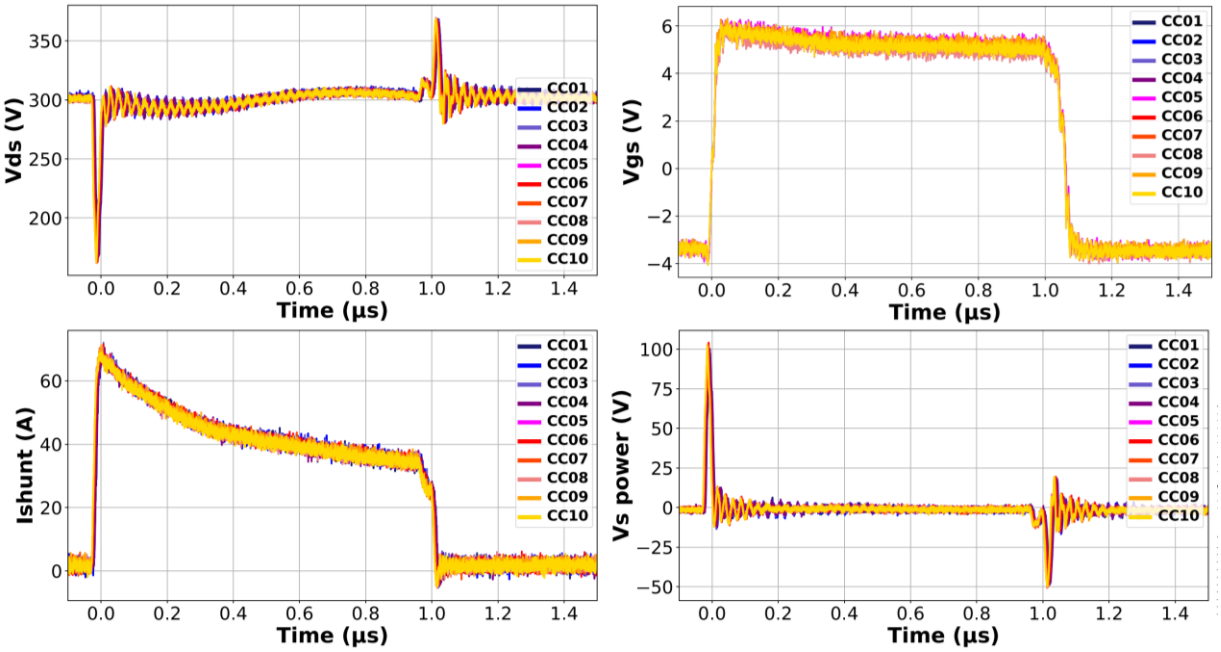

Figure 234: Experimental waveforms during repetitive short-circuits at V_{DS} = 300 V for a p-GaN component from supplier 1

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In conclusion, the p-GaN components of supplier 1 demonstrate good robustness in the face of short-circuits, in comparison with what has been seen previously with normally-on components in particular. These components also stand out from those of supplier 2, whose voltage limits are more restricted.

3.2.2.2 Supplier 2

The first voltage rise tests, still carried out on test-board 2023, are initially performed with driver 2023. As can be seen in Figure 235, although the test for V_{DS} = 200 V passed, in line with the optimization previously carried out, the following short-circuit, carried out for a drain - source polarization V_{DS} = 300 V, causes the component to break. The disturbances at the start of the short circuit demonstrate the impossibility of short-circuiting at this bias level.

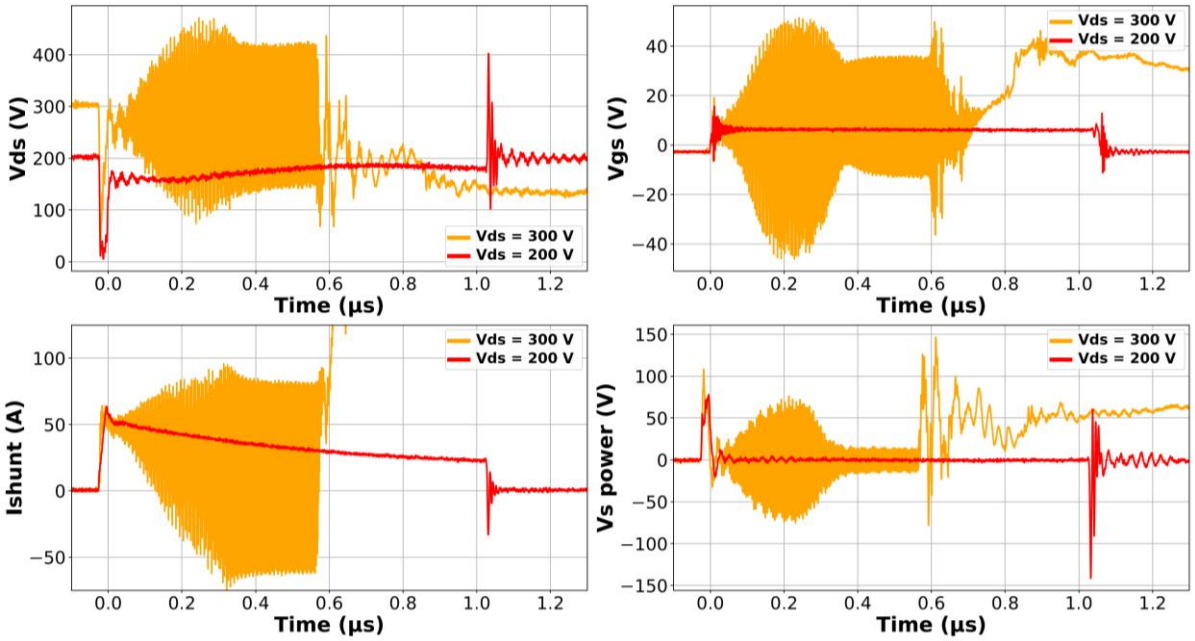

Figure 235: Experimental waveforms during a rise in voltage up to V_{DS} = 300 V for a p-GaN component from supplier 2

Nevertheless, this maximum drain-source polarization level can be increased with the addition of driver version 2024 and the ability to test at V_{DS} = 300 V, as shown in *Figure 236*. Short circuits at V_{DS} = 300 V are operable and repeatable. Nevertheless, non-negligible oscillations in the V_{GS} signal can be observed, which increase with V_{DS} voltage and conduction time. Thus, in *Figure 236*, oscillations are present but remain relatively limited due to the limited conduction time of only 250 ns. However, as soon as this conduction time is increased to 550 ns (violet case in *Figure 236*), the amplitude of oscillations increases significantly, with the risk of making the behaviour of DUT chaotic or even uncontrollable if the conduction time is further increased.

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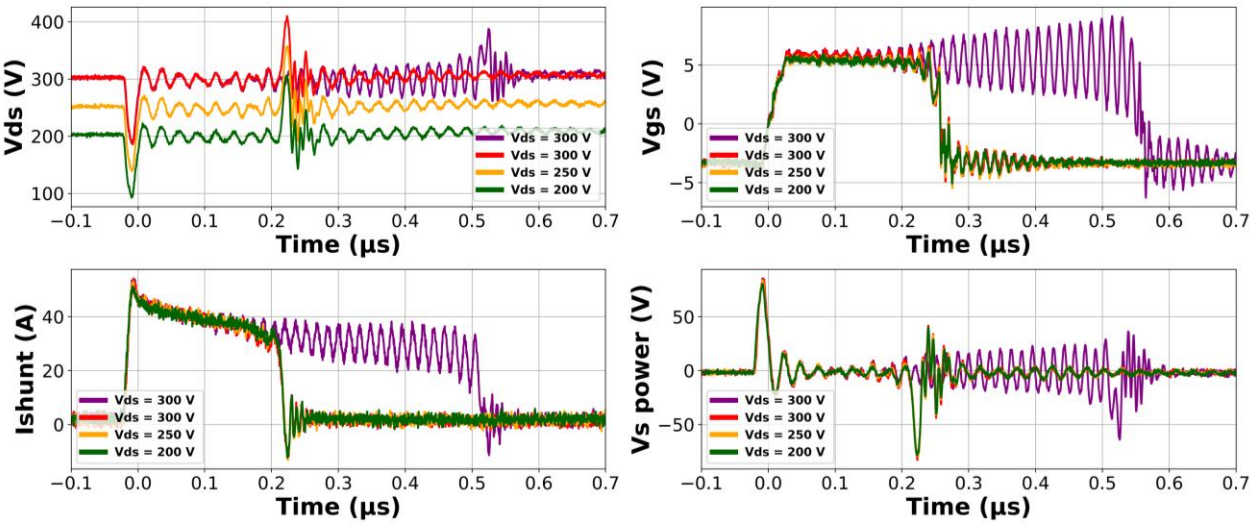

Figure 236: Experimental waveforms during a rise in voltage up to V_{DS} = 300 V for a p-GaN component from supplier 2 on test-board 2023 with 2024 driver

The new 2024 test-board will nevertheless push back these limits, with the absence of marked oscillations at V_{DS} = 300 V. Figure 237 again shows a V_{DS} voltage rise, this time on the 2024 test board, coupled to the 2024 driver. By comparison, the signals are much cleaner and more stable than with test-board 2023. However, there was a slight disturbance at the turn-off of the V_{GS} signal. This disturbance is around 6 V, possibly linked to the amplitude of the disturbance oscillations on the V_S signal when biasing V_{DS} = 300 V.

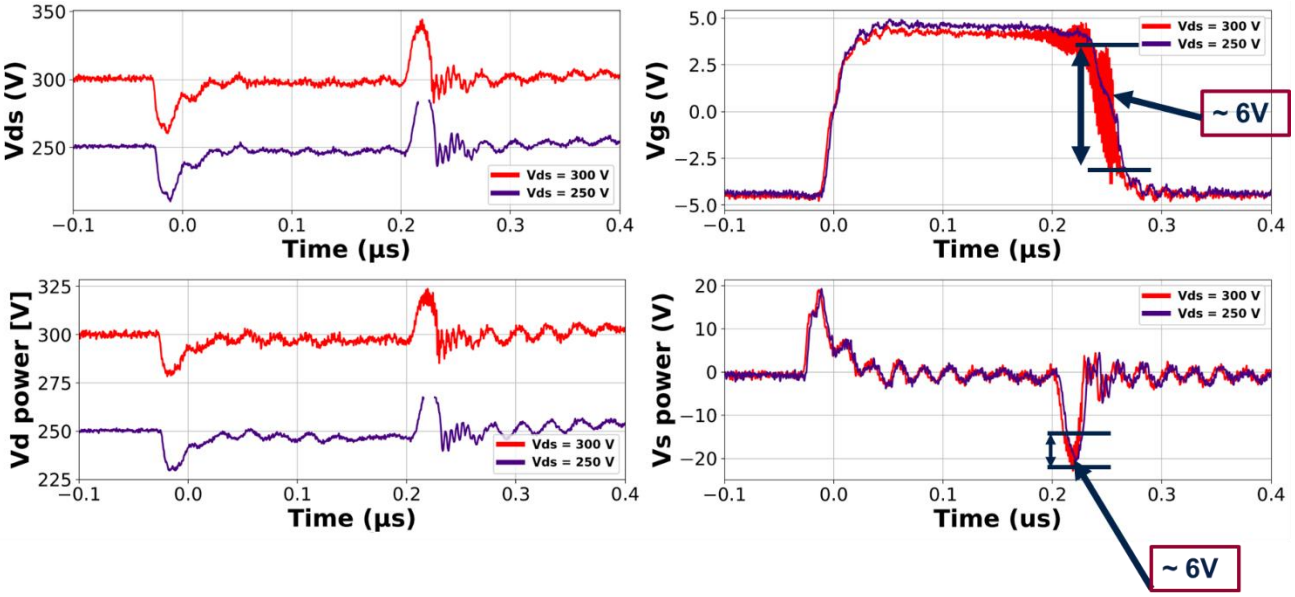

Figure 237: Experimental waveforms during a rise in voltage up to V_{DS} = 300 V for a p-GaN component from supplier 2 on test-board 2024 with 2024 driver

In conclusion, although the components from supplier 2 can be repeatedly short-circuited at V_{DS} voltages of up to 300 V, they are much more limited than the components from supplier 1, both in terms of V_{DS} voltage and conduction time. It will be observed later that the same conclusion can be drawn on the purely energetic aspect. Supplier 2 components are therefore less robust than supplier 1 components when it comes to short-circuits. In the final part of this chapter, it will be discussed the hypothesis put forward as to the greater robustness of components from supplier 1.

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3.2.3 Aging Degradations after Short-Circuit

3.2.3.1 Threshold Voltage Variation

3.2.3.1.1 Supplier 1

As with the study of normally-on components, the series of repetitive short-circuits are interspersed with electrical characterizations on a B1505 characteristic tracer.
Unlike normally-on components, the short-circuit repetition does not generate any observable dynamic variations in the V_{DS}, V_{GS} or I_{SHUNT} signals. As shown in *Figure 238*, the signals are superimposed and no variations are observable, despite the three series of five short-circuits experienced by component 60 from supplier 1.

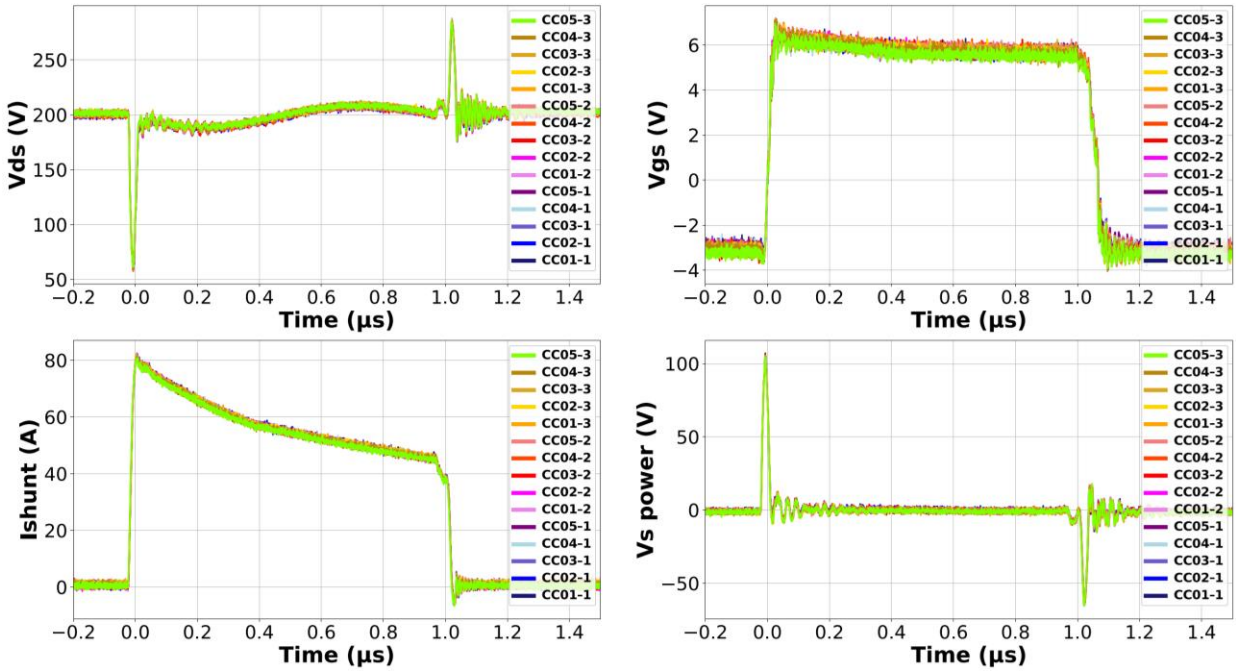

Figure 238: Absence of dynamic variations during repetitive short-circuits with V_{DS} = 200 V for a p-GaN component from supplier 1 on test-board 2023 with 2024 driver

While no dynamic variation was observed, the electrical characterizations did show a significant variation in the threshold voltage of short-circuit-stressed components. Figure 239 shows the evolution of the threshold voltage
for several components that have been repeatedly short-circuited.

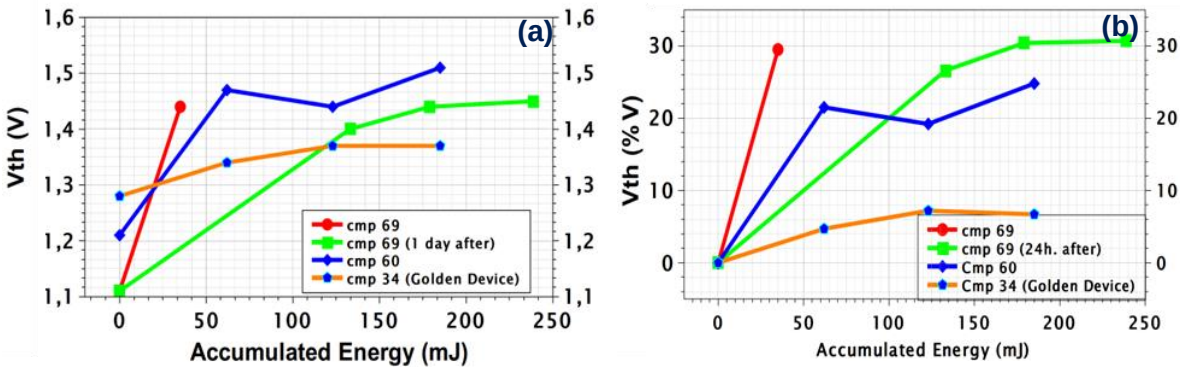

Figure 239: V_{th} variation for p-GaN component from supplier 1 (in value, (a)-left), (in %, (b)-right)

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As the normally-on components, the initial measure of V_{th} has been conducted with the reinitialization protocol Triple-Sense. Several observations can be made. Firstly, the application of these short-circuits causes a significant variation in the threshold voltage V_{th}, sometimes reaching a 30% deviation from the initial value measured before any short-circuit.
The second observation is that this variation is not immutable, as shown by the green and red curves in Figure 239, which illustrate the evolution of component 69 with a one-day interval. After 24 hours, V_{th} had returned to its initial value. Applying short circuits to components therefore causes trapping in the gate region, resulting in a variation of the Threshold voltage V_{th}. It should be noted that this trapping is short-term, as demonstrated by the return of V_{th} to its initial value 24 hours later in the absence of a short-circuit as shown with Figure 239 and the component number 69.

Finally, to ensure that the variations observed are indeed solely due to the application of short-circuits, a control component, known as a “golden device”, is used. This “golden device” undergoes the same electrical characterization steps, but without being short-circuited. This makes it possible to verify the origin of the variations observed in Figure 239. In this case, the electrical characterizations of the “golden device” component 34 are carried out at the same time as those of the “short-circuited” component number 60.
This temporal aspect is important, since the rise in room temperature, although air-conditioned, and its impact on the component electrical parameters must be taken into account during the measurements.

The lower variation of the golden device component, compared to component 60 and other short-circuited components, proves that it is indeed this major short-circuit stress that causes the V_{th} variations, and not the impact of the B1505 measurements.
However, a small variation can be observed for the golden device component. This could be explained by the overheating of the measurement room, whose air-conditioning is not perfect and tolerates a variation of one to two degrees Celsius.

In view of the higher voltage limit of components from supplier 1, tests were carried out not at V_{DS} = 200 V, but now at V_{DS} = 300 V. The conduction time remains unchanged at 1 µs, except for the first short-circuit, where the conduction time is halved to ensure that the DUT can withstand the 300 V drain-source bias. Figure 240 illustrates this series of repetitive short-circuits for V_{DS} = 300 V, interspersed with electrical characterizations at the B1505, before and after.

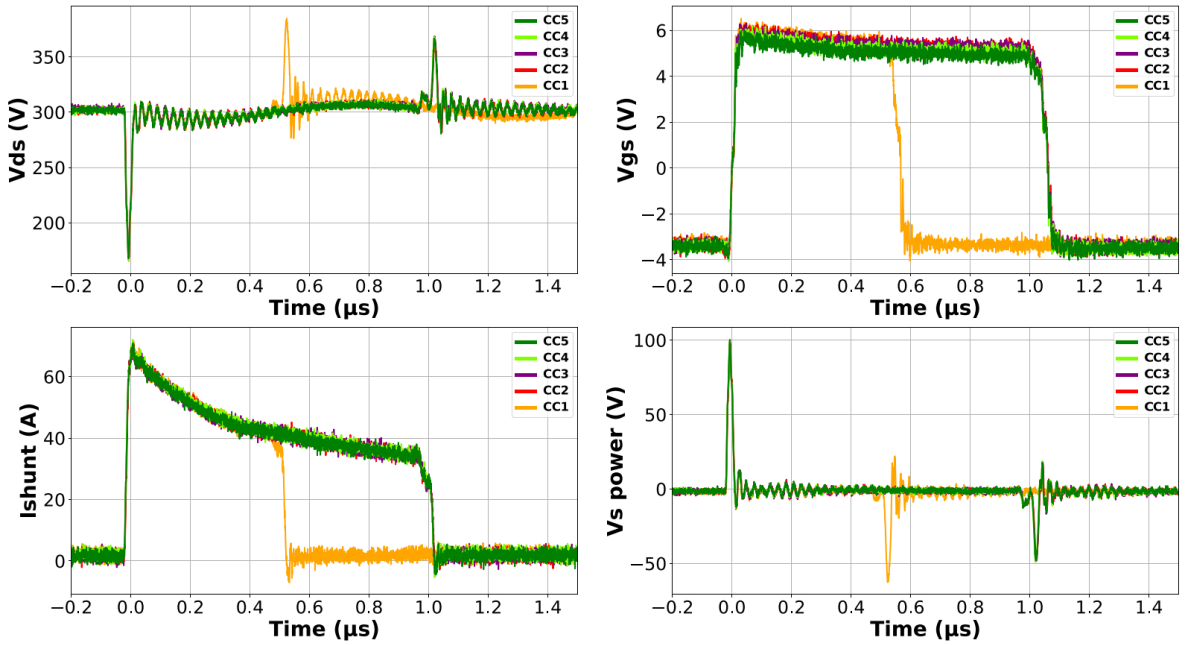

Figure 240: Experimental waveforms during repetitive short-circuits at V_{DS} = 300 V for a p-GaN component from supplier 1

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In view of the V_{th} variations observed at V_{DS} = 200 V, it would seem appropriate to assume that the effects observed would be amplified when V_{DS} voltage is increased up to 300 V. Figure 241 and Figure 242 show the opposite, with no significant variation in V_{th} following the application of repetitive short circuits at V_{DS} = 300 V. Additional series of short-circuits, as shown in Figure 240, are performed, notably with the component (cmp 137), and repeated one day later (cmp 137 1 day after). At the same time, the logic of using a control component, known as the "Golden Device", is repeated with component 48.
As seen previously with temperature changes and the impact of B1505 measurements, the variation in V_{th} for the Golden Device remains below 10%. On the other hand, the results become astonishing when it is observed that V_{th} variations for the stressed component remain at the same level as the control component. These results were confirmed one day later with the same stress sequence.
Given this lack of V_{th} variation despite significant short-circuits, it was decided to carry out a new short-circuit sequence 2 days after the start of the tests, this time for V_{DS} = 200 V, to see if the V_{DS} voltage level had any impact on the V_{th} variations observed. This is the "cmp 137 (2 days after, dark blue curve)" case for the short-circuit sequence shown in Figure 243. Figure 243 also illustrates short-circuit behaviour similar to that seen earlier in the tests at V_{DS} = 200 V.

For the component 137, for which no significant variation has been observed at V_{DS} = 300 V, a significant variation in V_{th} was observed after short-circuits conducted at V_{DS} = 200 V, with an increase in V_{th} of almost 30% compared to its initial value. This is in line with what had previously been observed in tests for V_{DS} = 200 V and Figure 239. This variation is corroborated by the fact that, in parallel with these tests, the variation in V_{th} of the Golden Device always remains strictly below 10%.
Short-circuiting at V_{DS} = 200 V is therefore more deleterious than short-circuiting at V_{DS} = 300 V. However, these tests will not be carried out on components from the second supplier.

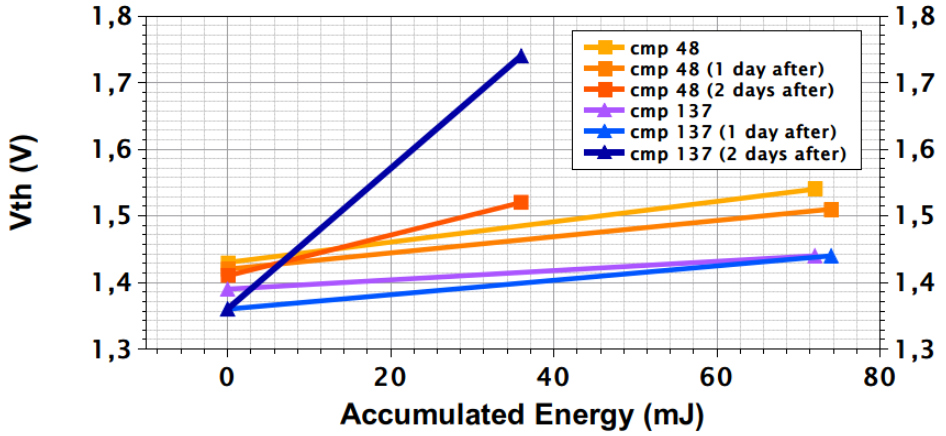

Figure 241: V_{th} variation for p-GaN component from supplier 1, in value, for V_{DS} = 200 V and V_{DS} = 300 V

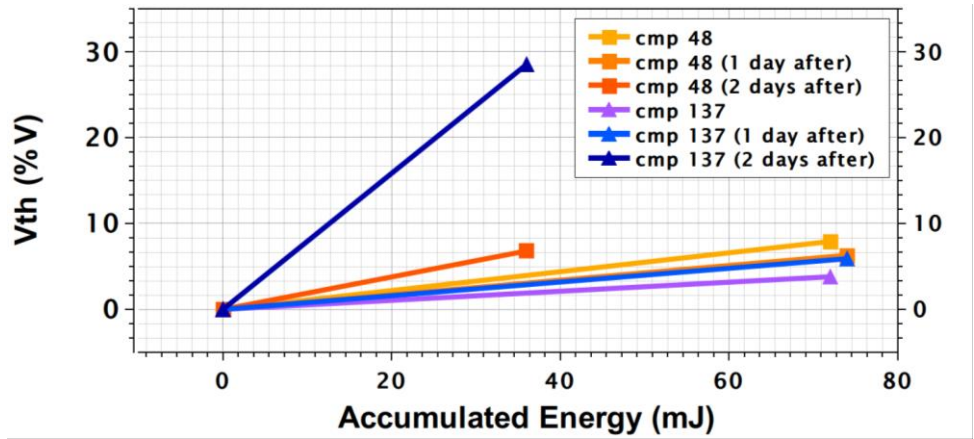

Figure 242: V_{th} variation for p-GaN component from supplier 1, in %, for V_{DS} = 200 V and V_{DS} = 300 V

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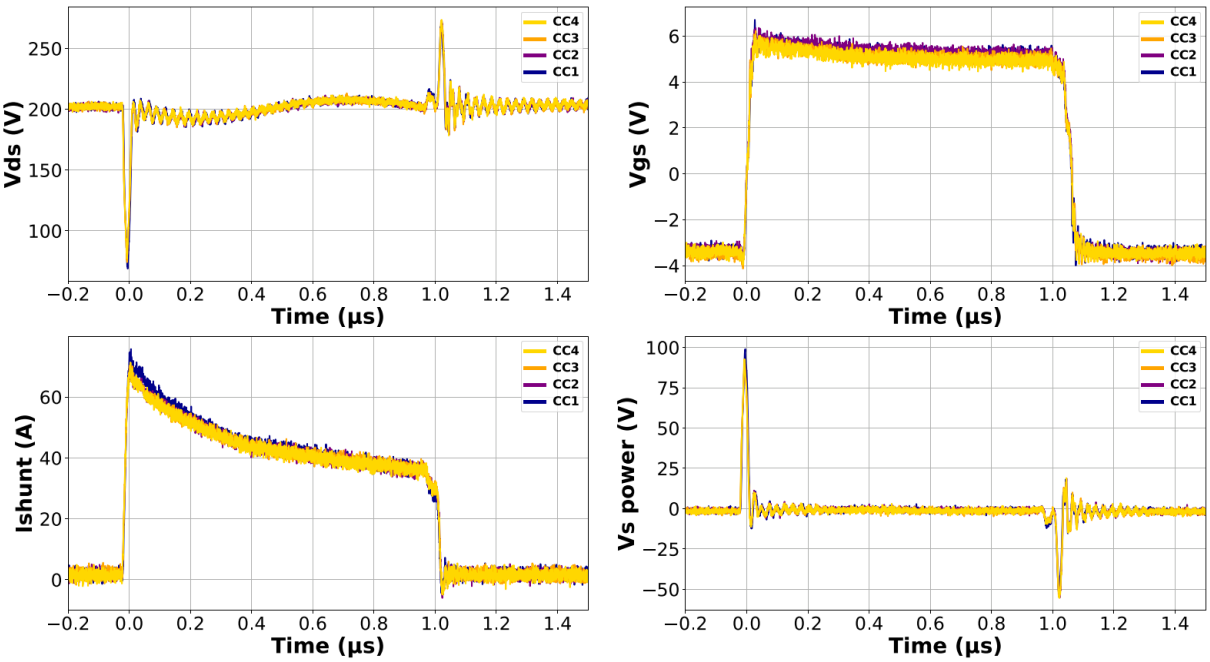

Figure 243: Experimental waveforms during repetitive short-circuits at V_{DS} = 200 V for a p-GaN component from supplier 1

3.2.3.1.2 Supplier 2

The same strategy is adopted for the components of supplier 2. Figure 244 illustrates the repetitive short-circuiting of one of the components of the second supplier, in this case component number 11. Twenty short circuits, divided into two equal sequences, are shown. The legend indicates CCX-Y, with X the number of the short-circuit performed, from 1 to 10, and Y the series, from 1 to 2 here.
As with the components from supplier 1, there are no dynamic variations during successive short-circuits. However, a slight change in the slope of the short-circuit current can be noted, as shown in Figure 244 with the I_{shunt} signal. This slight variation is not considered sufficient to warrant further investigation.

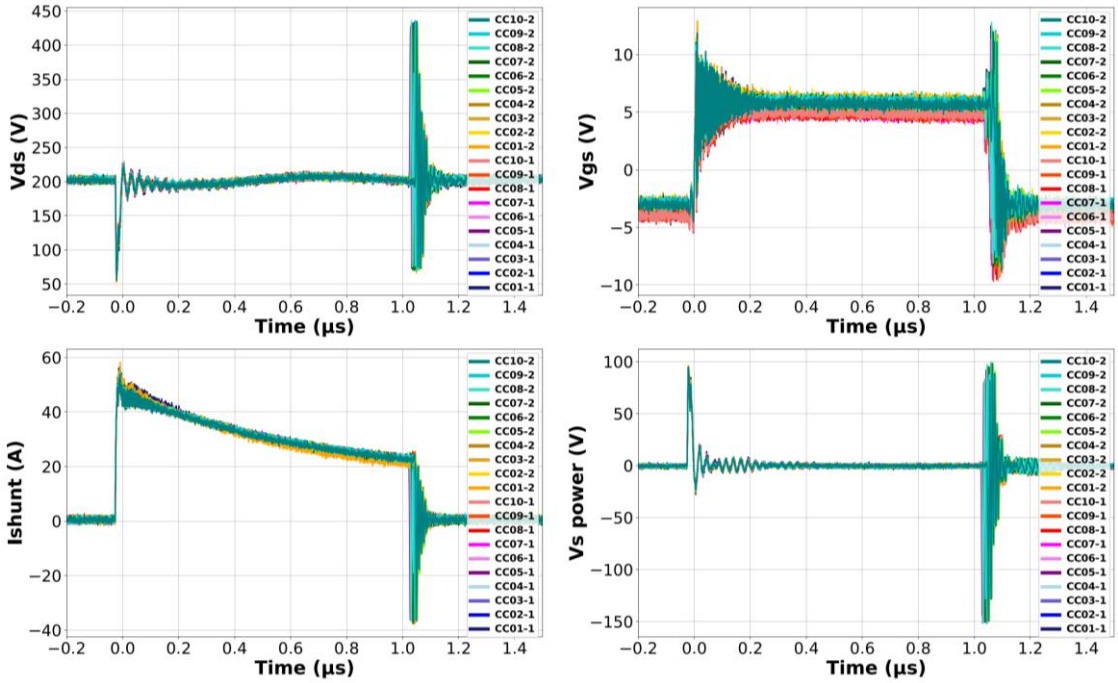

Figure 244: Absence of dynamic variations during repetitive short-circuits with V_{DS} = 200 V for a p-GaN component from supplier 1 on test-board 2023 with 2024 driver

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Electrical characterizations are carried out between each series of short-circuits. Figure 245 illustrates the variations in threshold voltage V_{th} in response to the various short-circuits. As previously, a "Golden Device" component is chosen to ensure that the parametric variations observed are indeed due to the short-circuit phenomenon and not to the B1505 tracer. The electrical characterizations of the golden device component 17 are carried out at the same time as those performed on the short-circuited component 18. Less marked than for the components from supplier 1, the components from supplier 2 nonetheless show a significant variation in V_{th}, happily exceeding 10% or even 20% for component 11 for example. As it was already the case in 3.2.3.1.1, the golden device, even without short-circuit stress demonstrates a variation. However, this variation remains reduced in comparison to the short-circuited components, what proves the V_{th} variation is mainly due to repetitive short-circuits.

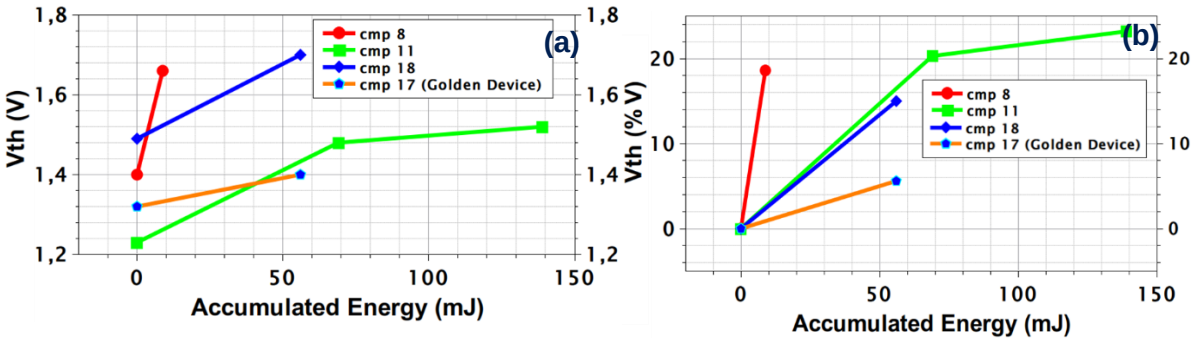

Figure 245: V_{th} variation for p-GaN component from supplier 2 (in value, a-left), (in %, b-right)

The higher variation of V_{th} in the case of supplier 1 (up to 30%) than supplier 2 (up to 20%) suggests deeper traps for the supplier 1. It also implies an increased difficulty to free up the trapped electrons as the traps are deeper and so require more energy to free up the electrons.
Moreover, it can be legitimately asserted the detrapping- are slower than the trapping-mechanisms, as the trapping could occur at high temperature during the short-circuit while the detrapping could occur at reduced temperature, after the short-circuit.

In addition to the threshold voltage V_{th}, the variation of the on-state resistance R_{DS_ON} is studied. The results are explained in the following section.

3.2.3.2 R_{DS_ON} Variation

3.2.3.2.1 Supplier 1

The value of the on-state resistance R_{DS_ON} is studied on the p-GaN components from supplier 1. The measurements are carried out within the same sequence of electrical characterizations at the B1505, after the V_{th} measurements. A first R_{DS_ON} measurement is taken before the short-circuits are applied. This measurement is taken as a reference. Subsequent R_{DS_ON} measurements, taken after the various short-circuits have been applied, are compared with this reference measurement.
Figure 246 shows the variation in R_{DS_ON} for component 69 over two days of testing. Figure 246(a) shows a non-negligible variation after the application of successive short-circuits with a cumulative energy of 36 mJ. Figure 246(b) illustrates the results of applying short-circuits 24 hours after the first ones in Figure 246(a). The variations are in the same trend as before, with an even greater increase in R_{DS_ON} resistance than a day earlier.

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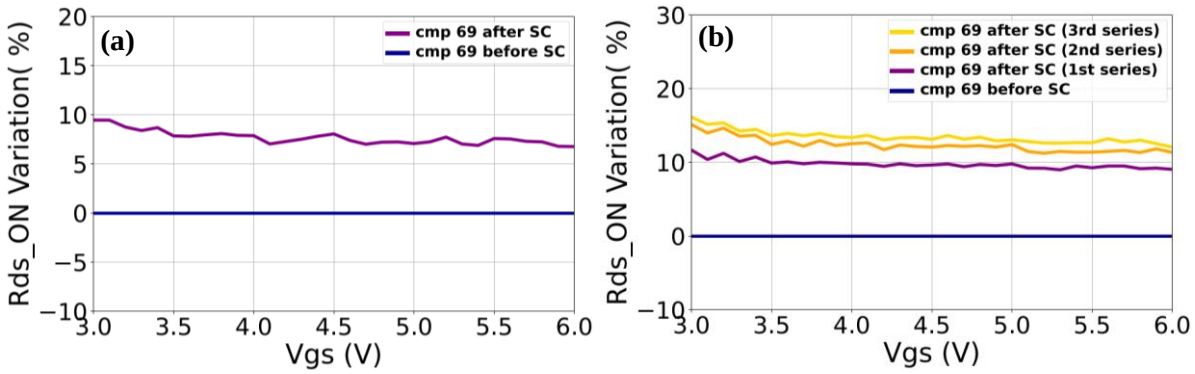

Figure 246: R_{DS_ON} variation for p-GaN component from supplier 1 in % (first day in a-left, one day after in b-right)

Measurements on the other p-GaN components of Supplier 1 give similar results, as shown in *Figure 247*.

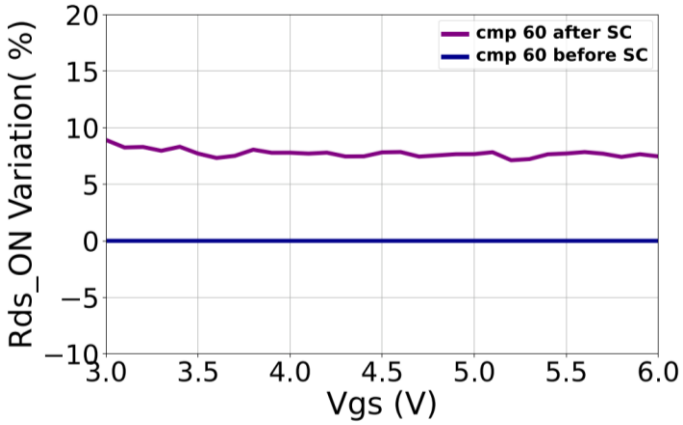

Figure 247: R_{DS_ON} variation for p-GaN component from supplier 1 in %

In comparison, the electrical characterizations carried out in parallel on the Golden Device, as shown in Figure 248, demonstrate negligible variation in R_{DS_ON} in the absence of short circuits. Figure 248 indeed shows no variation for the golden device. This has to be put in parallel to the non-negligible variation measured with the component number 60 shown in Figure 247

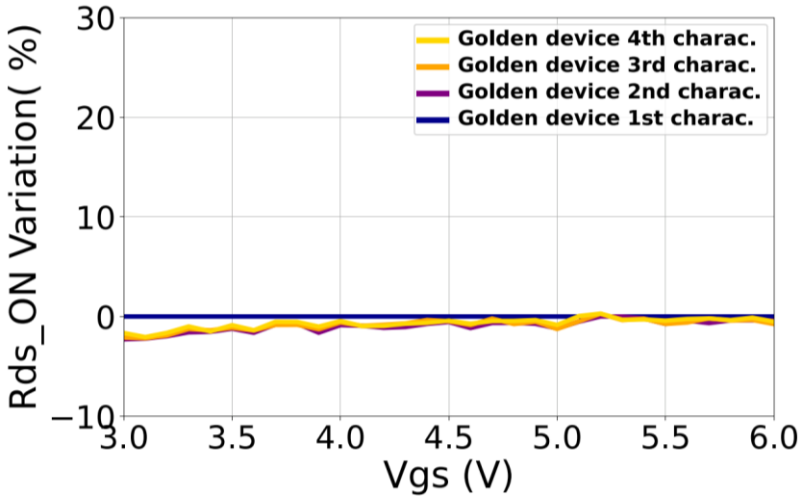

Figure 248: Negligible R_{DS_ON} variation for p-GaN component Golden Device (cmp 34) from supplier 1 in %

It can therefore be stated that short-circuits carried out at V_{DS} = 200 V, in addition to the V_{th} variations observed previously, cause non-negligible variations in terms of R_{DS_ON}.

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As seen previously, it is studied whether the V_{DS} voltage level has an impact on the R_{DS_ON} variation observed. The previous study was carried out at V_{DS} = 200 V so it was decided to work at V_{DS} = 300 V. Each characterization of the short-circuited stressed component is completed by a simultaneous characterization of a Golden Device component.

Figure 249(a) shows the R_{DS_ON} variations of the short-circuited component for V_{DS} = 300 V and V_{DS} = 200 V, as well as the R_{DS_ON} measurements for the Golden Device component.
The first series of short-circuits, carried out at V_{DS} = 300 V, gave no variation in R_{DS_ON}. These tests were repeated 24 hours later with no variation (purple curve in Figure 249(a)).
In view of this, it was decided to return to a short-circuit sequence similar to the one previously carried out, with a short-circuit voltage of V_{DS} = 200 V. Measurement of R_{DS_ON}, two days after the start of the tests, and this time for a drain-source bias V_{DS} = 200 V, yields variations similar to those observed previously, for example in Figure 246. At a lower energy level than in the V_{DS} = 300 V tests, the variations in R_{DS_ON} following the short-circuits for V_{DS} = 200 V are immediately visible.
The variation in R_{DS_ON} observed is indeed due to short-circuits, as shown in Figure 249(b), where no variation in the golden device number 48 can be distinguished between each electrical characterization.

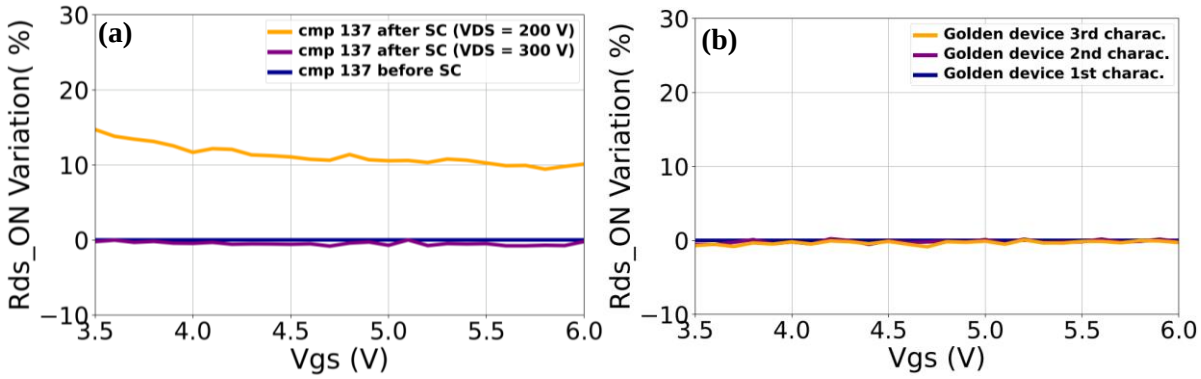

Figure 249: Presence or absence of R_{DS_ON} variation for V_{DS} = 200 V or V_{DS} = 300 V (a-left) and absence of variation seen on Golden Device (number 48) (b-right)

The R_{DS_ON} graphs presented above are produced for a voltage V_{GS} > 3 V. In fact, the measurements are carried out for a drain current I_d stabilized at 10 A. Figure 250 shows the V_{GS} voltage shift and therefore the offset on the threshold voltage, as well as the need to zoom in on the V_{GS} part (3 V / 6 V) or even (3.5 V / 6 V) of Figure 249. It can also be noted the lower saturation level, in relation to the already seen increase of R_{DS_ON}.

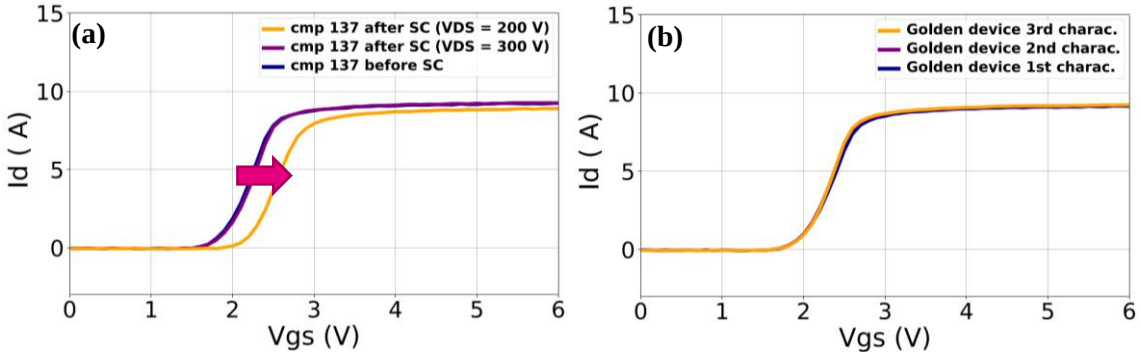

Figure 250: V_{th} shift and increase of R_{DS_ON} for short-circuited component (a-left) and absence of variation for Golden Device (b-right)

Additional measurements are taken 24 hours later on short-circuited device and golden device with the yellow curve on Figure 251. It can be observed a return back to the initial state in the absence of a short-circuit for the previously short-circuited component, number 137. As expected, no variation is noticed on the golden device. For its part, the golden device remains invariant as no shift can be seen in Figure 251(b).

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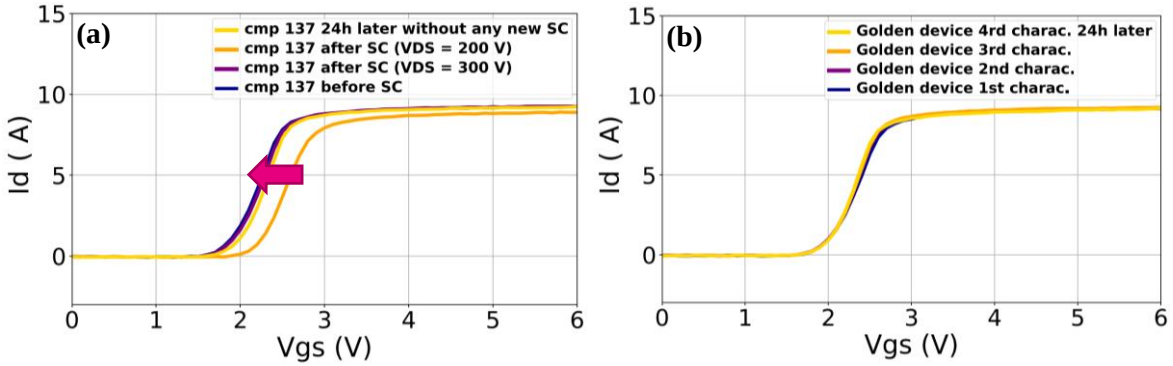

Figure 251: Return back to initial state in the absence of a short-circuit for previously short-circuited component (a-left) and absence of variation for Golden Device (b-right)

3.2.3.2.2 *Supplier 2*

The study of R_{DS_ON} is carried out in a similar way on the p-GaN components of Supplier 2. Figure 252 shows the R_{DS_ON} variation of the short-circuit-stressed component 18, compared with the Golden Device component 17. Several things can be noted. Firstly, unlike the components from supplier 1, repetitive short-circuits result in an improve of R_{DS_ON} resistance of around 15%. This variation is confirmed by parallel measurement of R_{DS_ON} for an unstressed component, which shows no considerable v variation.
The impact in terms of facilitated drain current conduction can be seen in Figure 253.

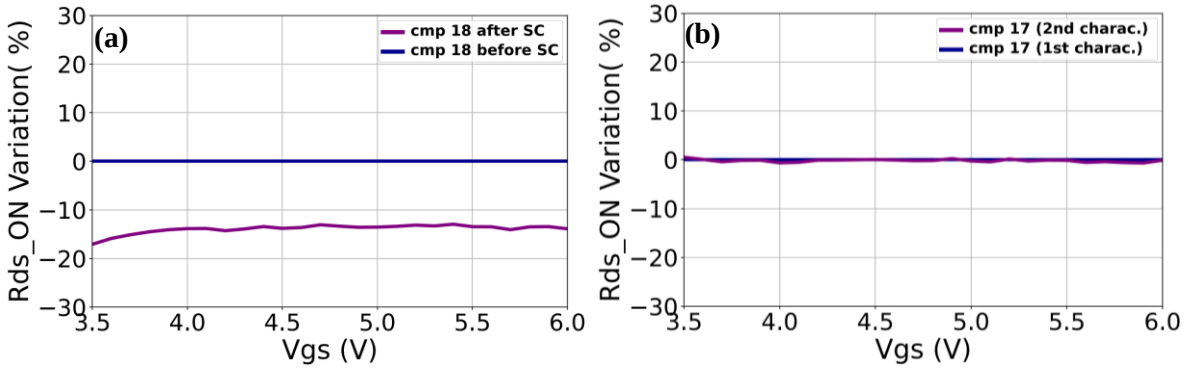

Figure 252: Presence at V_{DS} = 200 V of R_{DS_ON} variation (a-right) and absence of variation seen on Golden Device (b-left)

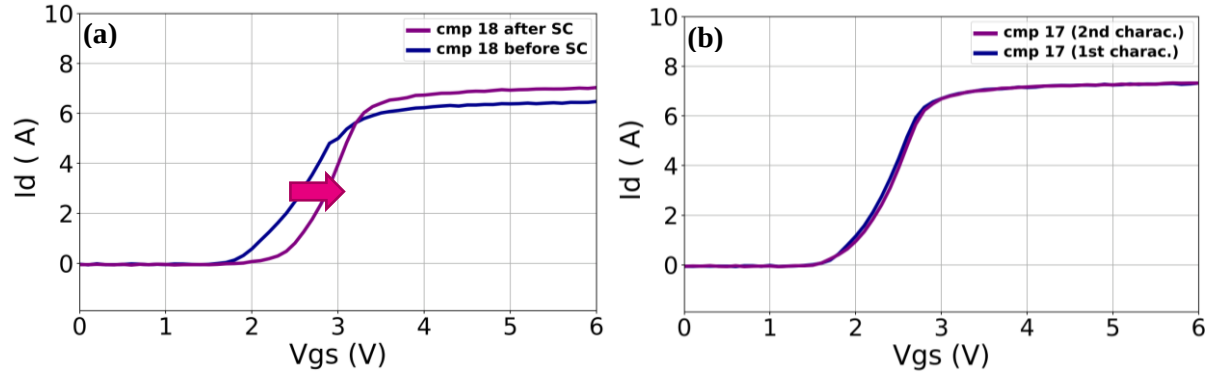

Figure 253: V_{th} shift and decrease of R_{DS_ON} for short-circuited component at V_{DS} = 200 V (a-right) and absence of variation for Golden Device (b-left)

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Figure 253 shows the increase in V_{th} since component 18, after the application of short-circuits, conducts later, similar to what was seen in Figure 250. On the other hand, conduction is improved with an increased level of current saturation, which is in line with the decrease in R_{DS_ON} resistance. In parallel of that and proving the shift is due to the short-circuit, curves for the Golden Device component overlay.

Zooming in on Figure 253 for the Golden Device component (Figure 254) nevertheless reveals a slight shift in V_{th} observed above in Figure 245 with the slight shift in conduction of component 17. However, this zoom does not reveal any increase in R_{DS_ON} of the Golden Device, in line with what was seen earlier in Figure 253. Because the short-circuit V_{DS} voltage is more limited than that of the components from supplier 1, the components from supplier 2 will not be studied for V_{DS} = 300 V.

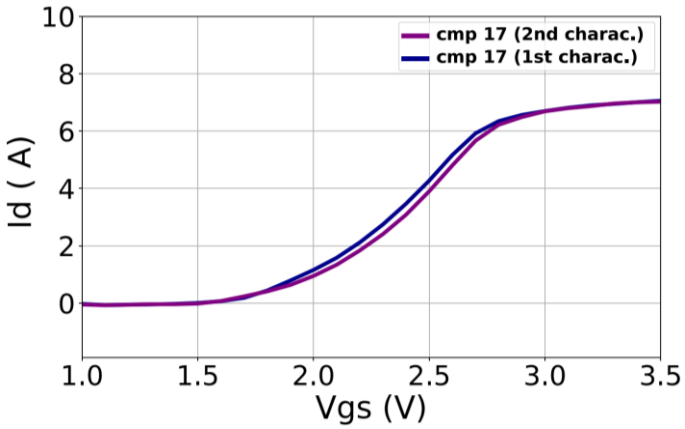

Figure 254: Reduced shift of conduction due to the variation of V_{th} observed upstream for Golden Device (number 17)

The study of parametric variations has highlighted two phenomena linked to the application of non-destructive repetitive short-circuits. Firstly, short-circuits have an impact on the variation in threshold voltage V_{th}, with a non-negligible increase. Secondly, the application of repetitive short-circuits also causes a variation in the on-state resistance R_{DS_ON}. If the V_{th} variations are in the same direction for both suppliers, the same thing cannot be said for the R_{DS_ON} variation which does not evolve in the same direction with an increase in the case of Supplier 1 components and a decrease in the case of supplier 2.

One possible hypothesis can be formulated. Still trapped electrons in the case of supplier 1 might explain the increased value of R_{DS_ON} while the release of formerly trapped electrons in the supplier 2, by supplying additional conductive electrons, decreases R_{DS_ON} in the case of supplier 2. As a consequence, the evolution of R_{DS_ON} would be dependent on the equilibrium between electrons trapping / detrapping. Another possible hypothesis is that repetitive short-circuits act on traps that are not the same than for V_{th} and classical Dynamic R_{on}

Finally, in the case of supplier 1 components, it turns out that increasing the V_{DS} voltage during short-circuits is not necessarily more deleterious, with no impact at V_{DS} = 300 V. It was quite realistic to expect higher degradation at higher drain – source polarization or at the least, the same level of degradation. The experience proved the contrary with an absence of variation at V_{DS} = 300 V. This phenomenon could have several explanations. Higher drain – source polarization implies a higher temperature and so a higher electron mobility what could lead to less trapping effect. A higher V_{DS} implies also a higher electric field and could also prevent trapping effect or at least enable very fast detrapping during the short-circuit as it has been explained by the authors of [168–171]. In this way trapping effect could occur only at intermediate level of V_{DS}.
Impact ionization with the possible generation of charge carriers at the AlGaN / GaN interface and therefore the compensation of V_{th} and R_{DS_ON} variation has been proposed. Detrapping effect have been encountered in [170] and a 2DEG mobility increase has been observed, what could make a possible link to the decreased value of R_{DS_ON} of devices from supplier 2.

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3.3 Different Types of Breakage

The breakage of component during short-circuit is always indicated by visible and sometimes severe damage, as can be seen in Figure 255 for instance, with the breakage of the device after a short-circuit failure at V_{DS} = 400 V. The conduction duration was as before set to 2 µs but the component broke just after 500 ns of conduction. Zooming in on the daughterboard and DUT, face down shows that the metallic pads have been melted and even the PCB tracks have been damaged.

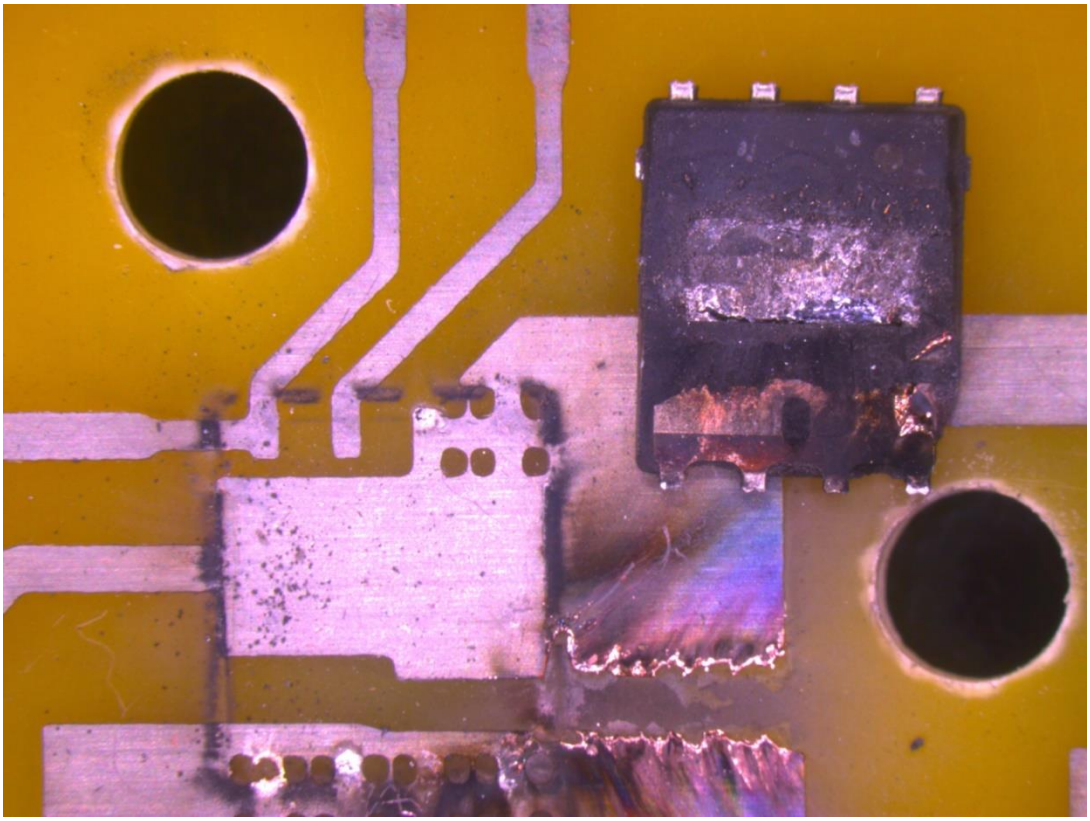

Figure 255: Image of the daughter board and the p-GaN component (supplier 1) after a breakage at V_{DS} = 400 V

It is also interesting to note that all the components break at the top, a region assumed to be closer to the gate.

Figure 256: Images of several broken DUT after repetitive short-circuits

In addition to these particularly violent breakages, it was possible to observe that the breakage scenario was not singular. Three types of breakage can be analysed.

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3.3.1 Breakage due to Accumulation

Firstly, breakage due to short-circuit accumulation seems to be the most obvious case. This is shown in Figure 257. The component was able to withstand several successive short-circuits. However, during the last short-circuit, which is identical to the previous ones, the component breaks in full conduction. This phenomenon occurs on all components and remains the predominant case of breakage.

As shown in Figure 222, Figure 224 and Figure 225, if components can withstand a certain amount of stress, the application of additional stress, albeit identical and previously withstood, causes the component to break.

As shown in Figure 257, the component perfectly withstands the 3rd short-circuit of the third series, lasting 750 ns at a voltage V_{DS} = 200 V. However, during the last short-circuit, which was fatal despite having identical characteristics, the component broke prematurely after only 450 ns of conduction, whereas it had repeatedly held 750 ns of conduction previously.

Figure 258 illustrates similar behaviour. Here, the component repeatedly withstands an 800 ns short-circuit and finally breaks after three identical short-circuits during exactly the same short-circuit, but this time after only 650 ns of conduction.

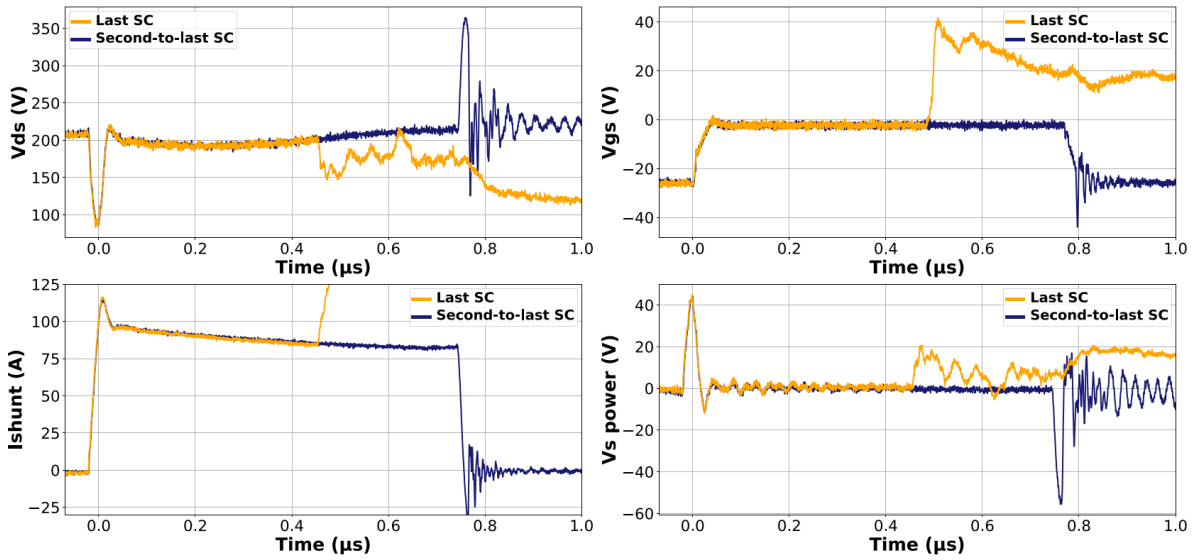

Figure 257: breakage of the DUT after the last repetitive short-circuit too many

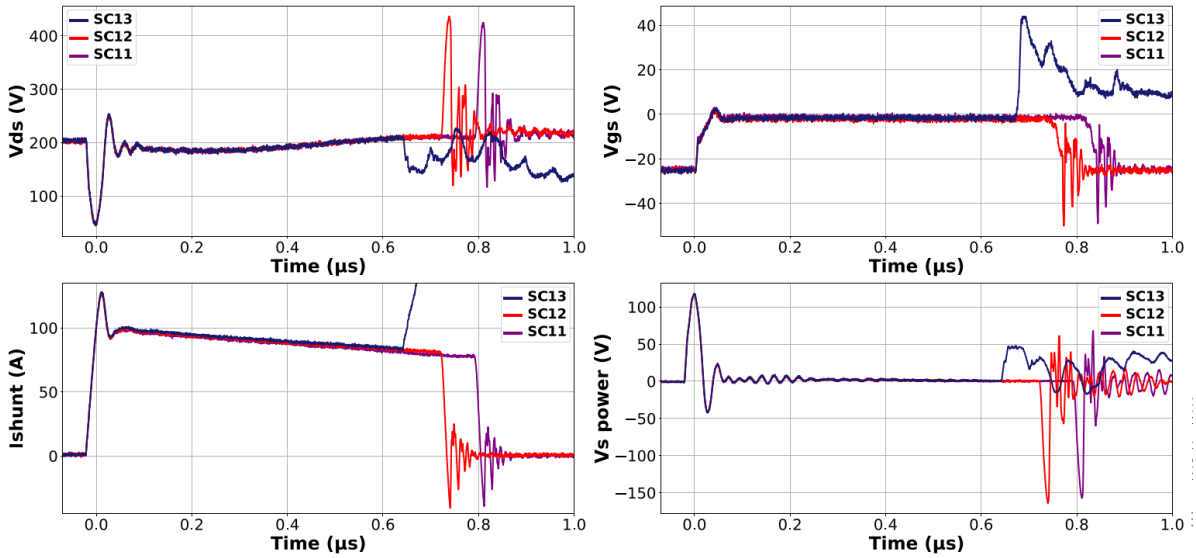

Figure 258: Breakage of the component 17B after several identical short-circuits

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In the present case, self-heating could not be held responsible, since a considerable time - five minutes is left between each short-circuit in the same series. Components therefore break as a result of the accumulation of repetitive short-circuits and degradation mechanisms involving more than just energy. If energy alone were the cause of breakage, the component would not have been able to withstand the previous short-circuit with identical characteristics.

This unsurprising phenomenon of breakage can be contrasted with two other, more surprising phenomena.

3.3.2 Limit in Voltage, Dielectric Breakdown or Impact in the Gate

The first astonishing case of breakage remains following the voltage rise, particularly on the components of supplier 1, illustrated in Figure 233. Figure 259 shows the V_{DS} and V_{GS} signals during this V_{DS} voltage rise. Two observations can be made. Firstly, breakage cannot simply be related to energy aspects, since the last short-circuit becomes fatal at V_{DS} = 400 V and at a reduced energy compared with the previous short-circuit at V_{DS} = 350 V. What is more, these failures occur very early in terms of cumulative energy, earlier than components short-circuited at V_{DS} = 200 V and capable of withstanding several dozen repetitive short-circuits. This type of breakage raises the question of a possible dielectric breakdown. Nevertheless, the overvoltage generated on the V_{DS} signal remain well within the 650 V limit of the component. A high-voltage probe capable of measuring signals up to 1200 V is used on the V_{DS} signal to ensure correct measurement of overvoltage, particularly during turn-off. The overvoltage seen are therefore real, and are not truncated by any limitations of the measurement probe.

The question of an impact on the gate can also be raised, with, as can be seen from the V_{GS} signal in Figure 259, a non-negligible degradation of the signal at turn-ON, as the drain-source polarization increases. This questioning can also be linked to the parametric variations observed on V_{th} and therefore at gate level. It can therefore be resolutely asserted that short-circuits have an impact on the gate.

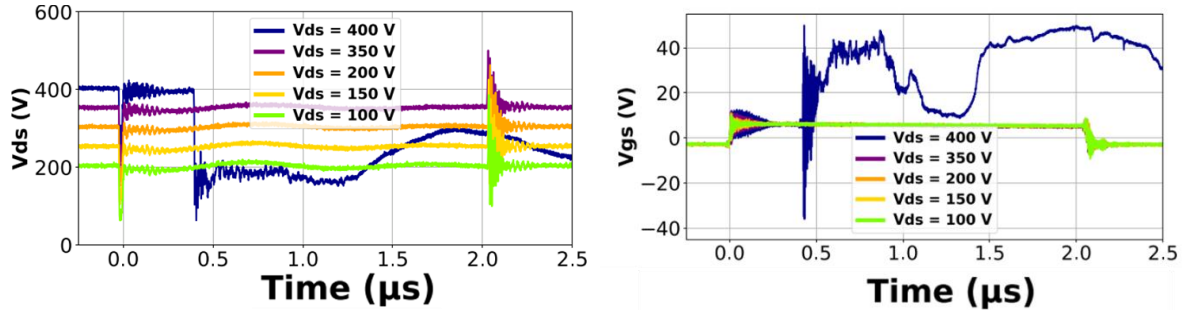

Figure 259: Experimental waveforms during a progressive rise in voltage for a p-GaN component from supplier 1, with an observed degradation of the V_{GS} signal and a maximum of 400 V for V_{DS} signal before breakage

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3.3.3 Another Type of Breakage: Unwanted Turn-ON After Successful Turn-OFF

The second astonishing case involves an untimely ON switch, a few hundred nanoseconds after a successful turn-OFF. The component is able to withstand the short-circuit for 1 µs, but switches on undesirably 600 ns later. The DUT then breaks immediately, the effects of the previous short having been unable to be mitigated during the several-minute interval normally separating each short-circuit. This phenomenon has also be seen with silicon and silicon carbide devices [172–177].

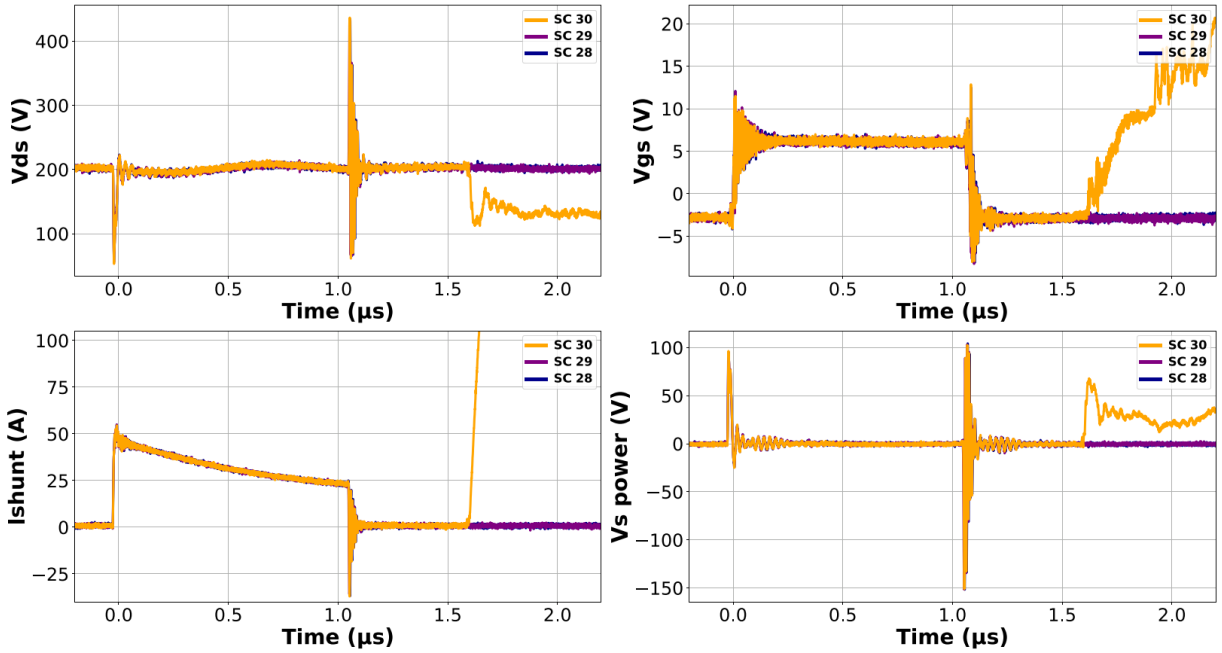

Figure 260: Breakage of the DUT despite a successful turn-OFF

This phenomenon is also seen at higher drain-source voltages, as illustrated in Figure 261, where the DUT, although having withstood the short-circuit at V_{DS} = 300 V, will start conducting again a few hundred nanoseconds later, causing its instantaneous breakage. The curves are superimposed below, with the short-circuit supported by the component in violet and the short-circuit occurring a few hundred nanoseconds later in red, which turned out to be fatal.

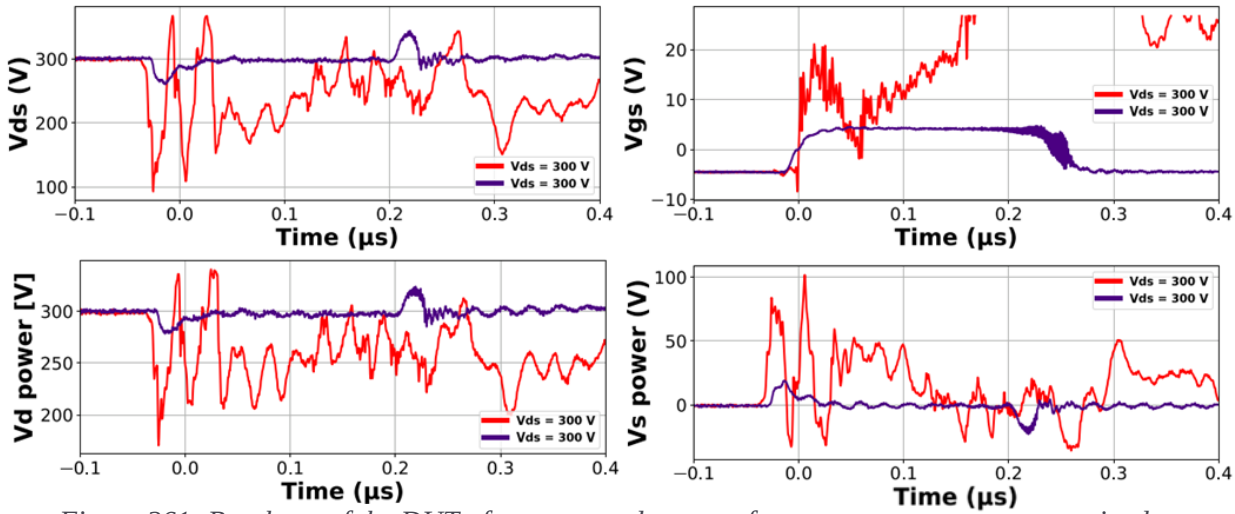

Figure 261: Breakage of the DUT after unwanted turn-on few nanoseconds after a sustained short-circuit at V_{DS} = 300V

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3.4 Possible Explanation about the Higher Robustness of Components from Supplier1

The components tested from the two suppliers were chosen with similar characteristics, particularly in terms of current rating and on-state resistance. What is more, most robust components, from supplier 1, have a higher current rating (15 A versus 11 A) and generate a higher short-circuit current. The solution to this increased robustness is therefore not to be found in these parameters.

Theoretically, the structure is similar, with a normally-off p-GaN structure. Both products come from the same manufacturer. However, access to the precise structure of the component, and in particular the "cooking recipe" of each manufacturer, is unknown, for evident reasons of industrial secrecy.

It was therefore decided to look at other parameters that could have an impact on short-circuit robustness.
The C_{iss}, C_{oss} and C_{rss} capacitances given in the product data sheets of the two suppliers are slightly different. According to Table 28 below, the values are quite different, ranging from simple to double.

	Input Capacitance (Ciss)	**Output Capacitance (Coss)**	**Reverse transfer Capacitance (Crss)**
Supplier 1 (V_{GS} = 0 V;V_{DS} = 400 V; f = 1 MHz)	125 pF	70 pF	1 pF
Supplier 2 (V_{GS} = 0 V; V_{DS} = 400 V; f = 100 kHz)	70 pF	30 pF	0.5 pF

Table 28: C_{iss}, C_{oss} and C_{rss} values for p-GaN components from two different suppliers (Table 1)

It was decided to verify these values experimentally on the B1505 curve tracer. The results are shown in Figure 262. C_{iss} and C_{oss} capacitance values are significantly higher for components from supplier 1 than supplier 2.
For C_{rss} capacitances, the values are very low, barely in the picofarad range, and the B1505 measurement is not considered sufficiently reliable. C_{rss} is hence not studied. C_{iss} and C_{oss} capacitance measurements, on the other hand, are repeated to ensure repeatability and accuracy, as shown in Figure 263 in the case of C_{oss} capacitance measurement for component from supplier 2.

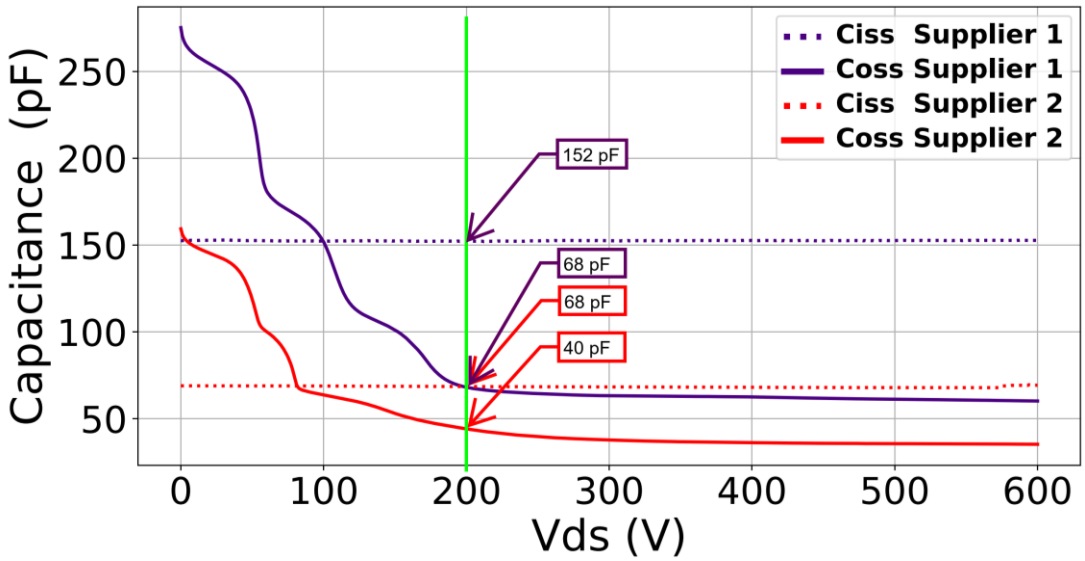

Figure 262: C_{iss} and C_{oss} capacitance of components from suppliers 1 & 2

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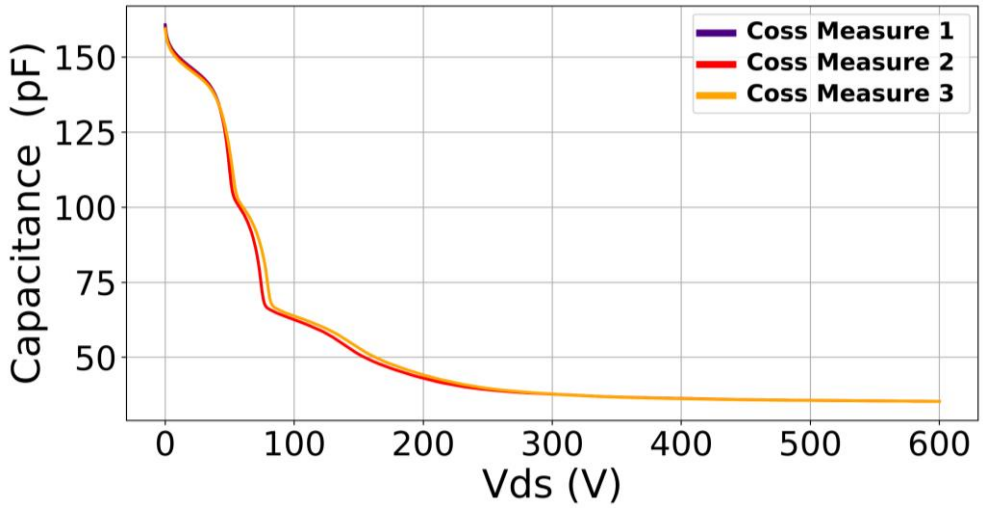

Figure 263: Successive measurements of C_{iss} for component from supplier 2

Components from supplier 1 demonstrated increased robustness, whether in terms of energy, maximum V_{DS} voltage or short-circuit stability. The absence of any significant differences in electrical parameters, apart from the C_{iss}, C_{oss} and C_{rss} capacitances, means that the explanation for the increased robustness lies in these small differences. This makes sense insofar as it is only the internal structure of the component and the arrangements of the various materials specific to each supplier, thus impacting the values of C_{iss}, C_{oss} and C_{rss} capacitances, that could explain this difference in robustness. It can therefore be concluded that the capacitances of p-GaN HEMT-type components could have an impact on short-circuit robustness.

3.5 Conclusion

Chapter 3 shed light on the impact of repetitive short-circuits and highlighted varying behaviours based on component types. For d-mode components, dynamic variations in the saturation level of short-circuit current were observed, along with current increases shortly before failure. The location on the wafer appeared critical with very different results among the different batch. Significant V_{th} variations were also identified during electrical characterizations. In contrast, p-GaN components demonstrated strong self-limiting drain current behaviour, confirming their enhanced short-circuit robustness. However, these components showed exacerbated V_{th} variations, reaching up to 30% in some cases.
Unexpectedly on-state resistance variations have been observerd. It differs by supplier, with increases for Supplier 1 and decreases for Supplier 2, suggesting short-circuits affect more than just the gate region. Another surprising finding showed that a V_{DS} bias of 300 V was less detrimental than 200 V for Supplier 1 components, what could be interesting to more deeply analyse. A possible explanation had been found to explain the different short-circuit behaviour between suppliers. It may come from higher C_{iss} and C_{oss} capacitances for more robust components. Lastly, the chapter identifies various failure types, including accumulation phenomena, voltage limits, and unwanted returns to the on-state.

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4

Conclusion & Perspectives

This thesis has lifted the veil on many aspects of the short-circuit phenomenon affecting GaN 650 V HEMTs. The first chapter opens by emphasizing the critical transition currently underway in power electronics. After decades of advancements focused on enhancing the reliability and optimization of silicon-based power devices, new technologies are emerging to meet evolving global challenges. These include worldwide energy conservation efforts and according to the growing electrification of systems, driven by the rise of electric vehicles and renewable energy integration, major transformations in energy distribution and grid infrastructure. However, progress is rarely instantaneous. Despite their significant potential, GaN power devices still face hurdles, particularly in terms of reliability and robustness. After having fully understood the physical mechanisms governing the operation of GaN HEMT, the formation of the 2DEG and the several structures of devices, a critical review of the state of the art in short-circuit performance had been carried out. Several failure mechanisms were thoroughly explored. While thermal runaway might initially seem the most apparent explanation, alternative physical phenomena challenge this assumption, especially in scenarios involving reduced failure energy. Charge-field interactions were closely analysed for their influence on device behaviour. Furthermore, impact ionization processes, involving hot electrons and hole generation, provide a plausible explanation for failures beyond thermal effects. A third possible cause of failure involves destructive oscillations. According to the literature, these oscillations can be linked to several origin, such as negative capacitance associated with Miller capacitance [130], LC parasitic elements due to packaging or influence of the silicon MOSFET [77]. These oscillations can affect the V_{DS} signals, resulting in an overcome of the breakdown voltage or the V_{GS} signal and an erratic behaviour, resulting to the failure of component. This critical analysis of short-circuit failures has helped to clarify the previously ambiguous state of the art, where conflicting findings were often presented. It has enabled the isolation of various explanations for short-circuit failures, providing a more solid foundation for designing the experimental test bench and fostering a more informed and critical approach to analysing future component failures during short-circuit testing.

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The Chapter 2 focuses on the design of the experimental bench. Although relatively straightforward at first glance, it presented several challenges and required numerous optimizations, particularly in relation to common-mode currents. This process highlighted the enhanced robustness and stability of certain components, while revealing the heightened sensitivity of others. A SPICE simulation, corrected as the thesis progressed, enabled to finely understand the behaviour of the experimental test bench, thereby providing the keys to optimising it and resolving the problems encountered. Based on these findings, the first version of the test-bench has been optimized. A second experimental test bench was developed, moving away from the motherboard-daughterboard configuration. This new design further improved short-circuit performance, specifically in terms of the V_{DS} voltage drop and the stability of the V_{DS} and V_{GS} signals. That enables to be in accordance with the future JEDEC standards about short-circuit test.

The Chapter 3 reveals the impact of repetitive short-circuits but also the different behaviour depending on the type of component. For d-mode components, dynamic variations were observed in the saturation level of the short-circuit current. A sudden increase in short-circuit current was also noted in certain components, which can be considered as precursor sign of impending failure. Finally, significant variations in the threshold voltage V_{th} were observed during the various electrical characterizations conducted with the B1505A. For the normally-off structure, the p-GaN components, consistent with existing literature, exhibited particularly high levels of self-limiting drain current, supporting the idea of enhanced short-circuit robustness for these devices. The dynamic variations observed in d-mode components were not found in p-GaN components. However, V_{th} variations, already notable in normally-on devices, were exacerbated in the p-GaN components, reaching up to 30% in some cases. The study of on-state resistance variations yielded unexpected conclusions, with an increase observed for Supplier 1 and a decrease for Supplier 2. Nevertheless, this reinforces the idea that while it has been established that short-circuits impact the gate region, as evidenced by V_{th} variation, this is not the only area affected by such significant stress. Another puzzling observation arose during the study of components from Supplier 1. A drain-source bias of V_{DS} = 300 V was found to be less detrimental than a bias of V_{DS} = 200 V. This phenomenon remains unexplained but warrants further in-depth investigation in future analyses. The stark differences in short-circuit behaviour between components from Supplier 1 and Supplier 2 could potentially be attributed to higher C_{iss} and C_{oss} capacitances in the more robust components. Finally, Chapter 3 highlights the different encountered types of failures, including accumulation phenomena, voltage limits, and unwanted returns to the on-state.

The corrections and improvements led to the experimental test bench took significantly more time than initially foreseen. While numerous tests were conducted, both to evaluate single short-circuit limits of components and to perform repetitive short-circuit series to observe potential parametric and dynamic variations, there remains room for further testing.

First, the study of normally-on components revealed that the location on the wafer had a significant impact on short-circuit robustness. Although the distinction between the three lots of normally-on components was clear, having precise mapping of the chip locations on the wafer would have been valuable. This would allow for conclusions regarding the impact of doping, epitaxial thickness, dislocations, or mechanical stress. This represents the first promising perspective for future work on short-circuit studies.

Second, the focus on p-GaN components from the two suppliers came at the expense of analysing the short-circuit performance of cascode components. Investigating these devices and comparing them to the d-mode components which are exactly the same incorporated in cascode structure would have been interesting.

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Finally, the study of short-circuit performance in p-GaN components with similar characteristics but from different suppliers highlighted C_{iss} and C_{oss} as physical parameter indicative of greater robustness. Expanding this analysis to additional suppliers would be beneficial. Additionally, a deeper investigation into component failures, particularly through Transmission Electron Microscopy (TEM) or Photoluminescence analysis, would provide further insights. Time-Resolved Photoluminescence (TRPL) could also be used to analyse defects and trap states induced by hot electrons in the DUT, by measuring luminescence after laser excitation[178–180]. Deep Level Transient Spectroscopy (DLTS) could also be interesting for studying structural changes caused by hot electrons in materials [181].

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Appendices

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5.1 Appendix 1: Heterojunctions mechanisms explained

Heterostructures are characterized by Fermi level of each of the components of this heterojunction and thus by the potential barrier that will form at the various interfaces. This barrier conditions the passage of an electron or a hole from one material to another. It is determined by comparing the energy required for an electron in each material to be extracted from that material and moved infinitely away from it.

5.1.1 Recap about doping semiconductors

- **Intrinsic semiconductors**: by definition, an intrinsic semiconductor is a pure semiconductor with no structural defects or chemical impurities. Its electrical behaviour is solely linked to its structure. Valence electrons therefore have no chance of becoming free electrons. This is what happens at 0 K. Beyond this, thermal agitation, as it increases, will free some of these electrons, moving them from the valence band to the conduction band and thus allowing the current to flow [182]. To understand the mechanisms involved, the example of silicon can be explained. The atomic number of Si is 14.

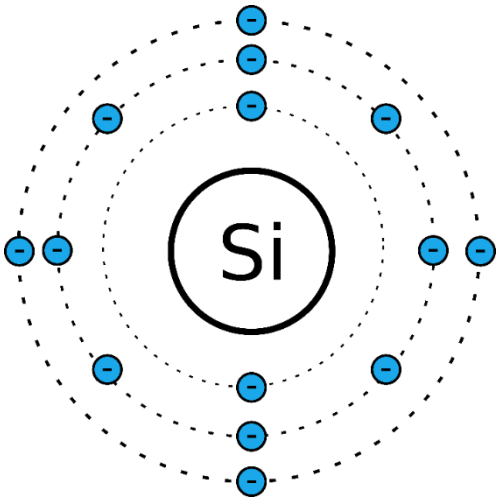

Figure 264: electrical structure of silicon atom

Silicon then has 4 valence electrons distributed over the last layer (M).
According to the octet rule, in order to stabilise itself, silicon will tend either to lose its 4 electrons and ionise into Si^{4+}, its outer layer thus becoming the (L) layer, or, on the contrary, to try to 'gain' 4 electrons by creating covalent bonds.
This phenomenon can be observed in the silicon crystal. Each atom in the lattice shares 1 electron with each of its neighbours, thus obtaining 8 peripheral electrons through covalent bonds.

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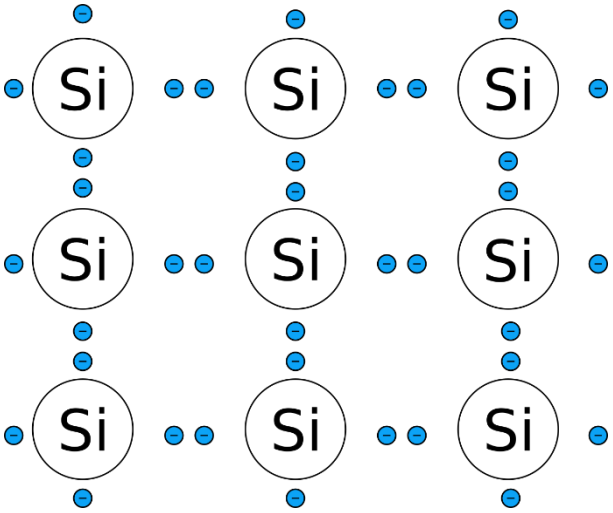

Figure 265: illustration of the sharing of electrons to satisfy the octet rule, resulting in a solid Si lattice

These covalent bonds are very strong, the electrons are strongly bonded and the crystal is therefore particularly stable. It is therefore unlikely that a bond will break and that electrons will circulate within the lattice. The only way to get electrons to circulate within the crystal is to break these covalent bonds. Energy must therefore be supplied by heating.
In this respect, the conduction of an intrinsic semiconductor depends solely on temperature. At 0 K, it is insulating. At room temperature (298 K), the energy supplied will enable certain bonds to be broken. When this bond is broken, a free electron appears, able to circulate in the network and therefore conduct electricity. The disappearance of the bond creates an empty entity, without charge, called a hole.
The electron also leaves an unattached proton in the Si atom, which is now not paired with an electron, giving the Si atom a positive charge. This charge is offset in the lattice by the negative charge of the free electron.

As a reminder, the thermal fluctuation energy is $\frac{1}{2}.k_B.T$
Using silicon as an example, the gap is 1.12eV, i.e. 87 times the thermal agitation energy at 25°C. The energy supplied will therefore only enable a tiny number of bonds to be broken. Only 3 electrons out of 10^{13} atoms will be involved [183], far too few to qualify as a conductor. The gap thus remains unbridgeable, making silicon, like other intrinsic semiconductors, an insulator.

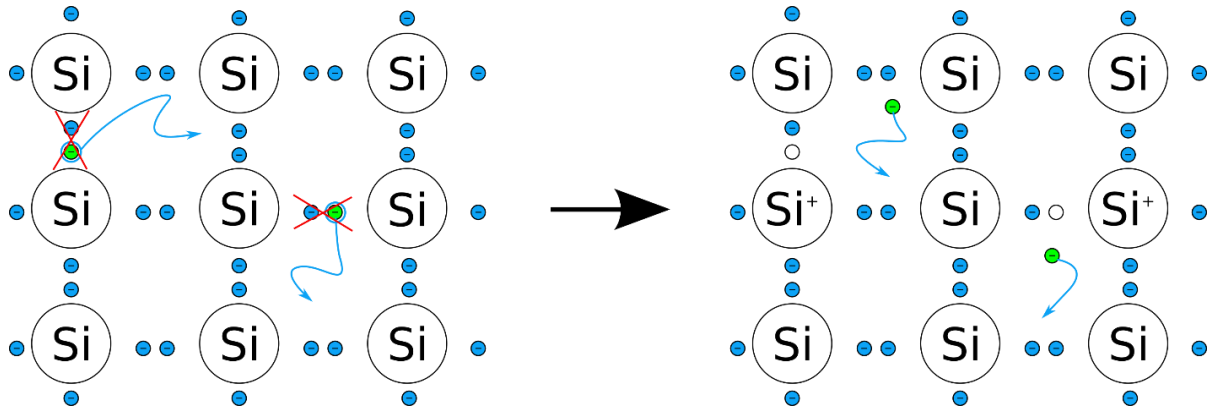

Figure 266: breaking of a covalent bond within the Si lattice and de facto circulation of a free electron within the lattice and creation of a hole

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In the case of an intrinsic semiconductor, every time a free electron is created, a hole appears. Their concentration is exactly the same. It will be seen that this is no longer the case with extrinsic semiconductors.

- **Extrinsic semi-conductors**: unlike the intrinsic conductors mentioned above, extrinsic semi-conductors are not pure because they contain impurities, called dopants, of the N or P type. These impurities, via the extra or extra electrons they possess compared with the electron pattern of the rest of the network, allow the circulation of free electrons (N-type doping) or holes (P-type doping). This doping creates additional energy levels within the band gap.

- **N doping**: a chemical element with one more valence electron than the chemical element making up the lattice is added. The example of silicon for the lattice and Arsenic (As) for the doping element is taken. The As atom shares 4 electrons with the Si atom and has an excess5th electron. As the lattice is much more stable with 4 electrons instead of 5, this 5th electron will easily move outside the lattice. This 5th electron is therefore in an additional energy level, high in energy and very close to the conduction band (a few units, at most a few tens of meV below the conduction band).
  It will therefore very quickly pass into the conduction band by thermal excitation, becoming free and thus participating in conduction. This electron remains free most of the time. However, it can sometimes fill a hole in a Si atom (a recombination phenomenon, albeit of low proportion, as seen in the case of intrinsic semiconductors). These free electrons are therefore considered to be the majority carriers, while the rare holes are the minority carriers.
  The Arsenic atom therefore acts as an electron donor, with the 'free' electrons from these impurity atoms becoming positively ionised when the electron leaves.

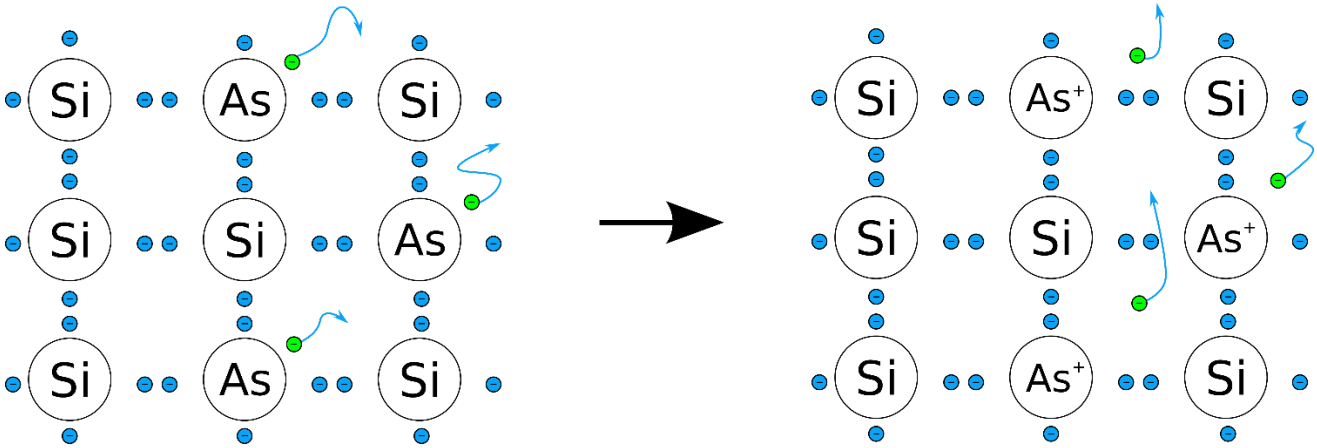

Figure 267: Illustration of N-type doping with arsenic, the As atom gives a free electron, for conduction

- **P doping**: unlike N doping, here a Si atom is replaced by an element from column III of the Mendeleyev table, such as Boron, which therefore has 3 electrons on its periphery. This creates an empty orbital located slightly above the Valence band (around 50 meV). This is because the impurities in the lattice will tend to attract an extra4th electron in order to stabilise the lattice (unlike the N type, which tended to reject it in order to increase its stability).
  The boron atom is trivalent and the Si atom is tetravalent. A bond will therefore be missing between these two atoms, compared with the usual configuration of the Si lattice, and a hole will appear, constituting the free carriers.
  With thermal excitation, an electron from the outer layer of a silicon atom (a valence electron) will easily detach and fill this empty orbital, which is only slightly higher in energy than its starting level, thus creating a hole in the outer layer of the silicon, which will then participate in conduction. The silicon atom loses an electron and becomes positively charged, a charge compensated by the

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negative charge of the boron atom, which becomes tetravalent (normally trivalent). A valence electron from another Si atom can then fill the hole and offset the positive charge, creating a hole and a positive charge on the Si atom to which it was initially bonded. In this way the hole has migrated and participates in conduction.
The empty boron orbital can also be filled by a free conduction electron, but these electrons are in low proportion (free electrons will mainly bind silicon and boron. They therefore recombine very little with a hole).
Doping is said to be sufficient when the number of holes (majority carriers) greatly exceeds the number of free electrons (minority carriers).

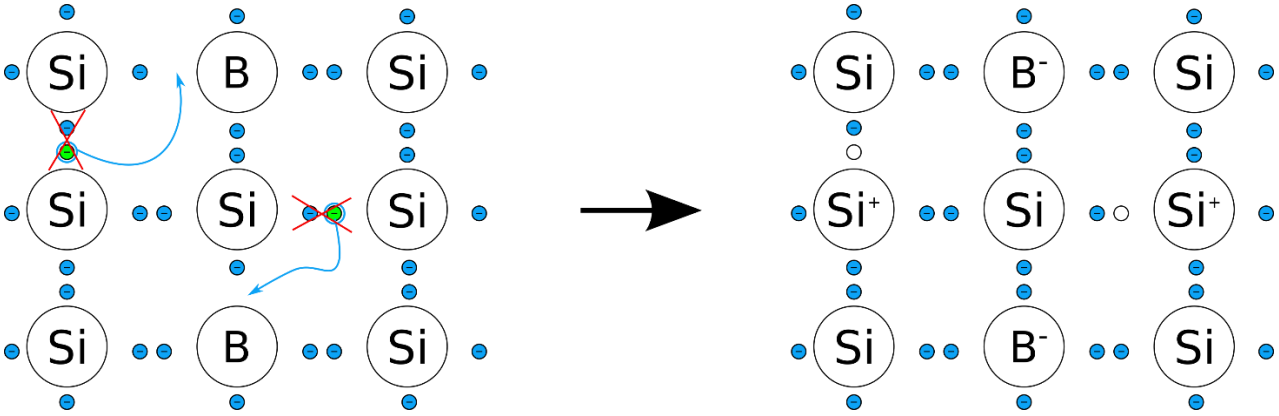

Figure 268: Illustration of hole displacement in the case of P-type doping with boron

It is important to remember that a hole is the absence of an electron, a sort of gap for a lattice Si atom. In fact, both the Si atom and the B atom have all their electrons, so there is no charge. The hole comes from a bond break that normally makes up the lattice. For this reason, these holes are only found on Si atoms in our example. Boron does not need a4th bond, so its absence is not perceived as a lack, hence the absence of a hole on boron. A hole is therefore clearly distinguishable from a positive charge.

5.1.2 Recap about Heterojunction and Metal-Semiconductor Contact

At this point, it is needed to return to the subject of heterojunctions and to few definitions, from [3,182].

- **Fermi's Energy** (E_F or level N_V): This is a function of temperature, but can be considered to be a constant equivalent to the highest energy level occupied by the electrons in the system at 0 K.

- **Vacuum Energy (**E_{vacuum} or level $\mathbf{N_V}$**)**: Potential level of energy of an electron in a vacuum near different materials. Vacuum level is the same for all materials and can therefore be used as a reference. Note that when the material contains charged zones (space charge region), they can modify the vacuum level in the vicinity) [3].

- **Work Function for the metal (**$\mathbf{\Phi_m}$**)** represents the energy required to pull an electron from the Fermi level of the semiconductor to a point located at infinity of the latter (or far enough away to avoid interaction with the semiconductor) [3].

- **Work Function for the semiconductor (**$\mathbf{\Phi_s}$**)**: represents the energy required to pull an electron from the Fermi level of the semiconductor to a point located at infinity of the latter (or far enough away to avoid interaction with the semiconductor) [3].

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- **Electron Affinity (χ)**: represents the energy required to strip an electron located at the bottom of the semiconductor conduction band to a state of rest, far away from the semiconductor [3]. $\chi = E_{vacuum} - E_C$

At thermodynamic equilibrium:

⇨ when metal and semiconductor are taken in isolation: the vacuum level is horizontal, the horizontal Fermi levels E_{FJ} (Fermi energy of the junction) in each material are distributed according to the work function of each one.

⇨ when metal and semiconductor are joined in a junction: the Fermi's level is horizontal throughout the structure, and the N_V vacuum levels are distributed according to the work function. It should be noted that in each of the materials, N_V will not necessarily be horizontal because the work function evolves according to the electronic redistribution, particularly near of the interfaces.

When a metal and a semiconductor are in contact, a barrier of potential E_b appears at the interface [182].

$$E_b = e\Phi m - e\chi$$

The band structure near the interface is thus conditioned by the value difference between metal work function Φ_m and semiconductor work function Φ_s .
As a reminder, electrons pass from one material to another if the work function of the first is less than that of the second [182].

The metal-semiconductor contacts govern the operation of the transistor, in particular through the formation of ohmic or Schottky contacts. Ohmic contacts are essential in a transistor because they allow the electric current to flow without any significant barrier between the metal and the semiconductor. This type of contact is found on the source and drain pads of the transistor, which must ensure good conduction performance at high currents. In contrast, with the difference of work function of metal and semiconductor, a Schottky contact creates a potential barrier and thus limits electrical conduction in one way. It enables the current to flow more easily in one direction (forward bias) and blocks it in the other (reverse bias). This type of contact is found in particular on the gate of a transistor [25].
The several cases will be further described, among them $\Phi_m = \Phi_s$, $\Phi_m > \Phi_s$ *or* $\Phi_m < \Phi_s$

5.1.2.1 Work functions Are Equals: $\Phi_m = \Phi_s$

At thermodynamical equilibrium, before association, $E_{Fmetal} \neq E_{Fsemiconductor}$
At thermodynamical equilibrium, after association, $E_{Fmetal} = E_{Fsemiconductor}$
When metal and semiconductor come into contact, they can exchange energy and form a single thermodynamic system.

- Here, $\Phi_m = \Phi_s$ so thermodynamic equilibrium is achieved without any exchange of electrons
- The barrier is established at the interface
- The result is a flat band system

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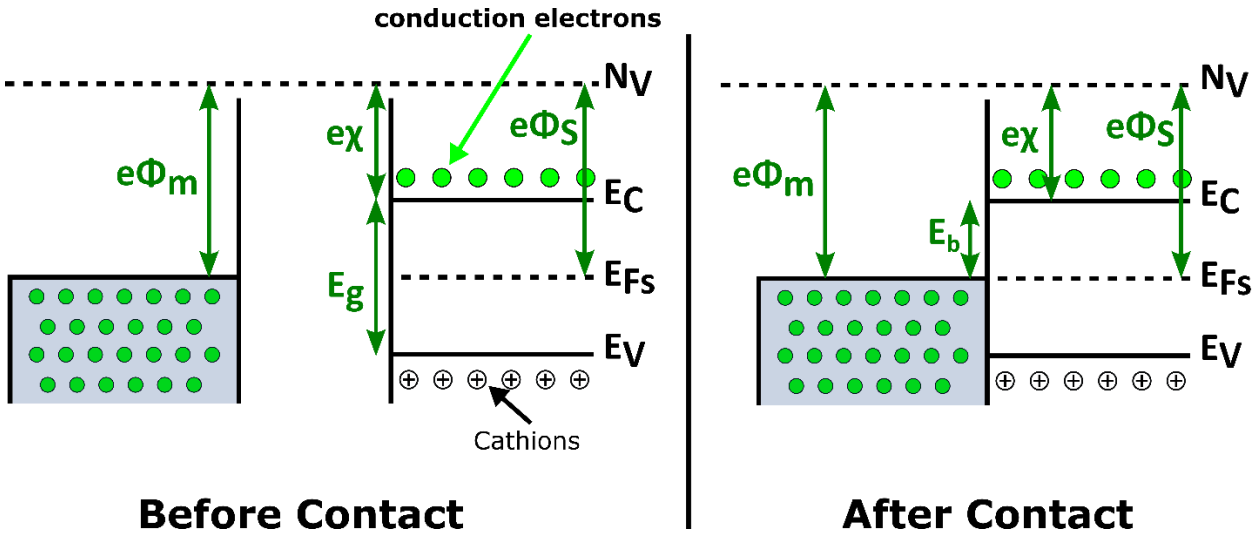

Figure 269: Illustration of energy diagrams before and after contact and equilibrium ref, for $\Phi_m = \Phi_s$

Polarisation:

If a positive voltage is applied on the metal side, the electrons are attracted to the metal. They can easily leave the conduction band and enter the metal, since $E_{F\ metal} < E_{C\ semiconductor}$
Conversely, if a positive bias is applied this time on the semiconductor side, the electrons come from the metal. However, they now face a potential barrier Eb.

5.1.2.2 Work Functions Are Not Equals: $\Phi_m > \Phi_s$

When the two materials are brought into contact with each other, according to $\Phi_m > \Phi_s$, electrons spontaneously transfer from the semiconductor to the metal. The system stabilizes in an equilibrium regime defined by the alignment of the Fermi levels.
The resulting energy diagram varies according to the doping type of semiconductor

- **Semiconductor type N:**

The electrons passing from the semiconductor to the metal cause energy changes in each of the materials.

The positive charges are the fixed charges due to the Nd+ donor ions, which obviously do not migrate. The semiconductor loses some of its free carriers (electrons), which pass into the metal and no longer compensate for the positive charges of the Nd+ donor ions.
This migration of the majority of free carriers therefore results in a depletion zone within the semiconductor and a zone of positive space charge appears. In the metal, on the other hand, a zone of electron accumulation occurs, resulting in a zone of negative space charge.

In the same way as in the PN junction, these two charged zones vary the vacuum level and create an electric field that eventually balances the diffusion forces and creates a potential barrier. The electrons that have migrated into the metal will tend to repel other electrons that also want to pass through the junction. Added to this is the attraction of the positive charges of the donor ions that have released electrons. For this reason, the bands curve upwards. This reasoning is illustrated in the following figure N° (figure with repulsion and attraction forces)

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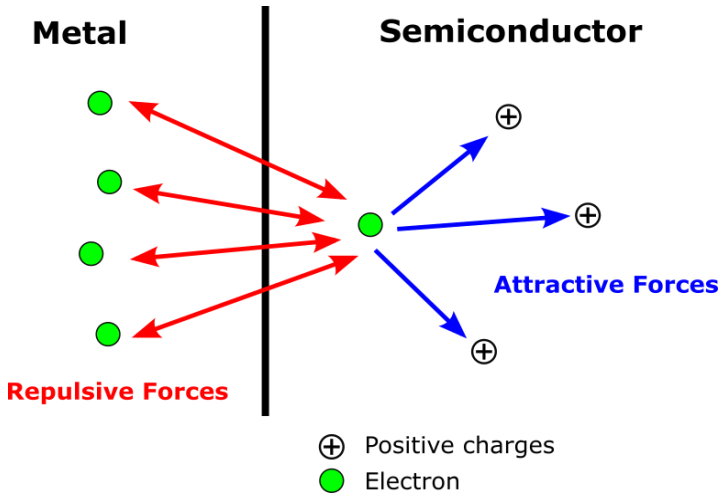

Figure 270: Illustration of the forces of attraction and repulsion involved at equilibrium ref

The diagrams above illustrate that the barrier height is different in the metal and in the semiconductor. The electrons in the semiconductor, present in the conduction band, see a lower potential barrier once they reach equilibrium ($E_b = e\Phi m - e\Phi s$) than those which are in metal ($E_b = e * \Phi m - e * \chi$). This difference is $E_c - E_F$, since E_F represents the highest energy level attainable by an electron in the metal. Electrons can therefore pass more easily from the semiconductor to the metal than vice versa.

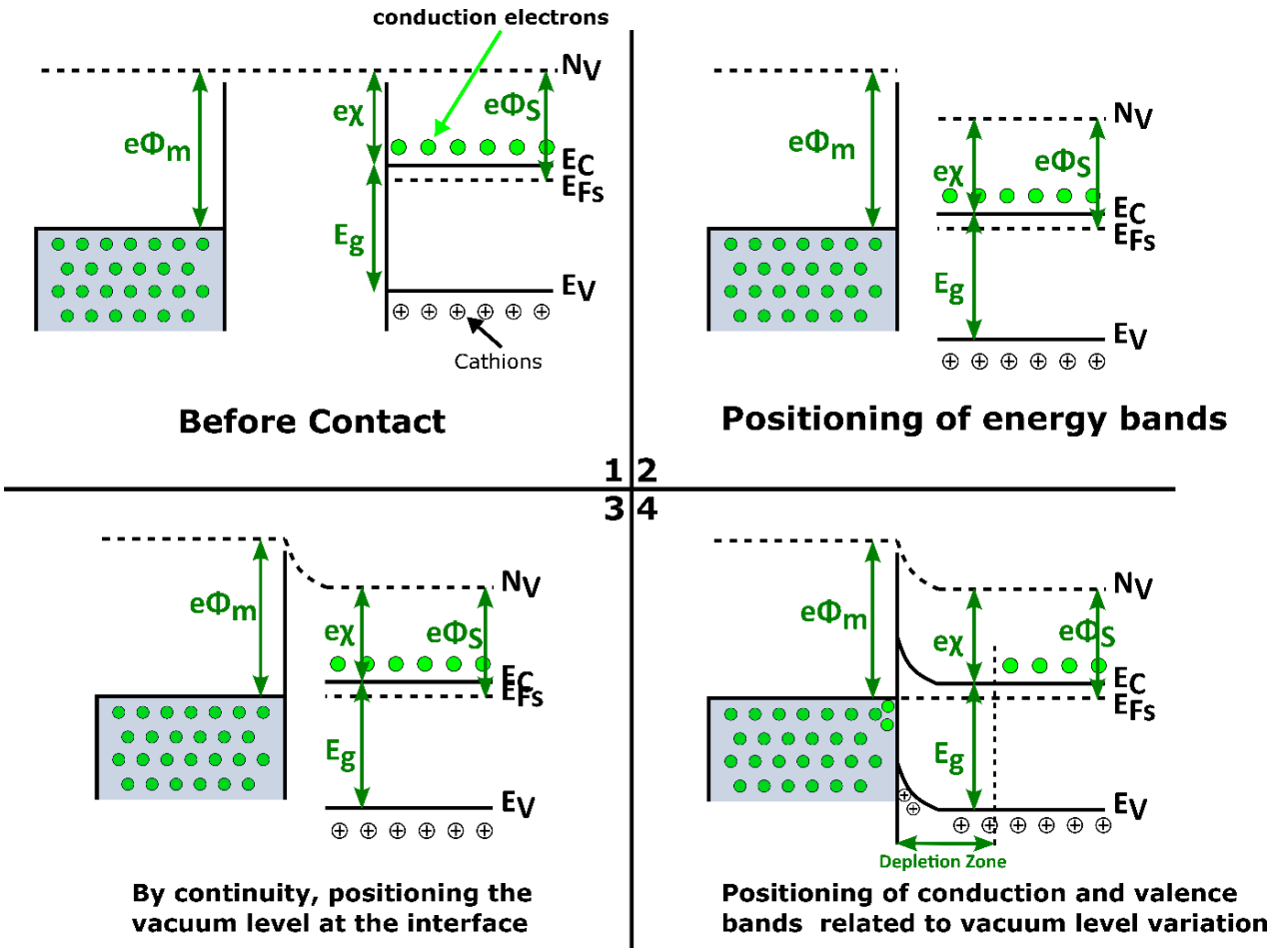

Figure 271: Illustration ref of the curvature of the energy bands in the case of an N-doped semiconductor and $\Phi_m > \Phi_s$

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Polarisation:

If a positive voltage is applied to the metal, relative to the semiconductor, the free electrons of the semiconductor are attracted to the metal. However, the electron barrier in the metal to semiconductor direction remains unchanged. The flow of electrons in the semiconductor-to-metal direction is facilitated, which is not the case for the metal-to-semiconductor direction. At the on-state it is therefore a Schottky contact.

If a negative voltage is this time applied to the metal, relative to the semiconductor, the electrons are then attracted in the opposite direction, to the back of the semiconductor, making it more difficult for the electrons to pass from the semiconductor to the metal. This helps to extend the depletion zone. Semiconductor-to-metal flow is greatly reduced, with fewer electrons diffusing than in the equilibrium state. The metal to semiconductor potential barrier remains unchanged (there is no potential drop in a metal). So, there is no metal to semiconductor flow either. As a result, there is no electron flow in either direction. It is now a blocked state.

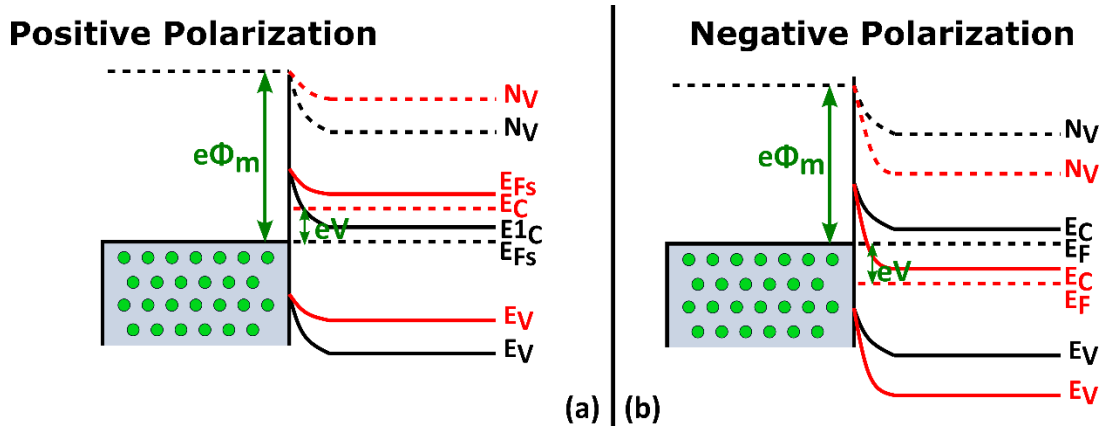

Figure 272: Energy bands changes in presence of positive (a) or negative (b) polarization for N-doped semiconductor

It can be noted that semiconductor-to-metal current can take several forms:

- Transport above the potential barrier: thermionic current (a)
- Passage through the potential barrier by quantum mechanism: tunnel current (b)
- Movement of electrons and holes within the depletion zone: recombination current (c)
- Transport of holes from the metal to the semiconductor: half-normal carrier current (d)

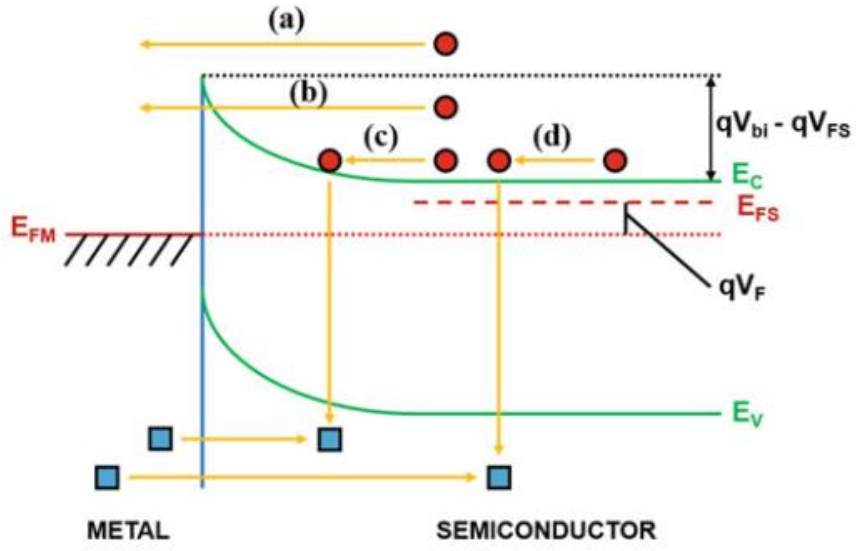

Figure 273: different types of current through heterojunction metal/semiconductor [3]

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➢ **Semiconductor type P:**

In this case, the majority carriers are now holes rather than free electrons.

When the materials are brought into contact, the free (minority) electrons from the semiconductor diffuse towards the metal and accumulate on its surface, the Fermi levels aligning.
With an N-type semiconductor, the positive charges created by the diffusion of electrons are fixed ions. With a P-type semiconductor, on the other hand, the positive charges and holes (the majority) are mobile.

The holes are attracted to the metal and accumulate on the surface of the semiconductor. For metal, the conduction electrons remain on the surface of the metal, over a small area, due to the already high proportion of conduction electrons in the metal, ($\approx 10^{22} cm^{-3}$ for metal versus a reduced density of donors or acceptors ($\approx 10^{16} cm^{-3}$-$10^{18} cm^{-3}$)). This is not the case for holes (proportion of ($\approx 10^{19} cm^{-3}$), which results in a spread of the space charge.

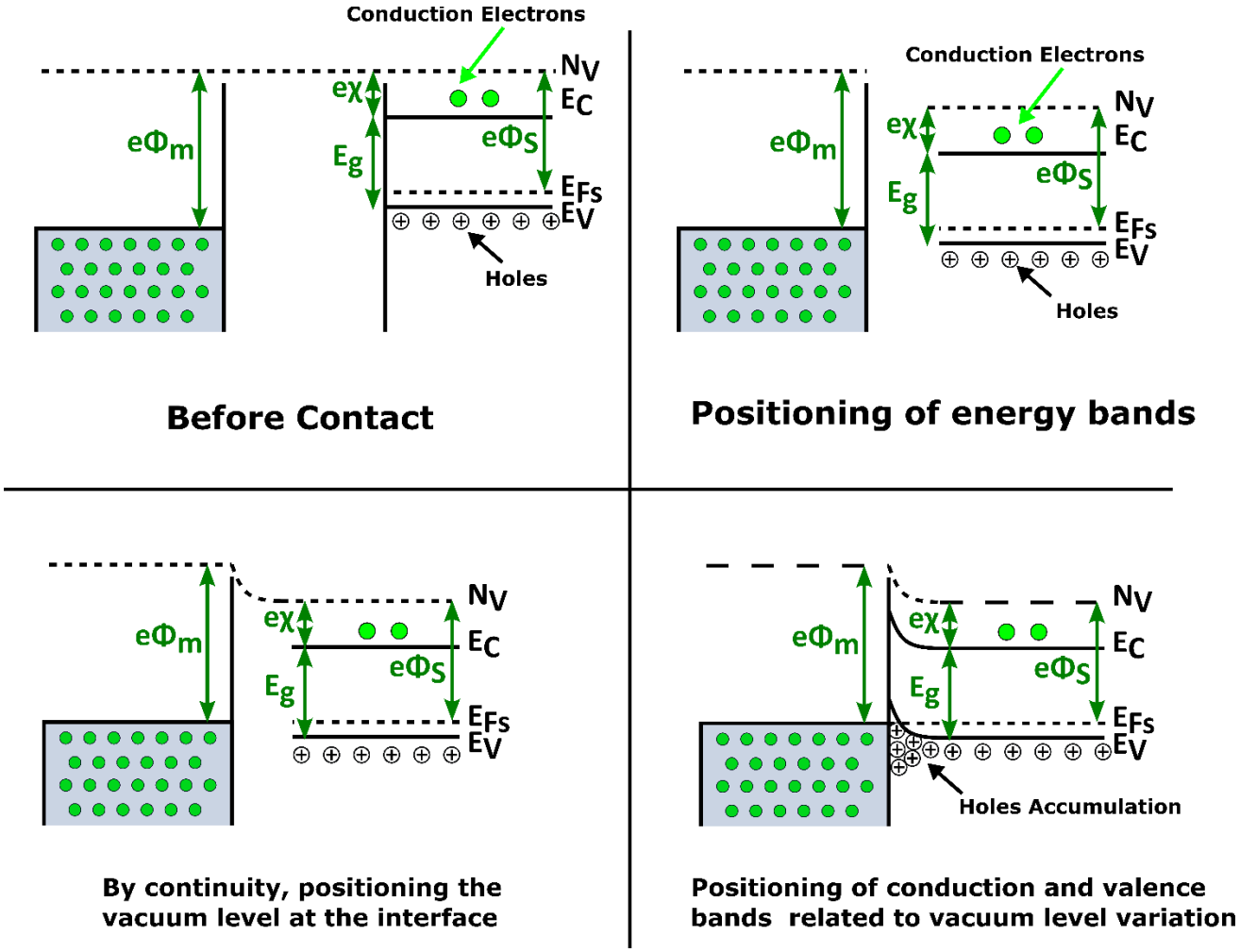

Figure 274: Energy bands changes in presence of positive (a) or negative (b) polarization for P-doped semiconductor

In the present case $\Phi_m > \Phi_s$ associated to P-type semiconductor, the main difference with the N-type lies in the fact that the majority of carriers, the holes, will constitute an accumulation regime rather than a depletion regime. There is therefore no empty insulating zone of carriers.

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At the interface, the arrival or departure of a hole in the semiconductor is immediately compensated by the arrival or departure of an electron in the metal. Regardless of the direction of polarisation, the contact is ohmic.
The energy bands change with polarisation [182]:

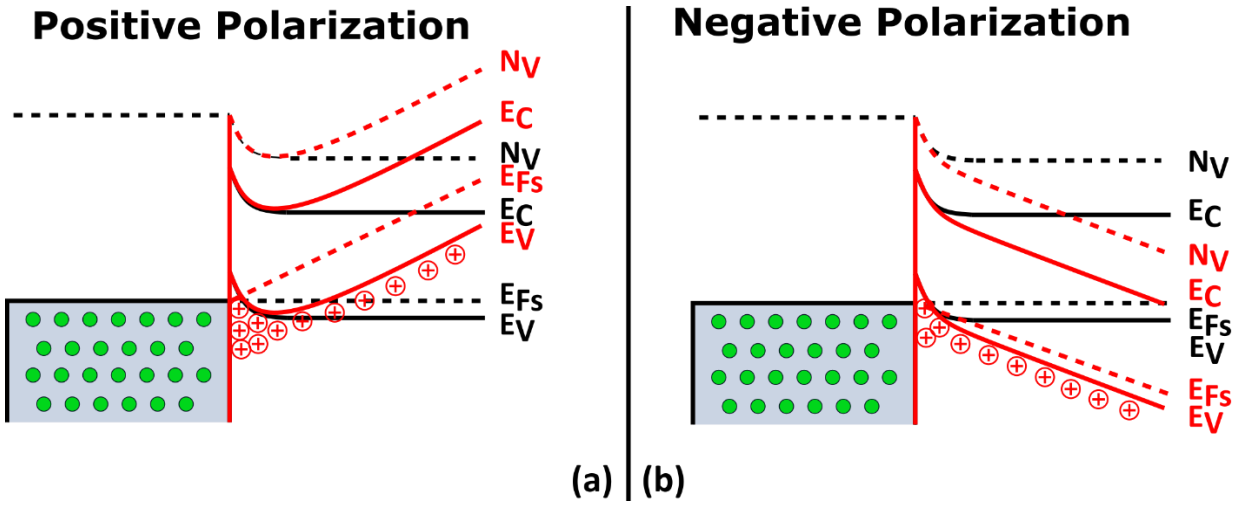

Figure 275: Energy bands changes in presence of positive (a) or negative (b) polarization for P-doped semiconductor [182]

5.1.2.3 *Work function are not equal: $\Phi_m < \Phi_s$*

The electrons now tend to leave the metal and move towards the semiconductor.
The system evolves until the fermi levels are aligned, depending on the type of semiconductor.

- **Semiconductor type N**:

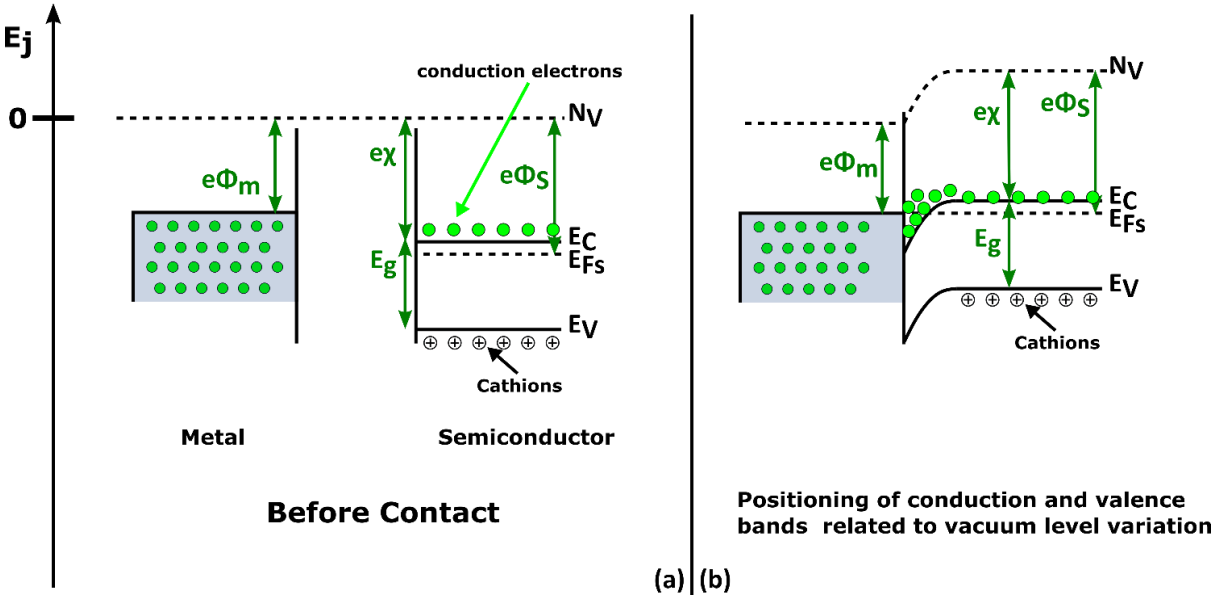

Figure 276: Illustration of the N-type metal-semiconductor system at equilibrium before contact and at equilibrium after contact

The electrons passing from the metal to the semiconductor create a localised electron deficit at the surface of the metal. In the semiconductor, on the other hand, there is a very small accumulation zone. The electrons near the surface of the semiconductor remain strongly attracted to the positive zone

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of the metal, where there is an electron deficit. This results in a downward curvature of the energy bands.

If the structure is polarised, the polarisation voltage is distributed throughout the semiconductor. Any electron arriving at the interface in the semiconductor passes freely into the metal and vice versa. The contact is ohmic.

- **Semiconductor type P**:

Electrons are transferred from the metal to the semiconductor. There is a deficit of electrons at the surface of the metal. In P-type semiconductors, it is not supposed to see a large number of free electrons appear, since these are normally the minority carriers, the majority carriers being the holes and giving the material its P-type doped character.

The metal causes a significant number of free electrons to appear in the semiconductor. These free electrons then recombine with the holes. The holes in the dopant atoms (boron, for example) are filled by an extra electron. The doping atoms therefore become negatively charged. By definition, these atoms are not mobile.

A zone of negative space charge is therefore created, along with an absence of carriers (recombined electrons and holes) This is known as the depletion zone.

The system evolves until the resulting diffusion field and voltage no longer change, stopping the diffusion of electrons.

The holes see the following potential barrier:

$$E_B = E_g + e\chi - e\Phi m$$

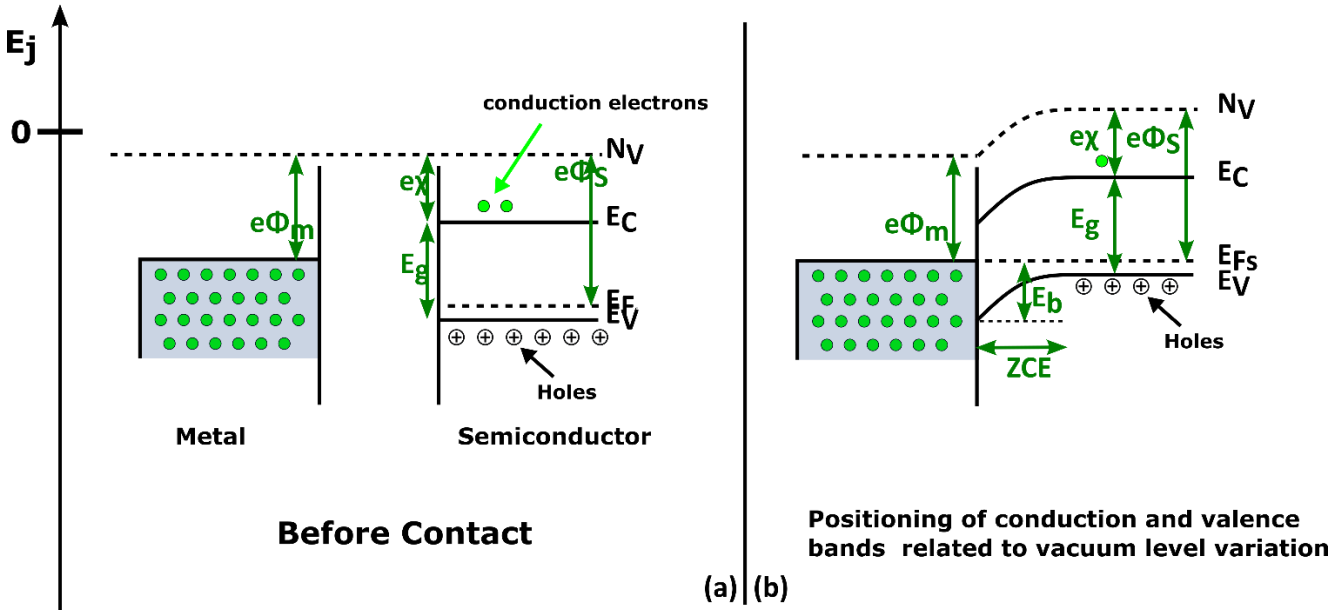

Figure 277: Illustration of the N-type metal-semiconductor system at equilibrium after contact

Polarisation:

The polarisation voltage is located in the insulating depletion zone.

If a negative voltage is applied to the semiconductor, the energy bands are raised, the electrons have even more difficulty in passing, the energy level of the holes is increased, the current does not flow and the structure is reverse biased and blocked.

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On the other hand, if a positive voltage is applied on the semiconductor side, the energy bands of the semiconductor are lowered and the potential barrier that the holes have to cross to flow is reduced, so the current flows freely. The structure is therefore polarised in the forward direction.

The P-doped metal-semiconductor structure, with $\Phi_m < \Phi_s$ is therefore a rectifier contact.

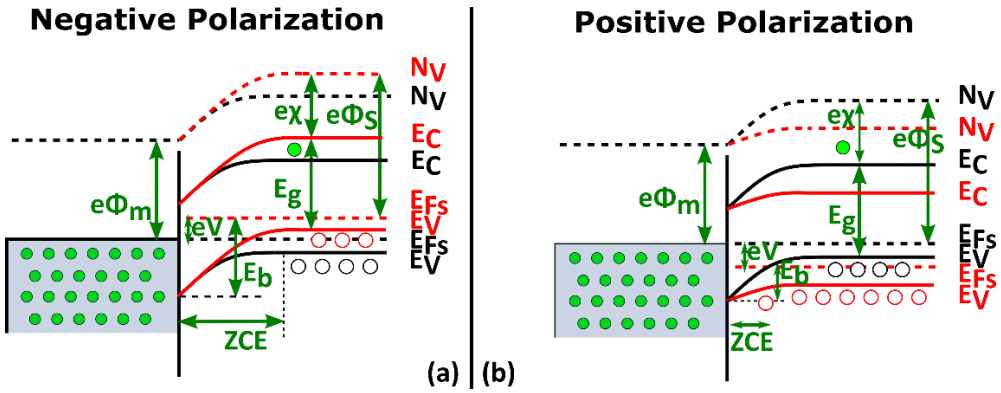

Figure 278: Impact of polarisation on the semiconductor side

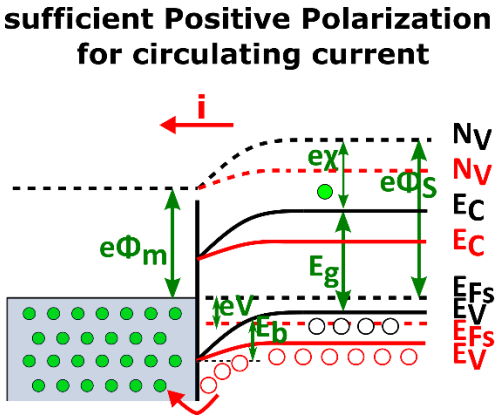

Figure 279: impact of sufficient positive polarization to enable a circulating current of holes, ref

This paragraph can be sum up as follows :

	$\Phi_m > \Phi_s$	$\Phi_m < \Phi_s$
N-Type Metal-semiconductor	Schottky contact	Ohmic contact
P-Type Metal-semiconductor	Ohmic contact	Schottky contact

Metal-semiconductor contacts have been seen. The previously seen structures were based on a difference in the doping of the same semiconductor, p-doped or n-doped. Other types of heterojunction exist with no longer with metal and semiconductor but two different types of semiconductors. The next structures (in particular HEMTs, see next chapter) are hence not only based on a difference in doping but also on a difference in gap, linked to the use of different semiconductors. For a good comprehension about the HEMT behaviour (which will be explained in b.4), the different possible cases are covered here.

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5.1.3 Heterojunction and Semiconductor-Semiconductor Contact

Heterojunction has been seen with contact between metal and semiconductor. What will be seen now is the contact between two types of semiconductors. GaN HEMT is based on a specific case among all those explained further.

5.1.3.1 $\Phi_1 > \Phi_2$

$\Phi_1 > \Phi_2$, the electrons will therefore diffuse from semiconductor 2 to semiconductor 1 and vice versa for the holes. A positive space charge will therefore appear in semiconductor 2 (electrons leaving) and a negative charge in semiconductor 1 (electrons arriving).

Depending on the type of doping, these space charges will not appear in the same way

- If semiconductor 1 is N-doped and therefore already contains free electrons, the arrival of new free electrons will correspond to an *accumulation* regime. The conduction band is already relatively full (high density of conduction electrons), so the electrons from semiconductor 2 remain localized at the interface with semiconductor 1.

- If semiconductor 1 is P-doped, the electrons recombine with the holes and a depletion zone appears. The acceptor atoms, in the case of P doping, are at a lower density ($10^{16}cm^{-3}$) than the donor atoms ($10^{18}cm^{-3}$), in the case of N doping. As a result, the depletion zone in semiconductor 1 is much larger than the space charge zone in the case of n doping (located near the interface).In semiconductor2, the space charge is positive

- If semiconductor 2 is N-doped, a depletion zone is established near the interface (free electrons are gone).

- If semiconductor 2 is P-doped, there is an accumulation zone (new holes are formed).

To separate the cases, it is needed to reasoning in terms of energy difference saying $\chi_1 > \chi_2$ means the energy of conduction band is deeper for semiconductor 1 than semiconductor 2.

It can also be said that χ_1 is further from the vacuum than χ_2. In this paragraph the parameter $\Phi_1 > \Phi_2$ is kept and the reasoning will be about χ_1, χ_2, E_{V1}, E_{V2} values variations

	Work function Φ	Electron Affinity χ	Valence Energy E_V
Sub-Case A	$\Phi_1 > \Phi_2$	$\chi_1 > \chi_2$	$E_{V1} > E_{V2}$
Sub-Case B	”	$\chi_1 > \chi_2$	$E_{V1} < E_{V2}$
Sub-Case C	”	$\chi_1 < \chi_2$	$E_{V1} < E_{V2}$
Sub-Case D	”	$\chi_1 < \chi_2$	$E_{V1} > E_{V2}$

Table 29: Different parameters Φ, χ; E_V for subcases A, B, C,D

The evolution of the energy bands is dissymmetric according to the doping level, with the greatest variation in Fermi level observed in the lowest doped semiconductor.
In this paragraph, for reasons of simplicity, it is assumed that the doping of the respective semiconductors is equivalent. The reasoning is identical with a variation in doping.

Energy levels in black are the levels before equilibrium, those in red after. In green are represented the characteristics of each semiconductor 1 or 2. Blue arrows represent the energy variation of each semiconductor

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Sub-Case A: $\Phi_1 > \Phi_2$, $\chi_1 > \chi_2$, $E_{V1} > E_{V2}$

Electrons flow from semiconductor 2 to semiconductor 1, a depletion zone is created in semiconductor 2, equivalent to a potential barrier.
The electrons arriving in semiconductor 1 remain localized, they do not diffuse through the whole semiconductor because the conduction band is already heavily filled. This is consistent with the potential well observed graphically[182].

Sub-Case_B: $\Phi_1 > \Phi_2$, $\chi_1 > \chi_2$, $E_{V1} < E_{V2}$

In terms of electron flow, the structure of the conduction bands is unchanged from sub-case A. The same effects are therefore seen. However, the valence band changes. The passage of holes from semiconductors 1 to 2 is therefore facilitated [182].

Sub-Case_C: $\Phi_1 > \Phi_2$, $\chi_1 < \chi_2$, $E_{V1} < E_{V2}$

The electrons diffuse from semiconductor 2 to semiconductor 1, but they now encounter a P-doped semiconductor 1 and not an N-doped semiconductor 1 as before. (reminder: in case of a n-doped semiconductor, the Fermi's level is close to the conduction band. In case of a p-doped semiconductor, the Fermi's level is close to the valence band) The electrons recombine with the holes and a depletion zone is created, in line with the potential barrier that can now be observed graphically.
The circulation of holes remains unchanged compared with case B [182].

Sub-Case_D: $\Phi_1 > \Phi_2$, $\chi_1 < \chi_2$, $E_{V1} > E_{V2}$

In terms of electron flow, the situation is similar to sub-case C. However, there is a difference in terms of hole flow. The curvature of the energy bands creates a potential well on semiconductor side 1. The holes are then confined in this well, allowing the formation of a "gas of holes" with certain specific properties, in particular increased mobility [182]. This well formation will be discussed in the chapter on the HEMT transistor, particularly in the case of the formation of a gas of electrons.

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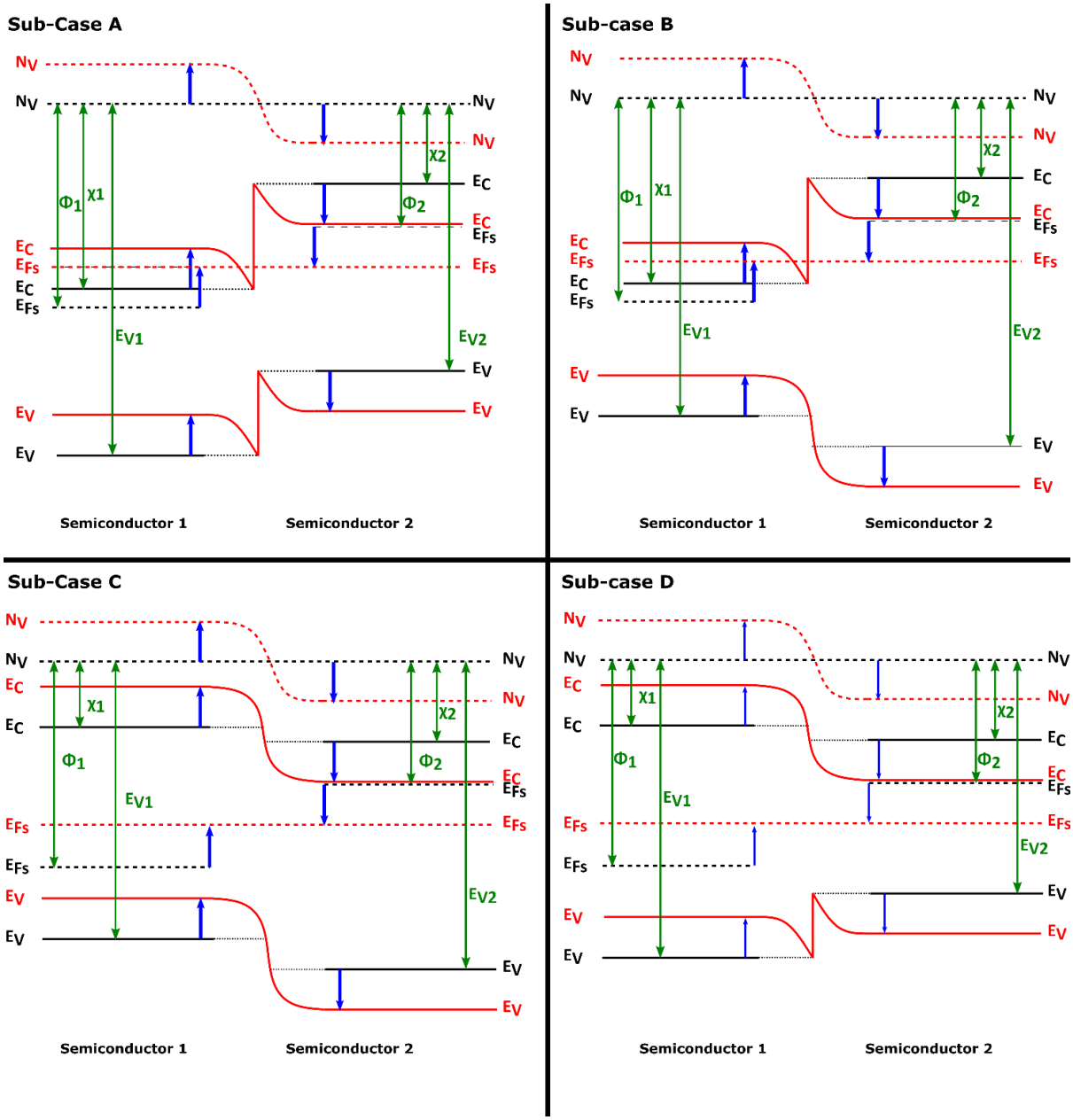

Figure 280: Illustration of the curvature of the energy bands in several sub-cases A,B,C,D

5.1.3.2 $\Phi_1 < \Phi_2$

The case $\Phi_1 < \Phi_2$ represents the same types except that they are reversed compared to the case $\Phi_1 > \Phi_2$. They are therefore not detailed further here.

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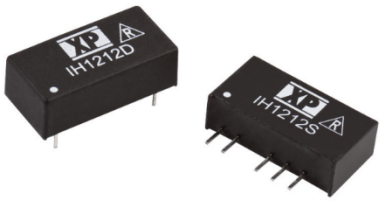
5.2 Appendix 2: Datasheets of DC / DC Converters

2 Watts
IH Series

xppower.com



- Dual Output
- SIP or DIP Package
- 1000 VDC Isolation
- Optional 3000–6000 VDC Isolation
- MTBF >1.1 MHrs
- –40 °C to +85 °C Operation
- 3 Year Warranty

Specification

Input

Input Voltage Range	• Nominal ±10%
Input Reflected Ripple Current	• 20 mA pk-pk through 12 µH inductor, 5Hz to 20 MHz
Input Reverse Voltage Protection	• None
Input Filter	• Capacitor

Output

Output Voltage	• See table
Minimum Load	• None[3]
Line Regulation	• 1.2%/1% Δ Vin
Load Regulation	• ±10% 20-100% load change (3.3 V models ±20%)
Setpoint Accuracy	• ±3%
Ripple & Noise	• 75 mV pk-pk max, 20 MHz bandwidth
Temperature Coefficient	• 0.02%/°C
Maximum Capacitive Load	• ±220 µF
Cross Regulation	• 3.3 V and 5 V: ±8%, all others: ±5%[4]

General

Efficiency	• See table
Isolation Voltage	• 1000 VDC[2]
Isolation Resistance	• 10^9 Ω
Isolation Capacitance	• 60 pF typical
MTBF	• >1.1 MHrs to MIL-HDBK-217F at 25 °C, GB

Environmental

Operating Temperature	• -40 °C to +85 °C
Storage Temperature	• -40 °C to +125 °C
Case Temperature	• 100 °C max
Cooling	• Convection-cooled

Notes

1. For DIP package, replace 'S' with 'D' in model number.
2. Add suffix 'H' to model number for 3000 VDC isolation. For higher VDC isolation, add suffix 'Hx' to model number where x=4 for 4000 VDC isolation, x=5 for 5200 VDC isolation and x=6 for 6000 VDC isolation.
3. Operation at no load will not damage unit but it may not meet all specifications.
4. When one output is set to 100% load and the other varies between 25%-100% load.
5. All dimensions in inches (mm).
6. Pin pitch tolerance: ±0.014 (±0.35)
7. Case tolerance: ±0.02 (±0.5)
8. Weight: SIP 0.004 lbs (2.2 g), DIP 0.005 lbs (2.4 g)

Input Voltage	No Load Input Current	Output Voltage	Output Current	Efficiency	Model Number[1,2]
5 VDC	30 mA	±3.3 V	±200 mA	65%	IH0503S
	30 mA	±5.0 V	±200 mA	72%	IH0505S
	30 mA	±9.0 V	±111 mA	77%	IH0509S
	30 mA	±12.0 V	±84 mA	78%	IH0512S
	30 mA	±15.0 V	±66 mA	80%	IH0515S
	30 mA	±24.0 V	±42 mA	80%	IH0524S
12 VDC	20 mA	±3.3 V	±200 mA	67%	IH1203S
	20 mA	±5.0 V	±200 mA	75%	IH1205S
	20 mA	±9.0 V	±111 mA	77%	IH1209S
	20 mA	±12.0 V	±84 mA	82%	IH1212S
	20 mA	±15.0 V	±66 mA	82%	IH1215S
	20 mA	±24.0 V	±42 mA	82%	IH1224S
24 VDC	10 mA	±3.3 V	±200 mA	68%	IH2403S
	10 mA	±5.0 V	±200 mA	75%	IH2405S
	10 mA	±9.0 V	±111 mA	80%	IH2409S
	10 mA	±12.0 V	±84 mA	82%	IH2412S
	10 mA	±15.0 V	±66 mA	82%	IH2415S
	10 mA	±24.0 V	±42 mA	82%	IH2424S
48 VDC	6 mA	±3.3 V	±200 mA	60%	IH4803S
	6 mA	±5.0 V	±200 mA	73%	IH4805S
	6 mA	±9.0 V	±111 mA	77%	IH4809S
	6 mA	±12.0 V	±84 mA	80%	IH4812S
	6 mA	±15.0 V	±66 mA	80%	IH4815S
	6 mA	±24.0 V	±42 mA	80%	IH4824S

Mechanical Details

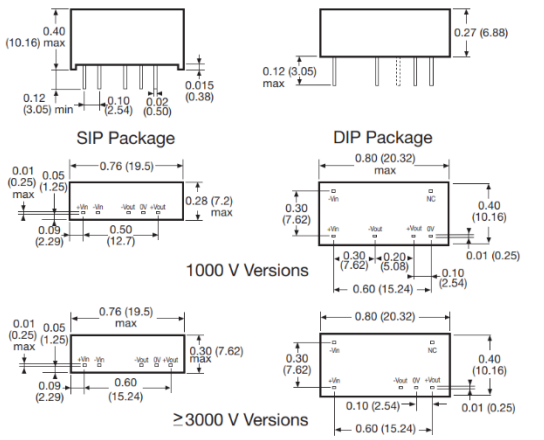


Figure 281:datasheet of DC / DC converters initially used

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Murata Power Solutions

MGJ2B Series

5.4kVDC Isolated 2W Gate Drive DC-DC Converters

FEATURES

- Optimised bipolar output voltages for IGBT/SiC & Mosfet gate drives
- Reinforced insulation to UL62368-1 recognised
- ANSI/AAMI ES60601-1, 1 MOPP/2 MOOP's recognition pending
- 5.4kVDC isolation test voltage 'Hi Pot Test'
- Ultra low isolation capacitance
- SIP package style
- 5V, 12V, 15V & 24V inputs
- +15V/-3V, +15V/-5V, +15V/-8.7V, +15V/-15V, +17V/-9V, +18V/-2.5V, +18V/-5V[3], +20V/-3.5V & +20V/-5V outputs
- Operation to 105°C
- Characterised CMTI >200kV/µS
- Continuous barrier withstand voltage 2.4kVDC
- Characterised partial discharge performance

PRODUCT OVERVIEW

The MGJ2B series of DC-DC converters is ideal for powering 'high side' and 'low side' gate drive circuits for IGBT/SiC and Mosfet gate drives in bridge circuits.
A choice of asymmetric output voltages allows optimum drive levels for best system efficiency and EMI. The MGJ2B series is characterised for high isolation and dv/dt requirements commonly seen in bridge circuits used in motor drives and inverters, while the MGJ2B extended temperature range and construction gives long service life and reliability.

SELECTION GUIDE

Order Code	Nominal Input Voltage	Output Voltage 1	Output Voltage 2	Output Current 1	Output Current 2	Input Current at Rated Load	Load Regulation (Typ)	Load Regulation (Max)	Ripple & Noise (Typ)[2]	Ripple & Noise (Max)[2]	Efficiency (Min)	Efficiency (Typ)	Isolation Capacitance	MTTF[1] MIL.	MTTF[1] Tel.
	V	V	V	mA			%		mVp-p		%		pF	kHrs	
MGJ2D051505BSC	5	15	-5	80	40	360	5.7	7	30	50	71	76	3	3136	95134
MGJ2D051509BSC	5	15	-8.7	80	40	390	6	7	30	50	73	77.5	3	2947	86077
MGJ2D051515BSC	5	15	-15	67	67	492	7	8.5	20	35	74	78	3	2164	84961
MGJ2D051802BSC	5	18	-2.5	80	80	410	9	12	20	50	70	75	3	2502	84300
MGJ2D052003BSC	5	20	-3.5	80	80	470	8	11	20	50	72	77	3	2500	86317
MGJ2D052005BSC	5	20	-5	80	40	440	6.2	8	30	50	74	78.5	3	2502	83736
MGJ2D121503BSC	12	15	-3	95	95	170	8	10	25	50	76	80	3	2933	96712
MGJ2D121505BSC	12	15	-5	80	40	150	4.7	6	30	50	75	80	3	3093	105983
MGJ2D121509BSC	12	15	-8.7	80	40	155	5.3	7.5	30	50	76	80	3	2760	95198
MGJ2D121515BSC	12	15	-15	67	67	203	6.0	8	24	40	78	82	3	2194	96436
MGJ2D121802BSC	12	18	-2.5	80	80	170	8	11	20	50	74	80	3	2175	85409
MGJ2D121805BSC[3]	12	18	-5	80	40	170	5.2	8	20	50	74	81	3		
MGJ2D122003BSC	12	20	-3.5	80	80	190	7	10	20	50	77	82	3	2373	89831
MGJ2D122005BSC	12	20	-5	80	40	195	5.5	8	30	45	78	82	3	2417	93548
MGJ2D151505BSC	15	15	-5	80	40	120	5	7	30	50	75	80	3	2735	90911
MGJ2D151509BSC	15	15	-8.7	80	40	130	5	7	30	50	76	80	3	2769	81620
MGJ2D151515BSC	15	15	-15	67	67	167	5.5	8	23	35	75	79	3	2459	91193
MGJ2D151802BSC	15	18	-2.5	80	80	130	8	11	20	50	73	79	3	2217	77469
MGJ2D152003BSC	15	20	-3.5	80	80	150	7	10	20	50	76	81	3	2379	84696
MGJ2D152005BSC	15	20	-5	80	40	145	6	8	30	50	78	81	3	2052	75638
MGJ2D241503BSC	24	15	-3	95	95	90	8	10	25	50	76	80	4	2629	73130
MGJ2D241505BSC	24	15	-5	80	40	75	4.6	7	30	50	74	80.5	4	2730	64179
MGJ2D241509BSC	24	15	-8.7	80	40	80	4.8	7	30	50	77	82	4	2896	77980
MGJ2D241709BSC	24	17	-9	80	80	105	6	8	30	50	78	83	4	2580	62586
MGJ2D241802BSC	24	18	-2.5	80	80	90	8	11	20	50	74	80	4	2674	75178
MGJ2D242003BSC	24	20	-3.5	80	80	90	7	10	20	50	76	82	4	2256	67350
MGJ2D242005BSC	24	20	-5	80	40	90	6	8	30	50	78	82	4	2227	68908

INPUT CHARACTERISTICS

Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage range	Continuous operation, 5V input types	4.5	5	5.5	V
	Continuous operation, 12V input types	10.8	12	13.2	
	Continuous operation, 15V input types	13.5	15	16.5	
	Continuous operation, 24V input types	21.6	24	26.4	
Input reflected ripple	051505, 051509, 051515, 052003 & 052005 types		40		mA
	121503, 121505, 121509, 121515, 122005, 151505, 151509, 151515 & 152005 types		20		
	051802, 241505, 241509, 241709 & 242005 types		15		
	122003, 121802, 121805, 151802, 152003, 241503, 241802 & 242003 types		10		

Figure 282: datasheet of DC / DC converters used for the 2024 version of driver power supply board

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5.3 Appendix 3: Datasheets of Drivers

UCC2753x 2.5-A and 5-A, 35-V_{MAX} VDD FET and IGBT Single-Gate Driver

1 Features

- Low-cost gate driver (offering optimal solution for driving FET and IGBTs)
- Superior replacement to discrete transistor pair drive (providing easy interface with controller)
- TTL and CMOS compatible input logic threshold (independent of supply voltage)
- Split output options allow for tuning of turnon and turnoff currents
- Inverting and noninverting input configurations
- Enable with fixed TTL compatible threshold
- High 2.5-A source and 2.5-A or 5-A sink peak drive currents at 18-V VDD
- Wide VDD range from 10 V to 35 V
- Input and enable pins capable of with standing up to –5-V DC below ground
- Output held low when inputs are floating or during VDD UVLO
- Fast propagation delays (17-ns Typical)
- Fast rise and fall times (15-ns and 7-ns typical with 1800-pF Load)
- Undervoltage lockout (UVLO)
- Used as a high-side or low-side driver (if designed with proper bias and signal isolation)
- Low-cost, space-saving 5-pin or 6-pin DBV (SOT-23) package options
- UCC27536 and UCC27537 pin-to-pin compatible to TPS2828 and TPS2829
- Operating temperature range of –40°C to 140°C

2 Applications

- Switched-mode power supplies
- DC-to-DC converters
- Solar inverters, motor control, UPS
- HEV and EV chargers
- Home appliances
- Renewable energy power conversion
- SiC FET converters

3 Description

The UCC2753x single-channel, high-speed gate drivers can effectively drive MOSFET and IGBT power switches. Using a design that allows for a source of up to 2.5 A and 5-A sink through asymmetrical drive (split outputs), coupled with the ability to support a negative turn-off bias, rail-to-rail drive capability, extremely small propagation delay (17 ns typical), the UCC2753x devices are ideal solutions for MOSFET and IGBT power switches. The UCC2753x family of devices can also support enable, dual input, and inverting and non-inverting input functionality. The split outputs and strong asymmetrical drive boost the devices immunity against parasitic Miller turn-on effect and can help reduce ground debouncing.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC27531	SOIC (8)	4.90 mm × 3.91 mm
UCC27531	SOT-23 (6)	2.90 mm × 1.60 mm
UCC27533	SOT-23 (5)	2.90 mm × 1.60 mm
UCC27536	SOT-23 (5)	2.90 mm × 1.60 mm
UCC27537	SOT-23 (5)	2.90 mm × 1.60 mm
UCC27538	SOT-23 (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Driving IGBT Without Negative Bias

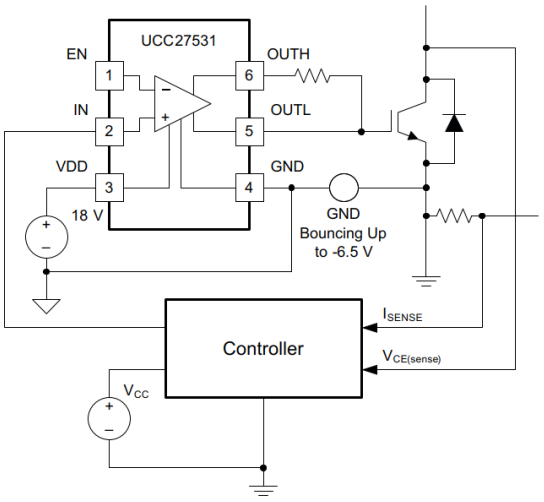

Figure 283: datasheet of driver initially used (2023 version)

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage 36V
Input Voltage (**Note 1**)..... V_{DD} + 0.3V to GND
Package Power Dissipation ($T_A \leq 70°C$)
PDIP ..... 730 mW
CERDIP ..... 800 mW
SOIC ..... 470 mW
Maximum Junction Temperature, T_J ..... +150°C
Storage Temperature Range ..... -65°C to +150°C

† Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25°C with 4.5V $\leq V_{DD} \leq$ 30V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current (**Note 1**)	I_{IN}	-1	—	1	µA	$0V \leq V_{IN} \leq 12V$
Output						
High Output Voltage	V_{OH}	V_{DD} – 1.0	V_{DD} – 0.8	—	V	I_{OUT} = 100 mA
Low Output Voltage	V_{OL}	—	—	0.025	V	
Output Resistance	R_O	—	7	10	Ω	I_{OUT} = 10 mA, V_{DD} = 30V
Peak Output Current	I_{PK}	— —	3.0 1.5	— —	A	Source: V_{DD} = 30V Sink: V_{DD} = 30V
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	0.3	—	A	Duty cycle ≤ 2%, t ≤ 300 µsec
Switching Time (Note 2)						
Rise Time	t_R	—	25	40	ns	**Figure 4-1**
Fall Time	t_F	—	33	50	ns	**Figure 4-1**
Delay Time	t_{D1}	—	62	80	ns	**Figure 4-1**
Delay Time	t_{D2}	—	78	90	ns	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	— —	2.5 0.3	4 0.4	mA	V_{IN} = 3V V_{IN} = 0V
Start-up Threshold	V_S	—	8.4	10	V	
Drop-out Threshold	V_{DO}	7	7.7	—	V	**Note 3**

Note 1: For inputs >12V, add a 1 kΩ resistor in series with the input. See **Section 2.0 "Typical Performance Curves"** for input current graph.

2: Switching times are ensured by design.

3: For operation below 7V, pin 3 ($\overline{\text{LOCK DIS}}$) should be tied to ground to disable the lockout and start-up circuit, otherwise, pin 3 **must** be left floating.

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5.4 Appendix 4: I²t Fuse Curve

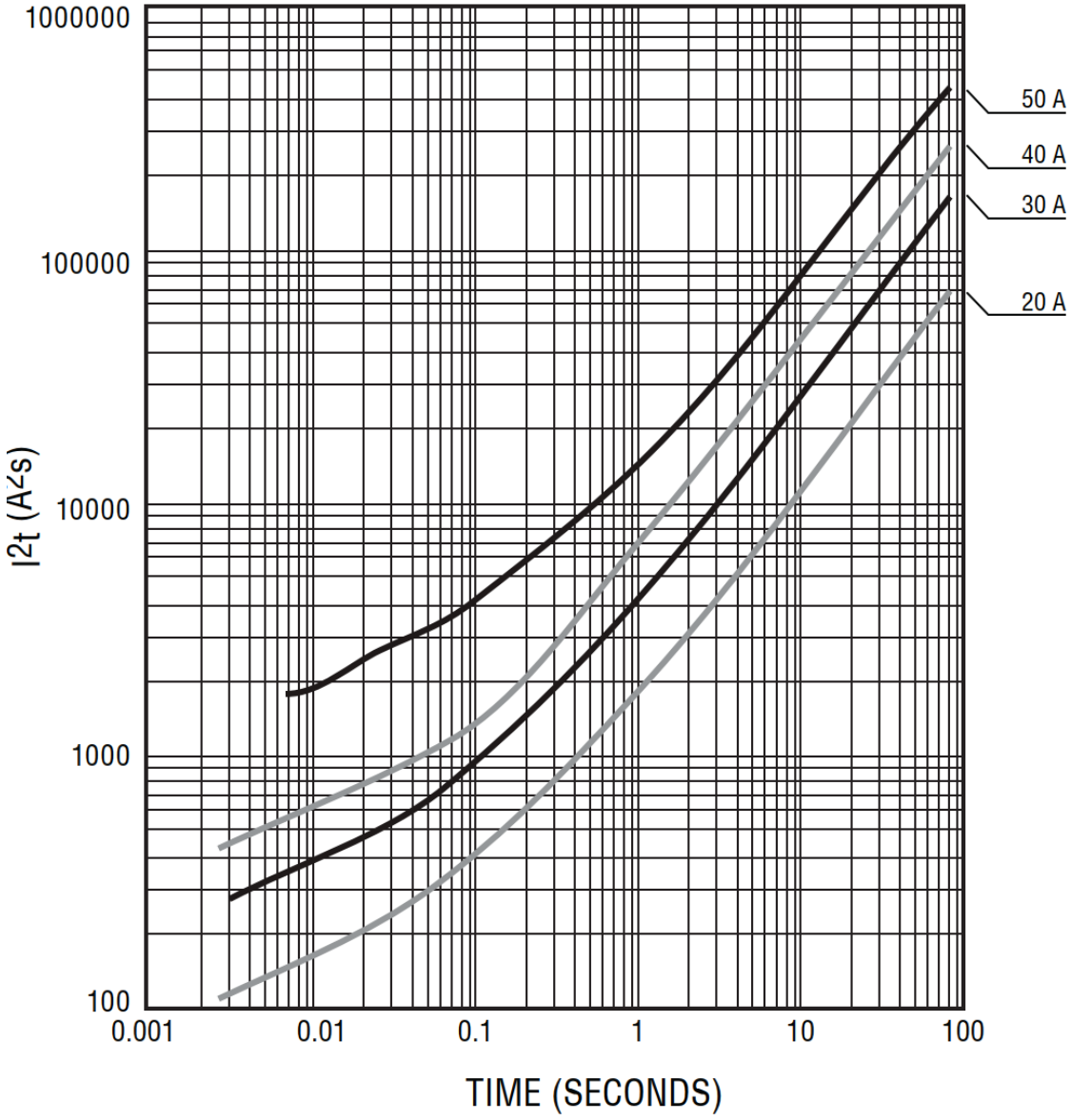

Figure 284: I²t Curve for the fuse reference SF-2923HC20C-2

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6

Résumé étendu (français)

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En 1890 la guerre des courants de Georges Westinghouse et Thomas Edison avait finalement privilégié le courant alternatif (AC), au détriment du courant continu (DC). Le réseau électrique a dès lors été construit en conséquence avec aujourd'hui près de 1.6 millions de kilomètres de lignes électriques [184] et une hiérarchisation de cet acheminement en courant alternatif . On retrouve les réseaux d'interconnexion à très haute tension, appelés autoroutes énergétiques, entre les pays ou pour de longues distances, assurant le transport de l'énergie depuis les sites de production. Leur tension est de 225kV voire 400 kV avec des pertes réduites. Au niveau régional et pour des tensions de 225 kV, 90 kV et 63 kV, on retrouve les lignes haute tension du réseau de transport. Ce type de réseaux assure également la fourniture énergétique des gros sites industriels. Enfin pour des tensions allant de 20 kV (moyennes et petites entreprises) jusque 400 V (application domestique), on retrouve le réseau de distribution [1]

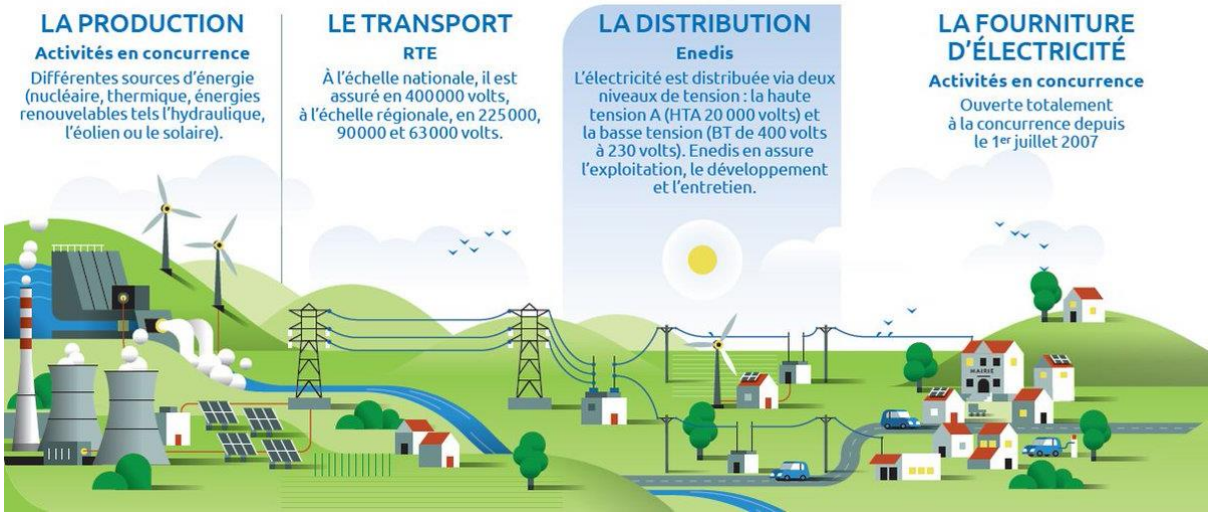

Figure 285: les réseaux de transport et de distribution de l'électricité, de [184]

L'apparition de moyens de production d'énergie renouvelables décentralisée tels que l'éolien on-shore ou off-shore ainsi que les panneaux photovoltaïques vient renverser le précédent schéma de production, acheminement et consommation de l'énergie électrique. De plus la demande mondiale d'électricité n'a fait que croitre et il n'est pas prévu qu'elle diminue durant les prochaines décennies. De 1990 à nos jours [10] a relevé une augmentation de 150% de la consommation.
Cette accélération s'explique en partie par l'essor de nouvelles technologies telles que les smartphones et les ordinateurs ou plus récemment des véhicules électriques et leurs chargeurs rapides, fonctionnant en courant continu.

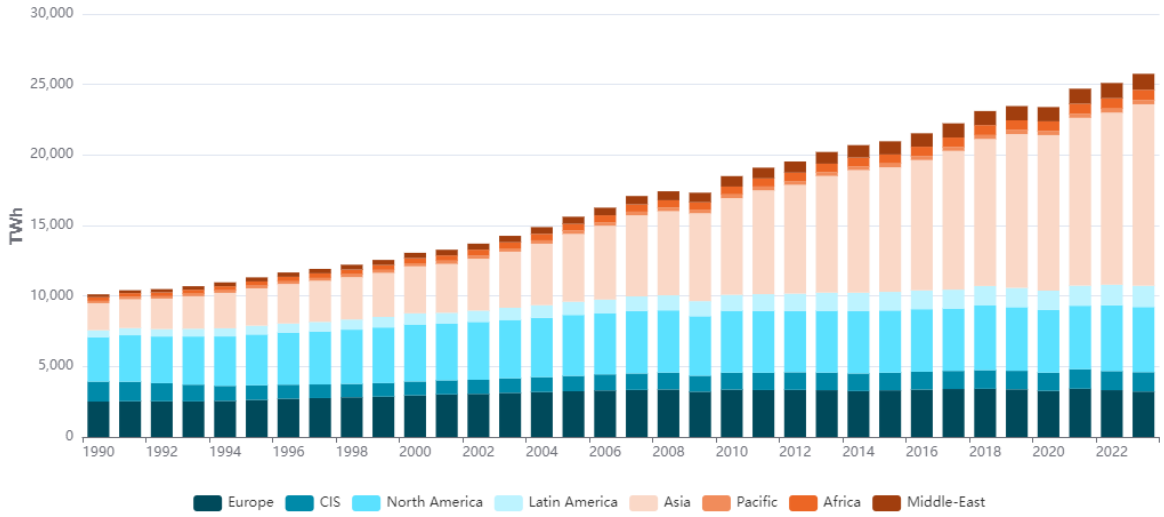

Figure 286: illustration de la demande croissante d'électricité, de [10]

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Ces nouveaux modes de consommation et de production redéfinissent nos schémas actuels et rendent particulièrement pertinent l'usage de réseaux DC et indispensable l'usage de l'électronique de puissance au moyen notamment des convertisseurs de puissance.Pour cela, l'industrie de l'électronique de puissance a développé des convertisseurs fiables à base de silicium. Pour autant, après des dizaines d'années d'optimisation et d'améliorations des performances, ce type de convertisseurs apparait dépassé au regard des nouveaux besoins énergétiques. Pour pallier cela, deux nouveaux matériaux ont été développés. Avec des pertes réduites, des calibres en courant et tensions plus élevées et une fréquence de commutation augmentée, les matériaux grand-gap tels que le nitrure de gallium (GaN) et le carbure de silicium (SiC) sont étudiés et représentent une solution pour répondre à ces nouveaux besoins.

Particulièrement apprécié dans le domaine RF avec une fréquence de commutation jusqu'à plusieurs dizaines de MHz [12–14], les transistors GaN sont actuellement étudiés en tant que composants de puissance pour des tension jusque 650 V, tandis que le SiC est plutôt réservé pour les applications au-delà de 1200 V. Pour rappel, les MOSFET en silicium ne peuvent excéder une fréquence de commutation de l'ordre de plusieurs centaines de MHz.

Cependant, les dispositifs de puissance à base de GaN doivent être améliorés, en particulier dans le domaine de la robustesse où les mécanismes de dégradations et de défaillance ne sont pas bien compris. Leur commercialisation à grande échelle passe nécessairement par une amélioration de cette fiabilité, indispensable pour les secteurs automobile et aéronautique.

Avec la présence concomitante de forts courants et tensions, les courts-circuits représentent l'un des événements les plus indésirables pour le composant semi-conducteur en raison de la quantité importante d'énergie à dissiper [21,22].

Cette thèse se concentre sur l'impact des courts-circuits sur les transistors GaN 650 V. Le chapitre 1 fournit les connaissances de base sur les semi-conducteurs afin de mieux comprendre les propriétés spécifiques du transistor GaN. Une attention particulière a été portée sur la compréhension des mécanismes physiques inhérents au fonctionnement des transistors GaN et notamment la formation du gaz d'électrons appelé 2DEG.Le chapitre 1 traite ensuite de l'état de l'art en matière de court-circuit pour les composants de puissance GaN. La littérature reste très lacunaire. Les mécanismes de fonctionnement et de casse en court-circuit sont globalement peu compris et les auteurs des papiers scientifiques se contredisent les uns avec les autres. Trois types de mécanismes de défaillance ont été identifiés. Leurs forces mais aussi leurs faiblesses ont été discutés dans ce chapitre afin de mieux préparer l'étude de la dégradation des transistors GaN en court-circuit.

Une approche innovante a été décidée et décrite dans le chapitre 2. En effet, la littérature s'appuie aujourd'hui sur des essais destructifs, avec l'inconvénient majeur que les puces sont difficiles à analyser une fois détruite, d'autant plus si l'on considère la puissance colossale à dissiper lors du court-circuit. A contre-courant de cela, il a été décidé de travailler sur des essais répétitifs et non-destructifs. L'analyse de composants de type normally-on est inexistante. Ils y sont étudiés dans cette thèse en complément des composants normally-off de type p-GaN provenant de deux fournisseurs distincts. Entre chaque série de court-circuit, le composant est caractérisé au moyen d'un traceur de caractéristiques de type B1505A et l'évolution des paramètres statiques du transistor tels que la tension de seuil V_{th} ou la résistance à l'état passant R_{DS_ON} sont analysés.

L'impressionnante vitesse de commutation des composants GaN a pour conséquence d'exacerber le moindre effet parasite. Plusieurs phases d'optimisation du banc expérimental de court-circuit ont donc été réalisées et sont décrites dans le chapitre 2. En parallèle de cela, une simulation SPICE a été développée afin de mieux comprendre le fonctionnement du banc expérimental. Ces analyses ont donné lieu à différentes améliorations et versions du banc de court-circuit, résumées de façon succincte dans le tableau 1 et détaillées dans le chapitre 2.

Le chapitre 3 s'intéresse dans un premier temps aux résultats des composants normally-on en matière de comportement, observations dynamiques et dégradations suite à l'application de courts-circuits répétitifs. La seconde partie du chapitre 3 traite des composants normally-off, aux comportements et à la robustesse en court-circuit bien distincts. Différentes variations et types de casses sont observés. En fin de chapitre, des éléments de réponse sont donnés quant à la robustesse accrue des composants du premier fournisseur.

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6.1 Chapitre 1: la technologie des transistors GaN et état de l'art en matière de court-circuit

6.1.1 Le matériau GaN

Le nitrure de gallium est un matériau semi-conducteurs composés d'éléments de la colonne III du tableau périodique des éléments (Gallium Ga, Aluminium Al, Indium In) associés à l'élément azote (N) de la colonne V. Ces matériaux, GaN, AlN, InN et leurs alliages sont communément appelés « matériaux III-N ».

6.1.2 Le HEMT, un transistor au fonctionnement bien particulier

6.1.2.1 Fonctionnement ***général***

La structure de transistor étudiée dans cette thèse est de type HEMT. Le HEMT (High Electron Mobility Transistor) est un transistor à effet de champ latéral. Sa principale différence par rapport aux autres transistors, tels que les JFET (Field Effect Transistor), les MOSFET (Metal Oxide Semiconductor Field Effect Transistor) et autres, réside en la présence d'un gaz bidimensionnel, le 2DEG, formé à l'interface de l'hétérojonction entre deux matériaux semi-conducteurs ayant des bandes interdites de valeurs différentes. Ce gaz se caractérise par une grande mobilité des électrons, ce qui permet au transistor de fonctionner à des fréquences plus élevées que les autres structures. Ce gaz présente également une densité électronique élevée [20,21,24,26,27].

L'hétérojonction d'un HEMT, historiquement constituée du couple de matériaux AlGaAs/GaAs est plus récemment constituée de matériaux AlGaN/GaN. C'est cette dernière association de semi-conducteurs qui présente un intérêt tout particulier pour les applications de puissance. Un schéma général de la structure a été dessiné sur la Figure 287 ci-dessous.

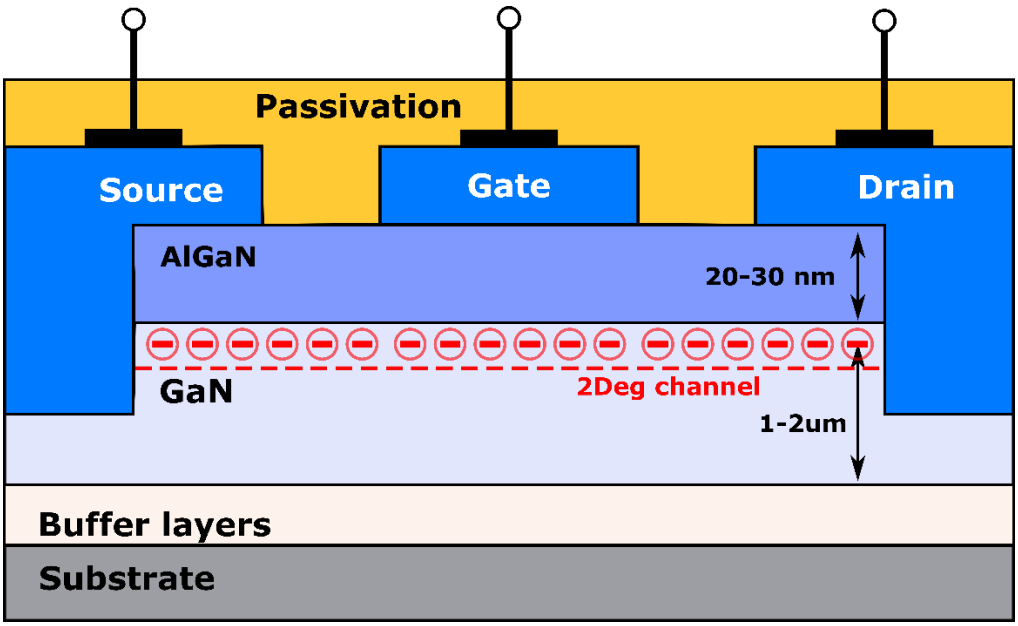

Figure 287: Vue en coupe d'un composant HEMT avec ses trois électrodes (Grille, Drain, Source), à partir de [7], [18], [19]

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La physique d'un transistor HEMT GaN fait intervenir plusieurs mécanismes. Tout d'abord la polarisation piézoélectrique déplace les électrons au sein de l'hétérojonction AlGaN/GaN. Les électrons excédentaires restent à ce stade encore confinés dans l'AlGaN dopé N. la différence de dopage et de gap va finalement leur permettre de basculer dans le GaN et de rester confiné dans un puit quantique, formé par la courbure des bandes énergétiques.
Le transistor HEMT tel qu'il est présenté est naturellement conducteur. Cela signifie que le transistor conduit même en l'absence de polarisation sur la grille ($V_{GS} = 0$ V). L'industrie préférant les composants normalement bloqués, différentes structures ont été développées.

6.1.3 Les différentes structures de HEMT

Différents types de structures existent. Parmi elle la plus simple est la structure cascode. En amont du HEMT GaN, un MOSFET silicium a été rajouté. Il vient piloter le HEMT GaN et lui confère ainsi son caractère normalement bloqué.

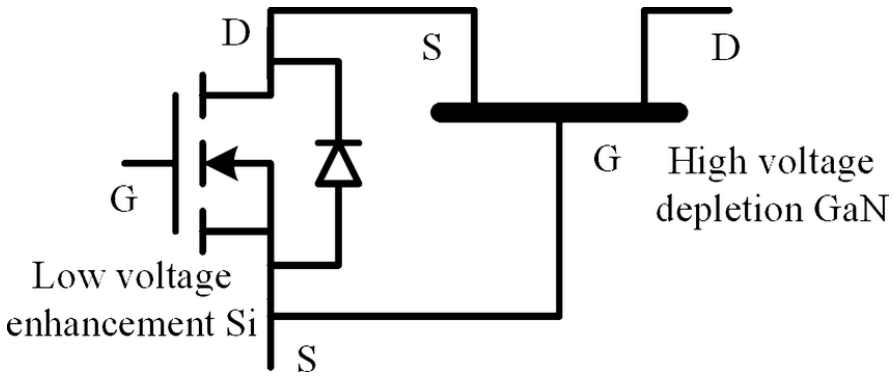

Figure 288: schéma d'une structure cascode combinant un MOSFET Si et un HEMT GaN

Son avantage est également son inconvénient majeur puisqu'on perd la commutions extrêmement rapide du HEMT GaN, cette dernière étant désormais pilotée par le MOSFET Silicium.

Les autres structures reprennent le schéma initial du transistor normalement passant et viennent apporter des modifications au sein de la structure physique. On retrouve ainsi le transistor à grille dite enterrée. Sur une profondeur d'une dizaine de nm, on vient graver la grille jusqu'à se rapprocher du canal 2DEG. La couche d'AlGaN réduite vient réduire la polarisation piézoélectrique et interrompt alors localement la formation du 2DEG. Cette technique, bien que conférant l'aspect normalement bloqué au transistor, n'en est pas moins exempt de défaut avec une criticité au niveau de la profondeur de la gravure et ainsi de la stabilité du V_{th}. La Figure 289 illustre cette structure où l'on retrouve cette grille dite enterrée.

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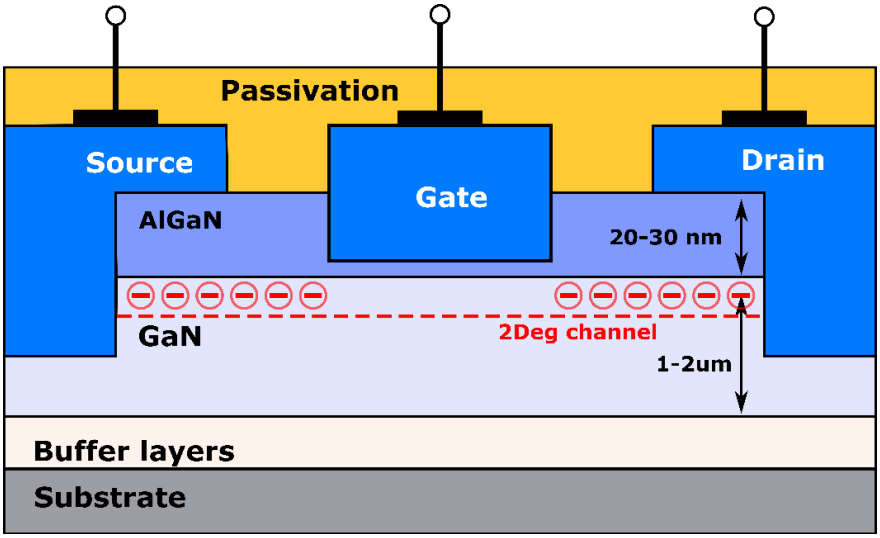

Figure 289: structure de HEMT dite à grille enterrée

La structure MIS(MOS)HEMT repose sur le même principe de base et s'attache à réduire le courant de fuite de grille par l'adjonction d'un isolant (structure MIS-HEMT) ou d'un oxyde (structure MOS-HEMT). Le principal inconvénient de cette structure réside dans l'instabilité du V_{th} avec des phénomènes de piégeage dans l'isolant. La Figure 290 illustre cette structure.

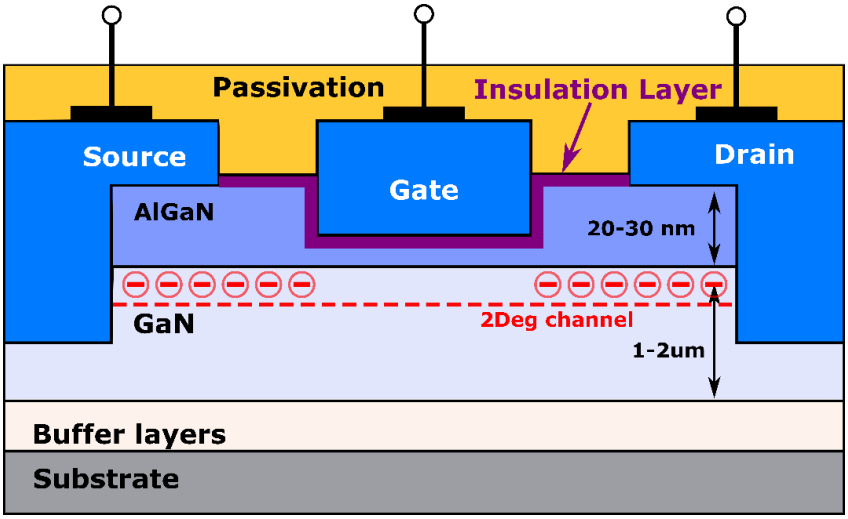

Figure 290: structure de MIS-HEMT

Une autre structure vient placer non pas un isolant sous la grille mais des ions fluorés. Ces derniers agissent comme une charge négative et, par conséquent, courbent vers le haut la bande énergétique du GaN, épuisant localement le puits quantique. En appliquant une tension positive sur la grille, le transistor est à nouveau capable de former le canal 2DEG et d'établir la conduction. Enfin on retrouve la structure p-GaN.

Une couche de GaN dopé p est insérée entre la grille et la couche d'AlGaN. Les trous chargés positivement attireront les électrons de conduction du canal. Leur départ du canal va donc le couper temporairement. Dans le même temps, les charges positives des trous en p-GaN sont recombinées avec les électrons de conduction déplacés du canal. Il n'y a donc plus d'électroneutralité dans le p-GaN, les charges négatives dominent et, repoussent les électrons du canal et cassent ce dernier de manière établie. Cette technique est encore à l'étude, notamment pour la rendre plus fiable et obtenir une tension de seuil élevée (>2V) [25,57]. Un exemple de structure p-GaN, associée à une architecture MIS-HEMT a été dessiné dans la Figure 291.

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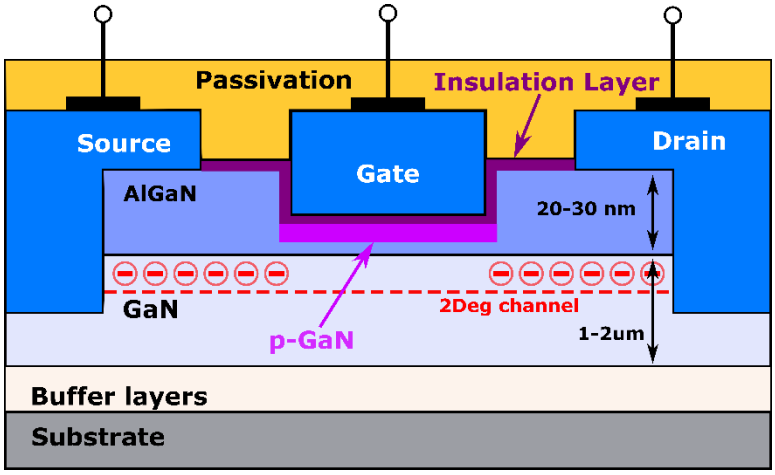

Figure 291: structure normalement bloquée d'un composant MIS-HEMT de type p-GaN

Une autre structure, également basée sur la mise en œuvre d'un matériau dopé p sous la grille, a été développée. Au lieu d'avoir du p-GaN et une barrière statique, la structure GIT (Gate-Injection-Transistor) repose sur l'injection active de trous grâce au matériau p-AlGaN [59–61] lorsqu'une tension positive suffisante est appliquée sur la grille. Un schéma de la structure est présenté à la Figure 292.

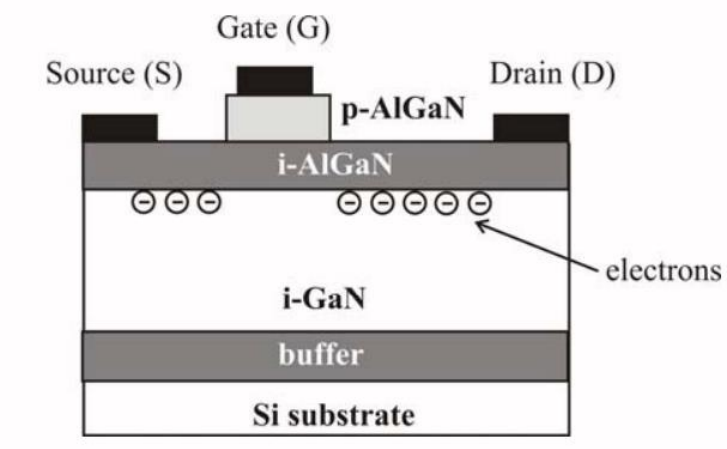

Figure 292: Structure GIT, tiré de [60]

Ces différentes structures confèrent le caractère normalement bloqué au HEMT GaN. Pour autant, ces différents ajustements ne sont pas exempts de défauts et peuvent occasionner des problèmes de fiabilité. Le court-circuit représente justement un enjeu crucial en terme de fiabilité. Avec la présence simultanée de forts tension et courant entre les bornes drain et source du composant et donc une énergie importante à dissiper à travers le transistor, les courts-circuits sont considérés comme l'une des incidents les plus indésirables, [[46,78,80–82].

6.1.4 Etat de l'art des courts-circuits pour les transistors de puissance GaN

6.1.4.1 Quelques définitions en la matière de court-circuit

La Figure 293 illustre les valeurs élevées simultanées du courant et de la tension lors d'un court-circuit. Les courts-circuits se caractérisent par une augmentation très rapide du courant, bien au-delà du courant nominal du composant et en moins d'une microseconde, puis par une forte réduction du courant de

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drain. Comme il a été expliqué plus haut, le comportement délétère vient du fait que pendant tout ce temps la polarisation drain-source reste à un niveau quasi-constant, à l'exception pendant les commutations ON/OFF où une brève chute de tension peut être observée.

En outre, l'un des avantages mais aussi l'une des difficultés des composants GaN réside dans le fait que les fronts de montée et descente du courant sont extrêmement rapides. GaN Systems a rapporté dans [83] que le courant de drain n'a besoin que de 5 ns pour atteindre 30 A à la mise en conduction. Avec une inductance parasite typique de 15 nH, cela conduit déjà à une surtension de 150 V.

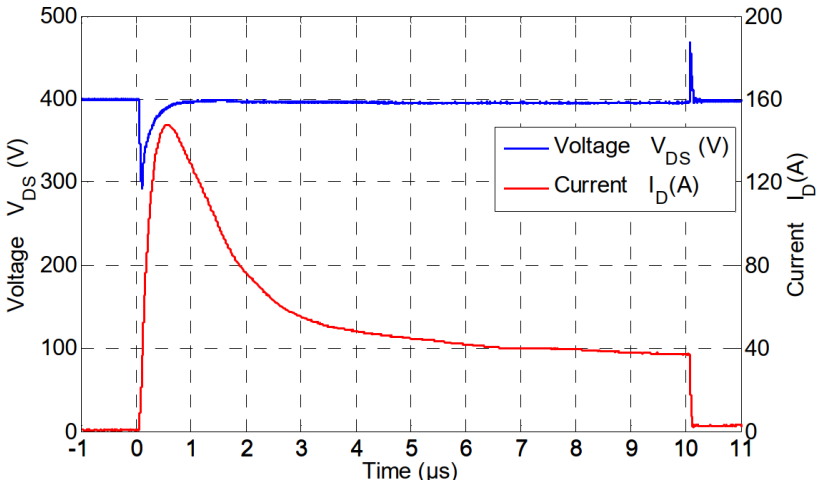

Figure 293: current and voltage waveforms during short-circuit [79]

Trois types de court-circuit existent. Parmi eux, on distingue les courts-circuits de type 1 et de type 2. Le type 3 est spécifique aux composants équipés de diode en anti-parallèle et pouvant effectuer de la conduction inverse[21,85].

Le court-circuit de type 1 est connu comme étant le plus fréquemment rencontré [34,78]. Par conséquent, le test de type 1 est privilégié dans l'industrie [11], [12] et donc dans les publications scientifiques. Pendant l'essai de type I, le composant est à l'état bloqué, et est donc soumis à une tension élevée. Le composant est rendu passant pendant la défaillance. Par conséquent, un courant important traverse le transistor. L'augmentation du courant est très rapide, de l'ordre de quelques dizaines de nanosecondes, et diminue ensuite. C'est pourquoi ce type de défaut est également appelé défaut de commutation dur. Comme la tension est toujours présente entre le drain et la source du dispositif, la dissipation de puissance est importante et une défaillance thermique peut se produire. La réduction du courant drain-source I_D à l'aide de systèmes de détection et de protection permet d'éviter la casse du composant. De telles solutions ont été brevetées, par exemple avec le limiteur de courant de court-circuit [46], mais elles restent limitées et présentent des inconvénients substantiels. Il convient également de mentionner qu'il existe plusieurs types de mécanismes de défaillance, non encore clairement expliqués aujourd'hui. Ils seront détaillés plus loin.

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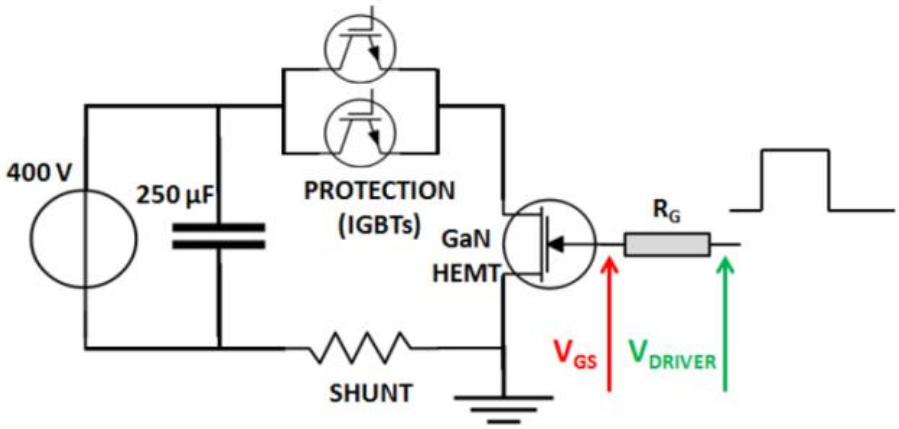

Figure 294: schéma d'un banc de test visant à reproduire les court-circuit de type 1 , tiré de [79]

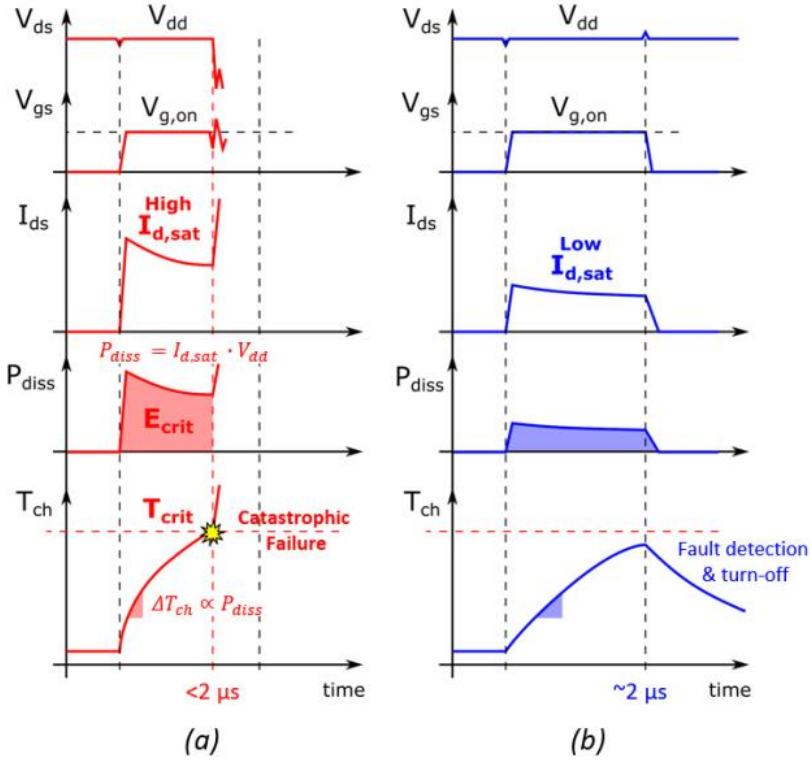

Figure 295: Formes d'ondes durant un court-circuit pour un courant élevé et une densité de puissance élevée (a) et un courant et une puissance plus faibles permettant au système de protection de détecter le défaut avant une température trop critique (b) [46]

Pour le court-circuit de type II, le composant sous test est déjà mis sous tension avant le défaut et conduit un courant. Pour cette raison, il est appelé défaut sous charge [21,35]. Compte tenu du fait que la conduite du défaut augmentera la tension grille-source, le type II est considéré comme plus nuisible que le type I [21].

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6.1.4.2 Bref historique et contextualisation

En 2013, l'auteur de [87] prédisait de mauvaises performances en court-circuit des composants GaN latéraux par rapport aux IGBT verticaux en silicium bien connus. L'auteur de cet article met notamment en évidence un champ électrique dix fois plus important pour les GaN latéraux que pour les IGBT au silicium lors de fortes polarisations drain-source. Couplée à une densité de courant accrue pour la technologie HEMT GaN, la puissance thermique dissipée lors d'un court-circuit est significative avec une possibilité de dizaines de kW à dissiper dans des dispositifs de quelques millimètres de large. Par conséquent, un court-circuit est lié à une augmentation très rapide du courant de drain [46]. Il serait d'autant plus destructeur que, contrairement à l'IGBT Si, le courant circule dans une région très fine appelée canal 2DEG (couche AlGaN de l'ordre du nm, GaN de l'ordre de la dizaine de nm [24]).La conséquence directe serait des points de chauffe extrêmement localisés. Si l'on ajoute à cela une conductivité thermique relativement mauvaise, à comparer notamment avec le carbure de silicium SiC, et l'apparition extrêmement rapide de ces points de chauffe localisés, la fiabilité des transistors HEMT GaN face aux courts-circuits est relativement complexe.

A titre de comparaison, les composants SiC peuvent supporter une durée de court-circuit comprise entre 8 et 13 µs, sur un bus DC de 600 - 700 V [21]. Selon les auteurs [88,89], les composants SiC sont capables de résister à des milliers de courts-circuits répétitifs d'une durée supérieure à 10 µs. La plupart du temps, la défaillance se produit dans l'oxyde de la grille. La réduction du courant de saturation et l'augmentation de la résistance à l'enclenchement sont les seuls signes de fatigue. Pour les composants en SiC, une augmentation du courant de fuite de la grille peut également être perçue comme un signe de court-circuit et permet de prévenir la défaillance [86]. Au contraire, il n'y en a à ce jour pas de signe précurseur connu pour les composants GaN [35,91].

Pour cette raison aujourd'hui l'origine des défaillances du GaN n'est pas bien comprise, avec des défaillances inexplicables, très rapides de l'ordre de quelques microsecondes voire de centaines de nanosecondes ou des défaillances longues de plusieurs dizaines de microsecondes).

Parallèlement à constat plutôt défavorable, si les premières études sur le court-circuit ont été observées à partir de 2013, dix ans plus tard, la situation n'en est pas clarifiée pour autant. Elle reste limitée à plusieurs égards, notamment du fait que la technologie Normally-Off avec composants p-GaN et cascode a été presque exclusivement étudiée au détriment de la technologie Normally-On [30], [31], [45], [45], [68], [69], [72], [75], [82]–[94].

Dans [35], certaines technologies ont été testées, notamment le HEMT normalement bloqué avec la structure p-GaN, le cascode le HEMT normalement passant. Un résumé est présenté dans le tableau 26. Le seul HEMT normalement passant qui a passé l'épreuve du court-circuit, d'une durée de 30 µs, avait une polarisation de grille proche de sa tension de seuil (état semi-on). Par conséquent, la défaillance était plutôt due au champ électrique élevé qu'aux caractéristiques du court-circuit. Pour les HEMT à enrichissement (E-HEMT ou HEMT en mode E, par opposition aux HEMT à dépletion, d-mode), même si quelques échantillons ont résisté au-delà de la durée critique de 10 µs, la majorité d'entre eux casse avant 1 µs de conduction. Cette non-robustesse des composants GaN peut être liée à la densité considérable de courant et à la puissance thermique importante à dissiper dans un faible volume.

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TABLE I
STATE-OF-THE-ART OF SC CAPABILITY

Device technology	V_{BR} (V) - I_D(A)***	V_{DC} (V)	t_{on}||t_{SC} (µs)	ΔI_D (%)	V_G (V)
GaN EHEMT [20]	200 - 3	50*	10	25	+4/0
		100	2	-	+4/0
GaN cascode [2]	600 - 20	150*	10	39	+12/0
		200*	10	-	+12/0
		<280*/**	10	-	+12/0
GaN cascode [18]	600 - 5	400	7.8	-	N/A
	600 - 16	400	7.7	-	N/A
	600 - 30	400	7	46	N/A
GaN DHEMT [19]	650 - N/A	250*	10	40	0/-15
		300	4	-	0/-15
		350	0.9	-	0/-15
		400	<0.5	-	0/-15
		400	30	-	-1.5/-15
GaN cascode [16]	600 - 18	100*	10	70	+10/0
		100	14	-	+10/0
		200	4	-	+10/0
		300	1.8	-	+10/0
GaN EHEMT [16]	600 - 16	100*	10	33	+5/-3
		150	4.5	-	+5/-3
		150*	4	-	+5/-3
		200*	2	-	+5/-3
GaN EHEMT [17]	650 - 60	400*	10	90	+5/0
		400	1.2	-	+5/0
		400*/**	500	-	+5/0
	650 - 30	270**	>800	-	+5/0
		270**	>800	-	+5/0
	650 - 22	400	~0.2	-	+5/0
		400	~0.2	-	+5/0

* Non-destructive SC results / ** Only for few parts / *** Rated values

Table 30: Etat de l'art à propos des tenues en court-circuit de différentes structures HEMT GaN, à partir de [35]

La Figure 296 résumé l'étendue des études pour les composants p-GaN. Elle représente la durée du court-circuit en ordonnée et la tension drain-source appliquée. Les points verts signifient que les dispositifs ont résisté au court-circuit tandis que les points orange indiquent qu'ils ont cassé. Si l'on peut noter que des composants résistent aux tensions les plus élevées, il faut préciser que c'est au prix de concessions techniques (environnement surchauffé ou résistance de grille accrue par exemple). Ces phénomènes seront expliqués plus en détail ci-dessous. En l'absence d'un tel ajustement, la polarisation drain-source maximale reste de l'ordre de 150 à 200 V. De plus, si la performance en court-circuit reste limitée en tension, les composants cassent très rapidement, parfois de manière aléatoire et, par conséquent, les mécanismes de défaillance restent incompris.

Aucun article ne s'intéresse à la technologie normalement-on, malgré le fait qu'il s'agisse de la structure la plus simple (pas de MOSFET Si en amont comme dans la structure cascode ou de modification spécifique de la structure ou de la grille comme dans la configuration p-GaN). En outre, les études actuelles se concentrent principalement sur la résistance du composant après un court-circuit unique et sur la durée avant défaillance.

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Une étude récente ([97]) a montré une amélioration majeure de la robustesse, avec un TLF (Time Leading to Fail, Temps avant défaillance) autour de centaines de microsecondes, sous une tension de bus de 400 V et une tension grille-source de 5 V (HEMT p-GaN provenant du fournisseur GaN Systems). Néanmoins, si la robustesse en la matière a fait des progrès, il n'en est pas de même pour la résistance à la fatigue. Il a été remarqué que des composants ne supportent pas plus de vingt courts-circuits de seulement 20 ns ([97]). C'est encore pire pour une durée de court-circuit de 1 µs, la défaillance arrivant au deuxième événement.

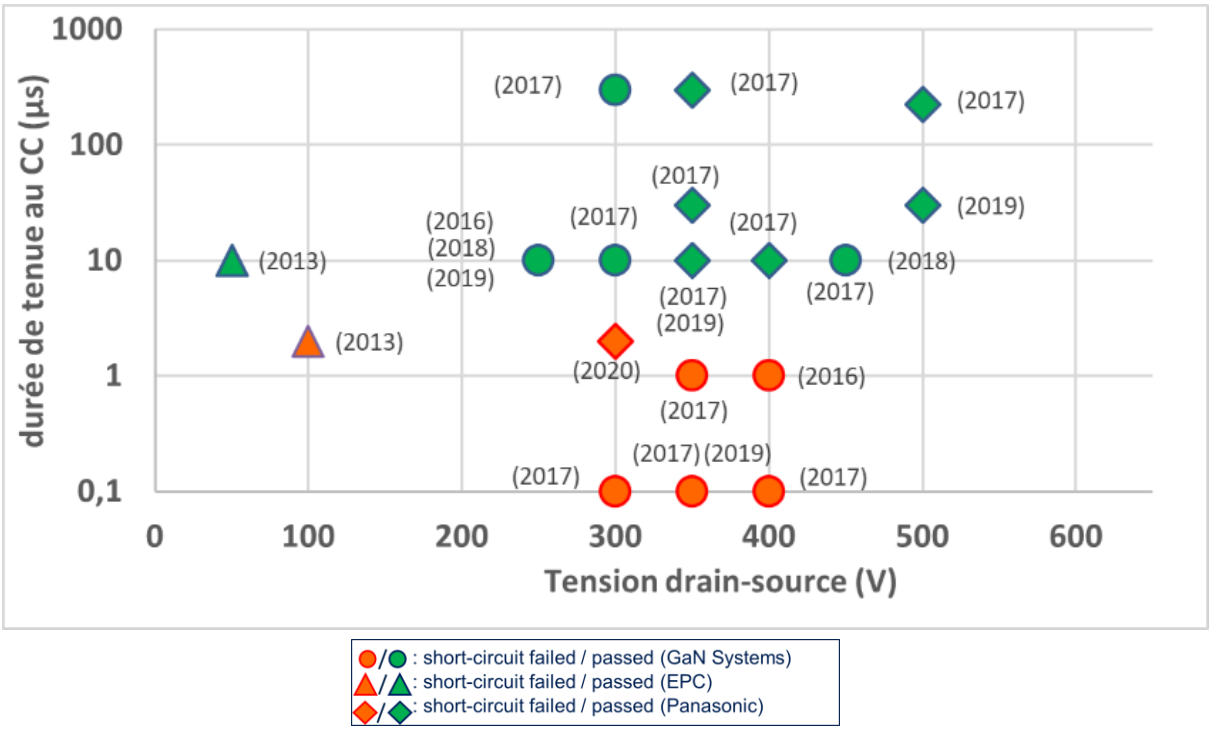

Figure 296: Etat de l'art à propos de la tenue en court-circuit unique pour des composants HEMT p-GaN, réalisé à parti de [34,35,78,81,91,101,103,103,104,104]

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6.2 Chapitre 2 : Développement et optimisation expérimentale du banc de court-circuit

6.2.1.1 Stratégie globale et originalité par rapport à l'état de l'art

Comme il a été mentionnée dans le chapitre 1, le court-circuit de type 1 est le plus rencontré [34,78] et est pour cette raison majoritairement étudié. Par conséquent cette thèse se focalise sur ce type de court-circuit.

La littérature actuelle s'est principalement concentrée sur l'étude des courts-circuits destructifs, avec l'inconvénient majeur de ne pas pouvoir étudier le composant une fois qu'il a été détruit. La stratégie de cette thèse ne se concentre pas sur les tests destructifs mais sur les tests répétitifs non destructifs. L'objectif est de visualiser les éventuelles variations paramétriques, statiques, du composant au moyen de caractérisations statiques réalisées avant et après la série de courts-circuits. Une attention particulière sera également portée aux éventuelles variations dynamiques du composant au fur et à mesure des différents courts-circuits. La variation statique de R_{DS_ON} sera également étudiée par des caractérisations.

En termes de stratégie de test, pour les courts-circuits de type 1, le composant est d'abord bloqué à l'aide d'un driver développé spécifiquement à cet effet, puis il est mis sous tension par une polarisation adéquate appliquée sur sa grille. Les composants normalement bloqués sont polarisés négativement avec un signal V_{GS} = -6 V afin de renforcer l'état bloqué. Les polarisations appliquées en fonction du type de composant et leurs paramètres généraux sont explicités dans le tableau ci-dessous.

Component	Supplier	V_{th}	V_{GS} OFF / V_{GS} ON	Id	R_{DS_ON}
D-mode	Supplier 1	-12.5 V	- 24 V / 0 V	10 A	250 mΩ
Cascode	Supplier 1	1.8 V	- 3 V / +6 V	10 A	190 mΩ
p-GaN	Supplier 1	1.8 V	- 3 V / +6 V	15 A	120 mΩ
p-GaN Prototype	Supplier 1	1.7 V	- 3 V / +6 V	11 A	150 mΩ
p-GaN	Supplier 2	1.7 V	- 3 V / +6 V	11 A	150 mΩ

Table 31: Récapitulatif des composants testés en court-circuit et de leurs caractéristiques principales

6.2.1.2 Conception du banc de tests

Pour recréer un événement de court-circuit, des condensateurs sont utilisés et connectés en parallèle avec le composant. Préalablement chargés par l'alimentation haute tension lorsque le composant est bloqué, ils se déchargent dans ce dernier lorsqu'il devient passant. De cette façon, c'est le composant qui définit la valeur du courant de court-circuit.
La sévérité du test dépend alors de divers paramètres tels que la tension délivrée par les condensateurs et la durée du court-circuit ou, dans le cas présent, le nombre de courts-circuits répétitifs effectués. Les éléments inhérents au banc, tels que les inductances parasites, peuvent également influencer le comportement du transistor pendant le court-circuit.
La rupture d'un composant entraîne le plus souvent un court-circuit entre le drain et la source [21], ce qui provoque une augmentation très rapide du courant circulant à travers le banc d'essai. Pour protéger le banc et éviter la projection de matière en fusion, un circuit de protection simplifié est inséré. Un premier schéma est présenté ci-dessous avec la Figure 297, C_b et C_S représentant les condensateurs utilisés. Il sera expliqué plus loin le choix du type de capacité.

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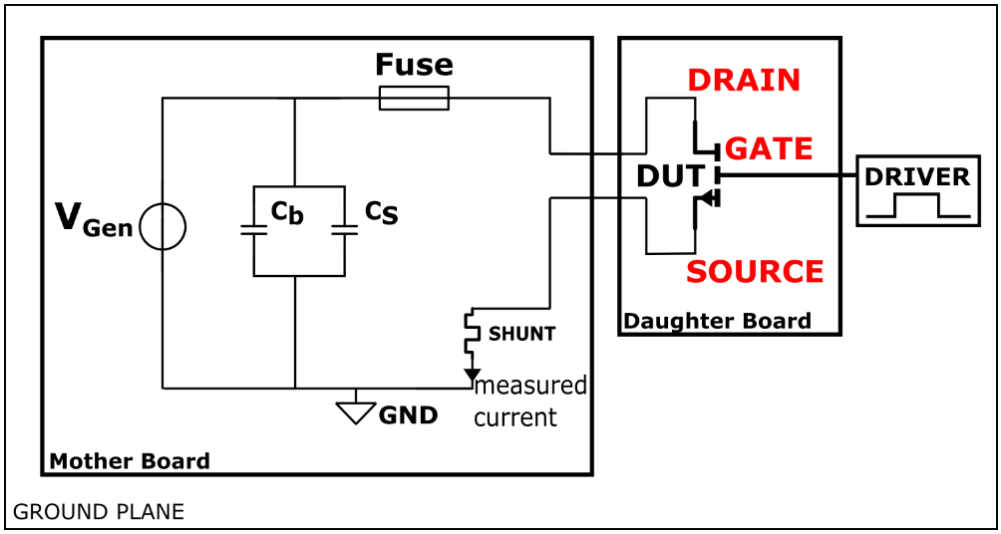

Figure 297: Schéma de principe du banc d'essai en court-circuit

Les études antérieures sur les courts-circuits ont souvent fait état de surtension élevée (>100 V) limitant la plage de tension drain-source pendant les tests de court-circuit [21]. En raison des fronts de courant très rapides typiques de la technologie GaN, la moindre inductance parasite dans la boucle de puissance du circuit imprimé entraîne une surtension importante et peut s'avérer délétère.

Pour les composants étudiés, avec un courant de court-circuit d'environ 50 A (estimation basse) et un temps de commutation typique de 20 ns, une inductance parasite de 80 nH provoque déjà une surtension de 200 V ! Le circuit a donc été conçu pour réduire au maximum les inductances parasites. L'élément de protection, souvent un switch actif comme l'IGBT, considéré comme hautement inductif, est remplacé ici par un fusible SMD, qui assure une protection suffisante avant sa possible destruction. Pour reproduire les conditions de court-circuit, et en particulier la montée rapide d'un fort courant, tout en minimisant la chute de tension, deux condensateurs de 2 µF (céramique à très faible inductance parasite, Cs) et de 133µF (polypropylène, Cb) sont connectés en parallèle.
Le banc d'essai se compose alors de trois éléments clés : la carte mère d'alimentation avec les condensateurs, le fusible et le shunt de mesure du courant ; la carte fille avec le transistor encapsulé dans son sarcophage, et la carte driver.

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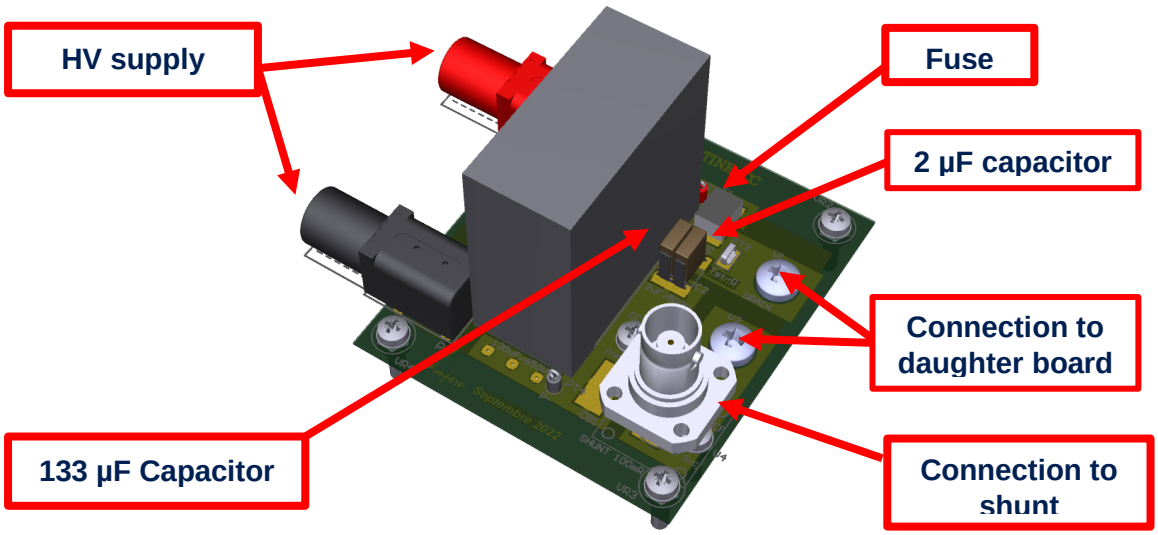

Figure 298: vue 3D de la carte mère / puissance

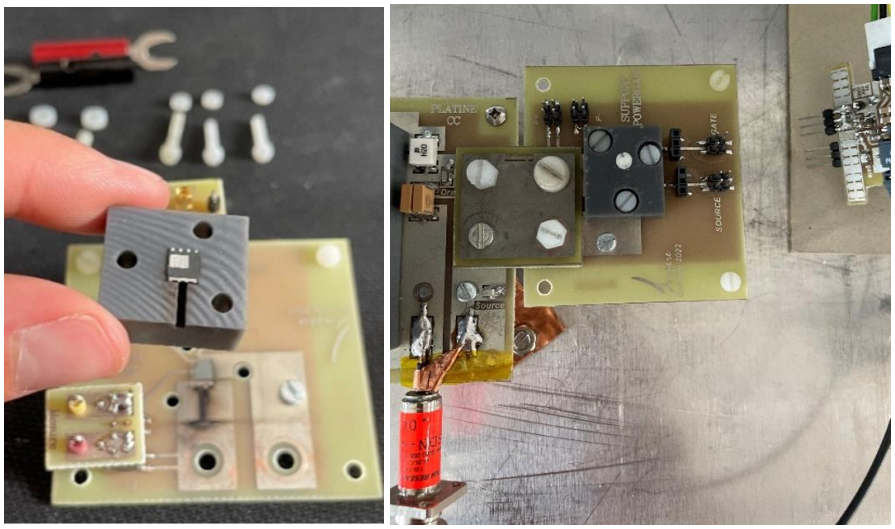

Figure 299: sarcophage obtenu par impression 3D (à gauche) et une fois monté sur la carte fille (à droite)

Une carte driver a été spécialement développée pour le banc d'essai. Elle se compose de deux parties : la carte d'alimentation du driver et la carte abritant le driver, comme le montre la Figure 300. La première carte, comme son nom l'indique, est utilisée pour alimenter le driver et ajuster les tensions de commande ON et OFF appliquées à la grille du composant.
Au moyen de connecteurs verticaux, l'ensemble des cartes alimentation driver et driver est branché le plus près possible du composant.

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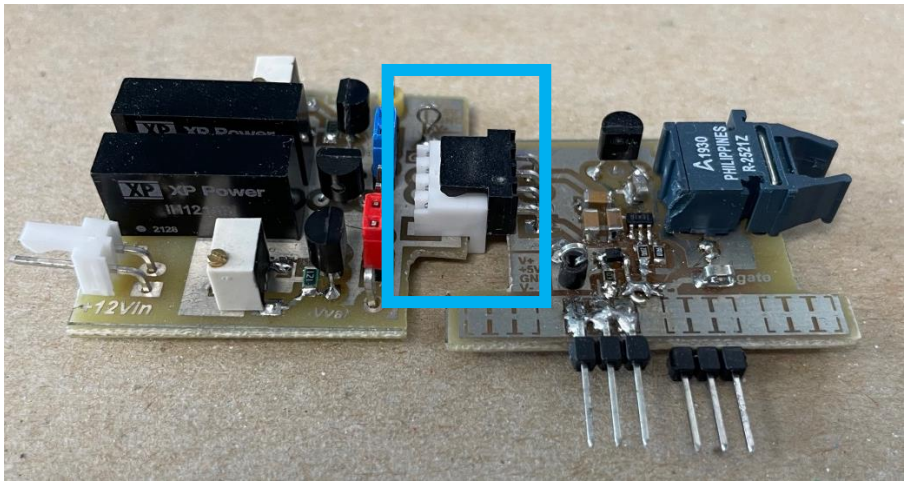

Figure 300: l'ensemble driver avec à gauche la partie alimentation driver et à droite la partie driver

La Figure 300 montre un connecteur blanc (dans un carré bleu) entre la carte d'alimentation driver te la carte driver. Ce connecteur permet d'éloigner l'alimentation du circuit d'attaque, si nécessaire. Ce connecteur peut être remplacé par des fils, ce qui permet d'éloigner l'alimentation driver de la carte driver ou encore l'utilisation de noyaux de ferrite pour la stabilisation du signal tel qu'il sera étudié dans la partie optimisation
Le signal logique est transmis via une fibre optique, arrivant d'un côté de la carte driver, tandis que les niveaux de polarisation de la grille sont liés la carte d'alimentation driver.

6.2.1.3 Composants normalement passant

6.2.1.3.1 Premiers tests et premiers problèmes

Un soin particulier a été apporté à la réduction des inductances parasites. Cela implique un routage soigné et une compacité optimisée, ainsi que des composants montés en surface avec une inductance parasite réduite. Malgré cela, les premiers courts-circuits ont provoqué des perturbations importantes et le banc a dû être ajusté.
Le premier court-circuit a été réalisé pour une tension drain-source V_{DS} de seulement 10 V. Une surtension non négligeable est observée à la commutation off sur les signaux V_{GS} et V_{DS} comme le montre la Figure 301. Pour V_{DS} = 50 V, les signaux oscillent au risque d'endommager le composant lors du passage à l'état OFF ou même de provoquer sa casse tel qu'illustré sur la Figure 301 (droite). C'est encore pire pour V_{DS} = 75 V. Des solutions ont donc dû être trouvées et sont détaillées plus loin.

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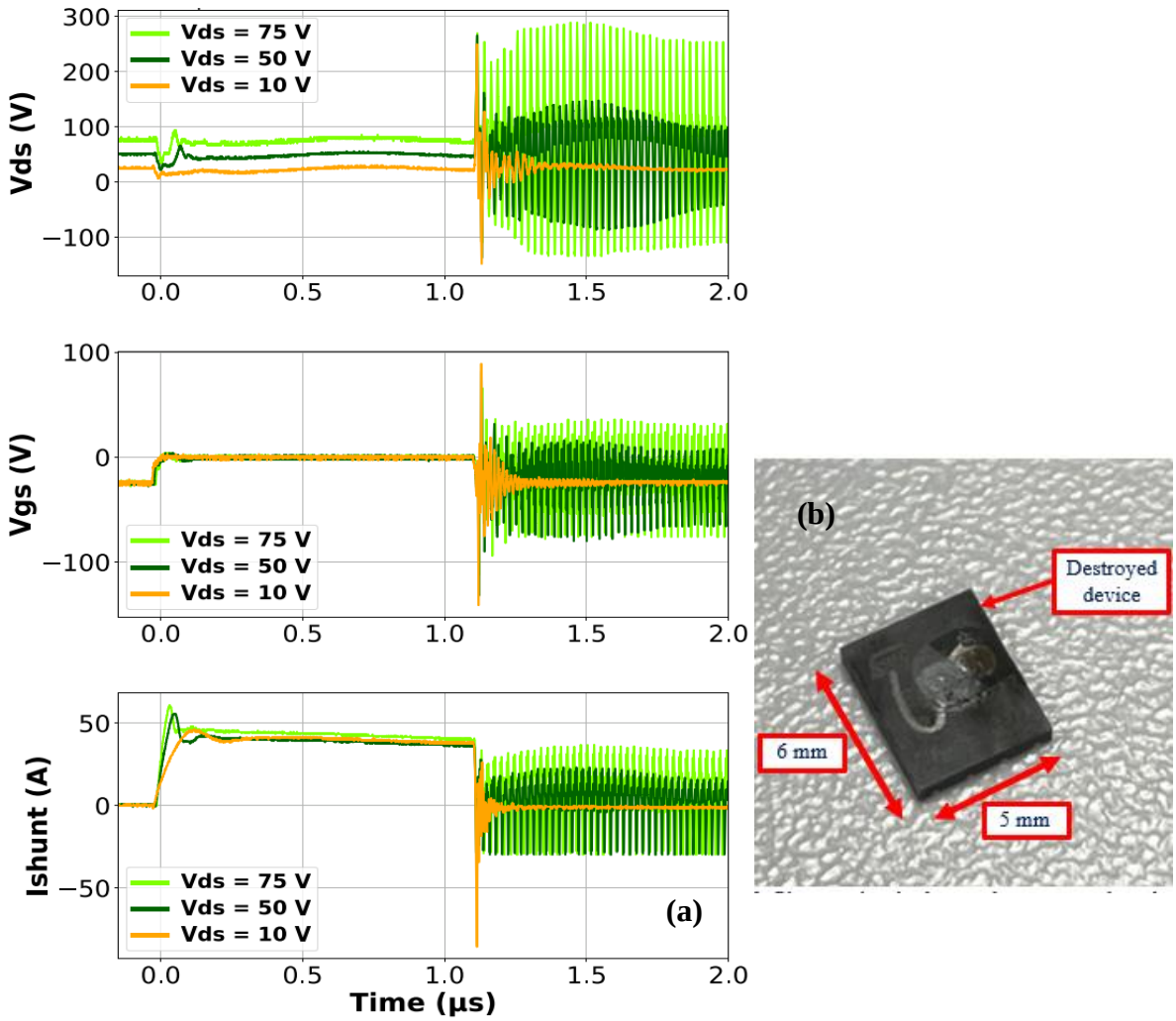

Figure 301: Signaux V_{DS}, V_{GS} et I_{SHUNT} fortement perturbés lors des premiers essais (a-droite), conduisant finalement à la casse du composant et sa décapsulation (b-gauche)

Les premières défaillances de composants apparaissent avec la décapsulation de ce dernier, comme le montre la Figure 301. La présence du fusible intact réduit la probabilité d'un emballement du courant de drain. À ce stade, la défaillance de la grille semble plus probable. Cependant, il n'est pas possible de conclure si la défaillance est due au fonctionnement apparemment instable du banc d'essai ou si le composant n'est pas suffisamment robuste pour résister à des courts-circuits successifs.

6.2.1.3.2 Développement d'une simulation SPICE

Une simulation SPICE a été développée. La simulation présente l'intérêt non négligeable de pouvoir accéder aux tensions à l'intérieur du composant pour les comparer aux tensions observées par les sondes. Un modèle de sonde passive a donc également été développé. Cette simulation a permis de mettre en avant les différences entres les signaux observés par le biais des sondes passives et les signaux réellement perçus par le composant sous test, illustrée sur la Figure 304. On y voit en bleu le signal délivré par la sonde passive, qui présente des surtensions beaucoup plus marquées que celle réellement perçus par le composant, en rose sur le graphe. Cela renforce l'idée d'une utilisation de sondes parfaitement adéquates à la vitesse de commutation des composants GaN.

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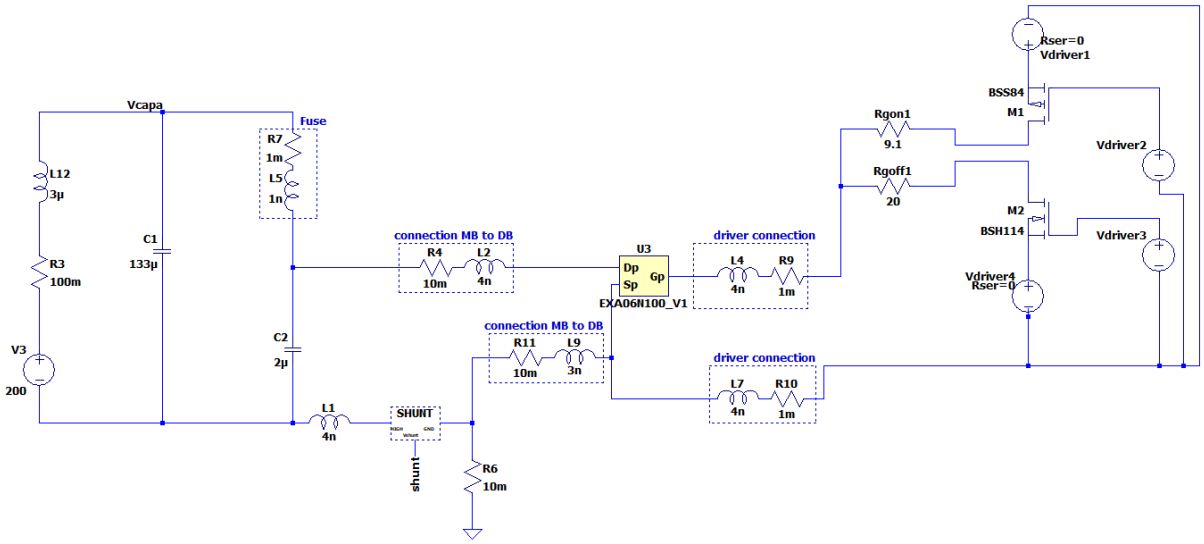

Figure 302: Simulation SPICE du banc d'essais en courts-circuits

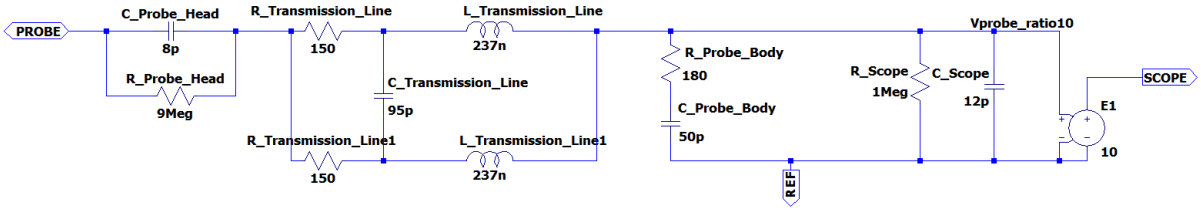

Figure 303: Modèle SPICE de sonde passive

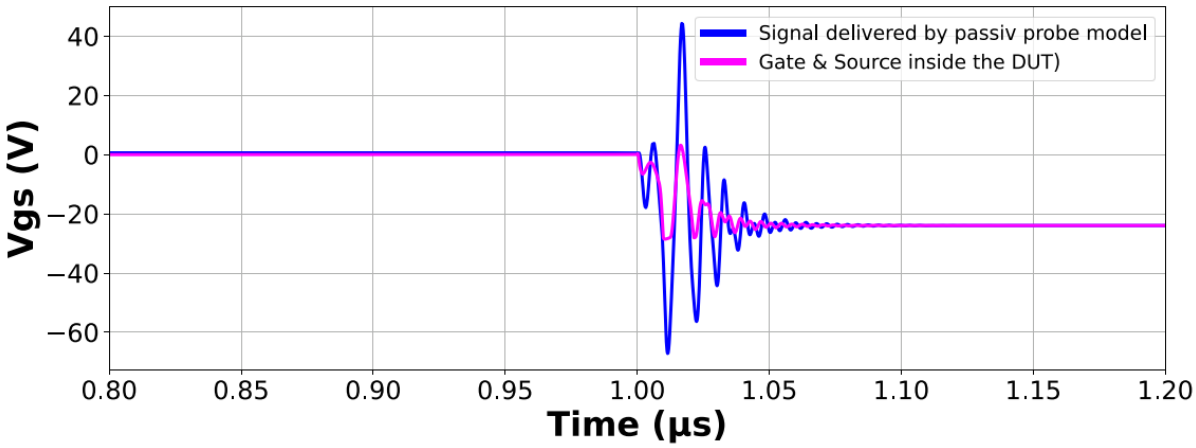

Figure 304: Comparaison des signaux simulés aux bornes du composant et en sortie d'une sonde passive de mesure

6.2.1.3.3 Étude expérimentale de l'impact des sondes

Si la simulation a pu mettre en lumière le fait que les sondes passives ne rendent pas forcément toujours une image fidèle à la réalité des signaux véritablement perçus par le composant, il reste questionnable le fait de savoir si, au-delà de cette déformation, les sondes peuvent être à l'origine de ces déformations. Deux configurations de tests ont alors été essayées, l'une avec 3 sondes passives mesurant V_D,V_G, et V_S et l'autre avec seulement une sonde passive sur V_S, servant de référence et permettant de vérifier si

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la présence ou non des sondes sur les signaux V_D et V_G affectent le comportement du banc. A l'image de la Figure 305, il n'a pas été constaté de différence sur le signal V_S. En revanche, cela a permis de constater que le signal V_S était particulièrement instable lors du turn-off du composant (zone entourée en rouge sur la Figure 305), ce qui amène l'idée d'une circulation de courants de mode commun, souvent à l'origine de perturbation haute-fréquence dans les systèmes de communication et les circuits électroniques sensibles [145–150].

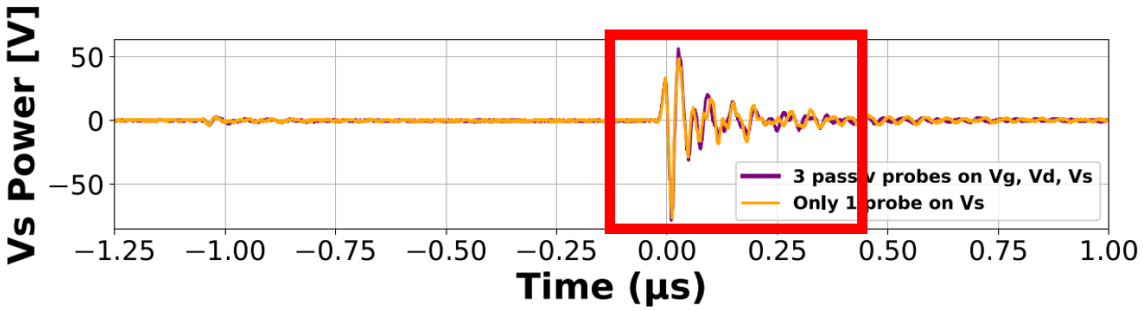

Figure 305: comparaison du signal V_S en présence ou non de sondes passives sur les signaux V_G et V_D

Cette instabilité du signal V_S a poussé l'idée d'un raccordement à un plan de masse. Bien que réduisant les perturbations, cette solution reste insuffisante et d'autres optimisations ont dû être réalisées.

La solution a donc été de se pencher vers d'autres types de sondes que les sondes passives, notamment celles présentant des taux de rejection de courant de mode commun plus important. En parallèle de cela, il a pu être prouvé que la configuration initiale de mesure, avec les boucles de masses attachées aux sondes et raccordées aux différents potentiels de source respectifs étaient particulièrement délétère. La comparaison des sondes passive, différentielle et différentielle isolée optiquement est présentée Figure 306 ci-dessous et est éloquente.

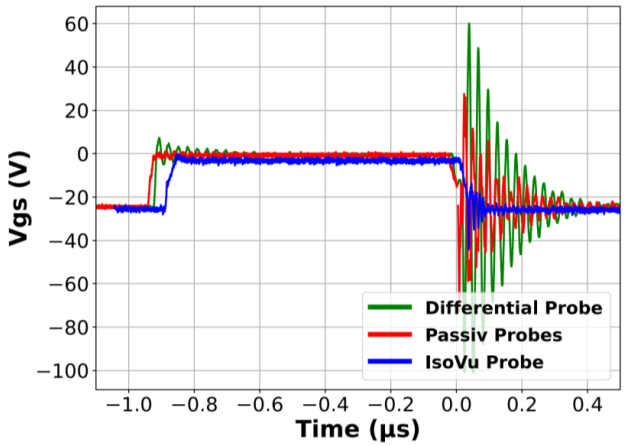

Figure 306: Comparaison de différentes sondes mesurant le signal V_{GS}

Cette analyse conduit à la stratégie suivante en terme de matériel de test:

Signal	**Types de sondes**
V_{GS}	IsoVu probe
V_{DS}	Two passiv probes and a math function from oscilloscope

Table 32: Configurations retenues en termes de sonde de mesure et de signal à mesurer

La dernière optimisation consistera en la réduction de l'inductance parasite du shunt de mesure, qui conduira aux courbes rouge et violet de la Figure 307.

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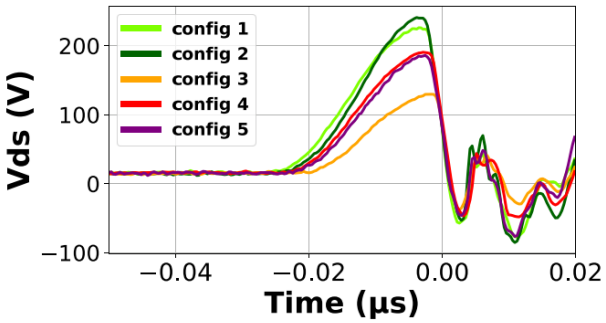

Figure 307: zoom Durant le turn-off du signal VDS

Ces différentes optimisations ont finalement permis d'augmenter la polarisation drain-source jusqu'à une valeur de 200 V en essais répétitifs, jusqu'alors impossible du fait des perturbations significativement élevée. Les formes d'ondes des différents signaux expérimentaux sont illustrées sur la Figure 312.

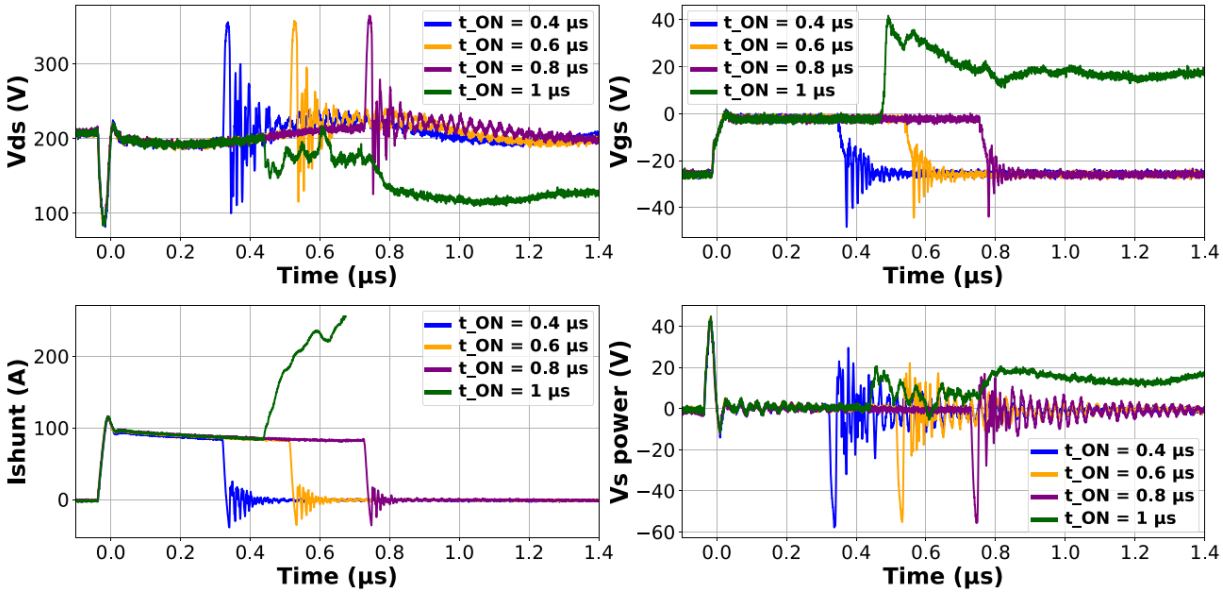

Figure 308 : Signaux expérimentaux V_{DS}, V_{GS}, I_{SHUNT}, $V_{S,POWER}$ pour des courts-circuits répétitifs à V_{DS} = 200 V sur des composants normalement passant

6.2.2 Composants normally-off et de nécessaires nouvelles optimisations

Si les premiers essais des composants de type cascode et p-Gan du fournisseur 1 ont pu se faire sans dommage à V_{DS} = 200 V, il en est tout autre pour les composants p-GaN du fournisseur 2, tel qu'illustré sur la Figure 309 ci-dessous.

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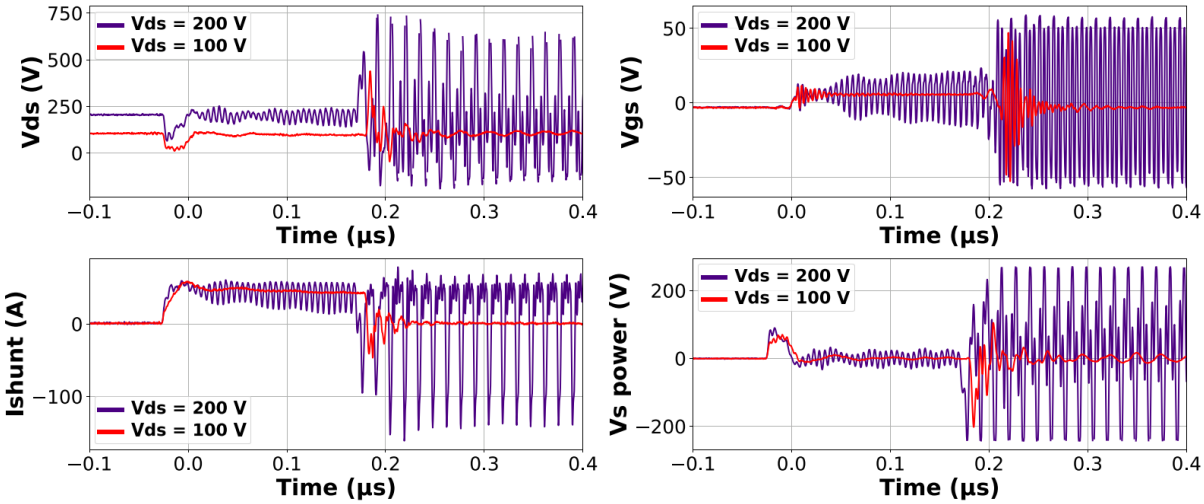

Figure 309: Test des composants p-GaN du second fournisseur pour des tensions V_{DS} de 100 V et 200 V

Différentes tentatives d'optimisations ont été réalisées. La diminution de la résistance de grille commandant la commutation à l'état OFF, R_{G_OFF}, abaissée selon les prescriptions du fournisseur, ou augmentée afin de réduire les oscillations ne donnent aucun résultat satisfaisant et les essais pour V_{DS} = 200 V restent impossible de façon répétée.
La simulation SPICE est retravaillée avec des inductances de pistes corrigées et augmentées ainsi que l'adjonction de capacité parasite modélisant la circulation de courant de mode commun telle qu'évoquée par plusieurs auteurs d'articles [149,159–162]. Cette simulation donne des résultats encourageants à l'image de la Figure 314 où on retrouve des signaux d'allure très similaire à ceux observés expérimentalement.

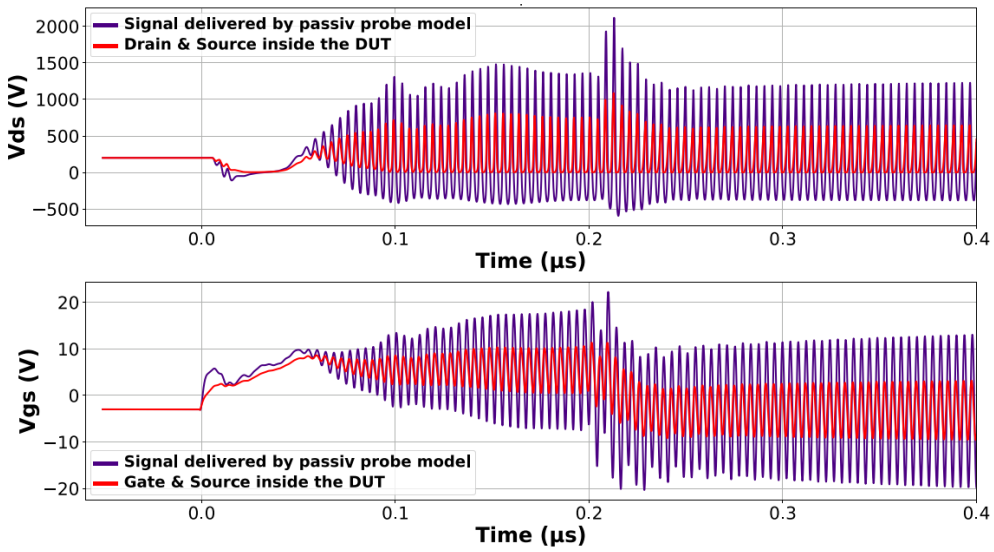

Figure 310: Formes d'ondes simulées des signaux V_{DS} et V_{GS} suite à l'ajout d'une capacité de mode commun sur la grille

Face aux résultats encourageants de la simulation, des tores de ferrite ont été ajoutés au niveau de la liaison driver commandant le signal de grille. Entrelacées deux puis cinq fois, ces configurations ont permis de significativement réduire les perturbations haute-fréquence tel qu'illustré Figure 315.

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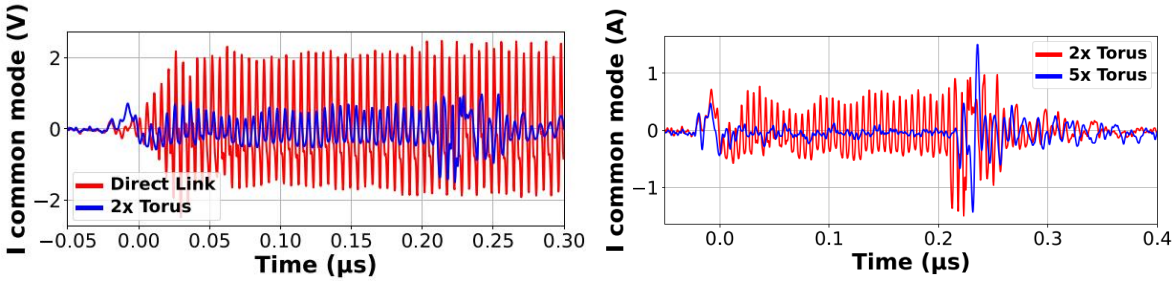

Figure 311: mesure expérimentale de la circulation de courant de mode commun au niveau gate-driver dans une configuration en branchement direct, bouclé deux fois et cinq fois

Cette dernière optimisation a non seulement permis de d'opérer des essais répétitifs et non destructifs pour des tensions VDS = 200 V, chose auparavant impossible, mais également de réduire les surtensions sur le signal VGS, jugé critique au bon fonctionnement du composant, de plus de 50% pour le fournisseur 2 et même 70% pour le fournisseur 1.
Il a également été prouvé que le driver ainsi que la capacité d'isolement de ses convertisseurs DC/DC gérant son alimentation ont un impact sur la stabilité et sur les surtensions des signaux tel qu'illustré sur la Figure 312.

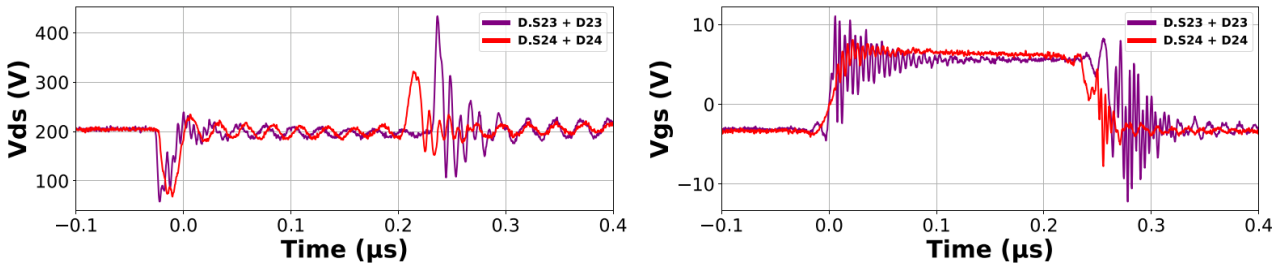

Figure 312: signaux expérimentaux V_{DS} et V_{GS} pour deux versions distinctes de cartes d'alimentation driver et driver

Enfin, une nouvelle carte de test, référencée 2024, a été développée. Son optimisation a permis de mettre en avant l'attention particulière qu'il faut porter au couplage électromagnétique. Son utilisation, à la compacité améliorée, a permi de fortement réduire les perturbations des signaux et notamment de diminuer la chute de tension VDS au turn-ON, élément clé pour les futures normes JEDEC en matière de court-circuit.

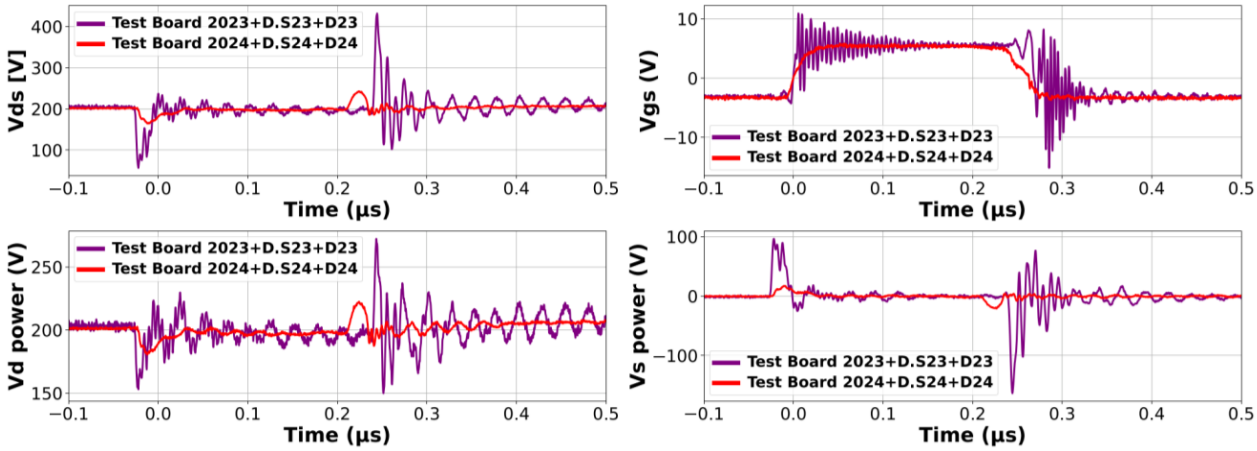

Figure 313: Comparaison des signaux expérimentaux pour des configurations complète (alimentation driver, driver et carte de test) en version 2023 ou 2024

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6.3 Chapitre 3: Résultats

6.3.1 Composants normalement passants

L'étude des composants normalement passant du fournisseur 1 a livré plusieurs résultats. Tout d'abord il a pu être relevé que l'emplacement sur le wafer avait un impact, les trois lots distincts de composants provenant d'un même wafer n'ayant absolument pas le même comportement en court-circuit. Certaines polarisations drain-source semblent également plus délétères que d'autres à l'image de la Figure 314 où des oscillations non-amorties peuvent être remarquées pour V_{DS} = 150 V. Ce même constat est retrouvé pour les composants des autres lots et a défini la tension de test V_{DS} à 200 V.

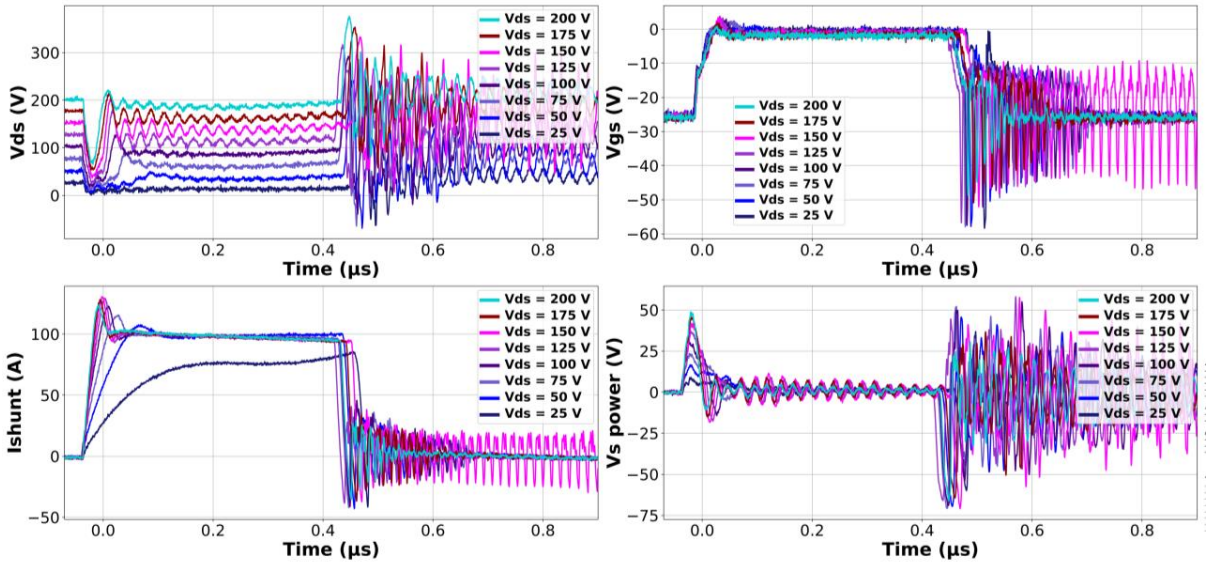

Figure 314: Montée en tension V_{DS} pour un composant normalement passant, du lot B

Des variations dynamiques ont également pu être observé avec une augmentation du niveau de saturation au fur et à mesure de chaque séquence de court-circuit. La Figure 315 illustre cela pour trois séquences, chacun entrecoupées de caractérisations électriques au B1505. Cette variation n'est pas immuable dans le temps puisque les premiers courts-circuits de chaque série ne sont pas nécessairement plus élevés que la série précédente.

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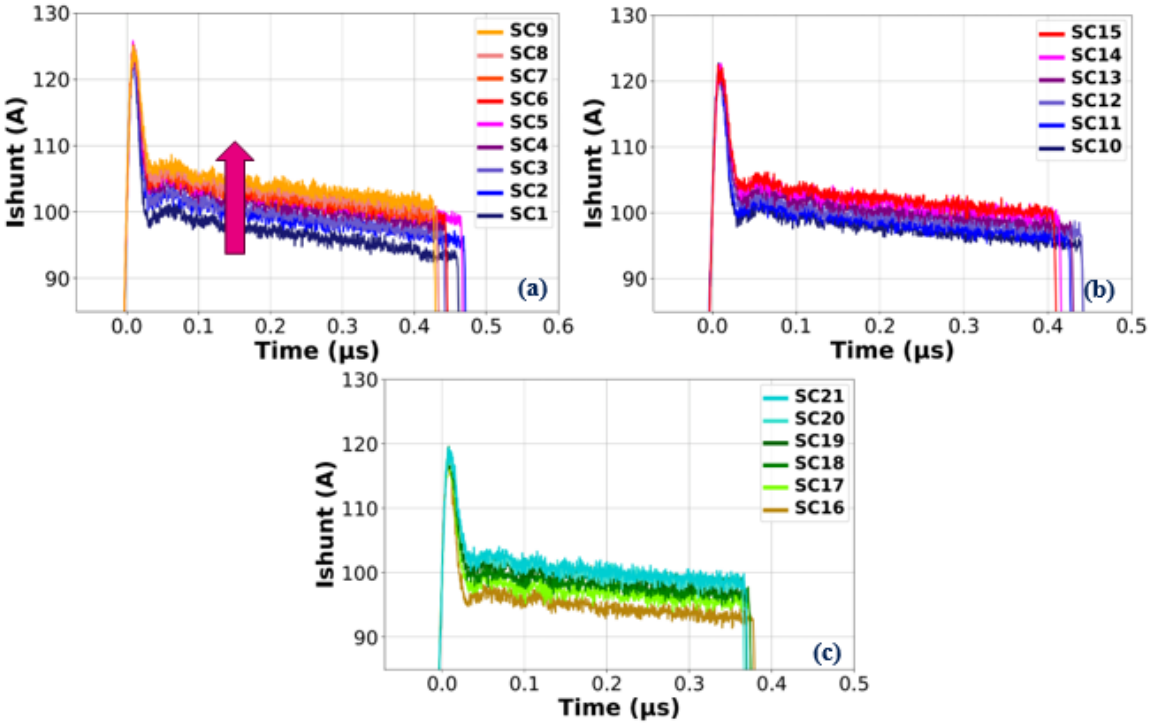

Figure 315: Augmentation du niveau de saturation du courant de court-circuit pour chaque série de courts-circuits

Un autre phénomène est observé pour certains composants avec une augmentation ponctuelle du niveau de saturation quelques courts-circuits avant le court-circuit fatal. La Figure 316 illustre cela avec, pour le dernier essai de la seconde série (SC03-2, en violet), une augmentation du courant au bout de 550 ns de conduction ainsi que pour l'avant dernier de la troisième série (SC03-3, en rouge) au bout de 700 ns de conduction. Le dernier court-circuit (SC04-3) sera fatal au composant. Ce même constat sera retrouvé sur d'autres composants.

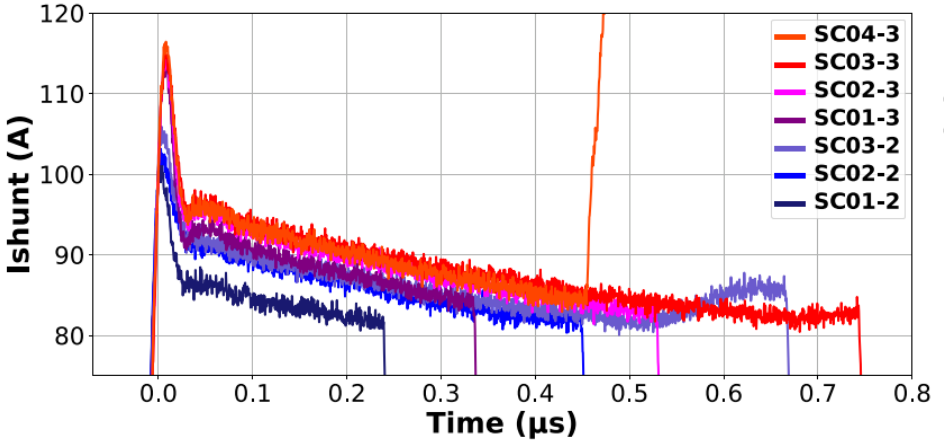

Figure 316: augmentation suspecte du courant de court-circuit peu avant la casse du composant

Les différentes caractérisations électriques au B1505, entre chaque série de courts-circuits répétitifs ont permis de mettre en avant des variations non-négligeables de la tension de seuil V_{th}, en particulier pour les composants du lot B. la Figure 317 illustre cela avec des variations dépassant majoritairement les 5% voire les 10%.

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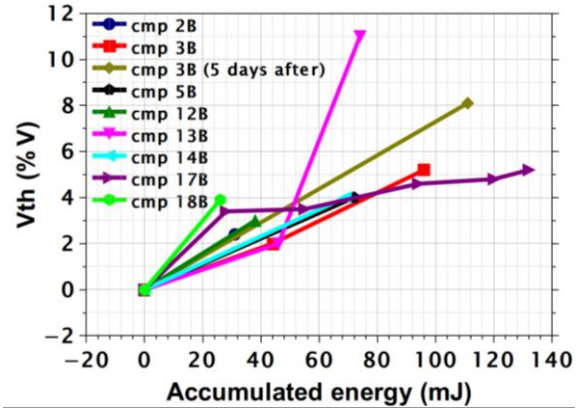

Figure 317: Variation de V_{th} en pourcentage pour les composants du lots B ayant subis plusieurs courts-circuits

Cette réduction de la tension V_{th} peut donc être interprétée comme la capacité du composant à conduire « plus tôt » qu'initialement prévu. Ceci est en accord avec l'augmentation du niveau de saturation du courant de court-circuit vu précédemment et pourrait confirmer un phénomène de piégeage.
Cette variation de la tension de seuil V_{th} peut également être liée à des électrons chauds. En effet, l'application d'une polarisation drain-source en présence d'un flux de courant constitue une situation privilégiée pour la présence de ce type d'électron très particulier, comme expliqué dans le chapitre 1, figure 46, avec notamment un effet tunnel, renforcé par la température, comme expliqué dans [75].

Une autre explication possible est que les électrons chauds créent des états de piège dans ou près de la région de la grille. Les états de piège sont des niveaux d'énergie dans la bande interdite du matériau où les charges peuvent être capturées et immobilisées. Ces états de piège capturent les charges positives environnantes. En effet, les électrons chauds, ayant une énergie cinétique plus élevée que la normale, peuvent interagir avec le réseau cristallin du matériau semi-conducteur, GaN dans ce cas, ou avec le diélectrique, créant des défauts structurels. Ces charges positives, qui contribuaient auparavant à la coupure du canal et à son aspect bloqué, sont désormais moins nombreuses. Les charges positives piégées dans les états de piège créent alors un champ électrique local qui s'oppose au champ électrique de la grille. Cela réduit la tension de seuil [164–167]
Au vu de ces variations paramétriques, un lien peut être établi entre l'impact des courts-circuits répétitifs et la variation de la tension de seuil V_{th}. Cela suggère que des mécanismes de dégradation physique se produisent à l'intérieur de la grille. Des analyses similaires sont effectuées sur des composants normalement bloqués dans la deuxième partie. Dans la dernière partie du chapitre 3, les différents types de casse rencontrés sont expliqués. L'hypothèse de la robustesse supérieure des composants normalement bloqués du fournisseur 1 est également discutée.

6.3.2 Composants normalement bloqués

Après la phase d'optimisation du banc pour les composants normalement bloqués, des essais progressifs en durée de conduction et en tension VDS sont menés. Il est rapidement constaté que les composants de type p-GaN des deux fournisseurs tiennent le court-circuit pour des durées de conduction bien plus longue qu'attendues. L'auto-réduction du courant de court-circuit est en effet significativement plus élevée que pour les composants normalement passants. La Figure 318 illustre cette auto-réduction du courant de drain ainsi que l'impressionnante tenue en court-circuit avec une durée de conduction de 10 µs pour une tension V_{DS} = 200 V.

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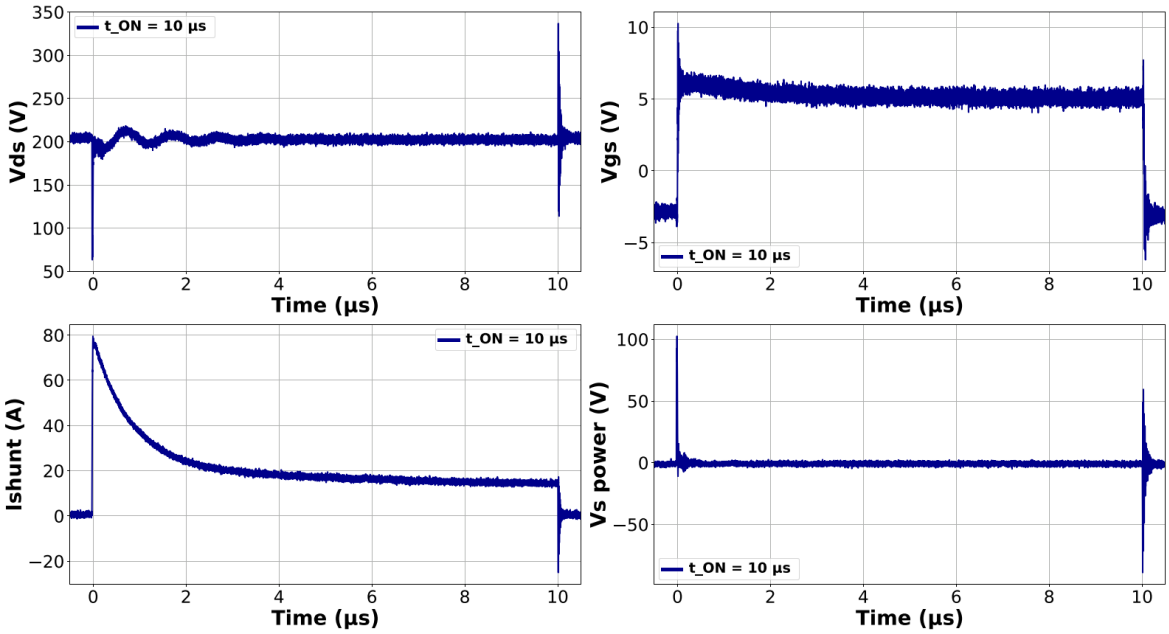

Figure 318: signaux expérimentaux illustrant l'auto-réduction du courant de drain

En matière de polarisation drain-source maximale, les composants de chacun des fournisseurs ne se comportent pas de la même façon avec une tension VDS maximum sans casse de 350 V pour le fournisseur 1 et des essais répétables là où le fournisseur ne peut tenir les courts-circuits en 300 V. Ces plafonds de tensions VDS ont pu être relevés suite aux différentes optimisations mais restent néanmoins en faveur du fournisseur 1.

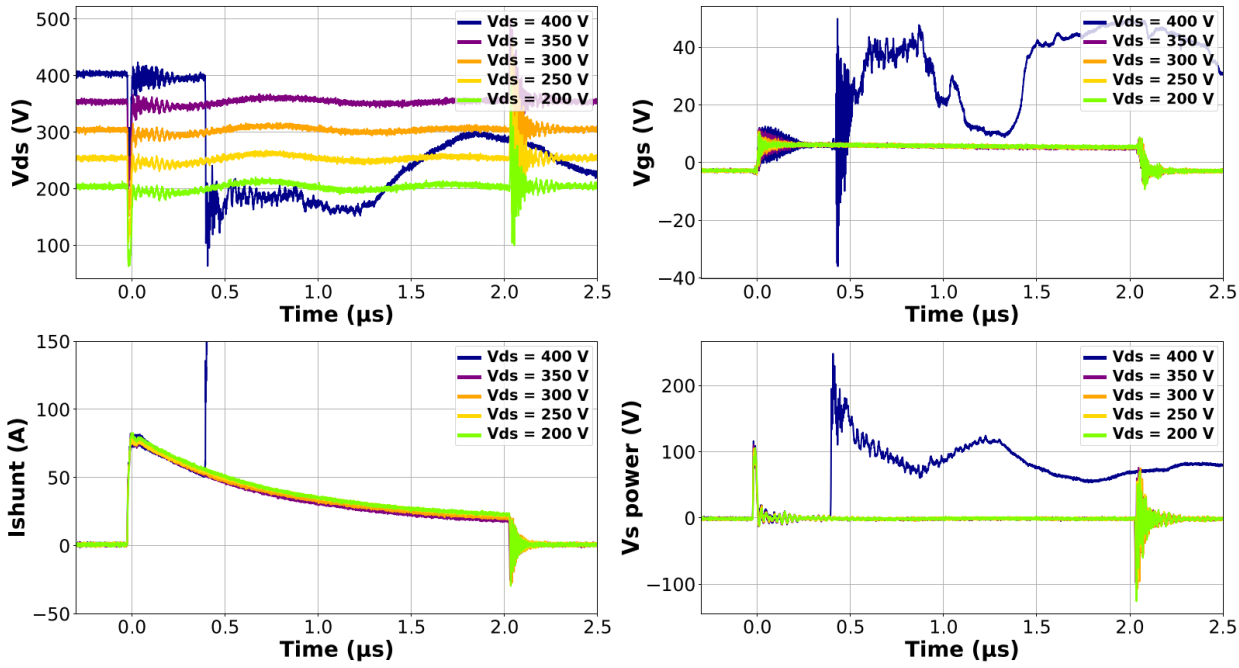

Figure 319: signaux expérimentaux durant une montée en tension VDS progressive, pour un composant de type p-GaN du fournisseur 1

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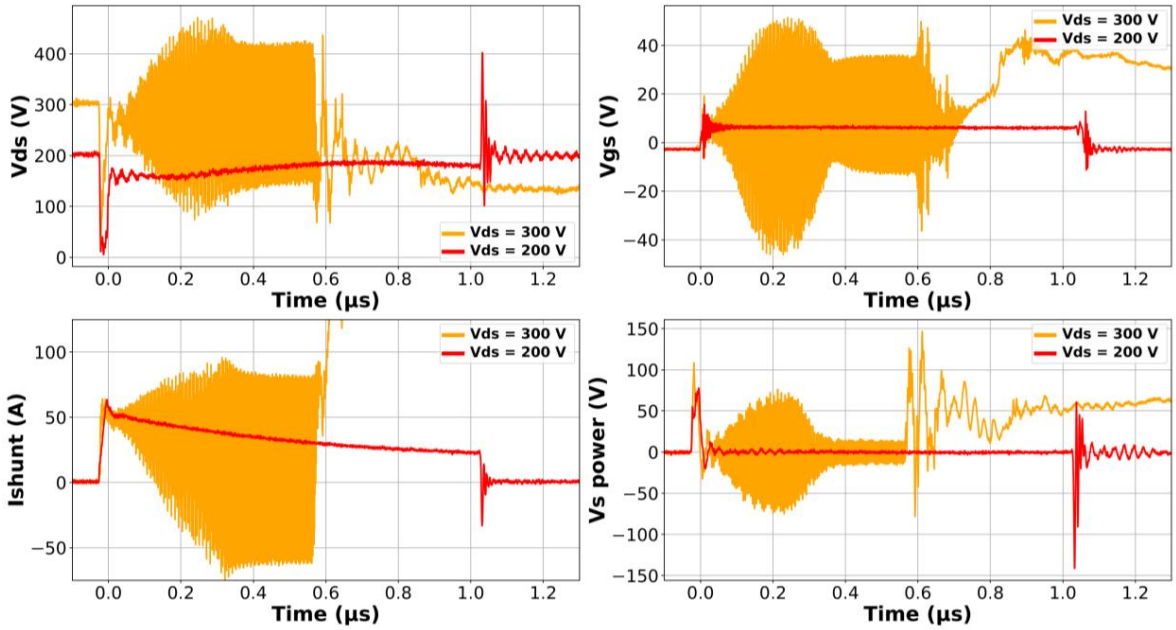

Figure 320: signaux expérimentaux pour une montée en tension VDS jusque 300 V, pour un composant de type p-GaN du fournisseur 2

Si aucune variation dynamique, similaire à celle des composants normalement passant n'est constatée, des variations de la tension de seuil sont constatées durant les caractérisations électriques effectuées entre chaque série de court-circuit.

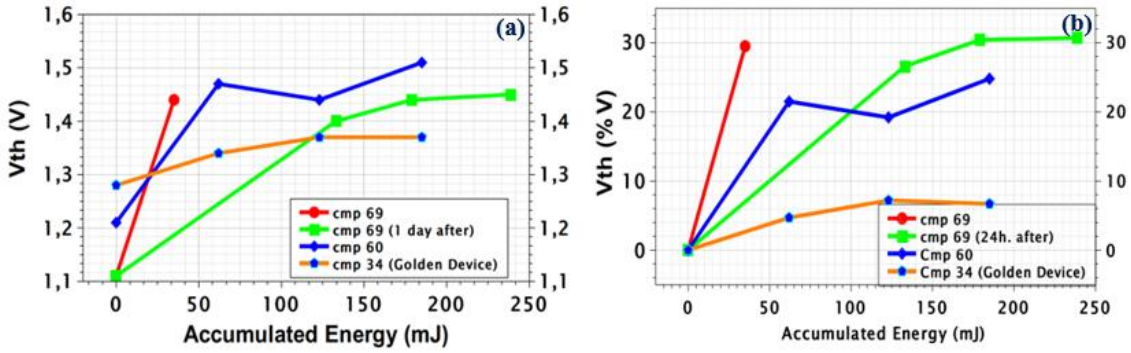

Figure 321: Variation de la tension de seuil V_{th} pour des composants p-GaN provenant du fournisseur 1 en valeur (a-gauche) et en pourcentage (b-droite)

La première observation réside dans le fait que l'application de ces courts-circuits provoque ainsi une variation importante de la tension de seuil V_{th}, atteignant parfois un écart de 30% par rapport à la valeur initiale mesurée avant tout court-circuit.
La deuxième observation est que cette variation n'est pas immuable, comme le montrent les courbes verte et rouge de la Figure 321, qui illustrent l'évolution du composant 69 à un jour d'intervalle. Après 24 heures, V_{th} est revenue à sa valeur initiale. L'application de courts-circuits sur les composants provoque donc un piégeage dans la région de la grille, ce qui entraîne une variation de la tension de seuil V_{th}.
Enfin, pour s'assurer que les variations observées sont bien dues uniquement à l'application de courts-circuits, un composant témoin, appelé « golden device », est utilisé. Ce « golden device » subit les mêmes étapes de caractérisation électrique, mais sans être court-circuité. Ceci permet de vérifier que ce sont bien les courts-circuits qui sont à l'origine de la variation, et non les caractérisations électriques effectuées au B1505. Les caractérisations électriques du composant « golden device » 34 sont effectuées en même temps que celles du composant « court-circuité » numéro 60, afin d'être dans les mêmes conditions de mesure.

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Cet aspect temporel est important, car l'augmentation de la température de la pièce, bien que climatisée, et son impact sur les paramètres électriques des composants doivent être pris en compte lors des mesures.
La plus faible variation du composant témoin, par rapport au composant 60 et aux autres composants court-circuités, prouve que le court-circuit est bel et bien la contrainte majeure provoquant les variations de $_{Vth}$, et non les caractérisations électriques au B1505.
Cependant, une petite variation peut être observée pour le composant du composant témoin. Celle-ci pourrait s'expliquer par la surchauffe de la salle de mesure, dont la climatisation n'est pas parfaite et tolère une variation d'un à deux degrés Celsius.
Les composants p-GaN du fournisseur 2 donnent les mêmes conclusions, à l'image de la Figure 324.

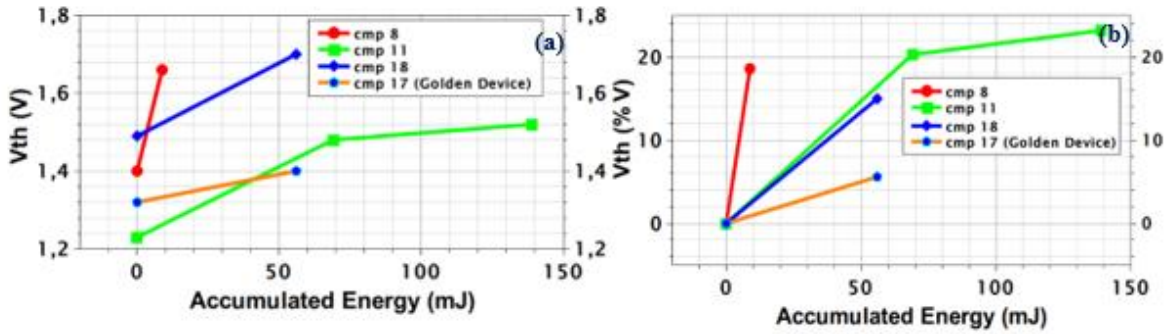

Figure 322: Variation de la tension de seuil V_{th} pour des composants p-GaN provenant du fournisseur 2 en valeur (a-gauche) et en pourcentage (b-droite)

Cette variation de la tension de seuil est accompagnée d'une variation de la résistance à l'état passant R_{DS_ON}. La variation se fait en revanche dans un sens opposé suivant le fournisseur. En effet, à l'image de la Figure 325, les courts-circuits répétitifs appliqués aux composants du fournisseur 1 tendent à augmenter sa résistance R_{DS_ON} tandis qu'ils tendent à la diminuer pour les composants du fournisseur 2.

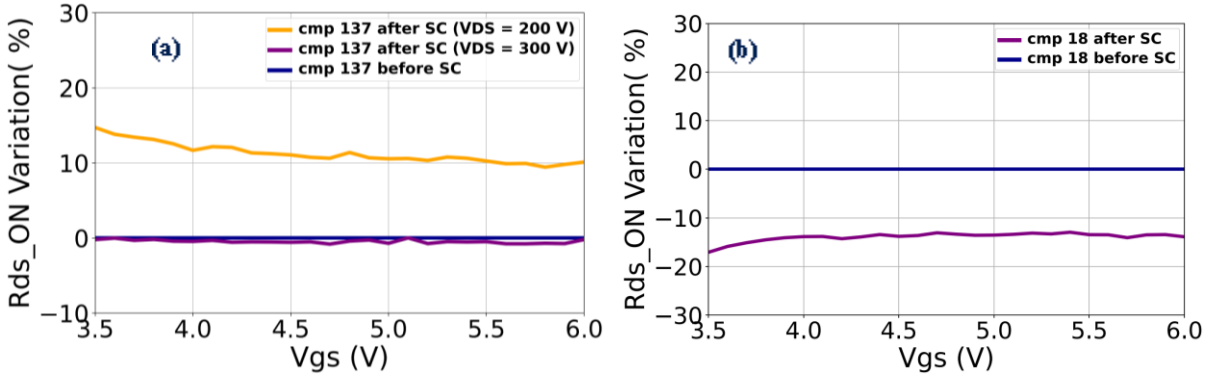

Figure 323: variations de RDS_ON suite aux essais en courts-circuits répétitifs à VDS = 200 V pour des composants de type p-GaN provenant des fournisseurs 1 (a-gauche) et fournisseur 2 (b-droite)

Compte tenu de la limite de tension plus élevée des composants du fournisseur 1, les tests ont été effectués non plus à V_{DS} = 200 V, mais désormais à V_{DS} = 300 V. Le temps de conduction reste inchangé à 1 µs, sauf pour le premier court-circuit, où le temps de conduction est divisé par deux pour s'assurer que le composant sous test peut supporter la polarisation drain-source de 300 V. La figure 33 illustre cette série de courts-circuits répétés. La Figure 324 illustre cette série de courts-circuits répétitifs pour $_{VDS}$ = 300 V, entrecoupés de caractérisations électriques au B1505, avant et après.

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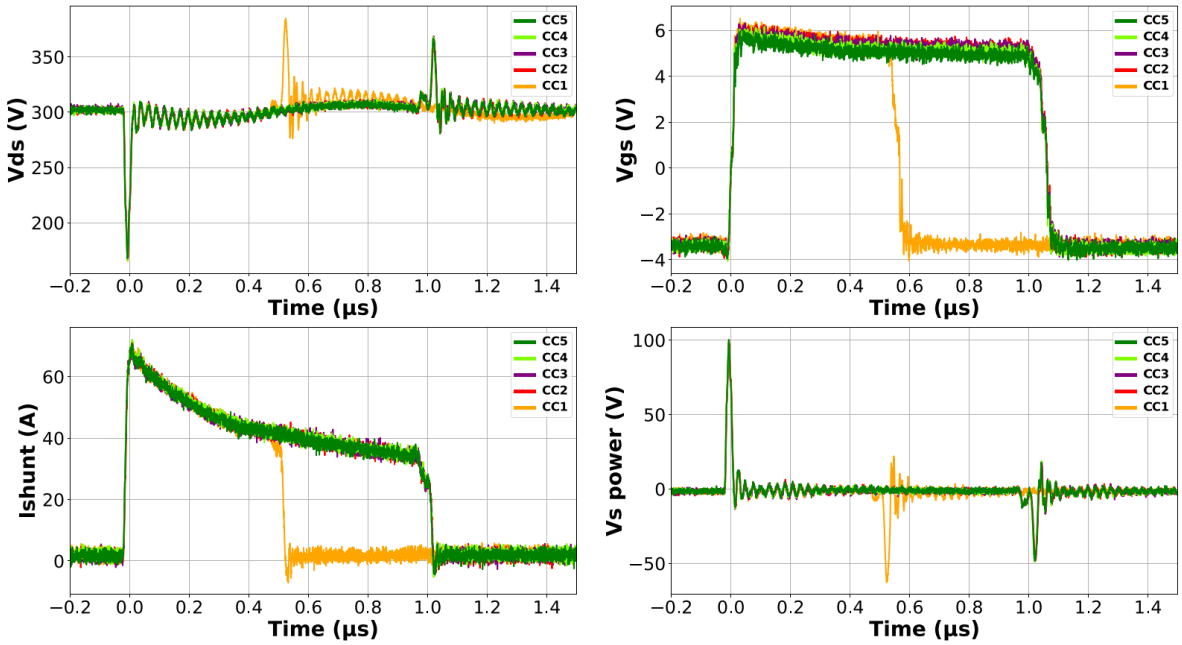

Figure 324: signaux expérimentaux pour une série de courts-circuits répétitifs à V_{DS} = 300 V, pour un composant de type p-GaN du fournisseur 2

A l'inverse de ce qui pouvait être attendu, les impacts constatés précédemment ne sont non seulement pas exacerbés pour une tension V_{DS} supérieure à celle testée précédemment, mais ils sont même réduits. La première conclusion aurait pu être que nous sommes en présence de composants particulièrement robustes. Afin de vérifier cela, de nouveaux tests ont été effectués, en revenant cette fois-ci à V_{DS} = 200 V. Avec une variation de 30 % pour V_{DS} = 200 V, en comparaison d'une absence de variation significative à V_{DS} = 300 V par rapport au composant témoin tel qu'illustré sur la Figure 325, le résultat est sans équivoque : une polarisation drain-source V_{DS} de 200 V est plus impactante qu'une polarisation augmentée à 300 V.

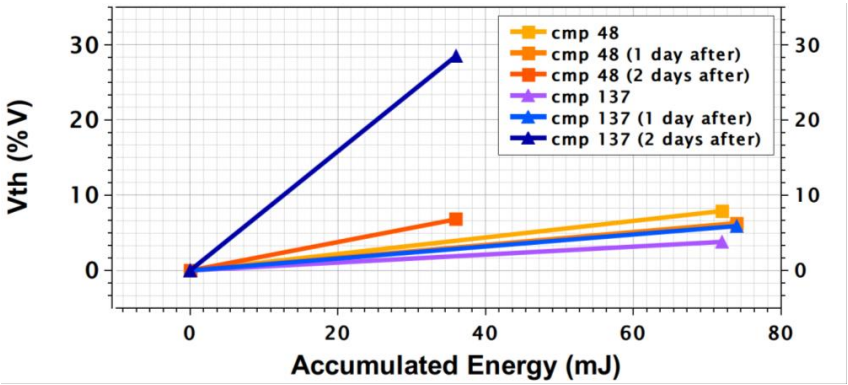

Figure 325: Absence ou présence de variation de V_{th} suivant le niveau de polarisation V_{DS} = 200 V ou V_{DS} = 300 V

Plusieurs types de casse ont pu être appréhendés. On distingue des casses due à l'accumulation de courts-circuits répétitifs à l'image de la Figure 326 ou le composant casse en pleine conduction alors qu'il avait parfaitement réussi à tenir le précédent court-circuit, aux caractéristiques identiques, des casses due à une limite de tension, faisant vraisemblablement intervenir d'autres mécanismes physiques (Figure 327) et enfin des casses du fait d'une remise en conduction intempestive du composant dont on peut supposer l'origine différente des deux premiers types de casse, à l'image de la Figure 328.

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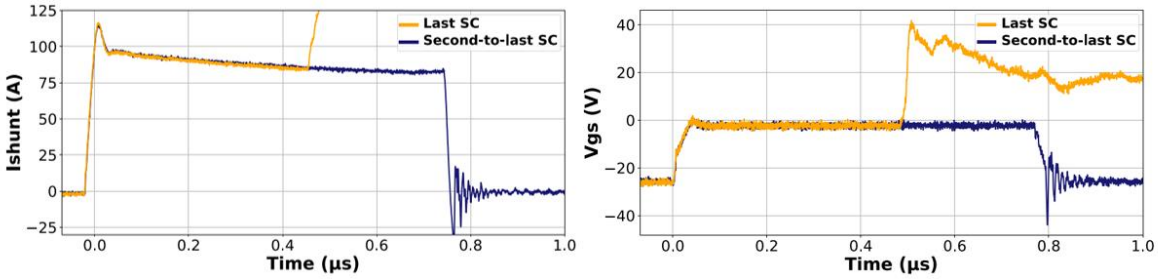

Figure 326: Casse du composant du fait d'une accumulation de courts-circuits répétitifs

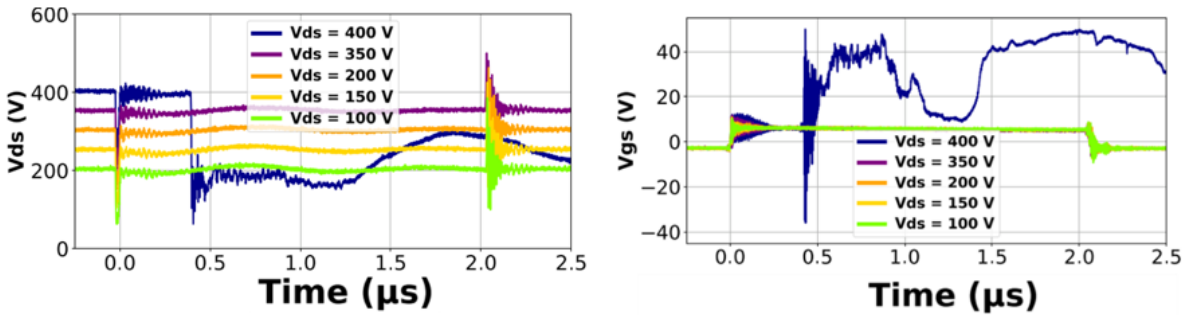

Figure 327: case du composant du fait d'une trop grande polarisation drain - source

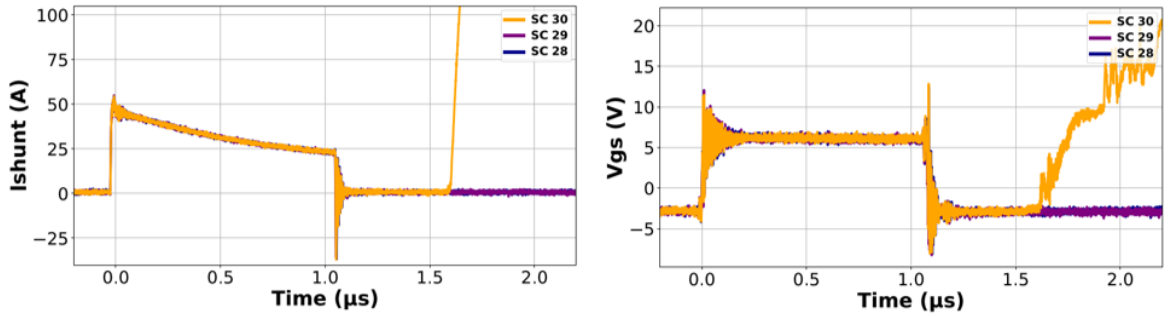

Figure 328: casse du composant du fait d'une remise en conduction intempestive malgré un court-circuit tenu

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6.4 Conclusion & Perspectives

Cette thèse aura exploré en profondeur les phénomènes de court-circuit affectant les HEMT GaN 650 V et met en lumière les défis et perspectives liés à leur fiabilité et robustesse. Après un état des lieux de l'électronique de puissance, marquée par la transition vers des technologies à large bande interdite comme le GaN, plusieurs mécanismes de défaillance en court-circuit ont été analysés, notamment l'emballement thermique, les interactions champ-charge, l'ionisation par impact et les oscillations destructrices. Ces analyses ont clarifié un état de l'art auparavant ambigu, ouvrant la voie à une conception optimisée de bancs de test pour mieux évaluer ces phénomènes et mieux comprendre les mécanismes de défaillances des composants lors des courts-circuits.

Le banc expérimental initial, bien que le design et la conception aient été soignés, a nécessité de nombreuses optimisations, notamment pour le traitement des courants en mode commun. Une seconde version a été développée, s'éloignant de la configuration carte mère-carte fille, et a permis d'améliorer encore un peu plus stabilité des signaux V_{DS} et V_{GS}. Cela a également d'être en adéquation avec les futures normes JEDEC en matière de standards de test en court-circuit.

Les essais sur les composants d-mode ont révélé des variations dynamiques du niveau de saturation du courant de court-circuit et des augmentations précurseurs de défaillances. Des variations significatives de V_{th} ont pu être observées. Les composants p-GaN quant à eux ont démontré une auto-réduction du courant de drain particulièrement efficace, leur permettant une robustesse accrue, mais avec des variations de V_{th} plus marquées, allant jusqu'à 30 % de différence par rapport à la valeur initiale. Une observation surprenante a révélé qu'une polarisation V_{DS} = 300 V était moins délétère qu'à 200 V. Ce phénomène reste aujourd'hui encore inexpliqué. Les différences de comportement en court-circuit des composants p-GaN suivant le fournisseur pourraient s'expliquer par des capacités C_{iss} et C_{oss}, plus élevée pour le fournisseur 1.

L'emplacement des puces sur le wafer, démontré comme hautement impactant pour les puces d-mode et influençant des paramètres comme le dopage, la hauteur d'épitaxie ou les contraintes mécaniques, est un facteur clé encore à explorer. L'analyse des composants cascode, non priorisée du fait de la nécessaire optimisation du banc pour les composants p-GaN dans cette étude, offrirait aussi des perspectives intéressantes. Enfin, des investigations complémentaires, comme la microscopie électronique par transmission (TEM), la photoluminescence résolue dans le temps (TRPL) ou la spectroscopie transitoire des niveaux profonds (DLTS), pourraient approfondir la compréhension des mécanismes de défaillance, notamment ceux induits par les électrons chauds. Cette thèse offre ainsi des pistes claires pour améliorer la robustesse des composants GaN et affiner les méthodologies de test.

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