Design toolkit for PCB-based power electronic systems

Bahaeddine Ben Hamed

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Design toolkit for PCB-based power electronic systems

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Abstract

Design toolkit for PCB-based power electronic systems

Power converters are complex systems involving tightly coupled multiphysics phenomena, including electromagnetic behavior, thermal effects, and material interactions. Their design is particularly challenging due to the heterogeneous nature of components, materials, voltage levels, and cooling strategies. In addition, growing demands for performance, miniaturization, and reliability further increase the complexity of the development process.

Modern electronic computer-aided design (ECAD) and simulation tools have significantly advanced. They offer improved accuracy, usability, and the ability to model detailed behaviors. However, the design workflow remains fragmented. Different specialized tools are used for each task, requiring multiple expert profiles, complex data handling, and raising compatibility issues between proprietary formats. This fragmentation slows down the process, especially when iterating between electrical, thermal, and mechanical aspects.

Physical prototyping represents another major bottleneck, particularly for advanced technologies like embedded PCBs. Lead times can reach several months, with high associated costs. Virtual prototyping is a promising alternative, but it remains underdeveloped in power electronics compared to fields like microelectronics.

This thesis introduces a design tool that automatically generates virtual prototypes of power converter PCBs. The goal is to produce reliable electro-thermal simulation models directly from PCB layout data, reducing reliance on physical prototypes. The tool integrates multiple steps: layout extraction, geometry simplification, electromagnetic modeling, thermal finite element analysis, and the generation of electronic schematics for circuit simulation.

Experimental validations were conducted on both simple and complex layouts. The tool successfully simulated parameters that are otherwise difficult to measure,

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such as junction temperature and switching waveforms. Results were compared to measurements from physical prototypes, validating the credibility of the generated models.

Performance analysis has shown that the thermal FEM (Finite Element Method) simulation stage accounts for the majority of computation time, consuming up to 95%. This is primarily due to the complexity of the transient FEM simulation and the mesh. However, this time consumption is still relatively minor compared to the time needed for hardware prototyping. The ability to explore designs before fabrication and access internal variables highlights the practical benefits of the proposed virtual prototyping approach.

Some limitations remain: dependence on proprietary software (Altium, ANSYS), meshing quality issues, partially automated electronic schematics' generation, and the need for manual input of boundary conditions. Future improvements could include adopting open standards like IPC-2581 and integrating open-source tools to improve interoperability and long-term sustainability.

In conclusion, this thesis demonstrates the potential of automated, layout-based virtual prototyping in embedded power electronics. The proposed tool is a solid proof of concept for a more unified, faster, and reliable design process. It lays the groundwork for next-generation ECAD environments where virtual prototypes can effectively complement or replace physical ones during early design stages.

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Résumé

Boîte à outils de conception pour les systèmes électroniques de puissance à base de circuits imprimés (PCB)

Les convertisseurs de puissance sont des systèmes complexes faisant intervenir des phénomènes multiphysiques couplés : comportement électromagnétique, effets thermiques et interactions matériaux. Leur conception est rendue difficile par la diversité des composants, matériaux, niveaux de tension et stratégies de refroidissement utilisés. À cela s'ajoutent des exigences croissantes en matière de performance, de miniaturisation et de fiabilité.

Les outils actuels de CAO électronique (ECAD) et de simulation ont beaucoup évolué. Ils sont plus précis, conviviaux et capables de modéliser des comportements détaillés. Toutefois, le processus de conception reste morcelé. Différents outils spécialisés sont utilisés à chaque étape, nécessitant des expertises variées, une gestion complexe des données, et impliquant des problèmes d'interopérabilité entre formats propriétaires. Ce cloisonnement ralentit le développement, notamment lors des itérations entre les aspects électriques, thermiques et mécaniques.

Le prototypage physique représente également un frein, en particulier pour les technologies avancées comme les PCB embarqués. Les délais de fabrication peuvent atteindre plusieurs mois, avec des coûts élevés. Le prototypage virtuel apparaît ainsi comme une alternative prometteuse, mais encore peu développée dans le domaine de l'électronique de puissance.

Cette thèse propose un outil de conception permettant de générer automatiquement des prototypes virtuels de cartes électroniques de convertisseurs. L'objectif est de produire des modèles de simulation électro-thermiques fiables à partir du layout PCB, en réduisant le recours au prototypage physique. L'outil développé intègre plusieurs étapes : extraction du layout, simplification géométrique, modélisation électromagnétique, simulation thermique par éléments finis et génération de schéma

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électronique pour la simulation de circuits.

Les validations expérimentales menées sur des cartes simples et complexes ont confirmé la pertinence des modèles générés. L'outil permet de simuler des paramètres difficiles à mesurer comme la température de jonction ou les formes d'onde de commutation. Les résultats ont été comparés à des mesures sur prototypes réels, renforçant la crédibilité de l'approche.

L'analyse des performances montre que la simulation thermique est l'étape la plus coûteuse en temps (jusqu'à 95% du calcul total), mais reste négligeable face aux délais de fabrication. La capacité à explorer des variantes avant fabrication, et à accéder à des variables internes, montre la valeur pratique du prototypage virtuel.

Des limites subsistent : dépendance à des logiciels propriétaires, problèmes de maillage, génération de netlistes partiellement automatisée, et absence de prise en compte automatique des conditions environnementales. Des pistes d'amélioration incluent l'adoption de standards ouverts (IPC-2581) et l'intégration d'outils open-source.

En conclusion, cette thèse démontre le potentiel du prototypage virtuel automatisé basé sur le layout dans le domaine de l'électronique de puissance embarquée. L'outil développé constitue une preuve de concept solide pour une approche unifiée, plus rapide et plus fiable du processus de conception.

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Résumé en français

Introduction générale

Au cours des dernières décennies, l'électronique de puissance a connu une transformation profonde, portée par l'émergence de nouvelles technologies de semi-conducteurs, la miniaturisation des composants passifs, et une demande croissante en densité de puissance et en rendement. Dans ce contexte, les outils classiques de conception de convertisseurs deviennent progressivement inadaptés. L'approche séquentielle, fondée sur l'alternance entre phases de conception manuelle et prototypage physique, se heurte à des limitations de plus en plus contraignantes : temps de développement allongés, coûts de prototypage élevés, et difficulté d'intégrer des phénomènes multiphysiques dès les premières étapes de conception.

Face à ces défis, le prototypage virtuel s'impose comme une solution prometteuse. Il s'agit de remplacer, autant que possible, les prototypes physiques par des représentations numériques du système, capables de simuler son comportement thermique, électromagnétique et électrique. Mais malgré les avancées en simulation, l'adoption du prototypage virtuel dans les environnements industriels reste limitée. En effet, il n'existe à ce jour aucun outil intégré permettant de passer directement de la conception d'un PCB à une modélisation multiphysique exploitable. Les ingénieurs doivent encore jongler avec plusieurs logiciels hétérogènes, reconstruire à la main les géométries, reparamétrer les matériaux, et opérer des choix d'architecture sur la base d'hypothèses incertaines.

L'objectif de ce travail de doctorat est de concevoir un nouvel outil de conception pour les PCBs embarqués dédiés à l'électronique de puissance, capable d'intégrer nativement les aspects de modélisation thermique et électromagnétique. Cet outil doit permettre d'automatiser la génération de prototypes virtuels à partir des fichiers de conception, et de guider efficacement les ingénieurs dans leurs

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décisions d'architecture.

Pour atteindre cet objectif, la démarche de recherche s'est appuyée sur quatre axes majeurs :

- une analyse critique des pratiques de conception existantes dans l'industrie
- la définition d'une architecture logicielle orientée multiphysique
- le développement de méthodes d'extraction automatique de modèles à partir du layout PCB
- la validation expérimentale sur plusieurs prototypes physiques.

Le mémoire s'organise autour de ces axes, répartis en cinq chapitres.Le chapitre 1 présente les principales contraintes de conception spécifiques aux convertisseurs de puissance. Le chapitre 2 propose un état de l'art sur les modèles existants et les outils de simulation. Le chapitre 3 décrit l'architecture du prototype logiciel développé. Le chapitre 4 valide expérimentalement les modèles générés, tandis que le chapitre 5 illustre l'utilisation de l'outil sur des cas concrets de conception.

Chapitre 1 – Contexte et motivations

L'électronique de puissance occupe une place centrale dans les systèmes énergétiques modernes, qu'il s'agisse de l'électrification des transports, des énergies renouvelables ou des applications industrielles à haute efficacité. Cette évolution s'accompagne de nouvelles exigences : compacité accrue, intégration poussée, et maîtrise des phénomènes parasites qui deviennent prépondérants à mesure que les fréquences de commutation augmentent.

Dans ce contexte, les circuits imprimés (PCBs) ne sont plus de simples supports passifs ; ils deviennent des éléments fonctionnels à part entière, dont l'architecture influence directement les performances électriques, thermiques et électromagnétiques du système. Le rôle du concepteur de PCB est donc profondément transformé : il doit désormais anticiper et intégrer des considérations multiphysiques dès les premières étapes de conception.

Or, les outils traditionnels de conception assistée par ordinateur (CAO) ne permettent pas cette intégration. Les flux de travail actuels restent largement séquentiels et cloisonnés. Ils nécessitent de multiples allers-retours entre différents logiciels pour simuler séparément les aspects thermiques, électriques et électromagnétiques, souvent après la fabrication de prototypes. Cette approche engendre une perte de

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temps considérable, des coûts élevés, et surtout une faible réactivité dans la phase de conception.

C'est dans ce cadre que le concept de prototypage virtuel prend tout son sens. Il s'agit d'élaborer des modèles numériques du système capables de reproduire avec précision les phénomènes physiques essentiels, et ce avant même la fabrication du premier prototype. Le prototypage virtuel promet une réduction significative des temps de développement, une meilleure optimisation des performances, et une plus grande robustesse face aux aléas industriels.

Cependant, malgré les progrès des outils de simulation, l'adoption du prototypage virtuel reste marginale dans les environnements industriels. Cela s'explique par plusieurs verrous technologiques et organisationnels :

- l'absence d'outils intégrés capables de lire directement les fichiers de conception PCB et d'en déduire des modèles physiques exploitables

- la complexité des phénomènes multiphysiques à modéliser conjointement

- le manque de méthodologies robustes pour intégrer ces modèles dans les flux de conception

Ce chapitre établit les fondements techniques et physiques à considérer lors de la conception de circuits imprimés destinés aux convertisseurs de puissance. Il analyse les phénomènes dominants intervenant dans ce contexte : les contraintes thermiques liées aux pertes de conduction et de commutation, les effets de la commutation rapide sur l'intégrité des signaux, et les problèmes de compatibilité électromagnétique (CEM) induits par les boucles de courant, les fronts raides et les impédances parasites.

Le chapitre met également en lumière le rôle critique du layout PCB dans la performance globale du système, soulignant que de nombreux choix technologiques ne peuvent être validés que par une compréhension fine des interactions multiphysiques.

Cette analyse souligne ainsi la nécessité d'une approche intégrée de la conception, dans laquelle le circuit imprimé n'est pas seulement un support physique mais un acteur actif de la performance électrique, thermique et CEM.

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Chapitre 2 – État de l'art des modèles et outils de simulation multiphysique

Ce chapitre explore les méthodologies actuelles et les outils utilisés dans la conception des systèmes d'électronique de puissance, en mettant l'accent sur les aspects liés à la modélisation, la simulation et l'optimisation multiphysique.

Il s'ouvre sur un rappel des fondamentaux du processus de conception d'un convertisseur de puissance, qui commence par la définition des spécifications techniques (tensions, courants, rendement, densité de puissance, contraintes thermiques, CEM, etc.). Ces spécifications conditionnent les choix de topologie, de composants, de stratégies de commande, et d'agencement physique du convertisseur. Le processus est itératif, visant à affiner le design à chaque cycle, souvent à l'aide de simulations.

Une attention particulière est ensuite accordée à l'intégration de modèles numériques et d'outils de simulation avancés. La simulation devient indispensable pour explorer les performances thermiques, électriques et électromagnétiques. Le chapitre présente plusieurs techniques courantes :

- L'utilisation de modèles électro-thermiques couplés pour prédire les pertes et les élévations de température.
- Les modèles comportementaux ou de jumeaux numériques permettant d'anticiper le comportement global du système avant la fabrication.
- L'intégration de solveurs multiphysiques pour simuler les phénomènes couplés dans des environnements complexes.

Le texte insiste sur le rôle critique des outils tels que LTspice, PLECS, Simulink, ou encore Ansys, qui permettent d'évaluer des stratégies de commande, les pertes de commutation, les régimes transitoires et les performances thermiques. Ces outils, bien que puissants individuellement, souffrent d'un manque d'interopérabilité et d'automatisation dans la chaîne complète de conception, en particulier lorsqu'il s'agit de passer du layout PCB à une modélisation fidèle.

Le chapitre discute également les tendances émergentes dans les pratiques de conception, telles que :

- L'utilisation de jumeaux numériques (digital twins) pour suivre l'évolution du système pendant son cycle de vie .
- La conception basée sur des modèles paramétriques automatisés .

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- L'intégration de bibliothèques de matériaux et composants dans des workflows personnalisés.

Enfin, le chapitre souligne les limites persistantes des outils actuels, notamment:

- Le manque de standardisation entre logiciels de CAO, simulateurs physiques et plateformes de prototypage.
- L'absence de passerelles automatisées entre le design géométrique et la simulation multiphysique.
- L'incapacité à gérer efficacement l'optimisation multidomaine dès les premières étapes du développement.

Ces constats motivent la suite de la thèse, qui vise à concevoir un outil dédié de prototypage virtuel multiphysique pour les PCB de puissance, capable de connecter les différentes briques de la chaîne de conception dans un environnement unifié, automatisé, et adapté aux contraintes spécifiques de l'électronique de puissance.

Chapitre 3 – Génération automatique de prototypes virtuels

Le troisième chapitre s'attache à formaliser le processus par lequel l'outil développé transforme un fichier de conception PCB en un prototype virtuel multiphysique exploitable (synopsis presenté dans la figure 1). Ce processus repose sur une série d'étapes structurées visant à extraire, interpréter et enrichir les données de layout, pour produire des modèles thermiques, électriques et électromagnétiques adaptés à l'analyse numérique.

L'organigramme de l'algorithme implémenté dans le logiciel eCAD, chargé de la génération d'un prototype virtuel, est présenté à la figure 2. Il débute par l'importation des fichiers de CAO, à partir desquels sont extraits les éléments géométriques de la carte : pistes, vias, plans de masse, composants, contours mécaniques et empilement des couches. L'outil reconstruit ensuite une représentation topologique et géométrique cohérente, à l'aide d'un moteur de parsing robuste intégrant des règles de reconnaissance automatique.

Une fois la géométrie reconstruite, le système procède à l'annotation physique du layout. Cette étape est essentielle : elle permet d'associer à chaque entité du PCB (trace, composant, plan de cuivre...) des propriétés telles que la conductivité thermique, la résistivité électrique, la dissipation thermique des composants ou encore

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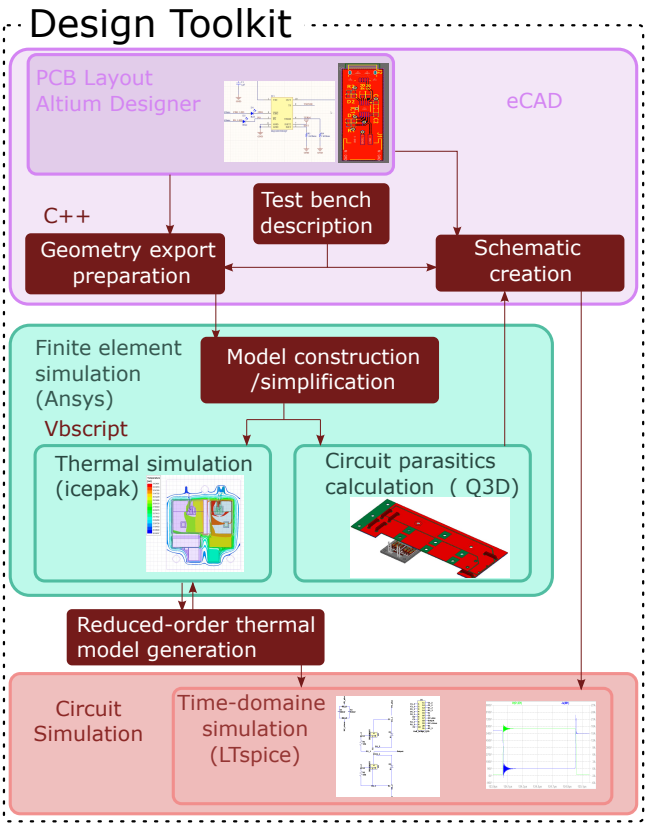

Figure 1: Synopsis de l'outil de génération du prototype virtuel.

les courants nominaux. Ces annotations peuvent être récupérées automatiquement (via des bases de données ou des bibliothèques de composants) ou bien définies par l'utilisateur. Le chapitre détaille ensuite la manière dont les modèles physiques sont dérivés de cette représentation enrichie :

- Modèles thermiques : construction du modèle 3D, comme illustré à la figure 4, puis génération de réseaux thermiques équivalents de type RC pour une analyse rapide, à partir de simulations 3D par éléments finis (FEM) (figure 3).

- Modèles électromagnétiques : construction de géométries 3D pour la simulation des champs (EM quasi-statiques).

- Modèles électriques : extraction de netlists depuis la topologie du PCB, génération de modèles SPICE avec les inductances parasites, capacités d'interconnexions, résistances de trace et effets de peau intégrés.

L'un des apports originaux de ce travail est l'automatisation de la segmentation thermique, permettant de diviser intelligemment le PCB en sous-domaines isothermes, adaptés à la génération de modèles thermiques de type compact. Cela évite un maillage trop fin, tout en conservant une bonne fidélité du modèle. Le chapitre présente également la structure du métamodèle de prototype virtuel, qui encapsule tous les

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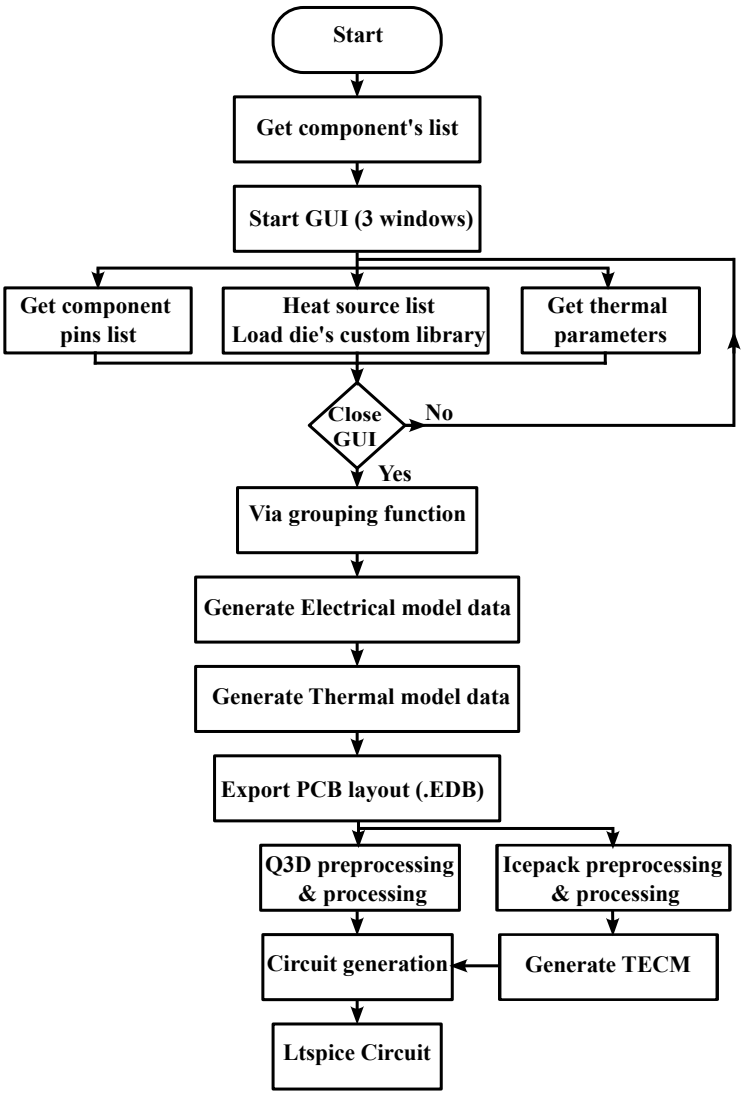

Figure 2: Organigramme pour l'algorithme du module implementé dans le logiciel eCAD Altium.

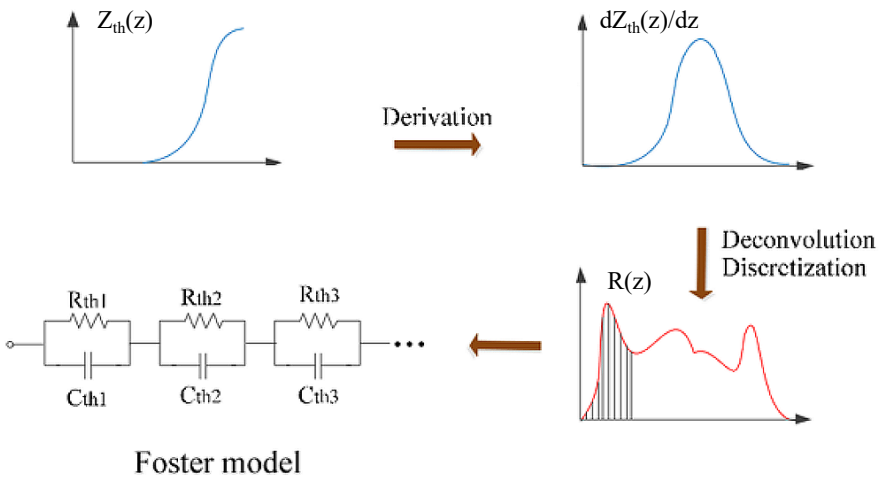

Figure 3: Approche d'identification du réseau thermique: algorithme de calcul du circuit équivalent de Foster [1, 2]

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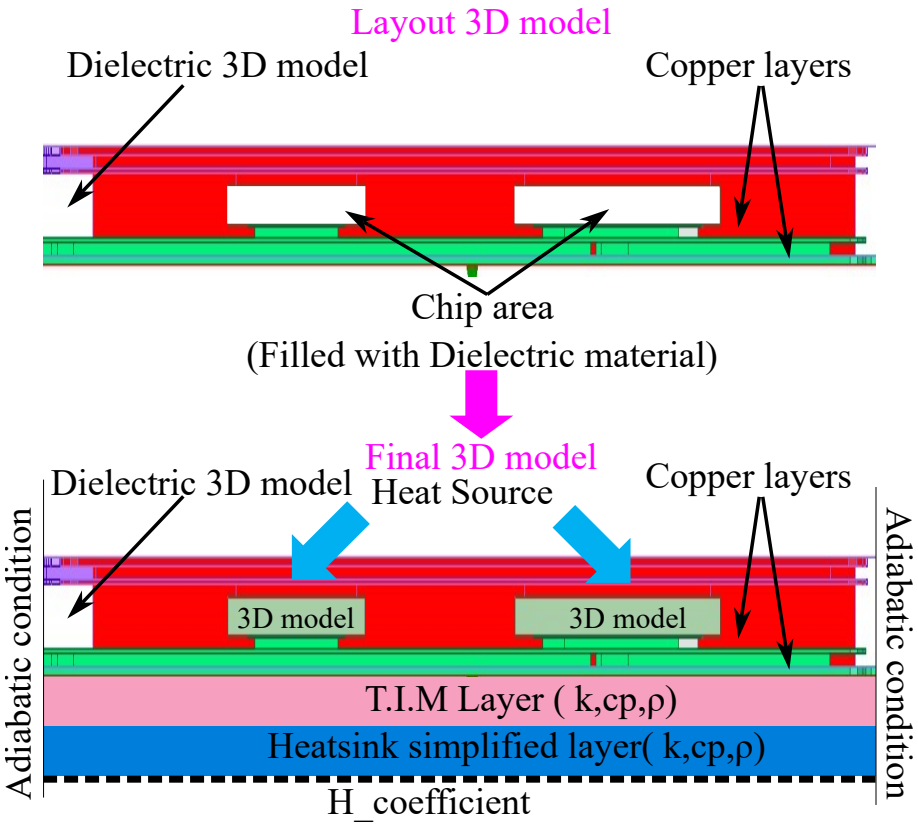

Figure 4: Transformation from the PCB layout 3D model to the final Thermal 3D Model.

fichiers de simulation, les paramètres physiques, les métriques calculées, et les relations entre entités du layout. Ce métamodèle joue un rôle clé dans l'évaluation comparative de variantes de conception. Enfin, plusieurs exemples illustrent l'efficacité du processus, avec des temps de génération très courts (quelques dizaines de secondes) pour des modèles intégrant plus de cent composants. Cette capacité à produire des prototypes virtuels à la volée ouvre la voie à une exploration rapide de l'espace de conception, ce qui constitue un levier majeur d'optimisation pour les ingénieurs.

Ce chapitre constitue ainsi la pierre angulaire de la plateforme développée, en démontrant que la génération automatisée de modèles multiphysiques est non seulement possible, mais également suffisamment robuste et rapide pour un usage en environnement industriel.

Chapitre 4 – Validation expérimentale du prototype virtuel

Ce chapitre est consacré à la validation expérimentale des modèles électriques et thermiques développés dans les chapitres précédents, ainsi qu'à leur intégration dans un modèle couplé électro-thermique. L'objectif est de vérifier la capacité du

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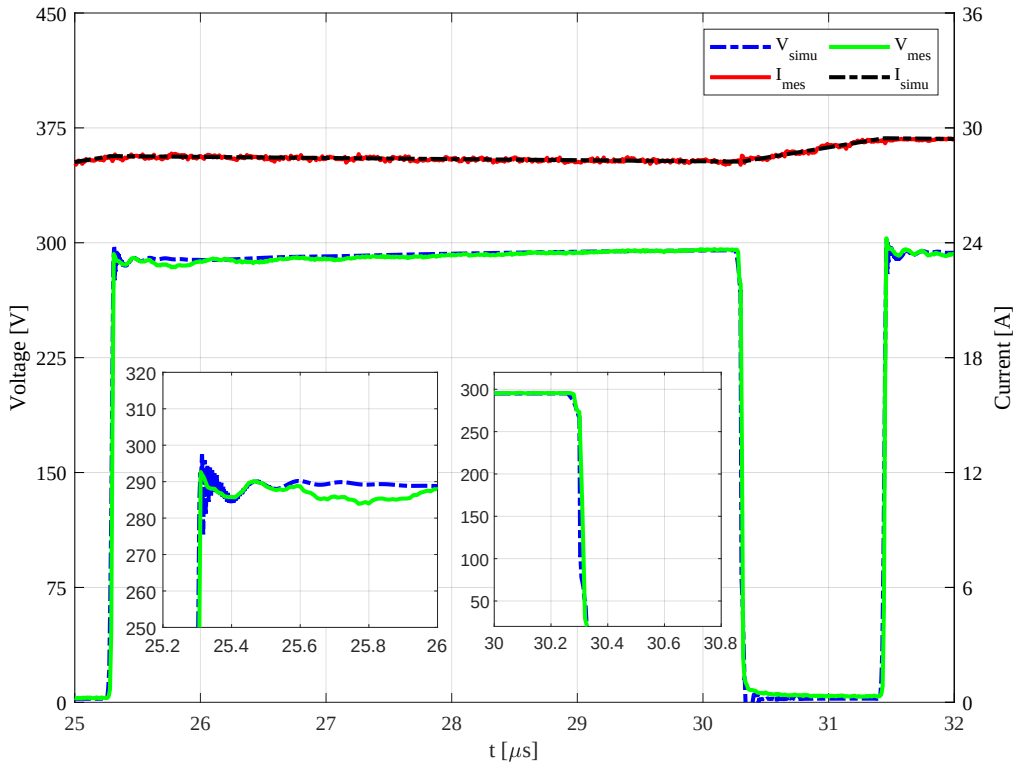

Figure 5: Exemple de forme d'onde à double impulsion.

prototype virtuel à reproduire fidèlement les comportements physiques observés sur différentes cartes électroniques de test. Plan de validation La méthodologie de validation repose sur trois niveaux :

1. Validation électrique :

   - Mesure d'impédance électrique : pour évaluer la justesse du modèle de parasites de routage.
   - Test à double impulsion (DPT) : pour valider les dynamiques de commutation du circuit simulé (figure 5).

2. Validation thermique :

   - Mesures d'impédance thermique sur une seule puce : pour évaluer le modèle thermique élémentaire.
   - Mesures multi-puces : pour tester la précision du modèle en présence de couplages thermiques croisés.

3. Validation électro-thermique :

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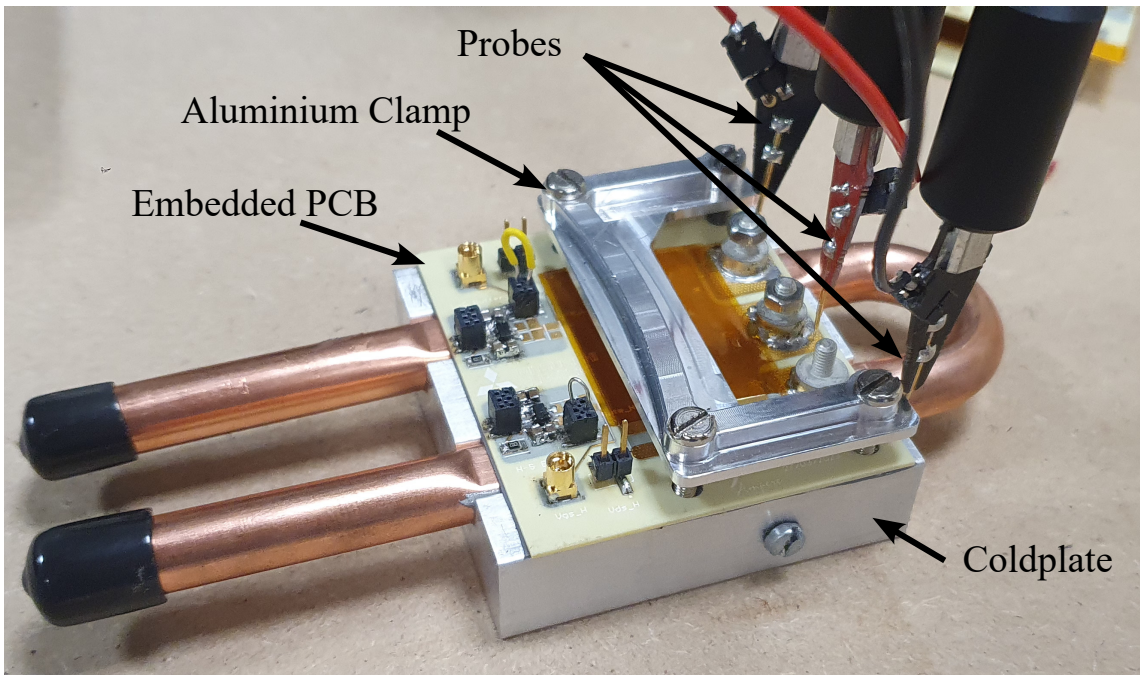

Figure 6: Montage de caractérisation électrique utilisant le traceur de courbes B1505A (équipé du module B1513C HVSMU) sur le composant DUT ④.

- Test de calorimétrie : pour mesurer l'efficacité énergétique globale du système.

Véhicules de test (DUT)

Cinq prototypes de cartes électroniques (DUT 1 à 5) ont été conçus, intégrant différents types de composants (Si, SiC, IGBT, MOSFET) et technologies (circuits discrets ou composants embarqués). Ils permettent de tester les modèles dans divers contextes :

- DUT 1 : une seule puce SiC embarquée dans une structure à deux couches de cuivre. Utilisé principalement pour la validation thermique élémentaire.

- DUT 2 : demi-pont de 4 puces (2 IGBT + 2 diodes) embarquées, utilisé pour la validation électrique (impédance, DPT) et thermique (y compris les effets de couplage).

- DUT 3 : demi-pont basé sur deux composants discrets en boîtier TOLL. Il permet d'examiner les limites des modèles dans des cas où les paramètres internes des boîtiers sont moins connus.

- DUT 4 et 5 : variantes embarquées du DUT 3, avec deux puces SiC. La différence réside dans l'orientation des puces (classique vs. flipped), permettant

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	Classic configuration (DUT ④)			Flipped configuration (DUT ⑤)		
	Measurement	Simulation	Error	Measurement	Simulation	Error
C_{Dc+}	69 pF	75 pF	8.7 %	93 pF	101 pF	8.6 %
C_{Dc-}	81.4 pF	81 pF	0.5 %	106 pF	105 pF	1 %
C_{AC}	60 pF	56 pF	6.6 %	4.3 pF	5.6 pF	30 %
C_{par,OSS_HS}	25.5 pF	27 pF	6 %	26.5 pF	29 pF	9 %
C_{par,OSS_LS}	139 pF	131 pF	6 %	150 pF	151 pF	0.3 %

Table 1: Mesure de capacité pour la validation d'un demi-pont embarqué : cas des composants DUT ④ et ⑤.

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de tester l'influence de cette orientation sur les performances électriques et thermiques.

Validation électrique

La validation du modèle électrique comprend notamment :

- La caractérisation d'impédance : réalisée avec un analyseur Keysight E4990 et une sonde dédiée, sur la boucle de puissance du DUT 2. Les modèles de routage sont générés automatiquement, sans ajustements manuels. Cette approche permet une extraction rapide des éléments parasites via Q3D Extractor.

- Le test à double impulsion : comparant les formes d'onde simulées et mesurées des tensions de commutation. Il permet d'évaluer la précision temporelle du modèle.

- Validation des capacités parasites : Un volet complémentaire de la validation électrique porte sur la mesure des capacités parasites des DUTs 4 et 5 (configuration de mesure illustrée à la figure 6, résultats synthétisés dans le tableau 1). Ces mesures, effectuées à l'aide d'un analyseur de courbes Keysight B1505A, permettent d'évaluer la fidélité des modèles générés automatiquement par le flux de conception, en ce qui concerne les capacités parasites différentielles et communes. Les résultats expérimentaux sont en bon accord avec les simulations, avec des écarts relatifs généralement inférieurs à 10%.

Ces résultats valident les modèles de capacité extraits automatiquement à l'aide de l'outil, et mettent en évidence l'importance ainsi que la dépendance des paramètres physiques et géométriques du layout sur la précision des résultats du prototype virtuel.

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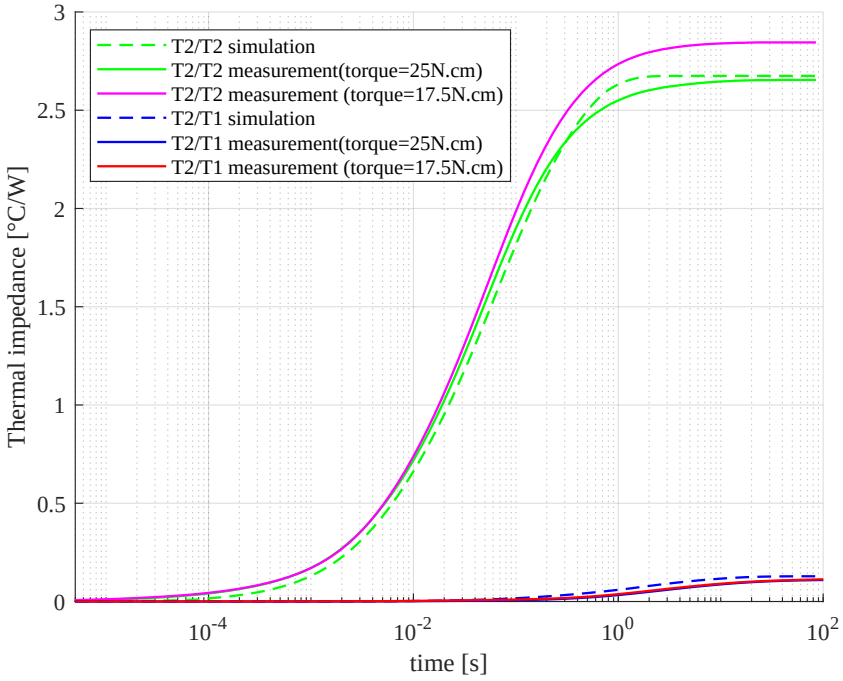

Figure 7: Comparaison de l'impédance thermique entre simulation et expérience pour le composant DUT ④. Deux séquences sont présentées : T_1 actif (T2, D1, D2 : inactifs) et T2 actif (T1, D1, D2 : inactifs). T1/T1 correspond à l'impédance d'auto-échauffement et T1/D1 à l'impédance de couplage thermique de D1 lorsque T1 est actif.

Validation thermique

La validation thermique est centrée sur la comparaison entre les mesures d'impédance thermique expérimentales et les simulations issues du prototype virtuel.

- Pour les mesures sur une seule puce, on utilise un protocole statique à quatre points pour évaluer la résistance thermique entre la jonction de la puce et les différentes couches du PCB.

- Les tests effectués sur des structures multi-puces, dont un exemple de mesure est présenté à la figure 7, permettent d'observer les effets de couplage thermique entre puces adjacentes. Ces résultats valident la capacité du modèle à représenter avec précision les transferts thermiques croisés, un enjeu majeur dans les architectures embarquées à haute densité.

Des comparaisons précises sont faites entre mesures et simulations pour chaque point d'injection de puissance. Les résultats montrent une concordance très satisfaisante, avec des écarts relatifs faibles sur la résistance thermique équivalente, ce qui confirme la pertinence du modèle thermique même dans des configurations complexes.

Enfin, la validation électro-thermique globale est effectuée à travers un test de calorimétrie (presentés dans les figures 8, 9 et 10), permettant de mesurer le rendement énergétique en fonctionnement réel.

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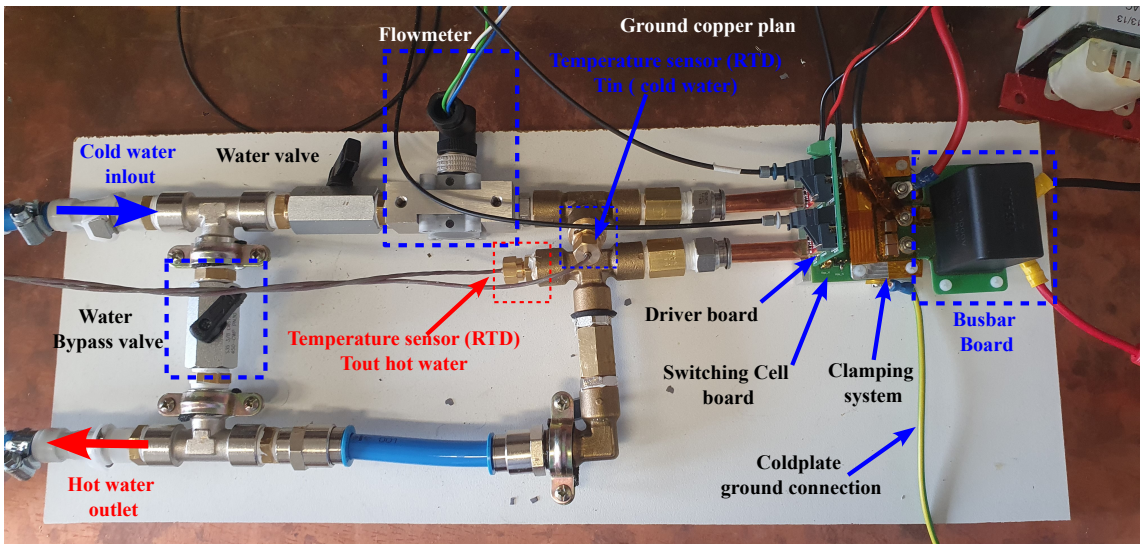

Figure 8: Montage d'essai complet : éléments de mesure calorimétrique, carte cellule de commutation, carte de commande et carte Busbar.

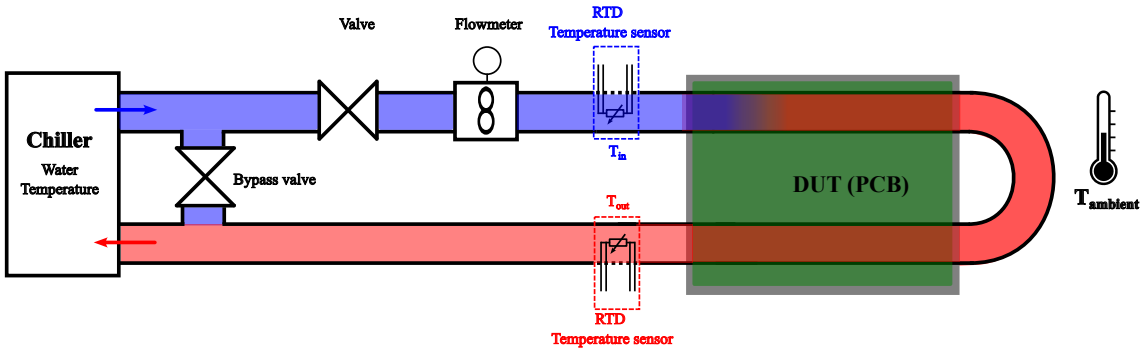

Figure 9: Schéma du circuit de refroidissement liquide et des éléments utilisés pour les mesures calorimétriques des pertes dans la cellule de commutation.

Ce chapitre conclut ainsi que l'outil développé fournit des modèles suffisamment fiables pour être intégrés dans un processus de conception agile, avec un compromis optimal entre précision, vitesse de calcul et degré d'automatisation.

Chapitre 5 – Mise en œuvre de l'outil sur des cas d'étude représentatifs

Ce chapitre illustre concrètement l'utilisation de l'outil de prototypage virtuel à travers plusieurs cas d'application typiques de l'électronique de puissance à base de PCB enfouis. L'objectif est de démontrer la pertinence de cet outil dans des contextes de conception réels, en mettant particulièrement l'accent sur la modélisation électromagnétique et thermique. L'étude principale porte sur la conception d'un onduleur ANPC (Advanced Neutral Point Clamped) destiné à des applications haute puissance. L'outil développé permet de prédire les performances des disposi-

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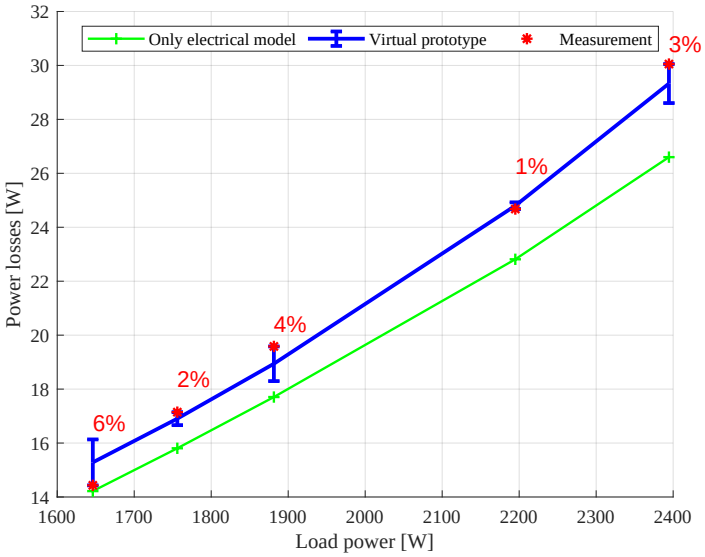

Figure 10: Mesures calorimétriques sur un circuit Buck pour différentes valeurs de puissance (Vin = 300 V, rapport cyclique de 0,38).

tifs avant leur fabrication, facilitant ainsi l'optimisation simultanée du rendement, de la dissipation thermique et des effets parasites.

Trois cas d'étude sont présentés, chacun correspondant à un scénario de conception spécifique :

1. Optimisation thermique d'un convertisseur de puissance embarqué.
2. Réduction des interférences électromagnétiques dans un étage de commutation rapide.
3. Amélioration du rendement global par restructuration du routage.

Pour chaque cas, la démarche suivie est systématique :

- Import du layout CAO dans l'outil.
- Génération automatique des modèles physiques (thermiques, électriques, électromagnétiques).
- Lancement d'une campagne de simulations explorant plusieurs variantes topologiques.
- Analyse des résultats pour orienter des décisions concrètes de conception.

L'onduleur ANPC est conçu pour répondre à des spécifications techniques exigeantes propres aux environnements haute puissance. Ses principales caractéristiques incluent une tension d'entrée de 750V (1,5 kV DC), une puissance de sortie de 100 kW (33 kW par phase), un rendement supérieur à 98%, et une densité de

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puissance excédant 30 kW/kg. Le refroidissement est assuré par un système à eau à 85 °C.

Le choix des composants technologiques repose sur un compromis entre performance et coût. Le circuit est réalisé sur un PCB à 4 couches, utilisant du cuivre de 105 μm. Des MOSFETs SiC (Wolfspeed CPM2-1200-0080) ont été retenus pour leurs performances de commutation et leur faible résistance à l'état passant. Deux matériaux diélectriques ont été comparés : le FR4 ($\lambda = 0,3$W/m·K) et le ML92 ($\lambda = 2$ W/m·K), ce dernier offrant de meilleures performances thermiques.

Pré-conception de l'ANPC et analyse des pertes

Avant la phase de conception du PCB, une étude analytique des pertes de conduction et de commutation a été menée sur quatre stratégies de modulation PWM. Les résultats montrent que l'utilisation de quatre puces en parallèle permet d'atteindre un rendement supérieur à 99%, la meilleure stratégie (PWM4) atteignant 99,3%.

Une analyse des boucles de puissance a permis d'identifier les inductances parasites associées aux boucles courtes et longues. La réduction de ces inductances est essentielle pour minimiser les surtensions et les oscillations, garantissant ainsi des performances stables et fiables du convertisseur.

Conception du PCB et optimisation des configurations

La conception du PCB a été explorée à travers plusieurs configurations de demi-ponts à deux niveaux, avec trois layouts testés. La première configuration (classique) offre une bonne gestion thermique ($R_{th} = 2,66$K/W avec le FR4), mais une capacité parasite élevée ($C_{AC} = 99,7$pF) induit des courants de mode commun. La deuxième configuration, grâce à un meilleur blindage, réduit la capacité parasite à 7,6 pF, mais présente un R_{th} plus élevé (5,08 K/W). La troisième configuration (flip-chip) représente un compromis, avec $C_{AC} = 6,4$pF et $R_{th} = 3,3$K/W. Les configurations classique et flip-chip ont été fabriquées pour la phase de validation décrite au chapitre 4.

Dans le cas d'un demi-pont multi-puces (4 puces), deux arrangements ont été évalués : un agencement aligné, induisant un déséquilibre de courant, et un agencement alterné, permettant une meilleure répartition du courant. Ce dernier réduit significativement les contraintes thermiques et dynamiques, renforçant la robustesse globale du système.

Optimisation du prototype ANPC

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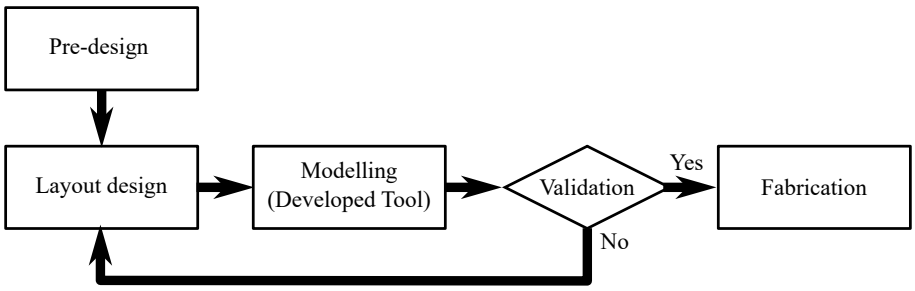

Figure 11: Workflow to follow in the design of the proposed power converter

Trois prototypes virtuels de l'ANPC ont été modélisés et comparés. Le prototype 3 a permis une réduction de 80% des inductances de boucle, améliorant notablement les performances électromagnétiques. Toutefois, l'éloignement des connecteurs DC a introduit une inductance parasite liée au busbar. Le prototype 2 a finalement été retenu pour son compromis optimal entre performance électromagnétique et faisabilité mécanique.

Retour d'expérience sur la méthodologie

La méthodologie adoptée, reposant sur la modélisation automatisée, a permis de réduire significativement le temps de développement par rapport à une approche traditionnelle basée sur le prototypage physique. Les simulations ont fourni des données complexes, comme les courants individuels par puce ou les températures de jonction, offrant une vision fine du comportement du système. Certaines limites ont néanmoins été identifiées : fragilité logicielle, dépendance à des outils propriétaires (tels qu'Altium et ANSYS), et précision limitée par les écarts entre conception et fabrication. De plus, la modélisation multi-cartes, notamment l'interaction entre le PCB et le busbar, n'a pas été abordée ici mais constitue une piste d'amélioration pour des travaux futurs.

Conclusion

Ce chapitre démontre l'efficacité de l'outil de modélisation automatisée dans l'optimisation des layouts de PCB, en équilibrant les performances thermiques et électromagnétiques, tout en permettant la prédiction fiable des performances avant fabrication. Il met en évidence l'importance d'une approche couplée électro-thermique dans la conception de convertisseurs haute performance, et ouvre des perspectives vers le développement d'outils plus robustes, ouverts et interopérables. Les résultats s'inscrivent dans une logique d'industrialisation de la conception de convertisseurs embarqués, avec un fort potentiel d'application dans des domaines variés nécessitant des systèmes de puissance compacts, fiables et performants.

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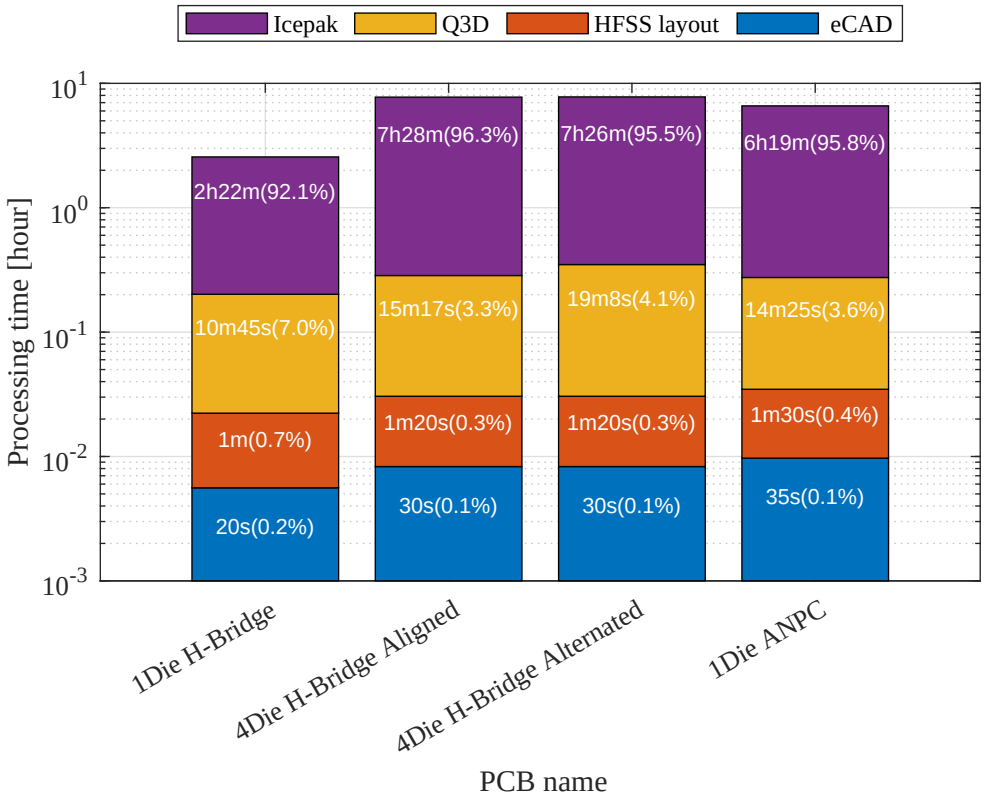

Figure 12: Breakdown of the time taken by the model-generation workflow. Note that the vertical scale is logarithmic.

Conclusion générale

Les travaux présentés dans ce manuscrit s'inscrivent dans le contexte de la transformation progressive des méthodes de conception en électronique de puissance, sous l'impulsion de la complexité croissante des architectures embarquées, de la pression sur les délais de mise sur le marché et de l'impératif d'optimisation multiphysique. Face à ces enjeux, la thèse a proposé une approche innovante fondée sur le prototypage virtuel automatisé des cartes électroniques, permettant d'anticiper les comportements thermiques, électriques et électromagnétiques dès les premières phases de conception.

L'objectif principal de ce travail a été la conception et le développement d'un outil logiciel capable de générer automatiquement des modèles multiphysiques exploitables à partir d'un simple fichier de layout CAO. À cette fin, une chaîne de traitement complète a été formalisée, intégrant la reconstruction géométrique, l'annotation physique, la génération de modèles, et la restitution des résultats de simulation. L'ensemble a été pensé pour garantir une interopérabilité maximale avec les outils industriels existants et une automatisation poussée, sans intervention manuelle entre l'import et la simulation.

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Les résultats obtenus ont démontré que les prototypes virtuels ainsi générés présentent un niveau de fidélité suffisant pour une utilisation en phase de conception, avec des écarts faibles par rapport aux mesures physiques, tout en conservant une rapidité d'exécution compatible avec une démarche itérative. Cette capacité à explorer efficacement des variantes topologiques ouvre la voie à une co-conception multiphysique intégrée, rompant avec les approches séquentielles traditionnelles.

Les cas d'application exposés en fin de manuscrit ont permis de valider l'outil sur des systèmes représentatifs, et de mettre en évidence ses apports concrets en termes de performance, de réduction du prototypage physique, et d'aide à la décision. Ces exemples démontrent le potentiel de la démarche pour s'inscrire dans un processus de conception industriel, agile et rigoureux à la fois.

Au-delà des résultats obtenus, ce travail pose les jalons d'un nouveau paradigme de conception, dans lequel la simulation n'est plus cantonnée à une phase de vérification en aval, mais devient un véritable moteur de conception en amont. Le prototypage virtuel devient alors un vecteur central d'innovation, de fiabilisation et de compétitivité dans le domaine stratégique de l'électronique de puissance.

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Chapter 1

Considerations for the design of power converters

Power electronic converters convert and control electrical power across a wide range, from milliwatts to gigawatts [3]. As the demand for efficient energy management systems continues to grow, power electronics have emerged as a critical focus of research and innovation, especially in light of the global transition to sustainable energy sources. The ability to efficiently convert and manage electrical energy is essential for integrating renewable energy technologies, electric vehicles, and advanced industrial systems into the existing infrastructure.

This dynamic field faces both significant challenges and exciting opportunities. It is crucial to design power converters that maximize efficiency while minimizing size and cost to meet the increasing demands of various applications. These challenges are further complicated by the necessity for converters to operate reliably under diverse conditions while complying with increasingly stringent regulatory standards for performance and environmental impact.

In this chapter, we will explore the fundamental components of power converters, discussing their operating principles, design considerations, the challenges of thermal management, and the latest technological advancements.

1 Power converter

Power converters are essential devices that manage the flow of electrical energy by altering the nature of the electrical signal between two systems. Their primary functions include converting direct current (DC) to alternating current (AC) and vice versa, as well as adjusting voltage, current, or frequency depending on system

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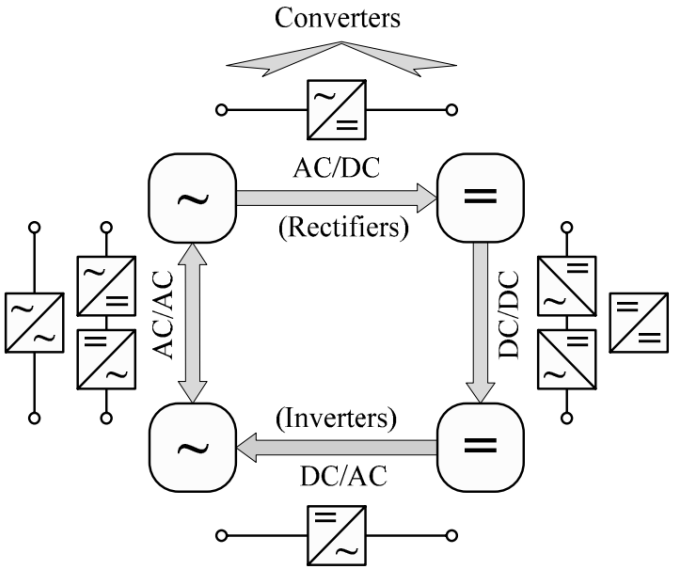

Figure 1.1: Basic types of the power electronics converters [4].

requirements. By converting, controlling, and regulating electrical energy as it flows from a source to a load, power converters play a crucial role in ensuring that energy is modified appropriately to meet various operational needs. Power conversion systems are typically categorized by the types of input and output waveforms, distinguishing between AC and DC signals, as illustrated in Figure 1.1.

A power electronic converter consists of a combination of various components and subsystems. These components typically include power semiconductor switches, gate drivers, cooling systems, passive components (inductors, capacitors, transformers, which can be used to form filters, to store energy, or convert voltages), sensors, control boards, and mechanical housing. The integration and interaction of these elements enable the converter to operate effectively and reliably, as illustrated in Figure 1.2.

The design of a power converter is a complex challenge. Multiple factors, including efficiency, size, cost, and thermal management influence it. The selection of components, topology, and control strategies significantly impacts the overall performance and characteristics of the system. Power electronics aim to achieve maximum efficiency and reliability [5] while minimizing costs, weight, and size. Smaller systems provide advantages such as faster switching, optimized interconnections, and fewer filtering components; however, they also face the challenge of limited surface area for heat dissipation. As a result, effective thermal management becomes crucial because preventing components from overheating is essential for reliable operation. Several key factors contribute to the design challenges associated with power converters:

- **Efficiency**: Power converters must operate with high efficiency to minimize

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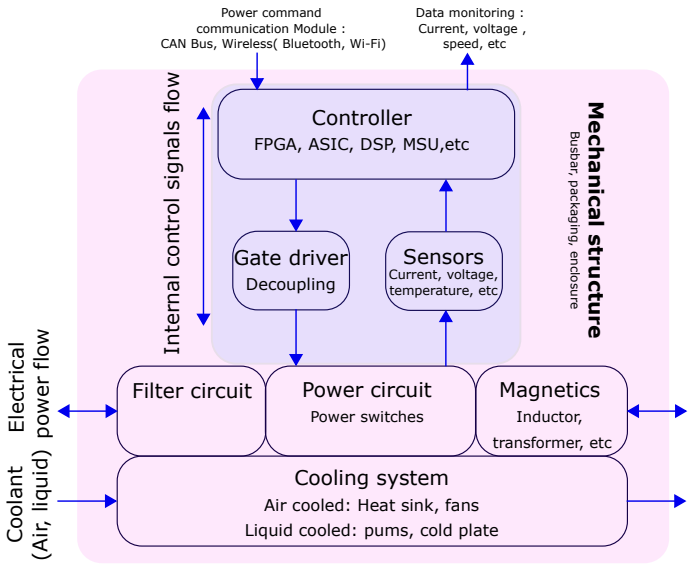

Figure 1.2: Power converter structure.

energy losses. Achieving this requires careful selection of components and control strategies to optimize performance across various conditions.

- **Thermal Management**: High-power applications, in particular, generate significant heat, making thermal management a critical concern. Techniques like heat sinks, fans, and liquid cooling systems are essential to prevent overheating and maintain system reliability.

- **Electromagnetic Interference (EMI)**: Power converters often produce high-frequency noise that can interfere with other electronic systems. Mitigating EMI requires thoughtful circuit layout, filtering, and shielding techniques.

- **Electronic Component Sizing**: Correct electronic component sizing is critical for ensuring that the circuit operates safely, efficiently, and reliably over its intended lifespan. It involves a balance of factors, including electrical parameters (voltage, current, power), thermal considerations, component tolerances, and cost.

- **Topology and Control Complexity**: The design of a power converter is largely determined by the topology of its circuit diagram (such as buck, boost, or full-bridge), which influences its efficiency, dynamic performance, and overall complexity. The way active power devices are controlled is also dictated by the choice of the topology.

  The control systems must be highly responsive to fluctuations in load and input conditions.

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- **Regulatory Compliance**: Power converters must comply with the industry standards for performance, safety, and emissions. Adhering to these standards ensures that converters operate seamlessly with other systems while minimizing the risk of interference or damage.

Finally, designing power converters is a complex and challenging process that requires balancing all these factors with cost considerations to produce economically viable products. This task demands a deep understanding of electrical engineering and substantial practical experience. The design process is iterative and often relies on advanced software tools and control algorithms to optimize converter behavior. Adherence to established industry standards, developed over decades of engineering expertise, ensures converters meet safety, reliability, and interoperability requirements. Despite these guidelines, the continual push for more efficient, compact, and cost-effective solutions drives innovation in design techniques and simulation methods.

1.1 Elementary power switching cell

Power converter designs are based on a fundamental element, the "switching cell", which is the elementary brick to build more complex structures [6, 7]. By adding additional switches, cascading cells, integrating components, and employing advanced control techniques, engineers can achieve higher efficiency, greater flexibility, and improved load handling. These enhancements are essential for designing power electronics systems targetted at various applications.

An illustrative example of an elementary switching cell is shown in Figure 1.3.

Essential components connected to the switching cell are inductors and capacitors, which store energy in magnetic and electric fields, respectively, and help regulate variations in voltage or current. When the energy flow is interrupted by the switching cell, inductors and capacitors supply energy, ensuring smooth, continuous power delivery and acting as filters to reduce ripple.

In addition to the essential power components such as switches, capacitors, and inductors, a converter requires various components for proper operation, including gate drivers and sensors. Figure 1.3 illustrates a simple commutation cell with control circuits and examples of voltage and current sensors used in power circuits. Design consideration for such low power circuits include electrical isolation (because of the high voltages in the power circuit) and electromagnetic immunity (to prevent the fast voltage and current transients in the power circuit from disrupting the

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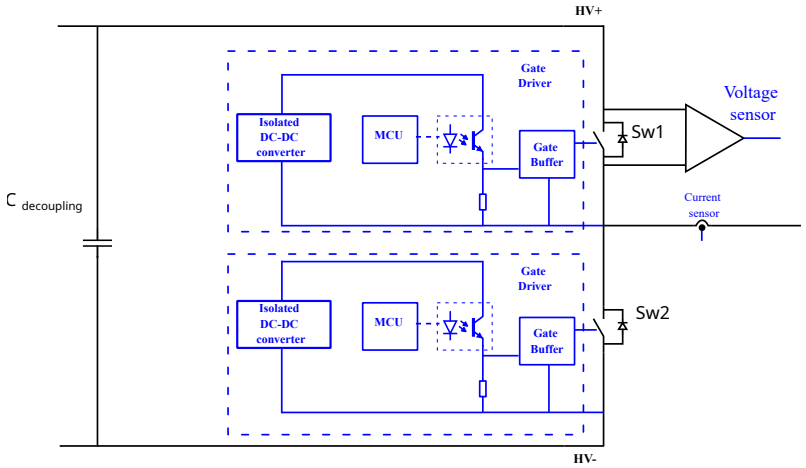

Figure 1.3: Elementary switching cell; Low and high power stages are represented in blue and black, respectively.

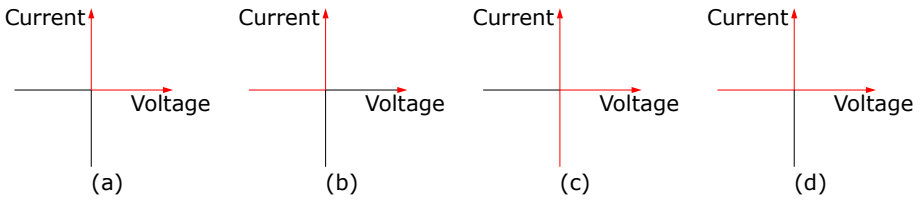

Figure 1.4: Switches ideal voltage/current characteristics.

sensitive control electronics).

1.2 Power switches

Power devices (transistors and diodes are at the heart of the switching cell. They can be represented by their I/V characteristics in both the conducting and blocked states, as shown in figure 1.4.

(a): the voltage can only be positive and the current positive. Example: bipolar transistor;

(b): the voltage can only be negative and the current positive. Example: diode;

(c): the current can flow in either direction, but only positive voltage can be blocked. Example: Metal Oxide Field Effect Transistor (MOSFET);

(d): the voltage can be clamped positively or negatively, but the current can only flow positively through the component. Example: the thyristor.

Wide Band-Gap semiconductors (WBG)

Silicon-based semiconductors have been the standard in power electronics for more than 65 years. However, with the increasing demand for higher efficiency, faster switching speeds, and the ability to operate at higher voltages and frequencies,

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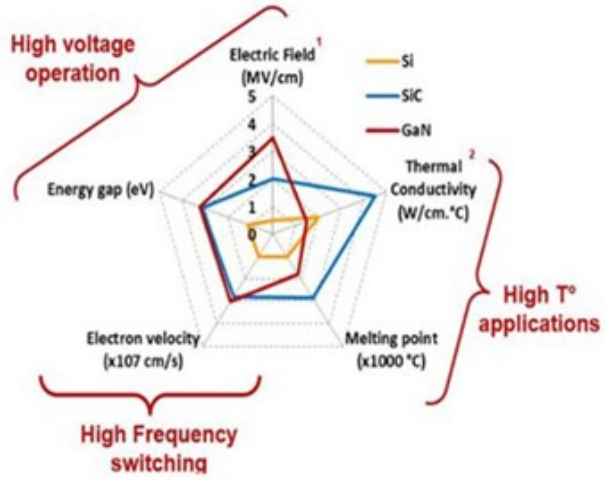

Figure 1.5: Physical characteristics of Si,GaN and SiC[8]

the physical limits of silicon have been reached and new devices made out of other semiconductor materials have recently become available.

Wide Band-Gap (WBG) semiconductors, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), offer significant performance advantages over traditional silicon.

The band-gap refers to the energy difference between the top of the valence band and the bottom of the conduction band. A larger band-gap allows wide band-gap semiconductor power devices to operate at higher voltages and temperatures.

GaN and SiC have band-gaps approximately three times greater than that of silicon (1.12 eV), at about 3.2 eV and 3.4 eV, respectively. A summary of the he main physical properties of the three semiconductor materials is presented in Figure 1.5. It illustrates the superior performances of SiC. With a saturation drift velocity more than double that of Si and a critical electric field nearly 8 times higher, SiC is one of the best-performing semiconductor materials. Additionally, 4H-SiC (the most common polytype of SiC) has a thermal conductivity that is more than twice that of silicon.

Figure 1.6 illustrates the application fields of different semiconductor materials, taking into account their power capabilities and operating frequencies.

Gallium Nitride (GaN), for instance, exhibits higher electron mobility, which makes it particularly suitable for high-frequency applications. This advantage is further enhanced by its very low parasitic capacitances. It is worth noting that besides power electronics, GaN is commonly used in radio frequency (RF) devices that operate in the gigahertz range.

In contrast, Silicon Carbide (SiC) has higher thermal conductivity but more lim-

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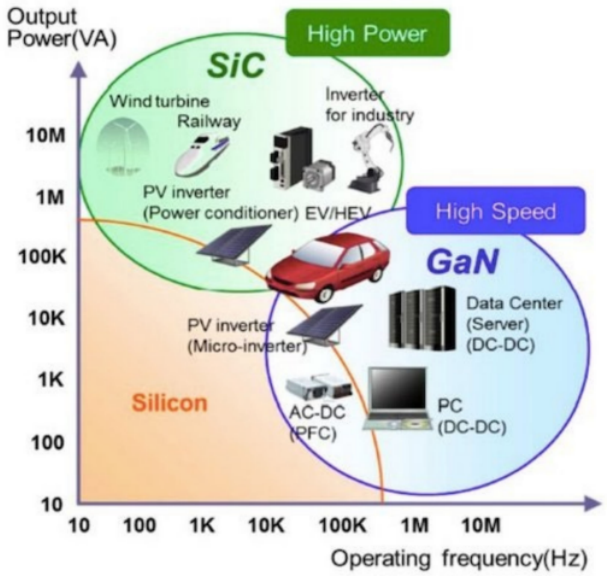

Figure 1.6: Application fields of semi-conductors[9].

ited frequency capabilities, although it still operates at frequencies higher than those of silicon. SiC is better suited for higher-power applications, including the elevated voltage requirements found in transportation, energy generation, and distribution.

1.3 Conclusion

In conclusion, the design of power converters is a complex process that requires balancing efficiency, reliability, and cost while adhering to industry standards. The integration of wide-bandgap (WBG) semiconductors represents a significant advancement in this field, enabling the development of more efficient and compact power converters. However, to fully exploit the potential of WBG devices, engineers must carefully address critical factors such as thermal management, losses, and packaging. Overall, the ongoing pursuit of innovative design techniques and advanced simulation methods is essential for creating high-performance power electronic solutions that meet the industry's evolving demands.

2 Switching Operation

2.1 Parasitic components

When studying an electrical circuit, interconnections are often considered as perfectly equipotential. However, this assumption is no longer valid when analyzing a power electronics circuit. Interconnection elements (i.e., all the tracks, bonding wires, Vias, or layers of copper that connect any two components) introduce parasitic

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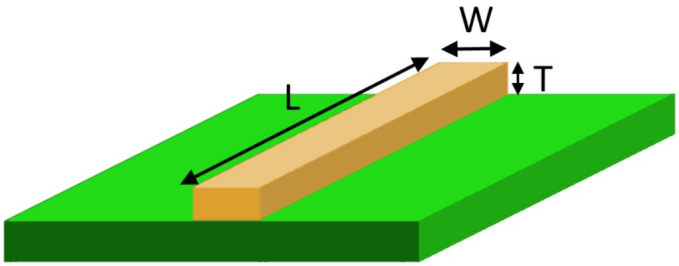

Figure 1.7: Stripline resistance[10].

inductances, resistances, and capacitance. These parasitic effects can significantly impact the performance of power electronics systems, especially at high frequencies or during rapid switching events. With the emergence of fast-switching devices based on SiC and GaN, the dynamic behavior of all components in a converter becomes even more critical to account for. These phenomena are explained in this section.

2.1.1 Conductors resistance

Every electrical conductor presents a resistance which depends on its dimensions, as described by eq. (1.1).

$$R = \frac{\rho(T) \cdot L}{T \cdot W} = \frac{\rho_0 \cdot L}{T \cdot W} \cdot (1 + \alpha \cdot (T - T_{ref})) \tag{1.1}$$

With:

$$\begin{cases} R & : \text{trace resistance } [\Omega] \\ \rho(T) & : \text{resistivity of the material } [\Omega \cdot m] \\ \rho_0 & : \text{resistivity of the material at } T_{ref} \ [\Omega \cdot m] \\ L & : \text{trace length } [m] \\ T & : \text{material thickness } [m] \\ \alpha & : \text{temperature coefficient of the resistivity} \\ T & : \text{operating temperature } [^\circ C] \\ T_{ref} & : \text{reference temperature (commonly 20°C)} [^\circ C] \end{cases}$$

At high frequencies, conductors experience a phenomenon known as the skin effect. The skin effect occurs because alternating current (AC) generates a time-varying magnetic field that induces eddy currents within the conductor. These eddy currents oppose the flow of the main current, causing it to be pushed toward the conductor's surface. As the frequency increases, the current is forced to flow through a progressively thinner conductor layer, effectively increasing its resistance.

For a conductor with a round cross-section, the skin depth δ measures how deeply the current can penetrate the conductor. It is given by:

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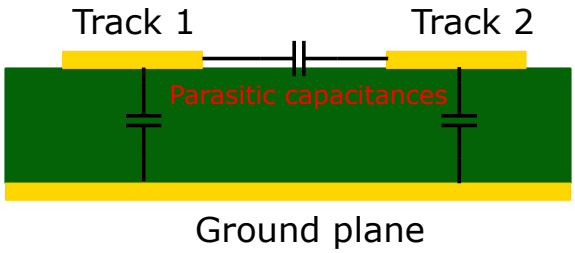

Figure 1.8: Stray capacitors between multiple conductors

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{1.2}$$

By inserting the formula for skin depth in (1.1), we can determine that the AC resistance equation shows an increase in AC resistance with frequency, as skin depth decreases with rising frequency:

$$R_{\text{AC}} = \frac{\rho(T)L}{A_{\text{eff}}(T)} = \frac{\rho(T)L}{W \cdot \delta(T)} = \frac{\rho(T)L}{W \cdot \sqrt{\frac{\rho(T)}{\pi f \mu}}} \tag{1.3}$$

With:

$$\begin{cases} \delta & : \text{ skin depth } [m] \\ f & : \text{the frequency } [Hz] \\ \mu & : \text{Magnetic permeability of the conductor } [H/m] \\ W & : \text{Width of the trace } [m] \end{cases}$$

In addition, the time-varying magnetic fields caused by the flow of AC currents can induce eddy currents in nearby conductors, resulting in a non-uniform distribution of current density (proximity effect). Consequently, the current tends to concentrate on the surfaces of conductors that are facing each other, which further reduces the active cross-section of the conductor and effectively increases their resistance.

To reduce the proximity effect, several strategies can be utilized. These include increasing the distance between traces or conductors to decrease current interaction, using wider traces to lower current density, and incorporating shielding with grounded conductors to minimize magnetic coupling.

2.1.2 Parasitic capacitance

Stray or parasitic capacitance refers to the unintentional accumulation of electric charge within a circuit. This type of capacitance can occur between conductors, as illustrated in Fig. 1.8.

As a quantitative example, let's consider a capacitor comprising two parallel

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plates of area A separated by a distance d. If d is sufficiently small compared with the smallest length of A, the corresponding capacitance is:

$$C = \epsilon \frac{A}{d} \tag{1.4}$$

$$\epsilon = \epsilon_0 \epsilon_r \tag{1.5}$$

with:

$$\begin{cases} C & : \text{capacitance } [F] \\ A & : \text{area of overlap of the two plates } [m^2] \\ \epsilon_0 & : \text{the dielectric constant } (\epsilon_0 \sim 8.854e^{-12} F.m^{-1}) \\ \epsilon_r & : \text{relative permittivity of the material} \\ & \quad \text{in-between the plates } (\epsilon_r \approx 1 \text{ for air}) \\ d & : \text{separation distance between the plates } [m] \end{cases}$$

In power electronic systems, stray capacitance can significantly impact the switching performance and efficiency. It adds to the internal switch capacitance, thereby prolonging the overall switching time and causing additional losses. Additionally, it may create resonant circuits with parasitic inductance, resulting in unwanted oscillations or ringing. Stray capacitances are also a significant contributor to electromagnetic interferences (EMI), as they provide undesired propagation paths for high frequency signals .

2.1.3 Parasitic inductance

A current flowing through a conductor creates a magnetic field, which produces an inductive effect within the conductor itself, or which can induce currents in other conductors nearby. Figure 1.9a illustrates the magnetic flux produced when two adjacent conductors carry currents in opposite directions, a typical situation in a PCB setup. The two yellow conductors, each of length l and separated by distance d, carry currents i_b and i_a. The resulting magnetic flux from i_a and i_b is shown with blue and red lines, respectively.

The electrical equivalent model is depicted in Figure 1.9b, where L_a and L_b represent the self-inductances of each conductor, and M_{ab} denotes the mutual inductance between the two conductors. According to Faraday's law, the induced voltages v_a and v_b in each conductor, resulting from the currents i_a and i_b, can be expressed as follows:

$$\begin{cases} v_a = L_a \frac{di_a}{dt} - M_{ab} \frac{di_b}{dt} \\ v_b = L_b \frac{di_b}{dt} - M_{ab} \frac{di_a}{dt} \end{cases} \tag{1.6}$$

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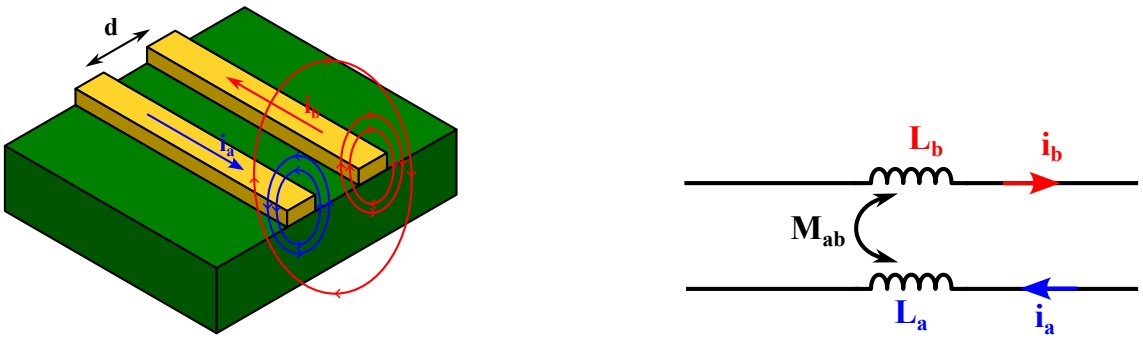
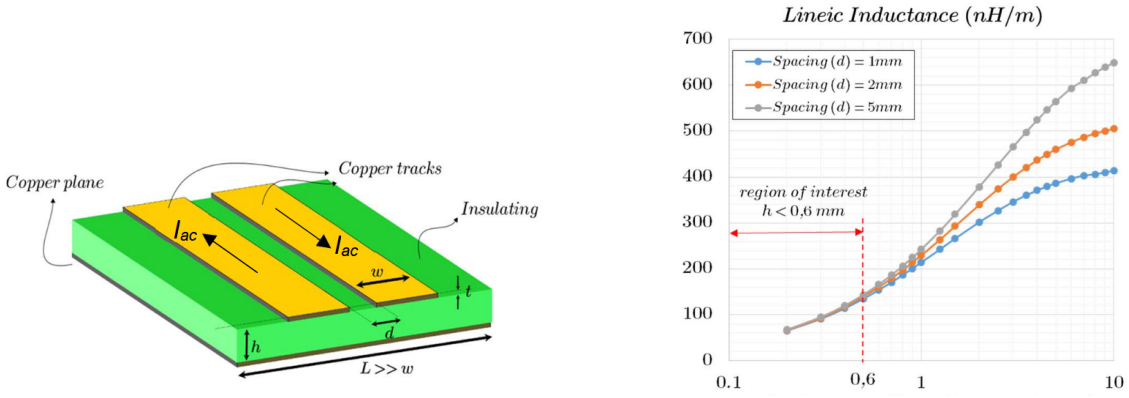


(a) (b)

Figure 1.9: Magnetic flux and inductances of two conductors with the same current direction. (a) Current and magnetic flux flow; (b) equivalent circuit.



(a) (b)

Figure 1.10: (b) Coupled microstrip schematic and.(b) Lineic Inductance as a function of thickness [13].

The parasitic inductance caused by interconnections in packaging can lead to significant voltage spikes during the turn-off transients of active switches (this is presented further below). These undesired voltage spikes may exceed the device's voltage ratings, posing a serious risk to the safe operation of fast-switching devices like SiC and GaN [11, 12]. Additionally, high stray inductance can increase turn-on and turn-off times, resulting in greater switching losses and energy dissipation, ultimately reducing efficiency.

To reduce parasitic inductance, minimizing the area between conductors where magnetic fluxes add up is crucial. This can be achieved by bringing the conductors closer together, reducing loop areas in high-current paths with short, wide traces, lowering impedance in return paths. This also requires placing switching components closer from each other. Additionally, the technique of ground plane shielding plays a crucial role in limiting the spread of magnetic fields and reducing inductive coupling between traces. This shielding effect can be explained as follows: fast current transients generate changing magnetic fields that induce eddy currents in the

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ground plane. According to Lenz's Law, these eddy currents create a counteracting magnetic field, which helps to confine the flux and reduce parasitic inductance.

In [13], the authors discuss the impact of substrate thickness on the inductance of a coupled micro-strip circuit. The research demonstrates that the track's lineic inductance strongly depends on the substrate thickness h. When the insulating substrate is sufficiently thin (i.e., $h < 0.6\,\text{mm}$), the inductance becomes mostly independent of track spacing d, emphasizing the importance of substrate design in managing inductive effects.

2.1.4 Conclusion on parasitic elements

Interconnects play a significant role on the performance of power electronic converters. In most cases, design engineers seek to keep parasitic inductances, capacitances and resistances as low as possible. Key mitigation strategies for stray inductance include reducing power loops, incorporating ground plane shielding and selecting the appropriate conductor thickness. On the contrary, reducing parasitic capacitance or resistance may require placing conductors further from each other, or further away from ground planes. Additionally, practical challenges such as clearance, insulation thickness, and manufacturing limitations must be addressed to ensure the circuit operates reliably and efficiently.

2.2 Switching cell

In this thesis, the semi-conductors used include Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), diodes, and insulated-gate bipolar transistors (IGBTs). This section focuses on a switching cell composed specifically of a diode and a MOSFET, but similar conclusions could be drawn for an IGBT/diode switching cell.

Here, the commutation process is analyzed to understand the critical aspects of how MOSFETs operate during switching events, including the effects of stray elements on the commutation process. Special care is given to assessing the duration of the commutation phase and the power losses associated with these transitions.

The analysis of the switching process is conducted using a device model proposed in the literature, which accounts for the dynamic behavior of the MOSFETs [14, 15, 16, 17].

Fig. 1.11a shows the cross-section of a typical MOSFET, along with its corresponding equivalent behavioral circuit. Notably, the internal capacitors of the MOS-

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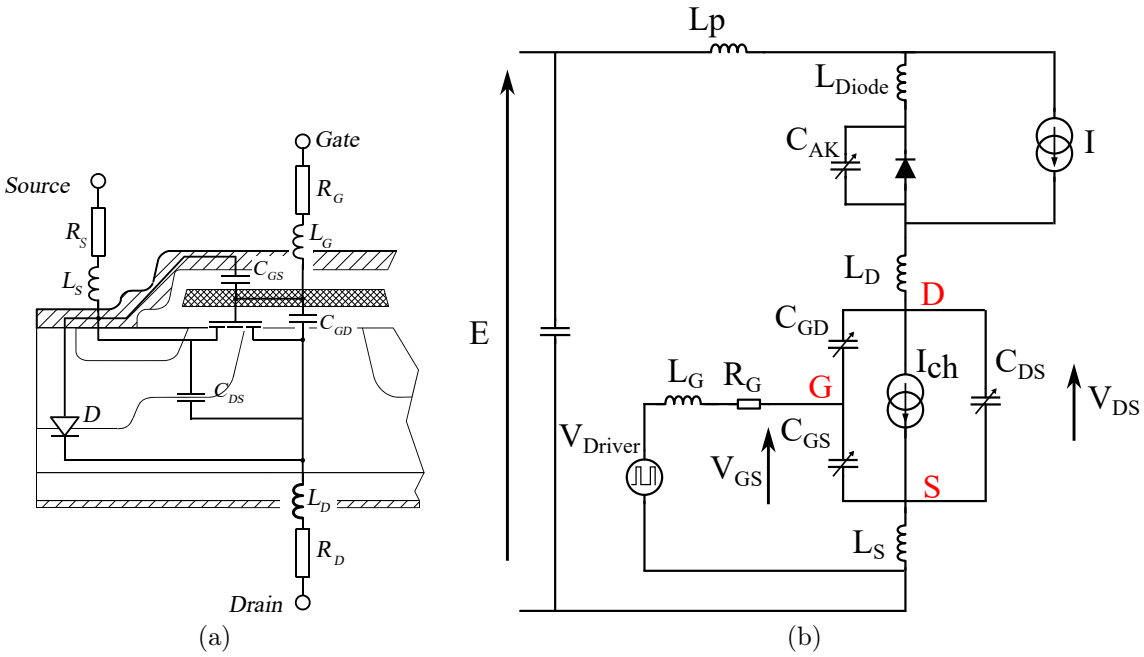

Figure 1.11: (a) Mosfet behavior's circuit with stray elements due to the package[18].(b)Commutation cell Mosfet diode.

FET, as illustrated in the equivalent circuit of the commutation cell (Figure 1.11a), have a strong effect on switching dynamics. They result from the arrangement of the semiconductor regions and insulating layers.

2.2.1 Switching waveforms

Fig. 1.11b illustrates the parasitic inductances resulting from the packaging of the semiconductor devices: L_S, L_D, L_G, and L_{Diode}, which correspond to the source, drain, gate of the MOSFET, and the diode, respectively. Additionally, the stray inductance of the power circuit (caused by the copper tracks connecting the devices) is denoted L_p. The internal capacitances are represented as C_{ds}, C_{gs}, and C_{gd}. The values of these capacitances vary non-linearly with the applied voltage V_{DS} and are typically expressed using datasheet parameters C_{iss}, C_{oss}, and C_{rss}, as follows:

$$\begin{aligned} &\text{Input capacitance :} && C_{iss} &&= C_{GS} + C_{GD} \\ &\text{Output capacitance :} && C_{oss} &&= C_{GD} + C_{DS} \\ &\text{Reverse transfer capacitance :} && C_{rss} &&= C_{GD} \end{aligned} \tag{1.7}$$

to simplify the analysis of the switching waveform, these capacitances are assumed to be constant.

Turn-on transition of the MOSFET

Figure 1.12, presents the 4 phases of the turn-on transition:

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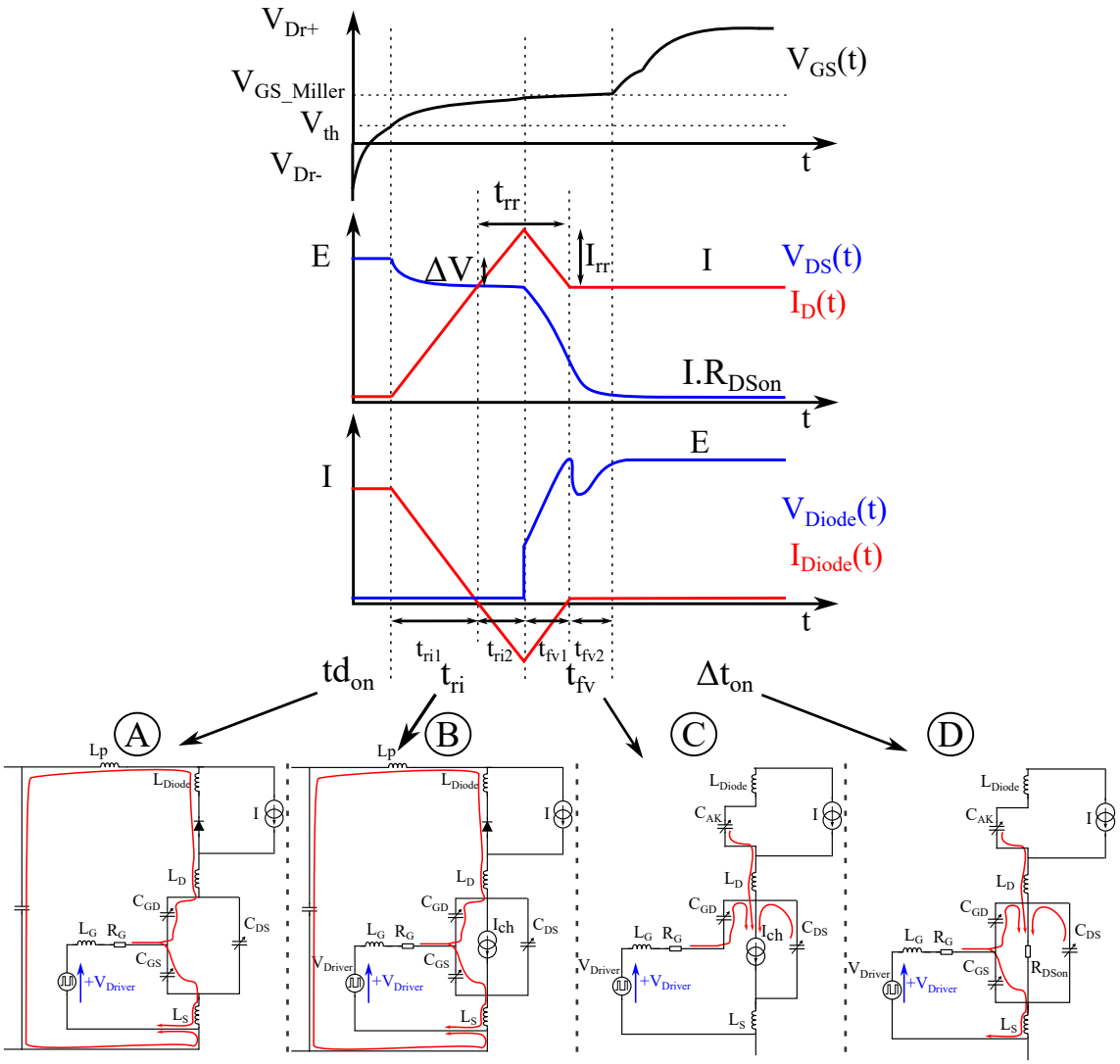

Figure 1.12: turn on waveforms

Ⓐ **Delay-time period** td_{on}**:** At the beginning, the power device is off, and the load current passes through the free-wheeling diode. At $t = 0$, the driver applies the positive value V_{Dr+}, charging the internal (and externally added) capacitors across gate-source C_{GS} and gate-drainC_{GD} with a current i_G limited by the gate resistor R_G and parasitic inductance L_G. The gate-source voltage increases with the time constant $\tau = R_G.C_{iss}$. The drain current is still null, and V_{DS} doesn't change from the value E. $V_{GS}(t)$ varies as follows :

$$V_{GS}(t) = (V_{Dr+} - V_{Dr-}).(1 - e^{\frac{-t}{\tau}}) + V_{Dr-} < V_{th} \tag{1.8}$$

The delay time is the time it takes for the gate-source voltage to reach the V_{GS} threshold voltage (V_{th}, at which the MOSFET starts turning on:

$$td_{on} = \tau.ln(\frac{V_{Dr+} - V_{Dr-}}{V_{Dr+} - V_{th}}) \tag{1.9}$$

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Ⓑ **Current rise time period t_{ri}:** When the gate-source voltage V_{GS} reaches V_{th}, the drain current begins to increase. This increase causes a voltage drop ΔV across the MOSFET due to the parasitic inductances, as described by equation 1.10:

$$V_{DS} = E - (L_S + L_D + L_p).\frac{di}{dt} = E - \Delta V \tag{1.10}$$

Note that the voltage across L_S acts as feedback for the MOSFET control V_{GS}. According to Kirchhoff's voltage law, we have $V_{Driver} = V_{R_G} + V_{L_G} + V_{GS} + V_{L_S}$. Therefore, increasing V_{L_G} at a constant V_{Driver} will tend to decrease V_{GS}, V_{R_G} and V_{L_S}.

The canal current rises following eq (1.11) with the MOSFETs forward non-linear factor transconductance gm that depends on V_{GS}:

$$I_{ch}(t) = gm(V_{GS}).(V_{GS}(t) - V_{th}) \tag{1.11}$$

The rise time continues until the drain current reaches $I + I_{RR}$ where I_{RR} is the diode diverse recovery current. The rise time can be calculated [19] by :

$$t_{ri} = \tau.ln(\frac{gm.(V_{Dr+} - V_{th})}{gm.(V_{Dr+} - V_{th}) - (I + I_{RR})}) \tag{1.12}$$

Ⓒ **Miller plateau time period t_{fv}:** At this level, the diode is blocked, and the gate-source voltage reaches V_{GS_Miller}. Both the gate current and voltage remain theoretically constant, with all the gate current flowing through the gate-drain capacitor:

$$i_g(td_{on} + t_{ri}) = -C_{GD}\frac{dV_{DS}}{dt} = -\frac{dQ_{DG}}{dt} \tag{1.13}$$

According to [19] and and using the voltage drop from equation 1.10, the drain-source voltage can be formulated as :

$$V_{DS}(t) = -\frac{V_{Dr+} - V_{th}}{R_G.C_{GD}}.t + (E - \Delta V) \tag{1.14}$$

This so-called Miller plateau ends when V_{DS} reaches $V_{DS} = V_{DS_sat}(V_{Dr+})$, which is a very low voltage. To find the period t_{vf}, eq 1.14 is solved for $V_{DS}(t_{vf}) = 0$:

$$t_{vf} = \frac{R_G.C_{GD}}{V_{Dr+} - V_{th}}.(E - \Delta V) = C_{GD}.\frac{(E - \Delta V)}{i_g(td_{on} + t_{ri})} \tag{1.15}$$

In this phase, the decrease of V_{DS} is pursued by the discharge of the capacitance C_{oss} and C_{Ak}. The Drain current is, therefore, higher compared with the power current

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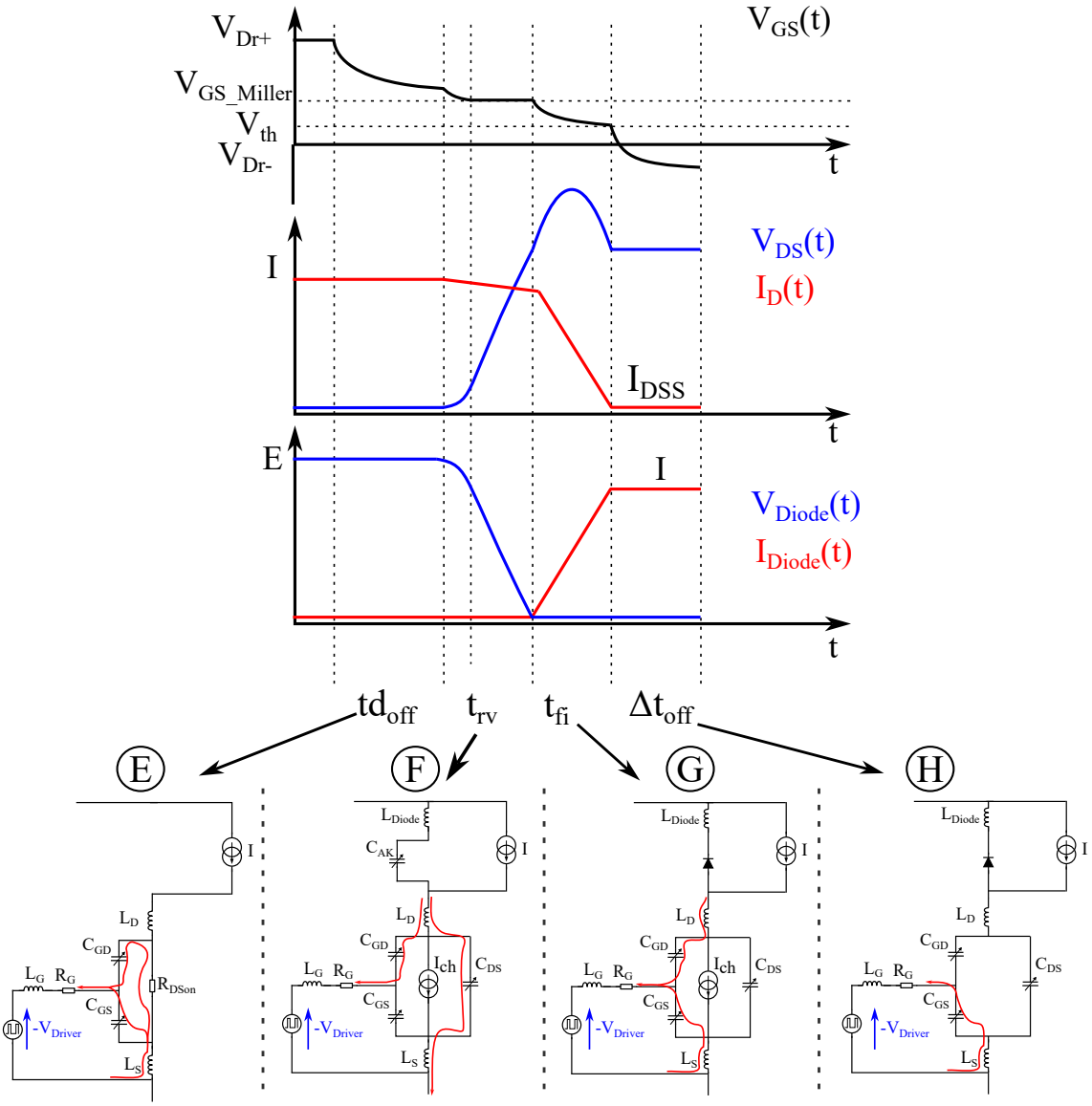

Figure 1.13: turn off waveforms

I:

$$I_D = I + \frac{d(C_{Ak}.V_{DS})}{dt} \tag{1.16}$$

(D) **Stabilization period Δt_{on} :** During this phase, the gate-source voltage V_{GS} continues to rise until it reaches the value set by the driver, V_{Dr+}. At the end of this stage, V_{DS} stabilizes at a value corresponding to $V_{DS_on} = I \cdot R_{DSon}$, marking the completion of the turn-on switching process.

Mosfet's turn-off transition

(The waveforms are shown in Fig 1.13)

(E) **Delay time period td_{off}:** At the beginning, the device is on, and the load current is flowing through the MOSFET, meaning $I_D = I$ and $V_{DS} = V_{DS_on}$. This phase starts with the driver applying a value of V_{Dr-}, which can be zero or, more

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commonly, a negative value. This step causes the gate-source (C_{GS}) and gate-drain capacitors(C_{GD}) to discharge through R_G, with a time constant $\tau = R_G.C_{iss}$:

$$V_{GS}(t) = (V_{Dr+} - V_{Dr-}).e^{\frac{-t}{\tau}} + V_{Dr-} > V_{GS_Miller} \tag{1.17}$$

$V_{GS}(t)$ continues to decrease until it reaches a constant level (Miller Plateau). At that stage, the drain current I_D still equals I. The gate-source voltage at the Miller plateau is traditionally approximated and defined as [20, 21] :

$$V_{GS_Miller} = \frac{I}{gm(V_{GS})} + V_{th} \tag{1.18}$$

From 1.17 and 1.18, the time needed for $V_{GS}(t)$ to reach the plateau can be determined by :

$$td_{off} = \tau.ln(\frac{V_{Dr+} - V_{Dr-}}{\frac{I}{gm(V_{GS})} + V_{th} - V_{Dr-}}) \tag{1.19}$$

Ⓕ **Miller plateau time period t_{rv} :** At this stage, the current flowing through the transistor does not equal the load current $I_{ch} \neq I$. A fraction of the current I in excess charges the capacitors C_{DS}, C_{GD}, and C_{Ak}, initiating the voltage switching phase. During this phase, the gate-source voltage is constant, and all the driver current is taken from the gate-drain capacitor, so the gate current is equal to :

$$i_G = C_{GD}.\frac{dv_{GD}}{dt} = C_{GD}.\frac{d(v_{GS} - v_{DS})}{dt} = -C_{GD}.\frac{dv_{DS}}{dt} \tag{1.20}$$

Using eq (1.18), the gate current can be expressed by:

$$i_G = \frac{V_{GS_Miller}}{R_G} = \frac{\frac{I}{gm(V_{GS})} + V_{th}}{R_G} \tag{1.21}$$

The combination of eqs. (1.20) and (1.21) results in the equation of the drain-source voltage :

$$V_{DS}(t) = \frac{\frac{I}{gm(V_{GS})} + V_{th}}{R_G.C_{GD}}.t + V_{DS_on} \tag{1.22}$$

The rise time t_{rv} needed for V_{DS} to reach the level E is defined as:

$$t_{rv} = \frac{(E - V_{DS_on}).R_G.C_{GD}}{\frac{I}{gm(V_{GS})} + V_{th}} \tag{1.23}$$

Ⓖ **Current fall time period t_{fi}:** In this phase, the drain-to-source voltage V_{DS} has reached the input voltage E, which causes the freewheeling diode to turn on. As a result, the current starts to flow through the diode, leading to a decrease in

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the drain current. This decline is limited by the voltage that develops across the parasitic inductances L_S, L_D, and L_p. The change in current can be expressed as:

$$i_D = gm(V_{GS}).(V_{GS} - V_{th}) \tag{1.24}$$

The discharge of the gate-source voltage from the Miller voltage V_{GS_Miller} (eq (1.18)) to the threshold voltage V_{th} can be expressed as:

$$V_{GS}(t) = V_{GS_Miller}.e^{\frac{-t}{\tau}} = (\frac{I}{gm(V_{GS})} + V_{th})e^{\frac{-t}{\tau}} \tag{1.25}$$

So, the period period t_{fi} is expressed as :

$$V_{GS}(t_{fi}) = V_{th} \Leftrightarrow t_{fi} = \tau.ln(\frac{V_{GS_Miller}}{V_{th}}) \tag{1.26}$$

The parasitic inductances will play a dual limiting role and create an additional overvoltage on V_{DS} due to the negative $\frac{di_D}{dt}$.

(F) **Stabilization period Δt_{off}:** At this stage, the current switching is complete, and all the load current is directed to the diode, which means that $I_{Diode} = I$. The transistor is fully turned off, allowing V_{GS} to reach V_{Dr-} according to the time constant τ. During this interval, oscillations may occur between the output capacitance C_{OSS} and the stray inductances.

The MOSFET being a voltage-controlled device, the parasitic capacitances impact the charging and discharging processes, affecting the timing and phases of the switching waveforms. Additionally, the gate resistor (or parasitic resistance not shown in the figure) limits the current, while stray inductance opposes changes in current. Together, these factors can slow the rise and fall times of the MOSFET's current waveforms, ultimately reducing the switching speed. Figure 1.14 from [22] illustrates various (Si) MOSFET switching waveforms obtained from simulations with different values of L_S and L_D, emphasizing their impact on the switching behavior of the MOSFET. To summarize, the stray inductances L_G, L_S, and L_D affect the switching behavior in the following ways:

- L_G: The gate inductance and the transistor's input capacitance can form an oscillator, resulting in very high commutation losses. However, changes in gate inductance have minimal impact on the waveforms [18].

- L_S: the parasitic inductance at the source is common to both the power loop and the control loop circuits. In consequence, it interacts with the driver

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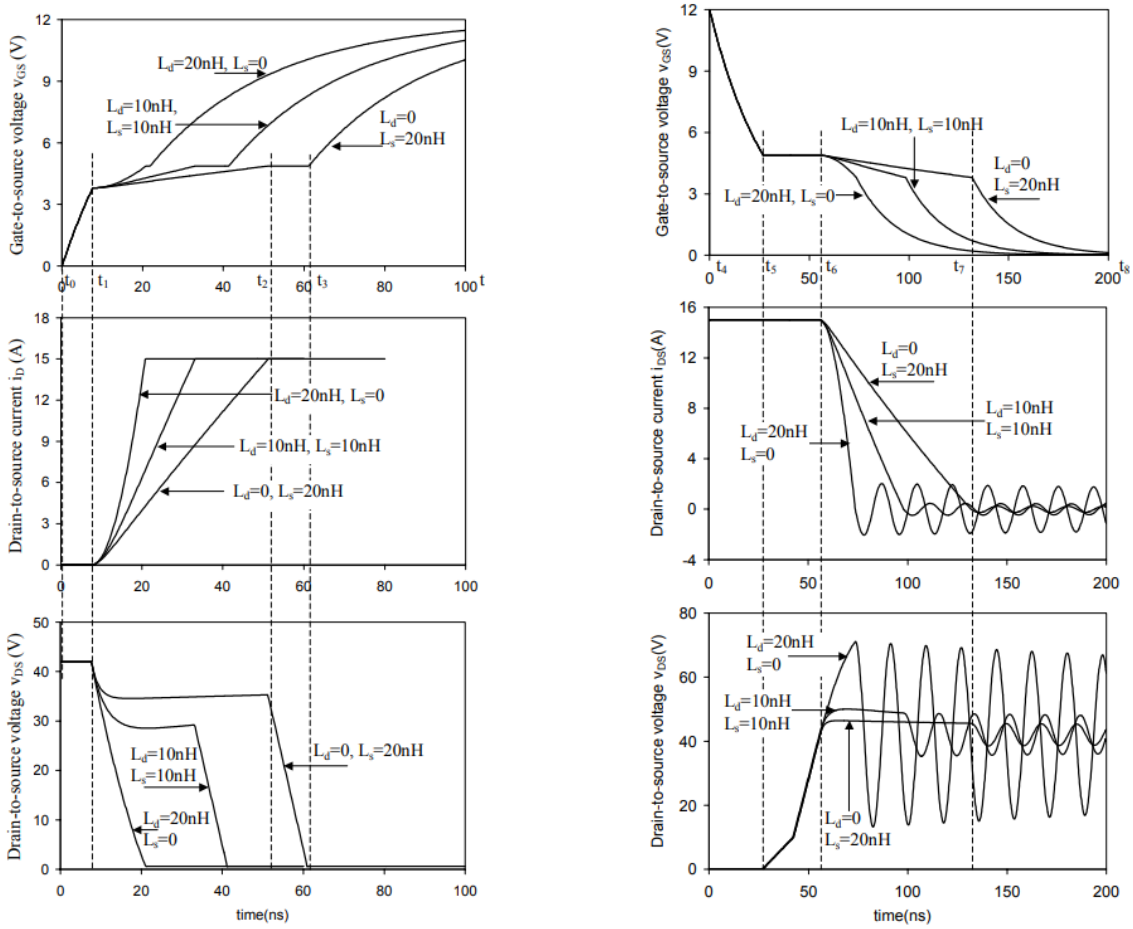

Figure 1.14: (a) turn-on waveforms ($v_{GS}(t)$, $i_{0D}(t)$ and $v_{DS}(t)$) with different L_d andL_s conditions and (b) the corresponding turn-off waveforms (simulation) [22].

circuit, creating a feedback effect that delays switching, thereby increasing switching losses.

- L_D: the drain inductance reduces the drain voltage while the turn-on in such a manner that it reduces turn-on losses. Nonetheless, it generates an overvoltage that increases the turn-off losses and ringing in the voltage and current waveforms during switching, leading to signal integrity issues and even device damage due to voltage spikes.

2.2.2 Power losses in Semi-conductors switches

As discussed in the previous section, the switching process of semiconductor devices in power converters is non-ideal, resulting in significant power losses. These losses are a critical factor in the design of power electronic systems, as they directly impact the overall efficiency of power converters. Here, we discuss switching ad conduction losses in more detail.

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Switching losses

When a semiconductor device switches, as illustrated in the MOSFET waveform figures 1.12 and 1.13, there are distinct transitions for the rise and fall of both current and voltage. At this time, both the voltage across the device and the current flowing through it are not zero simultaneously, resulting in power dissipation in the form of heat. The average power can be directly expressed by:

$$\begin{aligned} P_{Sw} &= \frac{1}{T_{Sw_on}} \int_0^{T_{Sw_on}} V_{DS}(t).I_D(t)dt + \frac{1}{T_{Sw_off}} \int_0^{T_{Sw_off}} V_{DS}(t).I_D(t)dt \\ &\approx (E_{on} + E_{off}).f_{sw} \end{aligned} \tag{1.27}$$

Where the switching frequency is denoted as f_{sw}, T_{Sw_on} and T_{Sw_off} represent the durations of the switching events, E_{on} and E_{off} represent the energies of the turn-on and turn-off transitions, respectively.

These energy losses can be calculated considering linear variations of the voltage and the current during the rise and fall times. In figure 1.12, the approximated turn-on waveform current rise t_{ri} and voltage fall t_{vf}periods can be divided into two periods each. At the period t_{fi1}, the drain current I_D increases to the load current I, while the voltage $V_{DS} = E - \Delta V$, where the voltage drop ΔV is caused by the parasitic inductances (equation 1.10). The energy can be computed as follows, considering $\frac{di_D(t)}{dt} = \frac{I}{t_{ri1}}$:

$$E_{on1} = \frac{(E - \Delta V).I.t_{ri1}}{2} = \frac{(E - \Delta V).I^2}{2.\frac{di_D(t)}{dt}} \tag{1.28}$$

In the second period of the current rise, we have the diode recovery phenomena effect, so the drain current increases to the value $I + I_{rr}$ with a current slope of $\frac{di_D(t)}{dt} = \frac{I_{rr}}{t_{ri2}}$. The corresponding energy is expressed by :

$$E_{on2} = (E - \Delta V).(I + \frac{I_{rr}}{2}).t_{ri2} = (E - \Delta V).(2I.I_{rr} + I_{rr}^2).\frac{dt}{2.di_D} \tag{1.29}$$

During the voltage fall period, V_{DS} decreases to the on-state voltage V_{DS_on}. In the initial part of this period, t_{fv1}, which concludes when the drain current I_D reaches the load current I, the current decreases with a slope of $\frac{di_D(t)}{dt} = \frac{I_{rr}+I}{t_{vf1}}$

$$E_{on3} = (E - \Delta V).(\frac{I}{2} + \frac{I_{rr}}{3}).t_{fv1} = (E - \Delta V).(\frac{I}{2} + \frac{I_{rr}}{3}).\frac{I_{rr} + I}{\frac{di_D(t)}{dt}} \tag{1.30}$$

During the second part of the Voltage fall period, t_{fv2}, the voltage slope of the

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voltage fall is approximately $\frac{dV_{DS}(t)}{dt} = \frac{E-\Delta V}{t_{fv2}}$. So the Energy is expressed as :

$$E_{on4} = (E - \Delta V).I.t_{fv2} = \frac{(E - \Delta V)^2 I}{\frac{dV_{DS}(t)}{dt}} \tag{1.31}$$

So, the turn-on energy losses are :

$$E_{on} = E_{on1} + E_{on2} + E_{on3} + E_{on4} \tag{1.32}$$

In Fig 1.13, the turn-off transient that contributes to energy losses can be divided into two phases: voltage rise t_{rv} and current fall time t_{fi}. This energy is expressed by:

$$E_{off} = (E + \Delta V).I.(t_{rv} + t_{fi}) \tag{1.33}$$

Conduction losses

In its on-state, a MOSFET behaves like a resistor (R_{DSon}). The conduction losses in the MOSFET are a result of the joule heating in that resistor. If $I_{D_{rms}}$ represents the root-mean-square (RMS) current passing through the MOSFET, then the conduction losses can be expressed as follows:

$$P_{Cond} = R_{DSon}(T).I^2_{D_{rms}} \tag{1.34}$$

The on-state resistance R_{DSon} of a MOSFET is strongly influenced by the temperature T. The typical temperature dependence of R_{DSon} can be expressed as:

$$R_{DS(on)}(T) = R_{DSon}(T_0) \cdot (1 + \alpha \cdot (T - T_0)) \tag{1.35}$$

Where:

$$\begin{cases} R_{DS(on)}(T_0) & \text{: the on-state resistance at a reference temperature } T_0 \ [\Omega] \\ \alpha & \text{: the on-state resistance temperature coefficient} \\ T_0 & \text{: the reference temperature in } [^\circ\text{C}]. \end{cases}$$

The diode demonstrates fast switching characteristics, resulting in minimal energy dissipation during turn-on or turn-off events. As a result, the switching losses in a diode are considered negligible compared to conduction losses. The conduction losses primarily originate from the forward voltage drop V_F that occurs during conduction. For a diode forward current I_{Diode}, the power losses in the diode can be expressed

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as :

$$P_{cond_diode} = V_F(T).I_{Diode} \tag{1.36}$$

Where V_F varies with the temperature[23], and can typically be expressed by [24]:

$$V_F(T) = \frac{n(T)kT}{q} ln(\frac{I_{Diode}}{I_S(T)} + 1) \tag{1.37}$$

Where:

$$\begin{cases} I_S(T) & \text{: Saturation current at temperature T.} \\ q & \text{: Charge of an electron } (1,602.10^{-19}C). \\ n & \text{: Ideality factor.} \\ k & \text{: Boltzmann constant } (1,381.10^{-23}J/K). \end{cases}$$

2.2.3 Conclusion

Parasitic capacitance and inductance significantly impact the switching dynamics of power semiconductor devices, affecting switching losses and the overall efficiency of power converters. A solid understanding and careful mitigation of these effects through design and modeling are essential for improving the performance of high-frequency power electronics. However, accurately extracting and simulating these parasitic elements is a complex and challenging task. To overcome these challenges, advanced modeling techniques and precise measurement tools are essential for optimizing power converter designs, minimizing switching losses, and enhancing overall system performance. Moreover, the combination of high losses and rising temperatures can lead to destructive thermal runaway, where excessive heating causes the semiconductor devices to fail, damaging the entire system. Therefore, it is critical to consider simultaneously the thermal management and the minimization of parasitic effects to ensure the reliability and longevity of power conversion systems.

2.3 Cooling

Effective thermal management is essential for ensuring the reliability and longevity of power converters, as temperature fluctuations can significantly impact the performance of semiconductor devices. A 10 °C temperature increase can halve a device's lifetime, with this effect becoming even more severe at higher temperatures [25]. Temperature rise accounts for approximately 55% of failures in electronic equipment, making it the leading cause of failure [26]. Consequently, it is crucial to consider both the thermal behavior and cooling requirements of power converter components, particularly within printed circuit boards (PCBs). Power semiconduc-

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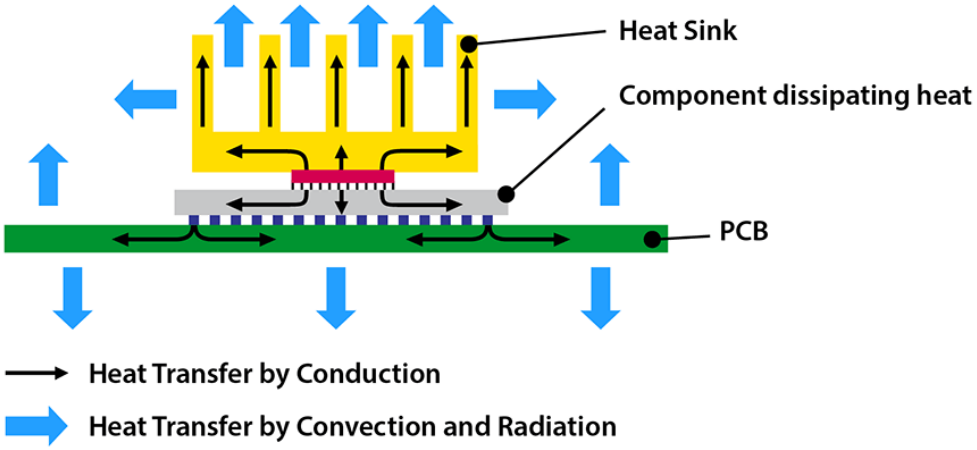

Figure 1.15: Heat transfer for electronics [27].

tors are highly temperature-sensitive. Their key properties such as ON-resistance, threshold voltage, and overall performance are directly affected by temperature. This makes precise temperature control critical for both short-term and long-term system stability.

Coupled electrical and thermal models allow designers to accurately predict temperature variations over time and implement effective cooling strategies. This proactive approach ensures the system operates within safe thermal limits, preventing damage and improving reliability. This section summarizes how heat can be removed from a system via conduction, convection, and radiation.

2.3.1 Heat propagation

The propagation of heat in a system can take place in three different ways, convection, heat radiation or heat conduction.

Heat conduction

The thermal conduction can described with the differential form of Fourier's law, where the heat flux density is the amount of energy that flows through a unit area per unit of time:

$$\phi = -\lambda \nabla T \quad \text{With} \quad \begin{cases} \phi\,[W.m^{-2}] & : \text{local heat flux density} \\ \lambda\,[W.m^{-1}.K^{-1} & : \text{material's conductivity} \\ \nabla\, T[K.m^{-1}] & : \text{temperature's gradient} \end{cases} \tag{1.38}$$

This type of heat transfer is particularly significant in solid materials that exhibit good thermal conductivity, typically ranging from $10 \leq \lambda \leq 400\, W.m^{-1}.K^{-1}$. In

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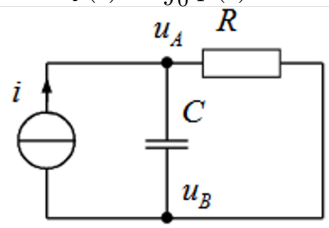
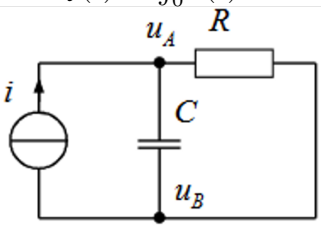
Thermal equation	Electrical equation
$C_{th} = \frac{dQ}{dT}$	$C = \frac{dQ}{dU}$
$C_{th} = c.\rho.d.S$	$C = \epsilon\frac{S}{d}$
$R_{th} = \frac{d}{\lambda.S}$	$R = \frac{d}{\sigma.S}$
$Q(t) = \int_0^t p(t)dt$	$Q(t) = \int_0^t i(t)dt$
	
$p(t) = \frac{T_A(t)-T_B(t)}{R_{th}} + C_{th}\frac{d(T_A(t)-T_B(t))}{dt}$	$i(t) = \frac{u_A(t)-u_B(t)}{R} + C\frac{d(u_A(t)-u_B(t))}{dt}$

Table 1.2: Equivalent circuit

liquids, thermal conductivity is less important, with values between $0.1 \leq \lambda \leq 1\,W.m^{-1}.K^{-1}$. In gases, thermal conductivity is negligible, at approximately $\lambda \approx 0.03\,W.m^{-1}.K^{-1}$.

For non-steady-state conduction, the heat transfer in solid materials can be expressed in the following form:

$$\nabla(\lambda\nabla T)+p_v = \rho C_p\frac{\partial T}{\partial t} \quad \text{With} \quad \begin{cases} t & \text{: Time} \\ p_v\,[W.m^{-3}] & \text{: Power density} \\ \rho\,[kg.m^{-}3] & \text{: Specific weight of the material} \\ C_p\,[J.kg^{-1}.K^{-1}] & \text{: Specific heat capacity of the solid for a constant pressure} \end{cases} \tag{1.39}$$

According to eq (1.39), heat conduction behaves similarly to the law of electrical charge conduction in an equivalent transmission line composed solely of resistance and capacitance. Thus, an analogy can be drawn between the electrical and thermal variables.

Thermal variables			Electrical variables		
T	Temperature	$[K]$	U	Voltage	$[V]$
ϕ	Power density	$[W.m^{-2}]$	J	Current density	$[A.m^{-2}]$
P	Heat flow	$[W]$	I	Current	$[A]$
Q	Heat	$[J] = [W.s]$	Q	Electrical charge	$[C] = [A.s]$
λ	Thermal conductivity	$[W.K^{-1}.m^{-1}]$	σ	Electrical conductivity	$[\Omega^{-1}.m^{-1}]$
R_{th}	Thermal resistance	$[J] = [K.W^{-1}]$	R	Resistance	$[V.A^{-1}] = [\Omega]$
C_{th}	Thermal capacitance	$[J.K^{-1}]$	C	Capacitance	$[A.s.V^{-1}] = [F]$

Table 1.1: Equivalence physical variables

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Heat convection

Convection is the process of heat transfer that occurs through the mass movement of a fluid, such as air or water. The mass movement can be forced, using a pump or a fan, or occur naturally: when a fluid is heated, it expands, becomes less dense, and rises away from the heat source, carrying energy with it. For instance, when air is heated above a hot surface, it rises due to its lower density. Similarly, hot water is less dense than cold water, causing it to rise and create convection currents that transport energy.

Convective thermal transfer can be formulated as:

$$\phi = h\Delta T \qquad \text{with} \qquad h[W.m^{-2}.K^{-1}]: \text{ Heat transfer coefficient} \tag{1.40}$$

The convective heat transfer coefficient is influenced by the physical properties of the fluid and the specific conditions of the fluid flow. This parameter varies based on several factors affecting convection, including surface geometry, the nature of fluid motion, fluid properties, and the bulk fluid velocity. For natural convection, the value of the convective heat transfer coefficient is approximately $h = 5\ W.m^{-2}.K^{-1}$, while for forced-circulation water cooling, it can reach $h = 50\ kW.m^{-2}.K^{-1}$.

In general, the convective heat transfer coefficient for laminar flow is relatively low compared to that for turbulent flow. This is because a turbulent flow forces mixing, reducing the stagnant fluid film layer at the liquid/solid interface.

Heat radiation

The power radiated by a surface with an emissivity ε at an absolute temperature T , over all wavelengths, is calculated using:

$$\phi = \sigma[\varepsilon(T)T^4 - \varepsilon(T_0)T_0^4] \tag{1.41}$$

With $\begin{cases} \sigma = 5,67.10^{-8}\ W.m^{-2}.K^{-4} & : \text{Stefan-Boltzmann's constant} \\ \varepsilon(T)\ \&\ \varepsilon(T_0) & : \text{Surface emissivity where T is the temperature} \\ & \text{of the hot surface and } T_0 \text{ that of the environnement} \end{cases}$

In most applications, the fraction of power removed thanks to radiation is considered negligible. However, numerous research projects have shown that heat radiation can represent a significant portion of the total power dissipation capability. This can be modified by managing the cooler's surfaces to enhance their emissivity, which in turn decreases the overall thermal resistance. For example, in the study referenced in [28], coolers coated with black paint exhibit four times greater heat radiation than

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aluminum heat sinks.

2.4 EMI

Electromagnetic Interferences (EMI) poses considerable challenges in the design of power converters, especially when utilizing WBG semiconductors such as SiC and GaN. While these semiconductors provide high efficiency and support high-frequency switching, their rapid switching capabilities can lead to significant electromagnetic disturbances, highlighting the importance of addressing EMI in the design process. The primary sources of EMI in these systems are the rate of current change ($\frac{di(t)}{dt}$) and the rate of voltage change ($\frac{dv(t)}{dt}$) during switching events. When a current changes rapidly, especially around inductive components like transformers or inductors, it generates fluctuations in the magnetic field, which can couple with other parts of the circuit. Similarly, fast voltage transitions can cause parasitic capacitances in the circuit to discharge or charge quickly, allowing high-frequency noise to circulate through the circuit and interfere with nearby electronics, affecting system performance.

EMI can be categorized into two main types: radiated and conducted. Radiated EMI occurs when high-frequency signals generated by rapid switching transitions spread through the air as electromagnetic waves. Cables carrying these high-frequency signals or power can act as antennas, emitting electromagnetic waves that may interfere with nearby electronic systems. This kind of EMI can disrupt sensitive electronics, such as communication systems or audio equipment.

In contrast, conducted EMI involves noise that propagates through power lines or ground planes within the electronic system. High-frequency voltage and current spikes generated during switching can travel along these paths, potentially interfering with the operation of other equipment and leading to violations of regulatory EMI standards. In power electronics, EMI signals are often categorized into two main types: Differential-Mode (DM) and Common-Mode (CM). Fig. 1.16 shows the current flows for both modes. This distinction is crucial for understanding how noise can influence circuit performance and for implementing mitigating measures.

- DM noise is represented by the red current path in Fig. 1.16. It primarily occurs along power and signal lines between two conductors with opposite polarity. Additionally, it can radiate into the environment, especially if the circuit layout features large current loops or involves high-frequency switching currents.

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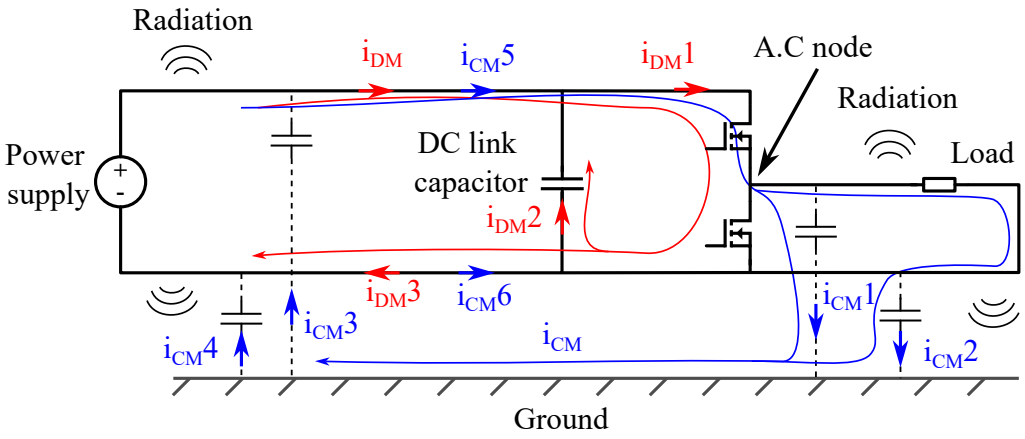

Figure 1.16: Electromagnetic source in a commutation cell

- CM noise is depicted by the blue current path in Fig. 1.16. It typically arises from noise coupling between a conductor, such as the switching node, and a common reference point, like the ground plane. The return path of the CM currents "escaping" from a converter is un-controlled and may involve other electronic systems, making CM current particularly prone to causing inteferences.

2.5 Conclusion

Managing parasitic elements in a power switching cell is key to optimizing performance. Stray inductances and capacitances significantly impact conduction and switching losses, affecting the overall efficiency of power converters. High efficiency is crucial for reducing energy consumption and operational costs and minimizing thermal stress on components. Excessive heat can harm reliability, reduce lifespan, and lead to more complex thermal management, increasing size and cost. These parasitic elements also influence the electro-magnetic emissions from converters, and are responsible for a large part of EMI issues.

The next section describes packaging strategies which allow for managing all these factors. This is essential to ensure the system works efficiently, and the components function together seamlessly.

3 Packaging

Packaging, as defined by Hopkins [29], "[..] is the arranging of physical components to provide a function or characteristic that is compatible with external interfacing elements." In power converters, this concept extends beyond the electrical components to include thermal management, layout design, and the overall

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mechanical structure of the PCB. Specialized PCB packaging plays a vital role in effectively managing electrical, thermal, and mechanical stresses. As mentioned in the previous section, parasitic components like inductances and capacitances can significantly affect switching behavior, leading to increased losses, ringing, and higher electromagnetic interferences (EMI), all of which degrade system efficiency and performance. To address these challenges [30, 31], the primary objectives of PCB packaging are to ensure efficient thermal dissipation for system stability, handle high currents and voltages to minimize power losses and EMI, provide mechanical robustness to withstand vibrations and shocks and enable compact, space-efficient designs. Additionally, long-term reliability is essential to maintain consistent performance, particularly in harsh environments.

3.1 Package design guidelines

3.1.1 Gate inductance

The gate circuit can be analyzed as an RLC circuit :

$$v_{Driver}(t) = L_G.\frac{di_G(t)}{dt} + i_G(t).R_G + v_{GS}(t) \tag{1.42}$$

replacing the gate current by $i_G(t) = C_{GS}.\frac{dv_{GS}(t)}{dt}$, and applying the Laplace transformation, the gate driver transfer function can be written as :

$$H(s) = \frac{v_{GS}(t)}{v_{Driver}(t)} = \frac{\frac{1}{L_G.C_{GS}}}{s^2 + \frac{R_G}{L_G}s + \frac{1}{L_G.C_{GS}}} \tag{1.43}$$

By analysing this equation using the standard form of a second-order system, and considering the damping ratio ζ, the gate loop inductance L_G can be expressed as [32]:

$$\zeta = \frac{R_G}{2}.\sqrt{\frac{C_{GS}}{L_G}} \Rightarrow L_G = \frac{C_{GS}.R_G^2}{4\zeta^2} \tag{1.44}$$

To prevent destructive voltage spikes in power converter designs (for a damped system where $\zeta \geq 1$), two primary approaches can be derived from eq. (1.44). One option is to increase the gate resistance, which helps dampen oscillations, at the cost of reduced switching speed. The more effective solution, however, is to minimize the gate inductance L_G, which significantly improves the performance of the gate drive circuit.

For safe operation, the gate inductance of SiC MOSFETs should generally be

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kept below 20 nH (underdamped). For faster switching and improved efficiency, it is recommended to reduce the gate inductance to less than 5.5 nH [32]. For GaN devices, which switch faster, primarily due to their lower gate capacitance, a reliable range for the gate inductance is between 1–2 nH [33, 34].

3.1.2 Gate and power circuit coupling

Minimizing the coupling between the gate and power circuits is essential for optimizing switching performance. One effective technique is to use a separate ("Kelvin") Source connection for the gate circuit. This method isolates the gate current path from the power path, ensuring that the gate voltage remains stable and preventing fluctuations caused by the power circuit's switching events. Additionally, careful design strategies that minimize mutual inductance and capacitance help ensure that the gate drive circuit operates independently of the power circuit.

3.1.3 Power loop inductance L_{loop}

In power converter systems, one critical design constraint is to ensure that the turn-off overvoltage ($\Delta V = k.E$, Fig. 1.17a) does not exceed 10% ($k \leq 0.1$) of the cell's input voltage E [35]. This constraint prevents component failure, thermal damage, or performance degradation. The overvoltage ΔV is mainly caused by parasitic inductances within the commutation loop L_{loop}, which includes the inductances from semiconductor packages, PCB traces, and capacitor leads. During the MOSFET turn-off, this inductance generates an overvoltage given by $\Delta V \approx L_{loop} \cdot \frac{\Delta I}{\Delta t}$, where $\Delta t \approx t_{fi}$ is the switching transition duration, and I is the load current. One way to manage this matter is to determine the maximum allowable parasitic inductance L_{loop} based on the converter's impedance and the switching speed of the components (duration of current variation t_{fi}) [36]:

$$L_{loop} \leq \frac{k.E}{\frac{I}{t_{fi}}} = k.t_{fi}.Z \quad \text{with} \quad Z = \frac{E}{I} \tag{1.45}$$

A graphical representation (Figure 1.17b) shows how the required inductance limits change with different t_{fi} values and converter impedances. Adhering to these limits ensures that overvoltage stays below 10% during turn-off, which aids in selecting the right components and designing a reliable converter. For designs using wide-bandgap (WBG) semiconductors, the goal is typically to maintain a parasitic inductance L_{loop} of less than 1 nH [37].

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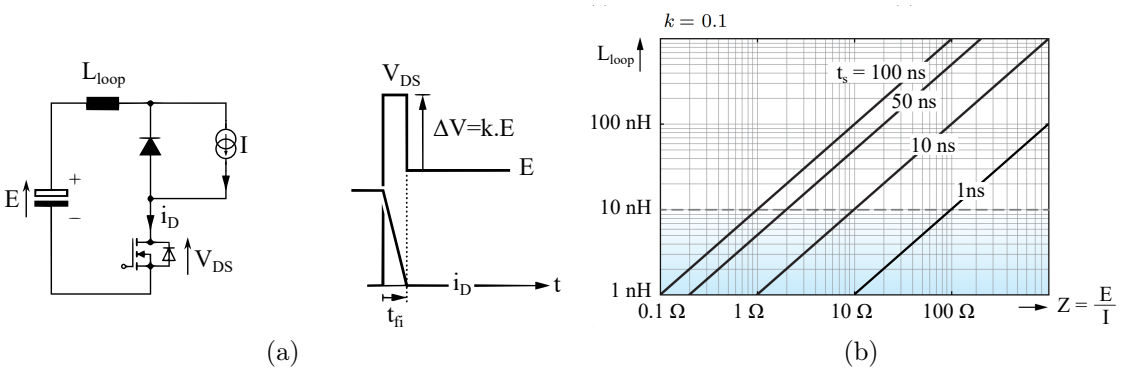

Figure 1.17: The impact of parasitic commutation loop inductance on switching overvoltages during turn-off event(a) Power loop inductance in a switching cell and its voltage overshoot $\Delta V = k.E$ for the current transition time t_{fi}.(b) Z and Ls to achieve a specific switching period while limit the overvoltage to 10% of the input voltage E [36].

3.1.4 Electromagnetic Compatibility (EMC)

Compliance with electromagnetic compatibility (EMC) regulations, such as those set by the International Electrotechnical Commission (IEC), is crucial for ensuring safety and reliability. This issue becomes particularly significant when using wide-bandgap (WBG) semiconductors, which offer fast switching speeds but can also generate substantial EMI. To effectively reduce these interference effects, it is important to implement a variety of strategies that can help reduce any unwanted interference.

One widely used technique is to incorporate snubber circuits which effectively dampen voltage and current spikes during switching events, thereby reducing the impact of $\frac{dv(t)}{dt}$ and $\frac{di(t)}{dt}$. A well-designed PCB layout is also crucial; techniques such as minimizing trace lengths, ensuring proper grounding, and placing decoupling capacitors near sensitive components help decrease parasitic inductance and capacitance, both of which contribute to EMI. Additionally, utilizing shielding techniques is a common practice that helps contain electromagnetic waves, preventing them from radiating into adjacent circuits.

Another established method involves employing soft switching techniques, such as Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS), which can further reduce the abruptness of switching transients, leading to lower EMI generation. Finally, integrating EMI filters at both the input and output stages is a well-recognized approach that effectively suppresses high-frequency noise conducted through power lines, enhancing overall system performance and compliance.

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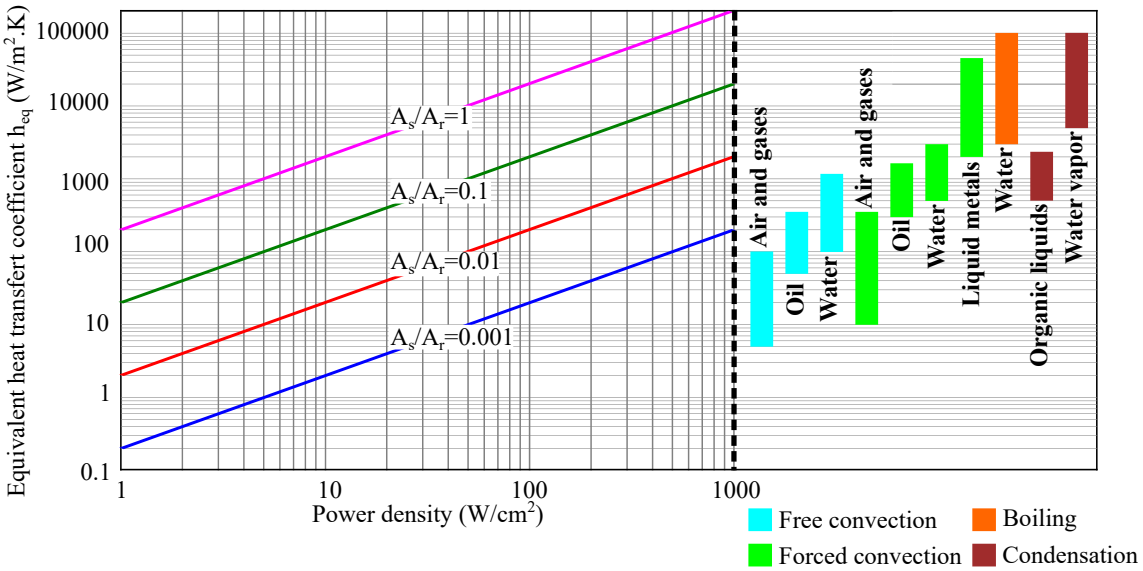

Figure 1.18: Equivalent convective heat transfer coefficient as a function of loss density for an arbitrarily set temperature rise ΔT of 50°C [37] and the different fluids and cooling modes for the corresponding h_{eq} range[38].

3.1.5 Thermal management

Among their many advantages, WBG semiconductor devices are physically smaller than their silicon counterparts for the same voltage and current ratings, allowing for converter size reduction. However, this also results in higher loss density and requires improved thermal management solutions. Indeed, a crucial aspect of thermal management is the surface area ratio between the heat source and the cooling surface $\frac{A_s}{A_r}$. A mathematical relationship can be formulated to describe the connection between the equivalent heat transfer coefficient h_{eq} and the thermal resistance R_{th}, which incorporates the heat source surface area A_s and the cooling surface area A_r[37]:

$$\frac{1}{h_{eq}} = R_{th}.A_r = \frac{\Delta T}{\frac{P}{A_s}\frac{A_s}{A_r}} \quad \text{With} \quad \begin{cases} A_s\,[m^2] & : \text{heat source surface area} \\ A_r\,[m^2] & : \text{cooling surface area} \\ P\,[W] & : \text{dissipated power at the source} \\ R_{th}\,[K.W^{-1}] & : \text{package thermal resistance} \end{cases} \tag{1.46}$$

Fig. 1.18 illustrates the application of eq. (1.46) to determine the heat coefficient required as a function of injected power density for various surface area ratios $\frac{A_s}{A_r}$ to maintain a fixed temperature rise of 50 °C. Additionally, it explores the possible cooling solutions based on the ranges of the equivalent heat coefficient h_{eq}. From this analysis, it is clear that a lower surface area ratio (i.e., a larger cooling surface relative to the heat source) reduces the cooling effort required. However, this typically

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results in a larger system volume, which can reduce the converter's volumetric power density. On the other hand, a higher surface area ratio allows for more compact designs with more efficient heat dissipation but may require additional cooling efforts to maintain high power density.

Reducing the temperature rise from the heat source to the cooler, which essentially means decreasing the thermal resistance, is a crucial strategy. This involves optimizing the internal structure of the power converter to create a more efficient heat path. Effective packaging ensures that the heat generated by the semiconductor chip is efficiently transferred to the external cooling system. This can be accomplished using materials with high thermal conductivity and low thermal resistance.

3.1.6 Reliability and Long-Term Performance

Packaging designs must ensure long-term reliability and performance by effectively managing mechanical stress caused by thermal cycling and vibration. This can be achieved by using materials with matching coefficients of thermal expansion (CTE) and robust bonding techniques. Bonding wires significantly contribute to power module failures, so reducing their reliance is essential to improving module reliability. In addition, encapsulation materials must protect devices from environmental factors such as humidity, dust, and corrosive elements. Packaging should also account for moisture sensitivity levels (MSLs) and employ materials that can withstand high temperatures to enhance durability and ensure consistent and reliable operation.

3.1.7 Fabrication Flexibility and Cost Considerations

Fabrication flexibility and cost are particularly important criteria regarding packaging. Materials such as ceramics (like aluminum oxide), copper, and aluminum offer a good mix of performance and affordability. They excel in thermal conductivity, electrical properties, and mechanical strength. However, ceramics can be brittle and tricky to work with, while copper and aluminum might need advanced techniques to dissipate heat and maintain mechanical integrity efficiently. There are also advanced materials like graphite and diamond that perform exceptionally well thermally, but they come with a high price tag or integration challenges in standard manufacturing processes.

Several manufacturing techniques are available, including die attach, wire bonding, flip-chip bonding, sintering, and injection molding. However, these methods have their drawbacks. For example, die-attach using silver-filled epoxy or solder can

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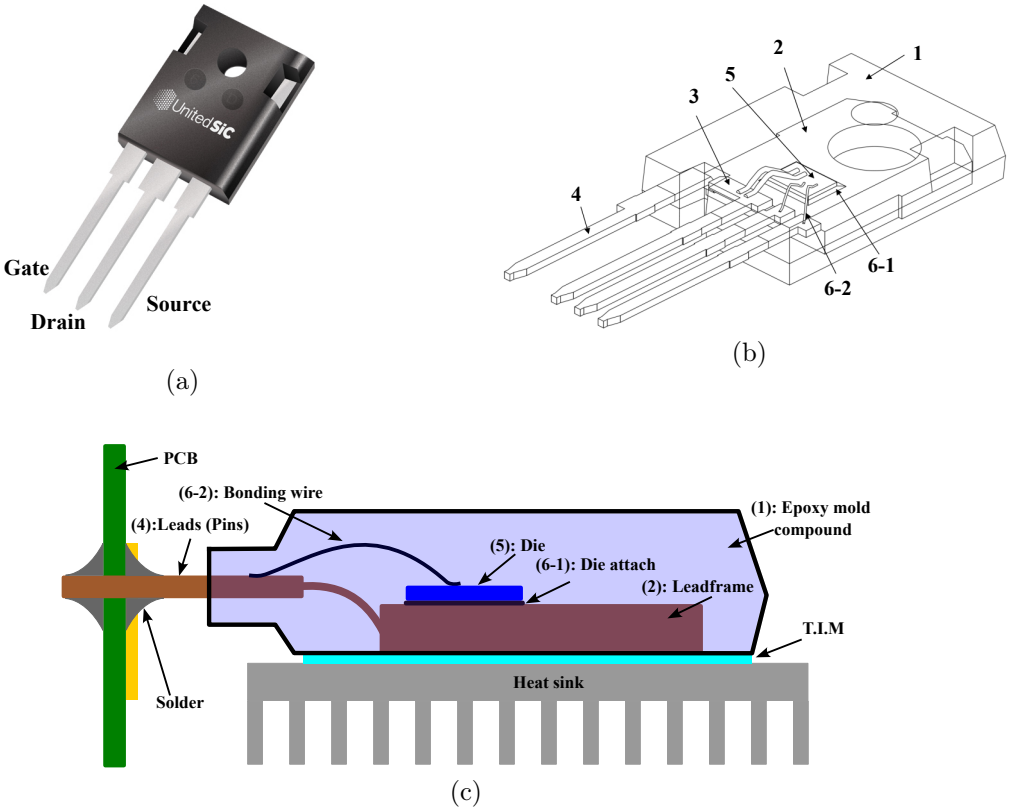

Figure 1.19: Overview of discrete components in power Electronics: TO-247 Packaging Structures: (a) TO-247-3 United SiC FET (UJ3C120150K3S) N-Channel 1200V, 18.4A in TO-247-3 Packaging; (b) Internal Structure Example of ROHM Semiconductor's TO-247-4 [39]; (c)Cross-section View of TO-247 with Through-Hole Soldering and Heat Sink Configuration.

lead to long-term reliability issues at high temperatures. Wire bonding and flip-chip bonding need careful handling to avoid damaging sensitive components, while sintering can be both complex and costly. Injection molding is a budget-friendly option but may restrict design flexibility for more intricate shapes, and is suited to large volume manufacturing because of high tooling costs.

3.2 Power Electronics Packaging Technology

3.2.1 Classical Packaging Approaches

The packaging methods have evolved to meet the increasing performance demands of modern components. Initially, classical packaging used discrete components mounted on printed circuit boards (PCBs) (Figs. 1.19 and 1.20 or power modules with Direct Bond Copper (DBC) substrates (Fig. 1.22), which are adequate for low- to medium-power applications. For PCB technology, discrete components can be mounted using through-hole or surface-mount technologies (SMT). Surface-mount components, which are more compact, are soldered directly onto the surface of the PCB, eliminating the need for drilled holes. SMT offers several advantages,

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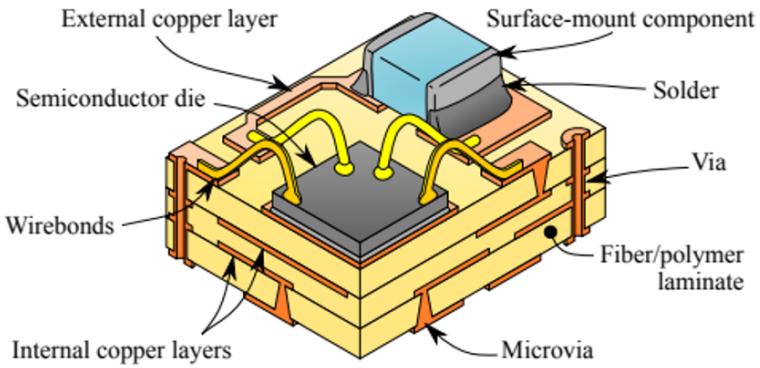

Figure 1.20: Multi-layer PCB

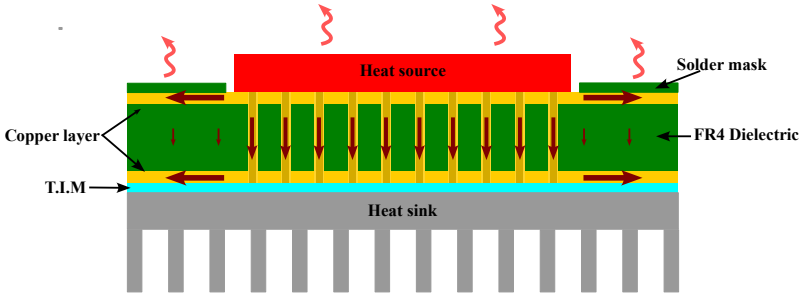

Figure 1.21: The principle heat transfer paths for a 2-layer PCB involve the use of thermal Vias[40].

including higher density, improved reliability, and reduced assembly costs.

The TO-247 package is a popular choice for power semiconductor devices in traditional PCB assemblies (Fig. 1.19). This robust through-hole package includes a metal tab for efficient thermal conduction. The TO-247 is mounted on a PCB by inserting its leads through holes (Fig. 1.19c), ensuring stable mechanical and electrical connections. A heat sink is added using thermal interface material (TIM) to enhance heat dissipation.

Inside the TO-247 (Fig. 1.19b), a semiconductor die is bonded to a copper tab (2), with wire bonding (6-2) connecting the die (5) to the external leads (4). The TO-247-3 (Fig. 1.19a) version features three leads for standard power applications, but these leads introduce stray inductance ranging from 6 nH to 15 nH. In contrast, the TO-247-4 (figure 1.19b), provides an additional Kelvin source configuration, separating control and power paths for the source. This minimizes control/power coupling, as discussed in section 3.1.2, and therefore limits the detrimental effects of the source stray inductance.

SMT components are directly mounted on a PCB, so they cannot be directly attached to a heatsink. Copper and FR-4 materials (the class of dielectric materials used in PCBs) have distinct thermal conductivities that impact heat management in PCBs. Copper exhibits a high thermal conductivity (398 W/m·K), enabling

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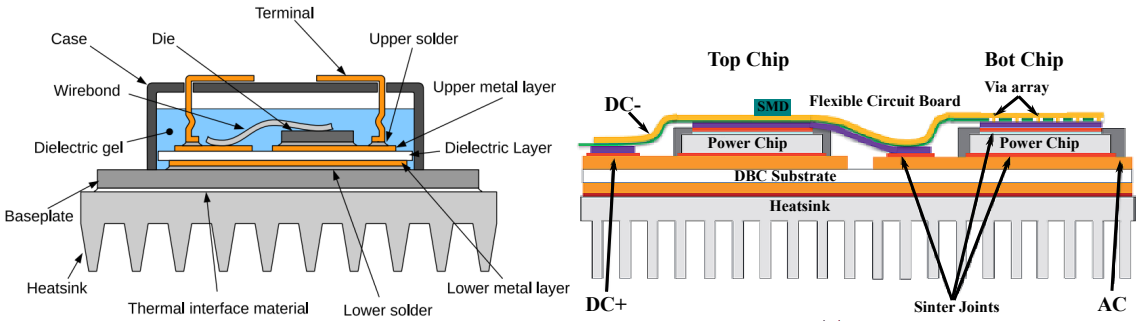

(a) (b)

Figure 1.22: Power Module Packaging: (a) Internal Structure of a Power Module Using the DBC Approach [41]. (b) SKIN DBC Module Packaging Approach, in which wire-bonds are replaced with a flexible PCB [42].

rapid heat distribution and preventing component overheating, while FR-4's low conductivity (0.3 – 0.4 W/m·K) can cause heat buildup and hotspots. To enhance thermal management, thermal vias (Fig. 1.21) provide pathways for heat to travel from power components to lower layers or heat sinks. Their size, number, and placement are crucial for optimal performance. Additionally, copper layers help distribute heat evenly. For high-performance applications, multilayer PCBs with embedded heat spreaders utilize multiple copper layers to efficiently disperse heat.

For power modules (Fig. 1.22), DBC substrates are commonly employed, consisting of a ceramic layer (typically aluminum nitride) bonded to a copper layer. The copper offers excellent thermal conductivity, while the ceramic provides electrical insulation, ensuring efficient heat dissipation from power components like IGBTs and MOSFETs.

3.2.2 Novel packaging approaches

As power electronics have advanced to higher power levels and faster switching frequencies, the limitations of traditional packaging methods have become more apparent. Current packaging technology primarily relies on assembling pre-made discrete components, each consisting of multiple parts manufactured using different processes. This complexity makes it difficult to reduce both the cost and size of converters [43].

Advanced packaging solutions have been developed to overcome these challenges, while simultaneously minimizing parasitic inductances and optimizing thermal management. One significant innovation is the introduction of 3D packaging, which offers greater flexibility in routing and improves cooling by adding additional heat dissipation surfaces. This approach effectively reduces the impact of parasitic elements and enhances the performance of components, especially those using wide bandgap

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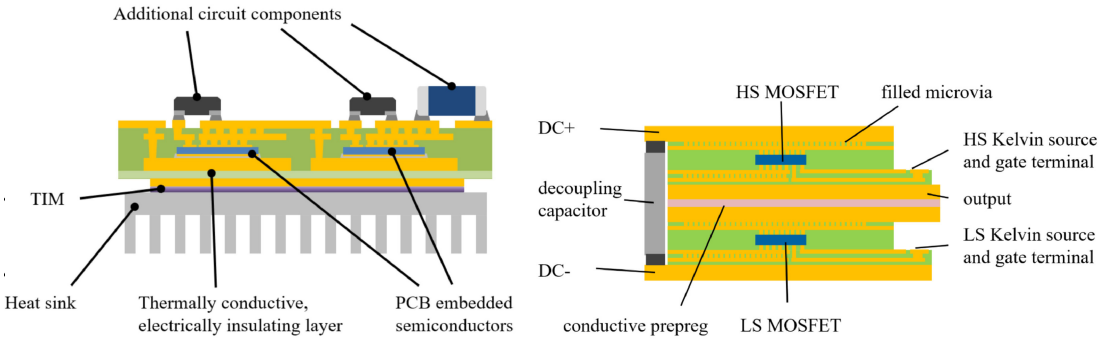
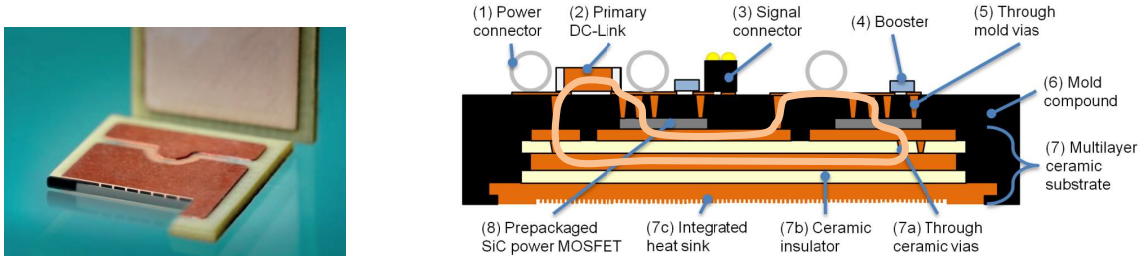


(a) (b)

Figure 1.23: The PCB Embedding Technique: (a) Semiconductor Die Embedded in PCB [44]. (b) Power Chip-on-Chip (PCOC) Module [45].



(a) (b)

Figure 1.24: (a) Rohm SiC MOSFETs [46] are prepackaged into a PCB. (b) Example of a multi-layer structure with embedded active components and ceramic layers, yielding a very small stray inductance ($L_{loop} \leq 1.6nH$) [47], and small thermal resistance ($R_{th} = 0.53K/W$).

materials like SiC and GaN.

Rigid PCBs face mechanical issues such as cracking, delamination, and solder joint fatigue caused by thermal cycling, high current densities, and vibrations. Flexible PCBs offer a solution by improving stress distribution, vibration resistance, and overall durability. The SKIN technology (Fig. 1.22b), developed by Semikron, uses a flexible PCB to replace wire-bond interconnects. The "Skinfilm" is a three-layer flexible PCB [48], with a thick aluminum upper layer for high currents, a copper lower layer for control circuits, and a polyamide insulating layer in between. Power chips are connected to the lower Skin layer using low-temperature silver sintering, while surface mount components are placed on the top using standard techniques like flip-chip or soldering. However, the complexities of this technology arise from the silver sintering process, which demands careful consideration and development. This is particularly true for the creation of multi-layer boards with thermally conductive Vias, necessitating a specialized approach[42]. Further improvements in power electronics packaging have been achieved by transitioning from wire bonding to Via interconnections, which enhance reliability by providing connections that are more resistant to mechanical stress and thermal expansion. Vias also improve thermal

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management and space efficiency. These advancements, combined with techniques like embedded die and flip-chip mounting, have enabled the shift from traditional 2D to 3D packaging in power electronics (Figs. 1.23a and 1.24).

With the embedding PCB technique, critical electrical components such as semiconductor dies and passive elements are directly inserted into the PCB, eliminating the need for separate packages. In most implementations, bare semiconductor dies are interconnected using laser-drilled microvias (µVias). This approach increases interconnection density, reduces the number of solder joints (which are a common source of failure [49, 50]) and minimizes overall volume. This integration technology enhances electrical and thermal performance by reducing parasitic inductances and eliminating the need for external components. The result is a more compact and efficient design, particularly beneficial for high-frequency and high-power applications.

The embedding PCB technique provides flexibility in integrating power semiconductors. These components can be fully embedded within the PCB, as shown in Fig. 1.23a. In [45], a power chip-on-chip (PCOC) module is presented with stacked high-side and low-side switches using a double-sided µVias embedding process. This design results in two nearly identical submodules laminated together to form a stacked half-bridge. Each switch consists of four parallel SiC MOSFETs, which are impedance-balanced with surface-mount decoupling capacitors. This configuration achieves an extremely low stray power loop inductance ($L_{loop} \approx 0.25\,\text{nH}$) [45]. Alternatively, a hybrid approach can be employed. In the method shown in Figure 1.24a, the semiconductor is prepackaged by PCB embedding technique before it is integrated into the assembly from Fig. 1.24b. This assembly combine the advantages of both direct integration (with the embedding of power devices and allowing SMT components to be mounted on top of the power devices) and traditional packaging (using ceramic insulating layers), leading to improved thermal management ($R_{th} = 0.53K/W$), reduced size, and increased interconnection density($L_{loop} \leq 1.6nH$) [47].

The HI-LEVEL project is an example of fully PCB-based power modules for automotive applications (Fig. 1.25a). In this design, the power chip is sintered onto a thick copper sheet (500 µm), which serves as a heat spreader. The module uses a dielectric layer for electrical isolation, with vias created via laser drilling and copper plating. This method allows for mass production at reduced costs. The final module integrates decoupling capacitors directly onto the PCB, reducing parasitic inductance to 2.8 nH and maintaining efficient thermal management. However, the

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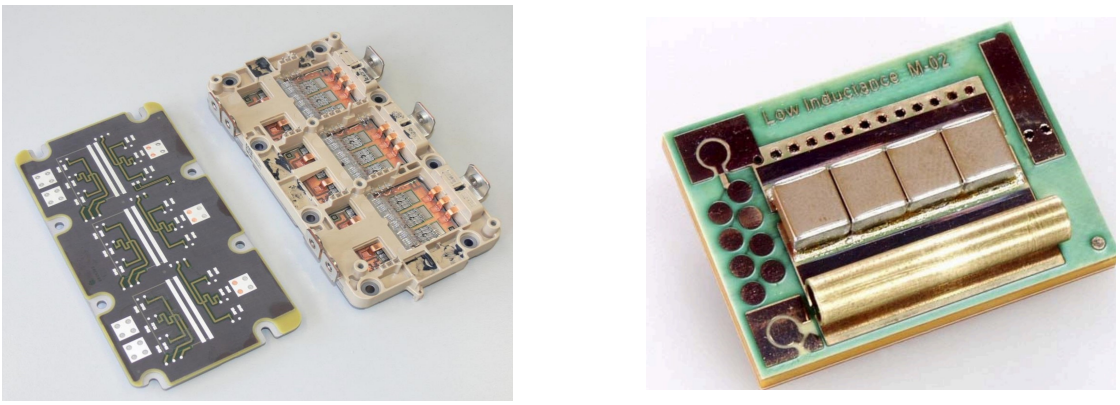

(a) (b)

Figure 1.25: Power chip embedded technologies projects. (a) 50kW IGBT Three-Phase Inverter Module from the HI-LEVEL project [51]. (b) Global view of the Very Fast Switching module [52].

design also highlights the mechanical stresses associated with thicker copper layers, which require careful attention to prevent damage to the power chips.

The Very Fast Switching (VFS) project introduces a packaging solution that directly integrates a PCB layer onto a DBC substrate (Fig. 1.25b). This approach eliminates the need for bonding wires or bumps by connecting the power device through vias in the PCB, while taking advantage of the thermal performance of DBC substrates. The use of vias significantly reduces parasitic inductance, achieving values as low as 0.5 nH. The design also benefits from the flexibility of PCB routing, allowing for closer integration of decoupling capacitors and minimizing parasitic effects.

Double-sided cooling (DSC) modules are another example of 3D packaging approaches. These DSC modules use both the front and back surfaces of the semiconductor chips for heat dissipation (Fig. 1.26), offering a significant improvement over traditional single-sided cooling designs. Introduced in 2001, DSC modules integrate power components such as IGBTs and diodes between two direct bond copper (DBC) substrates. This dual-surface approach results in up to a 76% increase in heat dissipation [53] or 40% reduction in thermal resistance [54, 55], significantly reducing thermal stress and enhancing the overall longevity of the module.

Double-sided cooling can also be implemented using PCB embedding. In these configurations, power components are integrated directly into the PCB, allowing for heat dissipation from both the front and rear surfaces. The integration of microchannel cooling systems within the PCB structure further enhances heat management, offering a compact yet highly efficient solution for embedded power semiconductors[56].

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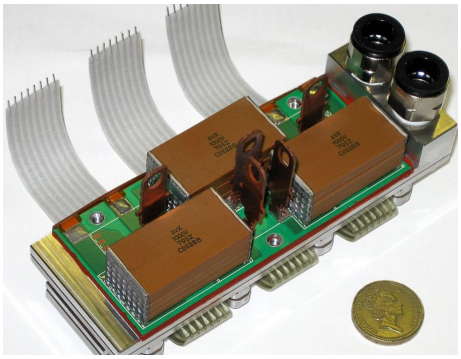
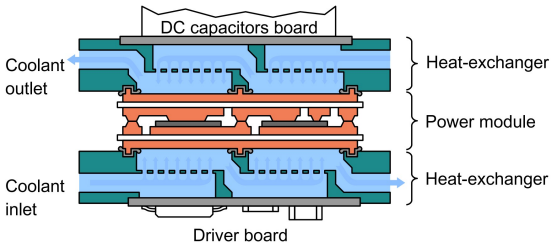


(a)



(b)

Figure 1.26: Double-Sided Cooling Modules (DBC) for Direct Water Cooling Systems [55]. (a) Overview of the Power Module. (b) Cross-Sectional View of the Direct Water Cooling System Setup.

4 Conclusion

This chapter has explored the key considerations in power converter design, focusing on the advantages and challenges presented by wide bandgap (WBG) semiconductors such as SiC and GaN. These devices offer significant benefits, including higher switching frequencies, reduced losses, and improved thermal management. However, they also introduce complexities related to switching behavior, stray inductances, and electromagnetic interference (EMI). The importance of addressing these challenges through optimized layouts and effective packaging strategies has been emphasized, as these are essential for minimizing losses, managing EMI, and ensuring efficient thermal dissipation.

Tab. 1.3 summarizes some of the packaging technologies which can be used to implement a power converter, and which are described in this chapter. A special focus is given to PCB-based technologies, as they offer good thermal and electrical performances, allow for compact designs, and rely on a mature manufacturing ecosystem. PCB embedding technology, in which the main power semiconductor devices are inserted within the PCB stack, is at the center of this thesis work.

However, to fully exploit the capabilities of WBG semiconductors and PCB embedding technology, special care must be given to the design stage. Indeed, it is difficult to rely on hardware prototyping with advanced technologies such as PCB embedding, as those can be costly to make. Powerful computer-aided design tools are therefore necessary to facilitate the design process and address these various challenges.

The following chapters will examine the design software and workflows essential for power electronics design. Emphasis will be placed on embedded PCB technology, which shows flexibility and potential in addressing the evolving demands of power

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Method	Specifications	Advantages	Disadvantages
Classical Packaging	- Chip is attached via soldering to substrates (e.g., DBC or copper sheet) - Electrical connections via bonding wires.	- Widely used in low and medium power applications. - Reliable technology - Cost-effective in discrete components and for smaller circuits.	- High parasitic inductance due to bonding wires. - Limited scalability for high-speed switching thermal stress due to poor thermal expansion balance. - Limited thermal management.
3D Packaging	- Uses vertical stacking for improved routing. - Connects chips via alternative methods (e.g., Vias, bumps, or direct soldering) instead of bonding wires	- Better heat dissipation with a new face for cooling. - Reduced parasitic elements. - Greater routing flexibility for high-speed switching applications.	- Complex manufacturing processes. - Potential challenges with alignment and isolation. - Increased fabrication cost.
Double-sided Cooling Module	- Cooling on both front and back faces. - Integrated water cooling or micro-channels for heat dissipation	- 76% increase in power dissipation efficiency. - Reduced thermal stress, extending module life. - Better thermal balance between faces.	- Manufacturing complexity (e.g., soldering, alignment). - Increased difficulty in ensuring electrical isolation. -High system cost due to its requirements for advanced cooling solutions.
Module with Integrated PCB (Very Fast Switching Project)	- Chip is attached via sintering to a DBC substrate - A PCB layer is created on the DBC surface to connect the chip with vias. - The top layer can integrate passive components.	- Eliminates bonding wires. - Low inductance (0.5 nH for package) -Enables high-speed switching(close integration of decoupling capacitors).	- Initial manufacturing cost can be higher. - Requires precise PCB design and via creation to ensure good performance
PCB-based Module (HI-LEVEL Project)	- Uses PCB as the substrate - Sintered chip onto copper for heat diffusion. - Components are encapsulated by dielectric material (FR4) with Vias for electrical connection	- Mass production potential reduces cost. - Flexibility in routing for high-speed applications. - Compact module design for automotive use.	- Higher mechanical stress in chips compared to traditional DBC modules. - Thermal management challenges due to copper layer.

Table 1.3: Summary of Packaging Methods for Power Electronic

converter design.

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Chapter 2

Design in Power electronics

Designing power electronic systems is a complex and multifaceted process. It encompasses essential elements such as system modeling, simulation, component selection, circuit design, control strategy development, and the careful consideration of thermal and electromagnetic performance. Optimizing the performance of power electronics requires the application of robust design methodologies and specialized software tools.

In this chapter, the latest techniques and tools currently shaping the field of power electronics design and modeling are explored. Recent advancements in simulation methods, the integration of digital twin models, and other innovative tools used in both research and industry practices are presented.

1 Converter design

The design process of a power electronics (PE) converter begins with a set of specifications. These specifications cover crucial aspects such as voltage and current ratings, dynamic behavior, temperature ranges, efficiency, power quality, power density, and cost. Additionally, compliance with regulatory standards, such as electromagnetic interference, safety, and mechanical robustness, is often required.

Throughout the design, the specifications guide critical decisions, including the selection of circuit topology, component values, modulation schemes, control strategies, and switching frequencies. The choice of components, their switching technology, and the design of magnetic elements are all influenced by these requirements. Moreover, the physical layout of the converter, including component placement, connections, cooling mechanisms, and protective elements, must be tailored to suit the application and environmental conditions.

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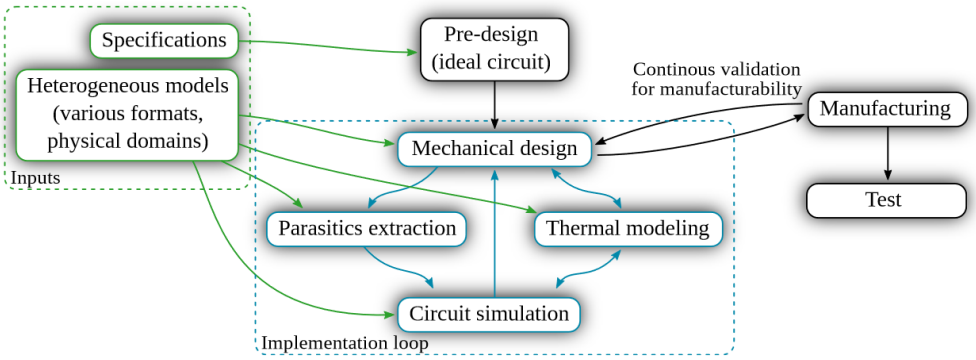

Figure 2.1: Overview of the design workflow of a power electronic converter [57].

Designing power converters is inherently complex due to the multitude of interdependent variables involved. As a result, the development process is typically iterative, with each cycle aiming to refine the design for improved performance, reliability, and manufacturability. A standard power converter design workflow, illustrated in Fig. 2.1 and described in [57], includes mechanical layout (e.g., PCB design), electrical and thermal simulations, and physical prototyping for experimental validation. While both simulation and prototyping are resource-intensive, requiring specialized tools, domain expertise, and considerable time, they are essential to achieving a functional and optimized design. Prototyping alone is not only expensive but also limited in its ability to explore the full design space. Simulation, though also costly, enables early detection of design flaws and allows engineers to evaluate multiple scenarios before committing to hardware. Ultimately, the combined use of simulation and prototyping reduces overall development risk and cost by identifying issues earlier in the design cycle.

The following sections will detail the systematic process involved in the operation of a conventional power converter, providing a clear overview of each step.

1.1 System specifications

Specifications include functional requirements such as input/output voltages, nominal power, efficiency targets (typically above 90%), and power factor (ideally above 0.9). Additionally, it's essential to define environmental factors that could impact the converter's effectiveness, such as temperature, humidity, vibration resistance, and compliance with electromagnetic interference (EMI) standards. Material and technology selection is also affected by regulations: recyclability, reduction of hazardous substances, fire-resistance. . . .

The manufacturing technology can also bring its own set of specifications, as each technology has specific limitations in terms of manufacturing capability.

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In essence, these specifications not only guide the design of power converters but also ensure that they fulfill performance, reliability, and environmental standards while remaining within budget.

1.2 Pre-design

During this stage, the appropriate converter topology is chosen based on the required type of conversion, such as rectifiers, inverters, DC-DC converters, AC-AC converters, high-efficiency resonant converters, or high-frequency converters for compact, efficient designs. Additionally, multi-level voltage converters may be selected to reduce distortion, with each topology serving different applications based on power and efficiency needs.

Alongside topology selection, the choice of control strategies plays a critical role. Depending on the system's performance requirements, different control approaches can be proposed, such as voltage mode control, current mode control, adaptive control, or digital control techniques. The selected control approach is designed to ensure stable operation, efficiency, and responsiveness to load variations, helping to achieve precise regulation and optimized performance.

Once the topology and control method are chosen, key components such as inductors, capacitors, and switching devices are selected and sized according to the system's requirements. The design is further refined using mathematical analysis to calculate key parameters and account for possible constraints on the load, frequency, efficiency, and the operating point limits (such as maximum voltage, current, or power). These calculations help ensure the system operates within safe and efficient limits.

To validate the design effectively, advanced circuit simulators such as PSIM, or Simulink-Matlab can be utilized. Circuit simulators like PSIM are particularly useful for high-level simulations of power electronics converters as they use simplified models and can quickly simulate losses and thermal effects. The models parameters can be extracted from data sheets (see Fig. 2.2). However, such a circuit simulator does not allow for fine calculation of the switching waveforms nor for taking into account the effect of circuit parasitics.

Simulations using these tools allow for testing the system's behavior under various conditions, considering operating point limits and other system constraints. By the end of the pre-design phase, the topology, control approach, components, and operating limits are well-defined, forming a solid foundation for the next steps in the design process.

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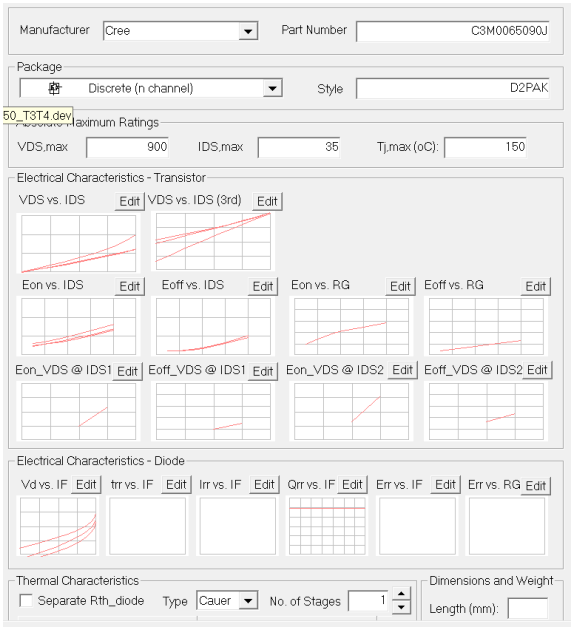
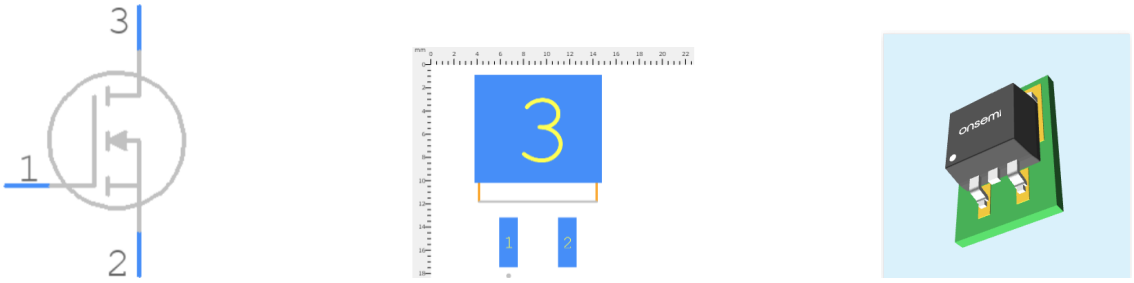


Figure 2.2: Circuit simulation software: Model database established on data-sheet (PSIM).



(a) (b) (c)

Figure 2.3: Power MOSFET eCAD library from Onsemi (a) schematic Symbol, (b) Footprint for the PCB layout, and (c) the 3-Model of the component's package

1.3 Implementation

The implementation of the pre-design circuit into a PCB (as we are focusing on PCB technology in this work) is carried out using electronic computer-aided design (eCAD) software. Designing a PCB with eCAD is typically done in two stages: schematic capture and PCB layout. Schematic capture involves creating the logical connections of the circuit, while PCB layout is concerned with the physical arrangement of components and the routing of conductive tracks.

1.3.1 Components library

Before beginning the design, a library of CAD parts must be prepared. This library, as shown in Fig. 2.3, includes schematic symbols (Fig. 2.3a), footprints (Fig. 2.3b) for the PCB layout, and step models (Fig. 2.3c)for 3D printed circuit board display. These parts are essential for designing the circuit and ensuring that all components are accurately represented in both the schematic and physical layout

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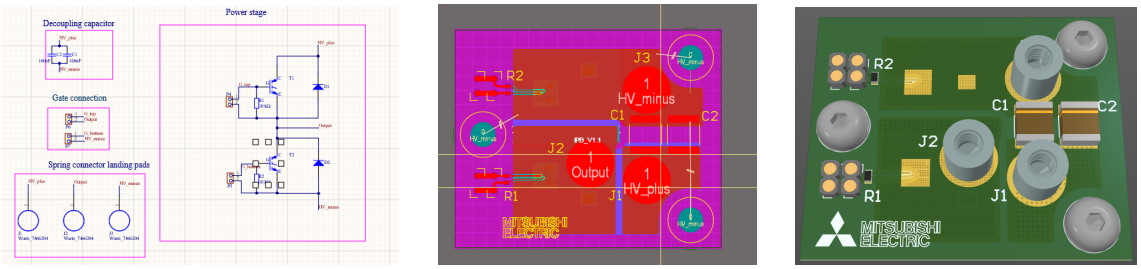

(a) (b) (c)

Figure 2.4: Half-bridge circuit design levels (a) schematic circuit,(b) PCB layout and (c) 3D View of the PCB.

stages.

1.3.2 Schematic circuit

A schematic representation of the circuit can be created using standard electronic components, such as resistors, capacitors, inductors, connectors, and integrated circuits. ECAD tools allow designers to place these components on a schematic sheet and connect them to form the circuit. This schematic serves as the blueprint for the PCB design, allowing to automatically validate later that the copper pattern provides all the interconnects needed, and that no unwanted short circuits have been formed.

1.3.3 Layout design

Once the schematic is complete, the PCB routing can begin. This stage involves defining the copper and dielectric layer details, such as their number and dimensions, and determining the board's shape, as illustrated in Fig .2.4b.

The designer then places the components on the board, before drawing the electrical connections between them (conductive tracks and copper planes). The eCAD software plays a crucial role in guiding the user to follow best practices and ensure predefined design rules are observed. Such rules are used to verify that traces belonging to different nets do not touch and dictate various parameters such as trace width, clearance, or minimum via diameter.

Designing a reliable and standards-compliant printed circuit board (PCB) requires significant engineering expertise. It is when the PCB layout is routed that parasitic elements are defined. Therefore, it is at this stage that electromagnetic interferences or stray inductances can be reduced. The placement of components on the PCB is also key for the thermal manangement, by ensuring that power-dissipating components are positioned where airflow is optimal or near cooling fea-

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tures

Note that elements such as the housing and cooling system of the PCB are typically addressed separately from the ECAD layout during the design process. These are not detailed in this work.

1.3.4 3-D representation

In addition to the 2D layout, ECAD software can also generate a 3D view of the routed PCB, as shown in Fig. 2.4c. This 3D visualization is particularly useful for assessing the geometry of the populated board before fabrication. However, it is important to note that this 3D representation only describes the geometrical envelope of a board and not its internal structure nor any other physical aspect. It lacks details such as the materials used, the physical parameters of the various layers, and other factors crucial for understanding the behavior of the components. As will be shown later, several simulation steps require to build a custom 3D model, without using that provided by the eCAD software.

At this point in the design, two approaches can be followed. If the design is complete and meets all required standards, the next step is to create manufacturing documents for the fabrication of the board. These documents are then sent to the manufacturer for board fabrication and assembly. A second approach is to use the design to generate electrical and thermal models, to simulate the behavior of the board, allowing to perform some validation before a hardware prototype is made. This is the approach followed in this thesis work.

1.4 Modelling

Modeling allows assessing a system's behavior before building a physical prototype. During the pre-design stages, analytical models can be employed to provide quick estimates of performance, like efficiency and voltage regulation, helping designers make initial decisions. However, these models often miss complex, nonlinear behaviors and dynamic interactions seen in real-world applications.

As the design process progresses, more complex mathematical models are created to enhance modeling accuracy. These models consider nonlinearities and dynamic behaviors, necessitating advanced numerical methods such as the Finite Element Method (FEM) and the Finite Difference Time Domain (FDTD) method for solving them. Models can cover a wide range of physical domains: electrical, thermal, and mechanical. Some models can also integrate coupling effects: electro-thermal

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coupling (losses in the electrical circuit are used to compute the temperature of the components) or thermo-mechanical coupling (to calculate stress and strain in the structure caused by changes in temperature). In this work, we focus on electrical, thermal and electro-thermal modeling and simulation.

1.5 Prototyping & Testing

A hardware prototype is needed for a design to be fully validated, but it can be costly and time-consuming. Prototypes allow for real-world testing of factors such as thermal management, electromagnetic interference (EMI), and mechanical stress. The key parameters investigated include temperature distribution, voltage and current waveforms, and efficiency under different conditions.

Fabricating prototypes can be expensive, especially when custom components or advanced manufacturing techniques are necessary. In particular, components embedded in PCBs incur higher fabrication costs and complexity due to the need for specialized manufacturing processes and precise material selection. These costs, which cover materials, labor, and advanced assembly tools are typically in the tens of thousands of euros.

Furthermore, measuring specific parameters in compact systems or integrated packages is particularly challenging, especially for data such as internal temperatures or current waveform measurements. When a measurement point is not accessible (whether because the sensing probe is too large, or too intrusive), indirect measurement techniques must sometimes be used instead. It is also often the case that a signal cannot be measured at all, such as the drain current of a MOSFET, as inserting a high-bandwidth current probe would take up a lot of space, and disrupt the converter layout.

In summary, the prototyping phase is essential. It ensures that a converter meets performance, safety, and regulatory standards, establishing a solid foundation for subsequent development and mass production. However, prototyping demands considerable expertise and effort; the iterative process of prototyping, in which designs are continually refined based on test results, can significantly lengthen a project development time and cost, especially when advanced manufacturing techniques are involved. Therefore, there is a strong incentive to rely as much as possible on modeling and simulation, and only produce a prototype for the final validation step.

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1.6 Conclusion

A converter's design process is inherently long, complex, and resource-intensive. It typically requires iterating over design corrections, prototyping and testing, leading to extended development timelines and increased costs. As power converter designs grow more sophisticated, there is a need for innovative workflows that streamline the design process and reduce the necessity for expensive iterations.

A study examined the effectiveness of current design tools and workflows [58]. The conclusion was that while simulation tools are beneficial for optimization and incremental improvements of parts of the power electronic circuits, they fail to model the full extent of the converter. In the case of new systems, such as power converters, the lack of a complete virtual prototype underscores the necessity of physical testing.

In response to these challenges, many recent research efforts are focused on developing more flexible and direct design approaches based on computer simulation. These innovations strive to improve the efficiency of the design workflow, reduce time-to-market, and minimize the financial burden associated with the development of power converters.

2 Modeling

Models help understanding the physical behavior or a system. They must be understandable so that we can study them, and they must be a good approximation of the real system, accounting for its most important features to accurately predict various phenomena. A good model strikes a balance between realism and simplicity, ensuring both accuracy and computational efficiency [59]. By simulating systems before physical implementation, modeling reduces risks, development time, and costs.

Power electronics systems often involve complex interactions between electrical, thermal, and mechanical domains. Understanding these interdependencies is key.

In the following, two main types of models are described: analytical models, which simplify system behavior based on fundamental principles, and numerical methods such as Finite Element Models (FEM) and circuit simulations, which provide more detailed predictions for complex systems but cannot be processed without a computer.

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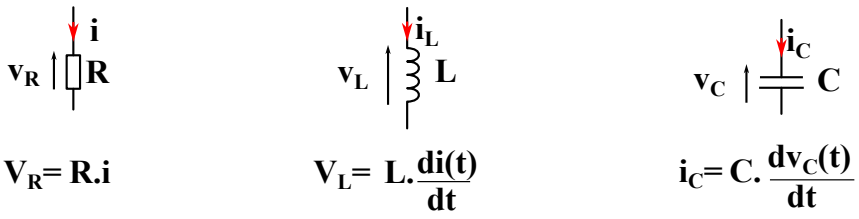

Figure 2.5: Basic ideal electrical models

2.1 Analytical Modelling

These models leverage well-established electrical principles, such as circuit theory, semiconductor physics, and thermal dynamics, to predict key performance parameters such as voltage, current, and power flow within power converters. Analytical models are particularly valuable when applied to linear or linearized problems, where complex systems are approximated to facilitate easier analysis, typically within a defined operational range.

To streamline analysis, common assumptions and approximations are employed. In thermal modeling, one-dimensional (1-D) assumptions are often used to depict heat flow, suggesting that temperature gradients predominantly occur in a single direction. This simplification facilitates the estimation of temperature distribution and heat dissipation in power components, avoiding the complexities of three-dimensional models. However, these simplifications result in a loss of accuracy. Therefore, while analytical models offer valuable insights within their validation range, they often necessitate refinement through detailed numerical simulations or experimental validation to ensure accuracy in complex or nonlinear scenarios.

2.1.1 Electrical analytical models

Fundamental Principles of Electrical Circuits

Electrical circuit analysis relies on idealized models of components such as resistors, capacitors, and inductors, as illustrated in Fig. 2.5. These models simplify the understanding of how these components behave while assuming ideal conditions that overlook real-world imperfections like temperature variations, parasitic effects, and component tolerances. At the core of circuit analysis is Ohm's law, which serves as the foundation for analyzing resistive circuits and establishing the relationship between voltage and current.

Another cornerstone of electrical circuit theory is Kirchhoff's Laws, as illustrated in Fig. 2.6, which are indispensable tools for analyzing circuits, These laws are based on the fundamental principles of charge and energy conservation. making them crucial for understanding current flow and voltage distribution in complex circuits,

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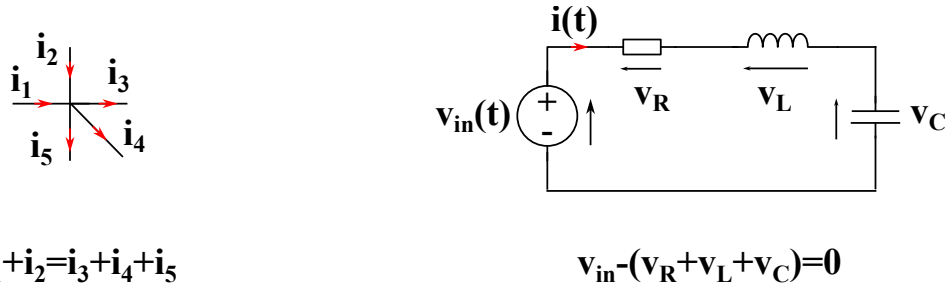

Figure 2.6: Kirchhoff's laws application example description

especially those with multiple branches and nodes. Mathematically, this can be expressed as:

$$\text{Kirchhoff's current Law} : \sum_{k=1}^{n} I_k = 0 \tag{2.1}$$

$$\text{Kirchhoff's voltage Law} : \sum_{k=1}^{n} V_k = 0 \tag{2.2}$$

Kirchhoff's Current Law (KCL) states that the sum of currents entering a node must equal the sum of currents leaving it, equation 2.1, ensuring the conservation of charge. Kirchhoff's Voltage Law (KVL) asserts that the sum of all voltages around any closed loop in a circuit must be zero, equation 2.2 reflecting the conservation of energy.

This approach enables us to describe the behavior of both simple and more complex systems, allowing us to develop differential equations that capture the dynamic responses of circuits, such as oscillations and damping. For example, the differential equation for an RLC circuit(Fig. 2.6) is given by:

$$V_{in}(t) = L\frac{d^2i(t)}{dt^2} + R\frac{di(t)}{dt} + \frac{1}{C}i(t) \tag{2.3}$$

Average circuit model

In the field of power electronics, understanding the dynamic behavior of systems is crucial for the effective design and analysis of circuits. Various modeling approaches are commonly used to study these dynamics, particularly through averaging and linearization methods.

Average switching models are especially valuable for systems that include switching components like transistors and diodes. Such models average the effects of the switches over one complete cycle of operation (Fig. 2.7a. Average switching models simplify the analysis of power converters by removing the need for a detailed time-domain analysis of every switching event.

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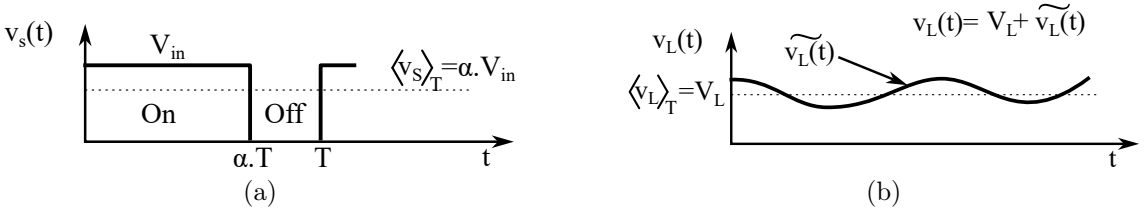

Figure 2.7: (a) Averaging model on switching voltage; (a) small signal model.

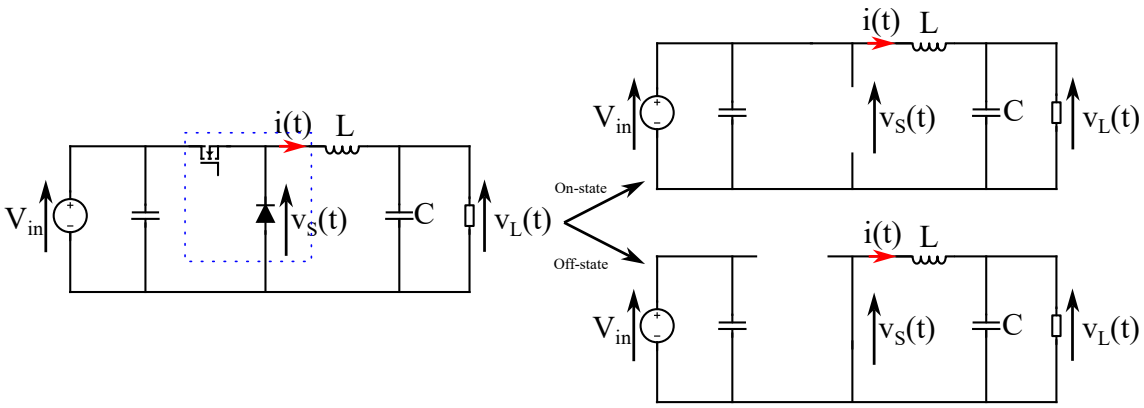

Figure 2.8: buck averaged electrical models

Small signal model

Another important modeling approach is the small-signal model (Fig. 2.7b), which focuses on analyzing a system's response to small perturbations around its steady-state operating point. In this model, nonlinear system equations are linearized around the operating point, making it easier to analyze the system's dynamics. This linearization enables the study of the system's behavior in the frequency domain, which helps in analyzing stability, frequency response, and control design. Small-signal models are particularly useful for designing control systems that can effectively respond to minor variations in system conditions.

Power electronic converters are inherently time-varying systems that exhibit multiple circuit states during a single switching period, as illustrated in Fig. 2.8. so, these systems can be effectively be described as a succession of different circuit states using Singular Value Decomposition (SVD). An average equation can be derived by applying a weighted time average to each state, providing an effective method for approximating the system's overall behavior [60].

$$\text{on-state } (1): \begin{cases} v_{in} &= L.\frac{di_L}{dt} + v_C \\ i_L &= C.\frac{dv_C}{dt} + \frac{v_C}{R} \\ v_L &= v_C \end{cases} \qquad \text{off-state } (2): \begin{cases} 0 &= L.\frac{di_L}{dt} + v_C \\ i_L &= C.\frac{dv_C}{dt} + \frac{v_C}{R} \\ v_L &= v_C \end{cases}$$

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$$(1) \times \alpha + (2) \times (1-\alpha) \quad \Rightarrow \quad \begin{cases} \frac{di_L}{dt} & = -\frac{1}{L}.v_C + \frac{\alpha}{L}.v_{in} \\ \frac{dv_C}{dt} & = \frac{1}{C}.i_L - \frac{v_C}{R.C} \\ v_L & = v_C \end{cases} \tag{2.4}$$

The average model captures the system's dynamics through a set of differential equations, as outlined in eq. (2.4) for the buck circuit shown in Fig. 2.8. It can be extended to model more complex systems, such as multicell converters [61], as well as other advanced configurations. It provides a comprehensive framework for examining a system's time-domain and frequency-domain behaviors.

2.1.2 Thermal analytical models

One of the commonly used methods for analyzing thermal behavior in power electronic systems is based on a one-dimensional (1-D) heat transfer assumption within an equivalent thermal network model. This approach is particularly effective for simple structures where heat conduction occurs primarily in a single direction—typically through the thickness of the substrate or material layers. However, in more complex layouts featuring vias, multilayer interconnects, or intricate routing, heat tends to spread laterally as well as vertically. Vias, for example, introduce vertical thermal paths that can bypass adjacent materials, while dense routing can create localized hotspots and non-uniform thermal distributions. These multidimensional effects violate the assumptions underlying 1-D models, potentially leading to significant errors in temperature prediction and thermal resistance estimation.

One-dimensional analytical thermal models are most applicable when the system consists of homogeneous material layers with consistent thermal properties, such as thermal conductivity and specific heat capacity. In such cases, heat flow is assumed to occur predominantly in one direction, which simplifies the prediction of temperature distributions and thermal responses by neglecting lateral heat diffusion. This allows the model to be represented as a series of thermal resistances connected linearly, enabling efficient thermal analysis with reduced computational complexity.

The one-dimensional (1-D) thermal analytical circuit model is essential for early circuit board (CB) thermal design, as illustrated in Fig. 2.9. This model simplifies heat transfer into a network of thermal resistances and capacitances, facilitating quick thermal analysis and predictions. It operates on the principle that heat flows due to temperature differences and is influenced by material properties and geometry. Heat conduction is represented by a linear arrangement of thermal resistances reflecting the physical layers in the CB assembly.

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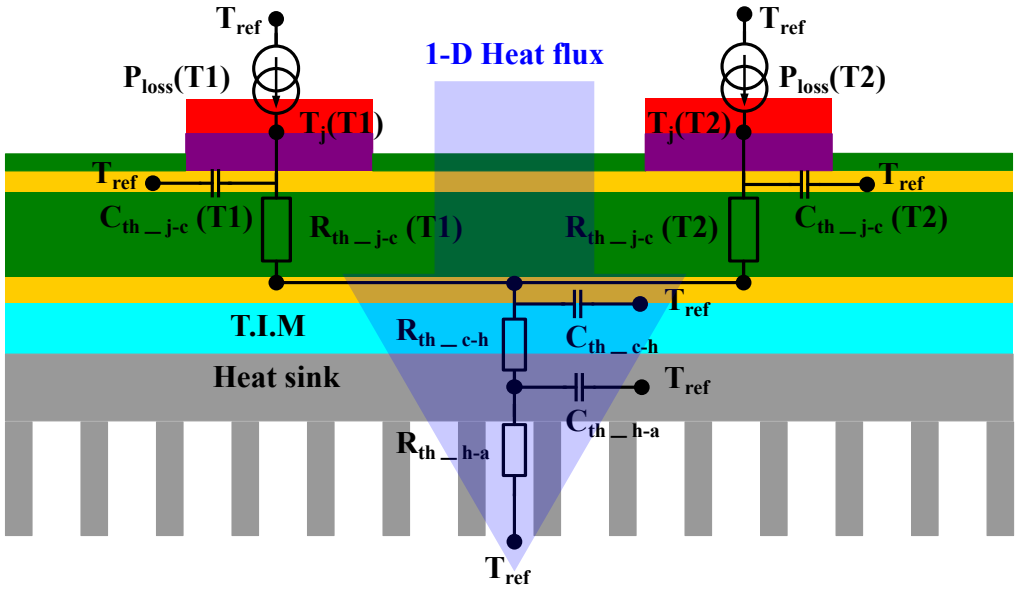

Figure 2.9: 1D equivalent thermal circuit model (TECM)

While effective and commonly used, the 1-D model may not accurately depict scenarios where heat disperses laterally, especially in compact assemblies with high heat-generating components. To improve accuracy, spreading thermal resistance is introduced, addressing the challenges heat faces as it radiates from a concentrated source into a broader area [62, 63, 64]. This accounts for the additional resistance encountered as heat spreads from a small source to a larger substrate—common in multilayer PCBs and heatsink interfaces. Combining 1-D conduction with spreading resistance provides a more realistic temperature profile, helping engineers identify thermal bottlenecks and design better cooling strategies without significantly increasing model complexity.

However, the 1-D model has inherent limitations, such as assuming unidirectional heat flow, which may not accurately reflect real-world thermal behavior in complex or densely packed designs. It also oversimplifies thermal dynamics by typically ignoring transient effects and averaging temperatures, potentially overlooking critical hotspots that can lead to component failure.

The 1-D assumption is valid in many cases, especially when the layers are relatively thin and the heat flow is predominantly unidirectional. However, if the layers have significant dimensions in other directions or if there are complex geometries, a more advanced model might be required that accounts for multi-dimensional heat transfer. In such cases, a more sophisticated model can be derived from the analytic model, such as the construction of a thermal RC network by meshing the structure as in the model HotSpot [65, 66], providing a more precise representation of heat distribution.

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2.1.3 Conclusion

In power electronics, both electrical and thermal analytical models are valuable for estimating system behavior, but they often rely on simplifications and assumptions. These models tend to overlook critical factors such as parasitic elements, high-frequency effects, and thermal interactions, which limits their ability to fully capture the complexity of real-world systems. While it is theoretically possible to describe these systems analytically, the complexity of solving such models can be extremely high, particularly due to non-linearities and the coupling of electrical and thermal effects. Therefore, numerical simulations are essential for accurately modeling and optimizing complex systems, as they can capture the detailed interactions that analytical models may miss.

2.2 Numerical Modelling

Numerical methods are employed to solve the differential equations that govern physical phenomena. By discretizing continuous domains, such as space and time, into smaller and more manageable elements, these methods allow for the approximation of solutions for each segment of the system.

A significant advantage of numerical modeling is its ability to address complex geometries and boundary conditions that are often beyond the capability of closed-form analytical solutions. This degree of flexibility results in more accurate and comprehensive simulations.

2.2.1 Circuit simulation tools

Circuit simulation allows for effective modeling and validation of how circuits behave under different input conditions. It facilitates a thorough analysis of transient responses, steady-state behavior, and frequency-domain characteristics. Circuit simulation tools are divided into two main categories: circuit-level simulation software, which analyzes detailed signal waveforms, and system-level simulation software, which provides a broader time scale for a higher-level overview.

Circuit-level simulation software, such as SPICE, LTspice, and PSpice, is designed to model interactions among electrical components. By solving the mathematical equations that govern these interactions, these tools predict circuit performance under various conditions. They typically operate on short time scales, ranging from picoseconds to milliseconds, making them particularly effective for analyzing high-frequency behavior, fast-switching transitions, and small-scale dynamic

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effects within the circuit.

On the other hand, system-level simulation software, such as PSIM, PLECS, MATLAB/Simulink, Modelica, VHDL-AMS [67, 68], and SystemVue, models entire systems rather than just individual components. These tools combine circuit-level models with control, mechanical, and thermal elements, facilitating the simulation of complex systems over longer timescales, from milliseconds to seconds. This higher-level modeling approach allows engineers to capture the complex interplay between various subsystems and assess their combined behavior in a holistic manner.

Modeling of components

Accurate component models are essential, especially in capturing the nonlinearities of semiconductor devices like diodes, transistors, and switches. These nonlinearities, which include changes in conductivity and threshold voltages, are crucial for representing how components behave under varying conditions. There are different types of modeling approaches used to represent devices. These approaches vary based on complexity, accuracy, and the type of analysis being performed. The possible components model techniques in the case of LTspice are:

- Native Models : They are built-in models for various components that facilitate quick simulations using standard parameters, while also allowing for customization as needed. These models are particularly useful for general circuit design and analysis, eliminating the need to create custom models. They represent physically-based analytical models that can incorporate geometry dependencies in the model equations [69].

  An example of such native model is the NMOS transistor (Level 1) with specific parameters such as the threshold voltage (Vto), transconductance coefficient (Beta), and channel dimensions (L and W):

```
M1 Drain Gate Source Bulk NMOS1
.model NMOS1 NMOS (Vto=1.0 Beta=120u L=1u W=1u)
```

Figure 2.10: Ltspice native Model.

- Equation-Based Models: The behavior of the device is described using mathematical expressions. These models can be very detailed, outlining not only the device's static characteristics (such as the current-voltage relationship) but also its dynamic behavior (including switching transitions and thermal behavior). In circuit simulators like LTspice, equation-based models are utilized

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alongside "behavioral" sources, such as voltage-controlled current sources or current-controlled voltage sources, to account for the device's non-idealities.

An example of an Equation-Based Model (MOSFET) is shown below, where the current depends on the gate-source voltage and the threshold voltage for the two different regimes (linear and saturation):

```
* Current in Saturation Region
I_D_SAT = Kp * (Vgs - Vth)^2 * (1 + LAMBDA * Vds)

* Current in Linear Region (Vds < Vgs - Vth)
I_D_LINEAR = Kp * (Vgs - Vth) * Vds - (Vds^2 / 2)

* Current Calculation
IF(Vgs > Vth && Vds < (Vgs - Vth)) I_D = I_D_LINEAR
IF(Vgs > Vth && Vds >= (Vgs - Vth)) I_D = I_D_SAT
```

Figure 2.11: equation Models.

- Subcircuit Models represents complex devices or systems using simpler components like resistors, capacitors, and transistors. This method is useful for capturing intricate behaviors, such as non-idealities and switching effects, that would be difficult to represent by a single component, or built-in model.

  Here is an example of a MOSFET Subcircuit Model, that includes the transistor with its parasitic capacitors and resistances:

```
* Simplified TO-247 SiC NMOS Model based on Wolfspeed C2M0080120D
* Subcircuit with parasitics and core MOSFET behavior
* Terminals: d = Drain, g = Gate, s = Source, Tj = Junction temp, Tc = Case temp

.subckt MySiC_TO247 d g s Tj Tc

* === Source Path ===
RS      s   sa      6.436m      ; Source lead/package resistance (TO-247)
LS      sa  s1      4.3n        ; Source lead/package inductance

* === Gate Path ===
RG_ext  g   ga      34.443m     ; External gate resistor (PCB + pkg trace)
LG      ga  g2      7.5763n     ; Gate lead inductance (TO-247)
RG_int  g2  gk      3.9         ; Internal gate resistance

* === Drain Path ===
RD      d   da      64.94u      ; Drain lead/package resistance
LD      da  d3      3.648n      ; Drain lead/package inductance

* === Capacitances ===
CGS     gk  s1      1122p       ; Gate-to-source capacitance (Cgs)

* === Nonlinear Capacitance Subcircuits ===
xCGD    d3  gk      cgd_behavior    ; Gate-to-drain capacitance (Cgd), nonlinear model
xCDS    d3  s1      cds_behavior    ; Drain-to-source capacitance (Cds), nonlinear model

* === Intrinsic MOSFET ===
M1      d3  gk s1  0  MySiC_Core     ; Core NMOSFET device (use LEVEL=1 or BSIM)

* === Body Diode ===
Dbody   s1  d3 body_diode           ; Intrinsic body diode

.model body_diode d (is=1.85u rs=30m tt=15n bv=1200) ; Diode model with breakdown voltage = 1200V

* === Thermal pins ===
* Connect Tj and Tc externally for electrothermal simulations
* Or use fixed voltage sources for isothermal simulations

.ends MySiC TO247
```

Figure 2.12: Subcircuit Model of a Simplified TO-247 SiC NMOS based on Wolfspeed C2M0080120D.

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- Look-Up Table (LUT) and Piecewise Linear (PWL) Models: Complex functions or behaviors can be approximated using pre-calculated data obtained from experiments or simulations. This method offers accurate values at various operating points, which can be difficult to express with an analytical equation. A non-linear function is divided into segments for the piecewise linear model, with each segment represented by a linear equation. These techniques are beneficial for non-linear characteristics, such as the reverse recovery time of diodes or the gate charge characteristics of MOSFETs.

  In the example below, a LUT (in the file `QGate.txt`) contains the gate charge characteristics of a MOSFET at various gate voltages. There is also a PWL current source between Node1 and Node2, which specifies current values at different voltages (for instance, at 0 V, the current is 0 A, and at 1 V, it increases to 5 A):

```
*  Look-Up Table (LUT) for MOSFET Gate Charge
.model MOSFET_LUT Table (Data='QGate.txt')

*  Piecewise Linear (PWL) Model
I1 Node1 Node2 PWL(0 0 1 5 2 10 3 15)
```

Figure 2.13: LUT Models

- Physics-Based Models aim to describe semiconductor physics in greater detail, focusing on aspects such as the behavior of charge carriers, recombination processes, and the physical structure of the device (e.g., PN junctions and drift-diffusion equations). These models tend to be more complex and are used when high accuracy is required for device simulations. Specialized Technology Computer-Aided Design (TCAD) tools are typically utilized for these device-level simulations, offering focused and precise analysis. Their downsides are their elevated computing costs, and their need for detailed information about the component's internal structure (chip layout, doping concentrations, etc., which are typically not known to the user).

Circuit simulators solve circuits using a combination of numerical methods and circuit analysis techniques. They represent the circuit as a set of differential and algebraic equations based on Kirchhoff's Current Law (KCL) and component models. Using Modified Nodal Analysis (MNA), they employ numerical methods like the Backward Euler method for transient analysis and the Newton-Raphson method for adjusting voltage and current estimates. However, limitations exist, particularly in power electronics. The accuracy of simulations depends heavily on the precision of

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component models and the detailed description of the circuit's environment, including parasitic effects. Simulations may become less accurate in the presence of highly nonlinear components, large switching transients, or inaccurate models of components and environmental conditions. Additionally, numerical methods may struggle with stiff systems or require excessive computational resources for large-scale circuits, leading to longer simulation times or reduced accuracy in certain conditions.

2.2.2 2D/3D Simulation

In thermal modeling, key equations focus on conduction, radiation, and convection of heat, while Maxwell's equations govern electromagnetic behavior. These equations can be addressed using various methods such as the Finite Element Method (FEM), Finite Difference Method (FDM), Finite Volume Method (FVM), and Boundary Element Method (BEM), depending on the complexity and accuracy required. Various software tools implement one or more of these methods. They are often designed to solve a specific set of equations, or to be used in a specific case.

Parasitic analysis is vital in power electronics, and simulation tools are used to identify stray inductance, capacitance, and resistance, to assist in solving performance problems like signal integrity and joule heating [70]. Known tools are InCa 3D (Cedrat) and Fasthenry (FastFieldSolvers) for inductance calculations and FastCap for capacitance extraction using the PEEC method. The Method of Moments (MoM) combined with the Fast Multipole Method (FMM) optimizes electromagnetic field solutions, as seen in the 3D RLCG parasitic extraction tool ANSYS Q3D Extractor [71].

For thermal management, ANSYS Icepak is widely employed to simulate and optimize the thermal performance of electronic systems. It uses computational fluid dynamics (CFD) and thermal modeling to predict temperature distribution and heat transfer, considering conduction, convection and radiative heat transfer.

An essential aspect of 2D/3D simulations is that proper geometry preparation is crucial for achieving accurate results. A CAD model should effectively represent the physical system while balancing detail and computational efficiency. After creating the model, materials must be defined with their key properties and boundary conditions should be established to specify how the system interacts with its environment.

Mesh generation is a key aspect, as it divides the geometry into elements for calculations. This process requires fine mesh density in areas with significant variation. Mesh refinement should target critical regions, and adaptive refinement can be

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applied during the solution process. A high-quality mesh is vital for avoiding errors and ensuring convergence, which ultimately leads to reliable and efficient simulation results.

2.3 Conclusion

In conclusion, the comparison of modeling approaches presented in Table 2.1 highlights that each method exhibits specific strengths and limitations, which depend on the nature and complexity of the system under study rather than allowing for a direct comparison.

2D/3D simulation tools provide high accuracy and are well suited for detailed multiphysics analyses, but their use becomes computationally demanding as the system size or complexity increases. Their precision thus comes at the expense of higher computational cost and longer simulation times.

Aspect	Analytical Modeling	Circuit Simulator Tools	2D/3D Simulation Tools
Accuracy	- Limited accuracy due to assumptions - Misses transients and nonlinearities.	- High accuracy for circuits. - Limited for thermal/mechanical effects.	- High accuracy for multi-domain systems. - Excellent for complex interactions.
Cost-Efficiency & Computational Power	- Cost-effective with minimal computational resources.	- Cost-effective for small circuits. - moderate computational needs.	- Expensive - Requires high computational power and memory.
Time Efficiency	- Fast for simple models - Slower for more complex ones.	- Fast for steady-state/transient analysis and prototyping.	- Time-consuming - Requires significant setup for complex systems.
Modeling Complexity	- Limited in handling nonlinearities or complex behaviors.	- Effective for linear/nonlinear circuits. - Limited for multi-domain.	- Handles nonlinear and multi-domain systems with high complexity.
Optimization & Limitations	- Limited to steady-state optimization. - Lacks multi-domain capabilities.	- Ideal for circuit optimization. - limited in multi-domain integration.	- Good for multi-domain optimization.

Table 2.1: Summary of Modelling Methods

Conversely, analytical modeling offers quick and cost-effective solutions for simpler systems, particularly in steady-state conditions, with minimal computational requirements. However, it remains limited in its ability to represent nonlinearities, transient phenomena, and complex interactions, which restricts its overall applicability.

3 Design tools

This section aims to explore and compare the design tools used in the microelectronics domain with those available for power electronics. By analyzing the

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differences in tool capabilities and design processes, we can identify how power electronics design tools can benefit from the advancements seen in microelectronics.

3.1 Microelectronics design tools

Historically, designing electronic circuits was a labor-intensive process involving manual drafting, calculations, and prototype testing. However, as circuit complexity grew, especially with the advent of integrated circuits (ICs) in the 1960s, the need for automation became increasingly apparent. Early design tools were rudimentary, focusing on tasks like schematic capture and simple circuit simulation.

The 1980s marked a pivotal shift with the rise of Electronic Design Automation (EDA) tools, transforming the microelectronics design workflow [72]. These tools allowed engineers to design, simulate, and verify circuits in a digital environment, significantly speeding up the design process and reducing the risk of costly errors. Key developments during this time included the introduction of simulation tools such as SPICE (Simulation Program with Integrated Circuit Emphasis) for analog circuits and the emergence of layout design tools that allowed engineers to define the physical structure of ICs.

As circuit complexity increased with the introduction of Very-Large-Scale Integration (VLSI) in the 1980s and 1990s, the scale of integration reached new heights, incorporating millions of transistors on a single chip. VLSI relies on defining clear and systematic design rules, which allow functional blocks to be assembled efficiently. This approach enables the automation of block placement and interconnections, making it possible to handle the complexity of large-scale designs. As semiconductor components continue to shrink, new interconnection methods are evolving to maximize efficiency and optimization. The performance of the resulting system is guaranteed through a structured design workflow inherent to VLSI, ensuring reliable, manufacturable designs. The design process is typically divided into two main phases, as illustrated in Fig. 2.14:

- Front-end design focuses on defining the functionality and logic of the circuit, including tasks like schematic design, functional simulation, and timing analysis. It ensures that the design meets performance requirements and behaves correctly.

- Once the front-end design is validated, the focus shifts to Back-End Design, which involves physical layout and optimization. This phase addresses the

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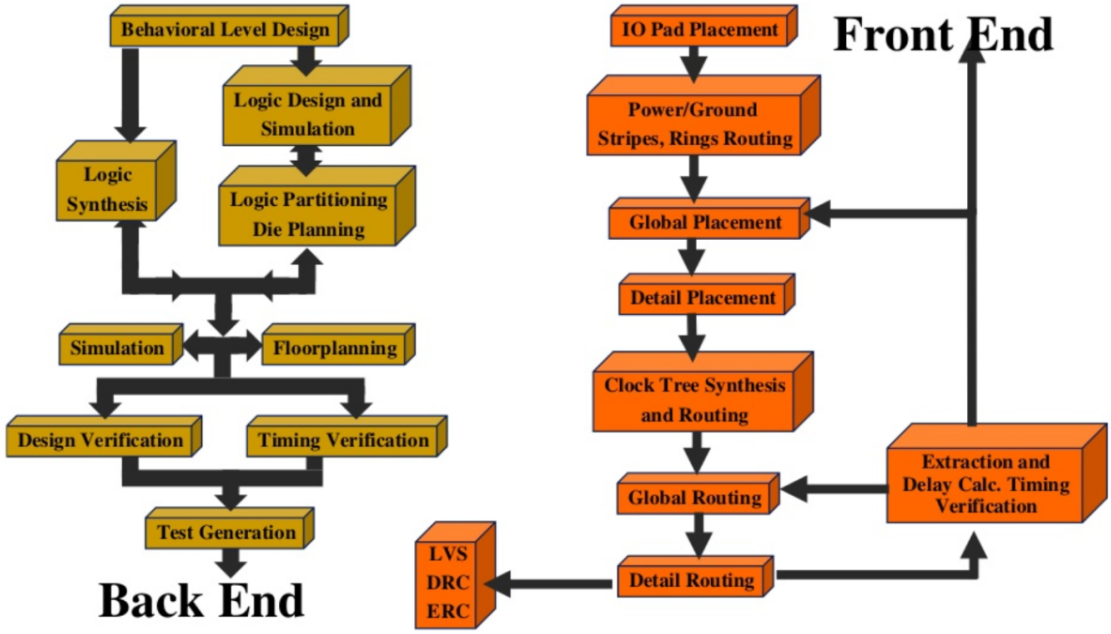

Figure 2.14: VLSI workflow [73]

placement and routing of components, ensuring that the design is manufacturable and performs efficiently in its physical form.

The Process Design Kit (PDK) is a critical enabler in this evolution. The PDK is a comprehensive library of resources supporting various stages of the design process. By incorporating a PDK, the design workflow becomes standardized for mature or emerging technologies. Integrating the PDK with EDA tools ensures a systematic and robust microelectronics design process. When a new technology emerges, it is incorporated into the PDK rather than requiring a fundamental shift in the overall design methodology. This approach streamlines the adoption of new technologies and ensures that designs remain manufacturable across different process nodes, making PDKs a key component in SoC (System-on-Chip) and VLSI development.

3.1.1 Microelectronics Vs. Power electronics designs tools

The progress in microelectronics system design compared to power electronics is largely due to differences in scale, component variety, and fabrication processes. Microelectronics has achieved significant progress due to its reliance on small, highly standardized components such as transistors and capacitors, which are well suited to automation. Dedicated EDA tools have been developed to handle these components efficiently, integrating features such as automated routing, layout optimization, and signal integrity analysis, thereby streamlining and accelerating the overall design workflow.

In contrast, power electronics deals with larger, more diverse components like

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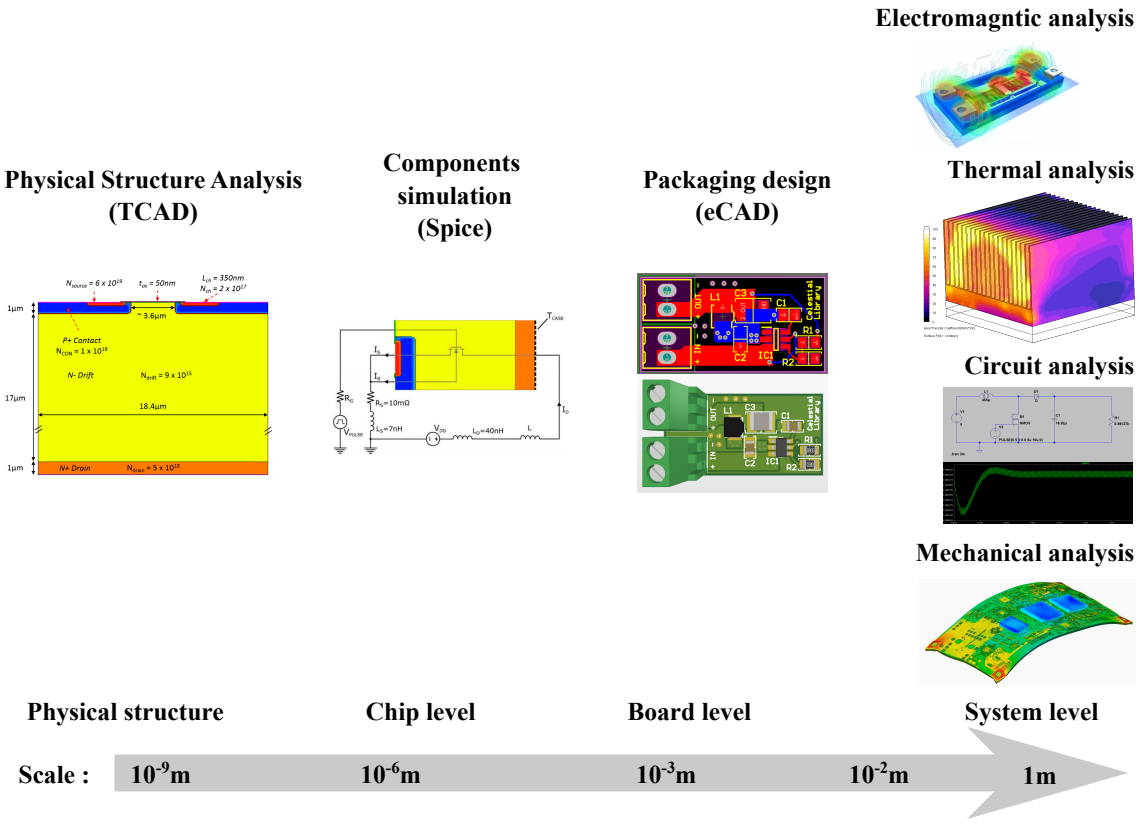

Figure 2.15: Diversity of Power Electronics Design Tools Based on Scale Level

transformers and high-power transistors, each requiring different design methods and fabrication techniques. The variety of components and manufacturing processes adds complexity, requiring multiple specialized tools that don't always work well together. While microelectronics benefits from integrated simulation platforms that handle electrical, thermal, and mechanical properties within one tool, power electronics still largely relies on multiple, fragmented tools, depending on the scale of the investigation, as illustrated in Fig. 2.15. This lack of integration slows down the design process and limits automation.

Overall, the high degree of integration and automation in microelectronics tools has made its design process more advanced and efficient. Power electronics, has yet to reach the same level of tool integration and workflow automation. The next section describes some approaches described in the literature to provide for a better power electronics design-workflow

3.2 Advanced converter design tools

Recent advancements in scientific research aim to refine the tools, methods, and workflows used in power electronics design, enhancing their ability to create more efficient and optimized power conversion systems.

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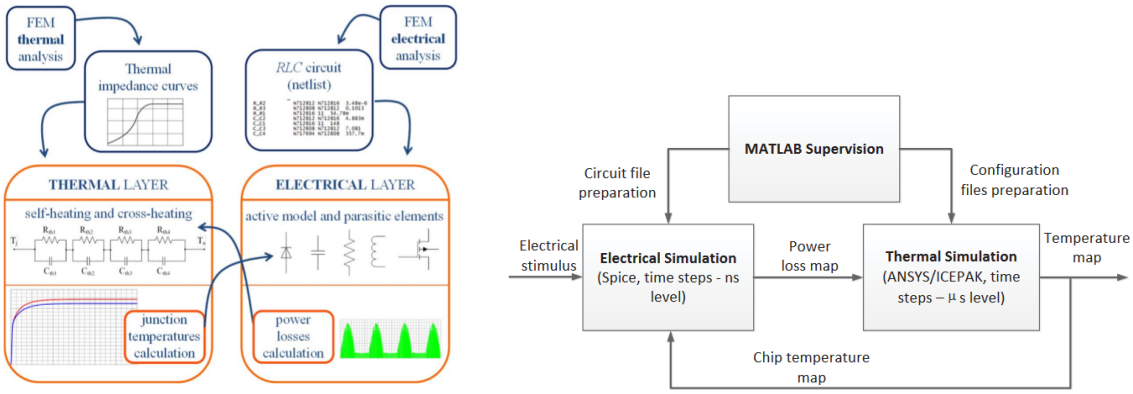

(a) (b)

Figure 2.16: Electro-thermal modelling approaches : (a) Layered approach adopted for the IPEM modeling [74]; (b) Structure of the electrical and thermal simulation setup [75].

3.2.1 Multidisciplinary models

One of the key components of these advancements is the analysis and generation of multidisciplinary models, particularly coupled electro-thermal models, which describe both electrical and thermal effects.

The coupling of electrical and thermal systems presents notable challenges due to their differing time constants. Electrical simulations often require nanosecond time steps, while thermal processes can span seconds or even minutes. To overcome this disparity, two primary methods have been developed: the "direct method" and the "relaxation method"[76].

The direct methods relies on two "layers", as described in [74]. These layers represent electrical behavior and thermal behavior respectively, both formulated as PSpice netlists, as illustrated in Fig. 2.16a, which are solved simultaneously. The electrical layer models parasitic inductances and power losses, while the thermal layer simulates heat propagation and the junction temperatures of active devices. These two layers are interconnected through a self-heating macromodel. The parameters for both the electrical and thermal layers are derived from finite element method (FEM) simulations. The thermal model layer is represented as a Foster-type RC-circuit, while the electrical layer is constructed using results obtained from electromagnetic analysis, incorporating elements such as bond wires and connectors.

An implementation of the relaxation method is depicted in Fig. 2.16b. Such electro-thermal modeling technique utilizes co-simulation for IGBTs, as presented in [75]. This method combines ANSYS/Icepak for thermal analysis, PSpice for electrical simulation, and MATLAB for coordination. In this approach, the IGBT is represented using a compact, physics-based model in PSpice, which divides the device into individual cells. The power loss for each cell is calculated and then

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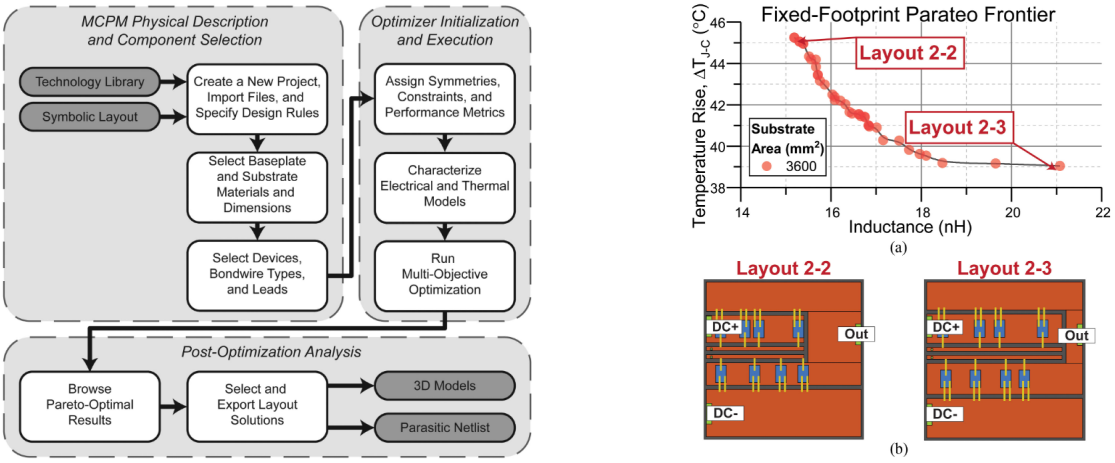

Figure 2.17: (a) workflow of PowerSynth and (b) Results (parasitic inductance and proposed layouts).

passed to Icepak for thermal analysis, after which temperature data is returned to PSpice. A case study demonstrated this modeling technique by testing the IGBT under short-circuit conditions with a 5x5 cell arrangement. Each simulation step takes approximately 90 s, and the entire 16 µs simulation is completed in about 12 mn on a 4-core computer. This approach effectively balances accuracy and speed, allowing for precise predictions of potential issues, such as hot spots, arising from variations in electrical and geometrical parameters, including threshold voltage and solder resistance.

3.2.2 Advanced layout tools

A second category of design tool advancements focuses on simulation-enhanced design platforms and layout optimization tools. This integration aims to improve traditional design methodologies and circuit board design tools, such as Electronic Computer-Aided Design (ECAD), enabling better compatibility with interconnected physical models. By linking PCB design tools to electromagnetic and thermal models, designers can effectively address challenges like thermal management and electromagnetic interference (EMI), ensuring that the final design performs optimally in real-world applications.

The PowerSynth project, illustrated in Fig. 2.17, is a multi-objective optimization tool [77] which simplifies the process of designing and verifying power semiconductor modules by refining both trace layout and die placement. By utilizing reduced-order models (ROMs) to analyze electrical parasitics and thermal interactions, PowerSynth addresses critical factors such as power losses and thermal

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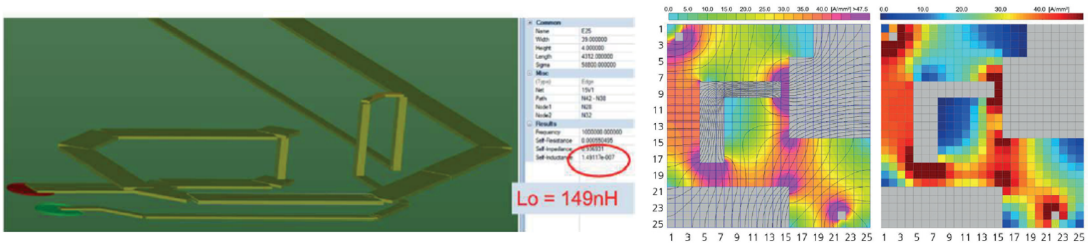
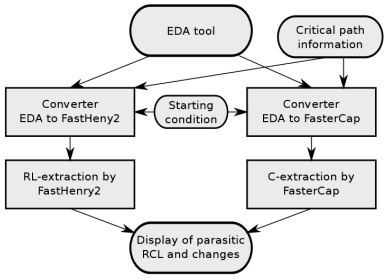
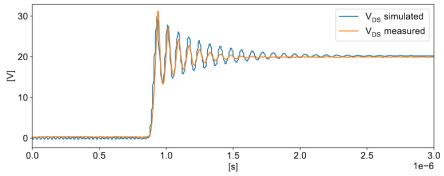


(a) (b)

Figure 2.18: Real-time loop inductance (a), loss and temperature distribution (b) estimation tool [78].



(a) Workflow of the automation process



(b) Simulated and measured turn-off drain source voltage of the MOSFET from the boost converter at 100 kHz switching frequency

Figure 2.19: Automated parasitic components extraction [79].

performance early in the design phase.

An improved approach to the PCB design process involves integrating a tool that estimates inductance and loss within eCAD tools [78]. This method enables users to select current loops within the PCB and to automatically calculate parasitic inductances using a Partial Element Equivalent Circuit (PEEC) solver. This real-time analysis helps identifying potential issues, such as excessive inductance or power losses, during the design phase, as illustrated in Fig. 2.18b.

Additionally, Automated PCB Parasitic Extraction has been implemented to focus on the critical areas of power converters [79], where parasitic effects have the most significant impact on performance. Using an algorithm integrated within an Electronic Design Automation (EDA) tool (Fig. 2.19), parasitics are extracted from the critical path to optimize switching behavior, improving simulation speed and relevance.

3.2.3 Integrated modular design approach

A key goal of these advancements is to simplify the overall design workflow by breaking down power converters into modular building blocks. This modular approach, inspired by microelectronics ("IP Blocks"), allows for greater customization

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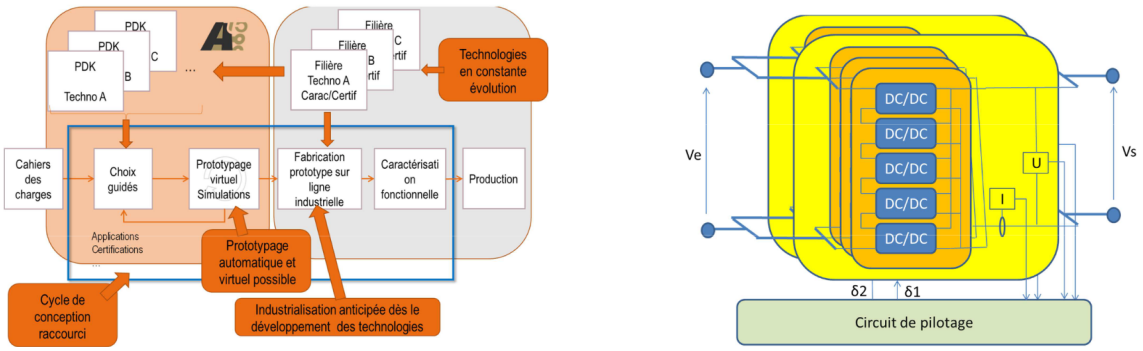

Figure 2.20: Micro-converters approach [80]: (a) design synopsis ;(b) A representation of a complete power converter composed of an assembly of elementary µconverters.

and optimization of individual components. As a result, the design process becomes dependent on predefined modules, which reduces overall flexibility, even though development time is significantly shortened and integration is facilitated.

A significant focus of this research is unifying the design process through modular, block-based approaches. Traditionally, power converter design has been complex and time-consuming, but modular strategies like the Micro-Converter and Power Electronics Building Blocks (PEBB) methodologies have made the process more efficient, scalable, and adaptable.

The Micro-Converter approach illustrated in Fig. 2.20 was developed by G2ELab [80]. It utilizes pre-qualified lower-power converters, referred to as "elementary bricks," which can be combined to create customized converters. This method is supported by a Power Design Kit (PDK) that provides the necessary components for PCB routing and simulations of both electrical and electromagnetic behavior. When integrated with tools like Altium Designer, the PDK simplifies the design process, facilitating everything from circuit topology selection to final implementation.

The PEBB methodology provides a platform-based approach [81] that focuses on reusing established components to develop complex products more efficiently [82]. In contrast to the IPEM (Intelligent Power Electronics Module, see below) approach, which divides functions into smaller parts, a PEBB consolidates these functions into macro-blocks that are tailored for specific applications. A functional decomposition is presented in Fig. 2.21. These standardized blocks are organized by frequency or power range, making them easy to interface with and adapt to a variety of converter designs. The PEBB methodology minimizes design risks and costs, facilitates faster development and customization, and effectively addresses the increasing complexity of power converter design.

The IPEM-Based Power Electronics System Integration approach tackles crit-

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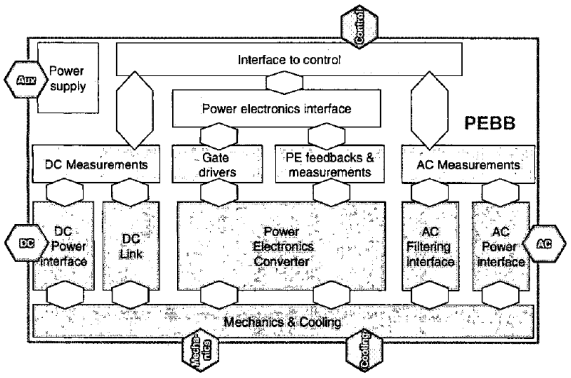

Figure 2.21: PEBB functional decomposition [82].

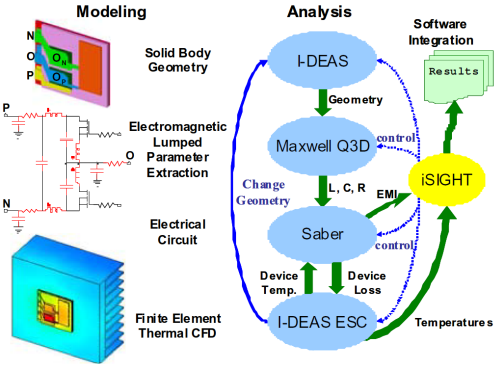

Figure 2.22: IPEM design proposed workflow [83].

ical challenges that hinder the widespread use of power electronics, such as high costs and low reliability [83]. These issues often arise from custom designs, long development cycles, and labor-intensive manufacturing. To address this, the Center for Power Electronics Systems (CPES) has developed integrated power electronics modules (IPEMs), which combine active and passive components with standardized interfaces. This enables automated manufacturing and mass production. IPEMs are versatile, supporting various applications by integrating essential system components like energy storage and thermal management. CPES has also pioneered an integrated design methodology using commercial software (Ansys Q3D, I-DEAS and Saber) for circuit, electromagnetic, thermal, and system optimization. The corresponding workflow is presented in Fig. 2.22.

4 Conclusion

When designing power electronics, it is essential to consider various specifications, constraints, and design choices carefully. Each step, from defining system specifications to pre-design evaluation and circuit simulation, plays a crucial role in ensuring the power converter's functionality, efficiency, and compliance. It is important to note that the current design approach for power converters relies largely on hardware prototyping. This differs from the design workflow used in microelectronics, where virtual testing and validation precede physical prototyping.

Currently, designing a working power converter still relies heavily on assumptions, arbitrary decisions, and experience. Many research articles are dedicated to the optimization of power converter design, which could simplify the process to following specific design procedures starting from system specifications. For relatively large converters, electrical simulation does not currently allow the generation of a

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complete "virtual prototype" that could replace a hardware prototype. There are many reasons for this, but one of them is the heterogeneity of technologies and design tools involved in designing a power converter.

The use of predefined elements and standardized design flow is evident in both modular and general designing methods. The construction of reusable elements is at the heart of the modular approach, which in many aspects tends to align with the well-established design approach of microelectronics. The development of PCB-based converters tends to reduce the diversity of technology and design tools (a complete converter can be described within the PCB eCAD tool), making it possible to automate model generation.

The chosen approach for this project is to create a workflow for virtual prototyping using mature simulation software. This choice aims to give more freedom to the designer, allowing them to create their unique electronic system and explore more possibilities without being chained to specific shapes, sizes, or part positions or being obliged to use predefined or reusable standard modules. Also, a choice was made to focus on automatic model generation, in which no data preparation (simplification, identification of critical area) is expected from the user.

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Chapter 3

Virtual prototype generation

Virtual prototyping, which involves using numerical models and simulations instead of physical prototyping, is an appealing approach for reducing development costs and time while providing access to valuable data like internal temperatures. However, one major challenge that has hindered power electronic designers from utilizing virtual prototypes is the lack of a unified system description. Power electronics systems typically consist of a mix of packaged devices, mechanical parts, and Printed Circuit Boards (PCBs). This complex arrangement is not fully captured in a single place, which makes preparing a model for computation a laborious task and often requires simplifying the model. Packaged devices are like "black boxes" with their internal details hidden from the circuit designer, making it difficult to model them alongside the rest of the converter.

The development of high-power PCB technologies has made it possible to build a full converter using only PCBs for interconnects and bare-die power semiconductor devices. This "rationalized" assembly provides a complete description of the converter in the PCB design software, including layout and bill of materials. In theory, this information can be used to automate the generation of models (thermal, electrical, etc.).

However, in practice, generating models from PCB design software is quite challenging, and the model preparation process requires significant user interaction. For instance, a solution presented by Hoffmann et al. [78] allows users to select conductors in a PCB and automatically compute parasitic inductance, resistance, and joule heating. While this approach is efficient, it requires expertise from the user to identify the circuit parts worth investigating.

The workflow shown in Figure 3.1 presents the application of virtual prototyping. With the ability to validate proper operation on a virtual model that can be quickly

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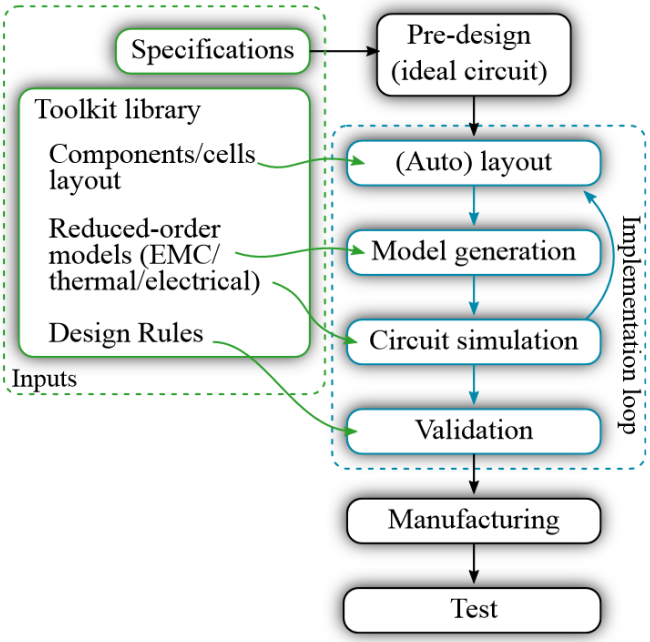

Figure 3.1: Proposed design workflow [57]

and automatically generated, this approach allows the designer to iterate over design variations quickly and to produce a satisfying prototype directly.

As presented in the previous chapter, several approaches have been proposed to improve computer-aided design. One approach focuses on providing real-time estimations of operating parameters [77, 78], such as temperature distribution or stray inductance, for a specific part of the system. Another approach involves a modular design using a limited number of micro-converters and pre-optimized modules [80, 82, 81].

Here, the goal is to generate models for an entire PCB without requiring expertise in model generation or using pre-defined structures. After the PCB design is created, the parasitic elements (capacitance, resistance, inductance, and their couplings) are calculated for each track, and are inserted into a circuit model along with all the components of the PCB. A similar method is used to create a compact thermal model. The resulting set of models can replicate the operating converter in the electrical and thermal domains, forming a "virtual prototype" of the circuit. Parts of the methodology presented in this chapter, particularly the automatic generation of electrical and thermal models from PCB design data, were previously published in the following articles: "Automatic Model Generation for PCB-based Power Electronics" and "Automatic Generation of Thermal Models for PCB-based Power Electronics" [84, 85]. In this chapter, we describe the way these models are generated from the eCAD data.

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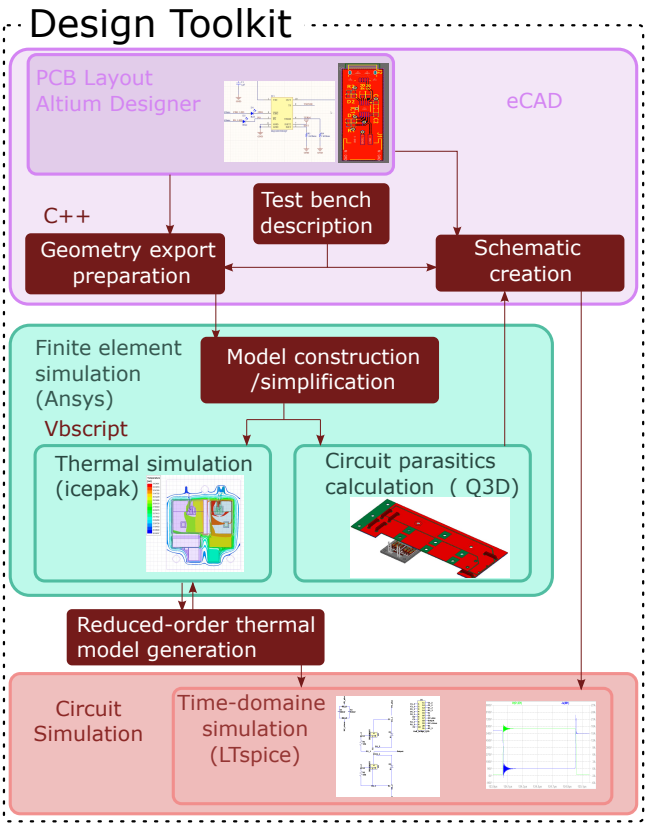

Figure 3.2: Virtual prototype synopsys

1 Overview of the procedure to build a Virtual Prototype

The modeling approach developed in this work is based on existing software tools, including electronic Computer-Aided Design (eCAD), Finite Elements (FE), Method of Moments (MoM), and circuit simulators. These tools are mature and can handle the high complexity of the models. The thesis contribution lies in:

- implementing code to connect various commercial software pieces
- processing the resulting data to automatically create a complete equivalent circuit model from the PCB design files
- investigating whether the models that can be generated this way are actually useful in a design process.

The workflow used to generate circuit models from the eCAD is illustrated in Fig. 3.2. The following pieces of software are employed: Altium Designer for eCAD (figure 3.3), Ansys suite (Q3D Extractor for computing circuit parasitics and Icepak for thermal analysis), and LTSpice for circuit simulation. The generation of a Virtual prototype involves three major steps:

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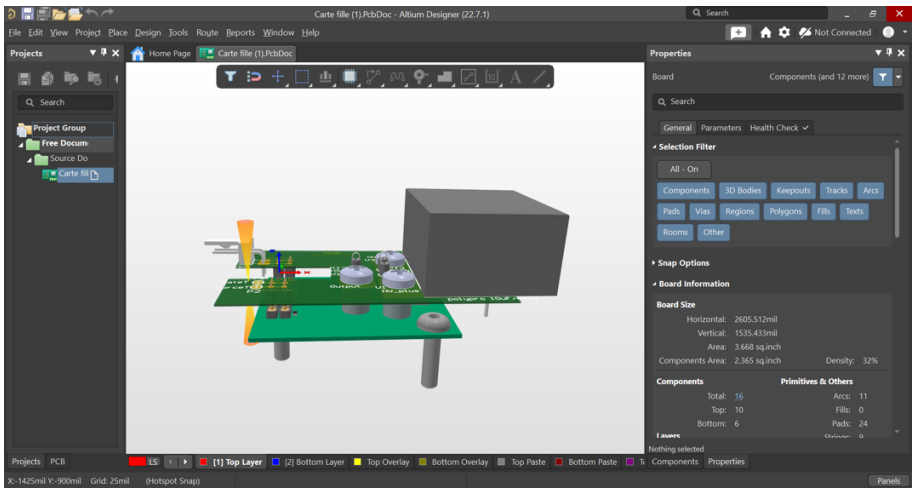

Figure 3.3: eCAD graphical user interface, showing a design where two PCBs are stacked

- Pre-processing: preparation of the FE/MoM models using the description of the PCB design.
- Simulation: FE thermal simulation (Icepak) & MoM electrical analysis (Q3D)
- Post-processing: Processing the resulting data of both thermal and electrical simulations to generate the circuit models and assemble them into the complete virtual prototype.

Our custom code is designed to handle various design files, models, and results. It is implemented as add-ons and scripts that are directly run from eCAD or FE/-MoM simulators using their scripting capabilities. The eCAD add-on illustrated in the flowchart 3.4, coded in C++, includes custom functions and methods that interact with the PCB design. It processes data, prompts the user for additional information, and manages data exchange. Additionally, the eCAD add-on generates system calls to run the FE/MoM simulators. The operation of these simulators is controlled by a custom script written in VBScript, which manages data import and the different stages of the workflow, including preparation of the 3D-model, simulation, and export of the resulting data. The software tools were chosen after extensive testing. Although other tools like Comsol or Ansys Mechanical can be used for thermal simulations, and Ansys Maxwell, HFSS or Comsol for electrical simulations, Q3D and Icepak were selected for their good performance, ease of use, and because they operate with the same 3D models, which means most of the pre-processing steps are common to both tools.

In this section, we present the preparation of the data needed for the FE/MoM simulation, based on the PCB description in eCAD. This includes a description of the data existing in the eCAD software, as well as of the data export/inport

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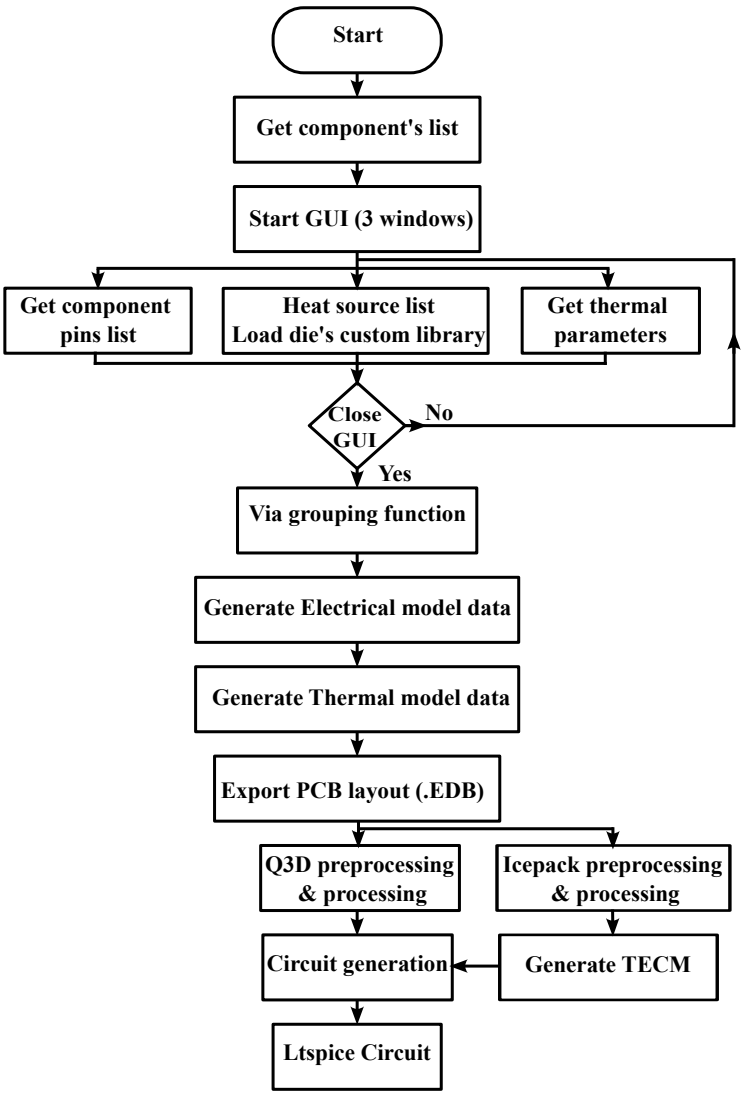

Figure 3.4: Flowchart for the Altium Add-On Algorithm

processes.

1.1 3D model preparation

The FE/MoM simulation tool requires a three-dimensional representation of the PCB geometry, which we will refer to as the "3D model". The quality of this model is crucial, and its preparation is described here. For the 3D model, the data needed to generate the necessary model can either exist in the eCAD description of the PCB or must be introduced by the user in custom ways, in the case the needed information is not managed of by the eCAD software.

Fig. 3.5 summarizes the data flows needed for designing a PCB, as well as to create a 3D model for electrical, thermal, and coupled models (Virtual prototype). This summary categorizes the data into two groups: the eCAD software's built-in data (schematic data, component data, and layout data), and a custom add-on program

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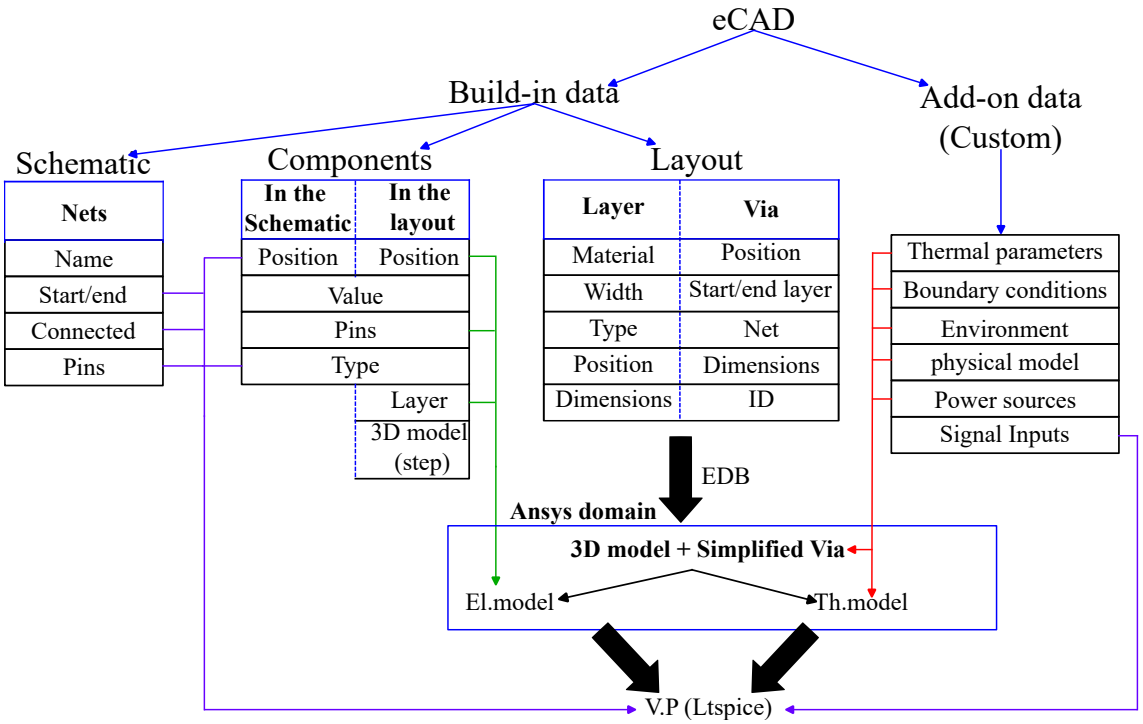

Figure 3.5: Exhaustive Data Classification Summary and Schematic Showing Utilization of Each Information Type

that has been integrated to collect extra information required to complete the model of the system under investigation. This ensures that all necessary data, including specific details not covered by the eCAD software, are accounted for to accurately complete the virtual prototype. It also shows the specific type of information and its use in generating the electrical model and thermal model in the Ansys domain or in building the final virtual prototype model (LTspice circuit).

1.1.1 Data described in eCAD

As mentioned in the previous chapter, eCAD is software primarily designed to create the files required by PCB manufacturers. Therefore, information that is not essential to this purpose may not exist in this type of software. However, due to the growing need for interfacing between different simulation software, additional data is regularly added to the eCAD description (e.g. physical properties of the materials).

When creating a PCB layout using eCAD software, the first step is to develop an electronic circuit (schematic) by adding electronic components and connecting them with nets (wires). Once the schematic is ready, the next step is to create the physical layout of the PCB ("routing"). During this process, the component symbols are replaced with their actual physical shapes (footprints), and the nets are translated into copper tracks. This stage involves defining the shape, positions,

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	Gerber	ODB++	IPC-2581	EDB
3D-model	– –	–	–	++
Layout details (materials,Nets)	–	–	+	++
Components details	–	–	+	++
Altium→HFSS layout	Yes	Yes	Yes	Yes
Altium→Siwave	Yes	Yes	Yes	Yes

Table 3.1: Comparison of the data transfer quality from Altium Designer to the Ansys suite.

and start and end points of all conductive elements (such as copper tracks, copper planes, and Vias/µVias) between the component footprints for every layer of the board.

Multiple file formats have been developed over the years for PCB layout descriptions, starting with the "Gerber" format (initially 2D, now extended to 3D), which was introduced in 1980, all the way up to more recent formats such as ODB++ and others. Each format has its own features, with variations between revisions (e.g., there have been 3 revisions of the ODB++ format so far) and between different implementations (some formats support proprietary extensions).

As a result, it's challenging to predict the quality of a layout description when exporting it from eCAD and importing it into FEM without conducting actual tests. The results of tests performed using Altium Designer and the Ansys Electromagnetic suite are summarized in Tab. 3.1. These tests revealed that some file formats do not preserve the 3D geometry of a multilayer PCB (they only describe 2D layouts, requiring some manual reordering), while others do not describe the component locations on the PCB.

It was also found that two software programs from the Ansys Suite (HFSS Layout and Siwave) can import PCB geometry descriptions. Both programs can generate a 3D model compatible with Q3D.

None of the standard file formats (Gerber, ODB++, etc.) allow seamless data transfer. However, a proprietary format (from Ansys) called "EDB" was found to offer better performance, with most features conserved and no errors observed. To use this format, an Altium plug-in provided by Ansys ("Ansys EDB Exporter" with a `*.def` file extension) must be installed. Exporting using the EDB format and importing through HFSS Layout is the approach adopted in this work.

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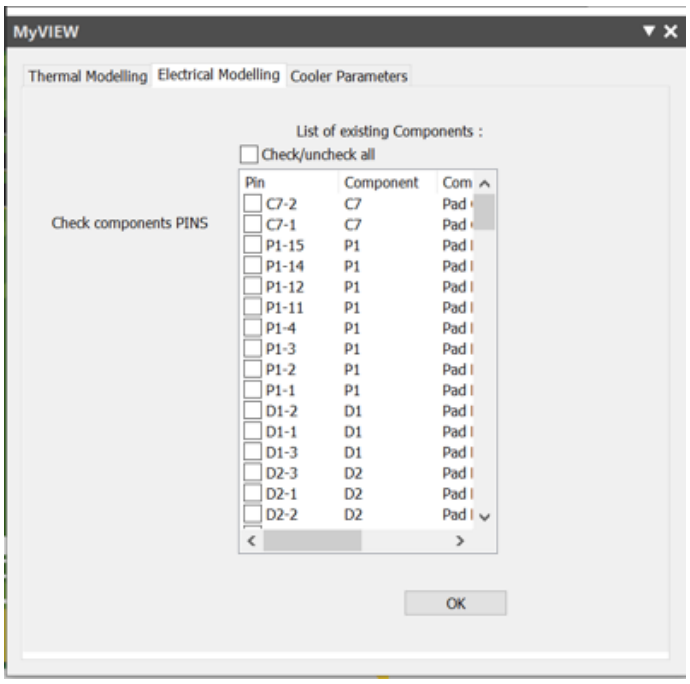

Figure 3.6: 1^{st} View to select the components for the electrical modelling

1.2 Custom data export

In our case, we need to build a virtual prototype that considers its environment (heat exchange interface, distance to conducting surfaces. . .). This requires detailed information about the external environment where the PCB will be implemented.

This information allows us to automatically extract corresponding boundary conditions (such as heat sources and cooling models), as well as what type of signals are present on the the system's electrical terminals.

Although eCAD offers insights into the PCB layout such as board size, layout, materials, and component details (position and footprint), it does not capture information about the board's environment (connections to supplies, control signals, loads, heatsinks) or the thermal properties of materials.

As a result, users are required to input this missing information. To facilitate this, we have included a custom graphical user interface (GUI) in the data export process, consisting of three windows. This interface allows users to enter data regarding boundary conditions, material properties, and information about the primary heat sources.

1.2.1 Electrical components window

The first window (Fig. 3.6) displays all the electrical components present in the PCB design. This allows the user to verify which elements should be included in the electrical model. The main purpose of this window is to ensure that our component

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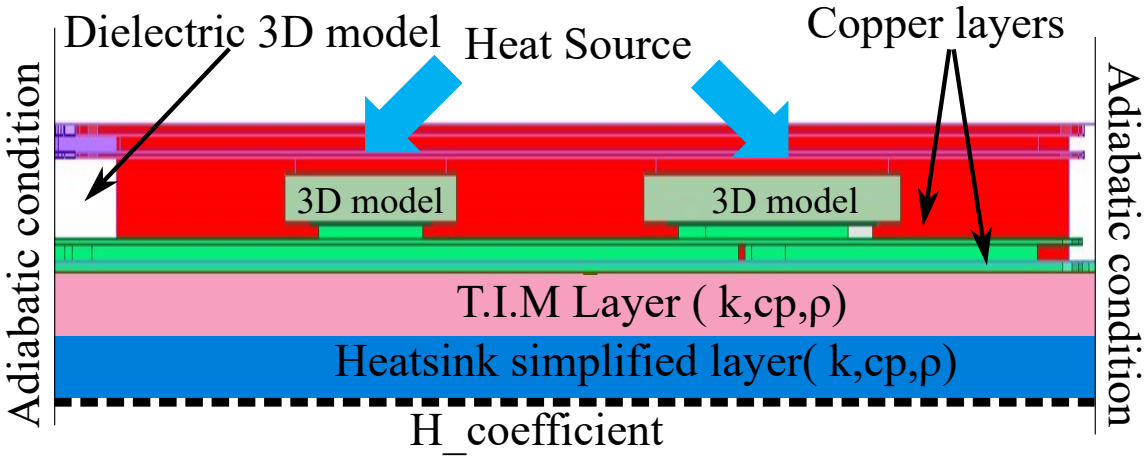

Figure 3.7: Final Thermal 3D Model Structure: PCB Layout 3D Model Objects (Copper Layers & Dielectric Layers) with Additional Custom Objects (T.I.M Layer & Heatsink) and Boundary Conditions

detection process is accurate, and it is validated by the user. The user has the option to eliminate any parts they consider unnecessary for the simulation or that have been wrongly defined. It has been observed that some components, especially custom-made ones, could be incorrectly defined. Examples of manual corrections needed are non-connected pins in integrated circuit packages or planar inductors that may be misclassified as multi-terminal components when they actually are a series-combination of tracks and Vias. In such cases, the user should unselect these pins so that they are not considered as terminal, eventually resulting in a smaller model. Alternatively, by default, all component pins are selected to be defined as terminals (sink/source).

1.2.2 Thermal model custom data

Fig. 3.7 displays a vertical structure such as those used in the Icepack 3D model. This visualization showcases the 3D model of the PCB (transparent, green, red, and purple elements). These elements are generated using information exported in the EDB format. The other (such as the 3D model of the heat sources, heat coefficient values, thermal parameters of the T.I.M., and the heatsink equivalent layer) are supplied by the user as the corresponding data are not managed by the eCAD.

As the model imported from the layout only describes the printed circuit board (with no components at all, neither embedded nor surface-mount), the 3D models of the heat sources must be created in their respective locations. In a typical power electronics system, the main power sources are the power switches(IGBT, MOSFET, diodes), inductors, and transformers. For the sake of simplicity, in our proof of concept, we chose to only consider the power switches.

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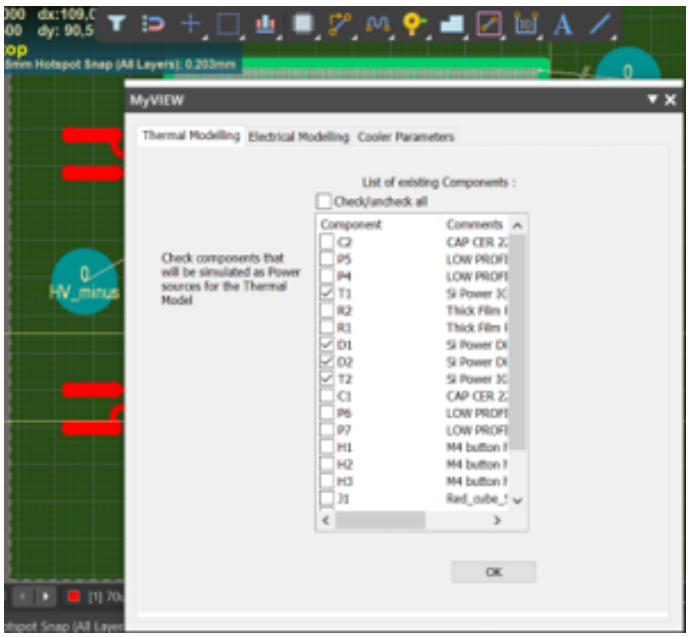


Figure 3.8: 2^{nd} View to select the Power Sources for the thermal modeling

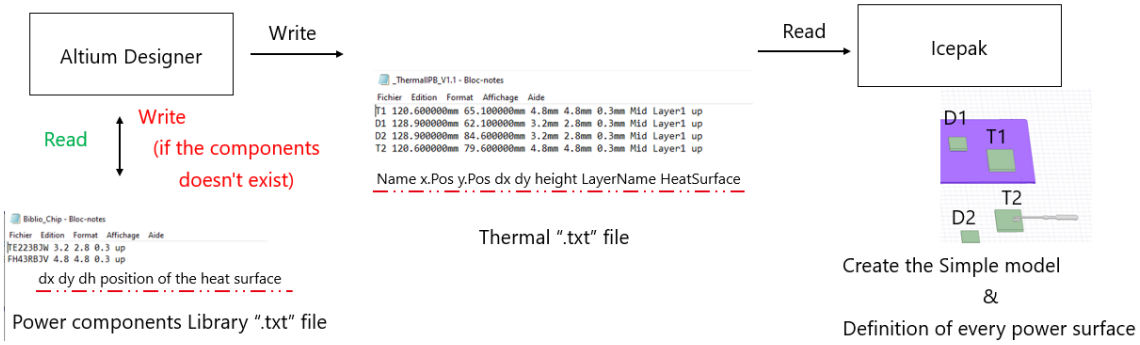


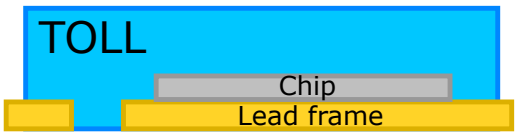
Figure 3.9: Chip custom library icepak

Power sources Window

In the second window (Fig. 3.8), users can choose the components they want to use as power sources for calculating thermal impedance (in this case, the power chips) from the list of all electrical components. The eCAD software treats all components equally, so manual interaction is required to specify the heat sources.

For thermal simulations, the 3D model must include the geometric description of the component being considered as a heat source. Unfortunately, the eCAD software

(a) Power Die structure



(b) The TO-Leadless package (TOLL) structure

Figure 3.10: Cross section of the two packages considered here (bare chip and TOLL package)

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(a) Die model (b) TOLL package model

Figure 3.11: Simplified models of the packages, for use in the Icepak model.

does not provide a usable description for this. Although the software has a 3D view feature for the PCB that uses ".step" files to describe component geometry, these models only show the external appearance of the components and do not provide additional data on the element's internal structure, materials, or location of the heat-dissipating element inside the package.

To address the lack of information in eCAD, we developed a very simple way to describe components: a text file containing component parameters such as their dimensions, and heat-dissipating surfaces. It is illustrated in Fig. 3.9. The user is required to write or update this custom library text according to the chip information that will be used in the analyzed PCB. This custom file provides the name, dimensions of the chip, and the heat source area location (the upper face or the bottom face). This file is added to the project files in the eCAD and is read by our custom C++ add-on. Then, for each power source component selected by the user, the add-on program uses the real position of the component in the PCB layout, computes and generates a text file summarizing the information needed to generate and locate the component in the 3D model.

Only two types of component packages are considered here: bare chips for embedding and TOLL packages for surface-mount transistors. The real structure of the packages is shown in Fig. 3.10, while their simplified 3D model is displayed in Fig. 3.11.

Cooling parameters window

The 3D model structure illustrated in Fig. 3.7, requires a simplified model of the external environment. A cooling system is an indispensable component of the complete converter structure, but it is typically not described in the eCAD. The cooling approach for PCBs varies based on the type of component packaging and PCB technology. For discrete component's technology, cooling can be achieved by mounting heatsinks on the component packaging (e.g., TO packaging) or on one or two faces of the PCB stack in the case of a medium cooling type, where the heat

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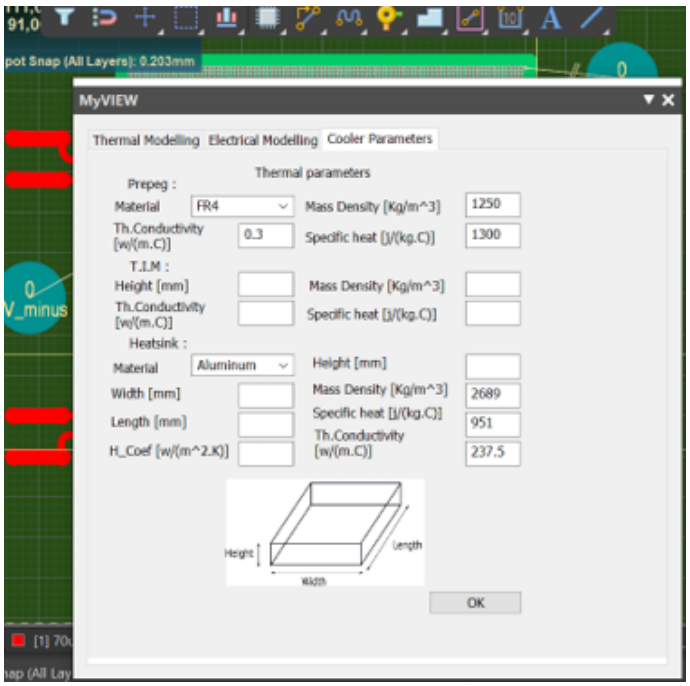

Figure 3.12: 3^{rd} View to define thermal parameters & boundary conditions

path is reinforced by thermal Vias. In our case, the cooling system is assumed to be located on the bottom face of the board. This specific type of cooling incorporates a thermal interface material (T.I.M) layer that fills the gaps between copper tracks and provides electrical isolation. In this scenario, a heatsink can be represented as a simple heat-exchange coefficient rather detailing its entire geometry.

In any case, the description of these elements is not included in the built-in data of the eCAD system; thus, a custom GUI (Fig. 3.12) has been implemented to gather the necessary information for generating the corresponding 3D model of such a structure (dimensions and thermal parameters of the T.I.M layer, the Cold plate and heat coefficient value).

1.2.3 Conclusion on data export

Among the various file formats that exixt to describe a PCB design, the "EDB" format was found to work best with the FEM/MoM software from Ansys. In addition, while data export mainly relies on such files that are generated directly by the eCAD, additional information was found to be necessary: manual simplification to weed out useless "components" (such as inactive pins in an IC package), selection of heat-dissipating elements, and definition of thermal boundary conditions. This manual input from the user is managed by custom GUIs.

Furthermore, it was found that the description of component packages is incomplete in the eCAD, as it does not detail their internal structure (geometry and

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materials). Therefore, an additional library file was introduced as a workaround.

1.3 3D model simplification

A typical PCB contains many small features, such as thin tracks and micro vias, which can make the FE/MoM models more complex. To simplify the geometry and reduce processing time, number of mesh elements, and memory usage, it is important to simplify the model while keeping the maximum error within acceptable limits.

These simplifications are carried out in the 3D model preparation stage before the simulation. To manage these simplifications, custom code is utilized in eCAD and EM/MoM software. Instead of relying on expert intervention to aggressively simplify the circuit by discarding irrelevant components, the focus is on utilizing automatic simplification methods that do not demand expertise. These methods are outlined below.

The geometric simplifications involve faceting circular surfaces, and substituting groups of vias with a single s"box". These geometric simplifications will be detailed in this section.

1.3.1 Faceting

The first step in simplifying the 3D-model geometry is to change its complex forms into simpler shapes to make the meshing process easier. Specifically, cylindrical shapes such as Vias and holes are not well-suited for meshing with polygonal elements. The idea is to transform the curves into faceted polygons. Ansys HFSS provides a feature for this kind of simplification.

An analysis was conducted on a case study involving a moderately complex 3D model to demonstrate the impact of geometry simplification. The case study involved a six-layer PCB with 70 µm-thick copper layers and a total of 20489 cylindrical Vias and µVias. The simulations aimed to assess the effects of converting cylinders and curves to polygons with different numbers of facets (N= 4, 12, 24). The effect of grouping vias clusters in "boxes" (as will be described in the next section) is also considered

The results of the analysis are shown in Fig. 3.13. This figure illustrates the impact of simplifications on processing time, mesh element count, memory usage, and maximum error. The error was calculated by comparing the R, L, and C matrices generated by Q3D Extractor for each element, with and without simplification. The value in the bottom right of Fig. 3.13 represents the largest deviation observed.

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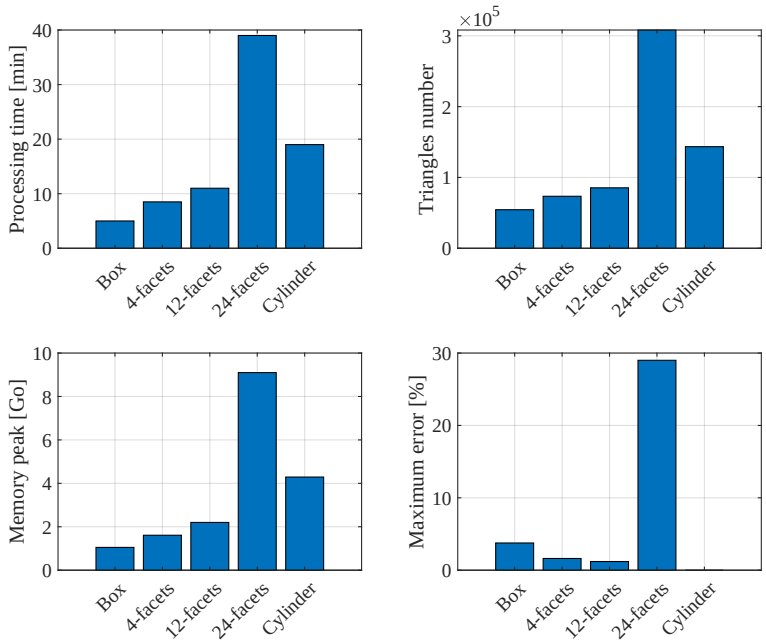

Figure 3.13: Effect of the geometry simplifications on Q3D Extractor calculations (processing time, number of elements in the mesh, memory used, and maximum error compared to the case without simplification – cylinder –), for the half-bridge example presented in this article (on a Core i7 workstation with 16 Go RAM.

The results depicted in Fig. 3.13 reveal that systematic simplification, such as faceting circular shapes, leads to a significant improvement in processing time and memory usage. The 4-facet simplification results in over a 50 %reduction in processing time and memory usage compared to the cylinder case, with only a slight increase in error (≈2 %). Increasing the number of facets to 12 has minimal impact on error reduction. However, further increasing the facets to 24 leads to a notable degradation in all parameters, including error, possibly due to numerical instabilities.

Additionally, box simplification offers a shorter processing time and memory usage compared to the 4-facet case, with a slightly larger but still acceptable error of approximately ≈4 %.

It can be concluded that systematic simplification, such as faceting circular shapes, leads to a significant improvement in processing time and memory usage, especially when combined with the grouping of via clusters (see further below). In light of these findings, an algorithm to automatically perform this via "boxing" is described in the next section.

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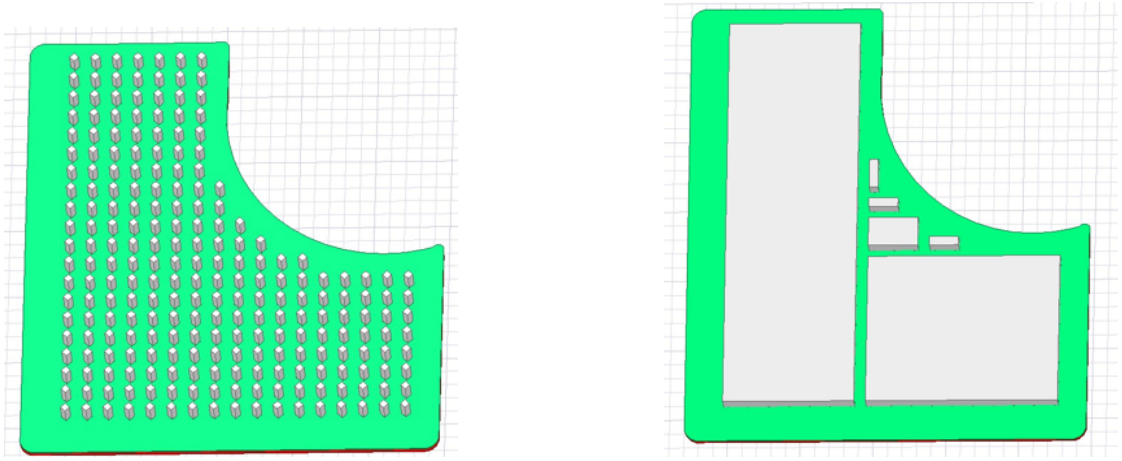

(a) A part of the 3D-model with 232 Vias

(b) The same object with the Vias simplified to 6 boxes

Figure 3.14: Advanced simplification: transforming the groups of Vias into conductive boxes

1.3.2 Via groups clustering

In power electronics PCB designs, Vias and µVias play vital roles, serving both electrical and thermal functions. They ensure interconnection between various copper layers. Due to the high currents that power PCBs need to handle, multiple Vias are often used in parallel to minimize parasitic resistance. Additionally, µVias are necessary for connecting embedded components. Since copper Vias provide significantly better thermal conductivity than FR4, large clusters of closely spaced Vias (ranging from hundreds to thousands) are employed to create a low-resistance path for the heat to flow from the components to the heatsink.

In this section, we will go deeper into the process of Via group clustering (or "boxing"). The concept involves grouping Vias of the same electrical net and type and then enclosing them within simple rectangular shapes, as depicted in Fig. 3.14. This approach results in fewer, larger blocks, which can be meshed with fewer elements in the FE models.

While RF simulation software like Momentum RF/ADS incorporates a via array merging tool, the software suite we currently utilize lacks a similar simplification feature. Hence, we have developed a custom algorithm to implement this concept, which applies to both thermal and electrical modeling.

Power electronics PCB designs often feature groups of Vias organized in aligned or alternate (staggered) patterns, as represented in Fig. 3.15. Detecting and transforming these arrangements into simpler shapes may seem straightforward. However, this task becomes more complex in multi-layer PCBs where multiple nets coexist in the same areas. It is crucial to ensure that when clustering the Vias, intersecting

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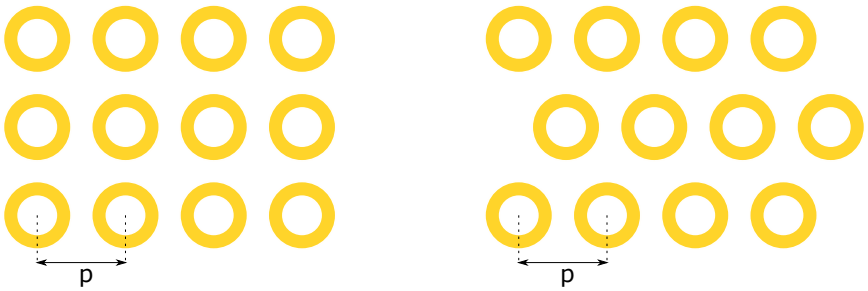
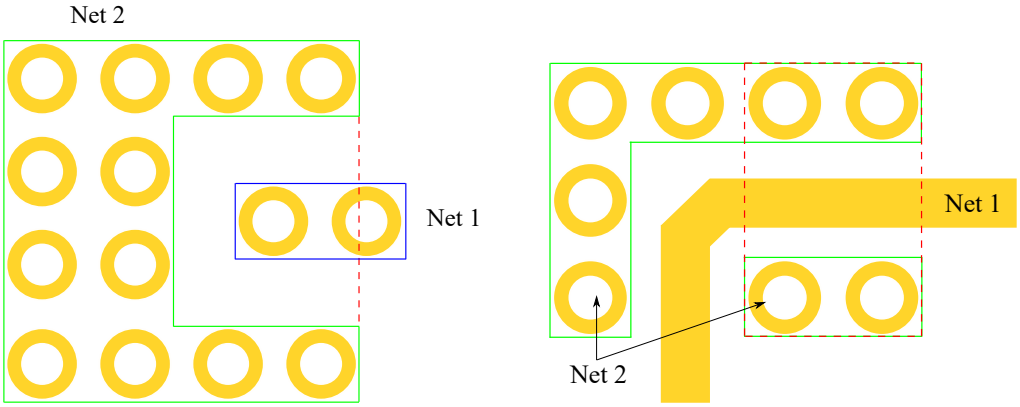


(a) Aligned Vias (b) Alternate Vias

Figure 3.15: Types of Via stitching



(a) Vias group 1 (b) Vias group2

Figure 3.16: Typical cases in which there is a risk of creating short circuits when clustering the vias of Net 2.

blocks are not formed, and short circuits between different nets are not created. Fig. 3.16 illustrateq typical scenarios that could lead to such issues.

The algorithm is written in two parts. The first part, written in C++, operates within the eCAD software and can access all the data related to the designed PCB. This part of the algorithm identifies groups of Vias suitable for the clustering transformation. It does this by segregating them based on the electrical nets they are connected to, as well as their start and end layers. The algorithm computes the dimensions and the location of the rectangular form of the biggest surfaces surrounding these Vias, which will replace them in the final generated 3D model. This operation is performed in the eCAD software add-on, as it has access to all the needed data (location, net of the vias, etc.) and because the C++ code operates faster compared to scripts in ANSYS. This part of the code generates a text file (Fig. 3.18) containing the information required for creating replacement shapes and their corresponding thermal parameters (discussed further below). This data is then used by the second part of the code, running in the HFSS Ansys module, to actually remove the listed vias and create rectangular shapes.

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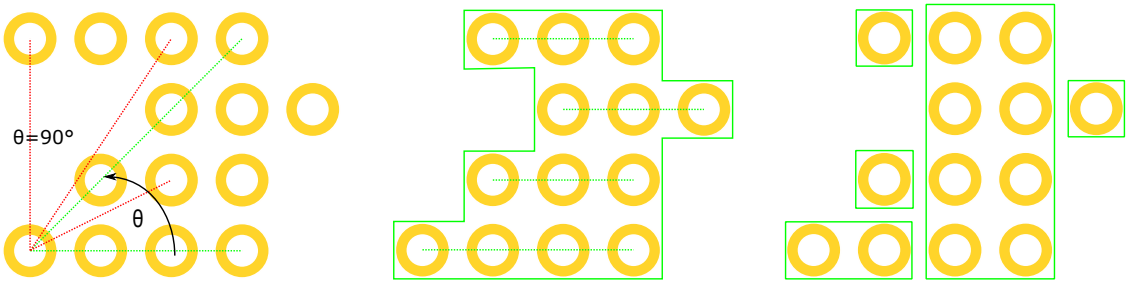

(a) Vias lines by angle (b) Vias polygon matrix construction (c) Rectangles reconstruction

Figure 3.17: Via grouping algorithm principle steps

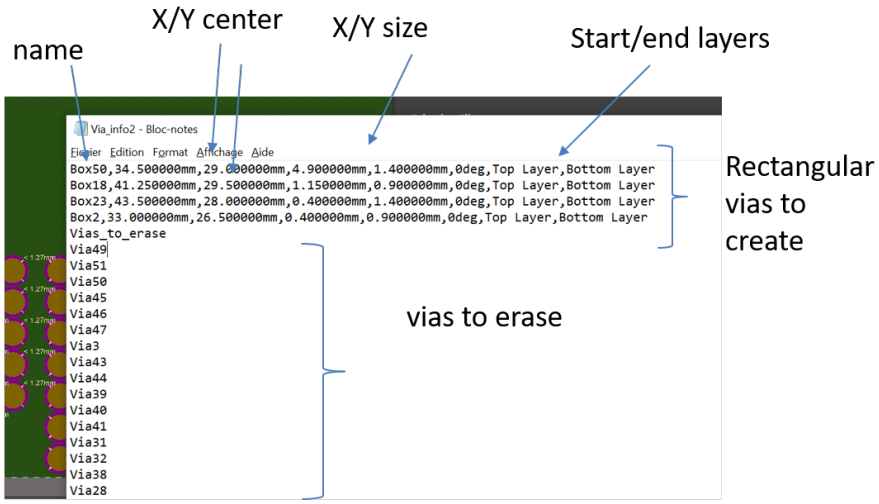

Figure 3.18: example of text file listing the blocks to be built and the Vias to be removed as part of the via clustering procedure.

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The first part of the Via grouping algorithm involves analyzing all the Vias data of the PCB layout in the eCAD. This includes the location of each Via, their starting and ending layers, and the electrical net to which they are related. Based on this information, a rearrangement of these Vias is created with increasing x and y coordinates in a 3-dimensional matrix (where the first dimension represents their type: same net, same starting/ending layers, and the second and third dimensions represent X and Y coordinates).

It is important to classify Vias by type to prevent short-circuit incidents when simplifying the geometry. Only Vias that are within a fixed maximum critical distance (for example, 2 times the size of the Vias) should be associated. Vias that are considered too far apart will not be associated. This condition prevents connecting different nets together, as shown in Fig. 3.16. The algorithm starts by identifying groups of closely spaced Vias of the same type and calculating their angles relative to the reference X-axis (as depicted in figure 3.17a). Beginning with a single Via, all the linear alignments it belongs to are detected, forming a set of lines—each representing an array of Vias aligned at a specific angle. These lines are then organized into a table for analysis.

To simplify the layout, the algorithm searches for patterns within these groups by treating them as imaginary, parallel lines of Vias aligned at the same angle. Priority is given to the longest lines, especially those oriented at 0° and 90°, which are more likely to form clean, rectangular shapes. A filtering process selects only the closest and most densely populated lines, and from these, a polygonal structure is created by combining the longest lines that share the same angle(as illustrated in Figure 3.17b). Once a polygon is formed, the Vias involved are removed from the main table to prevent duplication, and the process repeats for the remaining ungrouped Vias until the entire set is analyzed and grouped into simple, structured forms. The next step is to iteratively divide these groups into rectangles composed of the largest number of Vias possible, thanks to a code inspired by an algorithm for finding the largest rectangle in histograms [86](as shown in figure 3.17c). Finally, the algorithm computes the position and dimensions of this new rectangle that will replace the Vias groups and writes the necessary data into a text file (Fig. 3.18).

The thermal parameters (thermal conductivity and specific heat) of the equivalent blocks [45, 87] are determined using a simple surface-ratio relationship between the copper and dielectric regions for the thermal model. This surface-ratio equation is only adapted to work for the µVias and the mechanical Vias (3.1). The case of filled mechanical Vias is not considered here, although it could be implemented

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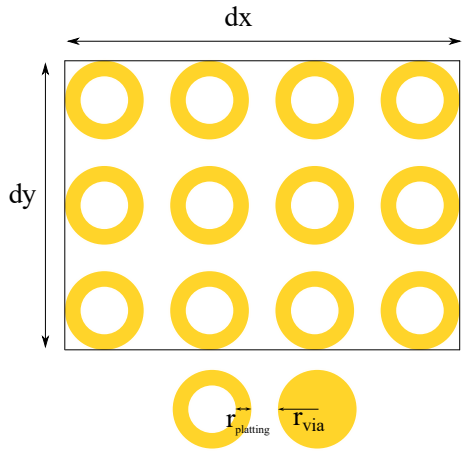

Figure 3.19: Example of a rectangular block for the Via group replacement and the definition of its geometrical parameters.

(providing information about the filling material is provided). Note that for the electrical model, the equivalent blocks are considered to be made out of pure copper, as the electrical resistance of the vias is very small.

$$X_{eq} = X_{preg}(1 + \frac{N.(S_{cu}.X_{cu} + S_{air}.X_{air})}{S_{box}.X_{preg}}) \tag{3.1}$$

$$with \begin{cases} X & = \rho,\ C_p,\ \lambda\text{: density of the material, specific heat capacity} \\ & \qquad \text{and thermal conductivity, respectively.} \\ S_{box} & = dx.dy \\ S_{cu} & = S_{via} - S_{air} \\ S_{via} & = 2\pi r_{via}^2 \\ S_{air} & = 2\pi(r_{via} - r_{platting})^2 \quad \text{if Via} \\ & = 0 \qquad\qquad\qquad\quad \text{if µVia} \end{cases} \tag{3.2}$$

1.4 3D Model preparation

Once the VBScript code in Ansys has imported the PCB layout (.EDB file), read the custom text file for the Vias boxing simplification and replaced the selected vias clusters with boxes, the next step is to generate a 3D model in ansys HFSS. At this stage faceting is performed on the model to reshape the round surfaces in to square forms, as presented before.

From this point, different operations are required for the electrical model (to be processed using Q3D Extractor) and the thermal model (Icepak). In fact, our process involves creating two distinct 3D models for thermal and electrical simulations. At this stage, the script can now set up the various simulation conditions for each 3D

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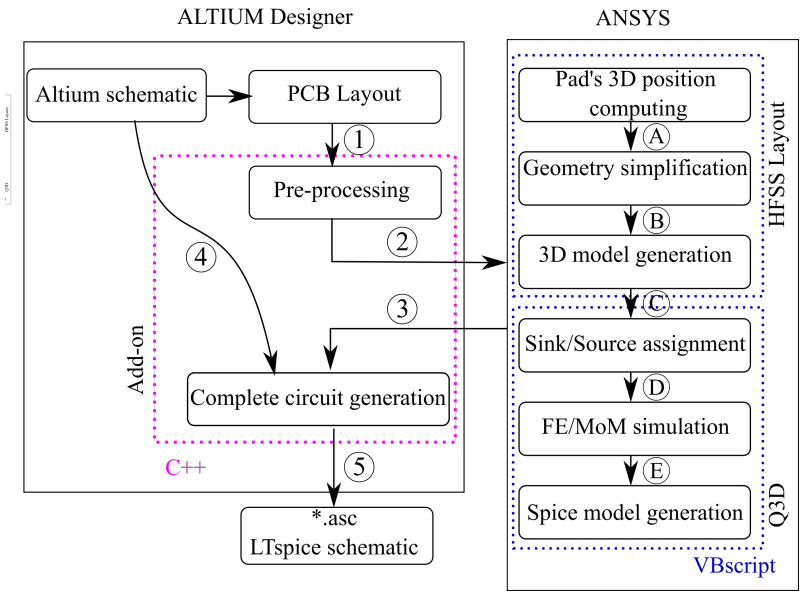
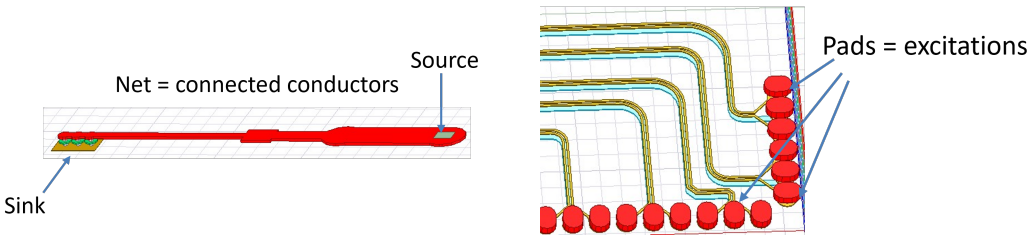


Figure 3.20: Description of the toolkit workflow



(a) Net & Terminals (b) Number of pads in different Nets

Figure 3.21: Denomination of elements in Q3D: a Net or groups of connected conductor objects (a); Many pads to be defined as terminals (Sink/Source)(b)

model corresponding to their specific requirements. These steps are outlined in the following sections.

1.4.1 Conditions set-up for Q3D

In the Q3D module of ANSYS, the script initiates by opening the first copy of the 3D model, designated as step Ⓒ in Fig. 3.20. As a reminder, the 3D model consists of copper layers with various tracks and electrical connections, dielectric layers, and simplified Via boxes, but no component models are included.

What is required to prepare the electrical 3D model includes unifying copper conductor objects and defining terminals corresponding to each component. It is important to note that these steps can be quite time-consuming and error-prone if done manually.

Unify object of same conductor

In Q3D, a group of connected electrical conductive objects is referred to as a

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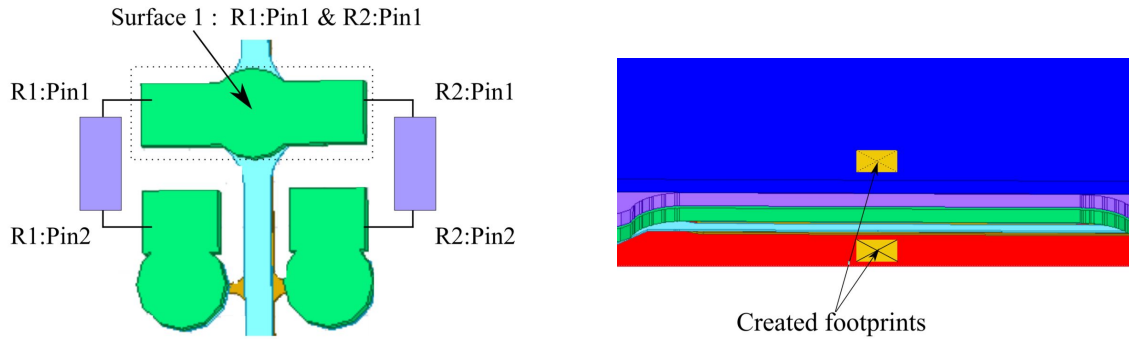

(a) Pins simplification (surface 1 is ≈2 mm long)

(b) Created surfaces for the sink/source assignments

Figure 3.22: Simplifying the number of terminals and creating footprints for detected faces with big area

"Net" (Fig. 3.21a shows a Net constituted by a number of conductive objects). The operation performed here involves unifying these various objects into one single object per Net. This simplification reduces the complexity of the 3D object definitions and aids in minimizing simulation memory usage and computational time.

Terminals definition

In the Q3D ANSYS simulator, a sink is defined as a terminal that absorbs current, while a source is a terminal that outputs current 3.21. Our custom script will use the Pin array data, which is a result of the data analysis step (referred to by Ⓐ in Fig. 3.20). It consists in computing the x,y,z, coordinates of each terminal surface. To compute these complete 3D coordinates, the algorithm uses the Pin's X and Y coordinates, the component's mounting layer information, and the layer thicknesses to determine the surface Z coordinates.

The automated process also addresses two specific issues. When a small surface, fixed in our case with a maximum area limit of 20 mm^2(defined by the largest footprint area of all the pads on our PCB), hosts two or more connections, it is simplified to a single terminal (Fig. 3.22a). On the contrary, small pads are defined on large conductor planes to define connection points (Fig. 3.22b) accurately (Q3D considers terminal surfaces to be equipotential, so it is important to define a small terminal area when it is located on a large plane).

Add simple model of cold plate

A conductor block is finally added to the bottom side of the PCB 3D model. This block represents a simplified cooler model if the user defined one using the export GUI (Fig. 3.12). This is crucial for accurately capturing the effect of the cold

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plate on the electromagnetic parasitic elements (capacitance and inductance).

1.4.2 Conditions set-up for Icepak

For the thermal model, several steps are needed to convert the 3D model of the layout (containing only simplified via groups, copper, and dielectric layers) into a complete 3D model ready for simulation using Icepak software (Fig. 3.24). This stage is denoted Ⓒ in Fig. 3.23. The task here involves adding the heat dissipating components to the 3D model, and adding the required thermal parameters and boundary conditions.

1- Defining the equivalent thermal parameters to the simplified Vias blocs

In Fig. 3.24, the transformed Via groups are still defined as copper blocks. At this stage, the script assigns the corresponding equivalent thermal parameters (λ, C_p, and ρ) for each of these blocks, computed using Equation (3.2).

2- Generating the 3D model for the cooling system

Based on the data (material parameters λ, C_p and ρ as well as the layer thickness) collected using our GUI, a 3D-model of the TIM and a simplified model of the cold plate (heat-exchange coefficient) are added to the bottom side of the PCB's 3D-model.

For further studies, a more sophisticated cooling system can be added to represent their geometry and environment more accurately. Icepak also provides the possibility of generating 3D models of coolers, such as heat sinks or fans.

3- Create the heat source 3D model

A simplified model is being created for each component selected by the user during the export process using the heat source selection window. An algorithm has been implemented to identify the reference designators and the 3D positions of the components based on the PCB layout. This algorithm extracts the necessary information from our custom power components library, which includes detailed physical descriptions of the components as explained in section 1.2.2. This process ensures the creation of valid 3D simplified models of the power components.

4- 3D-object subtraction

In Icepak software, the subtraction operation of objects in 3D models allows for the creation of complex geometries by subtracting one object from another.

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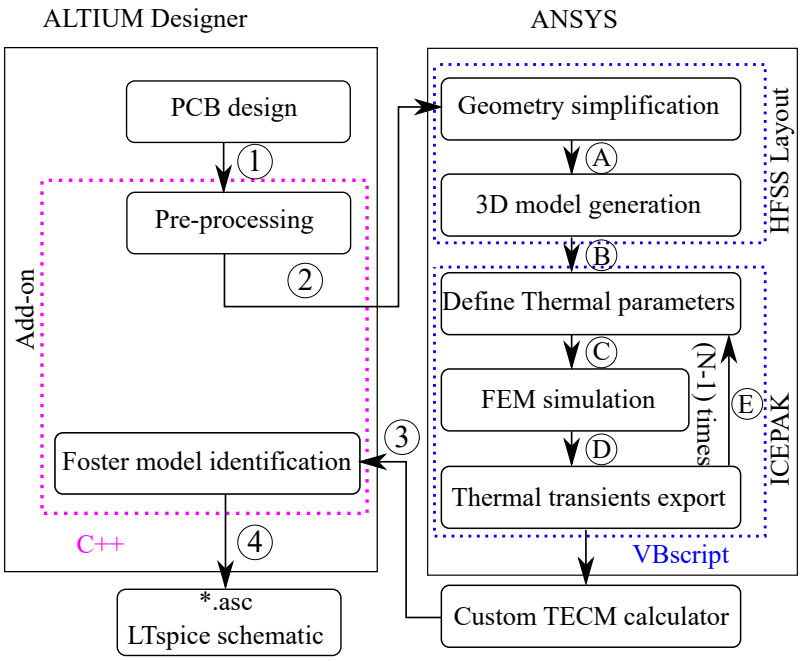

Figure 3.23: Description of the toolkit workflow

This feature allows the removal of a portion of one object from another, creating a void or cavity within the original object. In the initial state of the model in the figure 3.24 the dielectric material layers overlap on the newly created objects, such as the power components 3D-models and the boxed Vias groups. Therefore, the substraction operation must be applied to the dielectric layers and all the other the 3D-objects to create an accurately represented physical structure in the final 3D-model.

5- Defining boundary conditions

When performing thermal modeling in Icepak, defining heat sources and boundary conditions is essential to simulate the system's thermal behavior accurately.

This begins by defining a heat source on each corresponding face of the created 3D models of the power components. Additionally, a "temperature monitoring surface" is assigned to each of these components. It operates as a temperature sensor on the defined heat source surface, allowing the simulation to generate the necessary transient temperature curves. A list of the heat sources, containing their names, is then created, which will be used later for the iterative activation of these sources. To complete the definition of the thermal environment, the boundary conditions are set as shown in figure 3.24. This includes convective heat transfer coefficients on the bottom side of the cooling 3D model and adiabatic conditions on the rest of the external faces. This assumes that heat is only exchanged through the cooling side.

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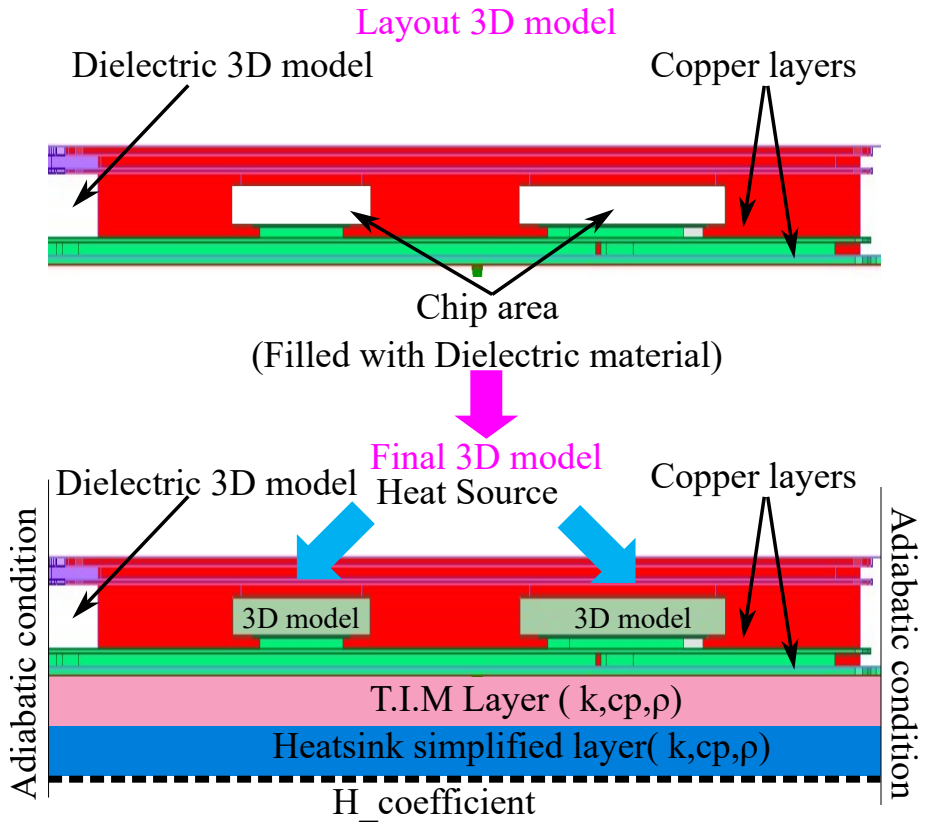

Figure 3.24: Transformation from the PCB layout 3D model to the final Thermal 3D Model

6- Simulation set-up

The final steps are to set the mesh options, thermal problem mode, time step, and simulation duration. The number of elements in the mesh plays a crucial role in determining the accuracy and computational efficiency of the thermal analysis. In our case, the mesh parameters are set to a minimum of 5 elements per object, with a maximum of 3 levels for the multilevel mesh feature. This feature adapts the mesh when transitioning between objects, especially when there is a significant size difference, such as between µVias and large planes. It also permits finer meshing in regions with high thermal gradients or complex geometries. The analysis mode is defined as a heat conduction problem.

Ultimately, a logarithmic time step is defined for the transient heat conduction simulations. Logarithmic time steps enhance the representation of transient thermal behavior, effectively capturing changes in temperature over several orders of magnitude (Smaller time steps at the beginning capture the fast dynamics accurately, while larger steps are sufficient later on). Logarithmic time step is also useful to build a compact RC model afterwards [2]. Arbitrarily, the simulation is set to a duration of 500 s, which is typically sufficient to ensure thermal steady state has been reach given the size of PCB electronics.

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1.5 Conclusion

The pre-processing phase involves the data export-import using the EDB file format for the layout description and custom text files which contain additional information (captured from the eCAD and from the user through custom GUIs (subsection 1.2).

An Ansys script then extracts the required information from these data to build the 3D model and perform systematic simplification (faceting, grouping of vias). It also prepares the 3D models for the electrical simulation (computing of the Pads locations and defining of the terminals of the electrical model) and for the thermal simulation (creation of the 3D model of the power sources and definition of the heat-dissipating surfaces).

The developed script effectively manages the pre-processing step, often the most time-consuming and tedious part of the simulation process.

2 Processing and post-processing

The simulation step starts automatically after completing the 3D model preparation steps. The algorithm in the Ansys environment runs the electrical simulation using Q3D Extractor and exports the analysis results as a SPICE circuit model (a feature of Q3D). For the thermal model, the algorithm runs successive Icepak simulations (one per heat-dissipating components) and processes the resulting temperature profiles to generate a compact RC model.

2.1 Electrical model

The process of creating the electrical model (Fig. 3.25) from the 3D model of the PCB is divided into two main steps:

1. Perform an Electromagnetic (EM) simulation using Ansys Q3D extractor
2. Process the simulation results and integrate them into the electrical circuit of the DUT

2.1.1 EM simulation

Ansys Q3D uses the Method of Moments (MoM) and the FEM with a quasi-static (QS) approach. This approach formulates equivalent circuits of layout parasitics in the form of R-L-C-G lumped elements (Fig. 3.26), where R-L and C-G are calculated

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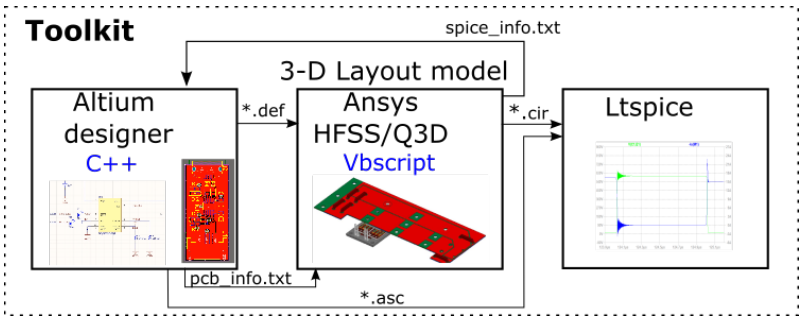
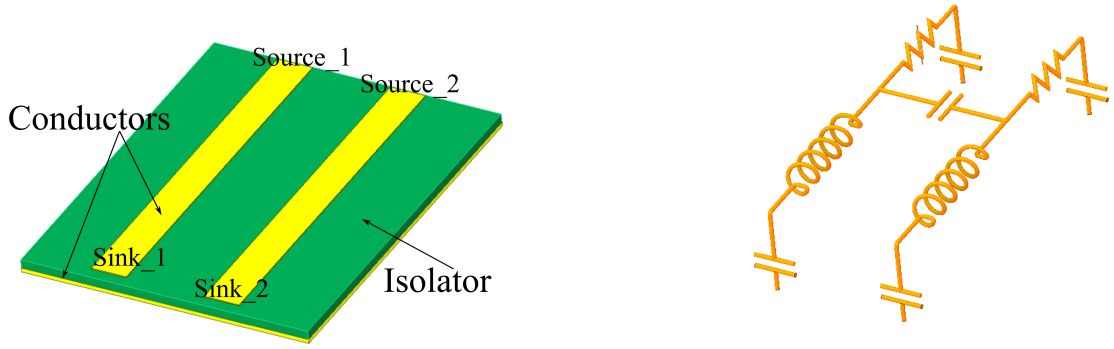


Figure 3.25: The workflow for generating an electrical model.



(a) 3D-model of a PCB sample as an input for Q3D

(b) RLGC equivalent model

Figure 3.26: 3D-model of a PCB sample as an input for Q3D and an example of the extracted RLGC model.

by decoupling the electric and magnetic field components in Maxwell's equations. Additionally, it calculates the capacitive and inductive effects using two independent solvers (3-D MoM electrostatic and a 3-D MoM Magnetostatic solver) [88, 89, 90]. Theoretically, Q3D is based on the PEEC method, which discretizes the quasi-static integral equations and transfers the problem from the electromagnetic domain to the circuit domain. At high frequencies, high-order modes and propagation effects become significant, rendering the QS assumption invalid. While the simulation results are precise up to hundreds of Megahertz, significant inaccuracy is observed at frequencies of 1 GHz and above. The frequencies encountered in power electronics applications include line frequency (50 Hz), switching frequency (ranging from tens of kHz up to the MHz range), and high frequencies linked with switching transients (from approximately 50 MHz up to approximately 1 GHz). Therefore, the quasi-static approach works well in this scenario.

2.1.2 EM Simulation results processing

Once the Q3D simulation is complete, an RLGC model of each interconnection (including the different coupling effects) is computed. This model is organized into

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	C1-2	C2-2	D1-2	C1	D1-1	D2-2	R1-1	E1	C2	C1-1	C2-1	D2-1	R2-1	E2	R1-2	G2
C1-2	1.779	1.487	1.234	1.270	0.415	0.622	0.433	0.445	0.575	0.336	0.308	0.288	0.237	0.247	-0.012	0.009
C2-2	1.487	2.544	0.990	0.985	0.410	0.577	0.389	0.401	0.512	0.308	0.444	0.206	0.138	0.147	-0.011	0.009
D1-2	1.234	0.990	2.720	2.633	0.873	0.470	0.777	0.794	0.575	0.318	0.236	0.494	0.578	0.589	-0.015	0.010
C1	1.270	0.985	2.633	3.497	0.605	0.704	1.180	1.195	0.871	0.289	0.191	0.601	0.739	0.750	-0.015	0.011
D1-1	0.415	0.410	0.873	0.605	1.848	1.144	1.420	1.446	1.194	0.321	0.306	0.342	0.373	0.387	-0.023	0.014
D2-2	0.622	0.577	0.470	0.704	1.144	3.494	1.382	1.407	2.807	0.120	0.159	0.843	0.286	0.301	-0.023	0.016
R1-1	0.433	0.389	0.777	1.180	1.420	1.382	1.937	1.890	1.498	0.281	0.252	0.441	0.529	0.543	-0.016	0.014
E1	0.445	0.401	0.794	1.195	1.446	1.407	1.890	1.920	1.523	0.291	0.261	0.452	0.540	0.554	-0.026	0.014
C2	0.575	0.512	0.575	0.871	1.194	2.807	1.498	1.523	3.147	0.189	0.178	0.791	0.980	0.994	-0.023	0.015
C1-1	0.336	0.308	0.318	0.289	0.321	0.120	0.281	0.291	0.189	1.788	1.503	1.223	1.276	1.288	-0.009	0.011
C2-1	0.308	0.444	0.236	0.191	0.306	0.159	0.252	0.261	0.178	1.503	2.600	0.953	0.957	0.969	-0.009	0.011
D2-1	0.288	0.206	0.494	0.601	0.342	0.843	0.441	0.452	0.791	1.223	0.953	2.887	2.761	2.774	-0.010	0.013
R2-1	0.237	0.138	0.578	0.739	0.373	0.286	0.529	0.540	0.980	1.276	0.957	2.761	3.681	3.619	-0.010	0.005
E2	0.247	0.147	0.589	0.750	0.387	0.301	0.543	0.554	0.994	1.288	0.969	2.774	3.619	3.635	-0.011	0.014
R1-2	-0.012	-0.011	-0.015	-0.015	-0.023	-0.023	-0.016	-0.026	-0.023	-0.009	-0.009	-0.010	-0.010	-0.011	0.047	-0.001
G2	0.009	0.009	0.010	0.011	0.014	0.016	0.014	0.014	0.015	0.011	0.011	0.013	0.005	0.014	-0.001	0.047

Table 3.2: An example of the inductance matrix (L_{AC} $[nH]$ for a frequency of 500 MHz) for a half-bridge cell (this test case will be presented in the next chapter). The matrix was computed using Ansys Q3D Extractor, with sources and sinks placed automatically. The diagonal elements indicate the inductance from each source to the corresponding sink of each net (there are 5 nets and 5 sinks). The off-diagonal elements represent the mutual inductance between any two nets.

tables that provide a comprehensive representation of the electrical characteristics of the circuit. For example, one of these tables is presented in Table 3.2. It contains the AC inductance values that form part of the RLGC model of a PCB sample.

Ansys Q3D can also generate a SPICE model from the RLGC parameters. This feature allows the creation of an equivalent circuit model that can be used for circuit simulation in tools like LTSpice. This equivalent electrical model is generally represented in a sub-circuit block model with the corresponding number of pins in LTspice. Fig. 3.27b displays the complete electrical model of a half-bridge PCB, where we can see the Q3D-generated block with 21 pins.

Integrating the Ansys Q3D-generated block in LTSpice can be challenging, especially when dealing with a large number of pins. Manually managing the interface between these two software tools requires careful attention to detail and can be time-consuming. Ensuring that the pin mappings and connections are accurately translated from the Q3D model to the LTSpice schematic becomes increasingly complex as the number of pins grows.

Automating the integration process can greatly minimize the chance of errors and simplify the workflow when working with complex models containing many pins. Because our modeling approach consists in systematically processing all the interconnets of a PCB, the resulting model can be highly complex.

In consequence, an automatic procedure has been established: utilizing the Spice model of the layout (③ in Fig. 3.20) and the schematic of the circuit as it has been designed by the user in Altium Designer ④, one last C++ Altium program is used to generate a LTSpice schematic (`*.asc` format). It reads the Altium schematic (Fig. 3.27a) to get the connections between components, as well as the locations

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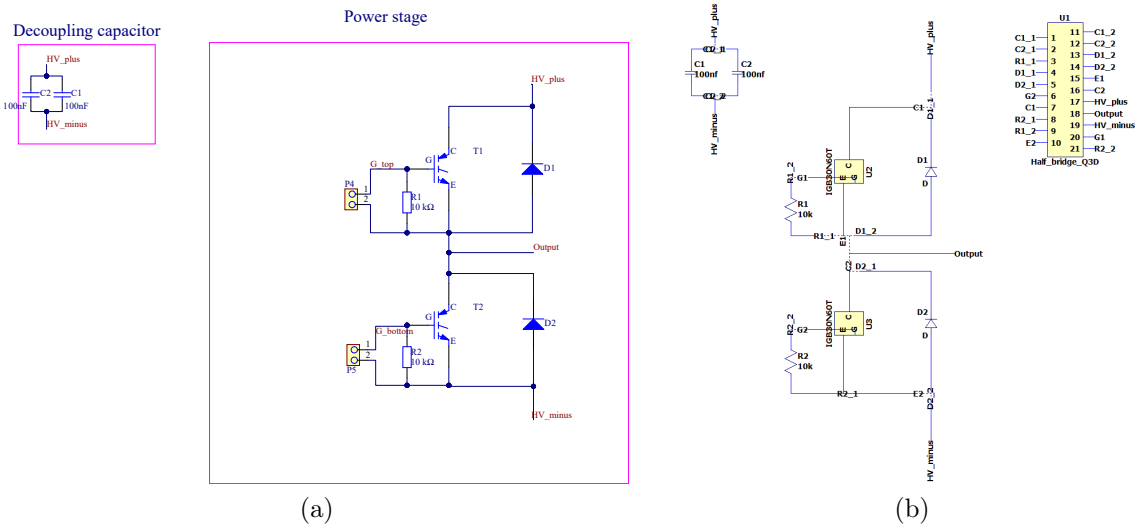

Figure 3.27: (a) Altium schematic of the embedded half-bridge structure used as an example and (b) LTSpice schematic generated automatically, using the Altium schematic to define the position of the component symbols. U1 (top right) contains the layout's spice model (parasitic elements) calculated using Q3D Extractor.

of the symbols on the schematic, to produce a readable output, in which all the connecting wires are replaced by their Q3D-calculated model (Fig. 3.27b).

The resulting schematic can then be opened in LTSpice, providing a human-readable complete schematic that simulates the electrical behavior of the DUT, including the effect of layout parasitics. To further improve this electrical model, an additional step must be performed manually, which involves adding the corresponding parasitic elements of the components themselves (such as the ESL/ESR of the capacitors) into their respective models. In our case, we incorporate the ESL and ESR values provided in the capacitors' datasheets into the corresponding capacitor models within the automatically generated LTspice complete circuit.

2.2 Thermal modelling

In this approach to thermal modeling, the goal is to create a RC behavioral model which includes each of the heat-dissipating components in the circuit (Fig. 3.28). This behavioral model concerns the thermal impedance between the "junction" of the main power-dissipating components (here, we are only considering the power semiconductor devices) and the environment, as well as the cross-coupling impedance (thermal impedance between any two components).

In the electrical modeling step presented in the previous section, the generation of the circuit model is taken care of by the simulation tool (Q3D, which includes a SPICE export feature). This is not the case for thermal modeling, for which a

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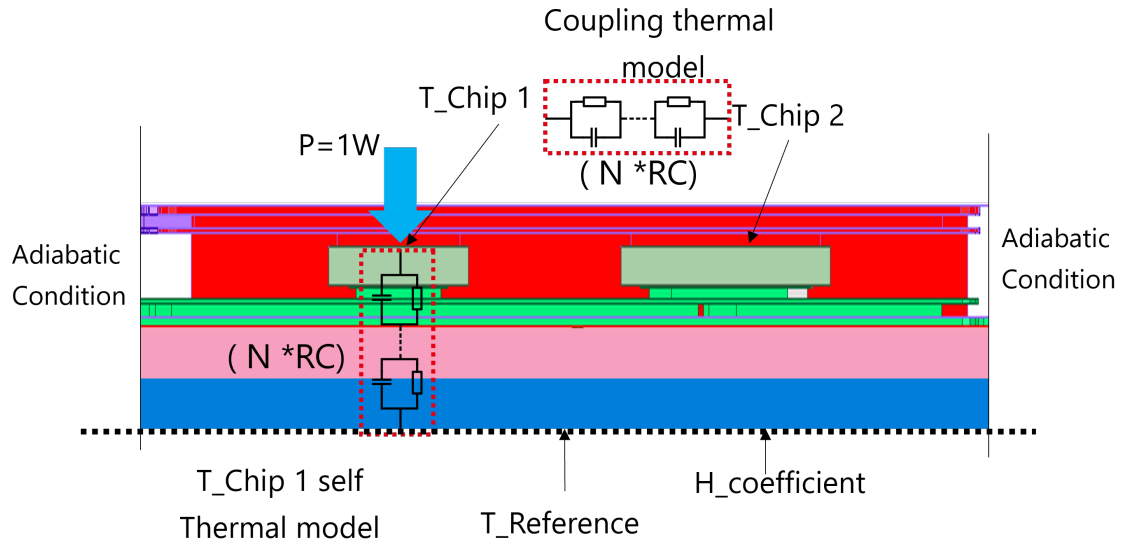

Figure 3.28: A sample of a complete 3D model of the DUT with defined boundary conditions and a circuit representation of the self and coupled thermal impedances for chip 1.

procedure has to be implemented to identify a circuit model. The approach involves two main steps:

1. Performing a series of FEM simulations to calculate the temperature changes in each of the heat-dissipating components.

2. Applying a custom identification procedure to generate a Thermal Equivalent Circuit Model (TECM).

2.2.1 FEM simulation

Once the essential preparations for the simulation are completed (see section 1.4.2, the transient thermal simulations are run. They follow an iterative approach where only one heat source is activated in each iteration (Fig. 3.28). This method is designed to examine the heat flow path from the source through surrounding materials, thereby assessing how a single heat generation point affects the system's overall temperature distribution and thermal performance. By focusing on each active heat source, we can quantify the coupling effect (how one source influences another). After each simulation, the transient temperature curves of each component considered are exported (whether the component was active or not). An example of such curves is given in Fig. 3.29.

2.2.2 Post-processing: Thermal Equivalent Circuit Model

The heating curves obtained from FEM simulations describe the temperature distribution within the system in response to each heating source. The procedure

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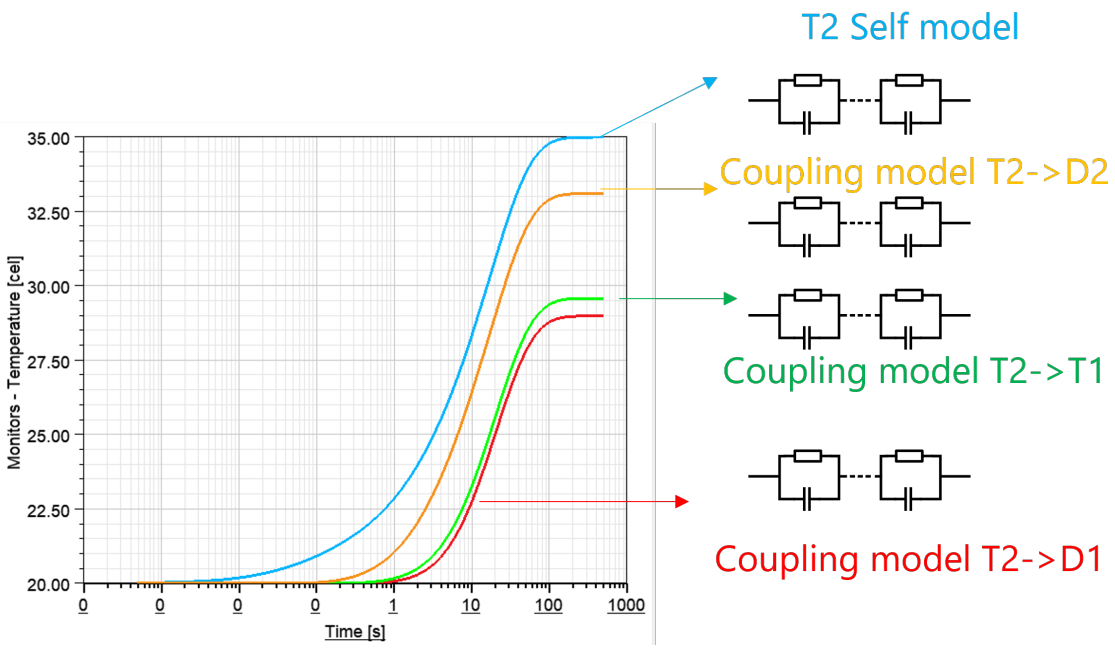

Figure 3.29: Heat curve result of the conduction simulation done by Icepak for the 3D model generated by the toolkit. IGBT T2 is active heat source in this sequence ($Power_{T2} = 10W$ and $T_{amb} = 20°C$)

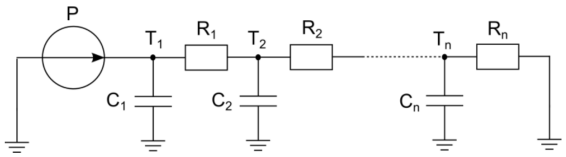

Figure 3.30: Cauer RC-network for one-dimensional heat flow

described in this section presents how to used these heating curves to generate a TECM. This model represents the thermal behavior of a PCB as an equivalent circuit such as those presented in Figs. 3.30 and 3.31.

In our case, the resulting TECM is structured using the Foster model (Fig. 3.31). It is a behavioral model created by fitting functions to measurement data or simulations. This contrasts with physically-based thermal models, such as the Cauer network, which are derived from the heat conduction equation and depend on the geometrical and material properties of the system's PCB. The critical difference between the two models lies in how capacitors are connected: in Foster networks, capacitors are connected in parallel with resistors, while in Cauer networks, they connect resistors to the ground. Although both models may yield identical temper-

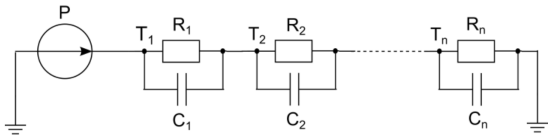

Figure 3.31: Foster RC-network

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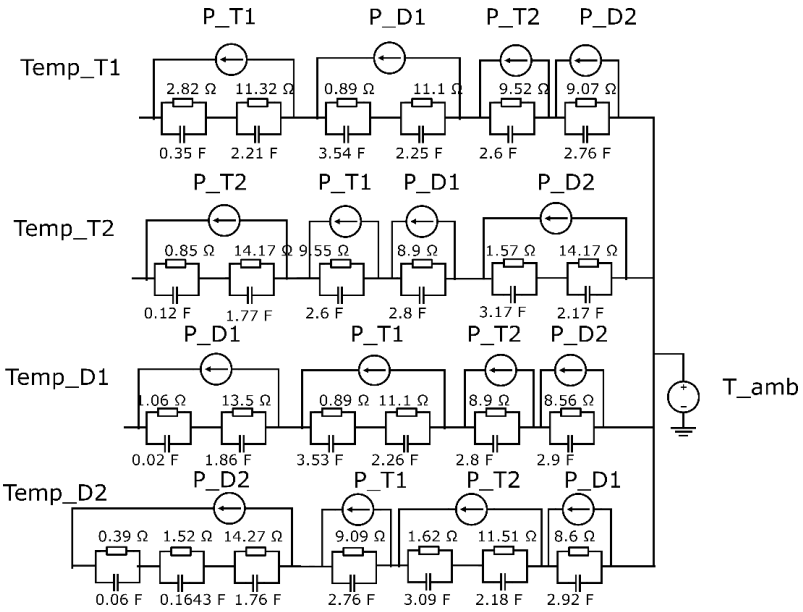

Figure 3.32: Complete equivalent circuit thermal model

ature responses for the first node (often the junction temperature), the values of their resistors and capacitors differ.

An example of a complete TCEM model for a half-bridge PCB (presented in the next chapter) is shown in Fig. 3.32. For each junction temperature (T_{T_1}, T_{D_1}, T_{T_2}, T_{D_2}), four Foster models (Z_{ij}) are connected in series. Each model is supplied with a current source that represents the power dissipated in the corresponding components.

2.2.3 Mathematical formulation of the Foster RC-network

This section presents a detailed development of the Foster network model using an analytical method. The transient heat conduction problem reduced to 1D, is given by:

$$\rho c_p \frac{\partial T(x,t)}{\partial t} = \lambda \frac{\partial^2 T(x,t)}{\partial x^2} \tag{3.3}$$

with

$$\begin{cases} T(x,t)\text{: temperature at position } x \text{ and time } t. \\ \rho, c_p \text{ and } \lambda\text{: density of the material, specific heat capacity} \\ \qquad\qquad \text{and thermal conductivity, respectively.} \end{cases}$$

This transient heat conduction problem can be solved using Duhamel's theorem. Duhamel's principle simplifies the analysis of these problems by utilizing the principle of superposition. It allows for a systematic approach by breaking down complex, time-varying scenarios into simpler, steady-state solutions, making it easier to cal-

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culate temperature distributions. The articles [91, 92] propose a solution that can be formulated as follows:

$$T(x,t) = T_{ref} + \int_0^t P(\tau)\frac{\partial Z_{th}(x,t-\tau)}{\partial t}\,d\tau \tag{3.4}$$

with

$$\begin{cases} Z_{th}(x,t-\tau)\text{: thermal impedance step response at position x and at a time-shifted by } \tau. \\ P(\tau)\text{: heat input at time } \tau. \end{cases}$$

For N heat source PCB, the superposition principle can be utilized [93]. Each heat source i can contribute to raising the temperature $T_j(t)$ at the center of the heat source j, where $i, j = 1, ..., N$:

$$T_j(t) = T_{ref} + \sum_{i=1}^{N_i}\int_0^t P_i(\tau)\frac{\partial Z_{th,ij}(t-\tau)}{\partial t}\,d\tau \tag{3.5}$$

The temperature rise in a chip originates both from self-heating and cross-coupling heating from other chips. Combining the thermal impedance Z_{th}:

$$Z_{th}(t) = \frac{\Delta T(t)}{P} \quad [°\text{C/W}] \tag{3.6}$$

with (3.5) yields (3.7). The diagonal elements ($i = j$) correspond to the characteristic impedance of each silicon chip, whereas off-diagonal elements ($i \neq j$) are mutual impedance

$$\begin{bmatrix} T_1 \\ T_2 \\ \dots \\ T_N \end{bmatrix} = \begin{bmatrix} Z_{th,11} & Z_{th,12} & \dots & Z_{th,1N} \\ Z_{th,21} & Z_{th,22} & \dots & Z_{th,2N} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{th,N1} & Z_{th,N2} & \dots & Z_{th,NN} \end{bmatrix} \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_N \end{bmatrix} + \begin{bmatrix} T_{ref} \\ T_{ref} \\ \vdots \\ T_{ref} \end{bmatrix} \tag{3.7}$$

A method used to determine the elements of this matrix is explained in [94, 95]. It involves injecting a step power loss into each chip individually and observing the corresponding temperature changes (see Fig. 3.29). To calculate the self-heating thermal impedance, the temperature difference between the junction temperature of the chip and a reference point (e.g., the ambient temperature) is divided by the power loss generated in that same chip.

To solve for the elements of the thermal impedance matrix, we will employ thermal network identification by deconvolution [1, 2], which can be regarded as a

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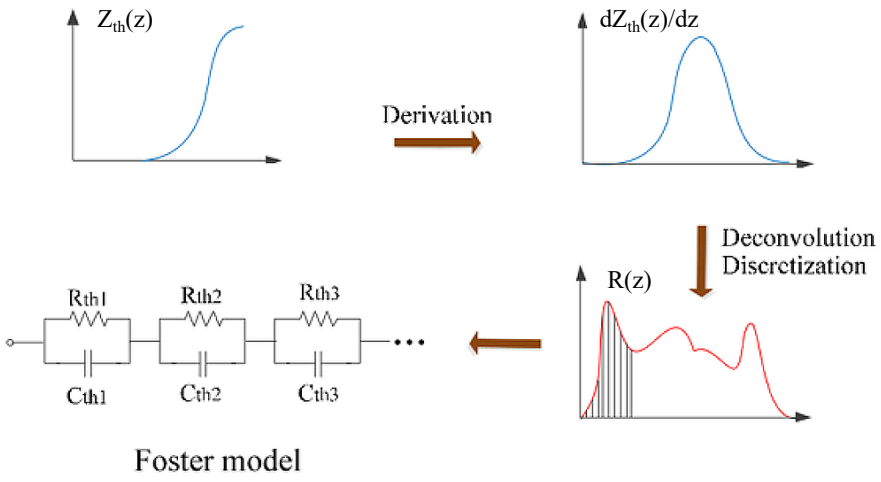

Figure 3.33: Foster equivalent circuit computing algorithm [1, 2]

curve-fitting approach. While traditional fitting methods often focus on the statistical optimization of parameters, deconvolution offers a more physically grounded perspective.

The Foster model representation of the step-response thermal impedance for the temperature measured at heat source j, in response to an injected power at heat source i, can be expressed as follows:

$$Z_{th,ij}(t) = \frac{T_j(t) - T_{ref}}{P_i(t)} \tag{3.8}$$

$$= \sum_{k=1}^{M_{ij}} R_{th,ij,k} \left(1 - e^{-\frac{t}{\tau_{ij,k}}}\right), \quad \tau_{ij,k} = R_{th,ij,k} C_{th,ij,k} \tag{3.9}$$

By introducing the logarithmic timescale $z = \ln(t)$ and $\zeta = \ln(\tau)$, and applying the time derivative, an equivalent form of the equation 3.9 can be expressed in the equation (3.10). Thus, the thermal time constant spectrum (TCS), $R(z)$, is expressed as follows [1, 96, 2]:

$$\frac{d}{dz} Z_{th}(z) = R(z) \otimes w(z) + n(z) \tag{3.10}$$

In this context, $\otimes$ represents the convolution operator, and $n(z)$ symbolizes the "measurement" noise (also applies to simulation data). The function $w(z)$, which serves as a fixed weighting function, represents the constructor. This fixed weighting function $w(z)$ captures the relationship between heat inputs and thermal responses, illustrating how heat distribution influences temperature changes across different

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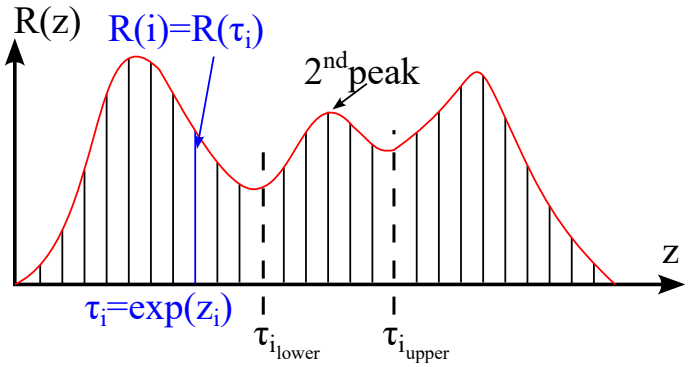

Figure 3.34: Discretized time constant spectrum $R(i)$.

time scales. It aids in accurate modeling, parameter estimation, and effective noise management in thermal network identification by deconvolution method (NID) [97, 98]. This relationship can be approximated by the following formula:

$$w(z) = \exp(z - \exp(z)) \tag{3.11}$$

Additionally, based on equation (3.10), the time constant spectrum can be expressed using formula (3.12):

$$R(z) = \frac{d}{dz} Z_{th}(z) \otimes^{-1} w(z) \tag{3.12}$$

where $\otimes^{-1}$ is the deconvolution operator.

The discretized time constant spectrum $R(i)$ can be estimated using iterative Bayesian deconvolution. This method combines measured temperature data and known heat inputs with prior information about the system. By applying Bayes' theorem, it iteratively increases both accuracy and resilience to noise [2, 99, 97, 100]:

$$R^{(n)}(i) = R^{(n-1)}(i) \sum_{k=0}^{M-1} w(k,i) \frac{\frac{d}{dz} Z_{th}(k)}{\sum_{j=0}^{M-1} w(k,j) R^{(n-1)}(j)} dt \ , \ i \in [0, M-1] \tag{3.13}$$

The iteration number n in the formula controls the convergence of the time constant spectrum estimation. Increasing n leads to more accurate and stable $R(i)$ reconstructions, but this should be balanced with noise sensitivity and computational cost.

The total thermal resistance associated with a specific time-constant interval $[i_1, i_2]$ is obtained by summing the contributions of the discretized time-constant spectrum $R(i)$ within that range. This summation, scaled by the time step $\Delta\tau$

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yields the cumulative resistance:

$$R_{th}(i_1, i_2) = \sum_{i=i_1}^{i_2} R(i)\Delta\tau \tag{3.14}$$

This value represents the portion of the overall thermal resistance that is attributable to processes occurring within the specified time-constant window. The corresponding thermal capacitance is derived from the identity:

$$\tau = R_{th} \cdot C \quad \Rightarrow \quad C = \frac{\tau}{R_{th}} \tag{3.15}$$

The proposed algorithm identifies local maxima in the time-constant spectrum curve to determine characteristic time constants τ that correspond to dominant thermal capacitances within the system. Each detected local maximum is interpreted as a significant thermal path or layer. The adjacent local minima surrounding each peak are used to define the lower (i_{lower}) and upper (i_{upper}) bounds of the corresponding time-constant interval(as illustrated in the figure 3.34). These bounds are the limits for summing the thermal resistance spectrum $R(i)$ within the identified region. By integrating $R(i)$ across this interval $[i_{lower}, i_{upper}]$, the thermal resistance associated with the identified thermal capacitance is computed.

Once all RC pairs have been extracted for each self and mutual thermal impedance, to improve the accuracy, a quadratic optimization process is performed on the reconstructed model (corresponding to the formula 3.9). In this step, the initially estimated RC values, obtained through the NID method, are used as starting points. The optimization minimizes the squared error between the simulated thermal impedance data and the reconstructed model response. This refinement enhances the fit and ensures better numerical stability and physical consistency.

After optimization, a SPICE-compatible netlist representing the identified RC ladder network is automatically generated. This netlist can be directly imported into simulation tools such as LTSpice, enabling detailed transient and steady-state thermal simulations that accurately reflect the system's original thermal behavior.

2.3 Conclusion on post-processing

Automatic simulation using Q3D Extractor and Icepak allows the generation of electrical and thermal models.

For the electrical model, Q3D directly generates a SPICE model, and our contribution was to automatically insert this model into the converter schematic to

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prevent errors and simplify operation, especially with complex models.

The thermal models require a more complex procedure: first, a succession of FEM simulations, in which only one component is active at a time, must be run to extract all the needed temperature profiles. Then, a custom TECM identification procedure based on Bayesian deconvolution is used to build a Foster model.

The validation of the models against experimental data is presented in the next chapter.

3 Conclusion

In this chapter, we have presented the workflow developed to automatically generate a virtual prototype. This process goes seamlessly from a power converter's printed circuit board design to a circuit model. By generating models for entire PCBs without requiring expertise in model generation or predefined structures, such approach can replicate the operating converter in the electrical and thermal domains, forming a comprehensive "virtual prototype" of the circuit.

The modeling approach in this work is focused on leveraging existing software tools such as electronic Computer-Aided Design (eCAD), Finite Elements (FE), Method of Moments (MoM), and circuit simulators. Our contribution lies in implementing code to connect various commercial software pieces and process the data to automatically create a complete equivalent circuit model from PCB design files. The workflow involves pre-processing, simulation using FE thermal simulation and MoM electrical analysis, and post-processing to generate the circuit models and assemble them into a complete virtual prototype. Custom code, implemented as add-ons and scripts, handles various design files, models, and results, interacts with the PCB design, processes data, prompts the user for additional information, and manages data exchange. This approach ensures that all necessary data, including specific details not covered by the eCAD software, is accounted for to complete the virtual prototype accurately.

Simplifying 3D models is a critical aspect of creating virtual prototypes for PCBs. Geometric simplifications such as faceting circular surfaces and grouping Vias are implemented. The resulting improvements in processing time, memory usage, and acceptable error margins demonstrate the significance of systematic simplification in the 3D model preparation stage for efficient simulation of larger systems. The custom algorithm developed for via grouping ensures that intersecting blocks are not formed and short circuits between different nets are avoided.

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The developed script manages the pre-processig (3D model preparation), processing (simulation) and post-processing (generation of compact models) stages. It follows essential steps for electrical modeling (such as defining terminals in Q3D) and thermal modeling (including defining heat sources, boundary conditions, and implementing subtraction operations in Icepak).

The resulting virtual prototype is an assembly of the generated electrical and thermal models. The electrical model is created using the SPICE model generated by Ansys Q3D (stray elements model) integrated in the electrical circuit of the system. The thermal model is developed by conducting FEM simulations to simulate temperature transient and then deriving a SPICE circuit model through a custom identification process.

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Chapter 4

Virtual prototype Validation

This chapter presents experimental test results and compares them with simulations to validate our modeling approaches. First, the electrical and thermal models are assessed separately. Then, they are merged into the "complete" virtual prototype (electro-thermal model).

Measurements are made on different types of PCB prototypes ("standard PCB technology" using discrete components and PCB-embedding technology).

Here is a more detailed view of the validation tests presented in this chapter:

1. Electrical validation:
   (a) Electrical impedance (validation of the layout parasitics model).
   (b) Double-pulse test (validation of the circuit model).
2. Thermal validation:
   (a) Single-chip thermal impedance measurements (elementary validation)
   (b) Multi-chip Thermal impedance measurements (validation of the cross-coupling predictions)
3. Electro-thermal validation:
   (a) Efficiency measurement using a calorimetry test.

1 Overview of the test vehicles

5 PCB designs are considered for test and validation. These DUTs differ in their number and types (Si diodes, Si IGBTs, SiC MOSFETs) of chips, and the PCB technology they employ (discrete and embedded).

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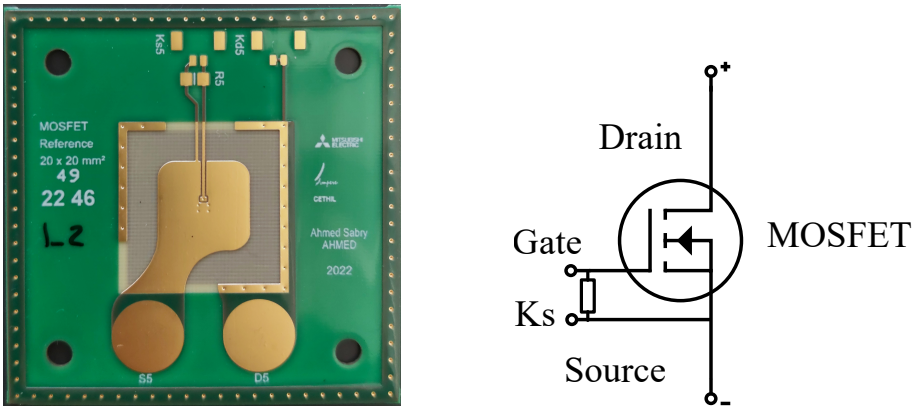
	PCB technology	Chips count	Electrical tests	Thermal tests
DUT ①:	Embedded	1		Self-heating Z_{th}
DUT ②:	Embedded	4	DPT Electrical impedance	Self-heating Z_{th} Cross-coupling Z_{th}
DUT ③:	Discrete	2	DPT Electrical impedance	Self-heating Z_{th} Cross-coupling Z_{th}
DUT ④:	Embedded	2	DPT Calorimetry test	Self-heating Z_{th} Cross-coupling Z_{th}
DUT ⑤:	Embedded	2	DPT Electrical impedance	Self-heating Z_{th} Cross-coupling Z_{th}

Table 4.1: DUTs used in this chapter



(a) (b)

Figure 4.1: DUT ① : Single chip (Cree CPM2-1200-0080A) prototype: photograph (a) and electrical circuit (b).

Tab. 4.1 presume information and comments about each one of the PCBs shown in Figs. 4.1, 4.2, 4.3, and 4.4.

DUT ①, presented in figure 4.1, includes a single SiC chip embedded in the PCB. The stuck used for this PCB is two copper layers connected with the embedded Die pads by µVias. This DUT is used for validation of the thermal model. Its structure is detailed in [101].

Fig. 4.2 presents DUT ②, a half-bridge cell comprised of 4 embedded Si dies (2 IGBTs and 2 Diodes). It was designed independently from this thesis work, and is rated at 600 V, 30 A. This DUT is used for double-pulse, electrical impedance, and thermal model validation (including cross-coupling effects). This 4 copper layer PCB is a good example of a simple switching cell with a large number of µvias.

Fig. 4.3 shows DUT ③, a half-bridge cell made of 2 discrete SiC MOSFETs in a leadless package (Wolfspeed C3M0060065L, TOLL package) and a buffer circuit for gate control. This DUT is also referred to as "Genesis discrete". Its design and that of the chip-embedded variant are described in the next chapter.

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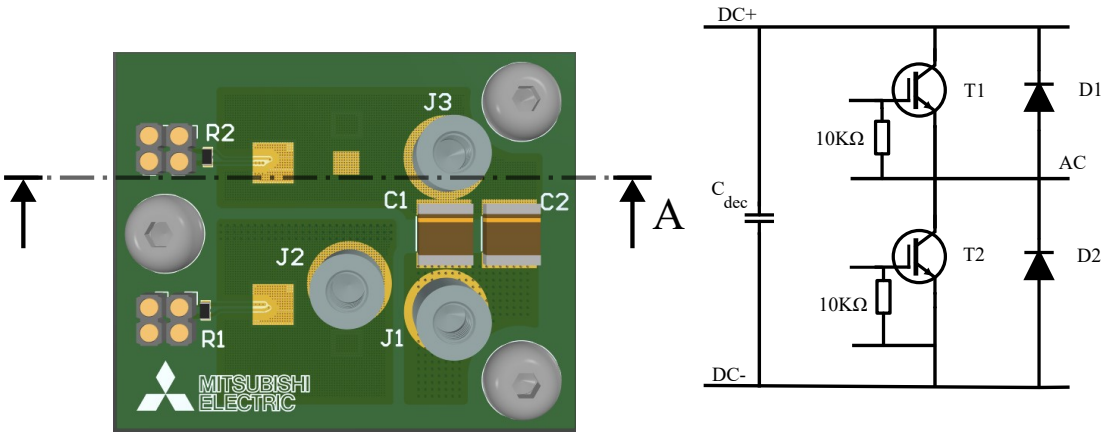
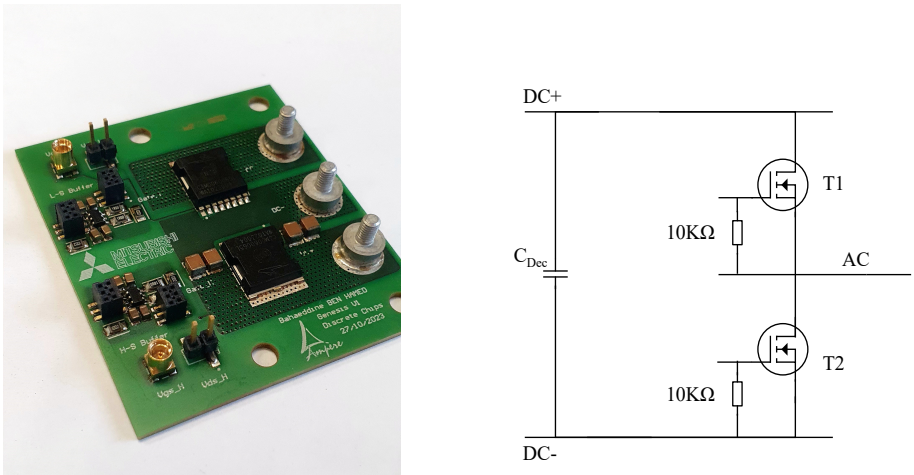


(a) (b)

Figure 4.2: DUT ②: Half-bridge PCB (2 IGBTs & 2 diodes): (a) upper view of the PCB, (b) circuit diagram

DUT ③ is used for double-pulse, thermal model, and power loss validation. This classic 4-copper-layer PCB with only through-hole Vias is a good test candidate for evaluating the limits of our models using less precise models and lesser known parameters (internal structure of the package, package-to-PCB solder bondline).



(a) (b)

Figure 4.3: DUT ③: Half-bridge PCB (2 Mosfet :Cree CPM2-1200-0080A): (a) Classic setup discrete PCB, (b)

Fig. 4.4 presents two embedded variants of DUT ③ which include 2 embedded SiC MOSFET dies (CPM2-1200-0080A):

1. DUT ④ (Fig. 4.4a): Classic setup of the power Dies, where both MOSFETs chips have the same orientation, their drain pad facing the bottom of the PCB

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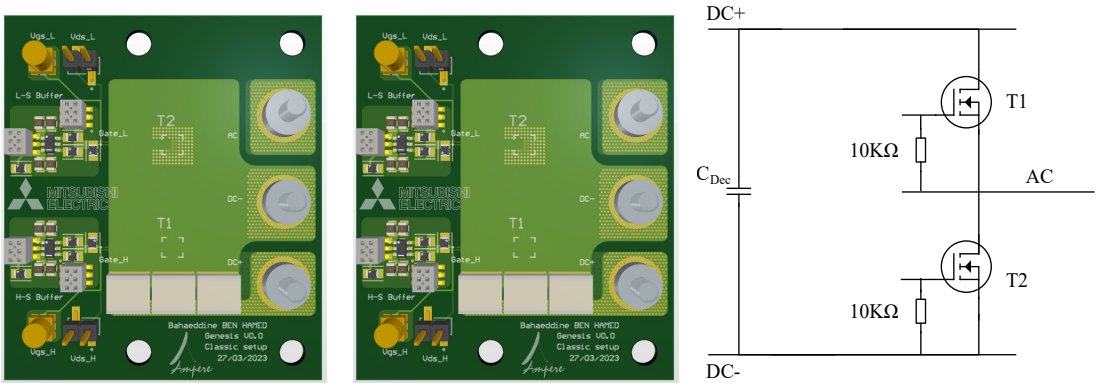

(a) DUT ④ (b) DUT ⑤ (c)

Figure 4.4: Half-bridge PCB with 2 embedded MOSFETs (Cree CPM2-1200-0080A): (a) Classic setup, (b) Flip-chip setup and (c) electrical circuit.

2. DUT ⑤ (Fig. 4.4b): one of the MOSFETs chips is "flipped", with its drain facing the top of the PCB. This is used to demonstrate the effect of chip orientation on layout parasitics and thermal resistance.

2 Validation of the Electrical Modeling Approach

As indicated above, electrical validation is based on two sets of measurements/simulations

1. Impedance characterization, to compare the predicted and measured layout parasitics

2. Double pulse test to compare the voltage switching waveforms.

2.1 Impedance Characterization

The layout model of DUT ② is generated automatically, following the steps outlined in Chapter 3.1, without any manual intervention. The data pre-processing and the preparation of the 3D model take only a few seconds, while the majority of the computation time is spent on the calculations performed by Q3D Extractor.

The impedance of the PCB's power loop is measured using a Keysight impedance analyzer E4990 and a Keysight impedance probe kit designed for in-circuit measurements. Since the embedded chips cannot be removed during the impedance measurement, the oscillator amplitude is set to a low level of 10 millivolts. This helps

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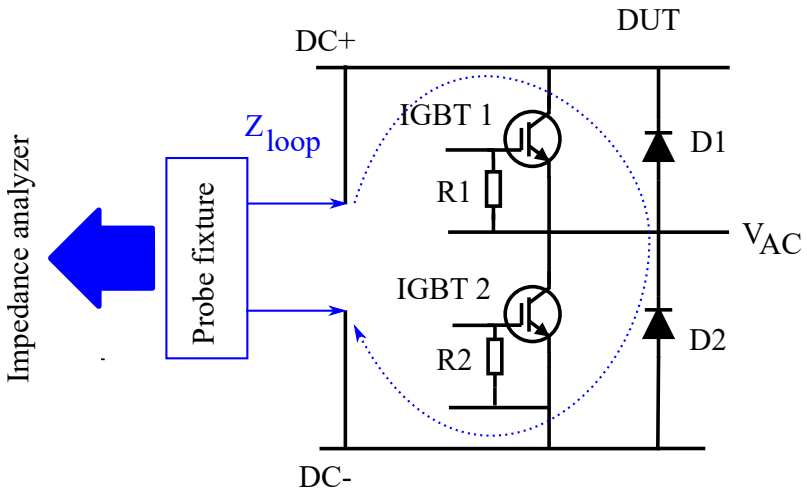

Figure 4.5: Circuit diagram for the impedance measurement of the power loop.

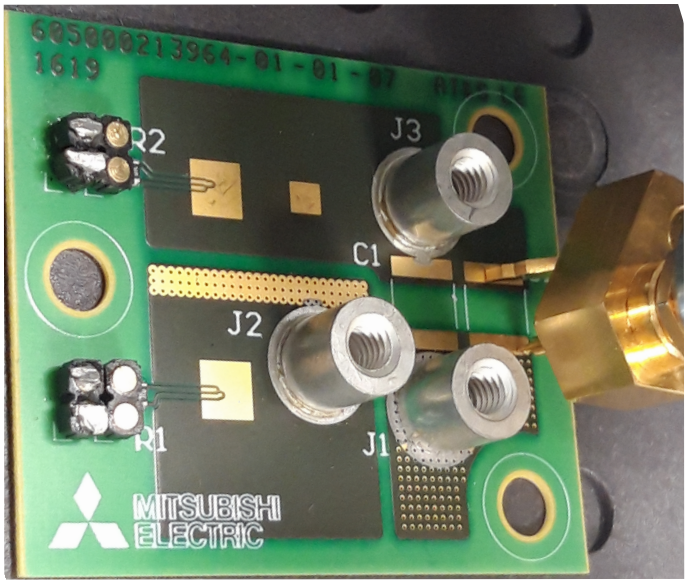

Figure 4.6: Close-up on the PCB under test (Dimensions: 35mm *45mm) and the tip of the Keysight 42941A probe placed across the decoupling capacitor footprint to measure the power loop impedance (decoupling capacitors not mounted).

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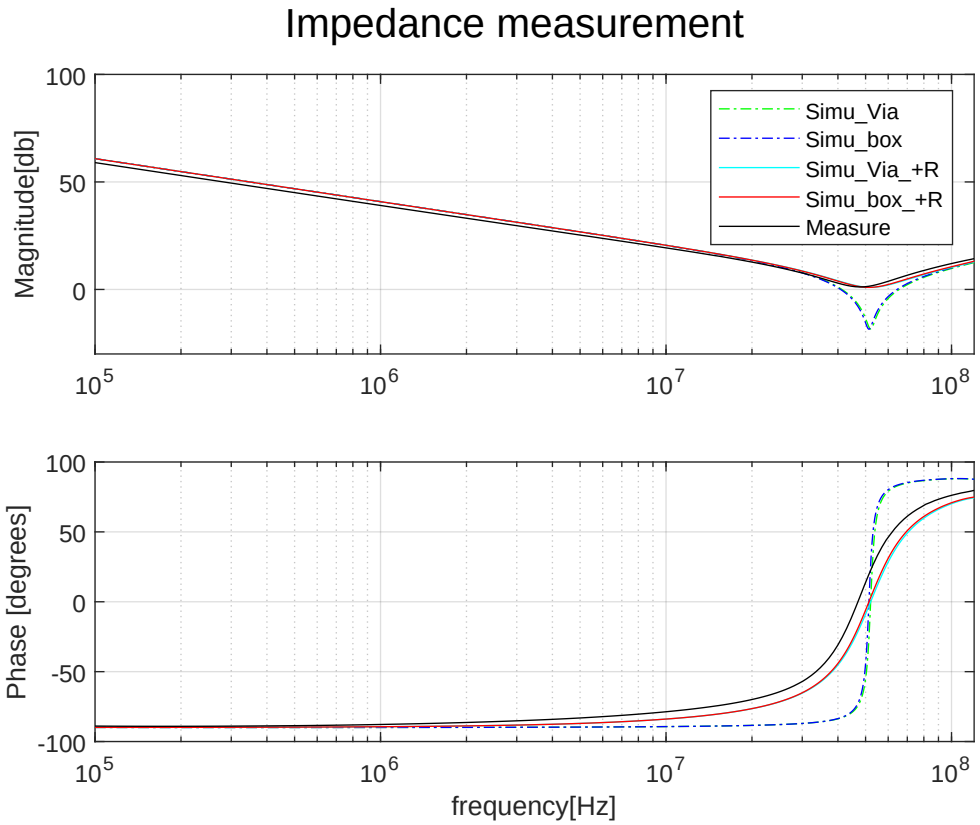

Figure 4.7: Experimental and simulated bode plot of the power loop impedance

prevent any non-linearities in the semiconductor chips from affecting the impedance readings. The frequency sweep is conducted within a range of 100 kHz to 120 MHz. Compensation is performed as specified in the user manual, including phase, open, and short compensations for the probe adapter and open and short compensations for the probe tip. The embedded IGBTs are left unconnected (i.e. no gate driver board is used), with pull-down gate resistors ensuring that their gate-to-emitter voltage is maintained at zero. No decoupling capacitors are installed on the PCB, and the impedance is measured across the footprint where these capacitors would typically be positioned (see Figs. 4.5 and 4.6).

The experiment is simultaneously reproduced through simulation using the Spice schematic created by the previously described workflow. In this simulation, the decoupling capacitors are removed and replaced with a 10 mV AC source. An AC simulation is then conducted over the same frequency range as used in the experimental setup. Two configurations are simulated: one without via simplification and another with "box" simplification.

The results are presented in Fig. 4.7. The simulation results ("Simu_via" and "Simu_box") are in good agreement with the experimental data, except at the resonance point, which occurs around 50 MHz. This discrepancy can be resolved

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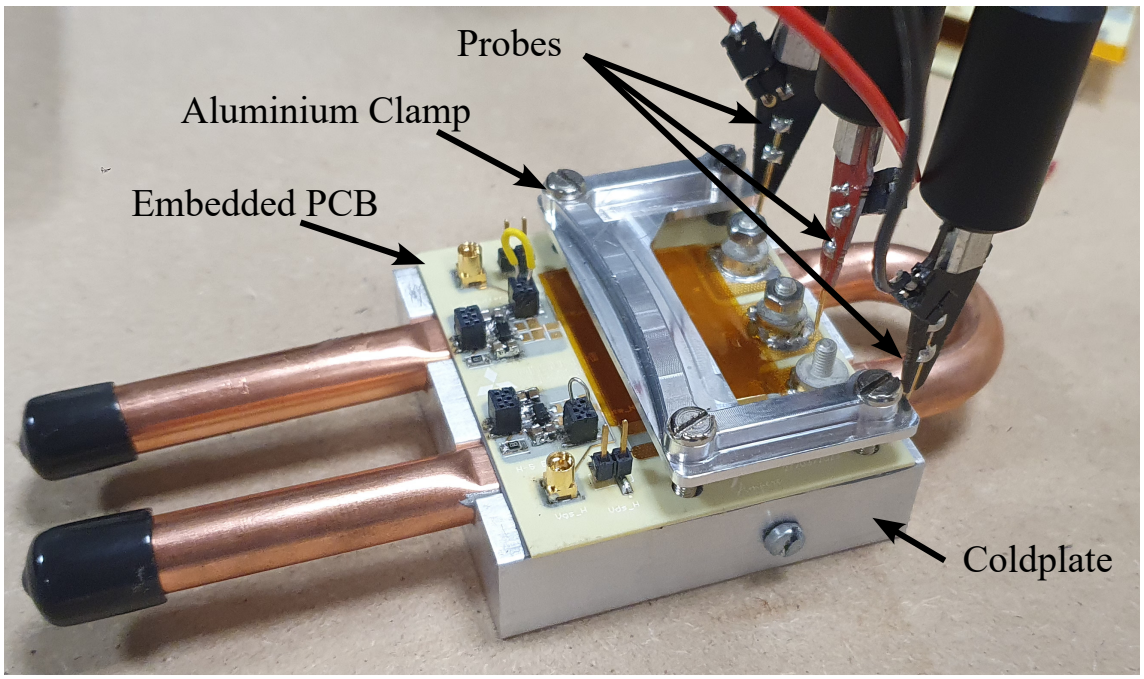

Figure 4.8: Electrical characterisation setup using the curve tracer B1505A (equipped with B1513C HVSMU module) on DUT ④

by adding a 1 Ω resistor in series with the voltage source in the simulation files ("Simu_via +R" and "Simu_box +R"). The additional resistance is likely related to the probe and PCB contact, as changing the probe position resulted in variations of 0.2 to 0.3 Ω at the resonance point. On the other hand, adjusting the frequency value used for calculating the layout parasitics in Q3D had no noticeable impact, even for values as high as 500 MHz.

Furthermore, a 4-point static characterization of the embedded IGBTs demonstrated low DC resistance (as low as a few tens of mΩ, including the dynamic resistance of the IGBTs). This indicates that the high resistance observed at the resonance point cannot be attributed to defects in the PCB's interconnects.

In conclusion, there is no significant difference between the simplified and non-simplified models. The simulated results show strong agreement with the measurements, for example, the simulated L_{loop} is 6.66 nH, while the experimental value is found to be 6.89 nH (determined by the impedance characterization shown in Fig. 4.5).

2.2 Parasitic capacitance comparison

The parasitic capacitance of the embedded half-bridge PCB (DUTs ④ and ⑤) was measured and compared with the results of the automatic model generation

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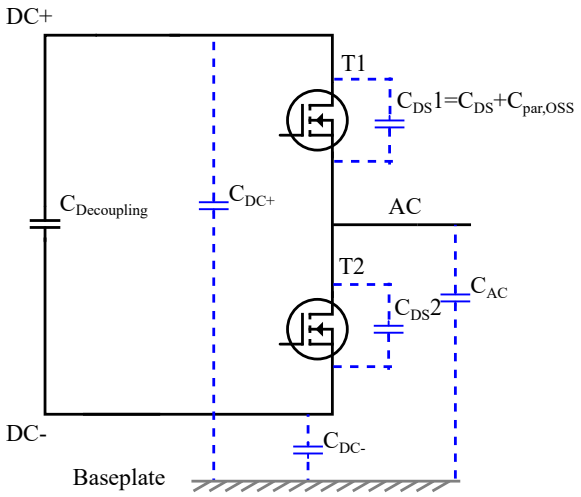

Figure 4.9: Equivalent parasitic circuit for Half bridge structure.

	Classic configuration (DUT ④)			Flipped configuration (DUT ⑤)		
	Measurement	Simulation	Error	Measurement	Simulation	Error
C_{Dc+}	69 pF	75 pF	8.7 %	93 pF	101 pF	8.6 %
C_{Dc-}	81.4 pF	81 pF	0.5 %	106 pF	105 pF	1 %
C_{AC}	60 pF	56 pF	6.6 %	4.3 pF	5.6 pF	30 %
C_{par,OSS_HS}	25.5 pF	27 pF	6 %	26.5 pF	29 pF	9 %
C_{par,OSS_LS}	139 pF	131 pF	6 %	150 pF	151 pF	0.3 %

Table 4.2: Capacitance Measurement for Embedded Half-Bridge PCB Validation: Cases of DUTs ④ and ⑤.

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workflow. The capacitance measurements were performed using the Curve Tracer B1505A, which is equipped with a B1513C HVSMU module, and connected with probes as illustrated in Fig. 4.8. This measurement setup provides a reliable method for characterizing the parasitic capacitances of embedded PCB structures.

Tab. 4.2 presents the capacitance values for both configurations of the half-bridge circuit (Fig. 4.9): the classic configuration ④ and the flipped configuration ⑤. Note that the differences between DUTs ④ and ⑤ will be discussed in the next chapter. Here, they are just considered as two different cases for validation purposes.In both setups, several important capacitances were measured, including the differential capacitances (C_{Dc+} and C_{Dc-}), the AC capacitance (C_{AC}), and the parasitic capacitances on the high-side and low-side, referred to as C_{par,OSS_HS} and C_{par,OSS_LS}, respectively. These measured capacitances are then compared to the corresponding simulation results.

The results for the differential capacitances, C_{Dc+} and C_{Dc-}, show errors of 8.7 % and 0.5 % for the classic configuration and 8.6 % and 1 % for the flipped configuration, respectively. The AC capacitance (C_{AC}) exhibits a larger deviation, with a 6.6 % error for the classic configuration and a 30 % error for the flipped

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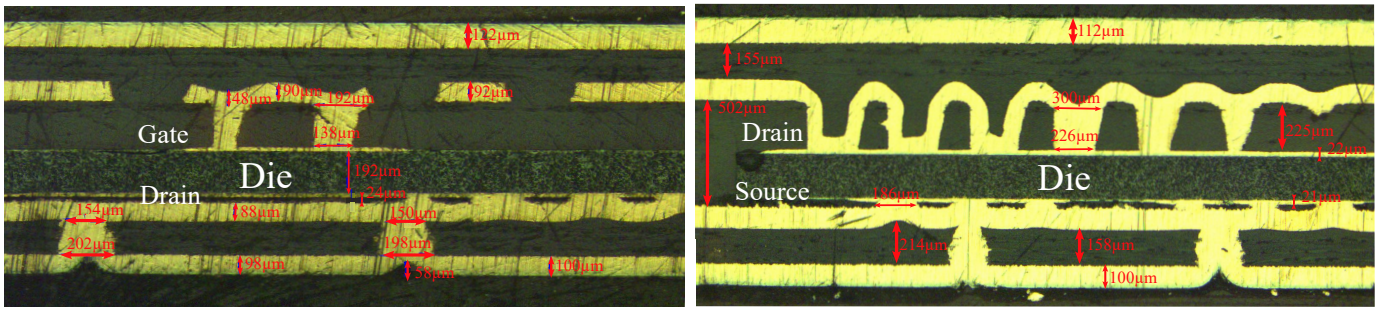

(a) (b)

Figure 4.10: Micro-Sectional View of Embedded Half-Bridge PCBs: (a) Classic Power Chip Configuration (④, with MOSFET Drain Facing coldplate); (b) Flip-Chip Configuration (⑤, with MOSFET Source and Gate Faces Towards coldplate).

configuration.

The high-side parasitic capacitance (C_{par,OSS_HS}) shows a relatively consistent match, with a 6 % error for the classic configuration and 9 % for the flipped configuration. The low-side parasitic capacitance (C_{par,OSS_LS}) has a 6 % error for the classic configuration and a near-perfect match (0.3 % error) for the flipped configuration.

The measurements and simulations demonstrate relatively good agreement, with the most noticeable discrepancies found in the AC capacitance. These errors can mainly be attributed to small differences that exist between the design of the PCB and its fabricated prototype. A cross-section analysis of the PCBs (Fig. 4.10) underscores this point.

The discrepancies observed between the measurement and simulation results can be linked to several key factors related to the fabrication of the PCB. The original layout specified a copper layer width of 105 µm, but the fabricated PCBs showed variations in copper widths of 112 µm, 92 µm, 88 µm, and 100 µm, resulting in discrepancies ranging from 6% to 19.3%.

Furthermore, the manufacturer uses prepreg sheets with a nominal thickness of 55 µm, leading to a targeted dielectric layer width of 165 µm (calculated as 55 µm multiplied by 3 layers). However, the actual fabricated PCB exhibited a dielectric layer width of 155 µm, reflecting a variation of approximately 6.45%.

The thickness of the embedded PCB core further compounds these variations. The desired configuration, which includes the embedded die and five layers of prepreg, was designed to total 465 µm (190 µm for the die plus 5 times 55 µm for the prepreg). In practice, the fabricated PCB core measured 502 µm, introducing a variation of around 7.3%.

Additionally, the placement of microvias alters the effective dielectric width.

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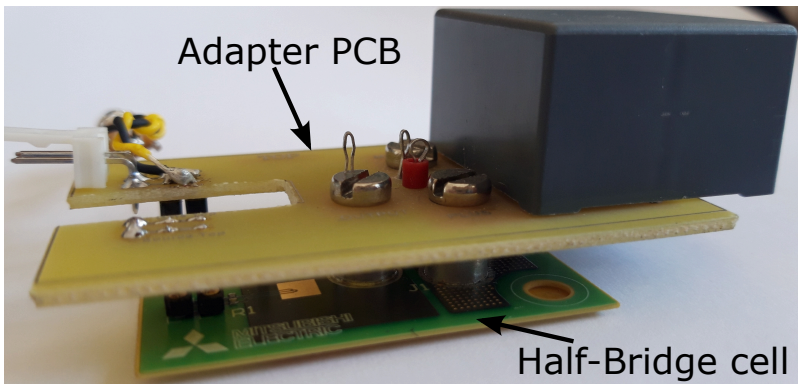

Figure 4.11: The half-bridge cell (with two IGBT and two diodes embedded in the PCB and two surface-mount decoupling capacitors). An adapter board is mounted on top for easier connection and to provide more decoupling capacitance.

While the layout design treats these areas as perfect planes, actual measurements revealed that the dielectric width in these regions had expanded to 214 µm due to the changing geometry of copper. As parasitic capacitance is directly related to dielectric thickness, the modeling accuracy aligns closely with the variability in dielectric thickness, which is what we observe here. These factors collectively contribute to the discrepancies between the simulation predictions and the actual measurements.

Moreover, the electrical parameters of the thermal interface material (TIM) used here (ref: TG-A1660-150-150-0.5) are not provided by the manufacturer's datasheet. As a result, these parameters were approximated from similar materials. This lack of precise data could also affect the variations in the capacitance values, specifically Cac, Cdc+, and Cdc-, leading to further differences between the simulations and the obtained measurements.

2.3 Double pulse test

In this section, we perform a double pulse test (DPT) on a half-bridge embedded PCB (DUT ②) and compare the results to the waveforms simulated using the automatically generated electrical virtual prototype model. DPT produces a representative set of switching waveforms without significant heat dissipation, allowing for decoupling thermal and electrical effects.

Figs. 4.11 and 4.12 illustrate the PCB setup, including the embedded half-bridge configuration and the decoupling capacitor adapter board, specifically designed to minimize noise and stabilize the power supply during operation.

The circuit setup for the DPT is shown in Fig. 4.12, which provides a detailed layout of the components involved in the testing process. The setup consists of the

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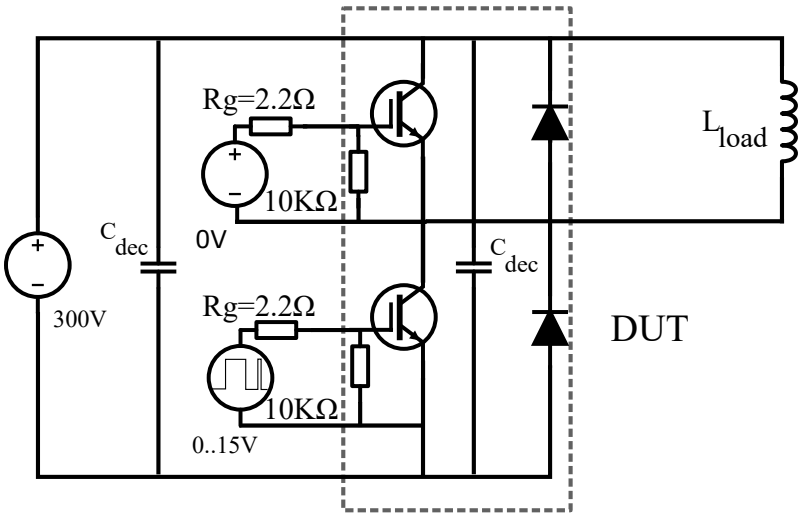

Figure 4.12: Double pulse test circuit. The dashed line corresponds to DUT ②.

half-bridge module and the necessary measurement equipment, including passive probes (TPP0500B voltage probe & TCP0030A current probe, Tektronix) and a scope with a bandwidth of 350 MHz (DPO4034B, Tektronix). Attention was paid to the grounding and signal integrity to ensure the reliability of the test results.

Results from the DPT are presented in Fig. 4.13, where the load current (in red) and the V_{ds} of the low-side IGBT are depicted. The measured waveforms are juxtaposed with the predicted waveforms obtained from the electrical virtual prototype model. A comparison reveals a good match between the experimental results and the simulated waveforms. The differences that can be observed for the high frequency ringing at turn-off ($t = 25.3\,\mu s$) are attributed to limitations of the Spice model of the semiconductor devices. Note that because some signals cannot be measured for embedded designs (collector and anode current, in particular), and because stray inductances are very limited with this kind of design, the amount of data that can be collected from DPT is limited. Calorimetric measurements, presented later in the chapter, are more informative.

3 Thermal modeling method Validation

3.1 Validation case 1: Single-chip PCB

DUT ① (Fig. 4.14) consists in an embedded single SiC MOSFET (Cree CMP2-1200-0080B chip) connected to the top and bottom copper layers using µVias. This internal structure is depicted in Fig. 4.15a.

With only one chip, a single transient thermal simulation is required, and no cross-coupling effect can be considered. The experimental cooling conditions (TIM

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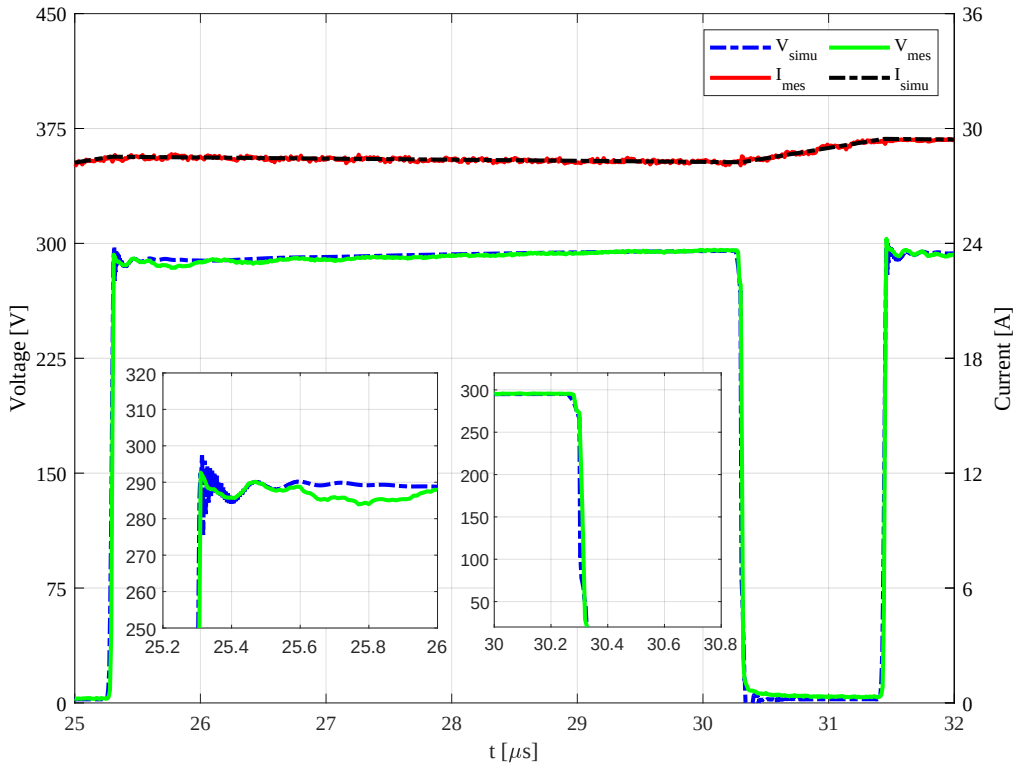
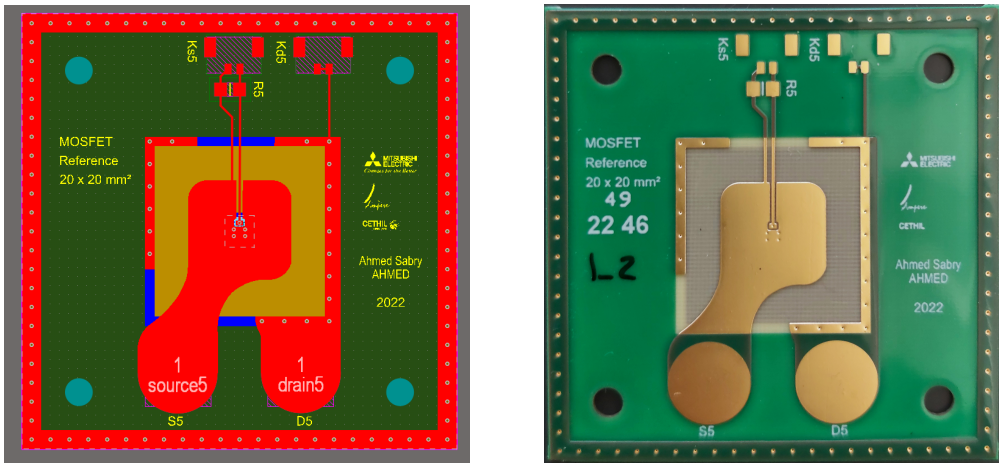


Figure 4.13: Example of double pulse waveform



(a) (b)

Figure 4.14: Single chip (Cree CPM2-1200-0080A) prototype (DUT ①): layout (a) and photograph (b).

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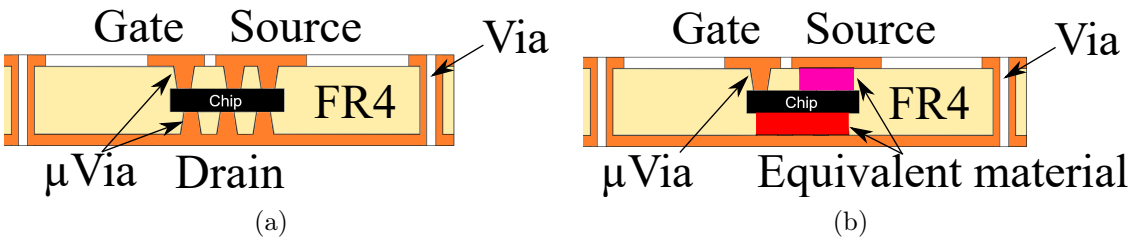

Figure 4.15: The internal structure of DUT ① (a) and the simplified via structure (b) considered for "box" simulations(not to scale / illustrative dimensions).

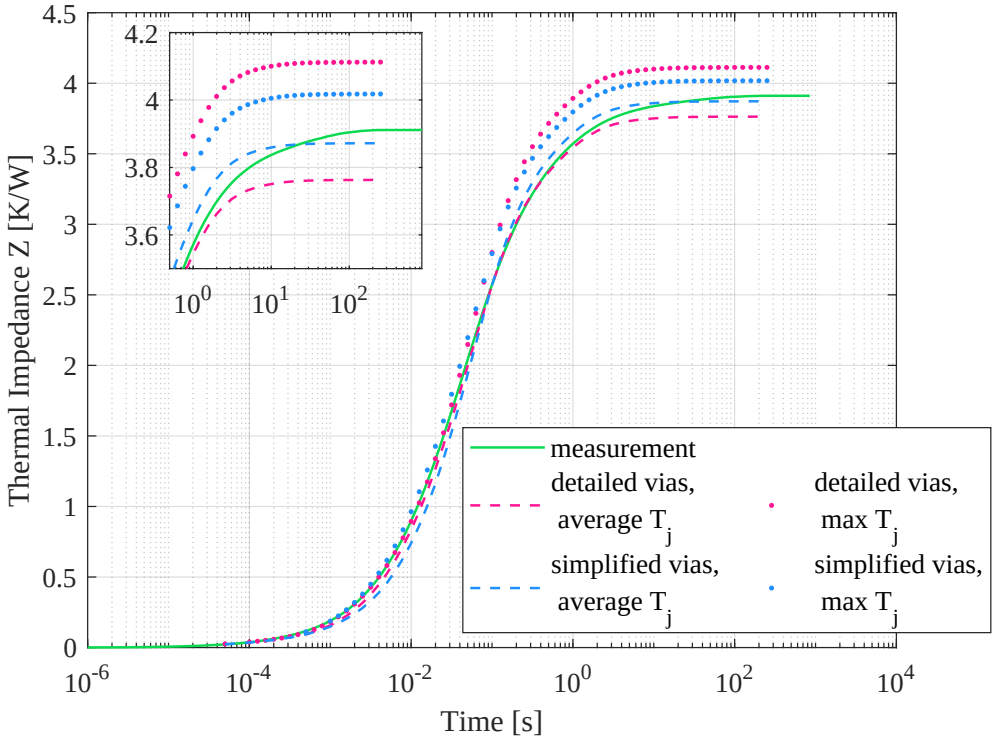

Figure 4.16: Thermal impedance comparison of the measurements and generated models

and water-cooled cold plate) are simulated by setting a bottom boundary condition for the PCB with H_{coeff} =6000 W K^{-1} m^{-2}(This value corresponds to the cold plate used during thermal resistance measurements and accounts for the effective PCB surface area). The ambient temperature (T_{amb}) is set to 20 °C.

In this example, two geometries are considered: the full geometry and a simplified version that uses an equivalent block instead of Vias groups (Fig. 4.15). In addition, two definitions are considered for the junction temperature in the simulations: either the average temperature at the top surface of the chip or the maximum temperature of the chip. In the experiments, the junction temperature is considered to be the value estimated using a Temperature-Sensitive Electrical Parameter (TSEP) of the transistor. The measurement technique and the experimental protocol are described in [101].

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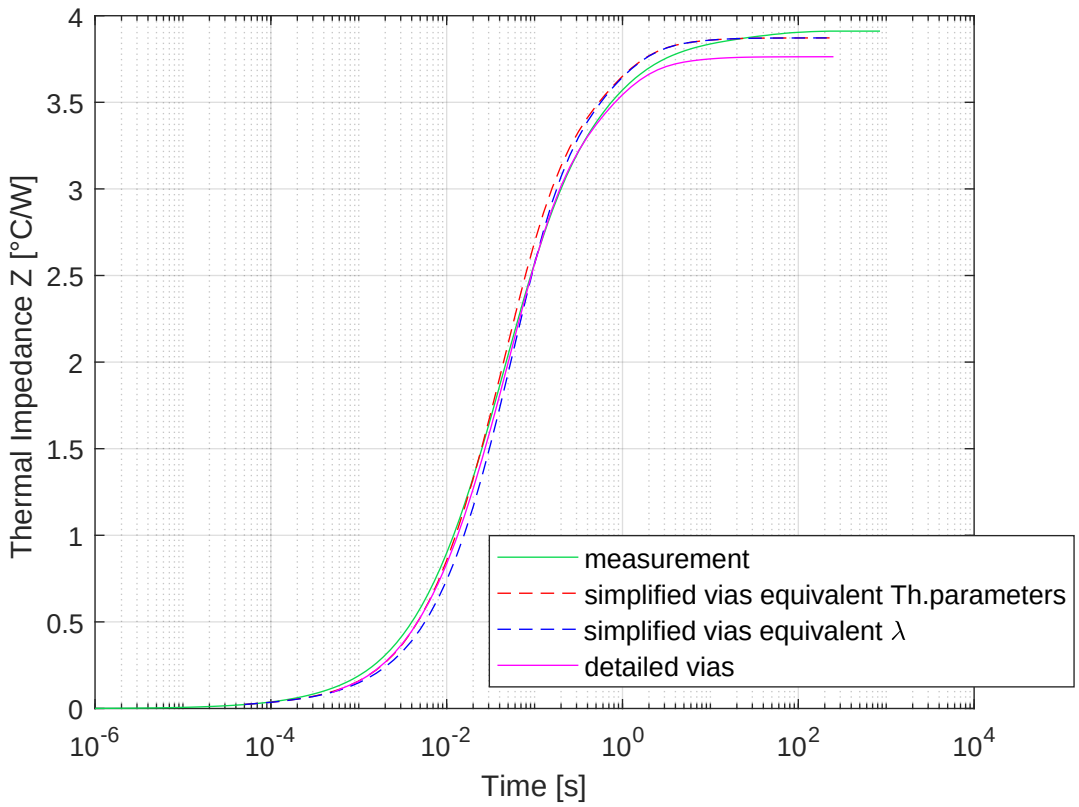

Figure 4.17: Thermal impedance of the models: replacing the vias with a block with all equivalent thermal parameters(λ , C_p, ρ); with only equivalent conductivity (λ, C_p and ρ being those of copper); detailed Via model and measurement.

Fig. 4.16 shows the thermal impedance measured on the prototype using a thermal impedance analyzer (Analysistech Phase 12B, plain line) and the 4 simulated thermal impedances (full geometry or simplified Vias; maximum or average chip temperature).

The thermal impedance computed using the average temperature value (dashed lines) tend to be lower, which is to be expected: average temperatures are lower than the maximum temperature, hence the lower Z_{th} values according to the thermal impedance equation (see eq. 3.8 in section 2.2.3 of chapter 3.1). Also, considering a uniform equivalent block (blue lines) results in a smaller difference between impedance curves calculated using average and maximum T_J values than between curves calculated for the discrete µVias (red lines). This could also be expected: the equivalent blocks provide a uniform cooling over the die surface, while µVias act like discrete heat sinks, resulting in more temperature variation over the chip surface (and more difference between the maximum and average values).

A noticeable difference between simulated and measured characteristics is the time to reach a steady state: in simulation, a steady state is reached at around 30 s, while the measurement reaches a steady state after $\approx$ 200 s. This is particularly

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visible in the inset from Fig. 4.16. This difference is a consequence of the boundary conditions used in simulation: the cold plate is represented using a simple heat-exchange coefficient, which adds no thermal mass to the structure. In reality, heat diffuses through the cold plate before reaching the cooling fluid, so the thermal dynamics of the plate add to those of the PCB, resulting in a longer time to reach a steady state. A more sophisticated modelling of the interface (for Example including part of the cold plate in the model) would be required to achieve more realistic dynamics.

One can also notice a smaller difference between simulations in Fig. 4.16, at around $t = 10\,\text{ms}$: the simplified models tend to predict a lower thermal resistance than detailed models (and simulation). This can be explained by the fact that for these models, only the thermal conductivity of the equivalent blocks are adjusted according to (3.1) (presented in chapter). In particular, the specific heat (C_p) and density (ρ) are considered to be those of copper. Adjusting both parameters (using a simple volume ratio between epoxy and copper in the via region) improves the fidelity of the simplified model, as can be seen in Fig. 4.17.

At this stage, however, the simulation using the average temperature and simplified geometry can be considered as satisfyingly close to the measurement results. This is the configuration which is used in the next validation case.

3.2 Validation case 2: Multi-chip PCB

3.2.1 Simulation

DUT ② (Fig. 4.18) is a half-bridge circuit consisting of 4 embedded power chips (2 IGBTs and 2 diodes). The corresponding 3D model is built automatically in Ansys Icepak thanks to the the toolkit presented above. The cut view presented in Fig. 4.18c shows the simplified Via models and a 0.2 mm TIM layer. A heat-exchange coefficient H_{coeff} of $6000\,\text{W}\,\text{K}^{-1}\,\text{m}^{-2}$ is applied to the bottom surface of the TIM layer.

Because the model contains 4 chips, 4 thermal transient simulations are run successively, with only one chip dissipating heat each time. As an example, Fig. 4.19a show the temperature profile (average T_J) of the 4 chips simulated using Icepak when IGBT T_1 is active and the other power sources are off. In this case, T_1 logically exhibits the largest temperature increase. D_1, which is attached to the same copper tracks as T_1, also experiences a significant temperature rise, despite dissipating no power. T_2 and D_2, which are further away, show almost no temperature increase

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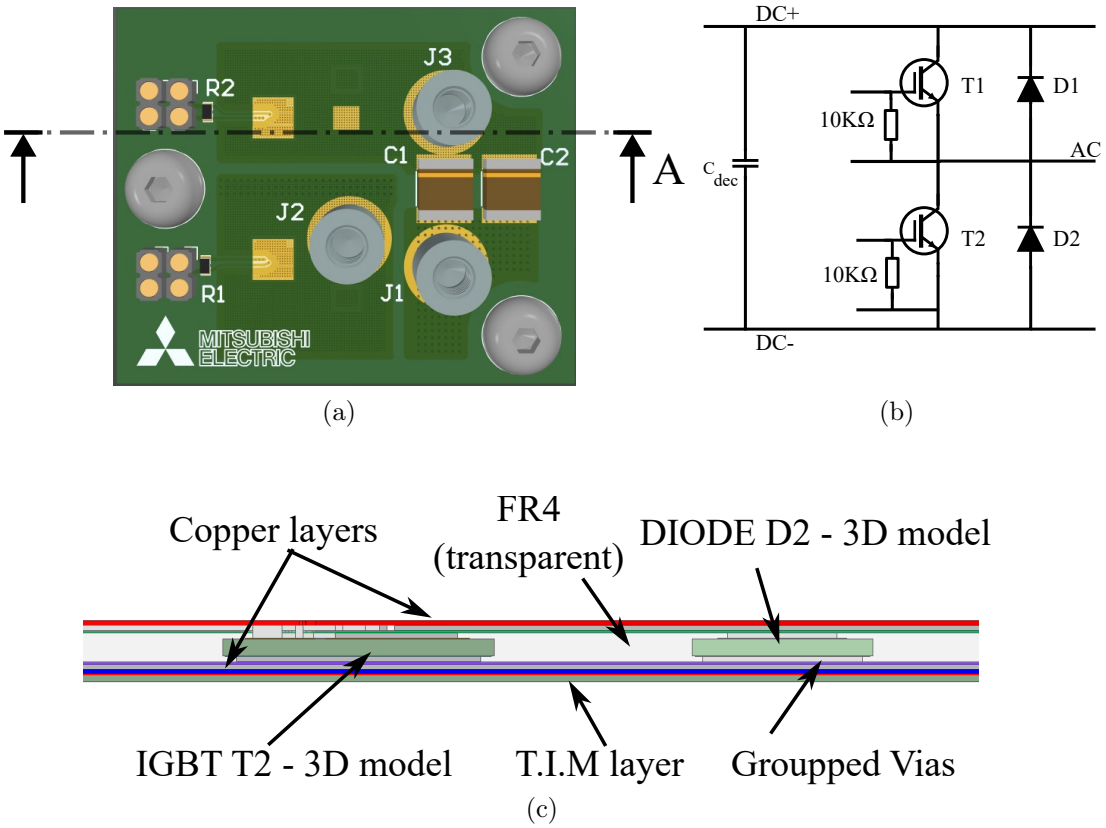

Figure 4.18: DUT ② (Half-bridge structure with 2 IGBTs & 2 diodes): (a) upper view of the PCB, (b) circuit diagram and (c) Section view (AA) of the corresponding 3D model in Icepak.

(i.e. negligible thermal coupling).

The simulation of this simplified 3D model takes 104 minutes on a desktop PC. Without Via simplification, the same PCB takes more than 30 hours.

The resulting TCEM model is shown in Fig. 4.19b. For each junction temperature (T_{T_1}, T_{D_1}, T_{T_2},T_{D_2}), 4 foster models (Z_{ij}) are connected in series. Each model is supplied with a current source which represents the power dissipated in the corresponding components. Tab. 4.3 gives the parameters values for each of the Z_{ij} elements in Fig. 4.19b. The order of each network (1, 2, 3 or 4 RC cells) is consistent

j\i	1	2	3	4
1	$R1 = 0.079$, $C1 = 0.004$ $R2 = 0.288$, $C2 = 0.0371$ $R3 = 1.143$, $C3 = 0.0724$ $R4 = 0.779$, $C4 = 0.724$	$R1 = 0.464$, $C1 = 1.749$	$R1 = 0.05$, $C1 = 26.23$ $R2 = 2.44e^{-6}$, $C2 = 3.13e^{6}$	$R1 = 0.02$, $C1 = 96.24$ $R2 = 5.29e^{-4}$, $C2 = 6.63e^{4}$
2	$R1 = 0.437$, $C1 = 1.959$	$R1 = 0.48$, $C1 = 0.003$ $R2 = 1.744$, $C2 = 0.019$ $R3 = 1.286$, $C3 = 0.358$	$R1 = 0.024$, $C1 = 81.091$ $R2 = 2.22e^{-14}$, $C2 = 8.986$	$R1 = 0.014$, $C1 = 139.3$ $R2 = 5.1e^{-4}$, $C2 = 3.9e^{4}$
3	$R1 = 0.054$, $C1 = 23.71$ $R2 = 8.977e^{-7}$, $C2 = 3.59e^{3}$	$R1 = 0.024$, $C1 = 77.25$ $R2 = 2.221e^{-14}$, $C2 = 1.12e^{15}$	$R1 = 0.179$, $C1 = 0.010$ $R2 = 1.158$, $C2 = 0.049$ $R3 = 1.091$, $C3 = 0.509$	$R1 = 0.589$, $C1 = 1.552$ $R2 = 0.004$, $C2 = 232.05$
4	$R1 = 0.021$, $C1 = 91.93$ $R2 = 8.1e^{-4}$, $C2 = 4.33e^{4}$	$R1 = 0.015$, $C1 = 152.1$	$R1 = 0.587$, $C1 = 1.6$ $R2 = 2.06e^{-6}$, $C2 = 6.32e^{6}$	$R1 = 0.24$, $C1 = 1.35$ $R2 = 0.758$, $C2 = 0.012$ $R3 = 1.487$, $C3 = 0.043$ $R4 = 1.35$, $C4 = 0.451$

Table 4.3: Thermal impedance parameters $Z_{i=1..4,j=1..4}$ of the model TECM presented in Fig4.19b , $[R] =^{\circ} C/W$, $[C] = J/^{\circ}C$

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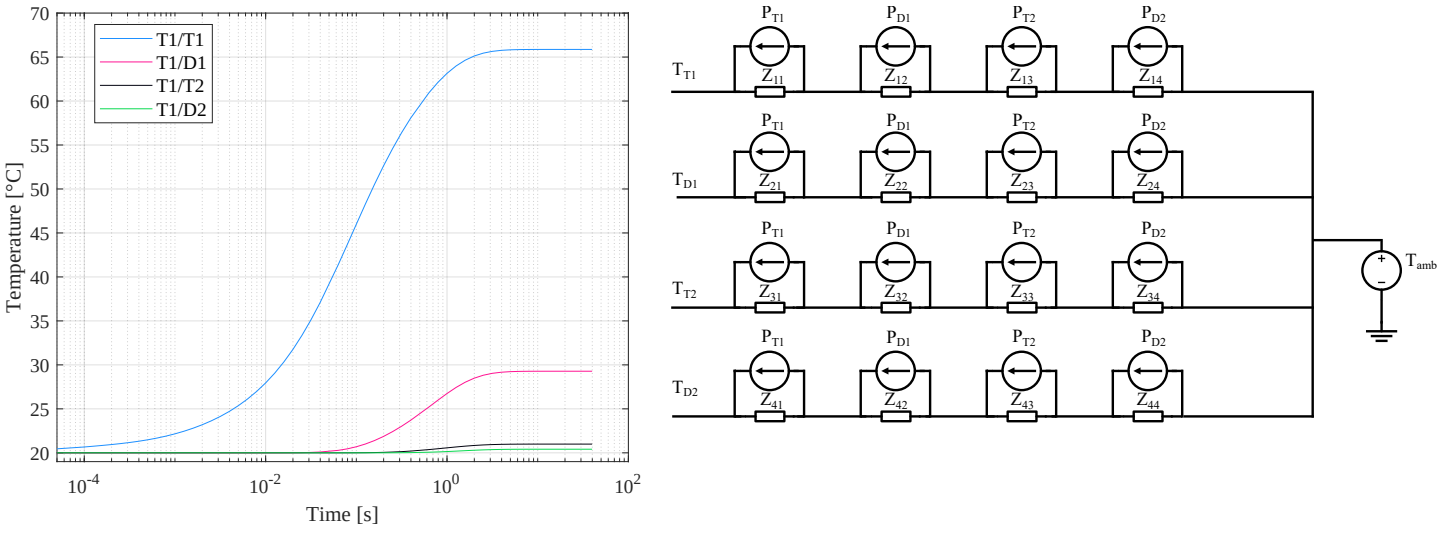

Figure 4.19: (a) Heat curve results from the conduction simulation performed by Icepak on the 3D model generated by the toolkit. In this sequence, IGBT T1 is the active heat source, with a power output of $Power_{T1} = 20W$ and an ambient temperature of $T_{amb} = 20°C$. (b) TECM circuit model created from the full simulation set (4).

with the intensity of the coupling: self thermal impedance have the highest order, strong couplings (e.g. between T_1 and D_1) have an order of 2, and weak couplings (e.g. between T_2 and D_2) are represented using a single RC cell. Please note that the order of each network is a result of the identification procedure and was not set beforehand.

For the measurement of the thermal impedance of the half-bridge PCB, the clamping system depicted in Fig. 4.20 is used: a gas cylinder applies force on the PCB through some pressure-distributing spreader; a TIM layer is placed between the sample and a cold plate. The thermal impedance of each IGBT and diode are measured with the thermal analyser using a TSEP (V_{CE} for the IGBT and V_F for the diode, both measured under a 5 mA reading current), while power is dissipated successively in each device.

The results obtained when dissipating power in T_1 or T_2 are presented in Fig. 4.21 (only the self impedances and the T_1/D_1 and T_2/D_2 couplings are shown). It can be seen that there is a good agreement between simulation and measurement when power is dissipated in T_2 (red and green curves). However, when power is dissipated in T_1 (blue and magenta curves), this is no longer the case, and the error in steady state can exceed 50 % for the cross-coupling thermal impedance between T_2 and D_2.The reason for this discrepancy is attributed to the poor pressure distribution, which affects contact quality and increases thermal resistance.

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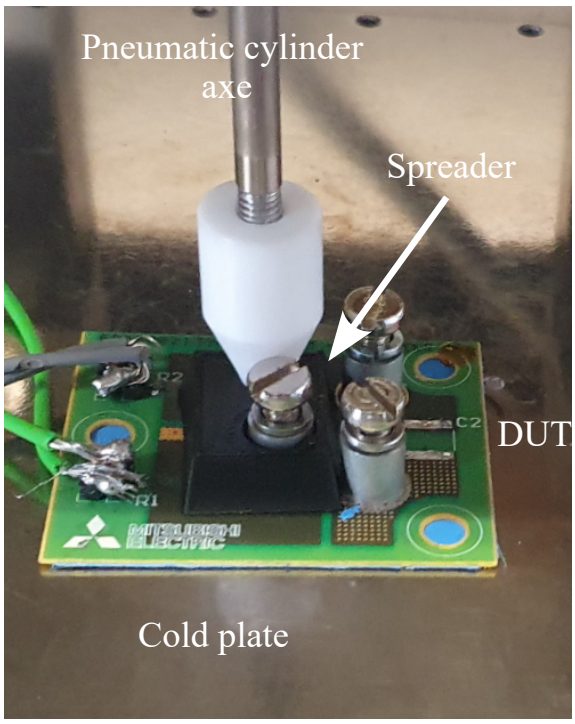

Figure 4.20: Close-up on the clamping system used to press the PCB against the cold plate: a pneumatic cylinder applies a 110 N force to the PCB through a plastic cap (white) and a 3D-printed spreader (black), used to balance the mechanical pressure over the active parts of the PCB.

3.3 Validation case 3: Multi-chip PCB

In this validation case, we focus on the impedance measurement of the two half-bridge embedded PCB configurations (DUTs ④ and ⑤). The measurement setup is illustrated in Fig. 4.22. In this setup, the PCB is securely mounted on a commercially available aluminum cold plate (reference: ATS-TCP-1000), whose dimensions correspond to those of the DUTs.

The reference temperature is monitored at the inlet of the cold plate using a thermocouple, as outlined in the setup shown in Fig. 4.22. Manual valves and a flowmeter (not shown) are used to adjust the flow rate of the cooling medium (water), allowing for precise management of the thermal conditions during testing.

A notable improvement in this case study is the introduction of a custom aluminum clamp designed specifically for securing the PCB to the cold plate. This custom clamp ensures optimal pressure on the power chips, thereby enhancing the thermal contact and improving the reliability of impedance measurements. The four screws of the clamp are tightened using controlled torque.

Comparisons between measurement and experiment are proposed for DUT ④ and ⑤ in Figs. 4.23 and 4.24, respectively. Two screw tightening torque values are considered experimentally (17.5 and 25 N cm), as we have little control on the corresponding pressure on the PCB (which affects the thermal conductivity of the

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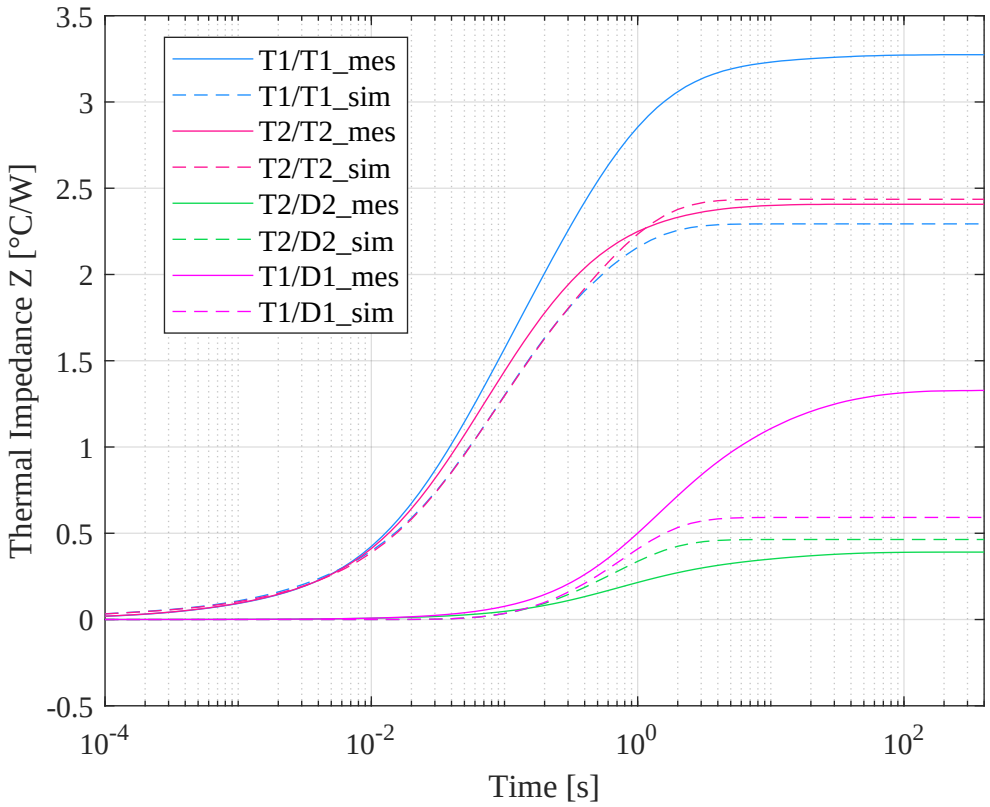

Figure 4.21: Thermal impedance comparison between the simulated results and the measured values. Two sequences are presented: when T_1 is active (T2,D1,D2 : OFF) and T2 active (T1,D1,D2 : OFF). T1/T1 is the proper heating impedance and T1/D1 is the coupling impedance of D1 when T1 is active

TIM). The results show a very good level of agreement with the simulation.

3.4 Discussion on thermal validation

The main hypothesis for this discrepancy between simulation and experiment, when power is dissipated in T_1, is believed to be due to poor control of the pressure on the sample: while special care has been taken to maximise pressure uniformity (Fig. 4.20), this is hampered by the geometry of the board, with one of the screw connectors placed directly on top of D_1. This geometry also forces the pneumatic cylinder to be placed closer to T_2 and D_2 than to T_1. Furthermore, the PCB is thin, making it flexible. This shows that such PCB is very sensitive to the way it is mounted on its cooler. A better agreement is observed when using a rigid clamping mechanism with more controlled pressure distribution, such as in validation case 3.

A second source of inaccuracy is also related to the pressure: it is the thermal conductivity of the TIM. TIMs usually are soft materials, and their thermal conductivity depends on pressure. In our model, we only consider a constant thermal conductivity, based on the average value found in the material's datasheet.

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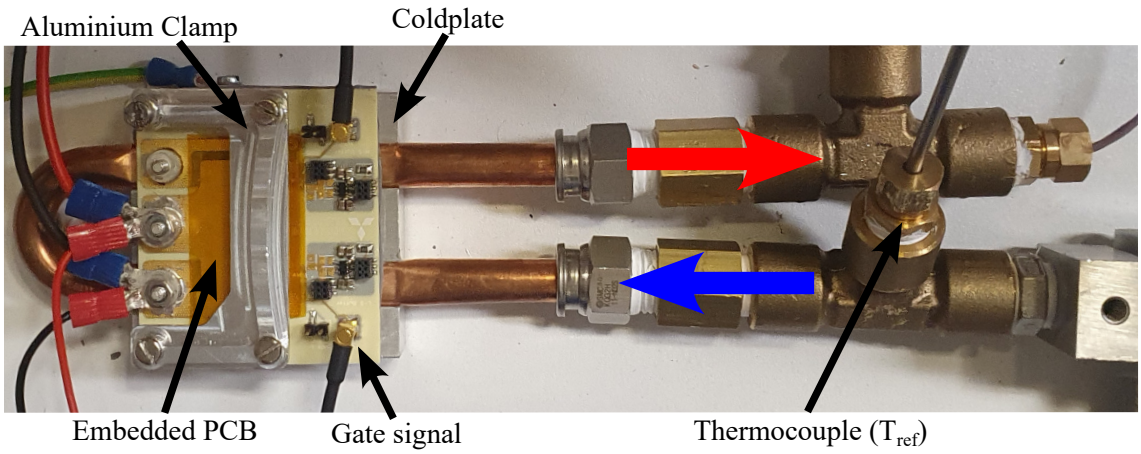

Figure 4.22: Thermal impedance measurements setup

Finally, the geometry of the µVias in the prototypes (Fig. 4.10, p. 133) and in the CAD description. Although they are considered to by cylindrical and full in the CAD, in reality they are conical and partially hollow. This means the actual quantity of copper available to carry heat away from the chip may be significantly lower than expected

Overall, it means that the variability in the thermal resistance of the prototypes is large. Therefore, thermal models cannot be expected to predict the actual thermal resistance with more than probably 10-20 % accuracy, unless all manufacturing parameters are very well controlled, and very good contact is achieved with the cooling system.

4 Validation of the Electro-thermal model

4.1 Buck circuit setup

A half-bridge structure with SiC chips is used here. Because of delays in the manufacturing of the PCB-embedded samples, this work is based on the variant that uses discrete MOSFETs (③). Fig. 4.25 shows the complete assembly of the converter on the cooling system. A dedicated busbar PCB, populated with ceramic and film capacitors, is used to connect the DC link with minimal stray inductance. While DUT ③ contains the output buffer of the gate drivers, an additional board is required to provide signal transfer and power supply isolation features. DUT ③ is mounted on the cold plate using a TIM using the clamp discussed in the previous section.

Fig 4.26 describes the way the DUT is connected. Fig. 4.27 presents the corresponding electrical circuit.

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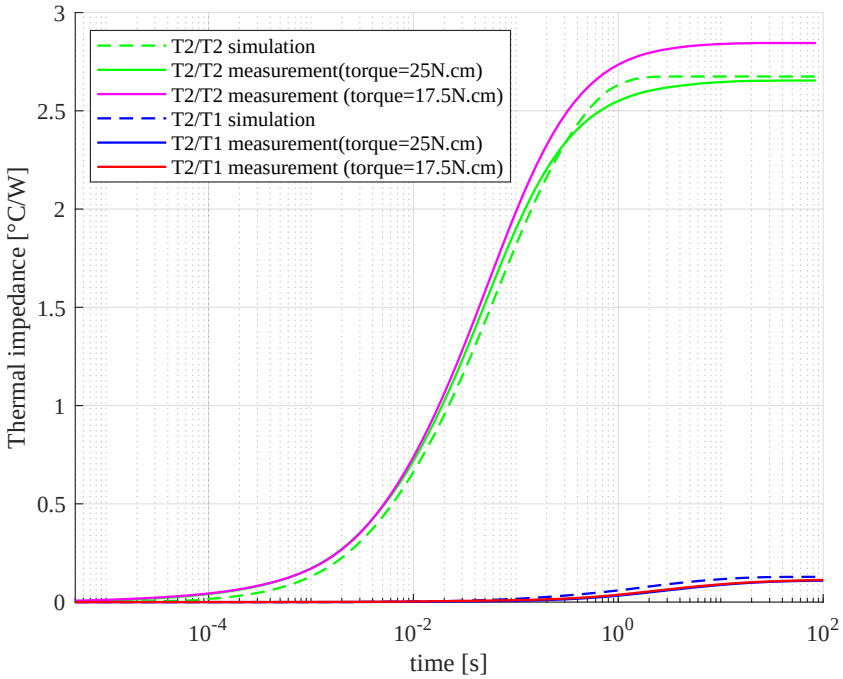

Figure 4.23: Thermal impedance comparison between the simulation and experiment for DUT ④. Two sequences are presented: when T_1 is active (T2,D1,D2 : OFF) and T2 active (T1,D1,D2 : OFF). T1/T1 is the self heating impedance and T1/D1 is the coupling impedance of D1 when T1 is active.

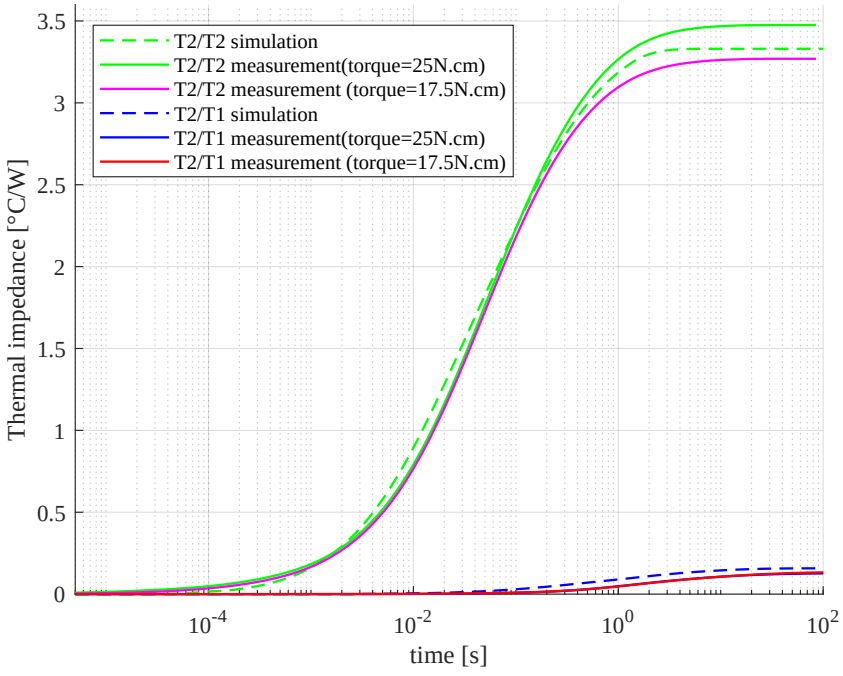

Figure 4.24: Thermal impedance comparison between the simulation and experiment for DUT ⑤. Two sequences are presented: when T_1 is active (T2,D1,D2 : OFF) and T2 active (T1,D1,D2 : OFF). T1/T1 is the proper heating impedance and T1/D1 is the coupling impedance of D1 when T1 is active.

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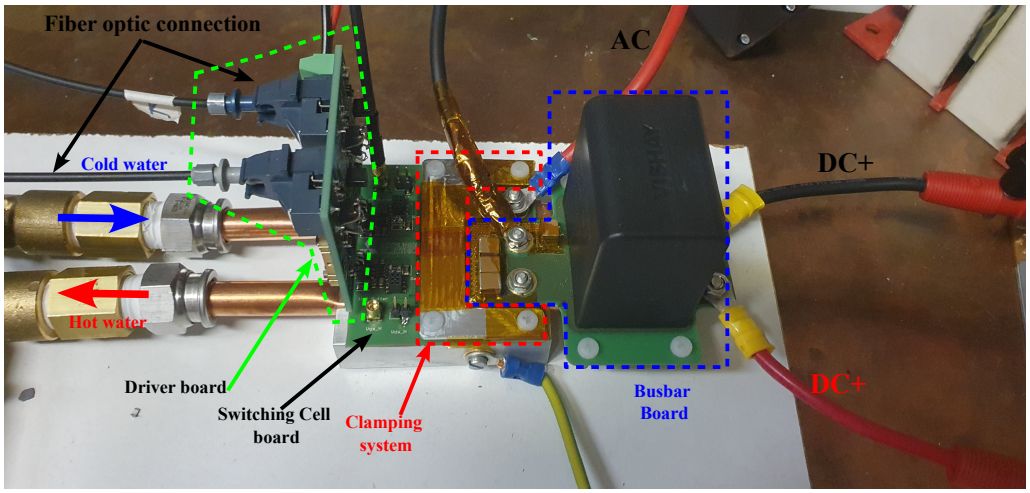

Figure 4.25: The buck PCB setup on the coldplate: Driver board, busbar board the switching cell board and the clamping system for better pressure spreading

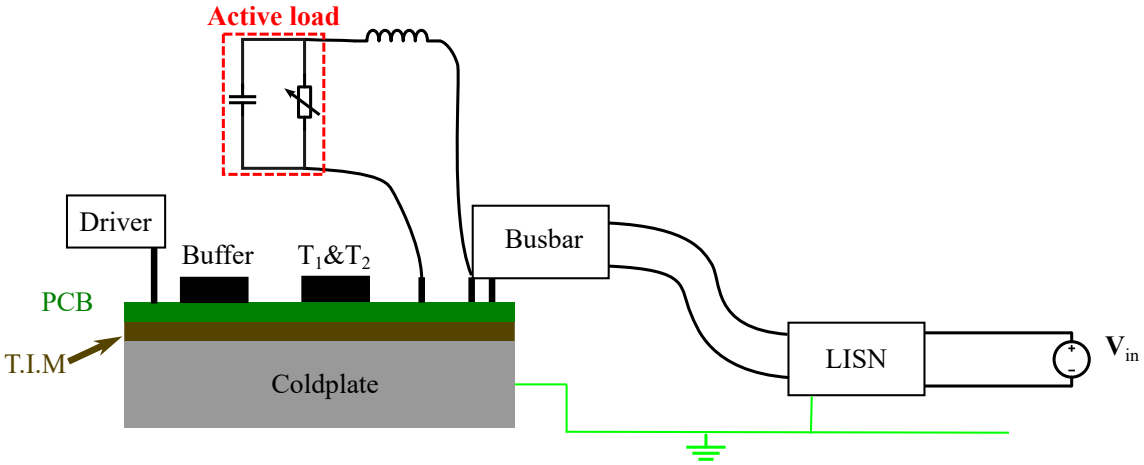

Figure 4.26: Illustration of the Buck circuit setup on the coldplate & highlighting the grounding line connection.

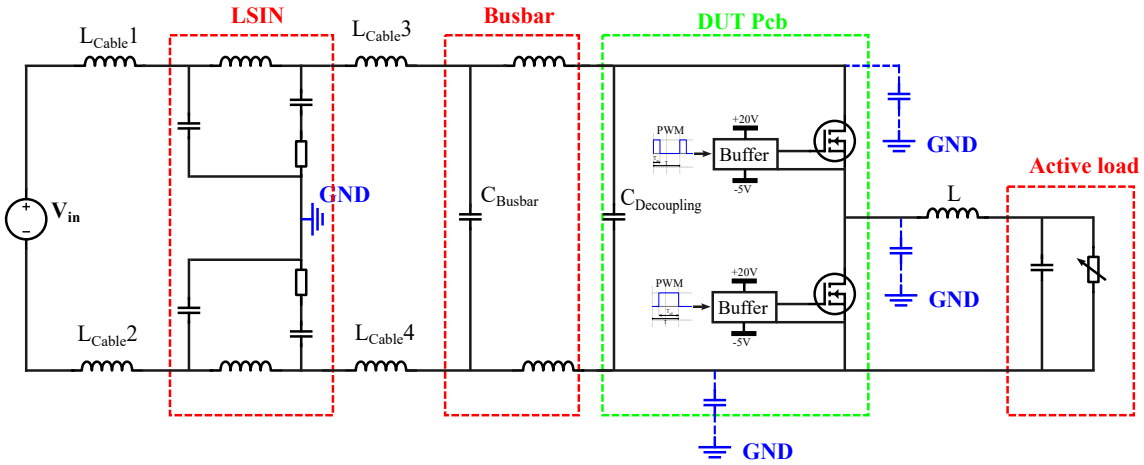

Figure 4.27: Complete electrical Buck circuit: model of the 2 LSIN modules, Busbar model, switching cell circuit (green) and the electronic load

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The Cold plate is connected to a copper ground plane by a short wire. Two LISN modules (Solar electronics company 9403-5-Bp-10-BNC) connect the input power source (SP600VDC3000W, 3 kW) to the Busbar PCB. Their grounds are also connected to the ground plane. The driver PCB provides isolated power supply ($-5\,\mathrm{V}/19\,\mathrm{V}$) to to the buffer circuit implemented in the DUT and hosts fiber optics receivers for the isolated transmission of PWM signals. These signals are generated using a National instrument module and a custom Labview GUI. The active load (PSBE 10750-60) is configured to operate as a constant resistor R_{load}, together with an input capacitance of 540 µF.

4.2 Calorimetry Test

The setup described here allows for measuring the power losses of the DUT with acceptable accuracy. It implements a flow calorimetry concept, in which the heat generated by the DUT is collected using a cooling fluid (here water). The fluid flow rate and temperature rise at equilibrium are measured. The power dissipated is then calculated as

$$P_{losses} = \Delta T.C_p.\dot{m} = \Delta T.C_p.\rho.Q \tag{4.1}$$

with C_p the specific heat of the fluid, ρ its density, $\dot{m}$ the mass flow rate, Q the volumetric flow rate and ΔT the temperature difference between the outlet and the inlet of the cold plate.

4.2.1 Calorimetry setup

Fig. 4.28 shows the complete setup used for the calorimetric measurement. The corresponding schematic is presented in Fig. 4.29: A chiller system controls the water's temperature and forces the water's circulation using an internal pump. Two valves (one in series with the cold plate, one bypassing the chiller) allow the water flow rate in the cold plate to be set. This flow rate Q is monitored using a flowmeter (Ref: RS 511-3965, constructor accuracy of 1.5 % & calibrated accuracy of 0.4%). Water temperature is measured at the inlet T_{in} and the outlet (T_{out}) of the cold plate. To ensure sufficient accuracy in the temperature measurements, 4-wire resistance temperature detector (RTD) temperature sensors are used (Pt100 with ref: RS 370-6571, classe A: $\pm 0.15 + 0.002.|t|[°c]$).

An accurate measurement of the temperature difference between T_{out} and T_{in} is key for the calorimetric method. In addition to using accurate sensors, this requires

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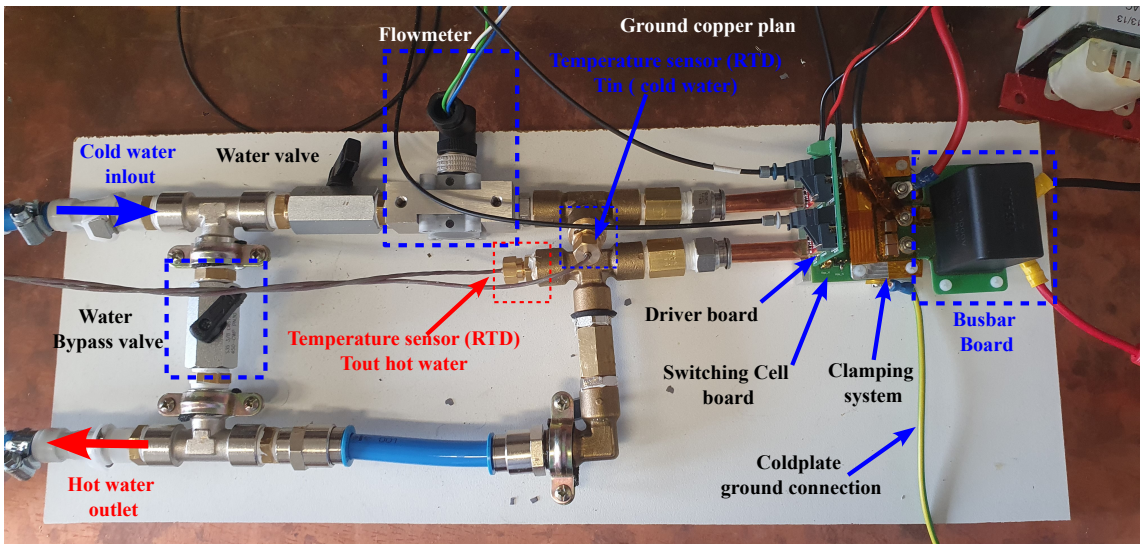

Figure 4.28: Complete test setup: calorimetry measurement elements, Switching cell board, Driver board and Busbar board.

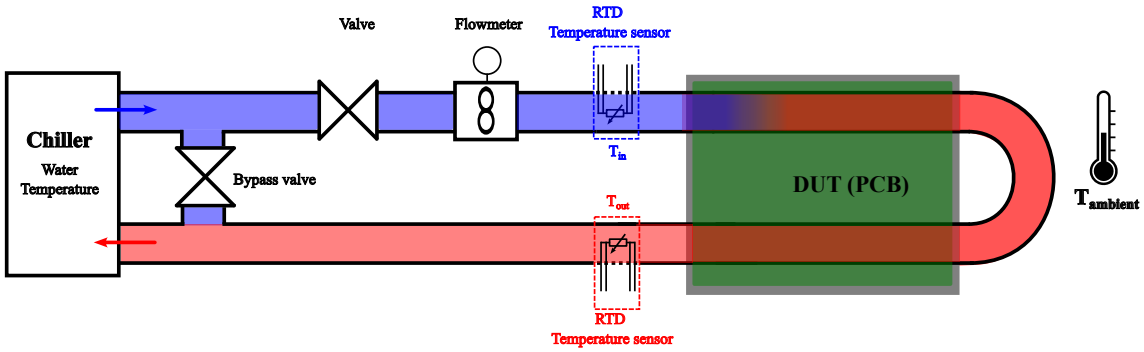

Figure 4.29: Schematic of the liquid cooling circuit and the elements used for the calorimetry measurements of the the switching cell losses.

special care in data acquisition. This is described later in this chapter and relies on the hardware described in Fig. 4.30. The signal from both RTD probes is acquired using a resistance-to-digital converter dedicated module (Adafruit MAX31865 RTD, 15-bit). The digital data is then transferred by SPI-communication to an Arduino board which performs the resistance/temperature conversion [102]:

$$R_{RTD} = ADC_{norm} \cdot \frac{R_{REF}}{A_{ADC}} + offset \tag{4.2}$$

$$R_{RTD}(t) = R_0 \left(1 + A\,T + B\,T^2\right) \quad for \quad T \geq 0C \tag{4.3}$$

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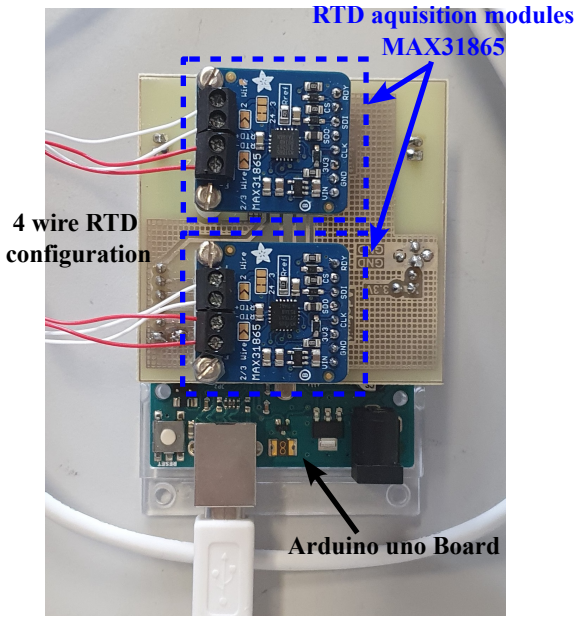

Figure 4.30: Custom acquisition system used for the RTD temperature sensors

with

ADC_{norm}: Normalized ADC reading
A_{ADC}: ADC resolution
R_{REF}: is the reference resistor used in the circuit (430 ohm 0.1%)
R_0: Resistance at 0°C (typically 100 Ω).
A and B : Callendar–Van Dusen coefficients and for PT100, standard values (IEC 60751) are:
$A = 3.9083 \times 10^{-3}\,°C^{-1}$
$B = -5.775 \times 10^{-7}\,°C^{-2}$

The Arduino board is connected by USB to a PC running a LabVIEW program. This custom program controls the sampling rate and moving average of temperature measurements (the sampling frequency and the number of data points will be discussed in the next section). It also plots the data and writes it to a file. Additionally, the program generates the switching signals necessary to control the Buck circuit using a National Instruments module.

4.2.2 Calorimetry measurement model

Flow calorimetry is based on the assumption that all heat dissipated by the DUT is collected by the cooling fluid and that the temperature difference is not affected by the environment. In this case, eq. (4.1) is valid and can be used to compute the power lost by the DUT. However, in the setup depicted in Fig. 4.28, the system is not thermally isolated, and some heat exchange with the ambient air takes place in the

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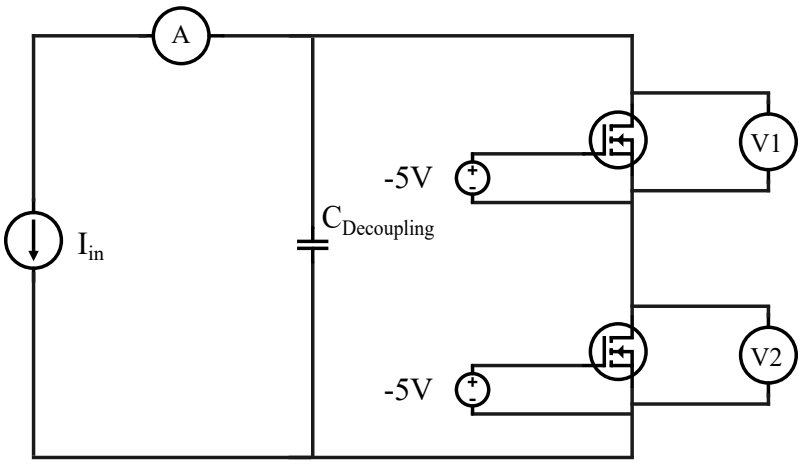

Figure 4.31: Calibration circuit of the calorimetry test setup.

part of the loop between both temperature sensors. This introduces a measurement error.

To limit this error, our measurement method includes a correction constant T_{offset} that can compensate for heat leakage, but also for temperature sensor and flowmeter deviation.

$$P_{losses} = (\Delta T - T_{offset}).C_p.\dot{m} \tag{4.4}$$

An influence of the ambient temperature was observed in some measurements, which can be attributed to heat exchange between the setup and the surrounding air through surfaces that are not thermally insulated. This can be analytically illustrated by the heat transfer equation 4.5

$$\dot{Q} = hA(T_{chiller} - T_{ambient}) \tag{4.5}$$

These exposed surfaces are visible in Figs. 4.28 and 4.29. One possible improvement would be to apply thermal insulation to these areas to reduce heat loss. However, this was not implemented in the current setup, as the resulting error from this heat leakage was considered negligible and was, for the most part, compensated by the offset value applied during calibration. Moreover, maintaining convenient access to the Device Under Test (DUT) was prioritized over minimizing these minor thermal losses.

The next sections present the calibration circuit and protocol used to identify T_{offset}. The idea is to inject a constant and known power loss and compare it to the measured value by calorimetry.

4.2.2.1 Calibration circuit

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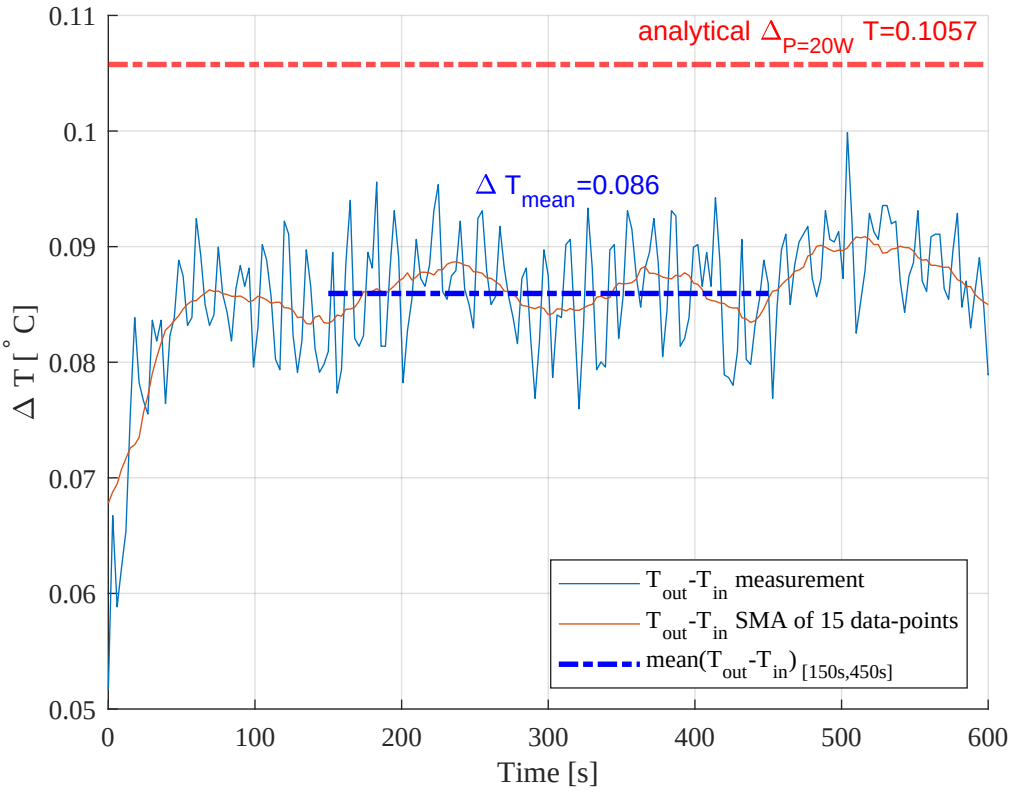

Figure 4.32: Temperature difference measured for $P = 20\,\mathrm{W}$ and $Q = 2.7\,L/min$. Acquisitions are performed with a period of 20 ms, and averaged over 150 points to plot the blue curve. The orange line is a 15-point moving average of the blue curve.

Fig. 4.31 presents the calibration circuit used to generate a known amount of power losses using the same DUT PCB as for the calorimetric measurements. A negative bias voltage is applied on the gate of both SiC MOSFETs to turn them off. A constant current I_{in} is then circulated in the body diodes of the MOSFETs. As the forward voltage drop in the body diodes is relatively large ($\approx$3 V), this circuit produces a significant amount of losses with a reasonable current level ($<$10 A):

$$P_{losses} = (V1 + V2) \times I_{in} \tag{4.6}$$

4.2.2.2 Measurement protocol

Fig. 4.32, shows a temperature acquisition performed for $P_{losses} = 20W$ using the calibration circuit. For this measurement, the $T_{out} - T_{in}$ data correspond to an average value of 150 data-points with a sampling period of 20 ms (the minimum acquisition period of our temperature sensor system), or one data point every 3 seconds. Applying a 15-point moving average filter on these data produces the orange curve. This curve evidences oscillations due to the chiller regulation system.

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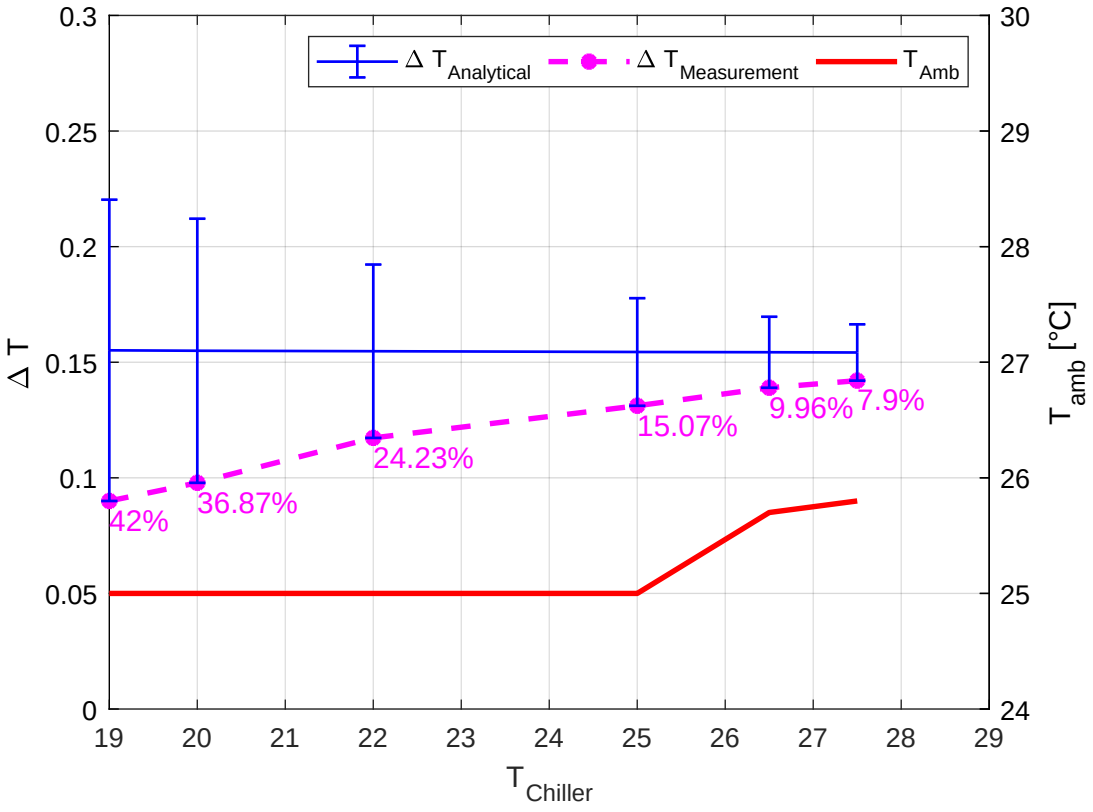

Figure 4.33: Temperature difference ΔT for a fixed injected power of $P = 29.4\,\mathrm{W}$ (blue curve) as a function of the temperature of the cooling water $T_{Chiller}$. The red curve shows the ambient temperature measured during the tests.

These oscillations have a period of 150 s, so an additional average (ΔT_{mean}) is calculated over 300 s (2 periods of chiller regulation system), which is enough to neutralize their negative effect on the accuracy. Considering that the steady-state begins from $t = 100$ s, ΔT_{mean} is computed over the time interval $[150s, 450s]$ for every measurement.

In Fig. 4.32, a difference of $0.0197\,°\mathrm{C}$ is observed between the measured ΔT_{mean} and the expected value $\Delta T_{P=20W}$ (calculated considering dissipated power and water flowrate). Therefore, an offset must be applied as introduced in eq. (4.4). This T_{offset} corrects for the errors of the flowmeter readings, the temperature sensors' inaccuracy and the heat transfer rate $\dot{Q}$ with the ambient air (heat leaks).

An analysis of the effect of the ambient and cooling fluid temperature is presented in Fig. 4.33. The test consists in injecting a constant $P_{losses} = 29.4\,\mathrm{W}$, while varying the water temperature $T_{chiller}$ between 19 and $28\,°\mathrm{C}$ and monitoring the ambient temperature T_{amb}. ΔT without the correction constant is measured and plotted in blue in the Figure, with the pink numbers indicating the difference in percentage (error) between the measured value and the analytical value of ΔT. This difference is effected strongly by the difference between the $T_{chiller}$ and T_{amb} as is described

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by the heat transfer equation 4.5. This significant effect of $T_{chiller}$ and T_{amb} on the measurements shows the importance of realizing the calorimetry test in a controlled room temperature to grant a constant T_{amb}.

The following protocol is used for the rest of the calorimetry test:

1. Conduct the test in a controlled room temperature(constant T_{amb}), to limit the error due to the heat leaks. $T_{chiller}$ is regulated to $\pm 0.1\,^{\circ}\mathrm{C}$

2. Realize a calibration test to determine the offset constant T_{offset} for the test environment and parameters (constant T_{amb}, $T_{chiller}$ and mass flow $\dot{m}$)

3. Compute (ΔT_{mean}) as the mean value of 100 data-points (300 seconds measurement interval $[150s, 450s]$) after the beginning of the steady-state (at $t = 100\,\mathrm{s}$) for every measurement.

4.2.3 Estimation of Measurement Accuracy and Uncertainty

This section presents a quantitative evaluation of the accuracy and uncertainty of the calorimetric measurement setup developed for power loss estimation on the half-bridge PCB. The setup relies on precise measurements of coolant flow rate and temperature difference across the heat sink to determine power dissipation.

4.2.3.1 Sources of Measurement Uncertainty

The total uncertainty in the power measurement arises primarily from two sensors: the flowmeter and the RTD temperature sensors.

- **Flowmeter**: The flow rate is controlled using a flowmeter with a full-scale value of 6.5 L/min. According to the manufacturer's specification, the uncertainty is ±1.5% of full scale (FSD), yielding:

$$\Delta Q = 0.015 \times 6.5 = 0.0975\,\mathrm{L/min}$$

- **Temperature Sensors (PT100)**: Platinum RTDs (PT100) are used to measure the inlet and outlet temperatures. The acquisition system introduces a maximum uncertainty of ±0.05%, while the intrinsic linearity error of the RTD is around ±0.15% according to IEC 751. However, by applying the Callendar–Van Dusen equation, a linearity of ±0.01°C is achieved over the operating range. For a typical measurement of temperature difference values

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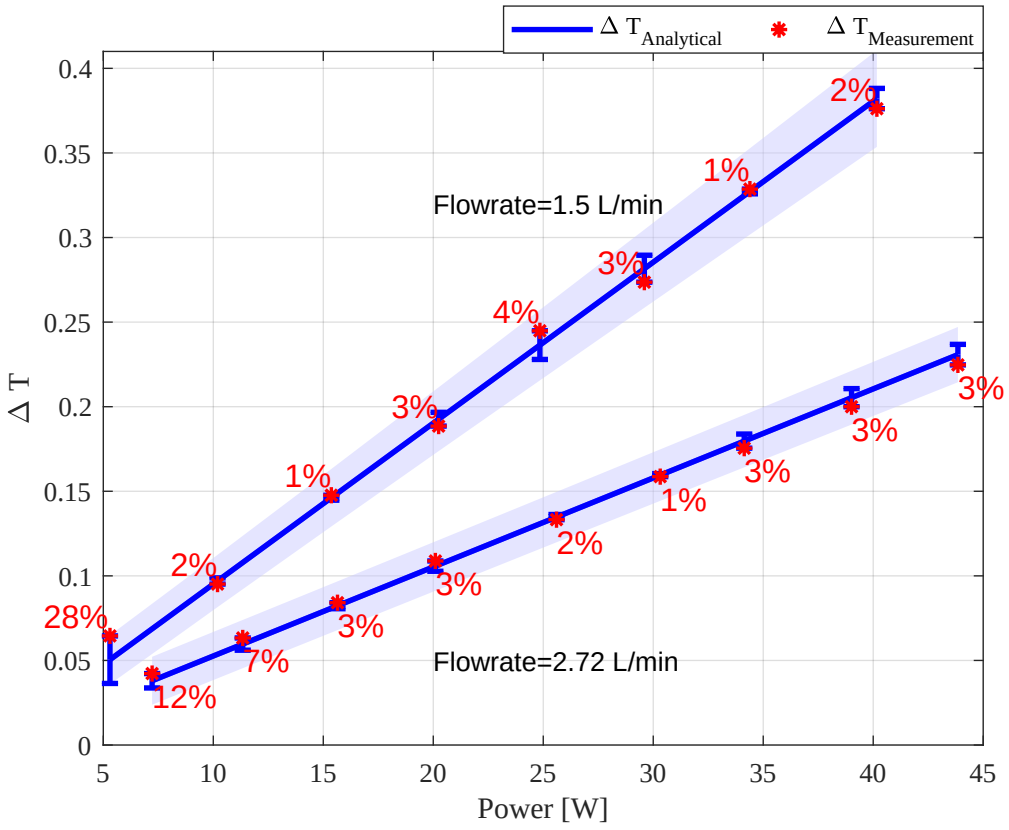

Figure 4.34: Comparison between injected and measured power for $Q = 1.5\,\mathrm{L/min}$ and $Q = 2.72\,\mathrm{L/min}$. Uncertainty bounds are shown as shaded areas.

$(\Delta T = 0.1°\mathrm{C}\,; 0.2°\mathrm{C}\,; 0.3°\mathrm{C}\,)$, the associated uncertainty is:

$$\Delta(\Delta T) = \sqrt{2 \cdot (0.01)^2} = 0.0141°\mathrm{C},$$

$$\Rightarrow \quad \frac{\Delta(\Delta T)}{\Delta T} = \begin{cases} \dfrac{0.0141}{0.1} = \mathbf{14.1}\% & \text{for } \Delta T = 0.1°\mathrm{C} \\ \dfrac{0.0141}{0.2} = \mathbf{7.05}\% & \text{for } \Delta T = 0.2°\mathrm{C} \\ \dfrac{0.0141}{0.3} = \mathbf{4.70}\% & \text{for } \Delta T = 0.3°\mathrm{C} \end{cases}$$

4.2.3.2 Propagation of Uncertainty in Power Estimation

From the power loss computation relation 4.1, assuming the uncertainties in Q and ΔT are uncorrelated, the relative uncertainty in power is:

$$\frac{\Delta P}{P} = \sqrt{\left(\frac{\Delta Q}{Q}\right)^2 + \left(\frac{\Delta(\Delta T)}{\Delta T}\right)^2} \tag{4.7}$$

The uncertainty is evaluated for two calibration flowrates:

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- **Case 1:** $Q = 1.5\,\mathrm{L/min}$

$$\frac{\Delta Q}{Q} = \frac{0.0975}{1.5} = 6.5\%$$

$$\Rightarrow \quad \frac{\Delta P}{P} = \begin{cases} \sqrt{(0.065)^2 + (0.141)^2} = \mathbf{15.5}\% & \text{for } \Delta T = 0.1^\circ\mathrm{C} \\ \sqrt{(0.065)^2 + (0.0705)^2} = \mathbf{9.57}\% & \text{for } \Delta T = 0.2^\circ\mathrm{C} \\ \sqrt{(0.065)^2 + (0.047)^2} = \mathbf{7.98}\% & \text{for } \Delta T = 0.3^\circ\mathrm{C} \end{cases}$$

- **Case 2:** $Q = 2.72\,\mathrm{L/min}$

$$\frac{\Delta Q}{Q} = \frac{0.0975}{2.72} = 3.58\%$$

$$\Rightarrow \quad \frac{\Delta P}{P} = \begin{cases} \sqrt{(0.0358)^2 + (0.141)^2} = \mathbf{14.5}\% & \text{for } \Delta T = 0.1^\circ\mathrm{C} \\ \sqrt{(0.0358)^2 + (0.0705)^2} = \mathbf{7.89}\% & \text{for } \Delta T = 0.2^\circ\mathrm{C} \\ \sqrt{(0.0358)^2 + (0.047)^2} = \mathbf{5.73}\% & \text{for } \Delta T = 0.3^\circ\mathrm{C} \end{cases}$$

These values define the expected uncertainty bounds for the calorimetric power measurements under each tested flow condition.

4.2.3.3 Estimation of Measurement Accuracy

To assess the accuracy of the measurement, the experimental results obtained from the calorimetric setup are compared with known injected power values, as determined using a calibration PCB circuit detailed in the calibration section 4.2.2.1. This analysis is conducted across a range of injected power levels for two different flow rate conditions: $Q = 1.5\,\mathrm{L/min}$ and $Q = 2.72\,\mathrm{L/min}$. Figure 4.34 illustrates the comparison between the measured and analytically estimated ΔT, based on the calorimetry relation outlined in equation 4.4. The deviation from the expected values indicates the system's accuracy, while the shaded area represents the uncertainty bounds.

The relative error is computed as:

$$\text{Error } [\%] = \left| \frac{\Delta T_{\text{measured}} - \Delta T_{\text{Analitical}}}{\Delta T_{\text{Analitical}}} \right| \times 100$$

and the corresponding accuracy is defined as:

$$\text{Accuracy } [\%] = 100\% - \text{Error } [\%]$$

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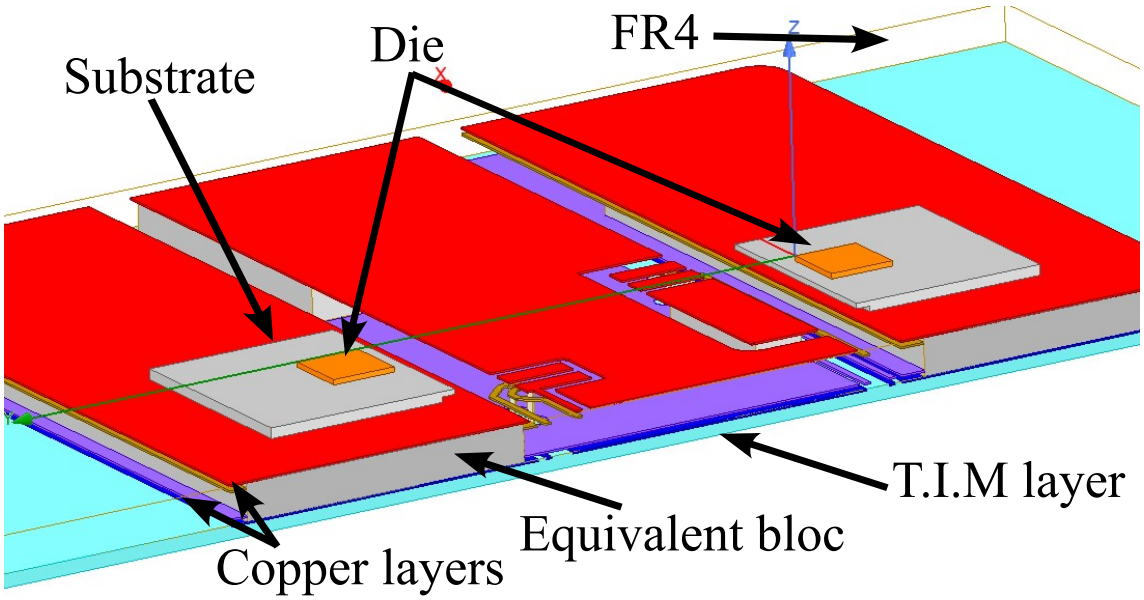

Figure 4.35: Cross-section vies of the built 3D model of the simulated PCB of the half-bridge discrete version

For low power loss conditions, such as $P = 10\,\mathrm{W}$ (corresponding to $\Delta T \approx 0.1°\mathrm{C}$) at $Q = 1.5\,\mathrm{L/min}$, and $P = 15\,\mathrm{W}$ (equivalent to $\Delta T \approx 0.08°\mathrm{C}$) at $Q = 2.72\,\mathrm{L/min}$, the relative uncertainty becomes significant, leading to reduced accuracy in the power estimation. This is primarily due to the dominance of the RTD sensor resolution and the flowmeter uncertainty relative to the small thermal signal.

As the temperature gradient increases, the measurement uncertainty decreases rapidly. For temperature differences above approximately $\Delta T \gtrsim 0.1°\mathrm{C}$, corresponding to injected powers exceeding 10 W at $Q = 1.5\,\mathrm{L/min}$ and 15 W at $Q = 2.72\,\mathrm{L/min}$, the accuracy improves significantly. In this regime, the calorimetric system achieves a relative accuracy greater than 93% in the worst-case scenario and typically exceeds 96%. These results confirm the effectiveness of the calorimetric system for reliable power loss estimation over a broad operating range, specifically, for powers above approximately 10 W at $Q = 1.5\,\mathrm{L/min}$, and 15 W at $Q = 2.72\,\mathrm{L/min}$.

4.3 Virtual Prototype Validation

In this section, the previously calibrated calorimetric setup is employed, following the established measurement protocol, to evaluate the power losses of the buck converter circuit. The measured losses are then compared against the estimations produced by the developed electro-thermal virtual prototype of the same PCB (the figure 4.35 a cross section view of the 3D-model used for the thermal simulation).

Figure 4.36 presents the comparison across different load power levels. The green curve corresponds to power loss estimations from the only electrical model

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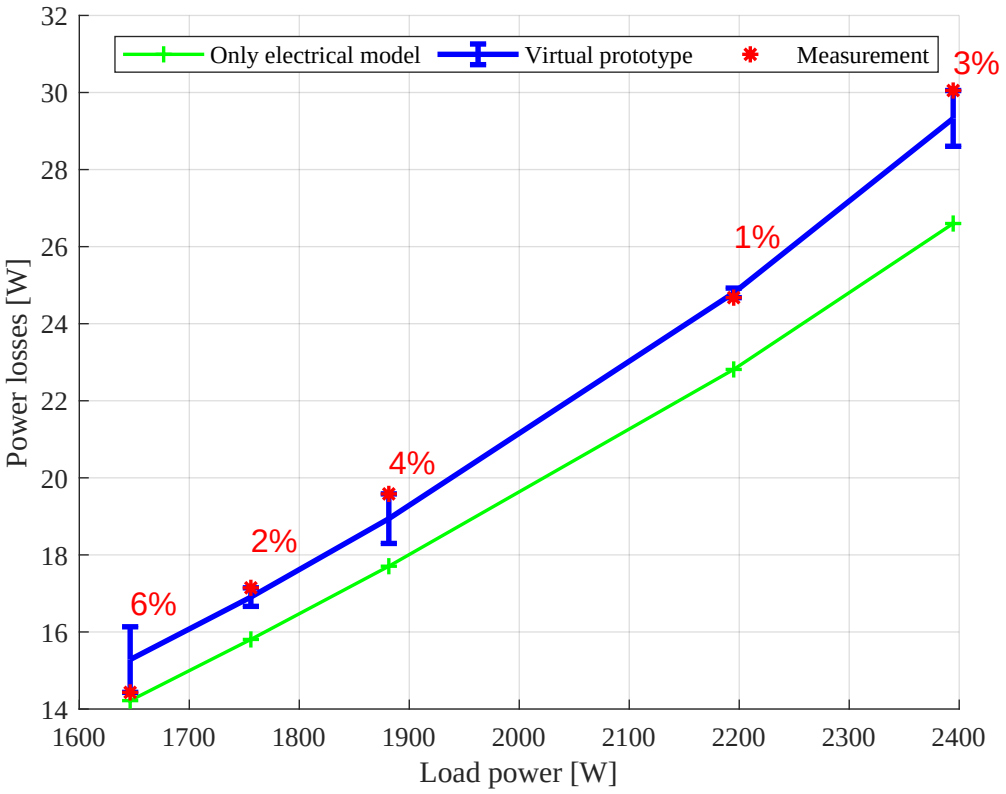

Figure 4.36: Calorimetry Analysis of Losses in a Buck Converter with 300V DC Input, 38% Duty Cycle, and Flow Rate of 2.72 L/min.

(no thermal model), the blue curve shows the predictions of the electro-thermal virtual prototype, and the red markers represent the experimental data obtained via calorimetry.

The results demonstrate a strong agreement between the virtual prototype and the measured data. The relative error remains around 6% at low power levels and decreases to below 4% as the dissipated power increases, which falls within the expected accuracy range of the calorimetric test bench.

The comparison also highlights a significant discrepancy between the only electrical and virtual prototype models, particularly at higher power levels. This underlines the importance of incorporating thermal effects to achieve accurate power loss estimations, thus validating the relevance and effectiveness of the virtual prototype modeling approach.

5 Conclusion

In this chapter, various tests were conducted to validate the results of the proposed workflow.

For electrical validation, a double pulse test and impedance characterization were

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performed alf-bridge embed- ded PCB and compare the results to the waveforms simulated using the automatically generated electrical virtual prototype model.

For thermal validation, several validation cases were presented to evaluate the accuracy and efficiency of the proposed thermal modeling approach.

First, a single-chip PCB was used to assess the fidelity of the simplified model based on average junction temperature and equivalent via blocks. Thermal impedance measurements were compared with simulation results, showing good agreement despite slight discrepancies in transient phases due to idealized boundary conditions.

Subsequently, a multi-chip half-bridge embedded PCB was analyzed to validate the modeling of self-heating and cross-coupling effects. A simplified representation of µVias enabled a significant reduction in simulation time while preserving the overall thermal behavior. Additionally, the influence of mechanical pressure between the power chips and the cooler was investigated, and a basic model of the cooler was introduced to support analysis of the system's thermal settling behavior.

To validate the electrothermal model, a calorimetry test was mounted, and high-accuracy temperature sensors were employed for the cooling system. An accuracy of 4% was achieved in measuring power losses using a model with an offset that was calibrated to compensate for heat leakage and limit various errors.

The generated models were primarily based on information provided by the manufacturer, including data sheets for the components used, LTspice models, and the layout design. The impact of differences between the manufactured prototypes and the PCB layout on the estimated end results was assessed, considering the effect of simplifications and assumptions used in the workflow.

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Chapter 5

Design of PCB-based inverters

The previous chapters are dedicated to presenting and validating the automated process flow for generating the models of a converter. In this chapter, we verify whether this method can be used in a real design case.

This chapter analyzes how it is possible to use the generated models to make design choices.

Specifically, the design of a 3L-ANPC PCB is examined, as it presents a suitable level of complexity for testing.

Because time constraints did not allow for the designed ANPC bridge to be built and tested, another, simpler application case is also presented in this chapter: the 2-level half-bridge in which layout variants are compared. It corresponds to DUTs ④ and ⑤ in the previous chapter.

1 Presentation of the test case

1.1 Specifications

The proposed power converter to be designed in this chapter is a DC/AC ANPC 3-phase inverter having the following characteristics :

- Input DC Voltage : $V_{DC} = 1500\,\mathrm{V}$, ($pm$ $750\,\mathrm{V}$)
- Output Power: $P_{out} = 100\,\mathrm{kW}$ ($33\,\mathrm{kW}$ per phase)
- Power efficiency: $\eta > 98\,\%$
- Power Factor: $PF = 0.9$
- Modulation Factor: $m = 0.9$

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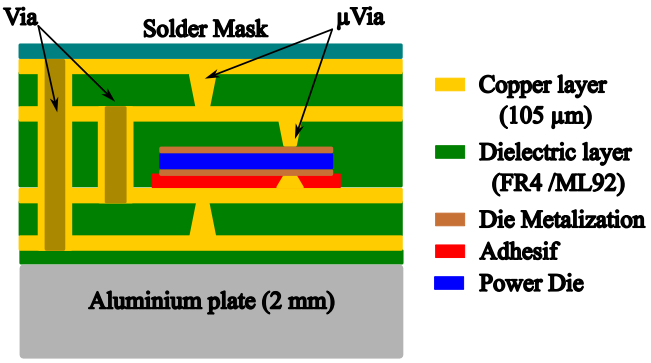

Figure 5.1: Embedded PCB stack-up with the possible Via & µVia types.

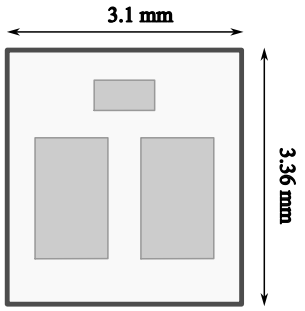

Figure 5.2: Wolfspeed CPM2-1200-0080 bare-Die[103].

- Power density: $> 30\,\mathrm{kW\,kg^{-1}}$
- Cooling Method: Water cooling via cold plate ($T = 85\,^{\circ}\mathrm{C}$)

Proposed design parameters:

To narrow the design domain and to ease fabrication, we have fixed some design parameters, such as the PCB stack-up to use or the power die reference:

- Embedded PCB technology using a 4-layer stack-up with a copper width of 105 µm (Fig. 5.1).
- Power Die (figure 5.2): SiC MOSFET 1200 V, 36 A, 80 mΩ (Wolfspeed CPM2-1200-0080 bare-Die)
- 2 possible Prepreg materials:
  - FR4: A common printed circuit board (PCB) material with a thermal conductivity of $0.3\,\mathrm{W\,m^{-1}\,K^{-1}}$;
  - ML92: A high-performance material with a thermal conductivity of $2\,\mathrm{W\,m^{-1}\,K^{-1}}$.
- Design rules according to the IPC2221 B Standard.
- A 2 mm aluminium baseplate, attached at the bottom of the PCB for effective heat dissipation and to mount the PCB on a cold plate without a complex clamp system.

Various configurations are analysed in the proposed converter design process to enhance the PCB layout, focusing primarily on reducing thermal resistance and minimizing parasitic elements. Chip parallelization is required to manage the required current, and a special care is given to the layout of a multi-chip switching cell in terms of thermal management and current balancing.

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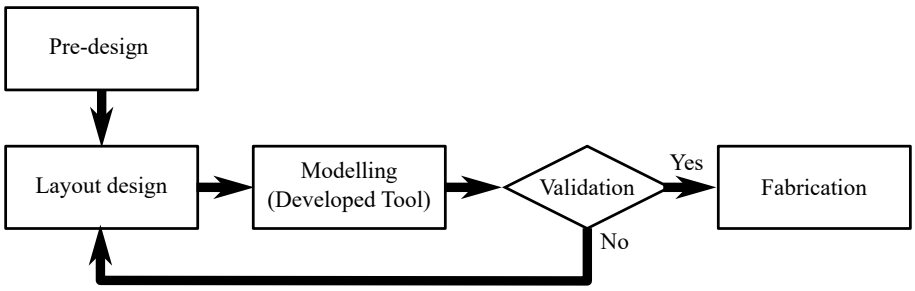

Figure 5.3: Workflow to follow in the design of the proposed power converter

1.2 Design Workflow

As the model generation method which is described in this thesis starts with a PCB design, the focus is on analyzing the effect of the PCB layout. In the design of a converter, however, significant work is required before laying out the PCB: selection of a topology, of each of the components, validation using analytical models, etc. Here, these steps are called "pre-design" (Fig. 5.3). While it is not the focus of this thesis work, it is a very important part of a converter design. Therefore, we describe the pre-design of the ANPC bridge in section 2, to illustrate how our method can be part of a complete design flow.

The primary focus of our design exercise is on optimizing the system's electrical and thermal performance by adjusting the arrangement of key components, including power chips, coupling capacitors, and vias. Additionally, the study compares the thermal performance of a new prepreg material with that of a more traditional material. The aim is to evaluate the potential thermal advantages of using the new material in the system layout. Each layout iteration results in a virtual prototype, which analyzed to estimate the system's waveforms and thermal behavior. This is addressed in section 3.

2 Pre-design

This section focuses on using analytical models to calculate the power losses associated with different configurations of parallelized power MOSFETs and control strategies, which are crucial for minimizing thermal stress and enhancing reliability. Additionally, we examine the various power loops within the multilevel circuit, highlighting how these elements interact. This theoretical work helps when analyzing the simulation results in section 3.

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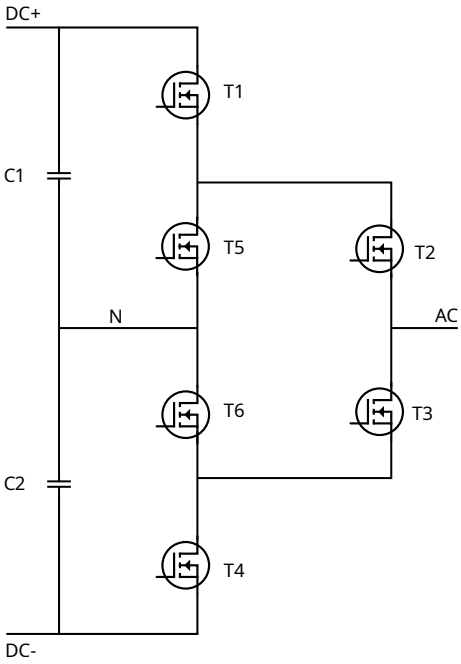

Figure 5.4: ANPC multilevel circuit

2.1 ANPC Converter

Fig. 5.4 illustrates the ANPC circuit, a multilevel converter commonly employed in industrial applications. This family of converter topologies is renowned for its high efficiency and versatility. The term "multilevel" was introduced with the development of the three-level converter by Nabae [104].Multilevel converters offer several key advantages: they help reduce common-mode voltage, improve voltage waveform quality, minimize input current distortion, balance voltage and thermal stress across components, and lower output harmonic distortion. By carefully optimizing the modulation scheme, switching events can be effectively distributed across the power devices. This approach prevents excessive stress on any single switch and minimizes overall losses [105, 106, 107].

A notable feature of this topology is the potential for hybridizing different switch technologies. A combination of the low-switching-loss advantage of SiC MOSFETs with the cost-effectiveness of Si devices can lead to a reduction in total cost by over 50 % while minimizing switching losses and improving efficiency by 0.5–1.0 % relative to an all-Si-IGBT power stage [108].

In our case study, because we only have one type of chips that can be embedded in PCBs (PCB embedding requires a specific, thick copper metallization of the chips), the circuit will consist entirely of SiC MOSFETs.

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2.2 Analytical Analysis

The 6 switches in an ANPC (Active Neutral Point Clamped) bridge can be operated using a variety of switching sequences. These modulation strategies are essential not only for defining the current paths during operation but also for ensuring balanced power losses across the semiconductor devices. A comprehensive literature review has identified four distinct PWM-based control approaches tailored for the ANPC topology. Building upon this review, we derive a set of analytical equations that characterize the current distribution and associated power losses in each MOSFET and intrinsic diode of the circuit.

To validate the accuracy of these analytical expressions, detailed simulations were conducted using PSIM, replicating the behavior of the converter under each modulation scheme. These simulations confirm the relevance and precision of the proposed models under realistic operating conditions. The complete set of analytical formulations and circuit behavior under each control scheme is provided in Appendix A.

This analytical investigation plays a central role in guiding the overall converter design. It provides essential data to determine the appropriate number of power devices in parallel, supports a reliable estimation of the converter's efficiency, and informs the selection of the most suitable control strategy for the target application.

2.2.1 Modulation Sequences

Modulation sequences define the temporal and spatial activation patterns of the switches within the ANPC bridge, directly influencing the converter's performance in terms of efficiency, thermal behavior, and EMI characteristics. Each sequence represents a specific philosophy of power distribution across the topology, with implications on switching losses, current loop geometries, and thermal gradients across the PCB. These sequences must be carefully matched to the system's operating conditions and performance targets.

The four modulation strategies evaluated in this work are:

- **PWM1 (Outer Cell Modulation):** In this scheme, cell 1 (T1/T5) and cell 3 (T4/T6) are operated at high switching frequency while cell 2 (T2/T3) remains static during most of the cycle. The commutation results in alternating current paths involving one active switching leg and one passive (static) leg. This modulation produces two distinct zero-voltage states (O^+ and O^-), each relying on different semiconductor pairs and consequently exciting different

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physical loops on the PCB. This can lead to spatial imbalance in thermal and electromagnetic behavior.

- **PWM2 (Central Cell Modulation):** This approach shifts the switching activity to cell 2 (T2/T3), while minimizing the use of the outer switches. By centralizing the commutations, the dominant loop geometry is altered, and the current paths become more compact. This reduces parasitic effects associated with long trace lengths in the outer legs, potentially improving EMI performance and switching efficiency.

- **PWM3 (Hybrid Modulation Based on Voltage Polarity):** Here, the switching activity alternates dynamically between cell pairs depending on the instantaneous sign of the reference voltage. During the positive half-cycle, one set of devices is modulated, while a different set is used in the negative half-cycle. This results in a hybrid behavior with more complex current paths, particularly around the zero-crossing of the output voltage where state transitions are more frequent. This sequence offers a trade-off between loss distribution and control complexity.

- **PWM4 (Simplified Zero-State Modulation):** This control method uses a single zero-voltage state regardless of the current direction. The switching activity is reduced and more predictable, leading to simpler control implementation. Although the loop activation is more uniform, this can result in localized heating and higher losses in specific devices if not properly balanced through design or cooling strategies.

Each of these modulation sequences has been analytically evaluated and simulated to understand its impact on switching losses, conduction losses, and current sharing among the devices. The insights derived from this analysis contribute significantly to the design choices made in the following sections.

2.2.2 Losses Analysis

Using the power chip specifications and converter requirements, we can perform an initial estimation to determine the number of parallel power chips required for each transistor position in the Active Neutral Point Clamped (ANPC) circuit. In particular, the converter's specifications demand a total output power of $P_{out} = 33\,\text{kW}$ per phase and a power factor of $cos(\varphi) = 0.9$. So the output power per phase

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is given by:

$$P_{out} = V_{out}^{rms}.I_{out}^{rms}.cos(\varphi) = 33\,\text{kW} \tag{5.1}$$

For a DC bus voltage of 1500 V ($\pm E = 750\,\text{V}$) and a modulation factor $m = 0.9$, the output voltage is :

$$V_{out} = m.E = m.\frac{V_{DC}}{2} = 0.9 \times 750 = 675\,\text{V} \tag{5.2}$$

Using eq. (5.1), the output current can be calculated as:

$$I_{out} = \frac{2.P_{out}}{V_{out}.cos(\varphi)} = \frac{2 \times 33000}{675 \times 0.9} = 108.64\,\text{A} \tag{5.3}$$

Each power chip has a current rating of 36 A. The number of parallel chips required is thus:

$$\text{Number of Parallel Chips } = \frac{I_{out}}{36} \simeq 3.02 \tag{5.4}$$

To go beyond this coarse estimation, a more detailed evaluation of the losses under various operational conditions and different scenarios is required. This analysis utilizes analytical formulas and the characteristics of the C2M1200 SiC MOSFET. Since the bare die datasheet does not provide specific switching energy values, this critical information is extracted from the LTSpice simulation model, as detailed in Annex B.

The conduction losses P_{Cond} in the MOSFET are primarily determined by the on-state resistance R_{DSon} and the drain current $I_{D_{rms}}$. These losses are calculated as:

$$P_{Cond} = R_{DSon}.I_{D_{rms}}^2 \tag{5.5}$$

The switching losses are evaluated by considering the total energy dissipated during turn-on E_{on} and turn-off E_{off}. The total switching energy E_{tot} is expressed as a function of the drain-source current I_D and the input DC voltage $E = \frac{V_{DC}}{2}$, normalized to a reference voltage V_{ref} :

$$E_{tot} = E_{on} + E_{off} = (a_M.I_{DS}^2 + b_M.I_{DS} + c_M).\frac{E}{V_{ref}} \tag{5.6}$$

Here, the coefficients a_M, b_M and c_M account for the nonlinear evolution of switching energies as a function of the switched current. These coefficients are derived from

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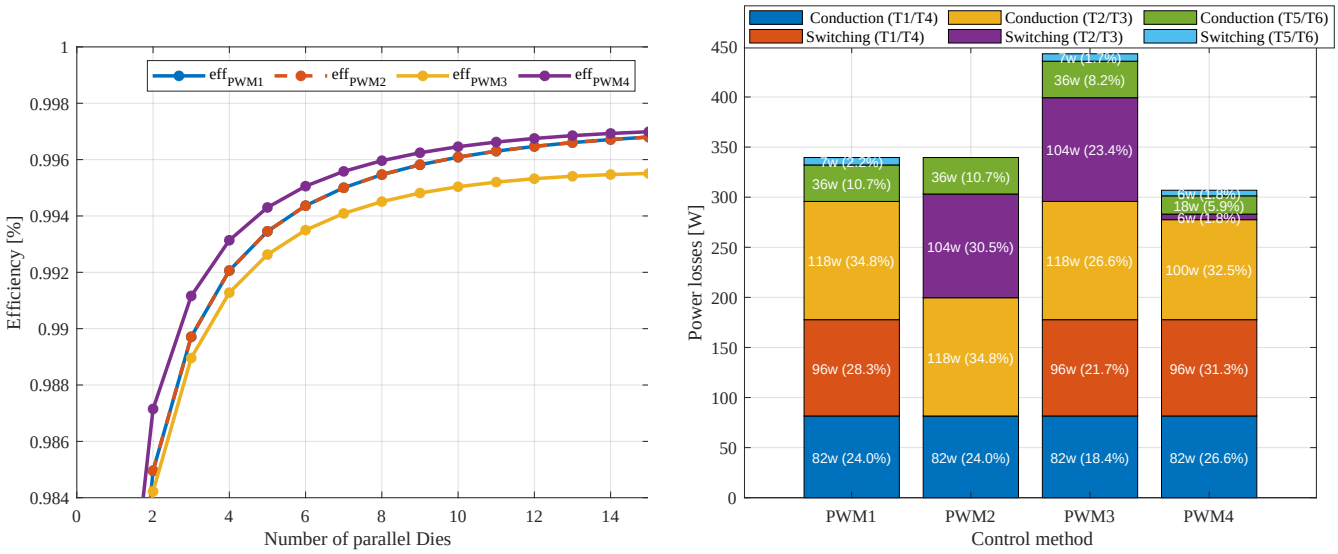

(a) (b)

Figure 5.5: (a): Efficiency estimation for the 4 PWM control approaches as a function of the number of paralleled chips, (b): Power losses distribution estimation; at Maximum Power of 33 kW, $f_{sw} = 20$ kHz, $m = 0.9$ and $cos(\varphi) = 0.9$.

the LTSpice simulation model and are critical for accurate loss estimation. The average switching power losses P_{sw} over a switching cycle are calculated by :

$$P_{sw} = \frac{1}{2\pi} \int_{\phi+\pi}^{\phi} (E_{on} + E_{off}).f_{sw}\, d\Theta \tag{5.7}$$

$$= \frac{1}{2\pi} \int_{\phi+\pi}^{\phi} (a_M.I_{DS}^2 + b_M.I_{DS} + c_M).f_{sw}\, d\Theta \tag{5.8}$$

where $\Theta = wt$ and $w = 2\pi f$ is the angular frequency.

The analysis presented here is based on analytical current equations derived for each PWM control sequence, as detailed in Appendix A. In Figure 5.5a, we examine the relationship between the number of parallel chips and the resulting losses. An estimation of the efficiency evolution is presented for these 4 PWM control approaches, considering various cases of parallelized power MOSFETs.

The results indicate that using four parallel chips enables an efficiency exceeding 99% for all the control methods. Notably, the PWM4 method achieves an efficiency of 99.3%. However, the final validation of the number of chips must be confirmed by assessing the junction temperature using the virtual prototyping approach design tool.

The calculated power losses distribution, categorized by types and location of losses is illustrated in Fig. 5.5b for a configuration of 4 parallel power chips. A notable observation is that the control strategies of PWM1 and PWM2 result in identical total losses. This can be explained by the fact that T2 and T3 switch

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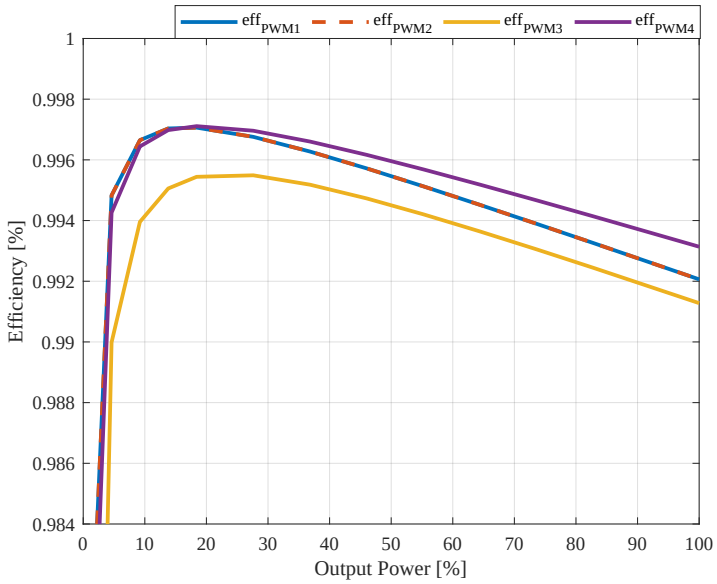

Figure 5.6: Efficiency estimation for the 4 PWM control approaches with Varying output Power for $P_{out_max} = 33\,KW$ in a configuration of 4 parallel chips, $f_{sw} = 20\,KHz$, $m = 0.9$ and $cos(\varphi) = 0.9$.

at the switching frequency in PWM1, while T1/T4 ($P_{sw} = 96\,\mathrm{W}$), and T5/T6 ($P_{sw} = 7\,\mathrm{W}$) alternate between line frequency and switching frequency during the negative and positive half cycles, respectively. In contrast, for PWM2, T1 and T4 operate primarily at line frequency, with high-frequency switching is handled only by T2 /T3 ($P_{sw} = 107\,\mathrm{W}$). The PWM3 strategy exhibits reduced efficiency largely because it doubles the output switching frequency. This leads to all cells operating at the switching frequency, resulting in a greater number of switching events, which in turn increases switching losses. Essentially, PWM3 can be seen as a combination of PWM1 and PWM2 within each switching cycle. The PWM4 strategy demonstrates significantly lower total power loss at this operating point. This advantage stems from its unique feature of having a single neutral state, allowing current to flow in either direction through both T2/T3 and T5/T6. This control strategy leads to a reduction in conduction losses (specifically, a 15 % reduction for T2/T3 and 50 % for T6/T5) and a slight reduction of the switching losses in the corresponding MOSFETs, compared to other control methods that utilize a single clamp path.

In Fig. 5.6, the efficiency of all control methods is evaluated across a range of power levels in a configuration of 4 parallel MOSFET-SiC devices. The efficiency exceeds 99% across nearly the entire power spectrum, with the PWM4 control method leading in performance starting from 15% of the maximum power output.

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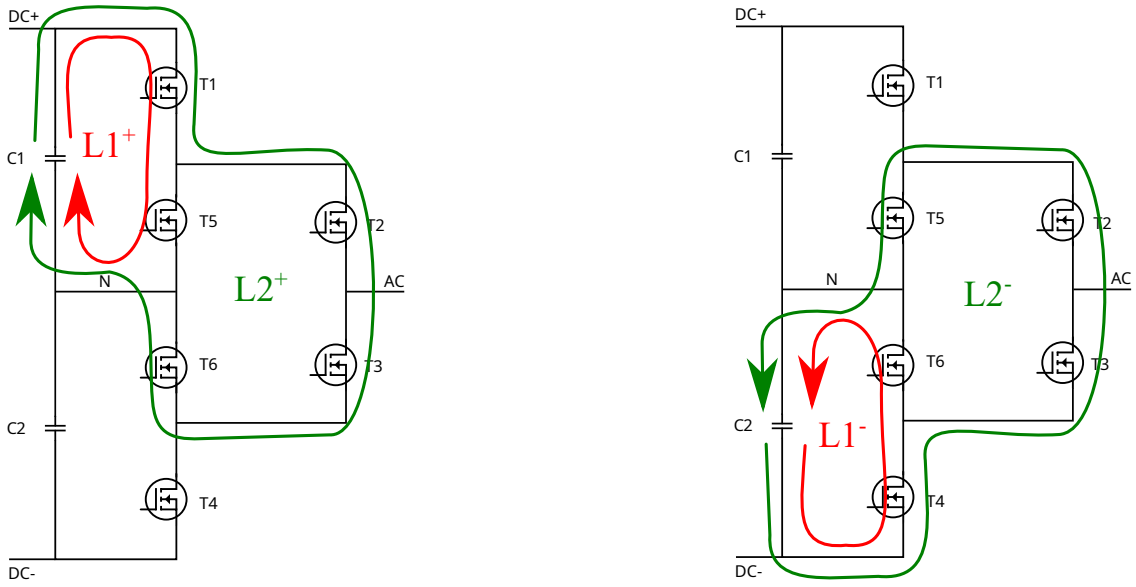

(a) positive loop

(b) negative loop

Figure 5.7: Identified power loops in the ANPC structure ($L1^+/L1^-$: short power loops, and $L2^+/L2^-$: long power loops).

2.3 Identified power loops

Figure 5.7 presents the four principal power loops identified in the ANPC converter topology. These loops correspond to dominant current paths during switching events in both the positive (Figure 5.7a) and negative (Figure 5.7b) output voltage half-cycles. Their geometry depends on the specific PWM strategy in use, with variations between short and long conduction paths, particularly during zero-voltage transitions.

Each modulation scheme (PWM1–PWM4) introduces distinct commutation patterns, with PWM1 and PWM3 enabling multiple zero-state loop configurations. Despite these differences, four key loop geometries consistently emerge as critical, especially during high di/dt transitions, where stray inductance can induce voltage overshoots. Accurate identification of these loops is essential for both analytical modeling and PCB layout, as they define the regions requiring minimized loop area and optimized return paths to reduce EMI and switching losses. These findings form the basis of the electromagnetic analysis presented in subsequent sections.

Conclusion of the Pre-Design Phase

This pre-design phase established a solid analytical framework to evaluate four PWM control strategies for the ANPC converter, focusing on current distribution, losses, and efficiency. The analysis led to a key design choice: using four parallel

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SiC MOSFETs per switch, which ensures over 99% efficiency, with PWM4 reaching 99.3% thanks to its simplified neutral state and balanced loss profile.

The study also identified the main power loops and their dependency on the switching strategy, offering essential guidance for minimizing EMI and thermal stress in the PCB layout. These results set the foundation for the next phase, virtual prototyping, where the analytical predictions will be refined under realistic operating conditions.

3 PCB Design

3.1 Introduction

Because of the practical issues associated with building a 24-chip ANPC half bridge (4 chips per switch position, 6 switches per half-bridge), it was decided early in the research project to follow a progressive approach: first we investigate a simple, 2-level, 2-chip half bridge, get the corresponding designs to be manufactured, then we move to 4-paralled-chips, 2-level half-bridge and finally to an ANPC structure. Indeed, a PCB with 24 embedded chip would not only be expensive to make, it would also result in a low number of working prototypes, given the manufacturing yield of a prototype run (96–98 %, a respectable value which is nonetheless too low when as many as 24 chips are involved).

3.2 Half-bridge Cell PCB

This first design step is used to investigate several layout configurations.

The primary parameters investigated here are the layout's parasitic elements and its thermal resistance. The design variation include the chips' location and orientation, the dielectric material's thermal conductivity, and the size of the copper pad underneath the chips.

3.2.1 Single-Chip design

The circuit and PCB stack for the half-bridge cell are illustrated in Fig. 5.8. The main parasitic elements of the layout are highlighted in blue. These include the power loop inductance L_p. They also include parasitic capacitances C_{DS1} and C_{DS2}, which are created by the copper tracks connected to each MOSFET's drain and source potentials. These capacitances influence the switching duration and losses in the MOSFETs. Furthermore, there are capacitances C_{DC-}, C_{DC+}, and

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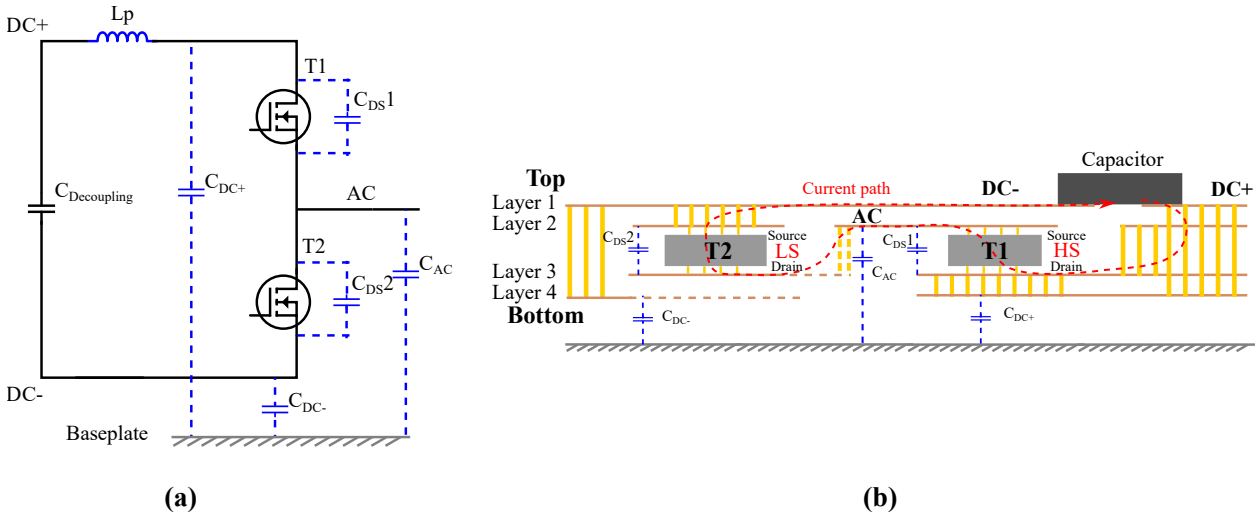
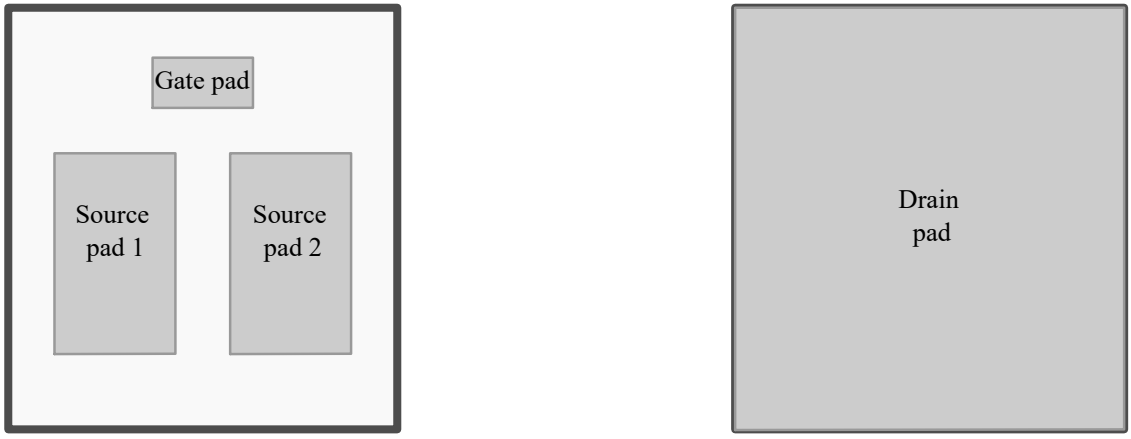


Figure 5.8: Half bridge parasitic circuit.



(a) Die TopView

(b) Die BottomView

Figure 5.9: Cree CPM2-1200-0080 Die Top & Bottom views

C_{AC} that are formed between the surfaces of the DC-, DC+, or AC tracks and the baseplate. These capacitances affect the electromagnetic behaviour of the system, as they provide paths for common-mode currents. This is particularly important of C_{AC}, as the AC track experiences fast voltage transients (which results in large displacement currents in C_{AC}).

3.2.2 PCB setup

Fig. 5.9 illustrates the two faces of the MOSFET dies that are used in this design. There are clear differences between the Drain pad surface on the bottom side and the Gate and Source pads on the top side. The µVias that establish the electrical connection between the chip and the corresponding copper planes and carry most of the heat away from the chips can only be placed on the metal pads of the chips. Therefore, the surface area of the pads is instrumental in directing the

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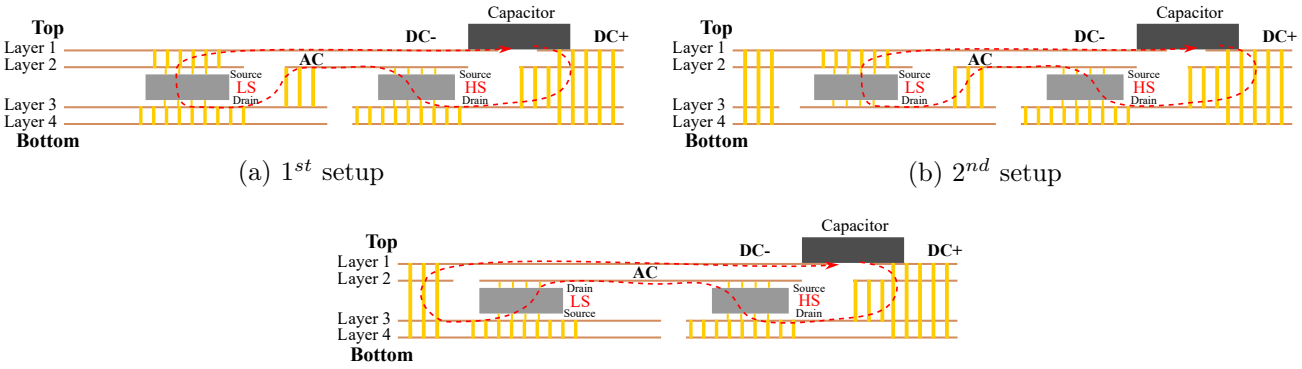
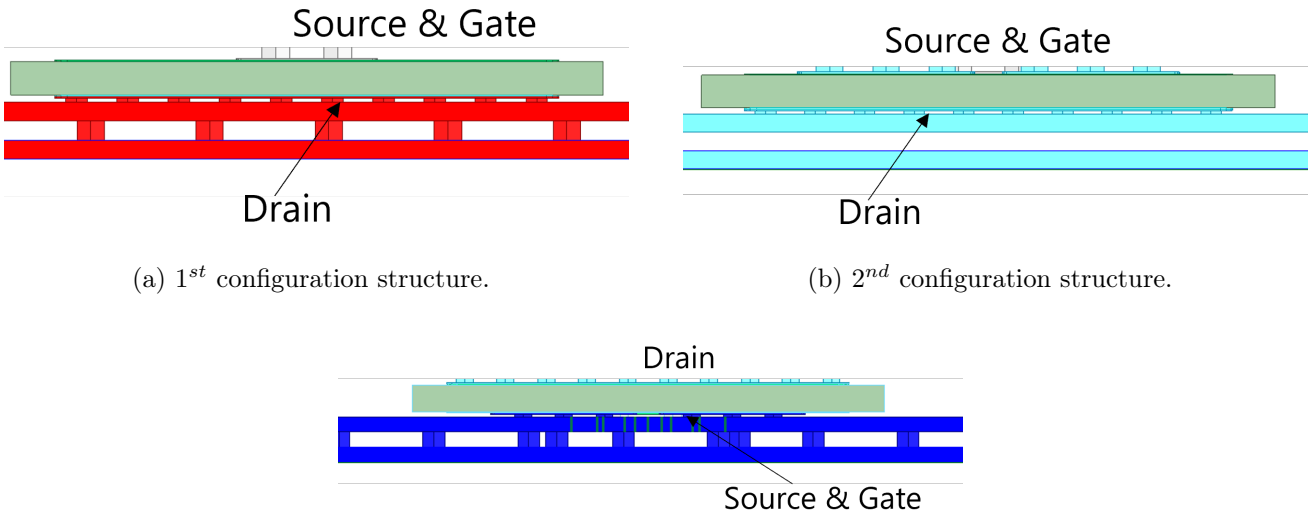


(a) 1^{st} setup

(b) 2^{nd} setup

(c) 3^{rd} setup

Figure 5.10: Analysed setups for the designing process



(a) 1^{st} configuration structure.

(b) 2^{nd} configuration structure.

(c) 3^{rd} configuration structure.

Figure 5.11: Cut view of the PCB structure at the level of Low-side power die for the 3 configurations.

heat generated by the power chip, ensuring efficient thermal performance within the established design parameters. Simply said, cooling of embedded chips is much more efficient on their drain side than on their source side, because much more µVias can be placed there.

The considered PCB stack consists of four layers of 105 µm copper.

This thickness dictates in particular the fabrication constraints for the size, spacing, and height of Vias. This is crucial, as these factors significantly influence thermal management performance. They effectively define a the volume of copper available for heat conduction between the die pad and the adjacent copper layers. This is described in [101].

Fig. 5.10 presents there possible arrangements for the half-bridge cell design. It

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shows a simplified schematic illustrating the Vias, connections of the copper plane for electrical potential, and the orientation of the power die, which can be in a "classic" orientation (source side facing up) or positioned upside down, commonly known as the "flip-chip" approach (source-side facing down). The three configurations in Fig. 5.10 correspond to designs cases which optimize some of the operational parameters (particularly thermal resistance or parasitic capacitance).

The 1^{st} configuration (Fig. 5.10a) represents the classic embedded setup, where the high-side and low-side power dies are positioned with their drain pad facing up, away from cooling side. In this case, the electrical potential of the fourth layer under the drain side can align with that of the drain, making it the AC point. This configuration allows for the efficient use of thermal Vias (as illustrated in Fig. 5.11a). It is expected not to be so attractive from a common-mode current point-of-view, as the AC track is directly placed at the bottom of the PCB, directly facing the baseplate (not shown here), and therefore forming large C_{AC}.

In contrast, the 2^{nd} configuration (Fig. 5.10b) has a different arrangement: the drain pad of the low-side chip does not share the same electrical potential as the 4^{th} layer, which is connected to a fixed potential to better shield the AC potential from the baseplate. As a result, thermal Vias cannot be used in this configuration (as illustrated in Fig. 5.11b). A much lower C_{AC} value can be expected, at the cost of a larger R_{th} for the bottom chip of the half-bridge.

The 3^{rd} configuration (Fig.5.10c) employs a flip-chip approach. This time, the AC potential is directly connected to the low-side chip drain through the 2^{nd} copper layer. This setup allows for thermal Vias between the 3^{rd} and 4^{th} copper layers, which are connected to the low-side source pad. This configuration not only enables shielding of the AC point but also facilitates the use of thermal Vias for both power dies. However, as the source and gate pads are much smaller than the drain pad (Fig. 5.9), a lower number of µVias can be used here (Fig. 5.11c). As a consequence, the R_{th} value will be larger for the low-side chip of the half-bridge than for the high-side switch.

3.2.3 PCB design considerations

Before implementing the layout variations presented above, this section addresses important considerations regarding copper surface located beneath the power MOSFETS. Indeed, the size of this copper pad plays an important rôle in both the thermal resistance and the parasitic capacitance. Optimizing it first reduces facilitates the design of the half-bridge layout.

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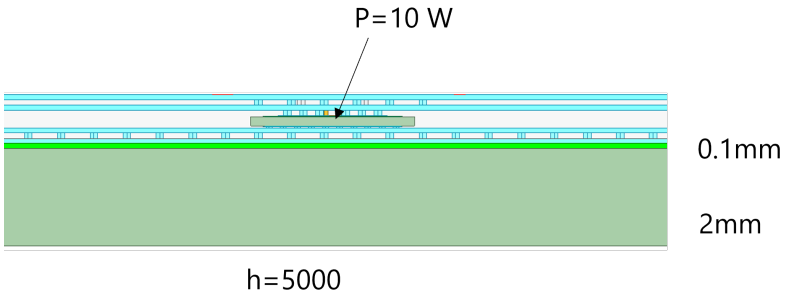

Figure 5.12: 3D model for the thermal resistance analysis vs. area (1^{st} configuration structure ,fig. 5.11a).

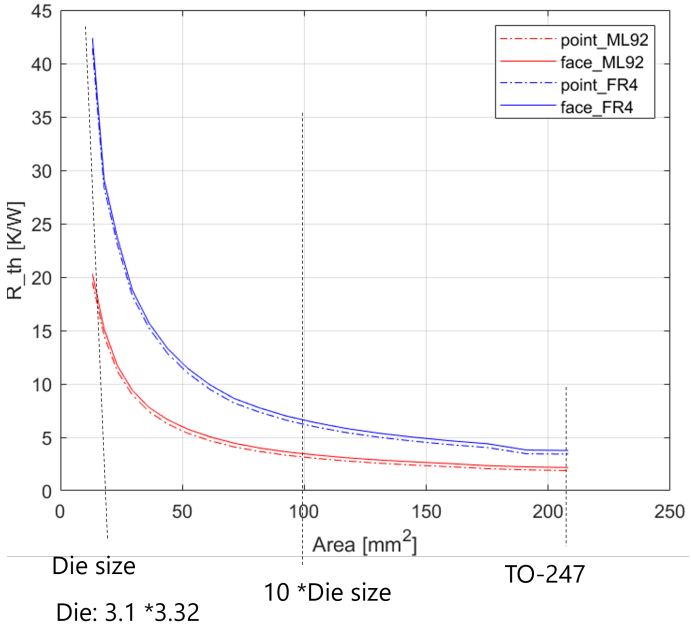

Figure 5.13: Thermal resistance vs area

To determine the optimal size of the copper pad attached to the drain surface of a power chip, an analysis of heat spreading resistance is conducted. This analysis uses Icepak parametric simulations iterating over different areas of the copper surface. The 3D model is depicted in Fig. 5.12, which corresponds to the configuration in Fig. 5.11a. The model features a power die surrounded by two copper layers on the top and two copper layers on the bottom, all connected by thermal Vias. The cooling system is modeled with a thermal interface material that has a thickness of 0.1 mm, along with a 2 mm aluminium plate with a heat-exchange coefficient of $5000\,\mathrm{W\,m^{-2}\,K^{-1}}$ at the bottom.

Figure 5.13 presents the thermal resistance calculated for two different dielectric materials: FR4 ($0.3\,\mathrm{W\,m^{-1}\,K^{-1}}$) and ML92 ($2\,\mathrm{W\,m^{-1}\,K^{-1}}$). This figure illustrates a sweep of the cooling area of copper, ranging from the die area to the effective area of the drain of a TO-247 package (14 mm x 17 mm). The dotted curve represents the temperature at the center top face of the die, while the solid curve indicates the

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	1^{st} setup	2^{nd} setup	3^{rd} setup
C_{DC+} [pF]	96.5	94.8	95
C_{DC-} [pF]	1.24	111.9	94.5
C_{AC} [pF]	99.7	7.6	6.4
L_p [nH]	0.723	0.717	0.778

Table 5.1: Half-bridge resulting parasitic capacitances and power loop inductance for each layout setup.

average temperature of the face.

For the rest of the study, a cooling area of 15 × 15 mm is used in the designs. This area is located on the asymptote where there is no further significant effect on the thermal resistance, which is comparable to the size of the TO-247 package. The data indicates that thermal resistance is significantly influenced by the area of copper through which heat is distributed.

3.2.4 Comparison of the 3 layout variants of a half-bridge.

The three variants depicted in Fig. 5.10 are designed, considering a 225 mm^2 heat spreading area per chip. Tab. 5.1 summarises the results of the simulation of the capacitances and the power loop inductance for the considered three half-bridge embedded PCB setups, obtained from the automatic model generation tool.

The stray inductance in the power loop does not show a significant difference between the first and second setups. However, the third setup exhibits an increase of approximately 7 to 8% when compared to both the first and second setups. This increase can be attributed to a slightly larger loop, as shown in Fig. 5.10c.

The 1^{st} setup features stray capacitances of $C_{DC+} = 96.5\,\text{pF}$ and $C_{AC} = 99.7\,\text{pF}$. This similarity is due to the equivalent copper surfaces designed for both the high side and low side of the half-bridge PCB, as illustrated in Fig. 5.10a. In contrast, there is a very low stray capacitance,C_{DC-}, measuring only 1.2 pF. This low value can be explained by the absence of any DC- surface facing the baseplate.

In contrast to the 1^{st} setup, the 2^{nd} and 3^{rd} setups show a clear shielding effect for the AC potential, resulting in low C_{AC} values of 7.6 and 6.4 pF, respectively. Moreover, C_{DC+} and C_{DC-}, are nearly identical in value (and with some refinement of the layout copper planes, can be made exactly equal). This is a very interesting feature, as dissimilar C_{DC-} and C_{DC+} values can contribute to the generation of common-mode current.

The results of the thermal analysis are presented in Tab. 5.2. Here again, the thermal analysis is conducted for both dielectric materials: FR4 ($0.3\,\text{W}\,\text{m}^{-1}\,\text{K}^{-1}$)

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	1^{st} setup		2^{nd} setup		3^{rd} setup	
	FR4	ML92	FR4	ML92	FR4	ML92
R_{th_HS} [K/W]	2.66	2.4 (-10%)	2.59	2.41 (-7%)	2.67	2.45 (-8%)
R_{th_LS} [K/W]	2.69	2.42 (-10%)	5.08	3.27 (-35%)	3.3	2.8 (-15%)

Table 5.2: Half-bridge resulting thermal resistance for each layout setup.

and ML92 ($2\,\mathrm{W\,m^{-1}\,K^{-1}}$).

As expected, configuration 1 (Fig. 5.10a), which includes thermal Vias paired with a drain pad at the bottom demonstrates the lowest thermal resistance on both the high and low sides when utilizing FR4 materials. Additionally, there is a 10 % reduction in thermal resistance when using ML92.

An imbalance in thermal resistance between the high and low sides is observed in the other two setups In the 2^{nd} setup, the low side switch exhibits the highest thermal resistance, which can be attributed to the lack of thermal Vias between the two bottom layers, hampering the heat flow to the cooling system. Conversely, the flip-chip configuration used in the 3^{rd} setup (Fig. 5.11c) has vials between the two bottom layers, but exhibits differences in the number of µVIas connecting the bottom side of the chips (as one chip is connected through its drain side, while the other is through its smaller source pads). Consequently, this configuration shows improved thermal resistance compared to the second setup (which has no thermal Vias) but performs worse than the first setup.

In conclusion, the 1^{st} setup demonstrates superior thermal management with minimal thermal resistance in the FR4 and ML92 configuration. However, it lacks the AC shielding advantages found in the other setups. The 2^{nd} setup does improve stray capacitance but does not perform as well in terms of thermal resistance, making it a less favorable option. Ultimately, the 2^{nd} setup effectively balances the need for lower stray capacitance and manageable thermal resistance in the case of the prepreg ML92, making an attractive choice for fabrication. With additional layout refinements, this setup can be further optimized to align thermal performance with effective shielding requirements in the design.

For our practical measurements, we choose to fabricate the 1^{st} and 3^{rd} setups, and the details of the tests can be found in Chapter 4 (DUTs ④ and ⑤).

3.3 Half-bridge with paralleled chips

This section presents the design process of a multichip half-bridge PCB, taking advantage of the detailed modelling of the layout parasitic to identify the best configuration. The modelling and simulation enable the estimation of parameters that

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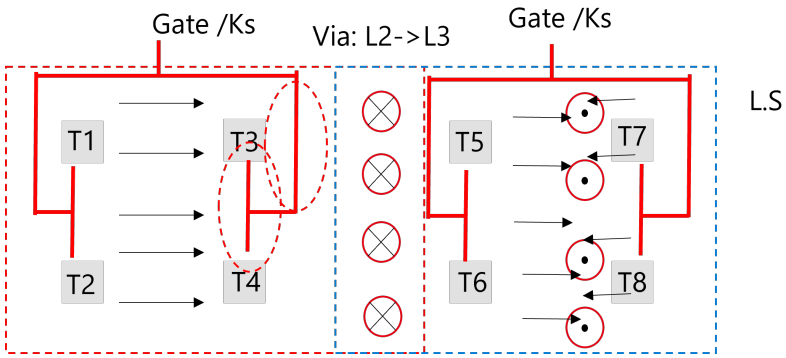

Figure 5.14: Multi-chip Half-bridge aligned arrangement of the power chips.

may be inaccessible even with a physical prototype (note that these designs have not been fabricated), offering valuable insights for optimizing designs.

3.3.1 Multi-Chip design challenges

Having more than one chip per switch significantly increases the complexity level of a design. Paralleling chips is helpful to increase the power of a converter, as the current is divided between several chips and the conduction losses are reduced (more details in section 2.2.2). However, when more power chips are added, a heat management problem arises as, with limited PCB dimensions, the heat transfer area is usually shared by the number of chips for the same dimension. In addition, routing the layout becomes more difficult due to the various constraints (in particular balancing the gate circuit or the power circuit to ensure uniform static and dynamic current distribution among the chips).

3.3.2 Multi-Chip Half-bridge designs

The analysis focuses on two distinct layout variants of the half-bridge cell circuit, each consisting of four chips (corresponding to the number of chips identified in the ANPC pre-design procedure). It was arbitrarily decided that the circuit would have the same outline as the single-chip half bridge presented above, to facilitate easy comparison (initially, we planned to have these multi-chip circuits built, but finally couldn't because of time constraints). Also, it is worth noting that to limit the design space, only the "classic" arrangement of the power chip is considered here (i.e. all chips are placed with their source facing up, and with vias between the two bottom layers for thermal management).

The first configuration of the multi-chip half-bridge is an "aligned" arrangement, illustrated in Fig. 5.14, in which the power dies are placed on a "grid" layout. In this representation, the gray rectangles are the chips, while the red lines indicate the

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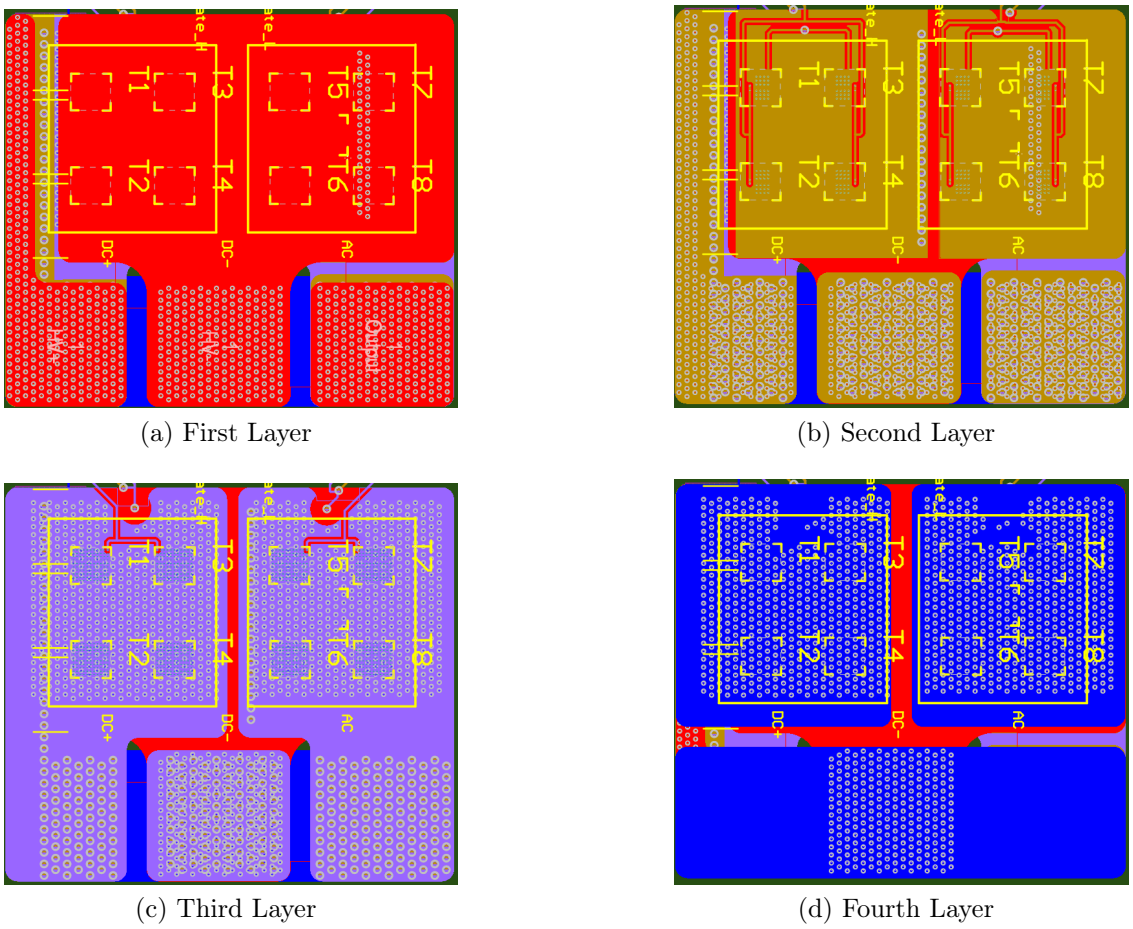

(a) First Layer

(b) Second Layer

(c) Third Layer

(d) Fourth Layer

Figure 5.15: A view of the 1^{st},2^{nd},3^{rd} and 4^{th} layers for the aligned chips layout arrangement.

approximate locations of the Kelvin source and gate tracks needed for controlling the switching operation. The black arrows show the expected direction of current flow (from the high-side, marked by the red dashed line, to the low-side, indicated by the blue dashed line). Additionally, the red circles illustrate the direction of the current flowing through the Vias to the upper or lower layers. Fig. 5.15 presents views of the second and third layers of the designed layout for the aligned chips scenario.

Here, special care is given to routing the gate tracks as symmetrically as possible, to ensure all chips are controlled similarly. The way the gate and kelvin source tracks are routed also has another effect: In the High-side, the current flow coming from T1 or T3 can not flow in a straight line to the AC potential (i.e. to the Vias located in the middle of the PCB) because the copper plane is cut by the kelvin source and the gate tracks. As a consequence, the current follows a longer path around this obstacle by going next to chip T4. This may translate in an increased electrical resistance for chips T1 and T3, generating an unbalance in the current distribution between the 4 parallel Dies.

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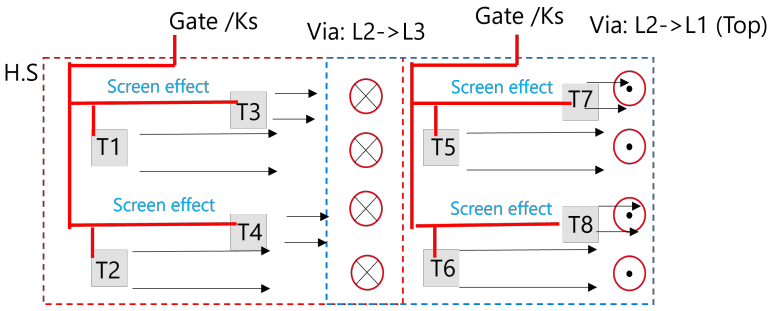
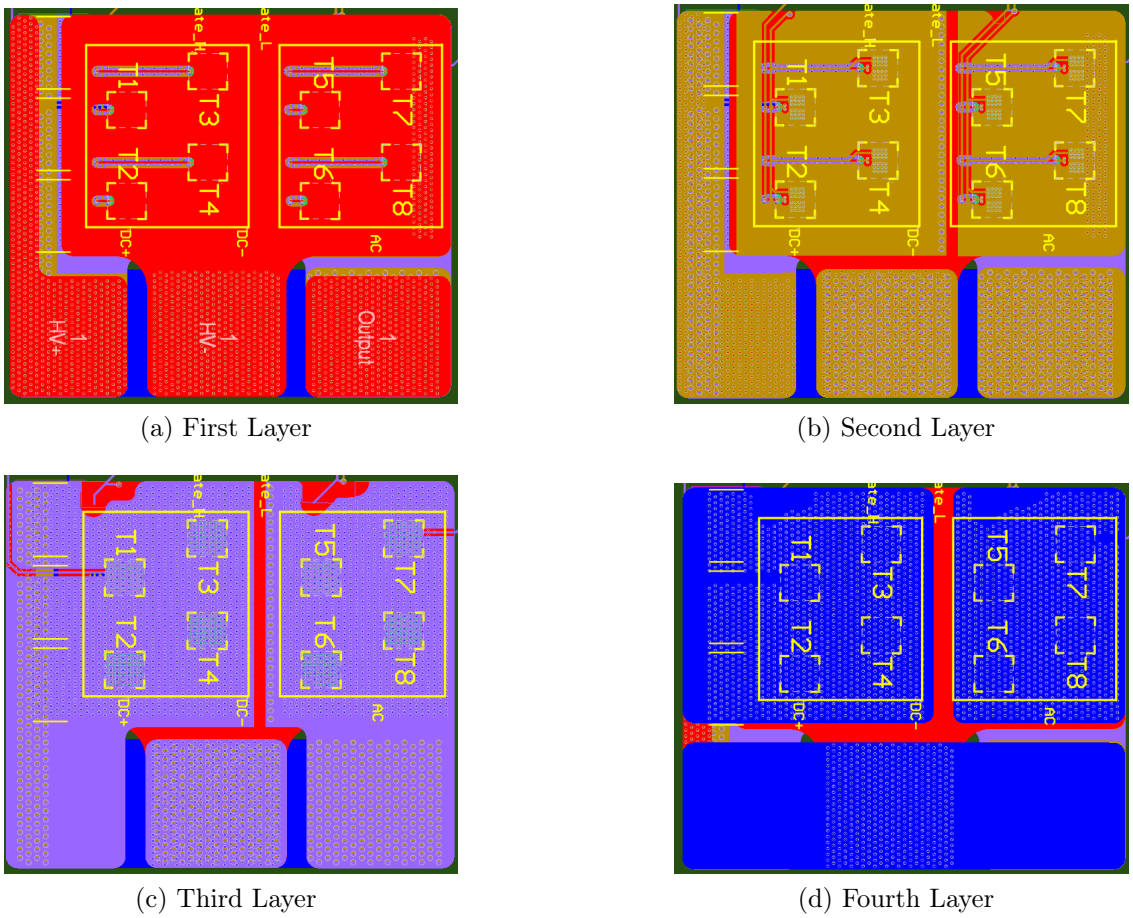


Figure 5.16: Multi-chip Half-bridge alternated arrangement of the power chips.



(a) First Layer

(b) Second Layer

(c) Third Layer

(d) Fourth Layer

Figure 5.17: A view of the 1^{st},2^{nd},3^{rd} and 4^{th} layers for the alternated chips layout arrangement.

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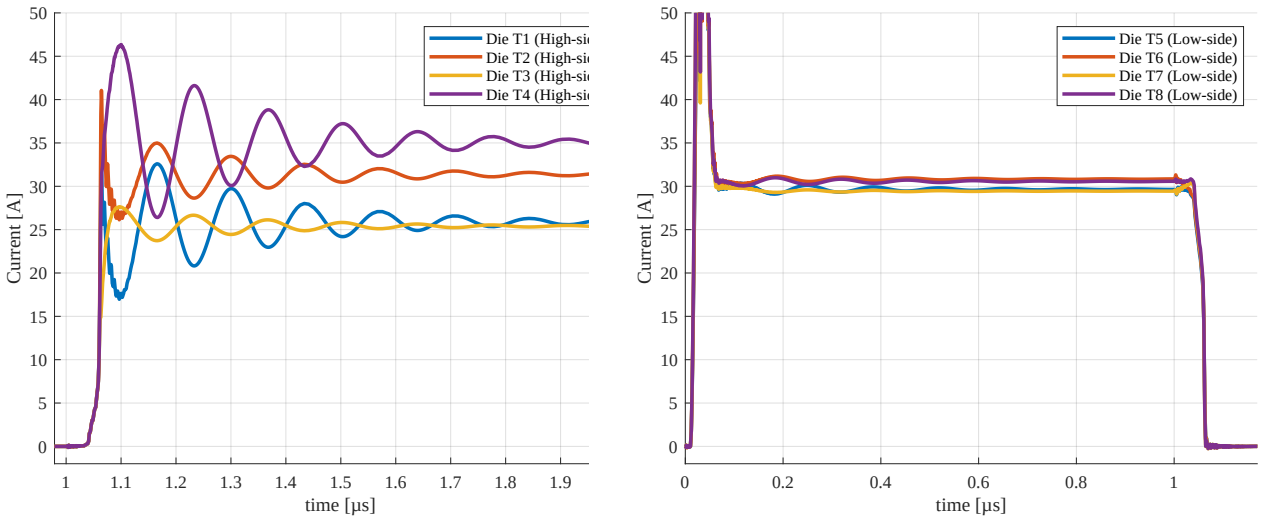

(a) (b)

Figure 5.18: Current curves : (a) for the high-side and (b) for the low-side of the half-bridge during the switching period with aligned chip arrangement.

	High Side	**Low Side**
Aligned Chips layout	$I_{T1} = 26.03A$ $I_{T3} = 25.36A$ $I_{T2} = 31.43A$ $I_{T4} = 34.94A$	$I_{T5} = 29.63A$ $I_{T7} = 29.44A$ $I_{T6} = 30.84A$ $I_{T8} = 30.57A$
Alternated Chips layout	$I_{T1} = 27.32A$ $I_{T3} = 29.05A$ $I_{T2} = 30.45A$ $I_{T4} = 30.86A$	$I_{T5} = 29.57A$ $I_{T7} = 29.43A$ $I_{T6} = 31.3A$ $I_{T8} = 30.19A$

Table 5.3: On-State Drain Current (I_D) Through Each MOSFET for Both Aligned and Alternated Chip Layouts.

Fig. 5.16 illustrates the second layout, which features a die arrangement and gate track design intended to facilitate the current flow. The corresponding second and third copper layers are shown in Fig. 5.17. This design creates pathways for the current by shifting the position of the first column of dies downward and the adjacent column upward, allowing the placement of gate and source tracks without obstructing the power current. In this variant, however, it is worth noting that the gate circuit layout is no longer symmetrical, which may yield unbalanced gate signals between the power dies.

3.3.3 Simulation results

Both circuits configurations are processed according to our automatic model generation system. The electrical models of the half-bridges are then inserted in a double-pulse circuit simulation run in LTSpice. In particular, we focus on the current flowing through each MOSFET die, a parameter which would be impossible to measure on a prototype without strongly altering its operation.

For the first configuration ("aligned" chips), the drain current waveforms in each

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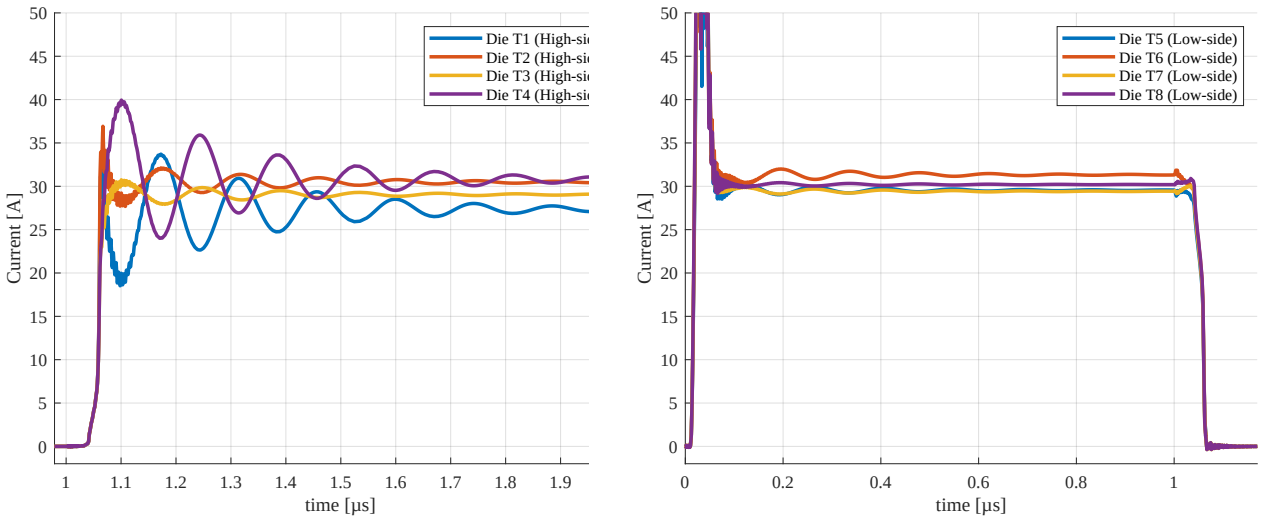

(a) (b)

Figure 5.19: Current curves : (a) for the high-side and (b) for the low-side of the half-bridge during the switching period with alternated chip arrangement.

chip are shown in Fig. 5.18. The results for the "alternated" chip configuration are shown in Fig. 5.19. The steady-state current values are also presented in Tab. 5.3.

For the high-side switch of the aligned design, T_1 and T_3 carry lower drain currents of 26.03 A and 25.36 A respectively, while T_2 and T_4 exhibit higher drain currents (31.43 A and 34.94 A). On the low side, we observe a more balanced current distribution, with measured values of 29.63 A, 30.84 A, 29.44 A, and 30.57 A for T_5, T_6, T_7 =, and T_8, respectively. This confirms that the longer path followed by the drain current of T_1 and T_3 (and caused by the gate circuit layout) actually results in a significant unbalance between the high-side chips.

The imbalance is much more limited among the chips of the high-side switch in the alternated variant. The currents in the high-side chips are now more uniform, ranging from 27.32 A to 30.86 A. Similarly, the low-side chips show good balancing, ranging from 29.57 A to 31.3 A. Furthermore, no dynamic unbalancing effect is observed, as it may have been the case because of the slightly dissimilar gate path. Overall, the peak current in the most stressed chip (T_4, at 40 A, Fig. 5.19) remains much lower than for the aligned design, despite its symmetrical gate layout (46 A in chip T_4, Fig. 5.18).

Table 5.4 presents the simulated thermal resistance matrix for two different chip placement strategies: the aligned configuration and the alternated configuration. Each matrix includes self-heating terms (diagonal elements) and cross-coupling terms, quantifying the mutual thermal interaction between chips T1 to T4. In both layouts, the diagonal elements (highlighted in blue) correspond to the thermal resis-

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		T1	T2	T3	T4
Aligned Chips layout	**T1**	2.85	0.54	0.6	0.32
	T2	0.54	2.88	0.31	0.58
	T3	0.6	0.31	2.8	0.53
	T4	0.32	0.58	0.53	2.78
Alternated Chips layout	**T1**	2.75	0.69	0.72	0.58
	T2	0.69	2.7	0.3	0.7
	T3	0.72	0.3	2.73	0.67
	T4	0.58	0.7	0.67	2.68

Table 5.4: High-side thermal resistance matrix including cross-coupling effects extracted by simulation (in °C/W)

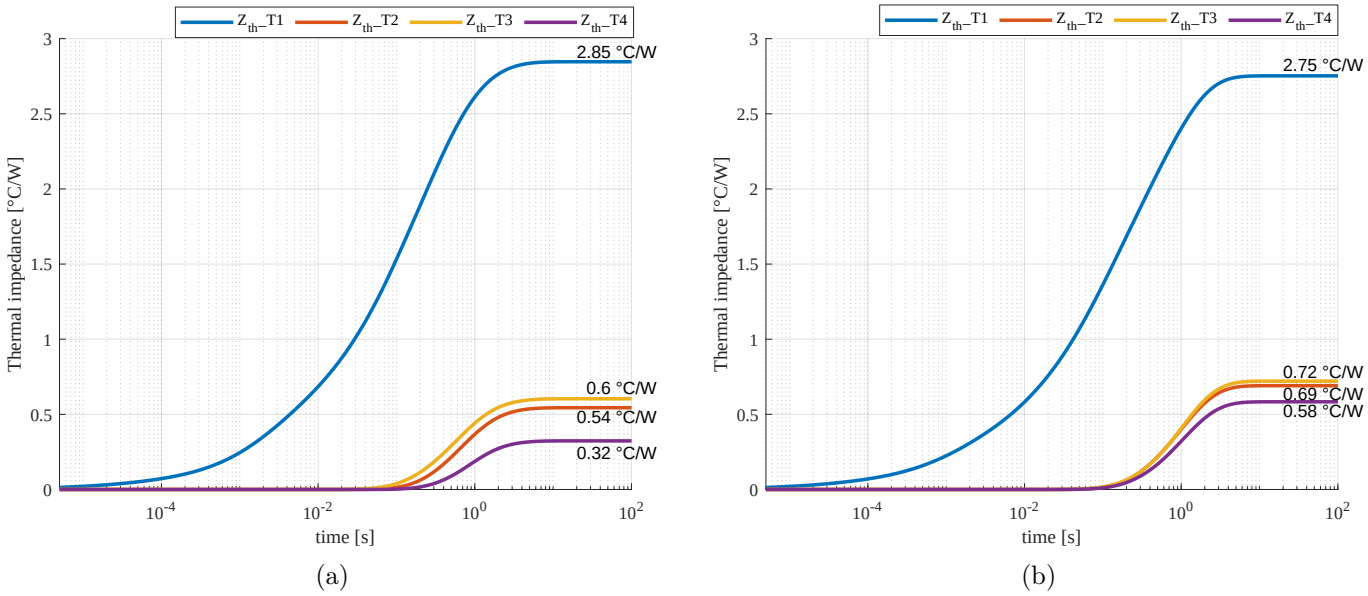

Figure 5.20: Thermal impedance of the 4-chip Half-bridge PCB : (a) Aligned chip configuration and (b) Alternated chip arrangement.

tance from each chip to the ambient environment. The aligned configuration exhibits slightly higher self-resistances, with maximum values reaching 2.88 °C/W (T2), compared to 2.75 °C/W in the alternated configuration (T1). The off-diagonal terms reveal the degree of thermal coupling between the chips. The alternated configuration consistently shows higher mutual thermal resistances for example, 0.72 °C/W between T1 and T3, and 0.70 °C/W between T2 and T4, while in the aligned configuration, these values remain below 0.60 °C/W. This indicates stronger thermal interactions in the alternated layout, likely due to closer physical proximity or increased shared heat conduction paths through the PCB.

3.3.4 Conclusions on chip parallelling

The simulation results demonstrate that the alternated layout configuration offers the most favorable overall performance. The corresponding PCB design is illus-

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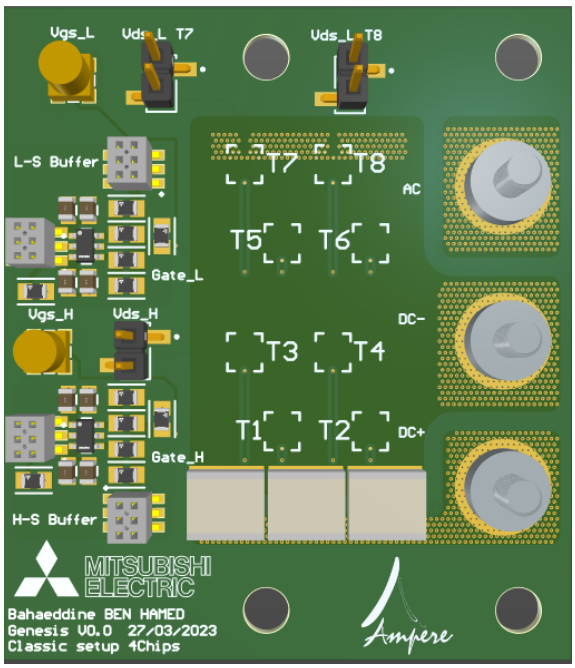

Figure 5.21: Visual Representation of a 4-Chip Half-Bridge PCB Design Generated by eCAD

trated in Fig. 5.21. This decision is grounded in the distinct advantages identified during the comparative evaluation of both layout strategies.

Notably, the alternated arrangement effectively addresses the current imbalance issues observed in the aligned configuration, where chips T_1 and T_3 were subjected to significantly lower currents than T_2 and T_4. Such asymmetries can lead to sub-optimal utilization of the switching devices and increased thermal stress on specific components. In contrast, the alternated configuration promotes a more uniform current distribution among all chips, largely due to its more symmetric conductor paths. This improved electrical balance is essential for enhancing system reliability and thermal homogeneity.

While the aligned layout exhibits slightly superior thermal decoupling, evidenced by lower cross-coupling thermal resistances, the alternated configuration was chosen for the final implementation. Targeted thermal optimizations were applied to offset the relatively higher thermal coupling inherent to this arrangement. These include enhancing copper spreading areas and optimizing the placement of thermal vias.

3.4 Design of an ANPC PCB

3.4.1 Design variants

After investigating single- and 4-chip, 2-level, half bridge structures, the next step towards the full ANPC inverter described at the beginning of the chapter is the design of a single-chip-per-switch, ANPC half bridge. Here, the objective is to

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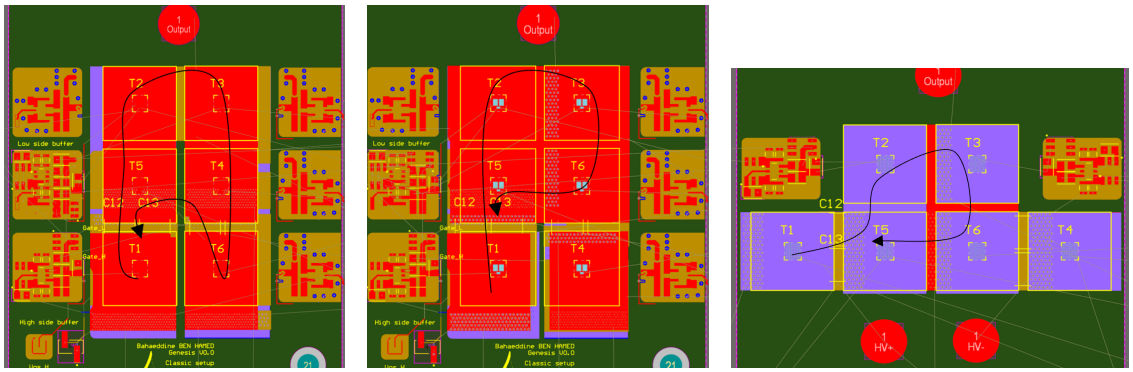

(a) ANPC layout prototype 1 (b) ANPC layout prototype 2 (c) ANPC layout prototype 3

Figure 5.22: ANPC layout prototypes: current path representation with black arrows in the positive loop ($L2^{+}$: as illustrated in figure 5.7a).

find the best position for the power chips, as there are many more possibilities with 6 switches than there are with a regular 2-switch half-bridge. To limit the design space, only "classical" chip orientation (source-side facing up) is considered here, and a fixed copper-pad size is used under the drain of each chip (the same as for the 2-level half-bridge PCB). Because parasitic capacitances and thermal resistances are similar to those of the half-bridge structure, we focus here on stray inductance. These may be relatively larger than for the 2-level half-bridge, as the PCB footprint is significantly larger to host 6 chips.

As described in the appendix, ANPCs modulation strategies involve different switching sequences, which means that the power loops are more complex than with a 2-level inverter. In section 2.3, we presented the "small" and "big" loop inductances which can be identified in the ANPC operation.

Considering the many constraints (distance between chip and gate drive circuit, footprint of the power connectors, drain pad size of the chips), 3 configurations are identified to implement an ANPC half-bridge (Fig. 5.22.

3.4.2 Simulation results for ANPC layout variants

The 3 layouts variants are processed to generate Q3D models, and the loop inductances are computed from the Q3D simulation results. The results are presented in Tab. 5.5, for all three designs, small and big loops (with two values for each, as there actually are two small and big loops, depending on load current direction).

For small loop inductance, prototype 1 has values of 0.807 nH for L_1^{+} and 0.808 nH for L_1^{-}. prototype 2 shows increases of approximately 4.9 % for L_1^{+} (0.847 nH) and 10.5 % for L_1^{-} (0.893 nH) compared to prototype 1. prototype 3 demonstrates

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	Current direction	prototype 1	prototype 2	prototype 3
Small Loop inductance [nH]	L_1^+	0.807	0.847	0.63
	L_1^-	0.808	0.893	0.621
Big Loop inductance [nH]	L_2^+	8.61	2.06	1.65
	L_2^-	6.32	1.72	1.42

Table 5.5: Power loop inductance results for the three proposed ANPC designs, classified by the directions of current flow in both the small and large loops.

notable reductions, with 0.63 nH for L_1^+ and 0.621 nH for L_1^-, reflecting decreases of about 21.8 % and 23.2 %, respectively. Overall, all these values remain small and would most likely be completely acceptable in operation.

The difference between the designs are more obvious when looking at he big loops: prototype 1 presents values of 8.61 nH for L_2^+ and 6.32 nH for L_2^-. Prototype 2 has significantly lower loop inductances, reducing L_2^+ by 76.1 % (down to 2.06 nH) and L_2^- by 72.7 % (1.72 nH). Prototype 3 offers even lower values with 1.65 nH for L_2^+ and 1.42 nH for L_2^-, reductions of 80.8 % and 77.5 %, respectively.

These results illustrate that while prototype 1 has the highest inductance, prototype 2 and especially prototype 3 show substantial performance enhancements. Because chip orientation and drain pad size are identical, all three prototypes are expected to exhibit the same parasitic capacitance and R_{th} values.

However, while prototype 3 offers the best performance regarding layout stray inductance, it requires substantial separation between the input DC connectors, DC+ and DC-. Indeed, these are located on two opposite sides of the PCB, specifically at the locations of T1 and chip T4, as illustrated in Figure 5.22c. This arrangement means that significant additional power loop inductance would be introduced when connecting the ANPC PCB to a busbar. It highlights a limit of the proposed modelling solution, where a detailed model is generated for the PCB layout, with no consideration to the environment of the board.

Once this practical aspect of connectivity is taken into account, prototype 2 emerges as the most favorable option. Its design allows for a mechanically feasible configuration with the DC+ and DC- connectors positioned closer together, facilitating the integration of the busbar PCB while minimizing additional loop inductance. This strategic choice ultimately balances performance with practical assembly requirements, ensuring optimal functionality in the power converter design. The final design is presented in Fig. 5.23.

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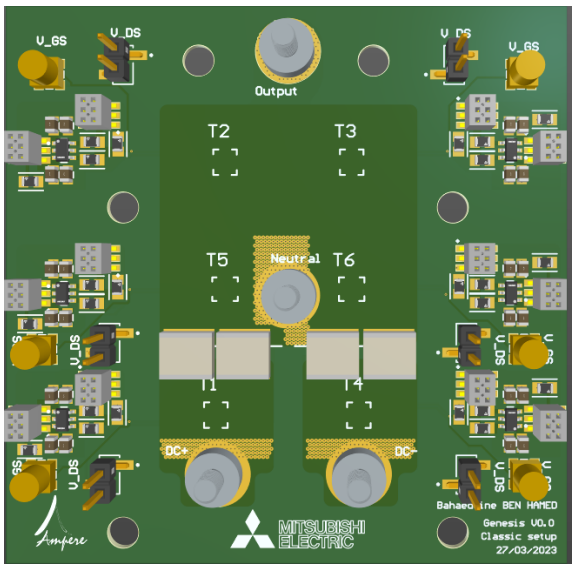

Figure 5.23: Chosen Layout Design for the ANPC PCB (74mm x 74mm Dimensions)

3.4.3 Conclusions on ANPC design

In conclusion, the design workflow allows to rapidly compute the loop inductances of several design variants, allowing for informed design choices to be made. With up to 80 % reduction in loop inductance from one variant to another, it is found that the implementation may have a significant effect on the converter performance.

However, a limitation is found in the fact that stray inductance is not only caused by the PCB layout, but also by the location of its connector and the relation with the busbar and decoupling capacitors. This means that additional work is required to manage multi-board designs.

4 Reflexions on the use of the model-generation workflow

In this chapter, the model-generation workflow presented previously is put to use on realistic cases, to identify its relevance to a power electronics engineer. While the previous sections focused on the results, we focus here on the practical aspects of the tool. This allows to identify key advantages of the approach, but also some of its limitations.

4.1 Practical use of the workflow

Fig. 5.24 presents an measurement of the time taken by the various steps in the generation of electrical and thermal models, for the various cases evaluated in

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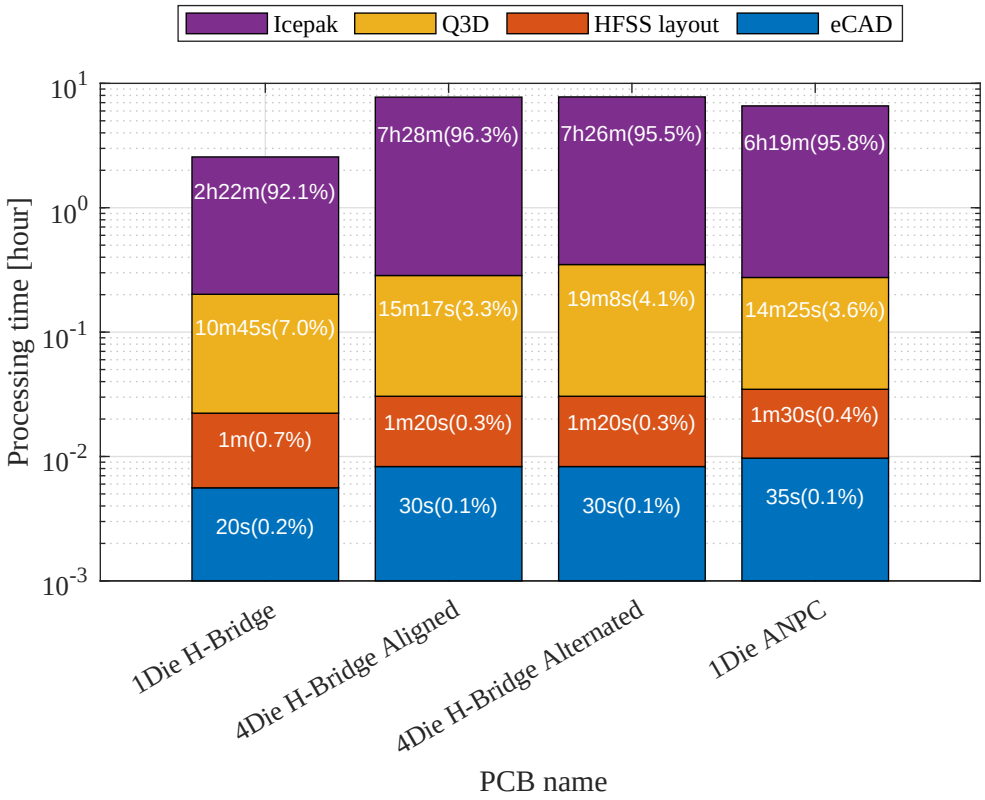

Figure 5.24: Breakdown of the time taken by the model-generation workflow. Note that the vertical scale is logarithmic.

this chapter. It shows that in all cases, the IcePak step takes up most of the time (typically 95 % of the total time), while the other steps are all executed in less than 21 min. Even though we limited geometry simplification to relatively simple techniques (replacing the vias with copper blocks; using the faceting features of Ansys HFSS Layout), the calculations and models remain manageable in terms of computing time for the electrical model. This is not true for the generation of the thermal model, which would require some additional simplification steps to make the FEM simulation shorter. Various solutions exist for this, such as a simplification of the copper layers based on averaging the copper density and using shell elements for the thin copper layers [109]).

Obviously, the model generation still takes a negligible time when compared to the production of a hardware prototype (which, in the case of PCB embedding technology, typically takes several months). It also allows to access some parameters (such as junction temperature or drain current) which would be difficult to acquire experimentally.

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4.2 Limitations

Over the duration of the thesis, the code base which forms the workflow (C++ code executed by Altium and VBScript running in ANSYS) was found to be fragile, and any upgrade in either Altium or ANSYS caused the model generation to fail. This is not a major issue for this work, which is intended as a proof of concept, but highlights the difficulty in getting complex pieces of software to work together without relying on strict specifications or standards.

Further work should be based on open standards (such as IPC 2581 for the description of a PCB), to make it easier to change any piece of the software chain (for example using different eCAD software). As the workflow is built upon several proprietary software platforms, which are not open-source, multiple licenses are required for full functionality. This adds to the cost and complexity of utilizing the tool in practice, and the possibility of exchanging some of the software with open-source alternatives would be usefull.

One of the primary concerns at the moment is the meshing quality when using Icepack. In some cases, the mesh generation can result in low-accuracy outcomes, suggesting that improvements in this aspect are essential to achieve reliable thermal simulations. Additionally, the creation of the LTspice schematic, while functional, is not fully optimized. Issues have been noted regarding the simulation of certain models, particularly when existing models devices are unavailable or inadequately defined. This limitation can lead to convergence problems, such as those encountered with the output buffer of the gate drive circuits in our examples, where proper convergence could not be achieved (the buffers were replaced with piecewise linear voltage sources). As circuit complexity escalates, the duration of simulations increases significantly, which can hinder the useability.

Another limitation of the proposed model-generation system is its lack of awareness regarding the environment of a PCB: boundary conditions must be defined manually: heat exchange coefficients, presence of metal ground, or even the type of electrical signals which are connected to the board. This is a consequence of using data from the eCAD software, which focuses on the board itself, and is not too much of a problem when analyzing a single-board system, as it only require a moderate amount of additional information. This is a bigger issue when considering a multi-board system, as coupling (for example stray inductance, as discussed for the ANPC case) is not considered. It is unclear how this problem could easily be addressed without fundamental changes to how the PCB design is described, though.

Finally, the accuracy of the design tool is limited by the differences between the

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design and the fabricated prototype, as was demonstrated for for the layer thickness, and shape/dimensions of the vias.

In conclusion, while the developed tool has promising capabilities for optimizing power converter designs, addressing the challenges related to meshing accuracy, schematic creation, simulation stability, and software dependencies will be crucial for enhancing its overall performance and usability in practical applications.

Conclusion

In conclusion, this chapter has detailed the design and analysis of various converter PCBs utilizing embedded technology for advanced configurations, such as the active neutral point clamped (ANPC) and half-bridge cells, with both multiple and single chips. Through the application of our innovative virtual prototype automatic generation tool, we have effectively simulated and examined critical factors influencing system performance, notably thermal characteristics and electromagnetic aspects, including stray inductances and capacitances.

The coupled simulations provided invaluable insights, enabling us to evaluate the system's behavior under varying operational conditions and configurations. This approach facilitated a comprehensive understanding of the interplay between electrical performance and thermal management, which is crucial for optimizing design iterations.

Moreover, the methodology employed emphasizes the importance of a meticulous design workflow, incorporating detailed assessments of power loop inductance, stray capacitance, and thermal impedance, as well as comparisons of different prepreg materials. This rigorous process not only enhances reliability but also significantly reduces the risks associated with the fabrication phase.

Overall, the insights gained from our studies underscore the necessity for advanced virtual prototyping in modern PCB design, ultimately paving the way for more efficient, reliable, and robust converter systems. The findings presented in this chapter contribute to the broader field of embedded power electronics, offering a foundational approach for future developments in high-performance converter designs.

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Conclusion

Power converters are inherently complex systems that involve tightly coupled, multi-physics phenomena, including in particular electromagnetic behavior and thermal effects. Their heterogeneous nature, involving various components, materials, voltage levels, and cooling strategies, makes the design process particularly challenging. Moreover, the increasing demands for performance, miniaturization, and reliability in power electronics, along with stricter design constraints, amplify the complexity and cost of the development process.

A review of the state-of-the-art reveals significant advances in the fields of simulation and electronic computer-aided design (ECAD). Existing tools have become increasingly accurate, user-friendly, and capable of modeling detailed behaviors. However, the workflow is fragmented, as different tools are often dedicated to specific tasks, requiring multiple expert profiles, complex data handling, and software licenses. Incompatible data formats, inconsistent modeling abstractions, and limited standardization hinder the conjoint operation of the tools. This leads to inefficiencies in the design flow, especially when iterating between a converter's electrical, thermal, and mechanical aspects.

In particular, the fabrication phase introduces a bottleneck: hardware prototyping for advanced technologies (e.g., embedded PCBs) is costly and time-consuming, with lead times extending over several months. In such contexts, virtual prototyping offers a promising alternative. However, this approach has not yet reached the level of maturity and integration seen in other domains such as microelectronics, where design automation and digital twins are already widely adopted.

In this PhD work, we addressed this gap by developing a proof-of-concept of a design tool to automate the generation of virtual prototypes for power converter PCBs. The goal was to create an end-to-end workflow that could reduce reliance on physical prototyping by offering reliable electro-thermal simulation models directly

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from the PCB layout. The tool integrates a sequence of model generation steps: layout extraction, geometry simplification, electromagnetic modeling, thermal finite element modeling, and netlist generation for circuit simulation.

This confirmed the relevance of the models generated, both for simple and relatively complex power converter layouts. The tool was able to automatically generate detailed models, and to simulate parameters that are otherwise difficult to measure, such as junction temperature or switching waveforms at the semiconductor level. Electrical and thermal models were successfully validated against measurements on real hardware prototypes, supporting the credibility of the proposed workflow.

A performance analysis revealed that the bottleneck in the model generation process lies in the thermal simulation step (specifically in IcePak), which takes up to 95 % of the total computation time. Nonetheless, this time remains negligible compared to a full hardware prototyping cycle. Moreover, the ability to explore designs before fabrication and to access otherwise hidden variables highlights the practical value of this virtual prototyping approach.

Several limitations were also identified. First, the current implementation depends on proprietary software (Altium, ANSYS), resulting in fragility when these platforms are updated, and limiting the portability and sustainability of the workflow. Future work should explore adopting open standards such as IPC-2581 for PCB data representation, enabling better interoperability and facilitating the integration of open-source components. Second, certain technical challenges remain, such as the generation of less computationally-intensive thermal models, incomplete automation of circuit netlist generation, and convergence issues in transient circuit simulations when accurate device models are unavailable. Additionally, the tool currently lacks environmental awareness: it requires manual input of boundary conditions, which becomes a limiting factor when scaling to multi-board systems.

Despite these constraints, the tool demonstrates a promising new direction for the power electronics community. It contributes to making the design process more vertical and unified, reducing the number of iterations between the design and fabrication phases. It also provides a basis for a new generation of design environments where virtual prototypes can serve as trustworthy surrogates for physical ones, especially in early design stages or for advanced technologies where manufacturing is slow and costly.

In conclusion, the results obtained in this thesis confirm the potential of automated, layout-based virtual prototyping in embedded power electronics. The tool developed acts as a proof-of-concept showing that it is possible to derive coupled

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electro-thermal models from PCB data in a time-efficient and semi-automated manner. While challenges remain, the methodological framework and experimental findings offer a solid foundation for further work. Bridging the gap between ECAD tools and system-level simulation remains a strategic objective for the future, with the promise of significantly accelerating innovation cycles and improving the reliability of power electronic systems.

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Appendix A

ANPC

1 Active Neutral Point Clamped (ANPC) Topology

This section presents four Pulse Width Modulation (PWM) strategies applied to the ANPC topology. These strategies differ in the number and nature of the zero switching states and the associated switching patterns. The goal is not to reduce the overall converter losses but to distribute them more evenly across the semiconductor devices, thereby improving thermal management and reliability.

1.1 NPC circuit

The 3L-NPC is the most popular 3L topology (Fig.A.1a). It is composed by four bidirectional switches and two clamp diodes. Each switch is capable to support a voltage equal to $V_{DC}/2$. The supply voltage source V_{DC} is made of two secondary sources serially connected.

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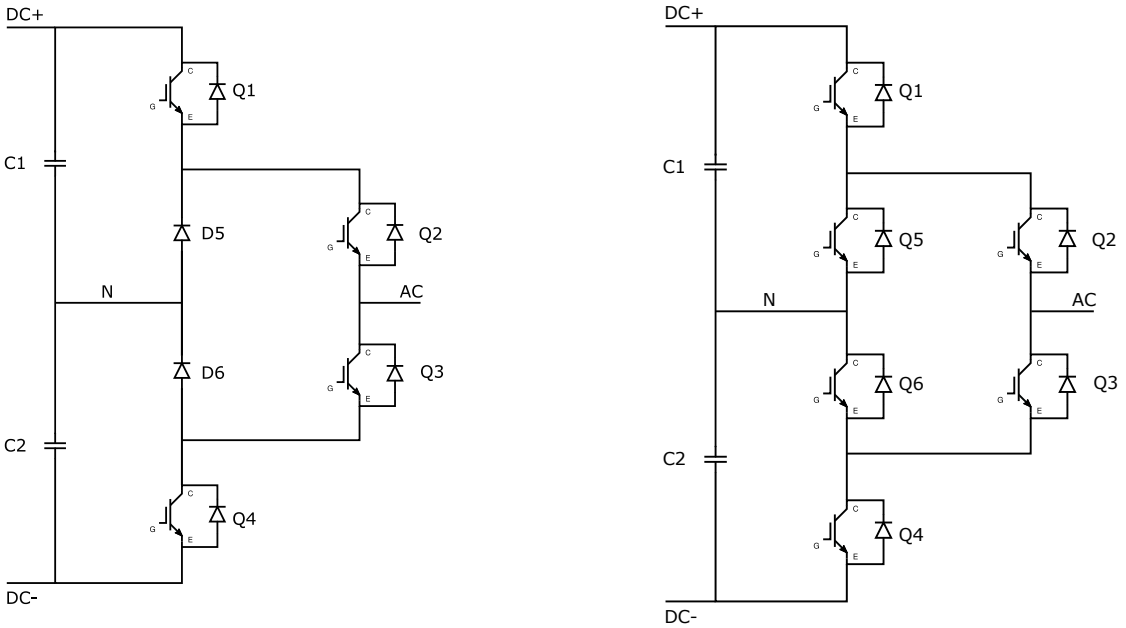
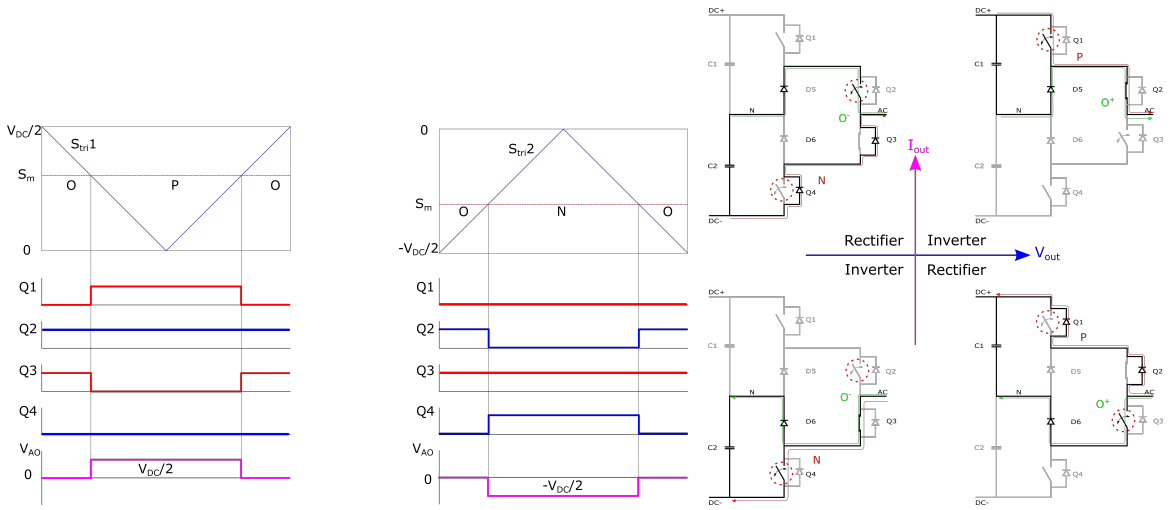


(a) NPC circuit (b) ANPC circuit

Figure A.1: ANPC&NPC multilevel circuit

Output Voltage (V_{AO})	Switching State	Switching Sequence			
		Q1	Q2	Q3	Q4
$-V_{DC}/2$	N	0	0	1	1
0	O	0	1	1	0
$V_{DC}/2$	P	1	1	0	0

Table A.1: Table of states for the NPC-topology



(a) (b)

Figure A.2: NPC

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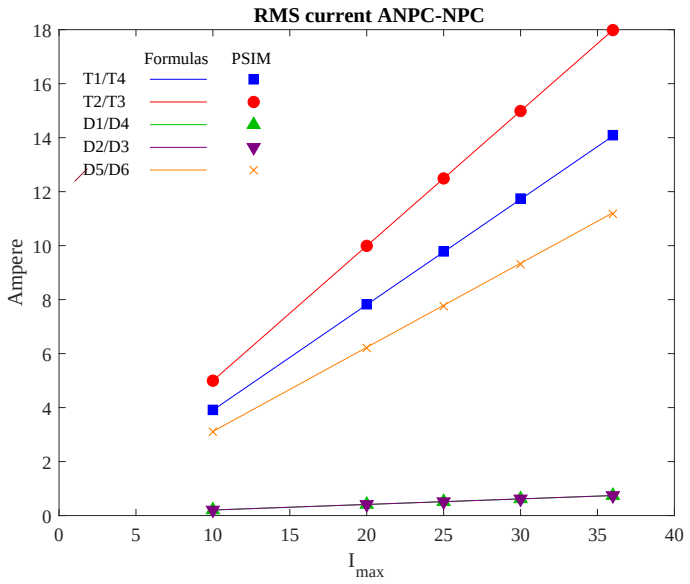

Figure A.3: NPC circuit

Switch	Switching Loss Formula
Q1/Q4/D5/D6	$\frac{1}{2\pi}[a_{sw}I^2[\pi-\varphi+\frac{sin(2\varphi)}{2}]+b_{sw}I\sqrt{2}(1+cos(\varphi))+c_{sw}(\pi-\varphi)]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Q2/Q3/D1/D4	$\frac{1}{2\pi}[a_{sw}I^2[\varphi-\frac{sin(2\varphi)}{2}]+b_{sw}I\sqrt{2}(1-cos(\varphi))+c_{sw}\varphi]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Switch	Switching Loss Interval
Q1/Q4/D5/D6	$(\varphi \rightarrow \pi)$
Q2/Q3	$(\pi \rightarrow \pi+\varphi)$
D1/D4	$(0 \rightarrow \varphi)$

Table A.2: NPC switching loss formulas

1.2 PWM1 Strategy

In the PWM1 strategy (see Fig. A.4), the switches in cells 1 and 3 operate at a high frequency, while the switch in cell 2 operates at the fundamental frequency, which is the frequency of the reference voltage. At any given moment, only one cell is actively switching.

Table A.3 summarizes the switching states and their corresponding output voltage levels. The zero voltage level can be achieved using two distinct states: $O-$ and $O+$, which correspond to negative and positive reference voltages, respectively.

Output Voltage (V_{AO})	Switching State	Switching Sequence					
		Q1	Q2	Q3	Q4	Q5	Q6
$-V_{DC}/2$	N	0	0	1	0	0	1
0	O^-	0	0	1	1	0	0
	O^+	0	1	0	0	1	0
$V_{DC}/2$	P	1	1	0	0	0	0

Table A.3: Table of states for the ANPCtopology PWM_1 control

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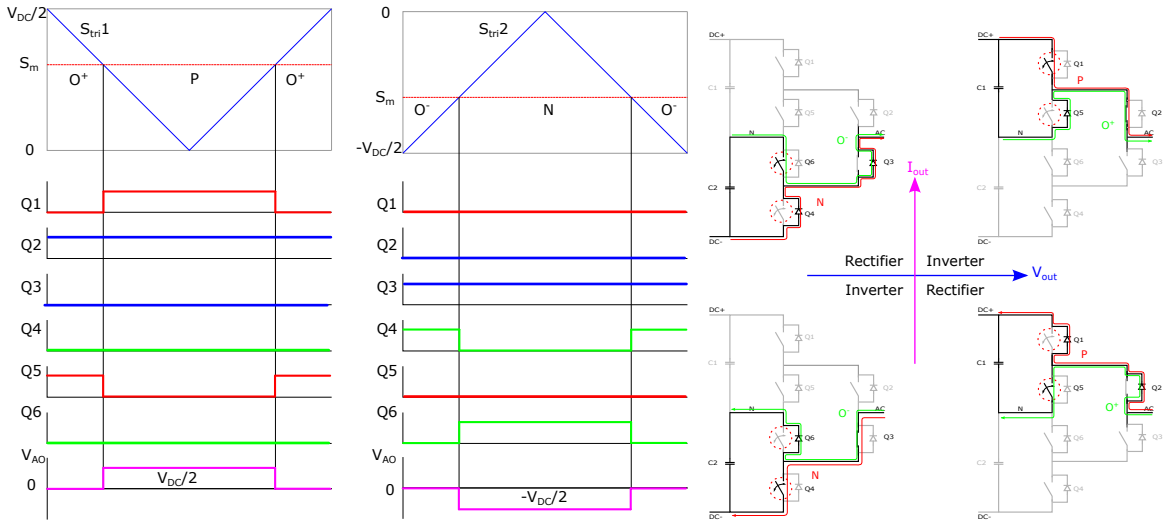

(a) a (b) b

Figure A.4: ANPC1

Switch	Switching Loss Formula
Q1/Q4/D5/D6	$\frac{1}{2\pi}[a_{sw}I^2[\pi-\varphi+\frac{sin(2\varphi)}{2}]+b_{sw}I\sqrt{2}(1+cos(\varphi))+c_{sw}(\pi-\varphi)]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Q2/Q3/D2/D3	0
Q5/Q6/D1/D4	$\frac{1}{2\pi}[a_{sw}I^2[\varphi-\frac{sin(2\varphi)}{2}]+b_{sw}I\sqrt{2}(1-cos(\varphi))+c_{sw}\varphi]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Switch	Switching Loss Interval
Q1/Q4/D5/D6	$(\varphi\rightarrow\pi)$
Q5/Q6/D1/D4	$(0\rightarrow\varphi)$

Table A.4: ANPC-PWM1 switching loss formulas

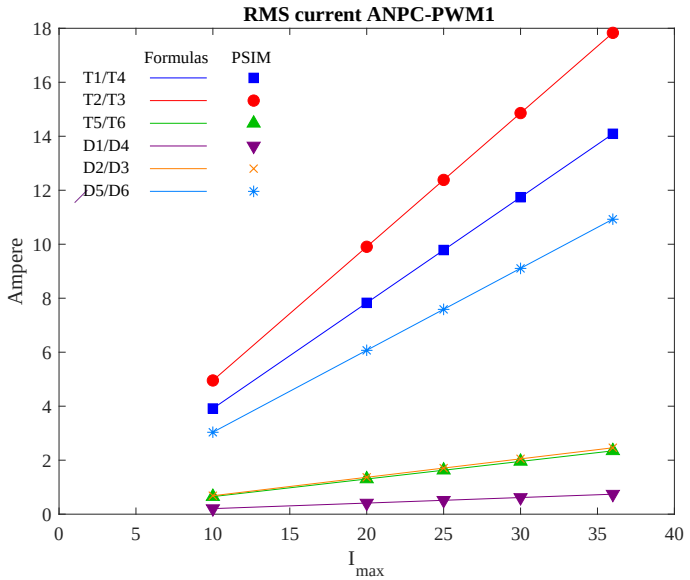

Figure A.5: ANPC-PWM1 circuit

The switching losses for this strategy are detailed in Table A.4, indicating which switches are active and during which intervals.

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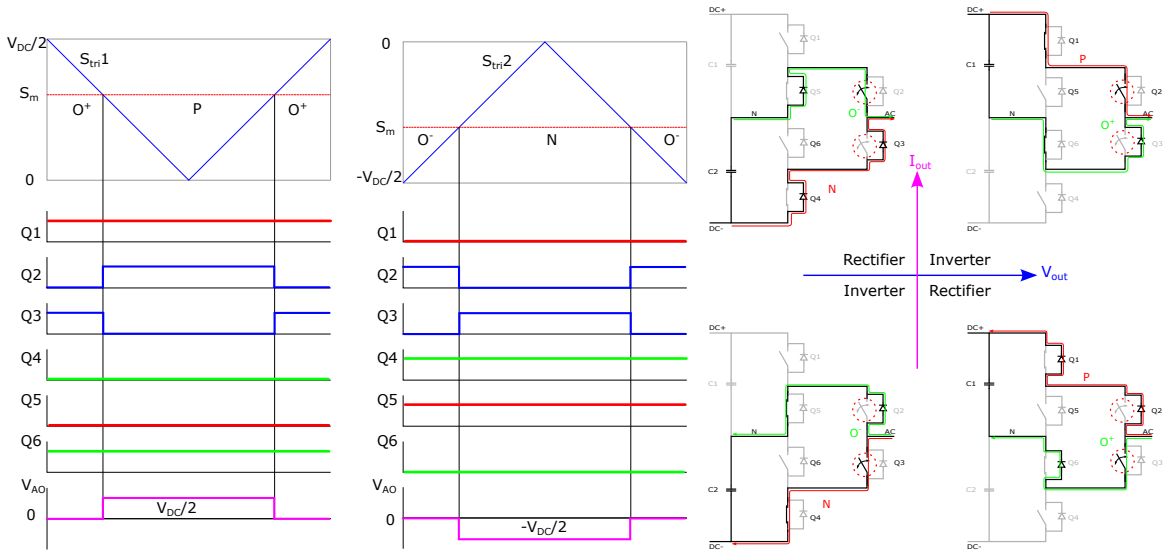
1.3 PWM2

In the PWM2 strategy (Fig. A.6), only cell 2 operates at high switching frequency, while cells 1 and 3 switch at the fundamental frequency. This strategy results in a redistribution of switching losses compared to PWM1. This strategy uses two carrier waves phase-shifted vertically with respect to the reference signal, allowing for finer control over switching transitions and resulting losses (Table A.6).

Output Voltage (V_{AO})	Switching State	Switching Sequence					
		Q1	Q2	Q3	Q4	Q5	Q6
$-V_{DC}/2$	N	0	0	1	1	1	0
0	O^-	0	1	0	1	1	0
	O^+	1	0	1	0	0	1
$V_{DC}/2$	P	1	1	0	0	0	1

Table A.5: Table of states for the ANPCtopology PWM_2 control



(a) a (b) b

Figure A.6: ANPC2

Switch	Switching Loss Formula
Q1/Q4/Q5/Q6 D1/D4/D5/D6	0
Q2/Q3/D2/D3	$\frac{1}{\pi}(\frac{\pi a_{sw}}{2} Is^2 + b_{sw} Is\sqrt{2} + \pi c_{sw}/2)\frac{V_{DC}/2}{V_{ref}} f_{sw}$
Switch	Switching Loss Interval
Q2/Q3	$(\varphi \rightarrow \pi + \varphi)$
D2/D3	$(\pi + \varphi \rightarrow 2\pi + \varphi)$

Table A.6: ANPC-PWM2 switching loss formulas

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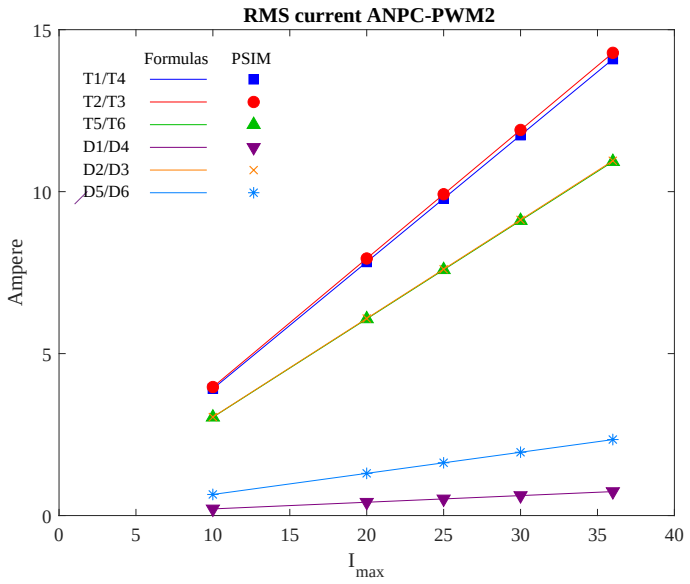

Figure A.7: ANPC-PWM2 circuit

1.4 PWM3

PWM3 is a hybrid strategy that combines the features of PWM1 and PWM2. It aims to improve the converter's performance, particularly near the zero-crossing of the reference voltage. Each switch operates at the base switching frequency f_s, but due to the switching coordination, the output voltage has an apparent frequency of $2f_s$, similar to a three-level Flying Capacitor (3L-FC) converter.

The key benefit of PWM3 is that it mitigates dead-time effects around $V_{ref} \approx 0$ by alternating the switching between different cell pairs:

When $V_{ref} > 0$: cells 1 and 2 switch.

When $V_{ref} < 0$: cells 2 and 3 switch. This strategy enhances the static performance and evenly spreads the switching activity.

Output Voltage (V_{AO})	Switching State	Switching Sequence					
		Q1	Q2	Q3	Q4	Q5	Q6
$-V_{DC}/2$	N	0	0	1	1	1	0
0	O_1^-	0	0	1	0	0	1
	O_2^-	0	1	0	1	1	0
	O_1^+	0	1	0	0	1	0
	O_2^+	1	0	1	0	0	1
$V_{DC}/2$	P	1	1	0	0	0	0

Table A.7: Table of states for the ANPCtopology $PWM3$ control

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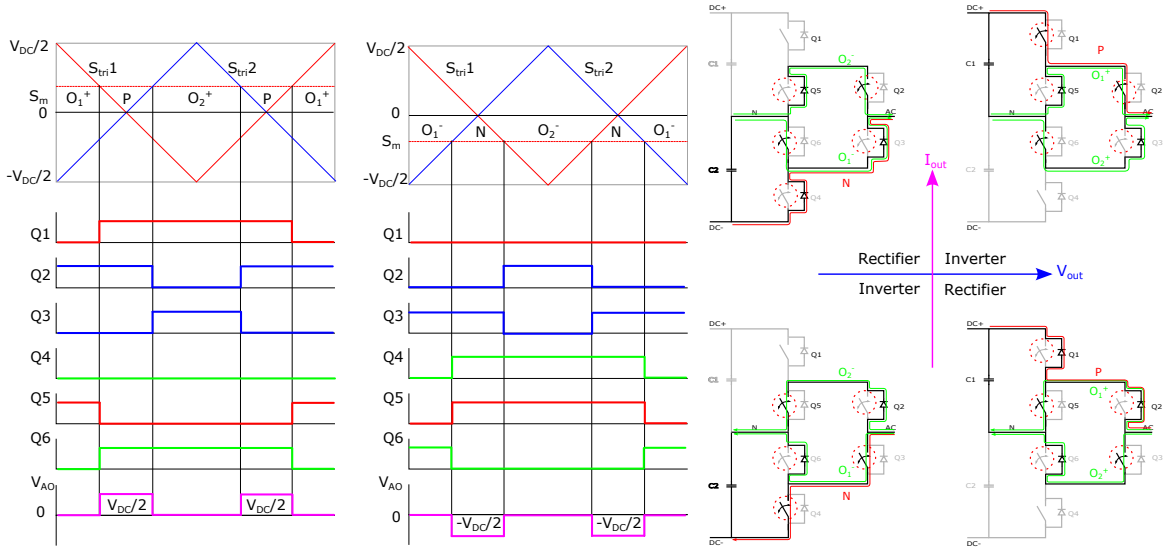

(a) a (b) b

Figure A.8: ANPC3

Switch	Switching Loss Formula
Q1/Q4/D5/D6	$\frac{1}{2\pi}[a_{sw}I^2[\pi-\varphi+\frac{sin(2\varphi)}{2}]+b_{sw}I\sqrt{2}(1+cos(\varphi))+c_{sw}(\pi-\varphi)]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Q2/Q3/D2/D3	$\frac{1}{\pi}(\frac{\pi a_{sw}}{2}Is^2+b_{sw}Is\sqrt{2}+\pi c_{sw}/2)\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Q5/Q6/D1/D4	$\frac{1}{2\pi}[a_{sw}I^2[\varphi-\frac{sin(2\varphi)}{2}]+b_{sw}I\sqrt{2}(1-cos(\varphi))+c_{sw}\varphi]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Switch	Switching Loss Interval
Q1/Q4/D5/D6	$(\varphi\rightarrow\pi)$
Q2/Q3	$(\varphi\rightarrow\pi+\varphi)$
Q5/Q6/D1/D4	$(0\rightarrow\varphi)$
D2/D3	$(\pi+\varphi\rightarrow2\pi+\varphi)$

Table A.8: ANPCPWM3 switching loss formulas

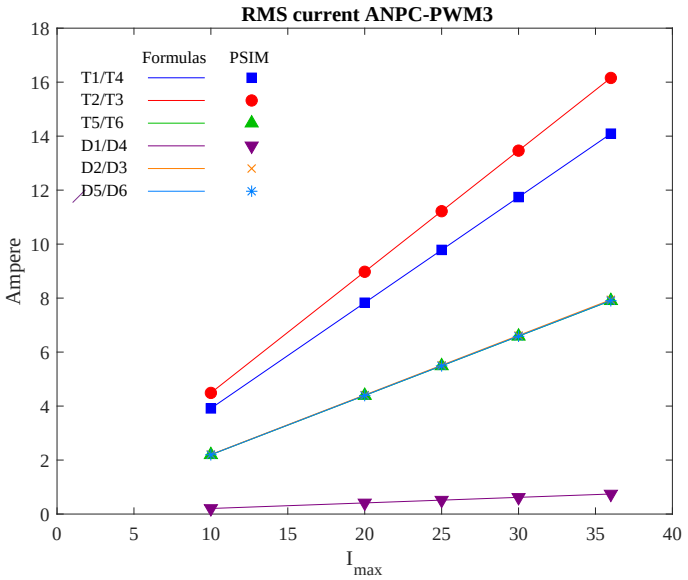

Figure A.9: ANPCPWM3 circuit

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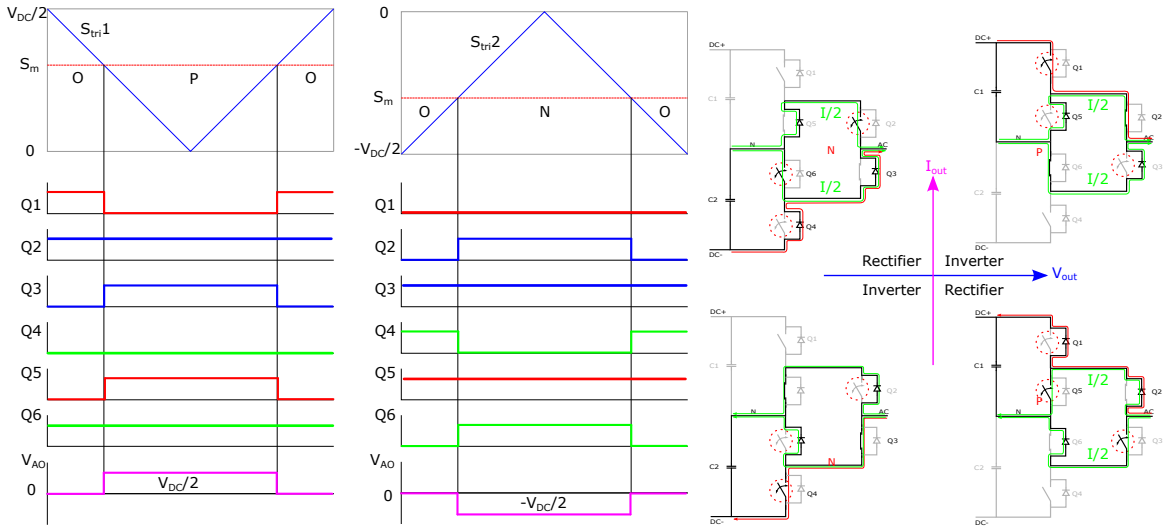
1.5 PWM4

PWM4 is an alternate approach focusing on symmetrical switching behavior. It simplifies the zero state to a single configuration, denoted as O. The switch usage in PWM4 leads to a more uniform thermal profile at the cost of a more constrained commutation scheme.Detailed current behavior and switching dynamics of Q2/Q3 and Q5/Q6 are illustrated in Fig. A.12 and Fig. A.13. This PWM technique provides an alternative distribution of switching losses, as summarized in the associated loss table.

Output Voltage (V_{AO})	Switching State	Switching Sequence					
		Q1	Q2	Q3	Q4	Q5	Q6
$-V_{DC}/2$	N	0	0	1	1	1	0
0	O	1	1	0	0	0	1
$V_{DC}/2$	P	1	1	0	0	0	1

Table A.9: Table of states for the ANPCtopology $PWM4$ control



(a) a (b) b

Figure A.10: ANPC4

Switch	Switching Loss Formula
Q1/Q4	$\frac{1}{2\pi}[a_{sw}I^2[\pi-\varphi+\frac{sin(2\varphi)}{2}]+b_{sw}I\sqrt{2}(1+cos(\varphi))+c_{sw}(\pi-\varphi)]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Q2/Q3/Q5/Q6	$\frac{1}{4\pi}[a_{sw}I^2[\varphi-\frac{sin(2\varphi)}{2}]+b_{sw}I\sqrt{2}(1-cos(\varphi))+2c_{sw}\varphi]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
D1/D4	$\frac{1}{2\pi}[a_{sw}I^2[\varphi-\frac{sin(2\varphi)}{2}]+b_{sw}I\sqrt{2}(1-cos(\varphi))+c_{sw}\varphi]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
D2/D3/D5/D6	$\frac{1}{4\pi}[a_{sw}I^2[\pi-\varphi+\frac{sin(2\varphi)}{2}]+b_{sw}I\sqrt{2}(1+cos(\varphi))+2c_{sw}(\pi-\varphi)]\frac{V_{DC}/2}{V_{ref}}f_{sw}$
Switch	Switching Loss Interval
Q1/Q4/D5/D6	$(\varphi\rightarrow\pi)$
Q2/Q3	$(\pi\rightarrow\pi+\varphi)$
Q5/Q6/D1/D4	$(0\rightarrow\varphi)$

Table A.10: ANPCPWM4 switching loss formulas

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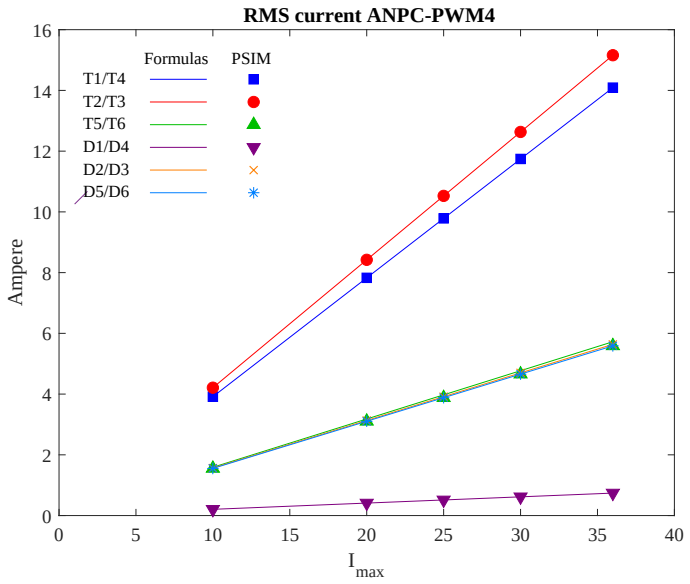

Figure A.11: ANPCPWM4 circuit

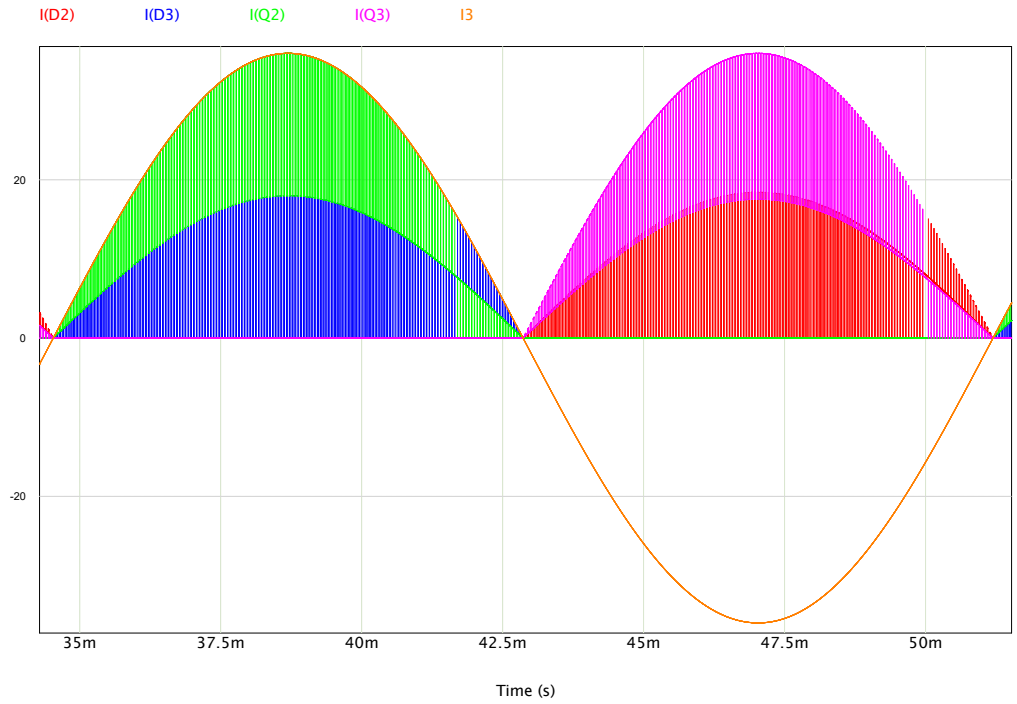

Figure A.12: ANPCPWM4 Q2 & Q3 current behaviour

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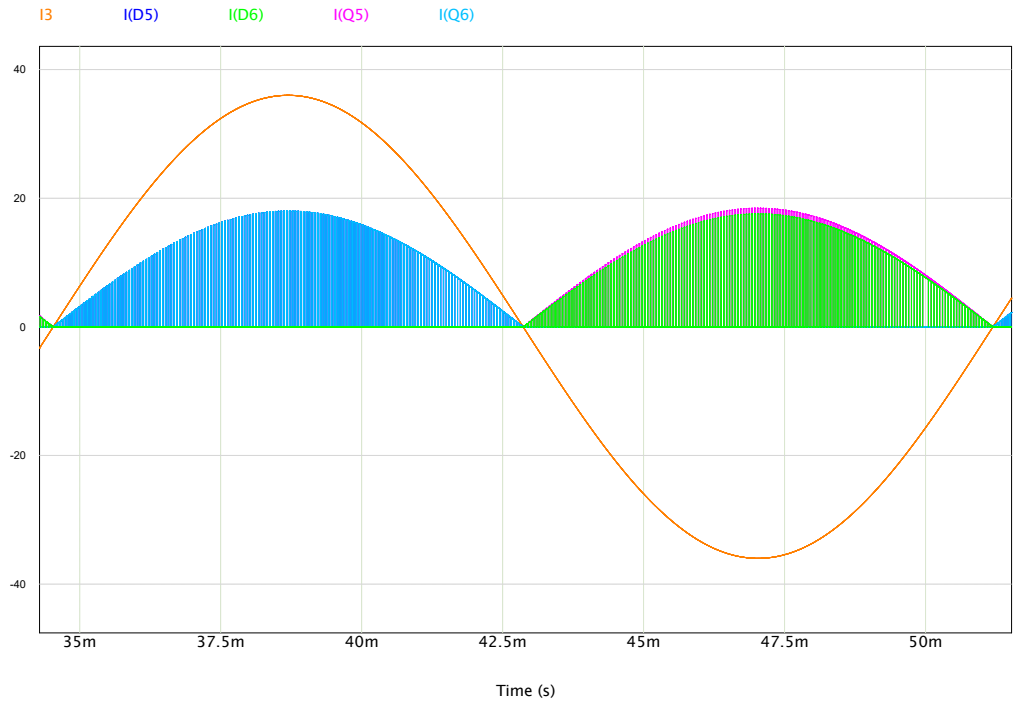

Figure A.13: ANPCPWM4 Q5 & Q6 current behaviour

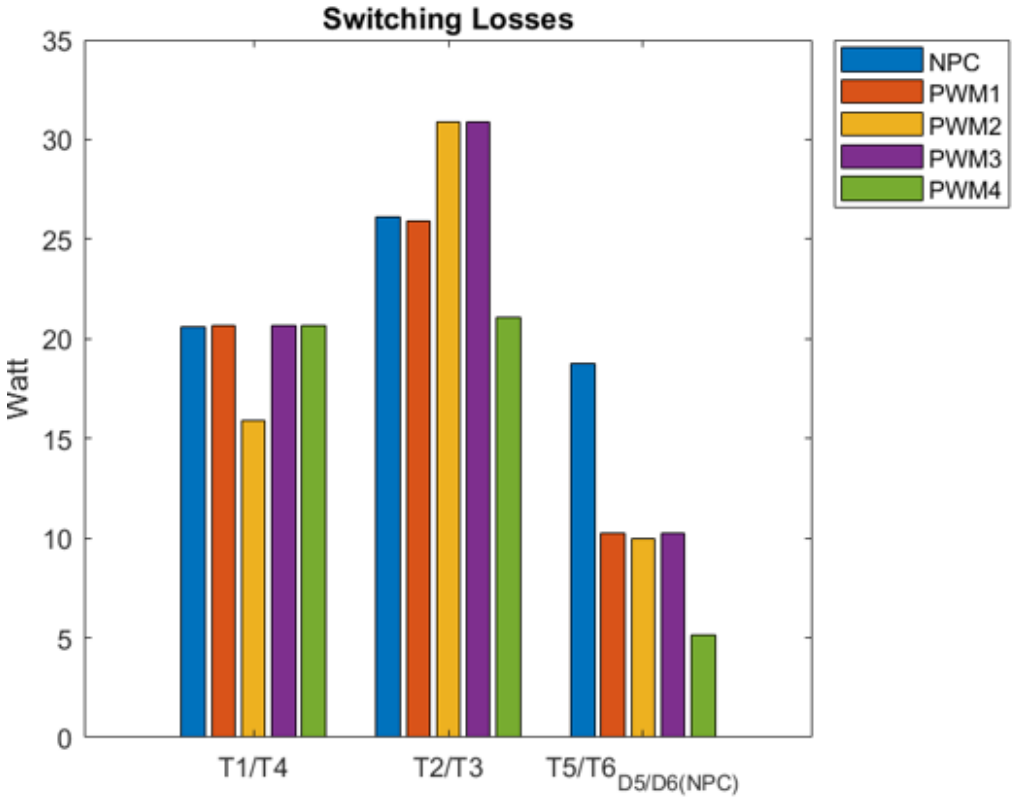

Figure A.14: Power losses comparison of the ANPC control algorithms

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	Switch	RMS Current	Average Current
PWM1	Q1/Q4	$\sqrt{\frac{mIs}{3\pi}(1+cos(\varphi))}$	$\frac{mIs\sqrt{2}}{4\pi}(sin(\varphi)+(\pi-\varphi)cos(\varphi))$
	D1/D4	$\sqrt{\frac{mIs}{3\pi}(1-cos(\varphi))}$	$\frac{mIs\sqrt{2}}{4\pi}(sin(\varphi)-\varphi cos(\varphi))$
	Q2/Q3	$Is\sqrt{((\pi-\varphi)+\frac{sin(2\varphi)/2)}{(2\pi)}}$	$\frac{Is}{\pi\sqrt{2}}(1+cos(\varphi))$
	D2/D3	$\frac{Is}{2}\sqrt{\frac{(2\varphi-sin(2\varphi))}{\pi}}$	$\frac{Is}{\pi\sqrt{2}}(1-cos(\varphi))$
	Q5/Q6	$Is\sqrt{\frac{\varphi}{2\pi}-\frac{sin(2\varphi)}{4\pi}-\frac{m}{3\pi}(1-cos(\varphi))^2)}$	$\frac{Is}{2\sqrt{2}\pi}(2(1-cos(\varphi))+m(\varphi cos(\varphi)-sin(\varphi)))$
	D5/D6	$Is\sqrt{\frac{pi-phi}{2\pi}+\frac{sin(2\varphi)}{4\pi}-\frac{m}{3\pi}*(1+cos(phi))^2)}$	$\frac{Is}{2\sqrt{2}\pi}(2(1+cos(\varphi))+m((\varphi-\pi)cos(\varphi)-sin(\varphi)))$
PWM2	Q1/Q4	$\sqrt{\frac{mIs}{3\pi}(1+cos(\varphi))}$	$\frac{mIs\sqrt{2}}{4\pi}(sin(\varphi)+(\pi-\varphi)cos(\varphi))$
	D1/D4	$\sqrt{\frac{mIs}{3\pi}(1-cos(\varphi))}$	$\frac{mIs\sqrt{2}}{4\pi}(sin(\varphi)-\varphi cos(\varphi))$
	Q2/Q3	$Is\sqrt{\frac{1}{4\pi}(2\varphi-sin(2\varphi))+\frac{4m}{3\pi}cos(\varphi))}$	$\frac{Is}{\pi 2\sqrt{2}}(2(1-cos(\varphi))+\pi mcos(\varphi))$
	D2/D3	$Is\sqrt{(\frac{1}{4\pi}(2(\pi-\varphi)+sin(2\varphi))-\frac{4m}{3\pi}cos(\varphi))}$	$\frac{Is}{\pi 2\sqrt{2}}(2(1+cos(\varphi))-\pi mcos(\varphi))$
	Q5/Q6	$Is\sqrt{\frac{pi-phi}{2\pi}+\frac{sin(2\varphi)}{4\pi}-\frac{m}{3\pi}(1+cos(\varphi))^2}$	$\frac{Is}{2\sqrt{2}\pi}(2(1+cos(\varphi))+m((\varphi-\pi)cos(\varphi)-sin(\varphi)))$
	D5/D6	$Is\sqrt{(\frac{\varphi}{2\pi}-\frac{sin(2\varphi)}{4\pi}-\frac{m}{3\pi}(1-cos(\varphi))^2)}$	$\frac{Is}{2\sqrt{2}\pi}(2(1-cos(\varphi))+m(\varphi cos(\varphi)-sin(\varphi)))$
PWM3	Q1/Q4	$\sqrt{\frac{mIs}{3\pi}(1+cos(\varphi))}$	$\frac{mIs\sqrt{2}}{4\pi}(sin(\varphi)+(\pi-\varphi)cos(\varphi))$
	D1/D4	$\sqrt{\frac{mIs}{3\pi}(1-cos(\varphi))}$	$\frac{mIs\sqrt{2}}{4\pi}(sin(\varphi)-\varphi cos(\varphi))$
	Q2/Q3	$Is\sqrt{\frac{1}{4}+\frac{2m}{3\pi}cos(\varphi)}$	$\frac{Is}{\sqrt{2}}(\frac{1}{\pi}+\frac{m}{4}cos(\varphi))$
	D2/D3	$Is\sqrt{\frac{1}{4}-\frac{2m}{3\pi}cos(\varphi)}$	$\frac{Is}{\sqrt{2}}(\frac{1}{\pi}-\frac{m}{4}cos(phi))$
	Q5/Q6	$Is\sqrt{\frac{1}{4}-\frac{m}{3\pi}(1+cos(\varphi)^2)}$	$\frac{Is}{\pi\sqrt{2}}(1+\frac{m}{4}((2\phi-\pi)cos(\varphi)-2sin(\varphi)))$
	D5/D6	$Is\sqrt{\frac{1}{4}-\frac{m}{3\pi}(1+cos(\varphi)^2)}$	$\frac{Is}{\pi\sqrt{2}}(1+\frac{m}{4}((2\varphi-\pi)cos(\varphi)-2sin(\varphi)))$
PWM4	Q1/Q4	$\sqrt{\frac{mIs}{3\pi}(1+cos(\varphi))}$	$\frac{mIs\sqrt{2}}{4\pi}(sin(\varphi)+(\pi-\varphi)cos(\varphi))$
	D1/D4	$\sqrt{\frac{mIs}{3\pi}(1-cos(\varphi))}$	$\frac{mIs\sqrt{2}}{4\pi}(sin(\varphi)-\varphi cos(\varphi))$
	Q2/Q3	$Is\sqrt{\frac{1}{8}+\frac{m}{6\pi}(1+4cos(\varphi)+cos(\varphi)^2)}$	$\frac{Is}{\sqrt{2}}(\frac{1}{\pi}+\frac{m}{4}cos(\varphi))$
	D2/D3	$Is\sqrt{\frac{1}{8}+\frac{m}{6\pi}(1-4cos(\varphi)+cos(\varphi)^2)}$	$\frac{Is}{\sqrt{2}}(\frac{1}{\pi}-\frac{m}{4}cos(\varphi))$
	Q5/Q6	$Is\sqrt{\frac{1}{8}-\frac{m}{6\pi}(1+cos(\varphi)^2)}$	$\frac{Is}{\pi\sqrt{2}}(1+\frac{m}{4}((2\phi-\pi)cos(\varphi)-2sin(\varphi)))$
	D5/D6	$Is\sqrt{\frac{1}{8}-\frac{m}{6\pi}(1+cos(\varphi)^2)}$	$\frac{Is}{\pi\sqrt{2}}(1+\frac{m}{4}((2\varphi-\pi)cos(\varphi)-2sin(\varphi)))$

Table A.11: ANPC RMS & Average Current formulas

	Conduction Interval				Modulation Function			
Switch	PWM1	PWM2	PWM3	PWM4	PWM1	PWM2	PWM3	PWM4
Q1/Q4	$(\varphi\to\pi)$				$m.sin(\theta)$			
Q1/Q4	$(0\to\pi)$				$1+m.sin(\theta)$			
Q2/Q3	$(\varphi\to\pi)$	$(\varphi\to\pi)$ $(\pi\to\pi+\varphi)$	$(\varphi\to\pi+\varphi)$	$(\varphi\to\pi+\varphi)$	1	$\frac{m.sin(\theta)}{1+m.sin(\theta)}$	$\frac{1+m.sin(\theta)}{2}$	$1+m.sin(\theta)$
D2/D3	$(0\to\varphi)$	$(0\to\varphi)$ $(\pi+\varphi\to 2\pi)$	$(0\to\varphi)$ $(\pi+\varphi\to 2\pi)$	$(0\to\varphi)$ $(\pi+\varphi\to 2\pi)$	1	$m.sin(\theta)$ $1+m.sin(\theta)$	$\frac{1+m.sin(\theta)}{2}$ $\frac{1+m.sin(\theta)}{2}$	$1+m.sin(\theta)$ $1+m.sin(\theta)$
Q5/Q6	$(0\to\varphi)$	$(\pi+\varphi\to 2\pi)$	$(0\to\varphi)$ $(\pi+\varphi\to 2\pi)$	$(0\to\varphi)$ $(\pi+\varphi\to 2\pi)$	$1-m.sin(\theta)$	$1+m.sin(\theta)$	$\frac{1-m.sin(\theta)}{2}$ $\frac{1+m.sin(\theta)}{2}$	$1-m.sin(\theta)$ $1+m.sin(\theta)$
D5/D6	$(\varphi\to\pi)$	$(\pi\to\pi+\varphi)$	$(\varphi\to\pi)$ $(\pi\to\pi+\varphi)$	$(\varphi\to\pi)$ $(\pi\to\pi+\varphi)$	$1-m.sin(\theta)$	$1+m.sin(\theta)$	$\frac{1-m.sin(\theta)}{2}$ $\frac{1+m.sin(\theta)}{2}$	$1-m.sin(\theta)$ $1+m.sin(\theta)$

Table A.12: ANPC switching loss formulas

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Appendix B

SiC MOSFET Parameter Extraction

Junction Temperature Estimation

The junction temperature (T_j) is a key factor in converter design. All semiconductors have a maximum junction temperature that must not be exceeded—typically around 150°C to 175°C. Additionally, the device lifetime is inversely related to the operating junction temperature. Therefore, accurate temperature estimation and efficient thermal management are essential for designing a reliable power converter.

The on-state resistance of the MOSFET, $R_{\mathrm{DS(on)}}$, increases with temperature. The following polynomial equation models this temperature dependence:

$$R_{\mathrm{DS(on)}}(T_j) = a_X \cdot T_j^2 + b_X \cdot T_j + c_X \tag{B.1}$$

Where: - T_j: Junction temperature (°C) - a_X, b_X, c_X: Fitting coefficients extracted from LTspice simulation or datasheet data.

Simulation-Based Parameter Extraction

Figures B.2 and B.1 present key characteristics of the SiC MOSFET CPM2-1200-0080 bare die, extracted using LTspice simulations.

Figure B.2 shows the normalized on-state resistance $R_{\mathrm{DS(on)}}$ as a function of the junction temperature. The data are obtained from the Cree-provided LTspice model and normalized with respect to the reference value $R_{\mathrm{DS(on),ref}} = 80\,\mathrm{m\Omega}$, which corresponds to the nominal value at room temperature.

Figure B.1, on the other hand, illustrates the switching energy losses of the same SiC MOSFET in a MOSFET-MOSFET assembly. This analysis, also based on LTspice simulation, provides essential insights into the dynamic performance of the device during switching events under typical operating conditions.

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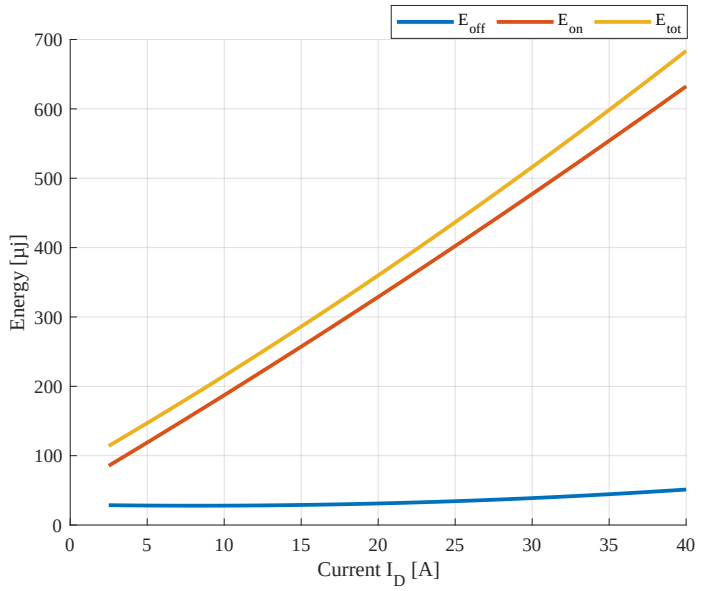

Figure B.1: Switching energy analysis of the SiC MOSFET CPM2-1200-0080 bare die in a MOSFET-MOSFET assembly using LTspice.

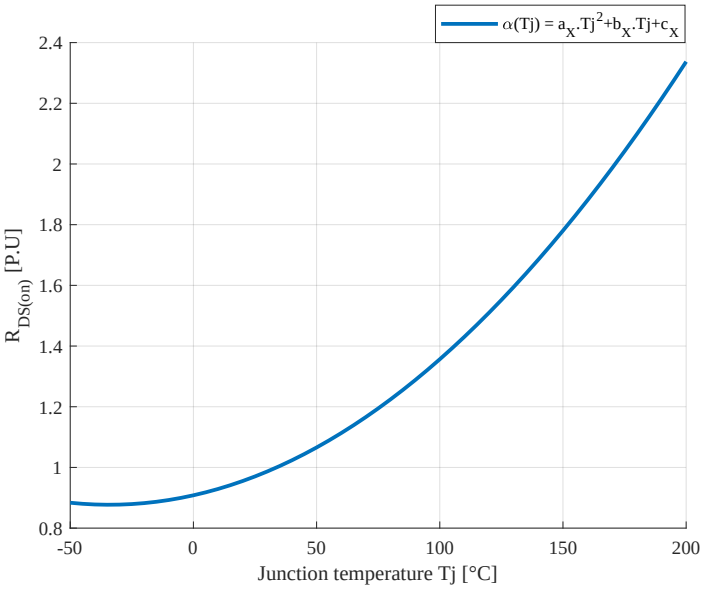

Figure B.2: Normalized on-state resistance $R_{\mathrm{DS(on)}}$ of the SiC MOSFET die (CPM2-1200-0080A) as a function of junction temperature. Reference value: $R_{\mathrm{DS(on),ref}} = 80\,\mathrm{m\Omega}$. Data extracted from the LTspice model provided by Cree.

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These simulation results serve as the foundation for the electrical and thermal modeling of the device within the converter design.

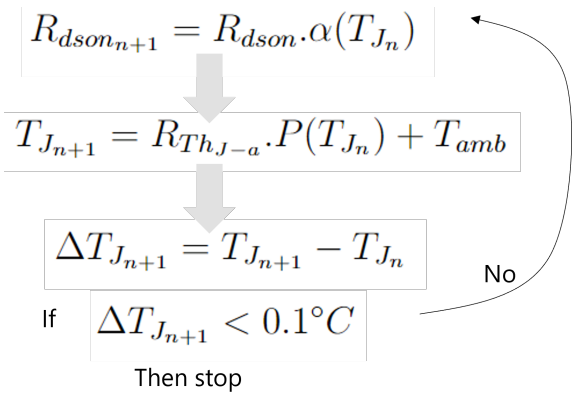

Figure B.3: Iterative algorithm used to account for $R_{\mathrm{DS(on)}}$ temperature dependence.

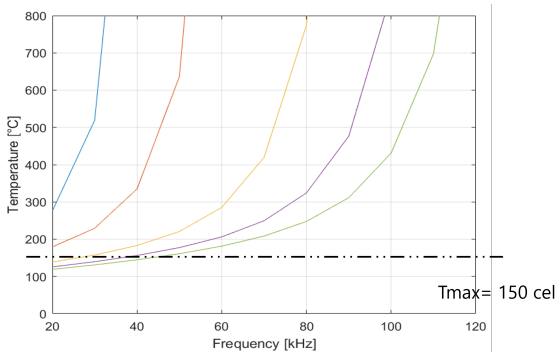

Figure B.4: Analytical estimation of junction temperature considering the temperature dependence of $R_{\mathrm{DS(on)}}$.

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Appendix C

Bayesian deconvolution

In the context of a continuous linear system, the output signal can be expressed probabilistically as:

$$\frac{d}{dz}a(t) = \int w(t|\tau)\, R(\tau)\, d\tau \tag{C.1}$$

Here, $w(t|\tau)$ represents the conditional probability distribution (or response kernel) linking the system response $a(t)$ to the underlying source signal $R(\tau)$.

To recover $R(\tau)$, the deconvolution problem can be reformulated using Bayes' theorem. Specifically:

$$R(\tau) = \int q(\tau|t)\, \frac{d}{dz}a(t)\, dt \tag{C.2}$$

where $q(\tau|t)$ is the posterior probability defined by:

$$q(\tau|t) = R(\tau) \cdot \frac{w(t|\tau)}{\frac{d}{dz}a(t)} \tag{C.3}$$

Since $R(\tau)$ is not known a priori, an iterative approach is used to estimate it. At iteration n, we define:

$$q^{(n)}(\tau|t) = R^{(n)}(\tau) \cdot \frac{w(t|\tau)}{\frac{d}{dz}a^{(n)}(t)} \tag{C.4}$$

The update equation for $R(\tau)$ at iteration n becomes:

$$R^{(n)}(\tau) = \int q^{(n-1)}(\tau|t)\, \frac{d}{dz}a^{(0)}(t)\, dt = \int R^{(n-1)}(\tau)\, \frac{w(t|\tau)}{\frac{d}{dz}a^{(n-1)}(t)}\, \frac{d}{dz}a^{(0)}(t)\, dt \tag{C.5}$$

Here, $\frac{d}{dz}a^{(0)}(t)$ corresponds to the measured data, while the estimated forward

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response at the previous iteration is computed as:

$$\frac{d}{dz}a^{(n-1)}(t) = \int w(t|\tau)\, R^{(n-1)}(\tau)\, d\tau \tag{C.6}$$

In the discrete case (e.g., with M sampling points), the update rule becomes:

$$R^{(n)}(i) = R^{(n-1)}(i) \sum_{k=0}^{M-1} w(k,i)\, \frac{\frac{d}{dz}a(k)}{\sum_{j=0}^{M-1} w(k,j)\, R^{(n-1)}(j)}\, dt \quad , \quad i \in [0, M-1] \tag{C.7}$$

This iterative Bayesian deconvolution method allows recovering the source signal $R(\tau)$ from the measured data $\frac{d}{dz}a(t)$, even in the presence of system convolution effects.

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FOLIO ADMINISTRATIF

THESE DE L'INSA LYON, MEMBRE DE L'UNIVERSITE DE LYON

NOM : **BEN HAMED** DATE de SOUTENANCE : **18/07/2025**
Prénoms : **Bahaeddine**

TITRE : **Design toolkit for PCB-based power electronic systems**
NATURE : **Doctorat** Numéro d'ordre : **2025ISAL0071**

École Doctorale : **Électronique, Électrotechnique et Automatique de Lyon**
Spécialité : **Énergie et Systèmes**

RÉSUMÉ :
Les convertisseurs de puissance sont des systèmes complexes faisant intervenir des phénomènes multiphysiques couplés : comportement électromagnétique, effets thermiques et interactions matériaux. Leur conception est rendue difficile par la diversité des composants, matériaux, niveaux de tension et stratégies de refroidissement utilisés. À cela s'ajoutent des exigences croissantes en matière de performance, de miniaturisation et de fiabilité. Les outils actuels de CAO électronique (ECAD) et de simulation ont beaucoup évolué. Ils sont plus précis, conviviaux et capables de modéliser des comportements détaillés. Toutefois, le processus de conception reste morcelé. Différents outils spécialisés sont utilisés à chaque étape, nécessitant des expertises variées, une gestion complexe des données, et impliquant des problèmes d'interopérabilité entre formats propriétaires. Ce cloisonnement ralentit le développement, notamment lors des itérations entre les aspects électriques, thermiques et mécaniques. Le prototypage physique représente également un frein, en particulier pour les technologies avancées comme les PCB embarqués. Les délais de fabrication peuvent atteindre plusieurs mois, avec des coûts élevés. Le prototypage virtuel apparaît ainsi comme une alternative prometteuse, mais encore peu développée dans le domaine de l'électronique de puissance. Cette thèse propose un outil de conception permettant de générer automatiquement des prototypes virtuels de cartes électroniques de convertisseurs. L'objectif est de produire des modèles de simulation électro-thermiques fiables à partir du layout PCB, en réduisant le recours au prototypage physique. L'outil développé intègre plusieurs étapes : extraction du layout, simplification géométrique, modélisation électromagnétique, simulation thermique par éléments finis et génération de schéma électronique pour la simulation de circuits. Les validations expérimentales menées sur des cartes simples et complexes ont confirmé la pertinence des modèles générés. L'outil permet de simuler des paramètres difficiles à mesurer comme la température de jonction ou les formes d'onde de commutation. Les résultats ont été comparés à des mesures sur prototypes réels, renforçant la crédibilité de l'approche. L'analyse des performances montre que la simulation thermique est l'étape la plus coûteuse en temps (jusqu'à 95% du calcul total), mais reste négligeable face aux délais de fabrication. La capacité à explorer des variantes avant fabrication, et à accéder à des variables internes, montre la valeur pratique du prototypage virtuel. Des limites subsistent : dépendance à des logiciels propriétaires, problèmes de maillage, génération de netlistes partiellement automatisée, et absence de prise en compte automatique des conditions environnementales. Des pistes d'amélioration incluent l'adoption de standards ouverts (IPC-2581) et l'intégration d'outils open-source. En conclusion, cette thèse démontre le potentiel du prototypage virtuel automatisé basé sur le layout dans le domaine de l'électronique de puissance embarquée. L'outil développé constitue une preuve de concept solide pour une approche unifiée, plus rapide et plus fiable du processus de conception.

MOTS-CLÉS : **conception assistée par ordinateur,génération automatique de modèles,Circuit imprimé,design for manufacturing,vérification automatisée,métrologie**

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