

# Hybrid InGaAs/SiGe technology platform for CMOS applications

Lukas Czornomaz

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# Filière technologique hybride InGaAs/SiGe pour applications CMOS

**Hybrid InGaAs/SiGe Technology Platform for CMOS Applications**

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# Hybrid InGaAs/SiGe Technology Platform for CMOS Applications

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# Abstract

High-mobility channel materials such as indium-galium-arsenide (InGaAs) and silicon-germanium (SiGe) alloys are considered to be the leading candidates for replacing silicon (Si) in future low power complementary metal-oxide-semiconductor (CMOS) circuits. Numerous challenges have to be tackled in order to turn the high-mobility CMOS concept into an industrial solution. This thesis addresses the majors challenges which are the integration of InGaAs on Si, the formation of high-quality gate stacks and self-aligned source and drain (S/D) regions, the optimization of self-aligned metal-oxide-semiconductor field-effect transistors (MOSFETs) and the co-integration of InGaAs and SiGe into CMOS circuits. All investigated possible solutions are proposed in the framework of very-large-scale integration requirements.

**Substrates -** InGaAs integration on Si is explored in the form of large-scale blanket layers obtained by direct wafer bonding (DWB) and micron-sized local islands by selective epitaxy in empty oxide cavities. With DWB, 200 mm InGaAs-on-insulator (InGaAs-OI) wafers are fabricated with a threading dislocation density (TDD) as low as $3\times10^{8}$ $cm^{-2}$, among the best reported values for InGaAs on Si. Donor wafer recycling is demonstrated with the use of hydrogen-induced thermal splitting. Hybrid dual-channel ultra-thin body and buried oxide (BOX) (UTBB) InGaAs/SiGe wafers are realized as a platform for CMOS circuit fabrication. Then, the confined epitaxial lateral overgrowth (CELO) of InGaAs and indium-phosphide (InP) in empty oxide cavities is investigated as a novel solution for the local integration of III-V materials on large-scale wafers.

**Process Modules -** Thermally stable gate stacks containing a thin amorphous silicon (a-Si) interlayer between the InGaAs channel and the high-k (HK) dielectric are scaled to sub-14 Å capacitance-equivalent thickness (CET). Remote oxygen scavenging of InGaAs native oxides is shown to yield up to 5 Å CET scaling on directHK/InGaAs interfaces, associated with a reduction of density of interface traps ($D_{it}$). As a result, an optimized *in-situ* plasma-enhanced atomic layer deposition (ALD) (PEALD) gate stack with direct HK/InGaAs interface is presented. Self-aligned S/D regions are developed with the use of optimized highly-doped InGaAs raised S/D (RSD). They are combined with self-aligned

nickel-indium-galium-arsenide (Ni-InGaAs) alloyed contacts and compared to direct metal contacts to RSD.

**Devices -** CMOS-compatible self-aligned InGaAs MOSFETs with several architectures are compared: bulk vs on-insulator, planar vs fins, gate-first (GF) vs replacement metal-gate (RMG), a-Si-stack vs direct HK stacks, Ni-InGaAs vs direct metal contacts. Optimized RMG InGaAs fin-based MOSFETs (FinFETs) with a PEALD direct HK gate stack and direct metal contacts have achieved record performance among CMOS-compatible InGaAs MOSFET on Si. Devices with gate length ($L_G$) = 50 nm and $W_{fin}$ = 15 nm show a subthreshold swing (SS) down to 80 mV/dec and an on-current ($I_{on}$) up to 156 $\mu$A/$\mu$m at fixed off-current ($I_{off}$) = 100 nA/$\mu$m and fixed operating voltage ($V_{DD}$) = 0.5 V.

**Circuits -** 2D co-planar hybrid InGaAs/SiGe CMOS circuits are fabricated using the DWB or CELO technique. Operational CMOS inverters and dense 6-transistors (6T)-static random access memory (SRAM) cells are realized, which represents the first demonstration of InGaAs/SiGe co-planar CMOS circuits on Si. 3D monolithic integration is proposed to co-integrate a "hot" bottom layer of SiGe p-MOSFETs and a "cold" top layer of InGaAs n-MOSFETs, with their respective independently optimized process. Excellent performance is obtained for devices on each device layer and 3D monolithic CMOS inverters are demonstrated.

# Contents

**Abstract** **iii**

**List of Acronyms** **viii**

**List of Symbols** **xii**

**1 Introduction** **1**

1.1 High-mobility materials for future CMOS nodes . . . . . 1

1.2 Challenges and solutions to integrate InGaAs on Si . . . . . 4

1.3 Requirements for self-aligned MOSFETs . . . . . 7

1.4 Hybrid CMOS circuits . . . . . 9

1.5 Thesis: Organization and relation to published work . . . . . 11

**2 Substrates: InGaAs Integration on Si** **12**

2.1 Introduction . . . . . 12

2.2 Direct Wafer Bonding . . . . . 13

2.2.1 Layer transfer of III-V heterostructures to Si wafers . . . . . 14

2.2.2 Thermal stability of InGaAs-OI layers and regrowth . . . . . 17

2.2.3 Recycling of the donor wafer . . . . . 21

2.2.4 Large-scale InGaAs-on-insulator substrates . . . . . 26

2.2.5 Hybrid InGaAs/SiGe dual-channel substrates . . . . . 28

2.3 Confined Epitaxial Lateral Overgrowth . . . . . 31

2.3.1 Concept . . . . . 32

2.3.2 Fabrication of empty cavities on Si refilled by III-V crystals . . . . 34

2.3.3 Material characterization . . . . . 36

2.4 Conclusion and outlook . . . . . 40

**3 Process Modules: Gate Stack and S/D Regions** **41**

3.1 Introduction . . . . . 41

3.2 MOS Gate stack . . . 43
3.2.1 a-Si based gate stack . . . 45
3.2.2 Remote oxygen scavenging on high-k/InGaAs interfaces . . . 50
3.2.3 Optimized plasma-based high-k/InGaAs gate stack . . . 57
3.3 Contacts . . . 59
3.3.1 Raised Source/Drain . . . 60
3.3.2 Ni-InGaAs: Self-aligned silicide-like contacts . . . 65
3.3.3 Direct metal contacts . . . 71
3.4 Conclusion and Outlook . . . 73

**4 Devices: Self-aligned CMOS-compatible InGaAs MOSFETs 75**
4.1 Introduction . . . 75
4.2 Gate-first Planar MOSFETs . . . 76
4.2.1 Impact of Ni-InGaAs contacts on "bulk" devices . . . 79
4.2.2 Split C-V and Effective mobility . . . 81
4.2.3 Short-channel devices and roll-off characteristics . . . 82
4.2.4 Tight-pitch InGaAs MOSFETs . . . 84
4.3 Non-planar MOSFETs . . . 86
4.3.1 Junction-less FinFETs . . . 87
4.3.2 Replacement-gate FinFETs on Silicon . . . 90
4.3.3 Gate-first FinFETs on selectively grown InGaAs on Silicon . . . 96
4.4 Conclusion and Outlook . . . 99

**5 Circuits: Hybrid InGaAs/SiGe CMOS 100**
5.1 Introduction . . . 100
5.2 2D Co-planar CMOS Technology . . . 101
5.2.1 2D InGaAs/SiGe CMOS based on DWB . . . 102
5.2.2 2D InGaAs/SiGe CMOS based on CELO . . . 108
5.3 3D Monolithic CMOS technology . . . 115
5.3.1 Circuit fabrication . . . 116
5.3.2 Impact of nFETs fabrication on pFETs performance . . . 118
5.3.3 InGaAs n-MOSFETs and 3D CMOS inverters . . . 119
5.4 Conclusion and Outlook . . . 121

**6 Conclusion 122**

**A List of Publications 127**

**B Contributions to this work** **135**

**C Acknowledgements** **138**

**D French Summary** **140**

D.1 Introduction . . . . . 140

D.2 Substrats : Intégration d'InGaAs sur Si . . . . . 141

D.3 Modules : Empilement de grille et régions S/D . . . . . 142

D.4 Composants : Transistors auto-alignés compatibles CMOS à base d'InGaAs 144

D.5 Circuits : Technologie CMOS hybride InGaAs/SiGe . . . . . 145

D.6 Conclusion . . . . . 147

**List of Figures** **148**

**List of Tables** **160**

**Bibliography** **161**

# List of Acronyms

| | |
|---|---|
| 6T | 6-transistors |
| a-Si | amorphous silicon |
| AFM | atomic force microscopy |
| $Al_2O_3$ | aluminum-oxide |
| ALD | atomic layer deposition |
| ART | aspect ratio trapping |
| BE | binding energy |
| BEOL | back-end-of-line |
| BOX | buried oxide |
| BTI | bias temperature instability |
| C-V | capacitance-voltage |
| CELO | confined epitaxial lateral overgrowth |
| CET | capacitance-equivalent thickness |
| $CHF_3$ | trifluoromethane |
| CMOS | complementary metal-oxide-semiconductor |
| CMP | chemical-mechanical polishing |
| CVD | chemical vapor deposition |
| DETe | diethyl telluride |
| DHF | diluted hydrofluoric acid |
| DI | deionized |
| DIBL | drain-induced barrier lowering |
| $DIO_3$ | ozone-rich dionized water |
| DWB | direct wafer bonding |

| | |
|---|---|
| EBL | electron beam lithography |
| EDX | energy dispersive X-ray spectroscopy |
| ELO | epitaxial lateral overgrowth |
| EOT | equivalent oxide thickness |
| ETSOI | extremely-thin silicon on insulator |
| FDSOI | fully-depleted silicon on insulator |
| FEOL | front-end-of-line |
| FIB | focused ion beam |
| FinFET | fin-based MOSFET |
| FWHM | full width at half maximum |
| GaAs | galium-arsenide |
| GaSb | galium-antimonide |
| Ge | germanium |
| GF | gate-first |
| GIDL | gate-induced drain leakage |
| GPA | geometrical phase analysis |
| $H_2$ | hydrogen |
| $H_2S$ | hydrogen sulfide |
| $H_2SO_4$ | sulfuric acid |
| HCl | hydrochloric acid |
| HF | hydrofluoric acid |
| $HfO_2$ | hafnium-oxide |
| HK | high-k |
| HKMG | high-k metal-gate |
| $HNO_3$ | nitric acid |
| I-V | current-voltage |
| ICP | inductively-coupled plasma |
| ILD | interlayer dielectric |
| $In_{0.52}Al_{0.48}As$ | indium-aluminum-arsenide (InAlAs) (with 52% of indium) |
| $In_{0.53}Ga_{0.47}As$ | InGaAs (with 53% of indium) |
| $In_{0.7}Ga_{0.3}As$ | InGaAs (with 70% of indium) |

| | |
|---|---|
| InAlAs | indium-aluminum-arsenide |
| InAs | indium-arsenide |
| InGaAs | indium-galium-arsenide |
| InGaAs-OI | InGaAs-on-insulator |
| InP | indium-phosphide |
| JL | junction-less |
| M1 | first metalization level |
| MBD | molecular beam deposition |
| MBE | molecular beam epitaxy |
| MOS | metal-oxide-semiconductor |
| MOSCAP | metal-oxide-semiconductor capacitor |
| MOSFET | metal-oxide-semiconductor field-effect transistor |
| MOVPE | metal-organic vapor phase epitaxy |
| MT | microtwin |
| $N_2$ | nitrogen |
| Ni-InGaAs | nickel-indium-galium-arsenide |
| NID | non-intentionally doped |
| NW | nanowire |
| $O_2$ | oxygen |
| PEALD | plasma-enhanced ALD |
| PECVD | plasma-enhanced chemical vapor deposition |
| RHEED | reflection high-energy electron diffraction |
| RIE | reactive ion etching |
| RMG | rapid melt growth |
| RMG | replacement metal-gate |
| RMS | root mean square |
| RSD | raised S/D |
| S/D | source and drain |
| SBH | Schottky barrier height |

| | |
|---|---|
| SEM | scanning electron microscopy |
| SF | stacking fault |
| $SF_6$ | hexafluoride |
| Si | silicon |
| $Si_2H_6$ | disilane |
| SiGe | silicon-germanium |
| SIMS | secondary ion mass spectrometry |
| $SiN_x$ | silicon-nitride |
| $SiO_2$ | silicon-oxide |
| SOI | silicon on insulator |
| SRAM | static random access memory |
| SRB | strain-relaxed buffer |
| SRH | Shockley-Read-Hall |
| SS | subthreshold swing |
| STEM | scanning transmission electron microscopy (TEM) |
| TBA | tertiarybutylarsine |
| TBP | tributylphosphine |
| TDD | threading dislocation density |
| TEM | transmission electron microscopy |
| TESn | tetraethyltin |
| TiN | titanium nitride |
| $TiO_2$ | titanium-oxide |
| TLM | transfer length method |
| TMGa | trimethylgallium |
| TMIn | trimethylindium |
| UHV | ultra-high vacuum |
| UTBB | ultra-thin body and BOX |
| XPS | X-ray photoemission spectroscopy |
| XRD | x-ray diffraction |

# List of Symbols

| | | |
|---|---|---|
| $C_{ox}$ | oxide capacitance | [F/m$^2$] |
| $D_{it}$ | density of interface traps | [/m$^2$.eV] |
| $H_{fin}$ | fin height | [m] |
| $I_{off}$ | off-current | [A/m] |
| $I_{on}$ | on-current at fixed off-current and operating voltage | [A/m] |
| $\lambda$ | wavelength | [m] |
| $L_C$ | contact length | [m] |
| $L_G$ | gate length | [m] |
| $L_t$ | transfer length | [m] |
| $\mu_{eff}$ | effective mobility | [m$^2$/V.s] |
| $N_d$ | $n$-type dopant density | [/m$^3$] |
| $N_{inv}$ | inversion-charge density | [/m$^2$] |
| $R_C$ | contact resistance | [Ω] |
| $R_{ext}$ | external resistance | [Ω.m] |
| $\rho_C$ | specific contact resistance | [Ω.m$^2$] |
| $R_{SD}$ | source and drain series resistance | [Ω], [Ω.m] |
| $R_{sheet}$ | sheet resistance | [Ω/□] |
| $t_{ch}$ | channel thickness | [m] |

| | | |
|---|---|---|
| $V_{DD}$ | operating voltage | [V] |
| $V_{ds}$ | drain-to-source voltage | [V] |
| $V_{fb}$ | flat-band voltage | [V] |
| $V_g$ | gate voltage | [V] |
| $V_{in}$ | input voltage | [V] |
| $V_{out}$ | output voltage | [V] |
| $V_{SW}$ | switching voltage | [V] |
| $V_T$ | threshold voltage | [V] |
| | | |
| $W_{fin}$ | fin width | [m] |

# Chapter 1

# Introduction

## 1.1 High-mobility materials for future CMOS nodes

The scaling of complementary metal-oxide-semiconductor (CMOS) technology by the microelectronic industry over the past five decades has revolutionized our society. It transformed the concept of computing from a high value asset, restricted to elites, into a commodity of everyday life. As a consequence, since the mid 2000's, there are more connected devices to the Internet than Humans on Earth.

Moore's law [1], first proposed in 1965, described and predicted from an economic stand-point that in order to turn the microelectronic industry into a successful and steadily growing business, the component density per unit area should increase with time such that the cost per component or function decreases. Rather empirically, it was estimated that the component density would double every two years. Those components are metal-oxide-semiconductor field-effect transistors (MOSFETs), solid-state switches at the base of logic circuits, the workhorse of this industry.

In 1974, this economical trend was then translated into a technology scaling avenue known as Dennard's scaling [2] or geometrical scaling. It describes how making a transistor smaller could make it to perform better by a simple scaling of its dimensions and operating voltages. As such, the electric field distribution in the smaller transistor remains the same as in the original one, while providing a higher switching speed and a lower power consumption.

The limits of lithography and manufacturing were steadily pushed further, maintaining the pace of geometrical scaling for decades until the early 2000's and the 90 nm node. It marked the first technology node where simple geometrical scaling did not provide the expected performance and power consumption gains [3]. It resulted in the use of higher operating voltages than anticipated, which marked the end of pure Dennard's scaling.

From this technology node and in all subsequent nodes, the ever smaller spacing between the source and drain (S/D) regions of transistors gave rise to more and more pronounced short-channel effects: degradation of threshold voltage ($V_T$), subthreshold swing (SS) and drain-induced barrier lowering (DIBL). Therefore, in the past decade, the industry has been gradually moving to innovation-driven scaling, with the successive introduction of numerous technology boosters to recover the desired performance gain by acting either on the speed or standby power.

Silicon on insulator (SOI) technology was developed to lower parasitics and improve the electrostatic integrity of transistors. The 45 nm node saw the introduction of high-k dielectrics which enabled a deep scaling of the equivalent oxide thickness (EOT) of the metal-oxide-semiconductor (MOS) gate stack, further improving the transistor electrostatics. At the 28/22 nm node, fully-depleted devices were introduced with the use of extremely-thin silicon on insulator (ETSOI) channels, or silicon (Si) fins extending current transport in the third dimension. All those innovations helped maintaining a good gate control over the channel which enables scaling the transistor dimensions.

The technology boosters described above were negatively affecting the channel transport properties owing to increased scattering from dopants, high-k dielectrics, buried oxide (BOX) interface, or fin sidewall roughness. Therefore, strain was introduced at the 90 nm node and used in every subsequent technology node to affect the band structure of Si such that the effective mass of carriers could be reduced (with compressive strain for p-MOSFETs and tensile strain for n-MOSFETs). It resulted in improved carrier mobility and on-current, thus faster switching speed or reduced power consumption.

Process-induced stress, such as the use of silicon-nitride ($SiN_x$) stressor layers or contact metal stress, was proposed as a source of strain which could affect both types of devices. Epitaxy of lattice mismatched materials was proposed as another possible source of channel strain. It could be introduced by growing the channel material on a buffer of different lattice constant, or by growing lattice mismatched S/D regions. Compressive strain for Si p-MOSFETs could be easily achieved by the use of silicon-germanium (SiGe) which has a larger lattice constant than Si. On the contrary, tensile strain in Si n-MOSFETs was more challenging as the only available option for a S/D material with a lower lattice constant than Si was Si:C, where carbon solubility, thus lattice mismatch, is very limited. The Si channel could be integrated on strain-relaxed SiGe buffer to introduce bi-axial tensile strain, but this approach led to defective channel material and was never used in manufacturing. Furthermore, the conduction band structure under bi-axial tensile strain is such that minimal improvements in effective mass can be achieved at high vertical field as carriers tend to repopulate the high effective mass valleys [4].

In the history of CMOS technology, p-MOSFETs were always achieving much lower on-current than n-MOSFETs owing to the large difference in the electron and hole effective masses. In today's available technologies, the effects of strain in p-MOSFETs are such that they start to exceed the performance of n-MOSFETs. Furthermore, a clear roadmap exists for continued on-current improvements in p-MOSFETs with the introduction of SiGe channels of increasing germanium (Ge) content [5]. This innovation not only helps enhancing compressive strain in the channel, but also reduces the intrinsic effective mass of carriers. It should result in the formation of an n-MOSFETs performance gap in future CMOS technology nodes.

III-V compound semiconductors and in particular arsenides and phosphides are well-known materials commonly used in the telecom industry for ultra-fast electrical amplifiers, lasers, modulators or detectors. Their lower electron effective masses compared to Si make them very appealing to solve the n-MOSFETs performance gap. Indeed, as SiGe can be used to lower the intrinsic hole effective mass for p-MOSFETs, III-V semiconductors could be used as n-channel material to lower the intrinsic electron effective mass for n-MOSFETs [6]. Among all possible materials, indium-galium-arsenide (InGaAs) with an indium-content of 50% to 75% appears as the most promising candidate because it offers the best compromise between low effective mass for high on-current (through high carrier mobility and injection velocity), and large enough bandgap to reach the off-current targets of modern CMOS technologies [6].

A hybrid InGaAs/SiGe CMOS technology represents an extremely appealing proposal on a scientific level. Nevertheless, numerous challenges must be tackled to transform this research concept into an industrial solution. The target is not only to propose solutions and demonstrate the feasibility of such technology for a manufacturing environment, but also to show significant benefits over state-of-the-art Si CMOS technology which is a steadily improving target.

The aim of this study is to assess the possibility of introducing a hybrid InGaAs/SiGe technology platform for CMOS applications by addressing the different material and integration challenges associated with its realization, in the context of a potential future high-volume manufacturing. The remaining sections of this introduction will present these challenges in detail and put in context the different technical chapters which are addressing the material integration aspects to obtain InGaAs on Si substrates, the main device architecture requirements to introduce InGaAs MOSFETs into CMOS circuits, and the co-integration challenges associated with a hybrid InGaAs/SiGe technology.

## 1.2 Challenges and solutions to integrate InGaAs on Si

Given the industrial ecosystem which exists around Si technologies, it is extremely unlikely that future mainstream CMOS technology would be manufactured on other substrates than Si wafers. Therefore, III-V semiconductors, and more particularly InGaAs for CMOS applications, *must* be integrated on Si. The resulting III-V material quality should be high enough to enable fabricating high performance devices comparable to what can be obtained on native substrates, with a high yield and low variability. Three main intrinsic material challenges make InGaAs integration on Si a very complex problem:

- The coefficient of thermal expansion of InGaAs is about 2.2 times larger than that of Si. Since InGaAs epitaxy is usually performed at elevated temperatures (500°C to 650°C), a large amount of strain can be induced in the InGaAs layer once cooled down to room temperature. If the strain-level is too high in relation to the InGaAs thickness, it might relax through the formation of micro-cracks or dislocations. In general, this effect can become problematic for layers thicker than 2 to 3 $\mu$m.

- III-V semiconductors are polar crystals as they contain both group-III and group-V elements, while Si (or SiGe) is a non-polar crystal since it is only formed from group-IV elements. The growth of a polar crystal on a non-polar semiconductor might lead to the undesirable formation of multiple anti-phase domains whose boundaries are crystalline planar defects which can extend from the growth interface to the surface. Those defects are generally nucleated at the edge of single atomic steps which are present on the surface of the initial non-polar substrate. The density of anti-phase boundaries can be mitigated either by having a single domain (grown from a seeding point smaller than a terrace length or from a perfectly atomically smooth surface), or by having a non-polar crystal surface reconstruction which forms double atomic steps.

- InGaAs, in its compositional range of interest (from 50%-In to 75%-In), presents a large lattice mismatch with Si of 8% to 10%. This difference in lattice parameter induces a high level of strain which can lead to the formation of linear or planar defects such as misfit and threading dislocations, stacking faults or micro-twins. Crystalline defects can form at the heterointerfaces when the strain is abruptly relaxed, or can develop during the growth of the buffer layers in the case of a gradual relaxation. Therefore, strain relaxation and defect filtering should be carefully engineered to prevent crystalline defects from reaching the active device layers.

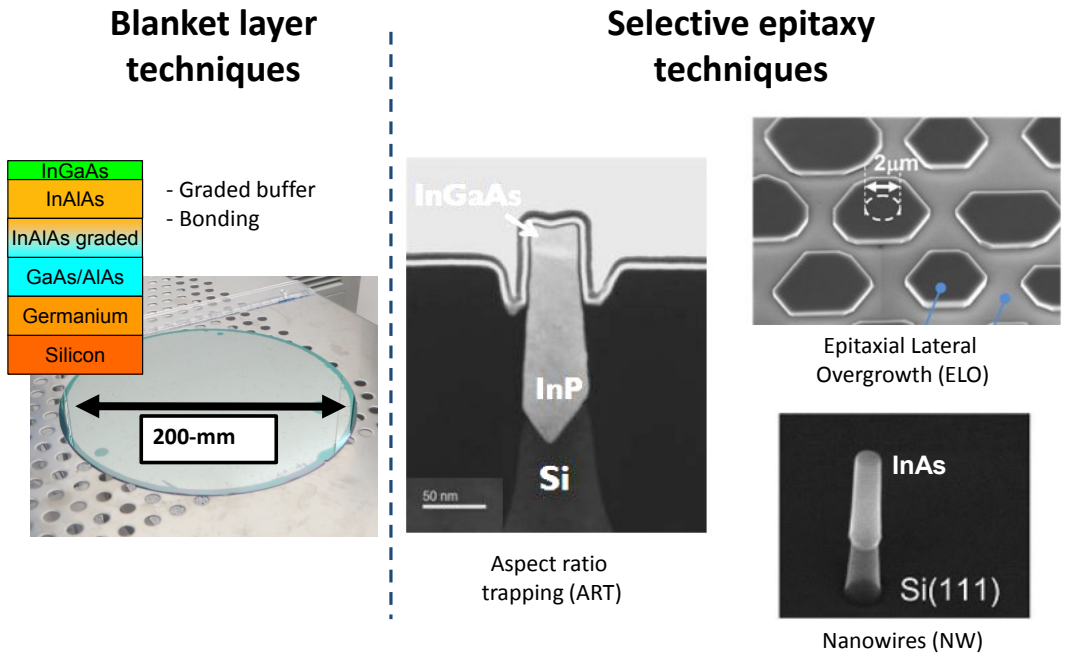



**Figure 1.1:** Overview of different methods to integrate InGaAs on Si substrates. Images taken from: blanket and bonding [7], aspect ratio trapping (ART) from [8], epitaxial lateral overgrowth (ELO) from [9] and nanowire (NW) from [10].

In order to circumvent these challenges, numerous integration approaches have been developed. They can be classified into two main categories, relying either on the use of blanket layers or local selective epitaxy (see Fig. 1.1).

The integration of InGaAs on Si as blanket layers only relies on an engineered epitaxy process to mitigate the formation of crystalline defects and to prevent their propagation to the active device layer. It is using thick strain-relaxed buffer (SRB) layers to gradually accommodate the lattice mismatch and relax the strain. Different strategies are possible to reach the lattice parameter of InGaAs (50%-In to 75%-In) on a Si wafer. For instance, a Ge layer can be used to handle the first 4% of mismatch, followed by a lattice matched galium-arsenide (GaAs) to switch from non-polar to polar crystals and finally an indium-aluminum-arsenide (InAlAs) layer of graded In-content to attain the lattice constant of targeted InGaAs composition [11].

The use of direct wafer bonding (DWB) is another method to obtain blanket layers of InGaAs on a Si substrate [12]. If the donor wafer is a III-V native substrate, a perfect material quality can be achieved. Since III-V native substrates only exist in small diameters, this technique is not applicable for large-scale CMOS applications. Recently, it has been demonstrated that InGaAs on Si blanket layers obtained by SRB can be used

as donor wafers for DWB [7, 11, 13, 14].

All blanket-layer techniques (including bonding from a SRB donor wafer) suffer from the same limitation: the density of crystalline defects cannot be reduced beyond a certain limit (low $10^8$ $cm^{-2}$ for InGaAs (with 53% of indium) ($In_{0.53}Ga_{0.47}As$) on Si) as the mitigation of defect formation can only be achieved by engineering the 2D epitaxial process itself.

Local selective epitaxy techniques propose to circumvent this limitation by combining the flexibility of nano-fabrication techniques with the engineering of the epitaxy process. As such, nano-fabricated structures can assist in mitigating defect formation, filtering or confining existing defects, and shaping the grown crystal. In addition, local selective epitaxy integrate micron-sized III-V crystals only where required which, compared to blanket layers, might reduce costs and simplify CMOS integration. It can also be seen as a common weakness of all local selective epitaxy techniques: it is very difficult to obtain large-area III-V crystals (more than a few microns).

Aspect ratio trapping (ART) [15] attracted a lot of attention recently [8]. It is based on the growth of III-V crystals in narrow silicon-oxide ($SiO_2$) trenches on Si, having a high aspect-ratio. Indeed, it was proposed that a high-enough aspect-ratio can terminate the propagation of crystalline defects at the $SiO_2$ sidewalls [16]. Excellent material quality could be obtained for indium-phosphide (InP) grown on 300 mm Si substrates [17].

In the epitaxial lateral overgrowth (ELO) method, the growth is initiated from a seed region opened in an oxide mask. In this region, a high density of crystalline defects are generated. The growth conditions are tuned to promote lateral growth rather than vertical growth. Therefore, the III-V crystal develops laterally above the oxide mask, leaving most crystalline defects confined in the crystal above the seed region. A high material quality is obtained in the laterally overgrown region which can be used as the active device layer [9, 18].

Another approach is to define small seed regions in an oxide mask to selectively grow III-V NWs. Their 3D geometry and small interfacial cross-section with the substrate ensure an efficient relaxation of strain which minimizes the formation of crystalline defects. It enables the realization of vertical devices [10, 19], which is an interesting option for future scaled CMOS technologies which might evolve in this direction.

Chapter 2 will be devoted to the integration of InGaAs on Si substrates to enable the realization of hybrid InGaAs/SiGe CMOS circuits, favoring techniques giving on-insulator layers. DWB will be investigated as a first option, and the challenges associated to its large-scale manufacturing will be addressed. Then, a novel integration scheme based on local selective epitaxy of III-V materials in empty oxide cavities will be proposed and

demonstrated.

## 1.3 Requirements for self-aligned MOSFETs

Extensive investigations exist in the literature on the fabrication and characterization of InGaAs n-MOSFETs. Numerous device architectures have been proposed and the vast majority of them were designed with the following guideline: find a device architecture which will simplify the process as much as possible while maximizing the device performance in order to experimentally prove the high expected potential of III-V MOSFETs for future CMOS applications.

This approach is very valuable for the scientific and industrial community as it allows to demonstrate InGaAs-based hardware exceeding the performance of Si MOSFETs. In the device architecture which appeared to be the most successful to achieve record performances [20–23], the S/D regions are formed first either by etching an already existing blanket layer of highly-doped InGaAs or by selectively growing it ; then the gate region is defined by lift-off with a large overlap with the contact regions. The resulting device has S/D regions self-aligned to the channel which ensures a low access resistance and thus a high performance, but not self-aligned to the gate.

All those "performance-optimized" architectures have in common the fact that they do not meet the requirements for large-scale manufacturing of CMOS circuits. They typically cannot be scaled down to aggressive pitch and contain a large and uncontrollable gate to S/D overlap. Nevertheless, they represent today's state-of-the-art InGaAs n-MOSFET performance [20], exceeding that of production Si n-MOSFETs.

In this thesis, it is decided from the beginning to focus on enabling InGaAs MOSFETs integration into CMOS platforms rather than using any means for achieving record performance. Therefore, the priorities are to first demonstrate CMOS-compatible self-aligned InGaAs MOSFETs on Si, then optimize the process for higher performance. The results will show record performance among all existing CMOS-compatible InGaAs MOSFETs on Si, but still behind that of "performance-optimized" InGaAs MOSFETs architectures on native III-V substrates.

The baseline device architecture selected in this work matches IBM's Alliance 22 nm gate-first (GF) fully-depleted silicon on insulator (FDSOI) technology [24], shown in Fig. 1.2. The high-k metal-gate (HKMG) stack is first formed on the channel, followed by dry etching of the gate. Ultra-thin spacers are formed on each side of the gate acting as a lateral isolation to the S/D. An *in-situ* doped selective epitaxy of Si and SiGe raised S/D (RSD) is carried out on n- and p-MOSFETs respectively. Dopants from S/D are diffused

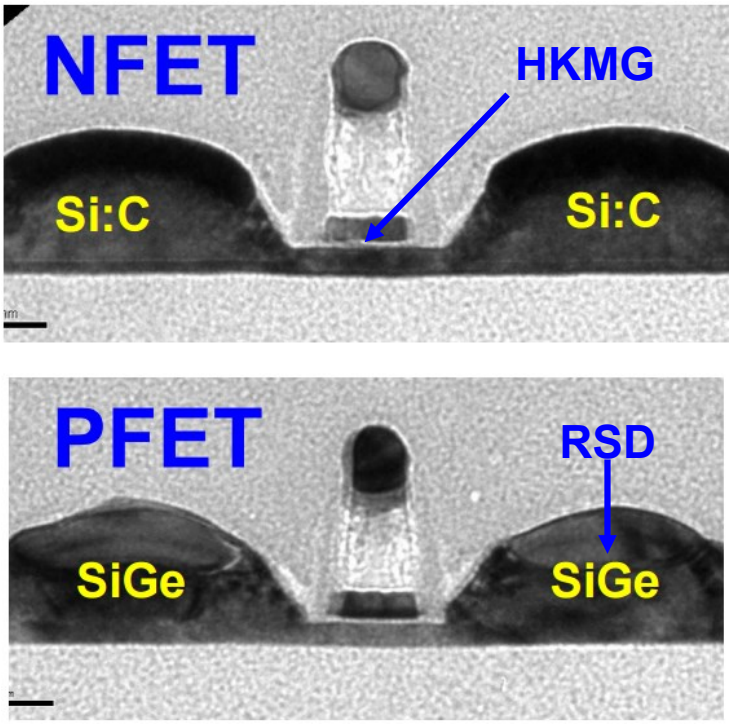



**Figure 1.2:** Transmission electron microscopy (TEM) cross-sectional view of gate-first (GF) fully-depleted silicon on insulator (FDSOI) n- and p-MOSFETs taken from [24].

underneath the spacers via a high temperature spike anneal. Finally, self-aligned nickel silicides are formed on the doped RSD, completing the front-end-of-line (FEOL) process. Tungsten plug contacts are realized and the back-end-of-line (BEOL) interconnects complete the chip fabrication. With this integration flow, the entire device is fabricated in a self-aligned way around the gate line. No lithography steps are required to position the S/D regions relative to the gate, and the gate to S/D overlap can be controlled by the spacer thickness and dopant diffusion.

In Chapter 3, it is proposed to adapt this baseline architecture for InGaAs n-MOSFETs by developing InGaAs-compatible HKMG stacks, replacing Si RSD by *in-situ* n-doped InGaAs RSD and by introducing self-aligned Ni-InGaAs metal contacts. Direct metal contacts to InGaAs for connecting the devices to the BEOL interconnects are also studied as an alternative to Ni-based alloyed contacts.

Based on those developed process modules, CMOS-compatible self-aligned InGaAs MOSFETs are fabricated and characterized in Chapter 4. Various device architectures are studied: bulk vs on-insulator, planar vs fins, GF vs replacement metal-gate (RMG), junction-less (JL) devices vs MOSFETs.

## 1.4 Hybrid CMOS circuits

The development of a low-power high-performance CMOS technology based on high mobility channels cannot be made exclusively out of InGaAs as channel material.

Firstly, InGaAs has a poor hole mobility, lower than that of Si, and cannot act as a "high-mobility" p-type MOSFET. The use of SiGe is currently the most promising option for future CMOS technologies [5], outstanding device performance is already demonstrated in p-type SiGe fin-based MOSFETs (FinFETs) [25–27]. It is therefore envisioned to build a hybrid CMOS technology with n-type InGaAs MOSFETs and p-type SiGe MOSFETs, where the In- and Ge-contents would be increased from generation to generation, providing higher mobility, higher strain and lower operating voltage. Another potential candidate for high-mobility p-type MOSFETs is galium-antimonide (GaSb), but it does not have a better hole mobility than Ge, has a much larger lattice mismatch and has a poor thermal stability limited to about 450°C. For those reasons, an hybrid InGaAs/SiGe technology remains the preferred approach.

Secondly, a CMOS chip does not only contain low-power high-performance core logic devices. It also needs high-voltage components such as I/O devices or protection circuits against electrostatic discharges. Those components are based on Si MOSFETs which can sustain much higher voltages than the core logic devices. Lower bandgap materials such as InGaAs or SiGe are not good candidates to realize those devices as a high breakdown voltage requires a wide bandgap. Therefore, a high-mobility CMOS technology is a true hybrid platform which not only needs to integrate InGaAs with SiGe but also with Si, on Si.

Numerous technology integration challenges have to be tackled. Firstly, the fabrication of MOSFETs on Si, SiGe and InGaAs requires very different thermal budgets. Si needs about 1100°C, SiGe requires around 950°C at 25%-Ge, 750°C at 50%-Ge and maybe 500°C for pure Ge, while InGaAs is limited to approximately 600°C. The boundary conditions for those thermal budgets have a different nature, some are related to a minimum temperature to efficiently activate dopants, some to obtain reliable gate stacks, some are limited by dopant diffusion or by intrinsic material degradation. Secondly, those three materials have very heterogeneous chemical properties. Most of the standard wet cleans and dry etching modules have to be adapted to provide the right selectivities to each material. For instance, the standard SC-1 and SC-2 for Si wet cleaning steps or the usual gate dry etching steps attack InGaAs at a very high rate. Removing these cleaning steps might largely impact the standard processes to fabricate Si and SiGe devices, yet compromising performance should be avoided. Finally, the method used to integrate InGaAs

on a Si platform should not limit density scaling. The main driving force behind the development of advanced technology nodes is the increase of the number of transistors per unit area. A transition to InGaAs-based n-MOSFETs should support the development of smaller, denser and faster chips ; it cannot compromise integration density. Each material integration scheme discussed in the introduction section 1.2 or in Chapter 2 has its own boundary conditions in terms of integration density which need to be jointly evaluated with the circuit designs. Indeed, it might not be required to replace every single low-power high-performance Si n-MOSFET by its InGaAs counterpart. In some possible scenarios, only a few percent of InGaAs devices might need to be introduced, which could completely change the preferred material integration method.

Very few reports exist on hybrid InGaAs/SiGe CMOS technology platforms as it is a complex and challenging milestone. Two circuit architecture are envisioned: 2D co-planar and 3D monolithic circuits. The 2D co-planar architecture is the industry-standard approach where both types of devices are co-processed simultaneously, at the same level on the wafer. In the case of the 3D monolithic architecture, two (or more) layers of transistors are stacked on top of each other, sharing a common BEOL. These two approaches have very different requirements in terms of thermal budget, number of lithography steps, process complexity and density of integration. These two architectures have already been demonstrated in the form of 2D co-planar InGaAs/Ge MOSFETs bonded on a Ge substrate [28], 3D monolithic InGaAs/Ge inverters on Ge wafers [29] and 3D monolithic InGaAs/SiGe ring-oscillators on Si substrates [30]. Although those demonstrations pave the way towards a manufacturable InGaAs/SiGe CMOS technology, they are using very primitive fabrication processes and low thermal budgets to circumvent the real challenges of co-integration, which results in poor performance compared with what can be achieved in stand-alone InGaAs MOSFETs.

In the last Chapter 5, we will address both 2D co-planar and 3D monolithic circuit architectures to demonstrate hybrid InGaAs/SiGe CMOS circuits on Si. DWB will be used to establish a primitive 2D co-planar platform, which will then be further developed into dense static random access memory (SRAM) arrays obtained by local selective epitaxy, featuring a full-scale process for the n-MOSFETs. Finally, DWB enables the 3D monolithic integration of InGaAs n-MOSFETs on state-of-the-art SiGe p-MOSFETs, with an independently optimized full-scale fabrication process for each device layer achieving excellent performance.

## 1.5 Thesis: Organization and relation to published work

The technical work is presented in four chapters following the main different aspects of the realization of a hybrid InGaAs/SiGe CMOS technology platform: Substrates, Process Modules, Devices and Circuits. The next paragraphs link the content of the technical chapters to the most relevant published work. A detailed list of published contributions can be found in Appendix A.

**Chapter 2, "Substrates"**, presents all the material developments performed in this work to integrate thin layers of InGaAs on Si substrates for subsequent device and circuit fabrication. This chapter is composed of two parts on wafer bonding of blanket layers, and local selective epitaxy in empty oxide cavities. The work on wafer bonding is mainly supported by reports at the International Electron Device Meeting [31], in Applied Physics Letters Materials [11], and at the VLSI Technology Symposium [13]. The part on selective epitaxy in empty oxide cavities refers to a report at the VLSI Technology Symposium [32].

**Chapter 3, "Process Modules"**, focuses on the most relevant process modules for the realization of high-performance self-aligned InGaAs MOSFETs. The first part presents development of HKMG stacks on InGaAs, the second part reports on the developments of self-aligned S/D regions and metal contacts. The work on HKMG stacks is mainly supported by reports in Applied Physics Letters [33, 34], in Microelectronic Engineering [35] and Solid State Electronics [36]. The part on S/D regions is mostly covered in Solid State Electronics [37].

**Chapter 4, "Devices"**, reports on CMOS-compatible self-aligned InGaAs MOSFETs with evolving device architectures towards higher performances: bulk vs on-insulator, planar vs tri-gate, gate-first vs replacement-gate. Those devices are covered in reports at the International Electron Device Meeting [31], at the VLSI Technology Symposium [13, 32], at the European Solid-State Device Research Conference [38], at the Device Research Conference [39] and in Electron Device Letters [40].

**Chapter 5, "Circuits"**, demonstrates several implementations of hybrid InGaAs/SiGe CMOS circuits based on wafer bonding of blanket layers or local selective epitaxy, in 2D and in 3D configurations. Those developments are mainly reported at the International Electron Device Meeting [31, 41, 42]. Part of this work is also submitted for the VLSI Technology Symposium in 2016 [43].

# Chapter 2

# Substrates: InGaAs Integration on Si

## 2.1 Introduction

This chapter focuses on the material integration aspects of InGaAs on Si. The targets are to provide high-quality material on a Si platform, using processes which can be used in a manufacturing environment. The proposed solutions need to be cost-effective and take into account the process integration restrictions imposed by the large-scale fabrication of CMOS circuits. Two methods are proposed to integrate InGaAs either as blanket layers on large-scale substrates or as local micron-sized patches.

Firstly, direct wafer bonding (DWB) is explored in section 2.2 to fabricate InGaAs-on-insulator (InGaAs-OI) substrates on the same model as the industry-standard SOI substrates. The base layer transfer technology is developed and optimized to yield robust bonded interfaces and high thermal stability. A path towards large-scale manufacturing is demonstrated through the recycling of the donor wafers and the realization of 200 mm InGaAs-OI substrates. The fabrication of hybrid InGaAs/SiGe CMOS circuits is enabled by the proposed concept of dual-channel substrates.

Secondly, a local epitaxy technique in empty oxide cavities in proposed in section 2.3. It relies on the direct selective epitaxy of InGaAs on Si and yields micron-sized islands of InGaAs, where it is required in the CMOS circuit layout. This method is inherently compatible with the large-scale manufacturing requirements of the CMOS industry.

The material developments presented in this chapter are the basis for all InGaAs on Si device and circuit demonstrators reported in this thesis.

## 2.2 Direct Wafer Bonding

The development of DWB was pushed by the need of the microelectronic industry for SOI substrates. The concept is to bring the surface of a donor and of a target wafer into intimate contact in order to create a strong bond between the two substrates. The donor wafer is then submitted to some treatments in order to realize the transfer of an active layer from the donor wafer to the target wafer. During this treatment, the donor wafer might be preserved and re-used, or destroyed.

In the case of SOI substrates fabrication, the bonding between the two Si wafers is obtained through an oxide layer. $SiO_2$ is grown or deposited on the surface of the target and/or donor wafer, the two surfaces are made hydrophilic through a wet clean process, and the wafers are bonded at room temperature. The bonding is obtained through the formation of H-bonds which are converted into Si-O bonds (through the release of some hydrogen or water at the interface) upon thermal treatment. Finally, part of the donor wafer is removed leaving a Si layer on top of the oxide layer (named buried oxide (BOX)) on the target Si wafer. The main challenges are the control of the final thickness, roughness and uniformity of the top Si layer as well as the removal of the donor wafer in a cost-efficient manner.

This technique became the industry-standard method for the fabrication of SOI substrates with the development of SmartCut$^{TM}$[44]. It is a cost-efficient donor wafer release technique based on H-implantation, which provides an accurate control of the top Si thickness, roughness and uniformity without sacrificing the donor wafer: it can be recycled and serve for several subsequent bonding steps.

DWB is a very versatile technique that enables the integration of diverse materials on diverse substrates: strained SOI [45], hybrid orientation composite SOI [45], germanium-on-insulator [46], silicon on lattice engineered substrates [47], and many others.

The integration of III-V materials on insulator on Si by DWB has been an active field of research since the 1980's mostly driven by optoelectronic applications. Its use for CMOS applications was introduced in [12] in 2009 with the demonstration of ultra-thin InGaAs-OI layers for the fabrication of n-MOSFETs. Inspired from this demonstration, the work presented in this thesis focused on several key aspects of the realization of ultra-thin body and BOX (UTBB) InGaAs-OI on Si substrates:

- Thickness and roughness control of the transferred layer (section 2.2.1)
- High thermal stability such that the InGaAs top layer can act as a virtual substrates for III-V epitaxy (section 2.2.2)

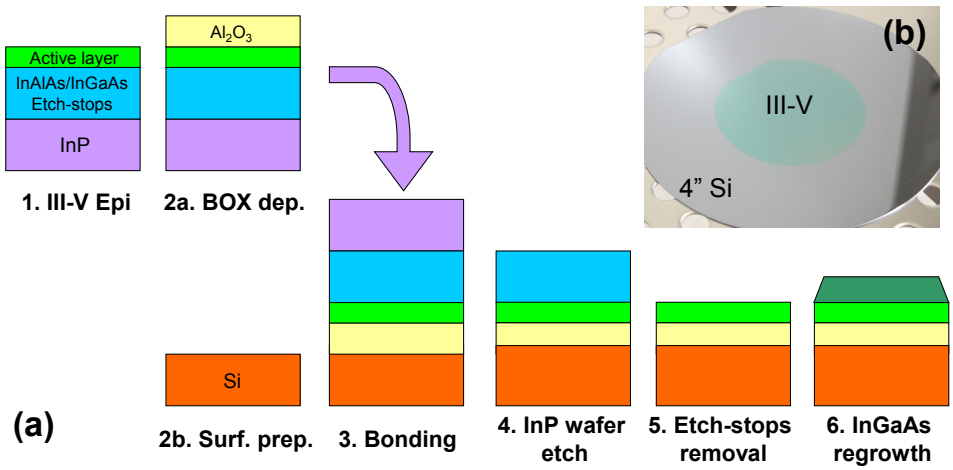



**Figure 2.1:** (a) Schematic process flow of the fabrication of UTBB InGaAs-OI substrates (1 to 5) and InGaAs regrowth module for S/D regions (6). (b) Picture of an InGaAs-OI substrate.

- Recycling of the donor wafer (section 2.2.3)
- Up-scaling path towards 300/450 mm substrates (section 2.2.4)
- Co-integration with ultra-thin SiGe layers (section 2.2.5)

### 2.2.1 Layer transfer of III-V heterostructures to Si wafers

The fabrication of an InGaAs-OI on Si wafer (described in Fig. 2.1) starts with a 2" semi-insulating high-grade (100)-oriented InP donor wafer loaded in a metal-organic vapor phase epitaxy (MOVPE) system. An etch-stop heterostructure composed of InGaAs, InAlAs and InP is grown at 550°C followed by the growth of the active layer of a certain target channel thickness $t_{ch}$. The active layer can be either an InGaAs layer or an heterostructure composed of InGaAs, InAlAs and InP (to form quantum wells, top or bottom barriers, etc.). Subsequently, the donor wafer is loaded in an atomic layer deposition (ALD) chamber where the BOX is deposited at temperatures ranging from 250°C to 300°C. ALD deposition is chosen for its low thermal budget, excellent thickness control and extremely low surface roughness.

The BOX is always deposited on the donor wafer so that the III-V/BOX interface can be engineered for low density of interface traps ($D_{it}$). For instance, an optimized MOS stack can be deposited at the InGaAs/BOX interface (from Chapter 3 section 3.2.3, used in Chapter 4 section 4.3.2), or a wider bandgap semiconductor barrier layer can be introduced (used in Chapter 4 section 4.2). Optionally, part of the BOX layer can also be deposited on the target Si wafer (see section 2.2.2).

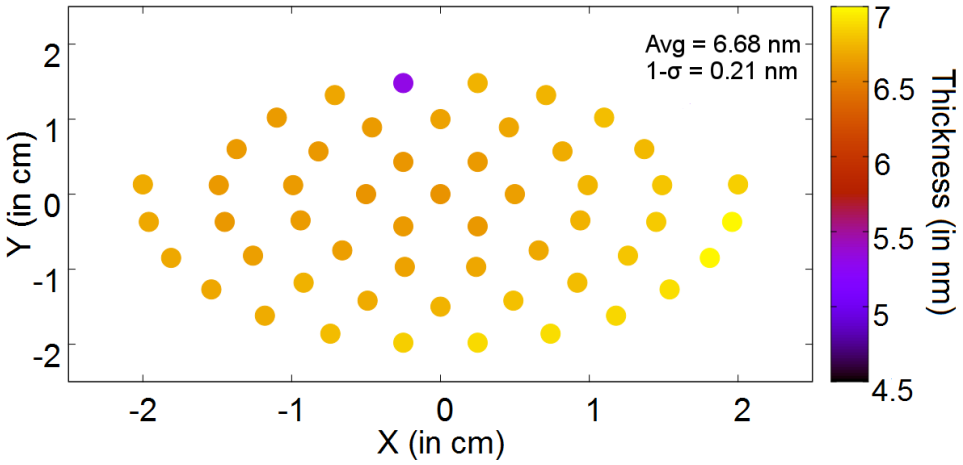



**Figure 2.2:** Ellipsometry thickness mapping of a 7 nm $In_{0.53}Ga_{0.47}As$ active layer on a 10 nm BOX on Si after etch-stop removal.

The target 4" (100)-oriented n-type ($n$-type dopant density ($N_d$) = $1\times10^{17}$ $cm^{-3}$) Si wafer is wet cleaned for organic contaminants and its native oxide is stripped in diluted hydrofluoric acid (DHF). A thin and high quality native oxide is then chemically regrown by exposing the wafer to ozone-rich dionized water ($DIO_3$), making its surface hydrophilic. The donor and target wafer surfaces are brought into intimate contact at room temperature and ambient atmosphere to initiate the bonding. The wafers are then annealed at 300°C for 2 hours in order to raise the bonding energy. The InP donor wafer is then etched in concentrated hydrochloric acid (HCl) until reaching the InGaAs/InAlAs etch-stop heterostructure, which is etched in diluted acids to ensure a soft-landing on the active layer. It yields the final InGaAs-OI substrate.

It is worth mentioning that this fabrication process ensures that: 1) the BOX thickness variability is extremely well controlled due to the nature of ALD deposition, 2) the thickness and composition variability of the active layer is defined by the MOVPE growth step, and 3) the surface roughness of the transferred layer is defined by the wet etch selectivity, the over-etch time, and the interface abruptness between the active layer and the underlying layer (controlled by the epitaxy conditions).

This process enables the transfer of a wide variety of InGaAs/InAlAs/InP heterostructures on insulator on Si including ultra-thin InGaAs layers of various composition and thickness, 2D electron gas heterostructures and infrared detector and laser stacks. To illustrate the controllability of the process, an example of an ellipsometry mapping of the thickness of an aggressively-scaled UTBB InGaAs-OI substrates with 7 nm $In_{0.53}Ga_{0.47}As$ and 10 nm BOX is shown in Fig. 2.2. Without any particular optimization towards im-

proved uniformity, a remarkable 1-$\sigma$ standard deviation of 2 Å is observed over the 2" transferred area. The standard deviation mainly arises from a temperature gradient of about 3°C across the wafer in the MOVPE system, which translates into a thickness gradient from the center of the wafers towards the bottom right edge. Thickness control of the channel is a crucial aspect of a DWB technology as the $V_T$ of MOSFETs can be strongly affected by thickness variations. A rate of 25 mV/nm was observed in [48].

High-resolution x-ray diffraction (XRD) is used on the InGaAs-OI on Si substrates to characterize the InGaAs thickness, composition and strain. $\omega - 2\theta$ scans around the (004) reflection of the InGaAs films are performed. An incident wavelength ($\lambda$) of 1.5415 Å emitted by a high intensity rotating anode is used with a Ge (022) monocrystal as a monochromator. The central and most intense diffraction peak corresponds to the (004) reflection of the InGaAs crystal. The angular position of this peak in $2\theta$ gives a direct information on the out-of-plane lattice constant ($a_\perp$) of the material based on the following relationship:

$$a_\perp = \lambda/2 \times \sin(2\theta/2) \tag{2.1}$$

In the case of a fully relaxed InGaAs film, its in-plane lattice constant ($a_\parallel$) and $a_\perp$ are the same. This lattice constant ($a_0$) can be related to an indium-content ($x$) following Vegard's law (interpolating between GaAs and indium-arsenide (InAs)):

$$a_0 = a_{InAs} \times x + a_{GaAs} \times (1 - x), \text{ where } x = In/(In + Ga) \tag{2.2}$$

In the case of a fully strained InGaAs film, its $a_\parallel$ will be the one of the original donor substrate ($a_{sub}$) and the out-of-plane lattice constant will be related to the in-plane lattice constant by the Poisson modulus ($\nu$) of the material (assumed to be $\nu = 0.33$ for InGaAs). In order to determine the indium-content of the material, we derive the lattice constant ($a_0$) that the material would have if it would have fully relaxed its strain with the following relation taken from [49]:

$$a_0 = \frac{(1-\nu) \times a_\perp + 2 \times \nu \times a_\parallel}{1+\nu}, \text{ where } a_\parallel = a_{sub} \tag{2.3}$$

From Eq. (2.2), $a_0$ can now be related to a corresponding indium-content. Based on those two simple models, a calibration plot is realized to relate the indium-content to its XRD (004) $2\theta$ diffraction angle for the two extreme cases of a fully relaxed InGaAs layer and a fully strained InGaAs layer to the lattice constant of an InP donor substrate (Fig. 2.3).

For materials having a high crystal quality and a low-enough surface roughness, finite

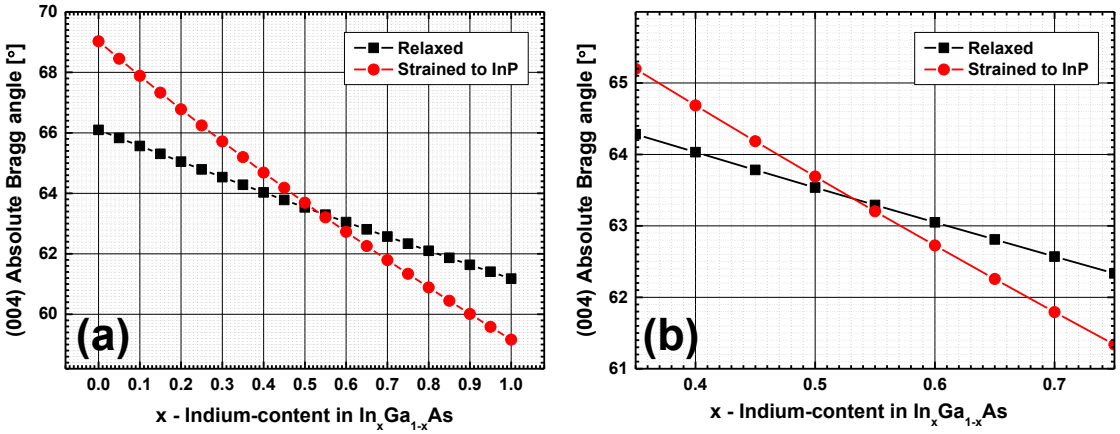



**Figure 2.3:** (a) Calculated $2\theta$ (004) diffraction angle in high-resolution XRD for InGaAs of varying indium-content when fully relaxed (black squares) or fully strained to the lattice constant of InP (red circles). (b) Magnified plot of (a) around the lattice matched conditions to InP.

size oscillations can be observed as periodic satellite peaks around the main diffraction peak. The period of those oscillations is related to the layer thickness $t_{ch}$ by the following relation:

$$t_{ch} = \frac{\Delta_n \times \lambda}{2 \times (\sin 2\theta_1 - \sin 2\theta_2)} \tag{2.4}$$

where $2\theta_1$ and $2\theta_2$ are two satellite diffraction peaks chosen on the same side of the main diffraction peak and $\Delta_n$ is the number of finite size oscillation periods between those two peaks.

Figure 2.4 presents XRD $\omega - 2\theta$ scans on the (004) reflection of InGaAs-OI substrates with a nominal 75% indium-content and various nominal $t_{ch}$ thickness (5 nm, 10 nm and 20 nm) below the theoretical critical thickness [50]. The InGaAs-OI films are therefore expected to be fully-strained. All samples present a main (004) $\omega - 2\theta$ diffraction peak at the same position which suggests that they are fully strained as strain relaxation would be expected to depend on the thickness. This assumption is confirmed by a measurement of the in-plane lattice constant on asymmetric (115) reflections (not shown).

### 2.2.2 Thermal stability of InGaAs-OI layers and regrowth

For the technology developments envisioned in this work, it is required that the InGaAs-OI substrates present a high-enough thermal stability to serve as virtual III-V substrates for subsequent III-V epitaxy step. This paragraph reports on a study carried out to improve the bonding energy in order to fulfill the CMOS technology requirements.

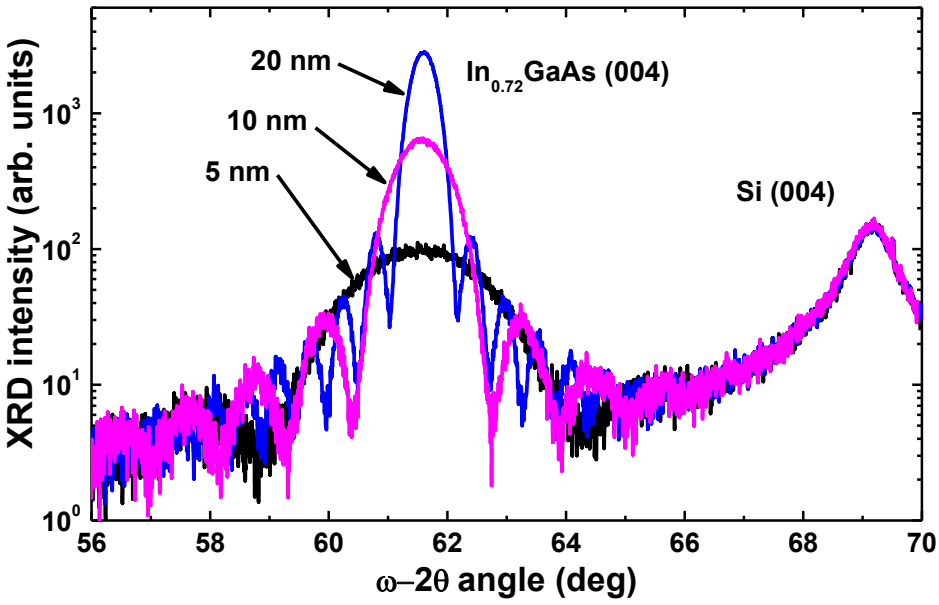



**Figure 2.4:** High-resolution XRD $\omega - 2\theta$ scans on the (004) reflection of InGaAs-OI substrates with a high indium-content and various nominal thickness. The diffractometer is aligned to the InGaAs reflection which explains the low amplitude of the Si signal.

The thermal expansion coefficient of InGaAs being twice as large as the one of Si, special care has to be taken about the bonding energy at low and high temperatures. Firstly, when bonding an InGaAs layer from an InP wafer, it is not possible to anneal the bonded wafer pair above 400°C otherwise the InP donor wafer breaks (contrary to SOI substrates that can be annealed at high temperature to improve the bonding energy). It implies that a high enough bonding energy needs to be achieved at temperatures below 400°C to enable the layer transfer process. Secondly, the bonding energy after layer transfer needs to be sufficient to overcome the stress induced during any high temperature process steps otherwise the InGaAs film will relax its compressive stress by forming a high density of delaminated "bubbles". InGaAs/InAlAs/InP epitaxy is typically carried out at growth temperatures ranging from 500°C to 650°C. For the envisioned process integration flow, the highest temperature seen by the InGaAs-OI substrates corresponds to the RSD module occurring at a maximum growth temperature of 600°C.

For that purpose, a set of 4" Si wafers bonded pairs are prepared with different bonding interfaces. For two sets of pairs, the surface of the Si target wafers is wet cleaned in order to form a thin, high-quality, chemically grown oxide, while a thermal $SiO_2$ oxide layer is grown or an $Al_2O_3$ oxide layer is deposited by ALD on the donor wafers. For a third set of pairs, an aluminum-oxide ($Al_2O_3$) oxide layer is deposited by ALD on

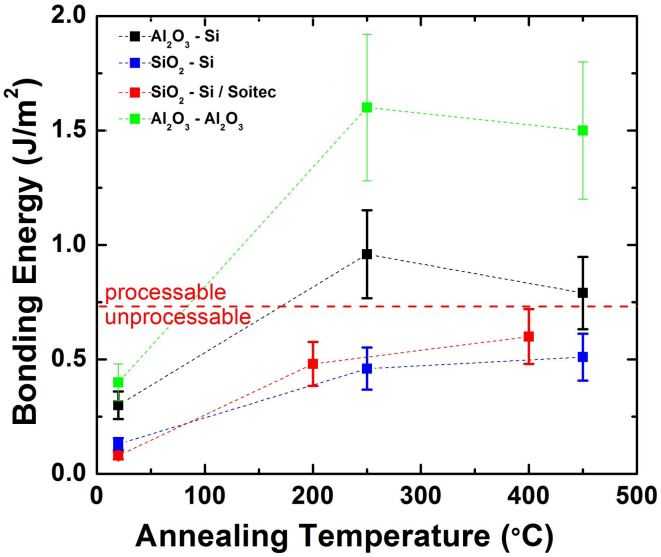



**Figure 2.5:** Bonding energy versus post-bonding annealing temperature for aluminum-oxide ($Al_2O_3$)-Si, $Al_2O_3$-$Al_2O_3$ and $SiO_2$-Si bonded pairs of wafers. No Plasma activation of the surface is done before DWB. For comparison, $SiO_2$-Si bonding energy data reported by SOITEC are included [51]. The red dashed line indicate the empirical minimal bonding energy required to enable device processing up to 600°C.

both donor and target wafers. Each pair of wafers is subjected to an annealing step at various temperatures ranging from room temperature to 450°C. The bonding energy is then extracted for each bonded pair using the Mazara's crack opening method [52] and plotted versus annealing temperature in Fig. 2.5.

The bonding energy of the $Al_2O_3$-based BOX is higher than that of the $SiO_2$-Si pair, in the temperature process window which prevents the InP wafer from breaking during annealing. One can see that after a 250°C annealing, the bonding energy of the $Al_2O_3$-Si pair almost reaches the value of 1 J/m$^2$ and 1.5 J/m$^2$ for the $Al_2O_3$-$Al_2O_3$ pair. It is possible to successfully process InGaAs-OI substrates for device fabrication up to 600°C by using $Al_2O_3$ BOX. Unlike with the $SiO_2$-Si substrate where the bonding energy is too weak and yields the delamination of the film, and its melting if the channel thickness is below 10 nm. It is therefore empirically estimated that the required minimal bonding energy for processing at 600°C is around 0.75 J/m$^2$. For all the further InGaAs-OI experiments presented in this thesis, an $Al_2O_3$ BOX is used and in most cases the bonding interface is an $Al_2O_3$-$Al_2O_3$ pair.

The high bonding energy obtained is expected to lead to an efficient transfer of the thermally-induced stress from the Si substrate to the thin InGaAs-OI layer during high temperature process steps. This stress could be relaxed through the formation of crys-

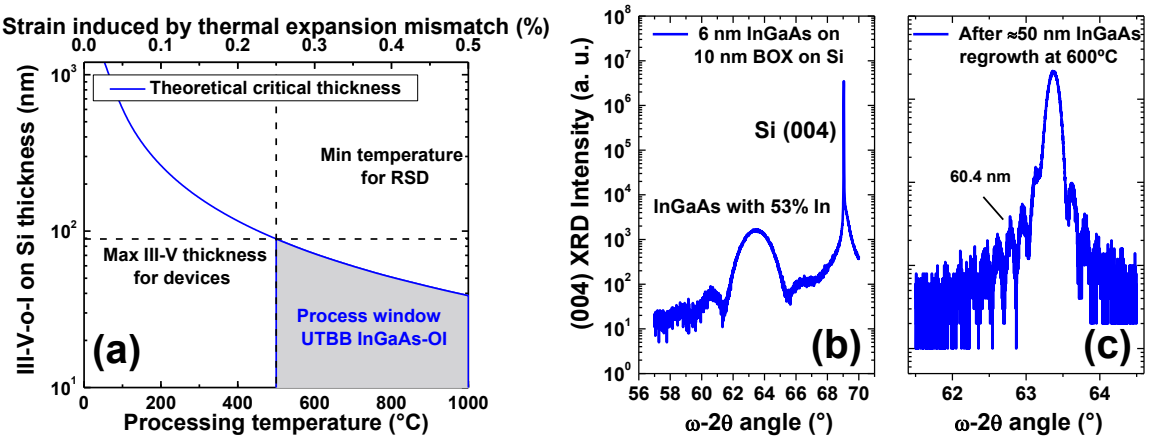



**Figure 2.6:** (a) Critical thickness in thermodynamic equilibrium [50] of InGaAs-OI on Si vs processing temperature. The strain is estimated from the processing temperature through thermal expansion mismatch assuming no relaxation in the BOX or at the bonding interface. (b) High resolution XRD $\omega - 2\theta$ scans on the (004) reflection of InGaAs-OI after layer transfer and (c) after about 50 nm in-situ Si doped $In_{0.53}Ga_{0.47}As$ regrowth by MOVPE at 600°C.

talline defects in the InGaAs layer that would be detrimental for the device performance. In Fig. 2.6(a), we estimated the compressive strain seen by InGaAs as a function of processing temperature assuming that the wafer pair is bonded at room temperature and that 100% of the strain due to thermal expansion mismatch is transferred to InGaAs (Si is unstrained and no strain relaxation takes place in the BOX). The critical InGaAs thickness below which no plastic deformation should occur is estimated by the Matthews-Blakeslee model [50]. It suggests that for a channel thickness below 100 nm, the crystalline quality should be maintained at temperatures of 500°C-650°C that are typical for InGaAs/InAlAs/InP epitaxy. Given the assumptions described above (no relaxation in the BOX and at the bonding interface) and the model used (assuming thermodynamic equilibrium), the calculated critical thickness is under-estimated. In practice, it is observed that layers up to 300 nm can be annealed at 600°C without degradation of the crystalline quality.

An UTBB InGaAs-OI on Si substrate is prepared with a 6 nm $In_{0.53}Ga_{0.47}As$ channel on a 10 nm thick $Al_2O_3$ BOX. An $Al_2O_3$-Si interface is used for the bonding and subsequently annealed at 300°C for 2 hours. The substrate is placed in the MOVPE system and first submitted to a 600°C anneal for 5 minutes under tertiarybutylarsine (TBA) overpressure and cooled down to room temperature. Subsequently, an $In_{0.53}Ga_{0.47}As$ regrowth at 600°C for 7 minutes is performed, yielding approximately 50 nm growth. The substrate is analyzed before and after regrowth by XRD (Fig. 2.6(b) and (c)). It clearly confirms

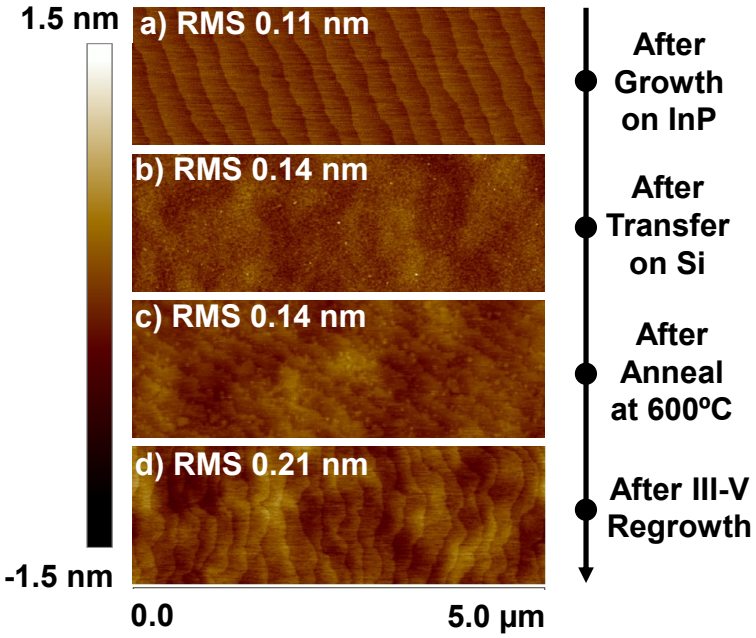



**Figure 2.7:** Atomic force microscopy (AFM) scans in tapping mode on the InGaAs surface after (a) growth on the donor wafer, (b) transfer to Si, (c) annealing at 600°C under tertiarybutylarsine (TBA) and (d) about 50 nm $In_{0.53}Ga_{0.47}As$ regrowth at 600°C.

that a 54 nm thick high quality InGaAs regrowth could be obtained, owing to the presence of sharp finite size oscillations. Furthermore, the InGaAs surface is analyzed by atomic force microscopy (AFM) after epitaxy on the donor wafer, after transfer to Si, after 600°C anneal and after regrowth (Fig. 2.7). Atomic steps are observed after $In_{0.53}Ga_{0.47}As$ growth on the InP donor wafer which get smoothened out by the selective wet etching steps during the layer transfer process. Upon annealing at 600°C, the surface reconstructs leading to the formation of atomic steps which are maintained upon $In_{0.53}Ga_{0.47}As$ regrowth.

Those observations confirm that the bonding energy is high enough to provide a thermal stability sufficient for device processing. It enables the fabrication of self-aligned InGaAs MOSFETs as presented in Chapter 4, which requires the selective growth of InGaAs on InGaAs-OI substrates at elevated temperatures.

### 2.2.3 Recycling of the donor wafer

A technologically robust DWB process is developed in the previous sections for the fabrication of InGaAs-OI substrates on Si allowing a high degree of control over the thickness, composition and roughness together with a high thermal stability for subsequent processing. This process is not economically viable since it yields the destruction of the

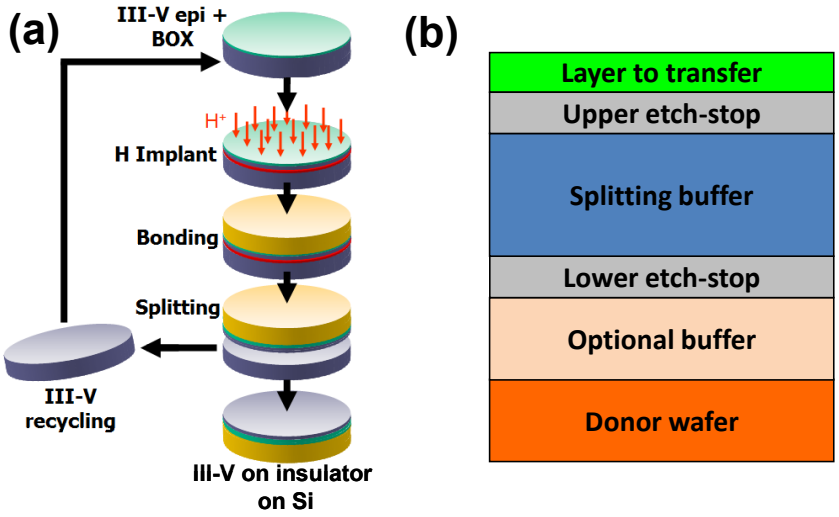



**Figure 2.8:** (a) Process flow for the fabrication of InGaAs-OI on Si substrates by DWB using hydrogen-induced thermal splitting to release the donor wafer and enable its recycling. (b) Schematic of the functional structure of the donor wafer.

donor wafer through wet chemical etching. This paragraph details the development of a hydrogen-induced thermal splitting process performed in III-V heterostructures which allows recycling the donor wafer as many times as required. It is based on the same principle as SmartCut$^{TM}$[44], but used in combination with a semiconductor heterostructure which improves the process controllability.

The method (Fig. 2.8(a)) relies on the implantation of a high dose of hydrogen in the III-V layers of the donor wafer before bonding, leading to the formation of a narrow band of extended defects. Upon annealing after bonding, hydrogen diffuses in the defects inducing an increase of their internal pressure and thus their increase in size. Owing to the presence of the bulk of the donor and target wafers acting as stiffener, the defects can only extend in-plane. They gradually start to coalesce leading to the fracture of the III-V layer at a depth corresponding to the projected range of implanted hydrogen. After splitting, the donor and target wafers can be cleaned in order to obtain a finalized InGaAs-OI substrate and a recycled donor wafer.

III-V materials offer the unique opportunity to engineer specially designed heterostructures which can assist the accurate control of the transferred layer as well as the recycling of the donor wafer if combined with the hydrogen-induced thermal splitting process. A functional donor wafer structure is proposed in Fig. 2.8(b), which enriches the SmartCut$^{TM}$concept [44]. It contains a splitting buffer into which the fracture should occur. The damaged splitting buffer post-fracture can be wet etched selectively to an upper and lower set of etch-stop layers in order to recover an atomically smooth surface. Finally,

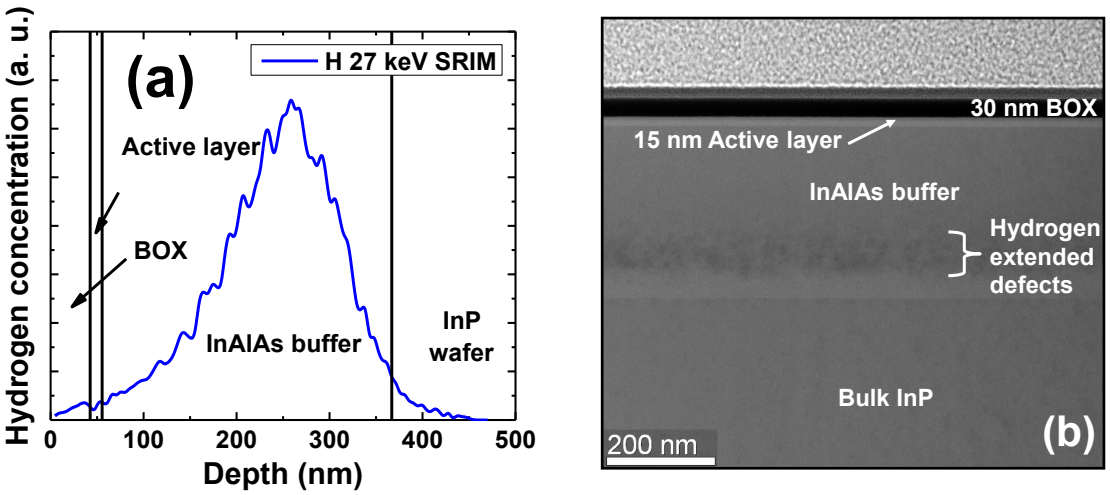



**Figure 2.9:** (a) SRIM [53] simulation of hydrogen dose implanted at 27 KeV in the III-V epi-stack. (b) Cross-sectional TEM image of the corresponding InP donor wafer with InAlAs (with 52% of indium) ($In_{0.52}Al_{0.48}As$) buffer, $In_{0.53}Ga_{0.47}As$ active layer and $Al_2O_3$ BOX layer after hydrogen implantation.

the etch-stop layers can be removed leading to the accurate transfer of the top layer to the target wafer and the recovery of a pristine surface on the donor wafer. The donor wafer can later be used for subsequent epitaxy of the initial structure, and the DWB process can be repeated. An optional buffer can be introduced between the donor wafer and the lower etch-stop layers in order to accommodate lattice mismatch in the case where the donor wafer is not lattice matched such as Si for example, as described in section 2.2.4.

Implant simulations are performed using SRIM [53] in order to estimate the implantations conditions required to locate the projected range of hydrogen in the splitting buffer. It should ensure that the band of extended defects is confined in the splitting buffer such that no damages are induced in the active layer or in the donor substrate. Figure 2.9 presents the simulation for a 27 KeV hydrogen implantation under 7°of tilt on an InP donor wafer comprising a 30 nm thick $Al_2O_3$ BOX, a 15 nm thick $In_{0.53}Ga_{0.47}As$ channel and a 300 nm thick InAlAs (with 52% of indium) ($In_{0.52}Al_{0.48}As$) splitting buffer. The corresponding transmission electron microscopy (TEM) cross-sectional view of the donor wafer post-implantation is also presented and highlights the presence of a $\approx$ 100 nm thick band of extended defects located in the InAlAs buffer. The implantation dose is varied from $5 \times 10^{15}$ cm$^{-2}$ to $6 \times 10^{16}$ cm$^{-2}$, the wafers are then annealed without being bonded to the target wafer. For samples subjected to an implantation dose of $2 \times 10^{16}$ cm$^{-2}$ and above, blistering is observed (formation of "bubbles" on the surface due to the out-of-plane expansion of the coalesced defects in absence of top stiffener). This dose is chosen

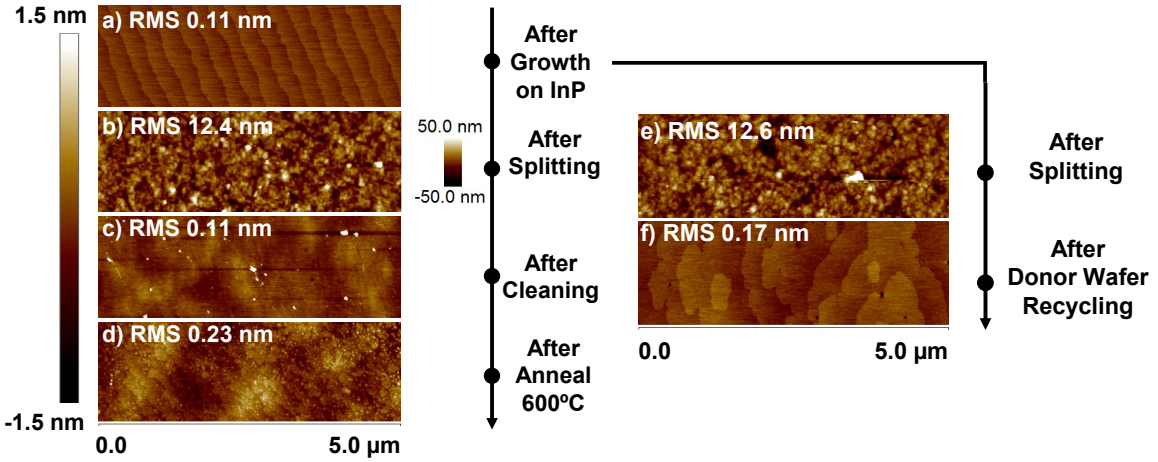



**Figure 2.10:** AFM scans in tapping mode on the surface of (a) the donor wafer after epitaxy, (b) target wafer after splitting, (c) target wafer after wet etching of the damaged splitting buffer, (d) after 600°C anneal of the transferred InGaAs-OI substrate, (e) donor wafer after splitting and (f) donor wafer after wet etching of the damaged splitting buffer and subsequent regrowth of the bonding stack.

for subsequent splitting experiments as the presence of blistering should translate in the proper splitting of the bonded wafer pair.

A H-implanted donor wafer is bonded to a target Si wafer and annealed at 300°C for 2 hours. Once unloaded from the furnace, the donor wafer is found separated from the target wafer confirming the proper splitting of the bonded wafer pair. An AFM scan of the fracture surface (Fig. 2.10(b) and (e)) on the donor and targets wafers reveal a surface roughness of about 12.5 nm root mean square (RMS) with a peak-to-peak topography of about 120 nm, in accordance with the thickness of the band of extended defects seen in the cross-sectional TEM in Fig. 2.9(b). The damaged $In_{0.52}Al_{0.48}As$ splitting buffer is wet chemically etched selectively to the target layer and the InP donor wafer with a 1:10000 and 1:100 selectivity respectively. The high selectivity to $In_{0.53}Ga_{0.47}As$ yields a very smooth, mirror-like surface (Fig. 2.10(c)) on the InGaAs-OI target wafer, while the moderate selectivity on the donor wafer induced a roughening of the InP surface (not shown). Upon annealing at 600°C under TBA in the MOVPE chamber, the InGaAs-OI surface reconstructs into atomic terraces (Fig. 2.10(d)) as in the non-splitting case (Fig. 2.7). The initial bonding stack is successfully regrown on the cleaned donor wafer leading to the formation of atomic steps on the surface (Fig. 2.10(f)) which are not as nicely ordered as in the case of a fresh InP substrate, due to the presence of an underlying roughness at the growth interface. Nevertheless, the surface roughness is small enough (0.17 nm RMS) to enable several subsequent bonding step.

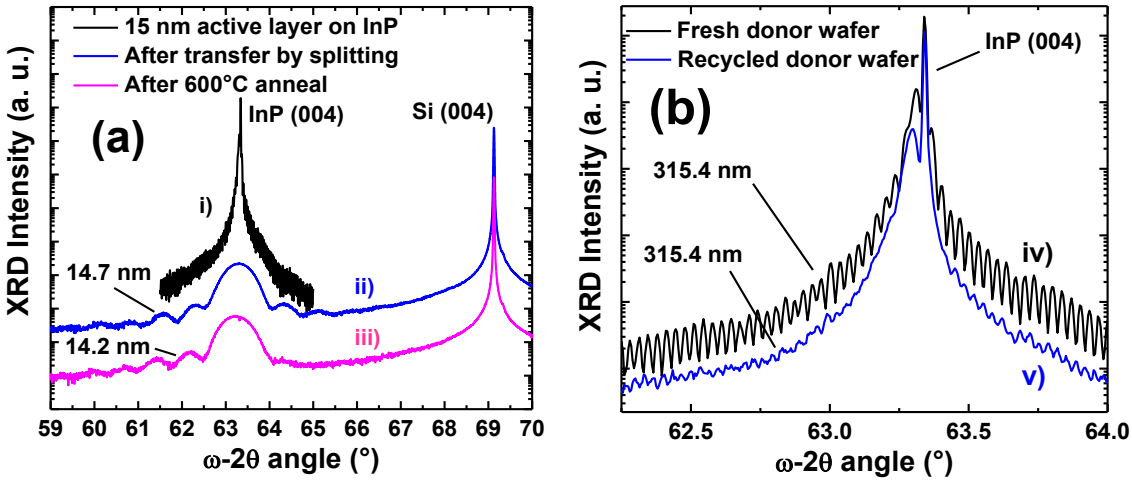



**Figure 2.11:** (a) XRD $\omega - 2\theta$ scans on the (004) reflections of (i) the donor wafer as grown, (ii) 15 nm thick transferred InGaAs-OI after splitting and wet cleaning and (iii) after annealing at 600°C in TBA. (b) XRD $\omega - 2\theta$ scans on the (004) reflections of (iv) the donor wafer as grown (same as (i)), and (v) after splitting, cleaning and regrowth of the initial epitaxy stack.

Figure 2.11 presents XRD $\omega - 2\theta$ scans acquired on the donor and target wafers after epitaxy of the bonding stack on the fresh InP donor wafer, after transfer, after 600°C anneal of the InGaAs-OI layer and after bonding stack regrowth on the recycled donor wafer. Firstly, the successful transfer of a high quality 15 nm thick $In_{0.53}Ga_{0.47}As$ layer is confirmed ; the layer remains stable upon 600°C anneal. Secondly, the regrowth of the bonding heterostructure on the recycled donor wafer yields the same composition and thickness as for the initial epitaxy on a fresh substrate. The finite size oscillations appear to be damped on the recycled wafer due to the roughening of the regrowth interface after wet cleaning of the splitting buffer with a 1:100 selectivity. In this experiment, if a lower etch-stop heterostructure would have been used as suggested in the functional schematic of a donor wafer in Fig. 2.8(b), no roughening of the InP surface would have occurred leading to a recycled donor wafer surface comparable to that of the initial donor wafer.

Splitting experiments are conducted using InP, $In_{0.53}Ga_{0.47}As$ or $In_{0.52}Al_{0.48}As$ as a splitting buffer. No significant difference is found in the implant dose required to trigger splitting, but a large difference in surface roughness after fracture is observed: 12.5 nm RMS on $In_{0.53}Ga_{0.47}As$, 14 nm RMS in $In_{0.52}Al_{0.48}As$ and 8.9 nm RMS in InP. It suggests a better confinement of extended defects in InP, thus a reduced vertical extension of the fracture which is desirable as it enables scaling down the splitting heterostructure thickness.

Those developments confirm that DWB of InGaAs could potentially be made eco-

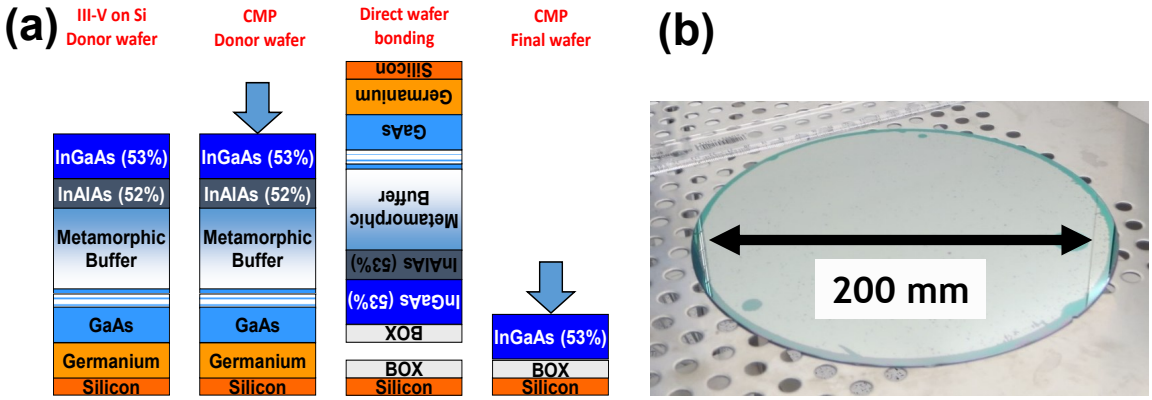



**Figure 2.12:** (a) Schematic of the SRB donor wafer structure and process flow for the fabrication of large-scale InGaAs-OI substrates from Si donor wafers. (b) Photograph of a 200 mm InGaAs-OI on Si obtained by this method.

nomically viable by recycling the donor wafer numerous times, which is one of the key milestones towards its integration in high-volume manufacturing. Nevertheless, the lack of large-scale InGaAs-OI substrates remains one of the main limiting factors for CMOS applications, a solution is proposed in the next section.

### 2.2.4 Large-scale InGaAs-on-insulator substrates

In all the previous sections, the fabrication of InGaAs-OI on Si substrates by DWB was described with an InP donor wafer. Using a III-V wafer as a donor wafer is convenient as it is lattice matched to the target layer to be transferred and thus provides an ideal material quality. Nevertheless, those wafers are very expensive and limited in size to a maximum of 4" for InP (and 8" for GaAs). The semiconductor industry currently manufactures circuits on 300 mm (12") wafers and is considering to shift to 450 mm wafers. In this context, DWB of III-V materials needs to be adapted to enable the fabrication of large-scale substrates.

The method proposed here is to replace the small InP donor wafer by a large-size Si donor wafer. The target InGaAs layer can be integrated on the Si donor substrate through the blanket growth of a strain-relaxed buffer (SRB) to accommodate the difference in lattice parameter. In this way, the 30-40 years of experience cumulated in the III-V epitaxy community to grow SRBs on Si wafers can be leveraged for the modern industrial needs of large-scale UTBB InGaAs-OI substrates fabrication.

The proposed fabrication process of the InGaAs-OI substrate by DWB is reported in Fig. 2.12. The donor wafer consists of InGaAs/InAlAs/GaAs/Ge grown by molecular

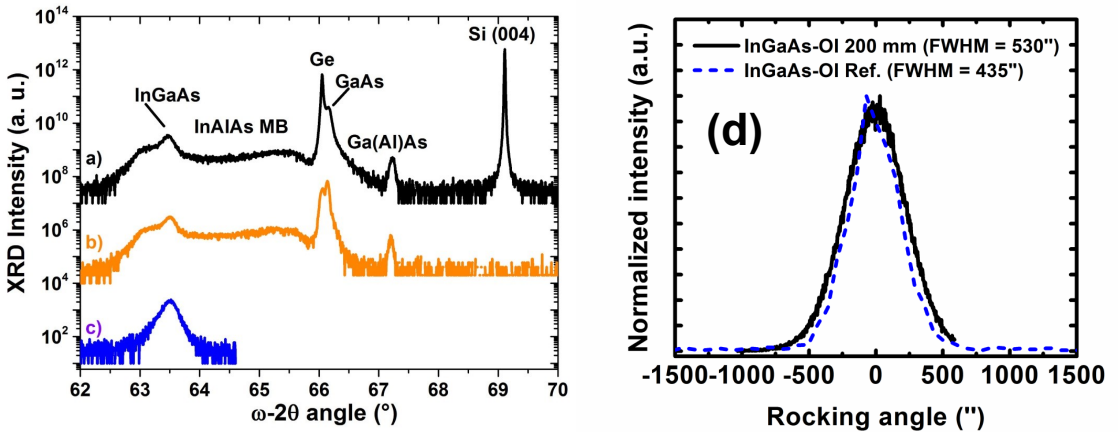



**Figure 2.13:** XRD $\omega - 2\theta$ scans aligned on the (004) reflection of the InGaAs active layer after growth on Si (a), after bonding and etching of the Si donor wafer and of the Ge layer (b) and after removal of the GaAs buffer and InAlAs grading buffer (c). XRD rocking curve ($\omega$ scans) of the (004) reflection of a finalized 200 mm InGaAs-OI substrate compared to a reference scan acquired on a InGaAs-OI layer bonded from an InP wafer.

beam epitaxy (MBE) and chemical vapor deposition (CVD) on 200 mm Si (100) substrate, with a 6°offcut towards <111> direction to favor the formation of double atomic steps, therefore suppressing the formation of antiphase domains. Firstly, a 2.5 $\mu$m thick Ge layer is directly grown on the Si substrate by CVD and submitted to cyclic anneals to improve its defect density. Secondly, a 0.5 $\mu$m Ga(Al)As and 1.5-2 $\mu$m InAlAs metamorphic buffer are grown by MBE with a graded indium-content up to 52% (lattice matched to $In_{0.53}Ga_{0.47}As$). Finally, the 500 nm thick $In_{0.53}Ga_{0.47}As$ channel is grown. Since the final roughness of the donor wafer post-epitaxy does not allow for DWB, a chemical-mechanical polishing (CMP) step is performed on the InGaAs active layer removing about 200 nm. The donor and target wafers are bonded and the donor wafer is chemically etched away although hydrogen-induced thermal splitting could also be used as described in section 2.2.3. Finally, a second CMP is done to adjust the final thickness of the InGaAs-OI layer.

Figure 2.13 presents XRD $\omega - 2\theta$ scans and rocking curve acquired at different stages of the layer transfer process. Firstly, the donor wafer is scanned (Fig. 2.13(a)) highlighting the presence of the Ge layer and GaAs layers, Ga(Al)As super-lattice satellite peak, the InAlAs graded buffer with an over-shoot in indium-content and the final $In_{0.53}Ga_{0.47}As$ active layer. The same scan is acquired after bonding and removal of the Si substrate and Ge layer (Fig. 2.13(b)). Finally, the transferred $In_{0.53}Ga_{0.47}As$ layer is shown (Fig. 2.13(c)). A rocking curve with a full width at half maximum (FWHM) of 530 arcseconds is acquired on the final 200 mm InGaAs-OI substrate which corresponds to a threading dislocation density (TDD) of only $3 \times 10^8$ cm$^{-2}$ the Ayers model [54]. This measurement is performed

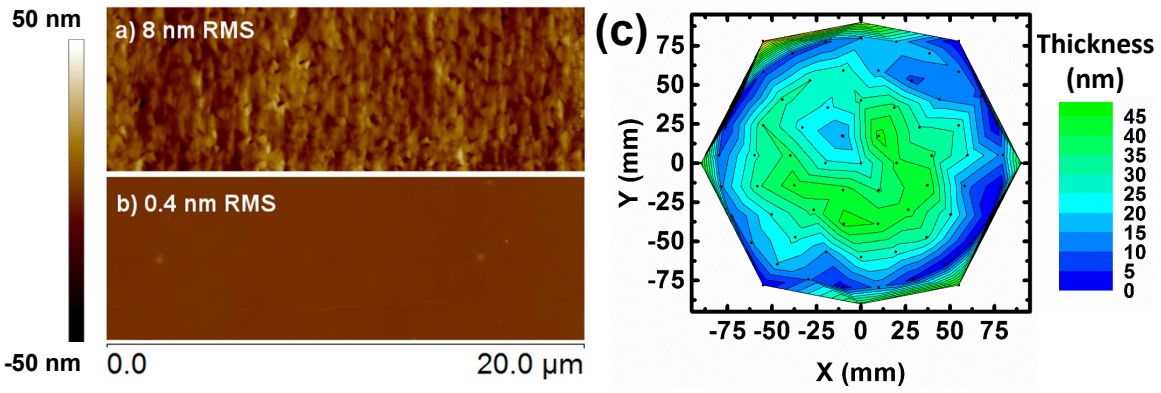



**Figure 2.14:** (a) AFM surface topography and corresponding roughness of the InGaAs-OI layer after growth and (b) after III-V CMP. (c) Spectroscopic ellipsometry thickness map on a nominally 30 nm thick 200 mm InGaAs-OI substrate.

in absence of an analyzer crystal (with a slit instead) and is therefore an overestimation of the real FWHM and thus TDD as the thickness broadening in $2\theta$ gets convoluted with the $\omega$ scan. For reference, an InGaAs-OI substrate with the same thickness (300 nm) transferred from an InP wafer is also characterized in $\omega$ scan with the slit.

Figure 2.14 presents AFM scans after donor wafer epitaxy (a) and after 200 nm of InGaAs CMP. The surface roughness is significantly reduced from 8 nm RMS down to 0.4 nm RMS thus allowing DWB. Once the layer transfer is completed, a second CMP step is performed to adjust the final InGaAs-OI thickness targeting around 30 nm. A thickness map acquired on the final 200 mm wafer is shown in Fig. 2.14(c). 80% of the surface has a thickness comprised between 25 nm and 40 nm, with non uniformities arising from the CMP process. The final 200 mm InGaAs-OI substrate has an average thickness, a thickness uniformity, crystalline quality and a surface roughness which are sufficient for the fabrication of InGaAs-based MOSFETs and CMOS circuits for research, although thickness uniformity should be improved for manufacturing.

### 2.2.5 Hybrid InGaAs/SiGe dual-channel substrates

The previous sections presented concepts and results about the development of highly-controlled large-scale InGaAs-OI on Si substrates by DWB which are thermally stable and whose donor wafer can be recycled. This section will extend the substrate work towards the co-integration of InGaAs and SiGe for CMOS applications.

The concept introduced here is to use DWB to produce hybrid dual-channel substrates which comprise blanket layers of InGaAs and of SiGe isolated from each other by an ultra-

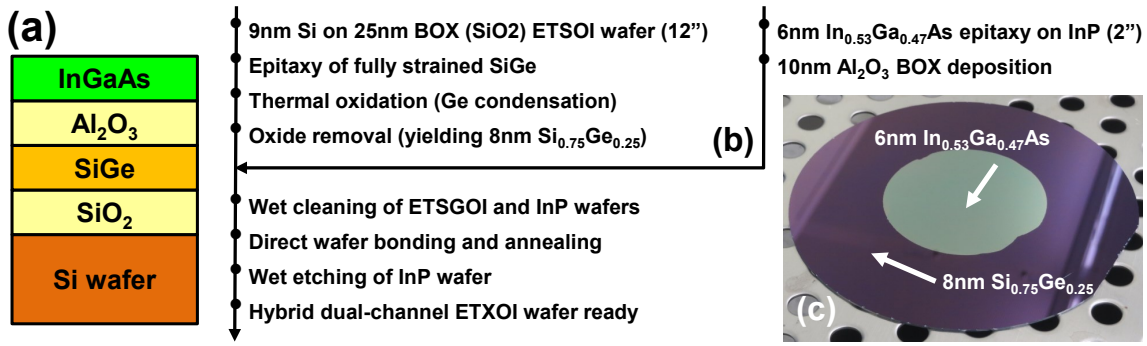



**Figure 2.15:** (a) Schematic of the targetted hybrid dual-channel InGaAs/SiGe substrate. (b) Fabrication flow and (c) photograph of a final dual-channel substrate with a 6 nm thick InGaAs channel on a 10 nm $Al_2O_3$ BOX on a 8 nm thick SiGe channel on a 25 nm $SiO_2$ BOX on Si.

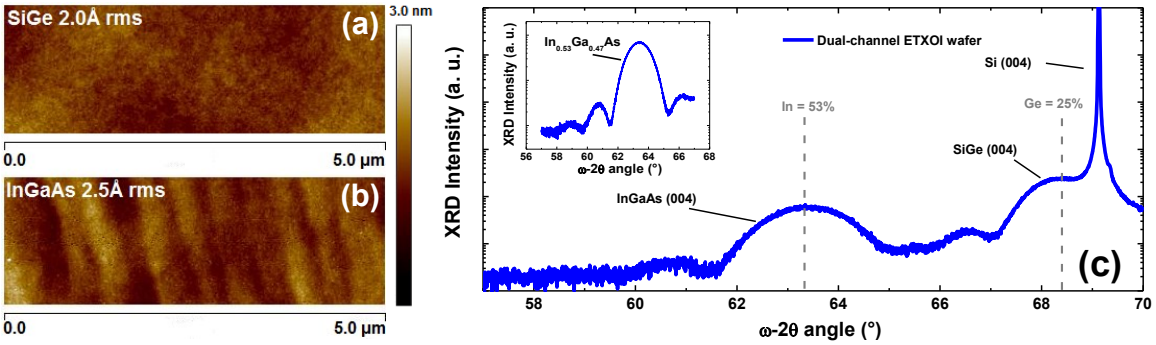



**Figure 2.16:** AFM scans on (a) the initial SiGe surface and on (b) the InGaAs layer of the hybrid dual-channel substrate. (c) XRD $\omega - 2\theta$ scan aligned on Si (004) of the dual-channel substrate comprising both InGaAs and SiGe channels. Grey dashed lines represent theoretical peak positions for InGaAs with 53% Indium and SiGe with 25% Germanium. The inset shows the InGaAs diffraction pattern on the same wafer but aligned on the InGaAs (004) reflection to resolve the finite-size oscillations.

thin BOX on a Si wafer. The fabrication starts from an industry-standard ETSOI wafer with a 9 nm thick Si channel on a 25 nm thick $SiO_2$ BOX onto which a defect-free fully-strained SiGe layer is grown. Thermal annealing and oxidation steps are then performed to form a uniform single phase of SiGe and subsequently increase the Ge content (Ge condensation as in [5]) by converting Si into $SiO_2$. The top $SiO_2$ layer is then removed leaving an 8 nm thick SiGe channel with 25% Ge. An $In_{0.53}Ga_{0.47}As$ channel layer is transferred on top of the SiGe channel using an $Al_2O_3$-$Al_2O_3$ bonding interface with a total BOX thickness of 10 nm.

As bonding occurs at full wafer scale, the InGaAs and SiGe channels are located at different z-levels. This height difference must be small enough, i.e. within depth of focus of the lithography tools (approximately 40 nm), to enable the co-planar fabrication of CMOS circuits. The proposed bonding process provides an height difference smaller than 20 nm owing to the ultra-thin $Al_2O_3$ bonding layer (10 nm). The morphology of InGaAs and SiGe is excellent with a low surface roughness (Fig. 2.16(a)), an ideal condition for wafer bonding and further device fabrication.

The XRD data collected in Fig. 2.16(b) highlight the presence of both materials on the same wafer and confirm that high structural quality of InGaAs and SiGe channels is preserved after layer transfer, owing to the high diffraction peak intensity and the presence of finite size fringes. Typical III-V integration schemes on Si relying on local epitaxy suffer from cross-diffusion problems - arsenic being an undesirable n-dopant in SiGe and Ge being also an n-dopant in InGaAs. As wafer bonding is intrinsically a low temperature process and as both materials are separated with an $Al_2O_3$ layer, a reduced cross-diffusion is expected between the InGaAs and SiGe layers. It could not be detected in further device analysis.

The InGaAs-OI and hybrid dual-channel substrates presented in this chapter are used for most of the devices of Chapter 4 and for the 2D CMOS circuit demonstrator in Chapter 5 section 5.2.1. Although it was shown that DWB could be an applicable method for large-scale integration of InGaAs on Si, its complexity and the fact that chip manufacturers will depend on certain wafer suppliers might limit the potential of this technique. In the next section, a local selective epitaxial approach is investigated as an alternative to DWB for the fabrication of InGaAs/SiGe CMOS circuits on large-scale substrates.

## 2.3 Confined Epitaxial Lateral Overgrowth

The cost-effective integration of high-quality InGaAs on large-area Si substrates is essential for developing a manufacturable CMOS technology based on high-mobility materials. Although DWB is efficient in integrating InGaAs on large area Si substrates as shown in the previous section (2.2), it may lead to higher costs for large volume manufacturing. Therefore, it could be highly beneficial to have a method of selectively growing InGaAs layers on standard Si wafers only where it is required, as long as the material quality and the processing complexity match the requirements of modern CMOS manufacturing:

- Compatible with standard (100) bulk Si substrate,
- Cost-efficient process inherently available on large wafer sizes (300 mm and above),
- Exploit standard available CMOS process modules,
- Tight lateral integration with SiGe and Si channels,
- Provide 30 nm to 50 nm tall and 5 nm to 8 nm wide fins with a pitch of 25 nm to 30 nm.

All the integration techniques available today fail in fulfilling at least one of those requirements. Blanket layer techniques such as SRB or DWB enable the fabrication of small fins at tight pitch using industry-standard patterning techniques but SRB typically uses 6°off-cut Si wafers and does not allow tight integration with SiGe, while DWB on large-scale wafers is probably the most expensive technique. Methods relying on selective epitaxy on Si have in common the inherent availability on large wafer sizes and are generally cost-efficient. The ART method or replacement-fin technique [8] is using standard CMOS process modules on (100) standard bulk Si wafers and is anticipated to enable the tight integration with SiGe fins. The main pitfall is its availability to provide fin width as small as 5 nm to 8 nm since it appears to be extremely challenging to scale the trench width below 20 nm [55]. Similar concerns exist for NWs [19] as it is not possible to scale their diameters down to the strict requirements of CMOS applications. Even the growth of NWs in constrained structures [56] faces the same limitations as the ART technique. The ELO method is generally not applicable to CMOS processing as it fails to provide micron-sized III-V areas with a controllable thickness in relation to the targeted fin height (50 nm or less) [9, 18]. The rapid melt growth (RMG) technique is in that sense attractive as it can provide micron-sized III-V areas with a well-controlled thickness [57, 58] but it

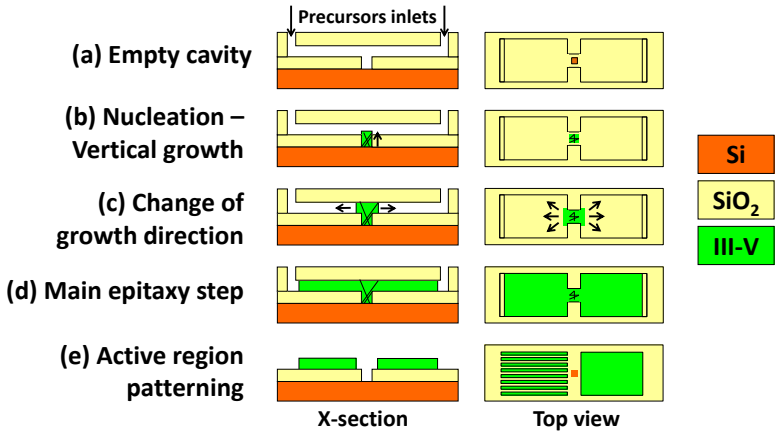



**Figure 2.17:** Schematic of the confined epitaxial lateral overgrowth (CELO) integration scheme. (a) An empty $SiO_2$ cavity on Si is formed which defines the final shape and thickness of the III-V layer. (b) III-V epitaxy starts vertically from the Si seed and (c) continues laterally towards the cavity openings. (d) Once the cavity is filled, (e) $SiO_2$ top layer is removed and the III-V layer is patterned into final n-MOSFET active regions.

is not applicable to ternary materials such as InGaAs since InAs and GaAs segregation occurs during the recrystallization owing to their different melting temperatures.

In this section, an original integration scheme will be presented, which fulfills all the above mentioned requirements for CMOS applications and uses most of the defect filtering mechanisms from the previously mentioned integration techniques. It is inspired from selective epitaxy techniques developed to realize SOI films such as the tunnel epitaxy technique [59, 60], patterned constrained epitaxy [61] or confined lateral selective epitaxial growth [62]. Firstly, the concept will be presented (section 2.3.1) followed by a detailed description of the integration scheme (section 2.3.2) and finally by characterizations of the obtained InGaAs and InP on Si layers (section 2.3.3). Devices fabricated on this material are presented in Chapter 4 section 4.3.3 and Chapter 5 section 5.2.2.

### 2.3.1 Concept

The underlying idea is to provide a method which relies on selective epitaxy on regular (100) Si wafers, utilizes standard CMOS process modules and yields micron-sized InGaAs layers of well-controlled thickness into which small fins can be patterned at tight pitch using conventional techniques.

As proposed in [16], a complete filtering of threading defects can be obtained by epitaxial growth of lattice mismatched crystals from a small seed in an oxide hole as long as the seed is small enough compared to the hole depth. The crystal size can then be

expanded and remains free of defects provided that it does not merge with another crystal. It is the selective epitaxy analogy of the bulk Czochralski crystal growth where the seed crystal is kept to a small diameter for some growth length before the large boule is pulled [63].

The purpose of the integration concept presented here is to leverage the same mechanism for the filtering of crystalline defects while controlling how the crystal is expanded in a different manner. For III-V growth on Si, a small seed also helps mitigating chances to nucleate anti-phase domain boundaries. Unlike for the ELO case where the expansion of the crystal is tuned by the growth conditions, here it is shaped by growing into predetermined confinement structures or empty cavities. It is therefore similar to the ELO method but occurring in a confinement structure, hence the proposed name of the integration scheme: confined epitaxial lateral overgrowth (CELO) [32]. In parallel, co-workers from IBM Research developed a similar approach to grow lateral NWs in empty cavities on SOI substrates [64]. All these epitaxy techniques in empty cavities can be classified as template-assisted selective epitaxy.

The overall integration concept is presented in Fig. 2.17. An empty $SiO_2$ cavity (or confinement structure) is defined on a Si substrate. This empty cavity needs to fulfill three requirements:

- It should contain a single access to the Si substrate which will act as a small seed for the nucleation of the III-V crystal.
- At least one opening should be made in the oxide to act as a gas inlet enabling the gas precursors to enter the cavity and initiate the III-V crystal growth.
- The 3D shape of the cavity should be tailored to the desired application as it defines the final shape of the grown III-V crystal including its thickness and surface roughness.

A III-V crystal growth is initiated in an MOVPE reactor which should nucleate on a Si surface and be very selective to $SiO_2$. Under such conditions, the crystal growth will start from the small Si seed in the cavity and develop vertically. No nucleation should occur inside the cavity on the $SiO_2$ surface otherwise the non-selective crystals of uncontrolled crystal orientation will block the cavity and prevent the Si seeded crystal from expanding. After a certain growth time, the III-V crystal will reach the upper surface of the cavity and cannot develop any further in the vertical direction, unlike for the ELO case. The growth will therefore continue only in the lateral direction until the III-V crystal reaches the cavity openings, then, the III-V crystal will exit the cavity and develop as for usual

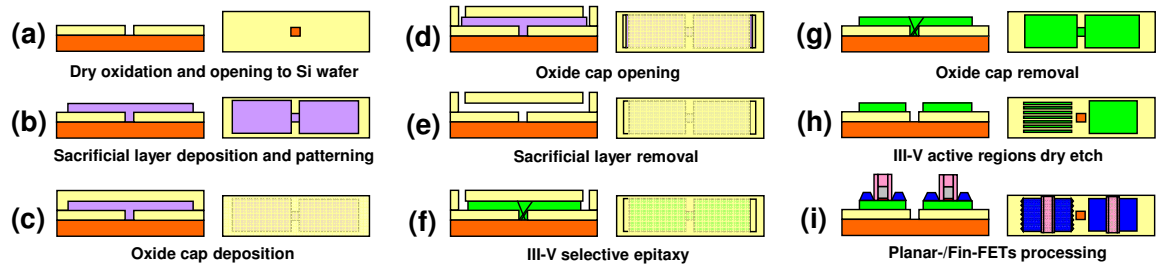



**Figure 2.18:** Process flow for the fabrication of empty $SiO_2$ cavities on Si fulfilling the requirements of the CELO integration scheme.

ELO. This excess of III-V crystal growing out of the cavity could be polished back, or simply the growth could be interrupted before the III-V crystal reaches the openings. Subsequently, the upper oxide can be removed to expose the grown III-V crystal which can be patterned using conventional techniques into narrow fins with a tight pitch for instance. In particular, the seed region which connects the laterally overgrown III-V to the Si substrate and contains most of the crystalline defects is removed. In this way, the remaining III-V crystal is electrically disconnected from the Si substrate as for usual InGaAs-OI layers. It will be demonstrated that:

- Fully-relaxed InGaAs and/or InP can be integrated on standard (100) Si in micron-sized areas with a minimal area penalty: strain relaxation and defect filtering occurs in the vertical direction while the lateral direction is used for active devices.
- There is no intrinsic limit on how close InGaAs and SiGe can be integrated besides lithography alignment accuracy.
- The fabrication process is extremely robust, uses only standard CMOS processes and gives a very high level of control over all dimensions and surface roughness.
- In contrary to ART, this method does not present any scaling limit associated with the cavity width for the 5 nm CMOS node and beyond. Indeed, the growth direction is normal to the fin *height* which is targeted between 30 nm and 50 nm, while ART exploits the growth direction normal to the fin *width* with targeted dimensions between 5 nm and 8 nm.

### 2.3.2 Fabrication of empty cavities on Si refilled by III-V crystals

The detailed fabrication process is presented in Fig. 2.18. It starts from a standard (100) Si substrate of any size. A thermal $SiO_2$ is grown with a certain thickness which will

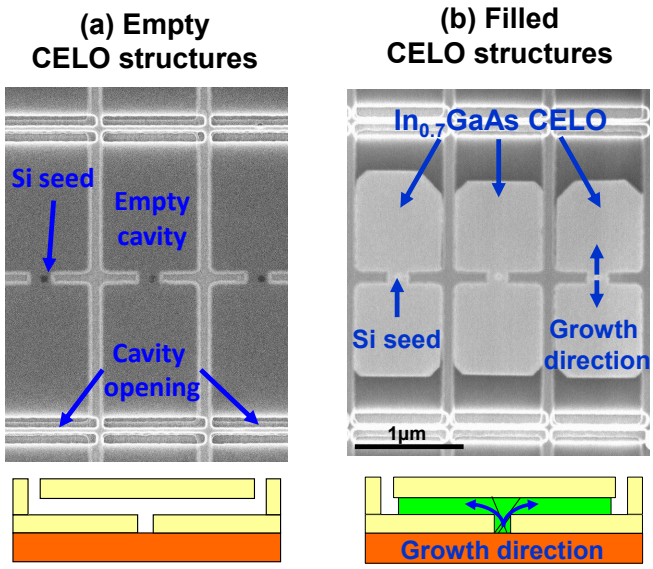



**Figure 2.19:** Top view scanning electron microscopy (SEM) image and associated schematic of CELO structures (a) before and (b) after InGaAs (with 70% of indium) ($In_{0.7}Ga_{0.3}As$) selective epitaxy by MOVPE.

later act as the BOX. Small openings are dry etched in the $SiO_2$ layer down to the Si substrate which will later act as crystalline seeds (Fig. 2.18(a)). A sacrificial material is deposited on the wafer and patterned by dry etching into a defined 2D shape which overlaps with at least one Si seed (Fig. 2.18(b)). Many properties of this patterned sacrificial material will define the final properties of the grown III-V crystal: 2D shape, thickness, thickness uniformity, surface roughness. Its deposition process should therefore be carefully optimized. Subsequently, the wafer is covered with a $SiO_2$ layer which will serve as the future suspended capping layer of the empty cavities (Fig. 2.18(c)). This capping oxide is dry etched down to the sacrificial material to form openings at the periphery of the future empty cavities (Fig. 2.18(d)). The sacrificial material is then completely removed selectively to $SiO_2$ and to the Si substrate resulting in empty cavities (Fig. 2.18(e)). The Si surface is wet cleaned in order to recover a pristine surface and optionally submitted to an anisotropic wet etch resulting in atomically smooth (111) facets. The wafer is loaded in the MOVPE reactor and an InGaAs or InP crystal is grown (Fig. 2.18(f)). The $SiO_2$ capping layer can be removed by dry or wet etching (Fig. 2.18(g)) and the defective seed region of the grown III-V crystal can be etched away (Fig. 2.18(h)). The resulting micron-sized III-V crystal can then act as a virtual substrate for subsequent growth of III-V heterostructures (for lasers or analog/high-frequency devices) or can be etched into small fins for CMOS applications (Fig. 2.18(i)).

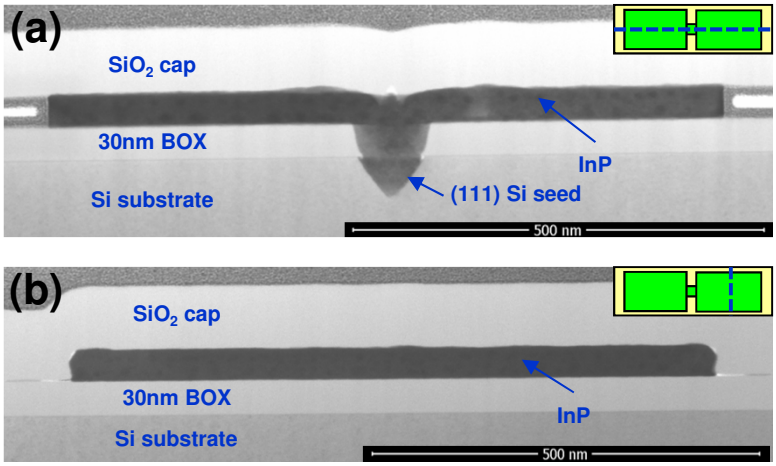



**Figure 2.20:** Cross-sectional TEM (a) along and (b) across the growth direction on 30 nm thick InP grown from a (111) Si seed on a 30 nm thick $SiO_2$ BOX. The inset cartoon presents the cutting direction as a blue dashed line.

Figure 2.19 presents top view SEM images of an array of empty $SiO_2$ cavities obtained by this fabrication process before and after epitaxy of $In_{0.7}Ga_{0.3}As$. The $In_{0.7}Ga_{0.3}As$ growth is stopped before the crystal reaches the cavity openings. One can clearly notice the presence of the small Si seed (about 40 nm in diameter), the suspended oxide which appears in dark-grey and the cavity openings at the top and the bottom. After $In_{0.7}Ga_{0.3}As$ growth, it becomes evident that the epitaxy started from the center of the cavity where the Si seed is located, and developed upwards and downwards in the direction of the cavity openings. The presence of well defined (100) and (110) facets at the boundaries of the grown crystals attests to the fact that those crystals are single crystalline with the same orientation as the Si substrate.

### 2.3.3 Material characterization

Empty cavities are prepared on a (100) Si substrate, having a height of 30 nm, a width of 800 nm and a length of 1.3 $\mu$m on each side of the seed (same geometry as in Fig. 2.19). The Si seed is 50 nm wide and is treated to have (111) facets. In order to study the defect filtering mechanism, InP is grown as its binary nature defines a fixed lattice constant and removes the uncertainty of composition variation that can be present in ternary materials such as InGaAs.

TEM sample preparation is carried out with a focused ion beam (FIB) along and across the growth direction, presented in Fig. 2.20. It should be noted that due to the very different sputter rate of In and P atoms under the Ga beam, TEM lamella preparation

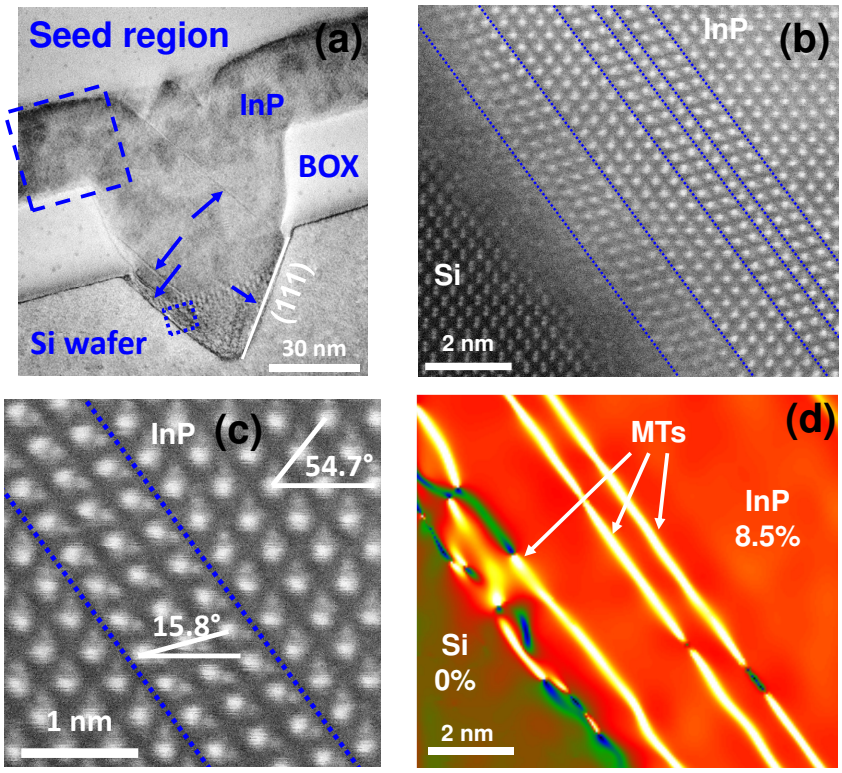



**Figure 2.21:** (a) High-resolution TEM image on the seed region of the sample shown in Fig. 2.20(a). Blue arrows indicates the position of planar defects. (b) High-resolution scanning TEM (STEM) image of the Si/InP interface corresponding to the small blue dashed square in (a). (c) Highly magnified STEM image of a MT. (d) Lattice mismatch map obtained by geometrical phase analysis (GPA) in the vincinity of the Si/InP interface.

containing InP usually gives rise to the formation of In droplets on the InP surface. This can be observed as a slightly darker local contrast scattered on the InP layer in Fig. 2.20(a). It is apparent that the growth started from the (111) Si facets, filled the seed region and started to expand in-plane for about 300 nm on each side. The growth front appears to be a (110) facet which helps preventing the formation of microtwins (MTs) (whose formation is favored with (111) facets). The view across the growth direction (Fig. 2.20(b)) confirms the proper lateral filling of the cavity to the nominal width of 800 nm.

Figure 2.21 presents a set of high-resolution TEM and STEM images on the seed region. First looking at the TEM view (Fig. 2.21(a)), a uniform Moiré fringes network can be observed at the bottom of the V-groove. It is arising from the interference between the electron beams diffracted by overlapping InP and Si, each having a fixed and different lattice constant. It seems to indicate a uniform relaxation of the InP layer at the earliest stage of growth. The high-resolution STEM image of the Si/InP interface (Fig. 2.21(b)) reveals the presence of a high density of planar defects on (111) planes parallel to the

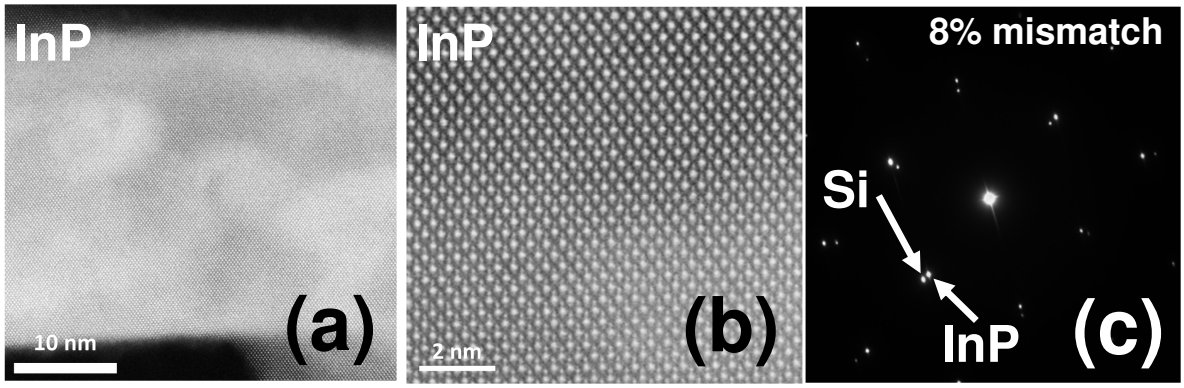



**Figure 2.22:** High-resolution STEM images (a) on the region corresponding to the onset of lateral growth (large blue dashed square in Fig. 2.21(a)) and (b) magnified view of the crystal structure. (c) Electron diffraction pattern acquired with a 50 nm apperture on a region away from the seed containing an InP/BOX/Si stack.

growth interface through which the InP crystal efficiently relaxes its strain in the first 5 nm of growth. A high-magnification STEM image on one of those planar defects (Fig. 2.21(c)) clearly confirms their MT nature: a section of InP crystal having its (111) planes rotated by 15.8° with respect to the (100) planes of the bulk is inserted through the formation of two stacking faults (SFs). In contrast, regular (111) planes are typically inclined by 54.7° with respect to the (100) planes. A lattice mismatch mapping is performed by geometrical phase analysis (GPA) (Fig. 2.21(d)). It confirms that the InP crystal gets fully relaxed to its nominal lattice constant within 2-3 nm from the interface. Similar observations on the strain relaxation of Si/InP interface were reported with the ART technique in [17]. This efficient strain relaxation process seems to be an intrinsic feature of the (111) InP/Si interface and is probably explained by the fact that it has the lowest stacking fault formation energy of all III-V semiconductors [65].

A few planar defects are escaping from the interfacial region, propagate through the grown InP layer and are terminated at the InP/$SiO_2$ interface with the BOX or with the upper capping layer (Fig. 2.21(a)). From the onset of lateral growth over the BOX (Fig. 2.22(a)) and up to the termination of the crystal towards the cavity opening, an ideal crystalline structure is observed (Fig. 2.21(b)). The electron diffraction pattern shown in Fig. 2.21(c) measures a lattice mismatch of 8% between Si and InP which confirms the full relaxation of the InP crystal.

For applications into high-mobility n-MOSFETs on Si, the integration of InGaAs is more relevant. InGaAs growth is carried out into similar empty cavities with a thinner BOX of 25 nm. This time, the growth is continued until the InGaAs crystal reaches the cavity openings in order to provide large areas for further device processing. A 30 nm

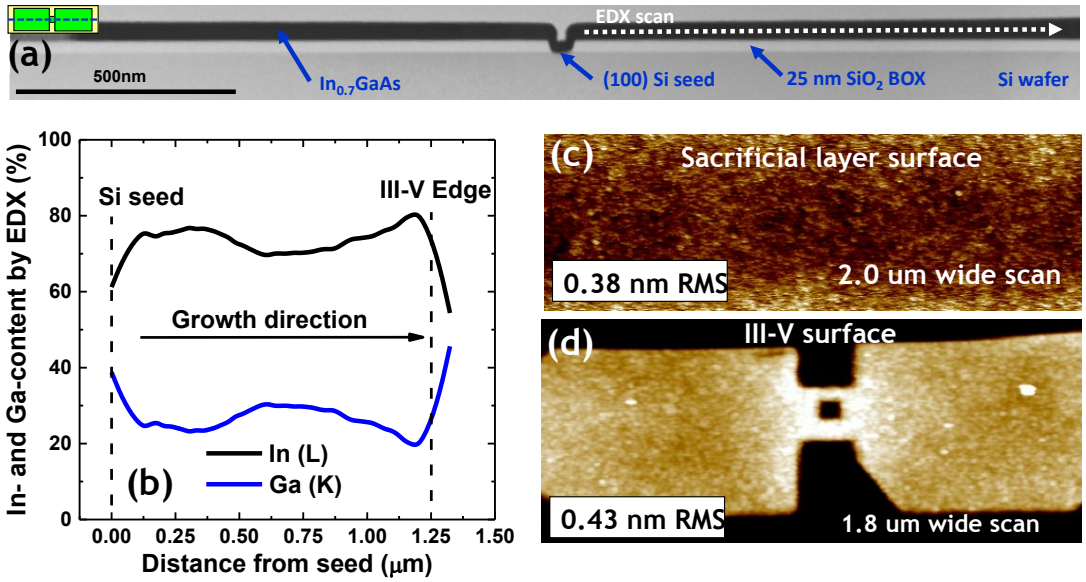



**Figure 2.23:** (a) STEM overview on a 30 nm thick and 2.5 $\mu$m long $In_{0.7}Ga_{0.3}As$ crystal grown from a (100) Si seed. (b) In- and Ga-content measured from energy dispersive X-ray spectroscopy (EDX) line scan on the L$\alpha$ line of In and K$\alpha$ line of Ga (white dashed scan line shown in (a)). (c) AFM scan on the surface of the sacrificial material as deposited and (d) on the InGaAs surface after growth and oxide cap removal.

thick and 2×1.25$\mu$m long $In_{0.7}Ga_{0.3}As$ layer is obtained (Fig. 2.23(a)). A composition analysis is performed by EDX line profiling in the TEM (Fig. 2.23(b)). The steep change of composition in the first and last 0.15$\mu$m are most likely measurements artifacts due to edge termination. In the core section of the InGaAs layer, the extracted composition varies from 70% to 75% of indium. No optimization is performed to minimize composition variation along the length of the crystal, but it is clear that it represents one of the main challenges of the technique. From a material stand-point, indium-content variation generates fluctuations of the lattice parameter and might lead to undesirable plastic relaxation in the channel region while from the technology stand-point, it induces mobility fluctuations and $V_T$ shift which are not desirable for CMOS applications.

Post-epitaxy, the capping oxide is removed exposing the InGaAs surface. AFM surface analysis reveals that the final InGaAs roughness clearly reproduces the initial surface granularity of sacrificial material (Fig. 2.23(c) and (d)). The final InGaAs as-grown surface roughness is 0.43 nm RMS which is good enough for a direct fabrication of n-MOSFETs without further surface treatments. Nevertheless, future work could focus on improving the sacrificial material deposition process in order to reach a final surface roughness below 0.25 nm RMS as can be obtained from bonded layers (Fig. 2.7).

## 2.4 Conclusion and outlook

DWB is used to fabricate UTBB InGaAs-OI on Si substrates. The optimized layer transfer process results in the successful demonstration of strained or unstrained InGaAs layers with a thickness as low as 5 nm. A high bonding energy above 1.5 J/m$^2$ is achieved with an $Al_2O_3$ bi-layer BOX as thin as 10 nm which enables high temperature InGaAs regrowth on the InGaAs-OI virtual substrate. A path towards the cost-efficient large-scale manufacturing of InGaAs-OI substrates is shown. A specially designed III-V heterostructure combined with hydrogen-induced thermal splitting enables recycling the donor wafer without compromising on thickness control and surface roughness. The fabrication of 200 mm InGaAs-OI substrates is demonstrated by using InGaAs integrated on large-scale Si substrates via a thick graded buffer as donor wafers. Those wafers present a TDD of $3\times10^8$cm$^{-2}$ extracted by XRD, among the best reported ones for InGaAs on Si. Finally, hybrid dual-channel substrates are fabricated to enable CMOS integration of InGaAs and SiGe on the same platform.

The CELO concept is proposed to locally integrate InGaAs on Si by selective epitaxy in empty oxide cavities. A robust fabrication process is developed fulfilling all requirements for large-scale CMOS manufacturing. The concept is validated through the demonstration of micron-sized islands of InP and InGaAs on Si. An efficient complete relaxation of strain is observed in the first few nanometers of growth with the formation of a dense MT network in the seed region. As-grown InGaAs layers present a low surface roughness of 0.43 nm RMS and a composition uniformity of 5%-In over 1 $\mu$m of lateral growth. Future studies should focus on extracting an accurate defect density from InP or InGaAs material integrated on Si by this technique, and optimizing the growth conditions accordingly.

InGaAs-OI layers obtained by DWB and CELO developed in this chapter are used in subsequent chapters for demonstrating devices and circuits on Si.

# Chapter 3

# Process Modules: Gate Stack and S/D Regions

## 3.1 Introduction

In this chapter, key modules for the realization of CMOS-compatible self-aligned InGaAs MOSFETs are developed. Among all numerous process modules required for the complete fabrication of transistors, the formation of the MOS stack and of S/D contacts is emphasized.

A MOS stack based on high-k metal-gate (HKMG) layers with a low $D_{it}$ and a scaled capacitance-equivalent thickness (CET) is required in order to obtain high-performance, low-power transistors with a steep SS approaching 60 mV/dec and a high mobility (section 3.2). Firstly, an amorphous silicon (a-Si) interlayer is proposed to be inserted between the high-k (HK) layer and the channel as a possible path to decrease $D_{it}$, CET and increase the thermal stability of the stack. Secondly, the use of remote oxygen scavenging is studied as a way to further scale down the CET and $D_{it}$. The influence of remote oxygen scavenging is investigated on gate stacks containing a-Si but also on stacks having a direct HK/InGaAs interface formed by thermal ALD. Finally, an optimized gate stack formed by plasma-enhanced ALD (PEALD) is shown, leveraging all the knowhow gradually acquired in the previous developments.

For the self-aligned formation of S/D regions (section 3.3), the use of highly-doped InGaAs raised S/D (RSD) is proposed. Various dopant species are investigated to reach a high doping concentration, preferably at low growth temperature (to preserve a low $D_{it}$ in GF integration schemes). Self-aligned Ni-alloyed contacts to InGaAs are developed, based on the concept of "salicides" (self-aligned silicides) for Si MOSFETs. The formation

of nickel-indium-galium-arsenide (Ni-InGaAs) alloy is studied and the resulting electrical properties are characterized. The alloying process is tuned to enable its integration on MOSFETs. Finally, direct metal contacts to highly-doped InGaAs RSD are investigated and benchmarked against Ni-InGaAs contacts.

The remaining modules of the InGaAs n-MOSFETs fabrication process are also developed. A substantial part of the work corresponds to the optimization of dry etching process for high-resolution etching of InGaAs fins, wet etching to recover a pristine InGaAs surface, dry etching of the gate and HKMG stack, deposition and dry etching of ultra-thin spacers. Those modules are not detailed in this thesis as some are developed in collaboration with team members, or, are developed on my own but do not present enough scientific interest or cannot be disclosed yet.

## 3.2 MOS Gate stack

The realization of a high-quality MOS interface on III-V semiconductors represents one of the main challenges to achieve good electrostatic gate control over the channel and the appropriate reliability. Unlike the case of Si interface, III-V semiconductors do not have a high-quality interface with their native oxide. In the case of InGaAs, the nature of the MOS interface is extremely complex as the three constituents of the channel material can present several oxidation states ($Ga_2O$, $Ga_2O_3$, $As_2O_3$, $As_2O_5$, $In_2O_3$, ...) and can have unsatisfied dangling bonds and metallic bonds (In-In, Ga-Ga, As-As). Those bonds can create a high $D_{it}$ with energy levels lying in the valence band, in the bandgap or in the conduction band [66, 67]. Interface traps located in the bandgap might pin the Fermi-level thus preventing the gate from changing the band bending from off-state to on-state of the transistor. They are mainly responsible for the degradation of the MOSFET sub-threshold swing (SS) and interact with the channel charge through a thermally-activated Shockley-Read-Hall (SRH) process [68]. Traps located in the conduction band interact with the channel charge in its on-state and might limit the maximum available mobile carrier density by pinning the Fermi level, thus limiting the maximum on-current [69]. In addition, traps might exist in the HK layer itself located in the near-interfacial region. They are often referred to as border traps and are usually reported to lie near the valence and conduction band edges [70, 71]. They are associated with a time constant which depends on their distance relative to the interface as they are accessed through tunneling [72, 73]. They are responsible for flicker noise and hysteresis in capacitance-voltage (C-V) or current-voltage (I-V) measurements which implies a higher $V_T$ variability and worser reliability. Finally, fixed charges might be present in the MOS stack [74]. They induce a rigid shift of the $V_T$ and might degrade mobility through remote Coulomb scattering.

The distribution in space and energy of interface states, border traps and fixed charges in an InGaAs MOS system is summarized in a band diagram shown in Fig. 3.1(a). Correspondingly, the effect of interface states, border traps or fixed charges on multi-frequency C-V characteristics of a metal-oxide-semiconductor capacitor (MOSCAP) are shown in Fig. 3.1(b, c, d). Firstly, interface states located in the bandgap can respond at low measurement frequencies giving rise to a "hump" in the transition region from depletion to accumulation (Fig. 3.1(b)). Furthermore, all interface states getting charged under the sweeping gate bias (even the ones not responding at the measurement frequency) are gradually shifting the flat-band voltage ($V_{fb}$) which leads to a "stretch-out" of the C-V characteristics at all frequencies: it appears as a shift from the ideal C-V curve which increases with gate voltage (as indicated by the three horizontal arrows of increasing

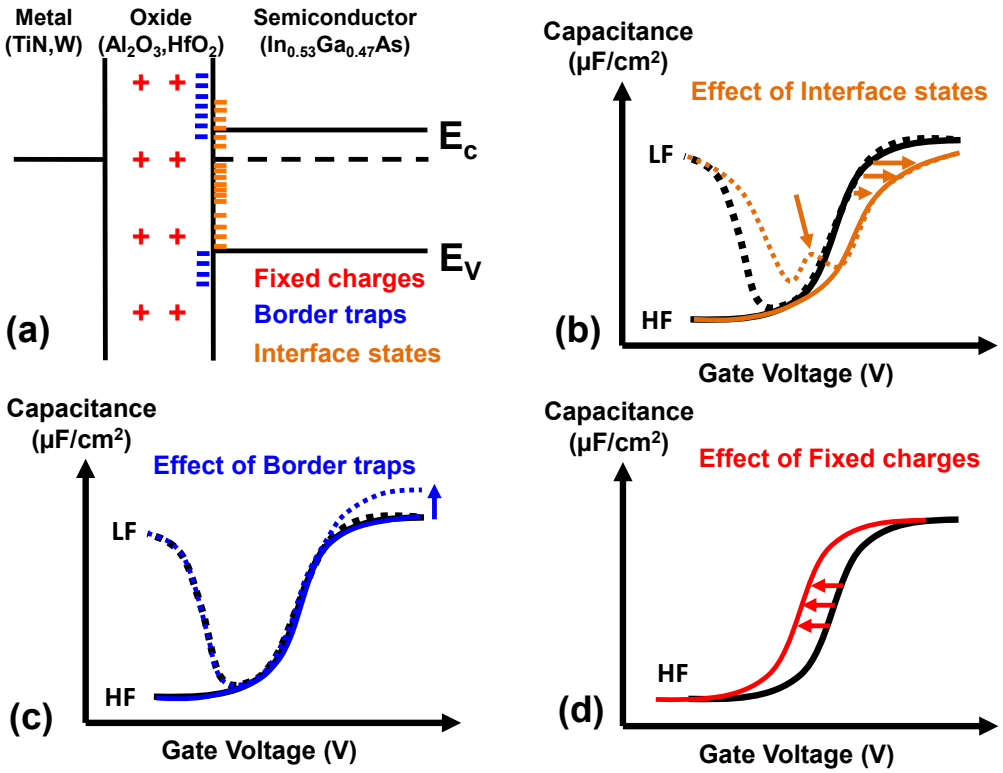



**Figure 3.1:** (a) Energy band diagram of an InGaAs MOS stack summarizing the presence of interface states, border traps and fixed charges. (b, c, d) C-V characteristics at high (HF, full lines) and low (LF, dashed lines) frequencies for an ideal MOS interface (black curves), compared with an MOS stack containing (b) interface states, (c) border traps and (d) fixed charges.

lengths in Fig. 3.1(b)). Secondly, border traps are mostly charged in accumulation as the increased electric field and band bending favors tunneling. It translates into a frequency dispersion in accumulation (Fig. 3.1(c)) induced by the portion of border traps whose time-constants are within the measurement frequency range. Finally, fixed charges give rise to a $V_{fb}$ modification which appears as a rigid shift of the C-V characteristics as indicated by the red arrows of equal lengths in Fig. 3.1(d).

The development of short-channel InGaAs MOSFETs imposes some requirements on the MOS gate stack, which are defined to match what is expected from Si transistors:

- The oxide thickness has to be scaled down to less than 15 Å CET.
- The $D_{it}$ in the upper part of the bandgap needs to be reduced below $3\times10^{12}$ $eV^{-1}cm^{-2}$ in order to achieve SS below 70 mV/dec with the above mentioned CET.
- The thermal stability of the gate stack has to be higher than 400°C for compatibility with the BEOL process, and preferably up to 600°C for GF processing.

- Fixed charges need to be minimized to reach a positive $V_T$ on transistors
- Hysteresis at least below 10 mV has to be achieved at 0.5 V operating voltage for CMOS circuit operation (although it might mostly give rise to reliability concerns).

MOSCAPs represent the main test vehicle for the development and characterization of MOS interfaces. Their fabrication is simple and minimizes processing steps that might degrade the MOS interface and enables a fast turn-around. As mentioned in the introduction of this chapter, several options are considered and reported in the following sections. Firstly, a stack based on the introduction of an a-Si layer between the HK and InGaAs is proposed as a potential solution for high thermal stability (section 3.2.1). Secondly, the impact of gate metal on MOSCAP properties is studied in the context of a-Si-based stacks as well as gate stacks having a direct HK/InGaAs interface (section 3.2.2). Finally, an optimized plasma-based ALD HKMG stack will be presented (section 3.2.3) as it will be also used for devices in Chapter 4.

### 3.2.1 a-Si based gate stack

The high $D_{it}$ at the HK/InGaAs interface is often primarily related to the presence of InGaAs oxides or sub-oxides. The direct deposition of the HK layer on a clean InGaAs surface free of oxygen necessarily leads to the formation of some InGaAs oxides at the interface. Even if this oxide formation can be largely limited to sub-monolayers, it is always present and might induce an increase of the $D_{it}$ and CET. Furthermore, an InGaAs MOS stack with a direct HK/InGaAs interface subjected to a high thermal budget (above 500°C) usually experiences an increase of the amount of InGaAs oxides, thus an increase of $D_{it}$ and CET (see section 3.2.2.2).

The starting idea of the proposed a-Si stack is to introduce an offset material between InGaAs and the HK layer which does not contain oxygen in order to prevent oxidation of the InGaAs surface during deposition and at high temperature [75]. The choice of a-Si is motivated by the fact that it presents a stable interface with $Al_2O_3$ or hafnium-oxide ($HfO_2$), it is a good oxygen diffusion barrier, and it does not diffuse in InGaAs at typical III-V processing temperatures.

#### 3.2.1.1 Deposition process

$HfO_2/Al_2O_3$/a-Si/InGaAs MOSCAPs are fabricated on 200 nm thick p-type $In_{0.53}Ga_{0.47}As$ epilayers grown by MOVPE on InP (100) substrates with a bulk doping of $5 \times 10^{17}$ cm$^{-3}$. $HfO_2$ is selected as the main HK layer for its high dielectric constant ($k = 16 - 20$) and

because it is the industry-standard HK material. A thin layer of $Al_2O_3$ is inserted between a-Si and $HfO_2$ as it was shown to suppress the formation of a lower-k hafnium-silicate [34].

After a 1 min dip in 5% hydrofluoric acid (HF) solution, the InGaAs epilayer is loaded in an ultra-high vacuum (UHV) molecular beam deposition (MBD) chamber and exposed for 30 min to a remote hydrogen-plasma at 250°C to remove residual oxygen and carbon from the surface [76]. A 1 nm thick hydrogenated a-Si is then deposited *in-situ* by e-beam evaporation under remote hydrogen plasma at room temperature. It is followed by *in-situ* deposition of 1 nm $Al_2O_3$ and 2 nm of $HfO_2$ at 250°C by e-beam evaporation of single crystal $Al_2O_3$ without additional oxygen and metal Hf under $2 \times 10^{-5}$ Torr of molecular oxygen, respectively.

MOS capacitors are fabricated using 200 nm of sputtered W as a gate metal and patterned using photolithography and dry etching. The samples are then annealed at temperatures around 550°C in a rapid thermal annealer under nitrogen for 30 min.

#### 3.2.1.2 Chemical analysis

The MBD chamber is connected through a robot in UHV to an *in-situ* X-ray photoemission spectroscopy (XPS) analysis chamber with a base pressure of $2 \times 10^{-9}$ Torr. The analysis chamber is equipped with a monochromatic Al K$\alpha$ X-ray source and a hemispherical analyzer (Phoibos150 from SPECS), mounted at 50° take-off angle, defined from the normal to the sample surface.

Figure 3.2 presents XPS spectra acquired at different stages of the gate stack deposition process. The starting surface after hydrogen-plasma clean (Fig. 3.2(a)) is $(4 \times 2)$-reconstructed (from reflection high-energy electron diffraction (RHEED), not shown) and free of InGaAs oxides (controlled on As2p, Ga2p and Ind3d, not shown). Then, a-Si deposition is carried out (Fig. 3.2(b)). The Si2p/Ga3p peak area ratio is proportional to the thickness of elemental Si and is used to adjust the thickness to 10 Å. $Al_2O_3$ is deposited without any oxidation of a-Si or InGaAs indicating the formation of a sharp, stable interface (Fig. 3.2(c)). Nevertheless, Al sub-oxides are detected (Fig. 3.2(b)). Upon $HfO_2$ deposition and post-metalization anneal, only 0.5 Å and 2.5 Å of a-Si is oxidized, respectively (Fig. 3.2(e,h)). At the end of the process, the $Al_2O_3$ layer is fully oxidized but shifts with respect to its bulk position indicating the formation of an Hf-Al-O alloy at the a-Si/$HfO_2$ interface. During the whole process, the InGaAs surface is not oxidized thanks to the remaining elemental a-Si and $Al_2O_3$ barrier layers.

Those results suggest that $D_{it}$ originating from InGaAs oxides should be suppressed using this process. Resulting CET is expected to be low as the HK layer is scaled and

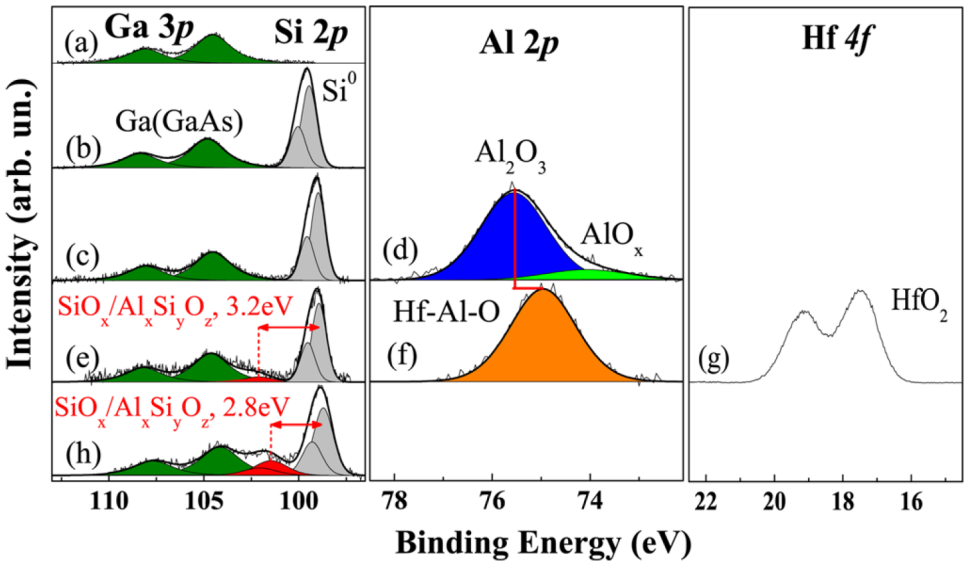



**Figure 3.2:** Ga3p, Si2p and Al2p core level XPS spectra after (a) hydrogen plasma, (b) 1 nm Si, (c-d) 1 nm $Al_2O_3$, (e-g) 2 nm $HfO_2$, (h) post-metallization anneal at 550°C in Ar for 30 min.

there is less than 3 Å of low-k oxides ($SiO_2$). The thermal stability should be excellent as almost no chemical changes are detected upon 550°C anneal. The electrical results in the next section support these assumptions.

#### 3.2.1.3 MOSCAP electrical characterization

Multi-frequency C-V characteristics acquired between 1 kHz and 1 MHz at room temperature are presented in Fig. 3.3(a). Firstly, a high accumulation capacitance is measured reaching 2.7 $\mu$F/cm$^2$ which corresponds to a CET of 12.7 Å. This result is consistent with the physical thickness of the deposited stack (3 nm Hf-Al-O with $k_{average}$ = 16 and 2.5 Å of $SiO_2$) as long as the remaining elemental a-Si is not included as part of the gate stack. It suggests that the accumulation layer forms at the a-Si/$Al_2O_3$ interface which might lead to a degradation of the transport properties in MOSFETs. If the accumulation layer would form at the a-Si/InGaAs interface, an accumulation capacitance of 2.2 $\mu$F/cm$^2$ to 2.3 $\mu$F/cm$^2$ would be expected. Secondly, the hysteresis at half the accumulation capacitance (gate voltage ($V_g$) = -0.25 V) is less than 10 mV for both 1 MHz and 100 kHz curves, which is very low compared to gate stacks having a direct HK/InGaAs interface [70]. Thirdly, the peak $D_{it}$ extracted by the high-low frequency method [77] is $5.5 \times 10^{12}$ eV$^{-1}$cm$^{-2}$ (Fig. 3.3(b)). Although the XPS chemical analysis indicated the absence of InGaAs oxides, multi-frequency C-V results clearly point to the presence of a significant $D_{it}$ in the bandgap: a large portion of the $D_{it}$ originates from the reconstructed InGaAs

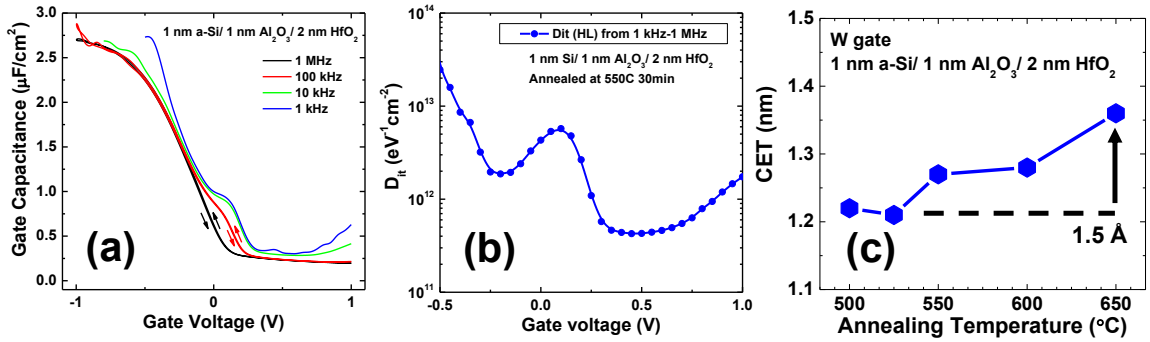



**Figure 3.3:** (a) C-V characteristics of a W/2 nm $HfO_2$/1 nm $Al_2O_3$/1 nm a-Si/$In_{0.53}Ga_{0.47}As$ MOS capacitor annealed at 550°C in Ar for 30 minutes and measured at 25°C in the dark from 1 kHz to 1 MHz. 100 kHz and 1 MHz curves are plotted with forward and reverse sweep. (b) $D_{it}$ versus gate voltage extracted by the high-low frequency method [77]. (c) CET measured at 1 MHz versus annealing temperature in Ar for 30 minutes.

surface (dangling or metallic bonds), or from its bonds with a-Si. Finally, the leakage current at $V_g$ = -1 V is $7.1 \times 10^{-1}$ A/cm$^2$. These results are remarkable for an MOS stack on InGaAs annealed at 550°C for 30 minutes.

The CET stability versus annealing temperature is reported in (Fig. 3.3(c)). A moderate 1.5 Å increase of the CET is observed upon increased temperature from 500°C to 650 °C. It highlights the good thermal stability of the a-Si/HK interface. It will be further discussed in the context of the impact of gate metal electrode on thermal stability in section 3.2.2.1.

It should be pointed out that the high-low frequency method [77] to extract $D_{it}$ values assumes that: 1) the C-V curve used as a high frequency reference is high enough such that no traps can respond to the *a.c.* signal (the presence of $D_{it}$ only appears as a stretch-out but not as additional capacitance); and 2) the C-V curve used as a low frequency reference contains the full *a.c.* response of all traps in the capacitance signal. When both of these conditions are satisfied for a certain bias range, the extracted $D_{it}$ numbers are accurate. If the high-frequency curve contains some capacitance response associated with traps, or if the low frequency curve does not contain the full response of traps, the extracted $D_{it}$ numbers are underestimated. In Fig. 3.3(a), it can be seen that the 10 kHz and 1 kHz C-V curves are almost identical which tends to confirm the saturation of the $D_{it}$ response at those low frequencies. Whether the 1 MHz C-V curve contains or not some capacitance response of traps is more difficult to assess. Consistent split C-V data are obtained on MOSFETs as reported in the next section. By comparing these split C-V characteristics with those of MOSFETs having gate stacks with a direct HK/InGaAs interface in Chapter 4 section 4.2.2, it will be demonstrated that the stretch-

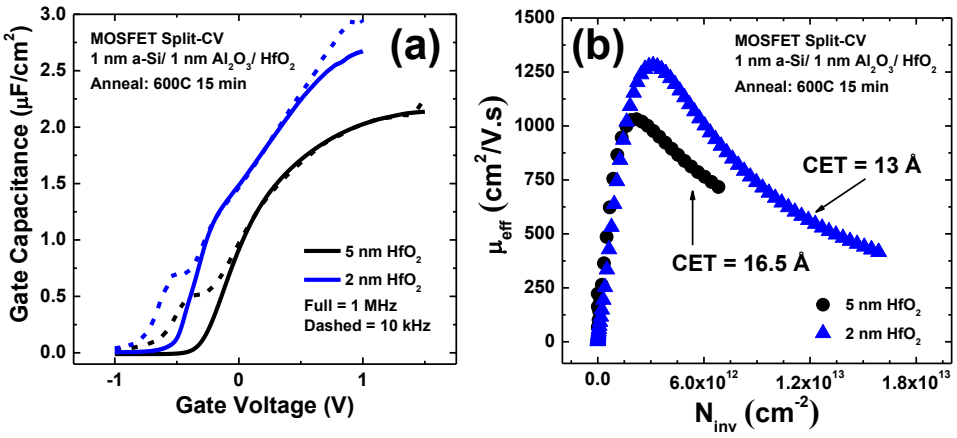



**Figure 3.4:** (a) Split C-V characteristics of W/$HfO_2$/1 nm $Al_2O_3$/1 nm a-Si/$In_{0.53}Ga_{0.47}As$ MOSFETs with $HfO_2$ of nominally 5 nm and 2 nm annealed at 600°C for 15 minutes in the MOVPE system and measured at 25°C in the dark from 10 kHz to 1 MHz. (b) Effective mobility ($\mu_{eff}$) versus inversion-charge density ($N_{inv}$) for the same MOSFETs. The channel is 10 nm thick and non-intentionally doped (NID), on NID $In_{0.52}Al_{0.48}As$ on InP.

out in a-Si-based stacks is much more pronounced which seem to indicate that the 1 MHz C-V curve contains a non-negligible response of traps and the extracted $D_{it}$ numbers are thus underestimated. It will be further confirmed by comparing the long-channel SS of transistors which is mostly influenced by $D_{it}$.

#### 3.2.1.4 Split C-V and Effective mobility

The a-Si-based gate stack is integrated in GF self-aligned $In_{0.53}Ga_{0.47}As$ MOSFETs (see Chapter 4 section 4.2). The channel is 10 nm thick and non-intentionally doped (NID), grown on 100 nm of NID $In_{0.52}Al_{0.48}As$ on semi-insulating InP. The residual doping is estimated to be n-type, below $2 \times 10^{16}$ $cm^{-3}$. The maximum thermal budget is 600°C for 15 minutes, corresponding to the RSD module with Si as n-dopants (see section 3.3.1). Two wafers are prepared with nominally 5 nm or 2 nm of $HfO_2$ on 1 nm $Al_2O_3$/1 nm a-Si and with a W gate.

Split C-V measurements are performed on transistors with a gate length of 25 $\mu$m (Fig. 3.4(a)). A large increase of the maximum accumulation capacitance upon $HfO_2$ scaling is observed from 2.1 $\mu F/cm^2$ to 2.65 $\mu F/cm^2$ which represents a CET reduction from 16.5 Å to 13 Å. An inaccuracy is expected in the $HfO_2$ thickness as this sample corresponds to the first attempt to deposit a thick layer by MBD. The $HfO_2$ thickness cannot be measured by XPS and adjusted (as usual) since photoelectrons from the InGaAs bulk are absorbed in the thick $HfO_2$ and not detected. Based on the CET values, it

most likely means that the deposited $HfO_2$ thickness is closer to 4 nm than 5 nm. A minimum capacitance in depletion below $1 \times 10^{-2}$ $\mu F/cm^2$ indicates the expected full depletion of the channel in off-state. The frequency dispersion behavior appears to be very similar to the MOSCAP data, although probing the upper half of the bandgap. A small frequency dispersion is observed in accumulation and around flatband (smaller than for p-type capacitors), while a peak $D_{it}$ response of $5.8 \times 10^{12}$ $eV^{-1}cm^{-2}$ is present, extracted by the high-low frequency method between 1 MHz and 1 kHz. Those results are in agreement with the $D_{it}$ profile extracted from a-Si MOSCAPs (Fig. 3.3(b)): a high peak midgap $D_{it}$ and a smaller $D_{it}$ towards the conduction band than towards the valence band, as can be reported on gate stacks with a direct HK/InGaAs interface [66]. As discussed in the previous section, these extracted $D_{it}$ values are most likely underestimated due to a non-negligible trap response in the 1 MHz split C-V curves.

The effective mobility ($\mu_{eff}$) versus channel charge density is calculated from the transfer characteristics of the MOSFETs and the split C-V measurements (Fig. 3.4(b)). The peak $\mu_{eff}$ increases from 1040 $cm^2/V.s$ to 1270 $cm^2/V.s$ upon scaling of the $HfO_2$ thickness. Since no change in the surface roughness is observed and only a marginal increase of the peak mobility is measured at low temperature (not shown), the increase of the peak $\mu_{eff}$ is attributed to a reduction of remote Coulomb scattering associated with fixed charges present in the bulk of the $HfO_2$ layer. As a negative $V_T$ shift appears upon $HfO_2$ scaling, it is concluded that a significant density of fixed positive charges is present in the $Al_2O_3$/a-Si stack which is compensated by fixed negative charges in the $HfO_2$. A reduction of the $HfO_2$ thickness yields a negative $V_T$ shift as the net fixed charge becomes more positive.

More device results with an a-Si gate stack are presented in Chapter 4 section 4.2 and compared to devices with a direct HK/InGaAs interface. In the next section, the influence of the gate metal on the gate stack properties is explored as a potential way to further improve CET and $D_{it}$ scaling.

### 3.2.2 Remote oxygen scavenging on high-k/InGaAs interfaces

The gate metal is known to play an important role in HKMG technology on Si not only to adjust the $V_T$ of transistors but also to scale CET. For instance, the remote interfacial layer scavenging technique presented in [78] relies on the use of a metal element in the gate having a higher oxygen affinity than Si such that the Metal/$SiO_2$ system evolves to Metal-oxide/Si (governed by the Gibbs free energy of formation). Oxygen from the $SiO_2$ interlayer gets transfered to the gate metal, which can significantly reduce the CET.

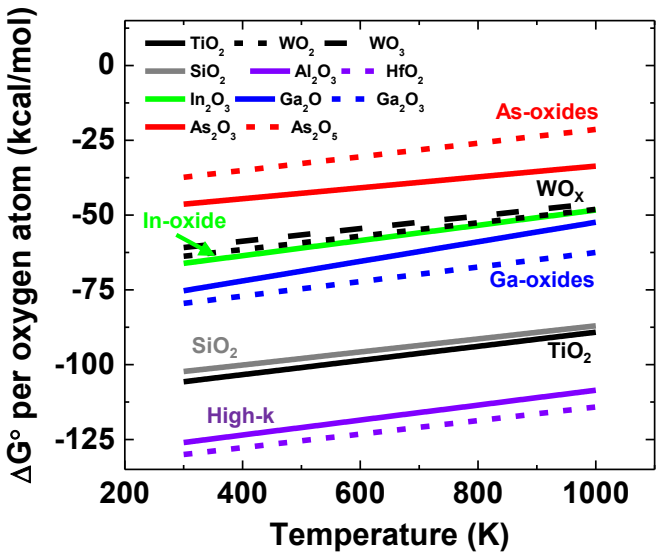



**Figure 3.5:** Gibbs free energy of oxidation per Oxygen atom plotted at 1 atm versus temperature for InGaAs oxides, high-k dielectrics ($HfO_2$, $Al_2O_3$), $SiO_2$, W oxides and titanium-oxide ($TiO_2$). Values calculated based on thermodynamic properties in [79, 80].

Figure 3.5 presents the calculated Gibbs free energy of formation of relevant oxides (for the InGaAs MOSs system) versus temperature at 1 atmosphere. The energies are normalized per oxygen atom such that the difference of energies in this plot directly relates to the energy associated with the transfer of an oxygen atom from one oxide complex to another. A negative change of the Gibbs free energy for a reaction at fixed temperature and pressure indicates that the reaction is evolving towards a thermodynamic equilibrium. Therefore, oxygen will tend to transfer from higher to lower Gibbs free energy oxides meaning that elements appearing lower in Fig. 3.5 have a stronger oxygen affinity. This is illustrated in the following example with the proposed oxygen transfer from Si to Ti. This reaction is spontaneous as the difference in Gibbs free energy of formation of $TiO_2$ and $SiO_2$ is negative.

$$SiO_2 + Ti \rightarrow Si + TiO_2 \tag{3.1}$$

$$\Delta G^{\circ}_{reaction} = (\Delta G^{\circ}_{TiO_2} + \Delta G^{\circ}_{Si}) - (\Delta G^{\circ}_{Ti} + \Delta G^{\circ}_{SiO_2}) = \Delta G^{\circ}_{TiO_2} - \Delta G^{\circ}_{SiO_2} \tag{3.2}$$

From Fig. 3.5, the relative energy ordering of the presented species does not evolve in the temperature range of interest, thus the tendency of oxygen to transfer from one

element to another will remain unchanged from room temperature to 1000 K. Those observations are indicative for a practical use, as they do not take into account the kinetic of a given reaction, and are true for stoichiometric compositions only. The reaction rate is governed by an Arrhenius law: a reaction might not occur at room temperature but an increasing thermal budget might trigger it once the activation energy is reached.

In the following paragraphs, the impact of the gate metal on interfacial reactions in MOS stacks on InGaAs will be discussed, focusing first on a-Si containing gate stacks (section 3.2.2.1) and then on direct high-k/InGaAs interfaces (section 3.2.2.2).

#### 3.2.2.1 High-k/a-Si/InGaAs interfaces

Figure 3.5 gives interesting insights into the mechanism of remote oxygen scavenging in HKMG stacks on Si, typically being composed of titanium nitride (TiN)/ $HfO_2$/ $SiO_2$/ Si. First of all, the considered HK layers ($HfO_2$ and $Al_2O_3$) are the oxides with the strongest oxygen affinity in this system. They will tend to get fully oxidized first. Secondly, Ti has a slightly stronger oxygen affinity than Si meaning that oxygen from the $SiO_2$ interfacial layer will tend to transfer to Ti in a Ti-rich TiN gate metal. Therefore, upon high-enough thermal budget and assuming that oxygen can easily diffuse through the HK layers [81], the interfacial $SiO_2$ will thin down until: a) it disappears completely as all oxygen is transferred to Ti; b) all the excess Ti in TiN gets oxidized; or c) the system is cooled down before completion of the reaction. Adjusting the exact thermal budget (temperature and time) or the dose of excess Ti in the gate metal defines the remaining $SiO_2$ thickness and thus the final CET.

The same principle can be applied to the a-Si-based gate stack on InGaAs. In section 3.2.1, W is used as a gate metal. A CET versus annealing temperature study (Fig. 3.3(c)) reveals a moderate 1.5 Å increase of the CET at high temperature. This phenomenon can be explained from Fig. 3.5 by the fact that in this system, besides the HK layers which are fully oxidized (Fig. 3.2), a-Si has the highest oxygen affinity. Upon annealing, any available oxygen will thus contribute to the formation of an $SiO_2$ layer. As no InGaAs oxides are detected, it implies that the W gate acts as a source for oxygen which regrows the $SiO_2$ interlayer and increases the CET. Similar observations were made on HKMG on Si [82].

In the presence of Titanium, Ti-rich TiN or aluminum as gate metals having a higher oxygen affinity than Si, the interfacial layer regrowth can be suppressed or even reversed such that the CET gets reduced upon annealing. As this $SiO_2$ interlayer is not at the InGaAs interface, no variation in $D_{it}$ is expected with a change of its thickness.

MOSCAPs are fabricated with 2.4 nm $HfO_2$/ 1.3 nm $Al_2O_3$/ 1 nm a-Si on $In_{0.53}Ga_{0.47}As$

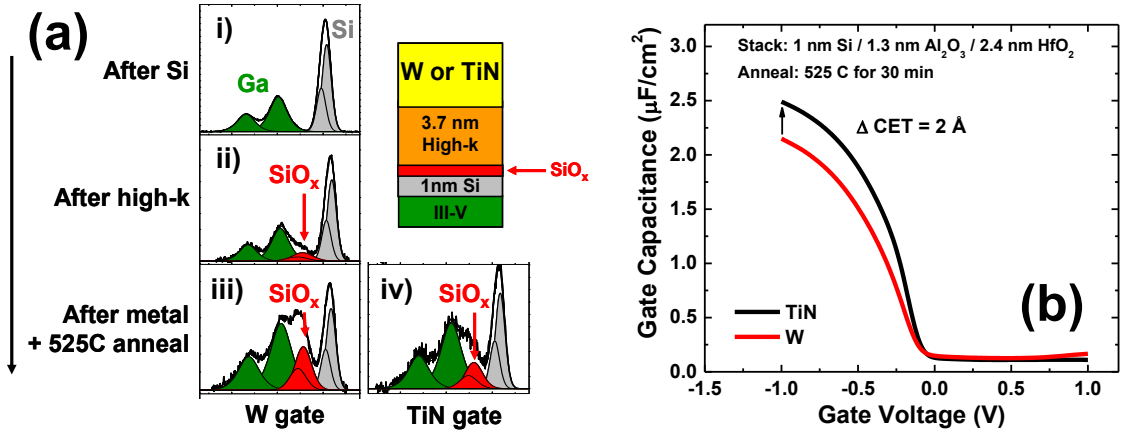



**Figure 3.6:** (a) Ga3p and Si2p core level XPS spectra after (i) hydrogen plasma and 1 nm a-Si deposition, (ii) 1.3 nm $Al_2O_3$ and 2.4 nm $HfO_2$ deposition, (iv) post-metallization anneal at 525°C in Ar for 30 min. (b) MOSCAPs C-V characteristics at 1 MHz with two different gate metals (TiN and W).

with a W or Ti-rich TiN metal gate. The samples are annealed at 525°C for 30 minutes. XPS chemical analysis is performed at each step of the process to monitor the thickness of elemental a-Si (Fig. 3.6(a)). For the spectra acquired after post-metal-deposition anneal, the gate metal is removed by dry etching before the analysis. A large amount of fluorine is detected in the $HfO_2$ due to the dry etching process but not in the $Al_2O_3$ or underlying layers giving confidence that the chemical analysis of the a-Si layer is not influenced by the dry etch process.

In the W case, similar results to those in Fig. 3.2 are obtained: 0.5 Å of elemental a-Si consumed upon $HfO_2$ deposition and additional 2.5 Å upon anneal. In the TiN case, only 1.5 Å of elemental a-Si is consumed throughout the whole process meaning that the TiN gate scavenged or prevented the formation of 1.5Å of $SiO_2$ at 525°C. This result is confirmed with C-V measurements on MOSCAPs (Fig. 3.6(b)) where a 2 Å reduction of the CET is observed. In addition, no $V_T$ shift or change of $D_{it}$ response (not shown) can be detected indicating that no fixed charges or interface/border traps are associated with the $SiO_2$ layer.

These results are in agreement with the Gibbs free energy plot (Fig. 3.5) as contrary to the case of W, TiN has a slightly higher oxygen affinity than $SiO_2$. Oxygen is thus expected to transfer from the $SiO_2$ interlayer towards the gate metal, inducing a scaling of the CET with no change in $D_{it}$. The remaining 1.5 Å $SiO_2$ seen by XPS (Fig. 3.6(a)) could originate from Si-O-Al bonds which would be more stable than $TiO_2$, or from a complete oxidation of the excess Ti in the 5 nm thick Ti-rich TiN gate metal.

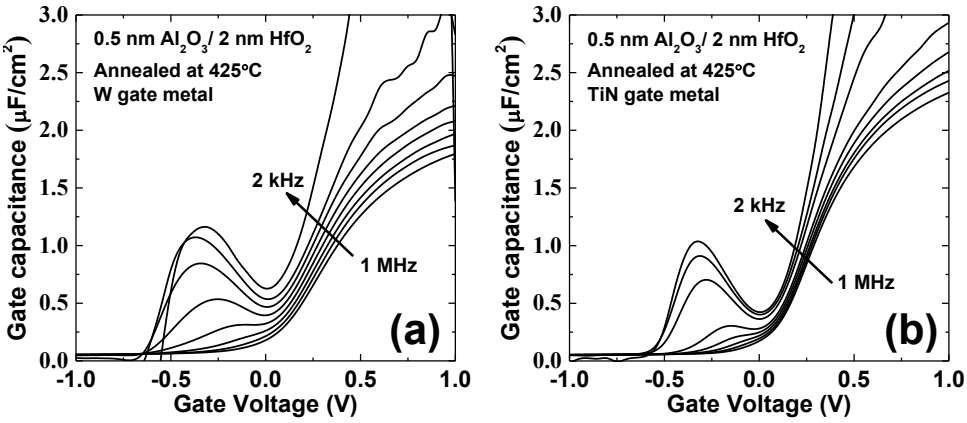



**Figure 3.7:** Multi-frequency C-V characteristics of MOSCAPs with (a) W and (b) TiN gate metal on 2 nm $HfO_2$/ 0.5 nm $Al_2O_3$/ n-type $In_{0.53}Ga_{0.47}As$, annealed at 425°C in Ar for 30 minutes. Measurements acquired at room temperature between 1 MHz and 2 kHz.

#### 3.2.2.2 Direct high-k/InGaAs interface

Oxygen scavenging might bring significant advantages to the development of MOS stacks on InGaAs going beyond the simple CET improvement observed in the case of a-Si containing gate stacks. The lower thermodynamic stability of InGaAs oxides compared to $SiO_2$ points to an easier transfer of oxygen from the HK/InGaAs interface towards the scavenging element (metal in the gate or oxygen-deficient HK). Furthermore, as InGaAs oxides are often referred to as being the origin of a substantial part of the $D_{it}$ at the HK/InGaAs interface, transferring oxygen from InGaAs oxides towards the gate metal could yield to large improvements in $D_{it}$.

MOSCAPs are fabricated with 2 nm $HfO_2$/ 0.5 nm $Al_2O_3$ on $In_{0.53}Ga_{0.47}As$ with a W or Ti-rich TiN metal gate. The samples are either measured with no further anneal or after anneals at temperatures ranging from 350°C to 500°C in Ar for 30 minutes. The surface preparation prior to HK deposition is a 1 minute DHF clean. The HK layers are deposited by thermal ALD at 250°C. The anneals are carried out in purified Ar and not in $H_2$/Ar to make sure that changes of $D_{it}$ are intrinsic and not related to hydrogen reducing oxides or passivating dangling/metallic bonds.

Figure 3.7 presents the multi-frequency C-V characteristics of MOSCAPs with a W or Ti-rich TiN metal gate annealed at 425°C. Two major differences are striking. Firstly, while the HK thickness is the same on both samples, a large difference in CET of 2.7 Å is observed pointing to a difference in the resulting HK/InGaAs interlayer thickness. Secondly, the frequency dispersion in depletion and around flatband is strongly reduced indicating a reduction of $D_{it}$. Indeed, all InGaAs oxide species have a significantly lower

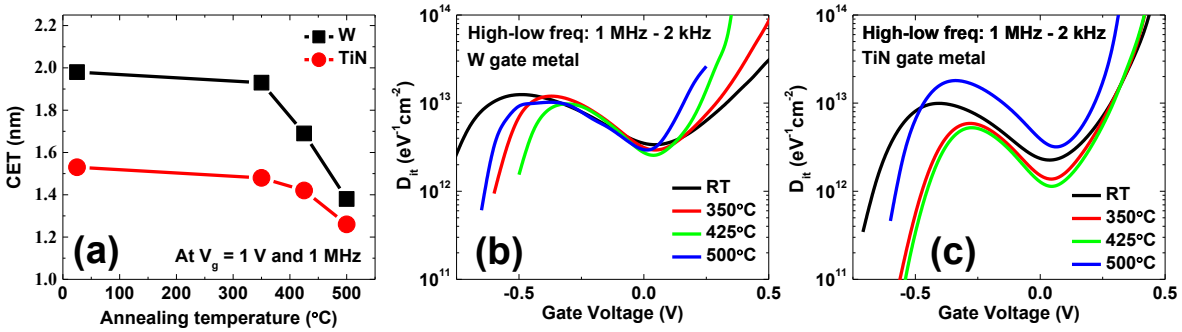



**Figure 3.8:** (a) CET versus annealing temperature in Ar for 30 minutes on MOSCAPs with W or TiN gate metal on 2 nm $HfO_2$/ 0.5 nm $Al_2O_3$/ n-type $In_{0.53}Ga_{0.47}As$. (b) $D_{it}$ versus annealing temperature for MOSCAPs with W or (c) TiN as gate electrode.

Gibbs free energy of formation than $TiO_2$ meaning that InGaAs oxides have a strong tendency to decompose and transfer oxygen towards the TiN gate metal. On the contrary, the oxygen affinity of W is only higher than the one of As-oxides. Therefore, only As-oxides might transfer to the W gate but are also likely to convert into more stable In- or Ga-oxides.

This simple picture becomes more complex when studying the temperature evolution of CET and $D_{it}$ in MOSCAPs with W or Ti-rich TiN gates. Figure 3.8(a) reports CET versus annealing temperature up to 500°C, while $D_{it}$ profiles extracted by the high-low frequency method are reported in Fig. 3.8(b) and (c). For this calculation, the accumulation capacitance at 1 MHz and $V_g = 1$ V is used as oxide capacitance ($C_{ox}$) in order to deconvolute the contribution of CET scaling from the intrinsic change of $D_{it}$. The $D_{it}$ numbers are thus over-estimated.

The largest difference in CET of 4.5 Å is observed on MOSCAPs which are not annealed. As gate metal deposition is performed at room temperature, it indicates that a significant oxygen transfer already happens during TiN deposition at room temperature. The InGaAs oxide thicknesses present after W and TiN metal deposition are estimated to be respectively 10 Å CET and 5 Å CET. A moderate decrease of CET is observed up to 350°C followed by a significant reduction of CET up to 500°C, down to 13.8 Å and 12.6 Å for W and TiN respectively. The remaining InGaAs oxides are estimated to contribute for 4 Å and 3 Å CET respectively, close to the minimum required to form the HK/InGaAs interface.

From Fig. 3.8(b), it can be observed that while a significant change of CET occurs in the case of W gate, there is barely no change in $D_{it}$ for the whole temperature range. With a TiN metal gate (Fig. 3.8(c)), a substantial improvement in $D_{it}$ occurs up to 425°C

followed by an increase at 500°C, to a level comparable to that of the W gate.

With a TiN gate, all InGaAs oxides are expected to be reduced by the gate metal. Most of them are already decomposed at room temperature (probably the As- and In-oxides), and the more stable Ga-oxides get reduced upon annealing up to the point where only the connections between InGaAs and $Al_2O_3$ remain, around 425°C. This is accompanied by an improvement of $D_{it}$ related to the reduction of InGaAs oxides. At 500°C and above, thermal desorption of remaining Ga-oxides and up diffusion of InGaAs elements into the HK stack might explain the decrease in CET, increase in $D_{it}$ and leakage. Another possible cause of the increase in $D_{it}$ is the increased density of metallic bonds and/or dangling bonds upon reconstruction of the interface in the absence of InGaAs oxides interlayer.

With a W gate, twice the amount of InGaAs oxides is detected at room temperature compared to TiN, since W cannot scavenge In- and Ga-oxides. This probably explains the higher $D_{it}$ at room temperature compared to TiN. At 350°C, the system behaves as with TiN meaning that almost no oxygen transfer occurs (no change in CET) as all possible reactions are probably below their activation energy. Increasing the temperature up to 500°C results in a strong reduction by 5 Å of CET which is associated with no change in $D_{it}$. As per Fig. 3.5, the only possible reactions are a transfer of oxygen from As- and In-oxides towards Ga-oxide which can have a higher dielectric constant and/or a thermal desorption of those oxides. Since the $D_{it}$ profile does not change, it implies that either those reacting oxides are not responsible for $D_{it}$ in the upper half of the bandgap, or that the reduction of $D_{it}$ induced by their dissociation is compensated by the creation of metallic and/or dangling bonds adding $D_{it}$ in the upper half of the bandgap.

In light of the comparison of W and TiN gates, it appears that the low temperature behavior (below 350°C) can be properly explained by a simple oxygen scavenging model governed by the Gibbs free energies of formation of oxides, while oxygen scavenging competes with thermal desorption at higher temperatures. A chemical analysis of the gate stack versus temperature was carried out by XPS on a hard X-ray synchrotron beamline in SOLEIL to distinguish between oxygen transfer to the gate metal or thermal desorption. Hard X-rays were necessary to see photoemission from both InGaAs/HK and HK/metal-gate interfaces, as the total HKMG stack is 9 nm thick. Unfortunately, the study was not conclusive: Firstly, the InGaAs-oxide photoemission signals have a significant overlap with photoemission from $HfO_2$ and TiN thus reducing the sensitivity of the analysis ; secondly, the differences of oxide thickness mentioned here (few Å CET) appeared to be beyond the sensitivity limit with hard X-rays. Further analysis will be performed by TEM.

Nevertheless, the results obtained in this section clearly point to the crucial role of the

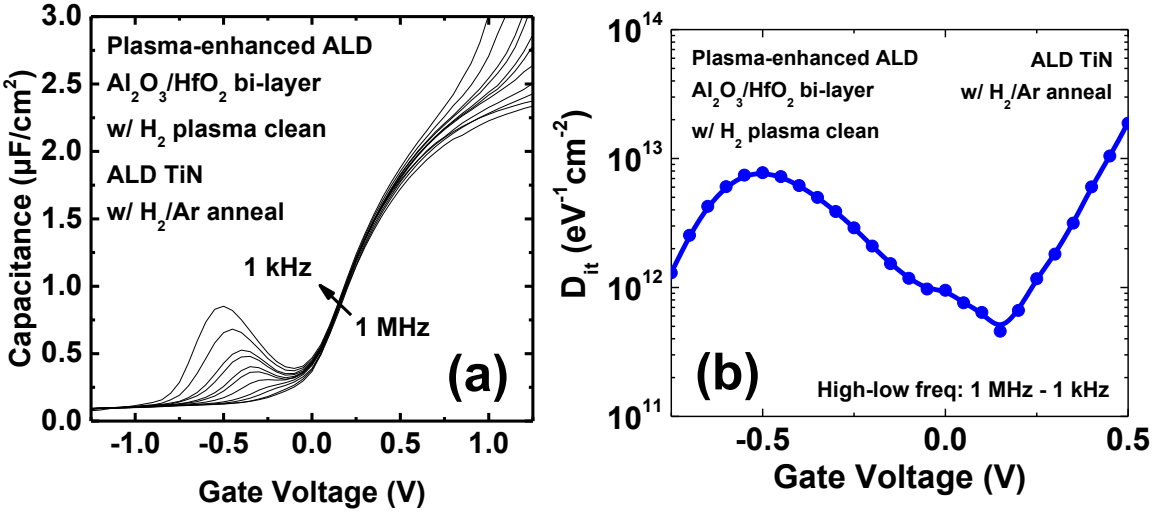



**Figure 3.9:** (a) Multi-frequency C-V characteristics from 1 MHz to 1 kHz of a MOSCAP with an optimized PEALD stack comprising an in-situ hydrogen-plasma surface clean, an $Al_2O_3/HfO_2$ bi-layer and in-situ Ti-rich TiN gate metal annealed in $H_2$/Ar. (b) Corresponding $D_{it}$ versus gate voltage profile extracted by the high-low frequency method between 1 MHz and 1 kHz.

gate metal as an additional factor for improving MOS interfaces on InGaAs. Significant CET reduction can be obtained as well as improvements in $D_{it}$ for direct HK/InGaAs interfaces as long as the thermal budget is carefully optimized.

### 3.2.3 Optimized plasma-based high-k/InGaAs gate stack

Based on findings from the previous sections, the formation of a low-$D_{it}$ direct HK/InGaAs interface with a scaled CET boils down to the accurate control of the interfacial layer by tuning the surface clean, initial stages of HK deposition, gate metal composition and thermal budget. In this section, results are presented on an optimized gate stack which integrate all the previously mentioned features.

The use of optimized *ex-situ* wet chemical treatments [83] was shown to greatly improve the control over the interfacial layer but it limits the CET scalability as the transfer in air from the wet chemistry to the ALD reactor always results in some oxide regrowth. Ideally, one would prefer to clean the InGaAs surface *in-situ*, in the ALD reactor, prior to HK deposition. Another important aspect is to mitigate the InGaAs surface oxidation during the initial stages of HK deposition by controlling the strength of the oxidation half-cycle during the first ALD cycles.

PEALD is rapidly gaining popularity over the conventional thermal ALD due to additional advantages, including improved material properties, deposition at reduced substrate

temperatures, increased choice of precursors, and good control over film stoichiometry and impurity [84]. In addition, it provides the unique opportunity to use *in-situ* plasma treatments to clean surfaces as well as a large control over the plasma density and energy during the oxidation half-cycle.

The key features of PEALD open a whole new range of opportunities to improve HK/InGaAs interfaces. Firstly, it is proposed to transfer the hydrogen-plasma clean for InGaAs oxides from the UHV MBD chamber (section 3.2.1, [76]) to the PEALD reactor in order to offer an *in-situ* clean of the InGaAs surface. Secondly, a low density and low energy $O_2$ plasma step replaces the $H_2O$ pulse as the oxidant to avoid/minimize plasma-induced damages and oxidation of the InGaAs surface. In this way, the formation of interfacial oxides can be reduced to its absolute minimum. Thirdly, an *in-situ* plasma-enhanced Ti-rich TiN gate metal is used to prevent excess oxygen incorporation in the gate stack through moisture adsorption in hygroscopic $HfO_2$, and as a remote oxygen scavenger. Finally, a hydrogen ($H_2$)/Ar annealing step is performed as it appears to largely reduce the density of fixed charges and $D_{it}$.

The details of this process optimization are beyond the scope of this work as they are mostly carried out by Dr. Vladimir Djara and Dr. Éamon O'Connor. Nevertheless, since the gate stack is integrated in InGaAs MOSFETs in Chapter 4 section 4.3.2, the resulting stack properties are presented here. Figure 3.9(a) presents the multi-frequency C-V characteristic from 1 MHz to 1 kHz of a MOSCAP with the plasma-based optimized gate stack. A competitive CET of 15.5 Å at $V_g = 1$ V is reached as well as a remarkably low frequency dispersion in the transition region from the onset of depletion ($V_g = 0$ V) towards accumulation ($V_g = 0.5$ V). It points to a low $D_{it}$ in the upper part of the InGaAs bandgap, crucial for the resulting SS in MOSFETs. The $D_{it}$ hump in depletion ($V_g$ = -0.5 V) and the C-V divergence in accumulation at low-frequencies are smaller than in Fig. 3.7(b) pointing to a smaller mid-gap $D_{it}$ and a smaller gate leakage for the same CET. The $D_{it}$ extraction obtained by the high-low frequency method between 1 MHz and 1 kHz (Fig. 3.9(b)) confirms a 5-fold reduction $D_{it}$ through the whole upper-half of the bandgap compared to Fig. 3.8(c), reaching an excellent minimum $D_{it}$ below $5 \times 10^{11}$ $eV^{-1}cm^{-2}$.

Those promising MOSCAP results translate to excellent subthreshold performance in self-aligned $In_{0.53}Ga_{0.47}As$ MOSFETs with a replacement-gate process (Chapter 4, section 4.3.2).

## 3.3 Contacts

In order to benefit from InGaAs superior transport properties and achieve a high drain current performance, it is crucial to develop low resistance self-aligned S/D access regions suitable for high-performance logic at 10 nm node and beyond. These contacts have to be highly compatible with standard CMOS flows, scalable to the small-pitch requirements and thermally stable to stand the back-end process.

Several approaches have been tried such as ion implantation which has shown its limits due to the too high thermal budget required to achieve a decent S/D dopant activation [85, 86]. Selective epitaxy of *in-situ* doped InGaAs S/D regions has been done by MBE [87, 88], and MOVPE [89], achieving a high carrier density in a self-aligned gate-first (GF) scheme. These two approaches require a III-V cleaning recipe which includes a wet etch down to an etch-stop layer before regrowth. Etching the channel material prior to S/D formation is not an option in the case of fully-depleted architectures like planar UTBB or fins InGaAs-OI MOSFETs.

The formation of metal contacts with a low specific contact resistivity is typically achieved by the use of self-aligned Nickel-silicide on Si. Self-alignment of the metal contacts helps in reducing the contribution of the S/D sheet resistance in the total external resistance of the MOSFETs. A similar concept can be applied to InGaAs to obtain self-aligned metal contacts, as proposed in [90]. Nevertheless, excellent specific contact resistivity values are reported with non self-aligned direct metal contacts [91, 92] and might thus be also considered.

In this section, the use of selectively grown *in-situ* doped InGaAs RSD is proposed. Combined with a gate-first (GF) integration on fully-depleted channels (GF is taken as an example, results would also apply to replacement metal-gate (RMG)), a specific pre-epitaxy surface clean is developed with no recess of the channel (section 3.3.1). Self-aligned Ni-InGaAs metal contacts on RSD are evaluated with a focus on the selective removal of unreacted Ni as well as thermal stability of specific contact resistivity to doped RSD (section 3.3.2). Finally, direct metal contacts are studied and benchmarked to Ni-InGaAs in order to assess the real need for self-aligned metal contacts in InGaAs-based MOSFETs (section 3.3.3).

A summary of the proposed final architectures is presented in Fig. 3.10 for both self-aligned Ni-InGaAs contacts and direct metal contacts. The resistance contribution of first metalization level (M1) is a very challenging part of the total external resistance for advanced nodes but will not be discussed as the problem is not specific to InGaAs MOSFETs. The focus will be on the sheet resistance of RSD regions, metal/RSD contact

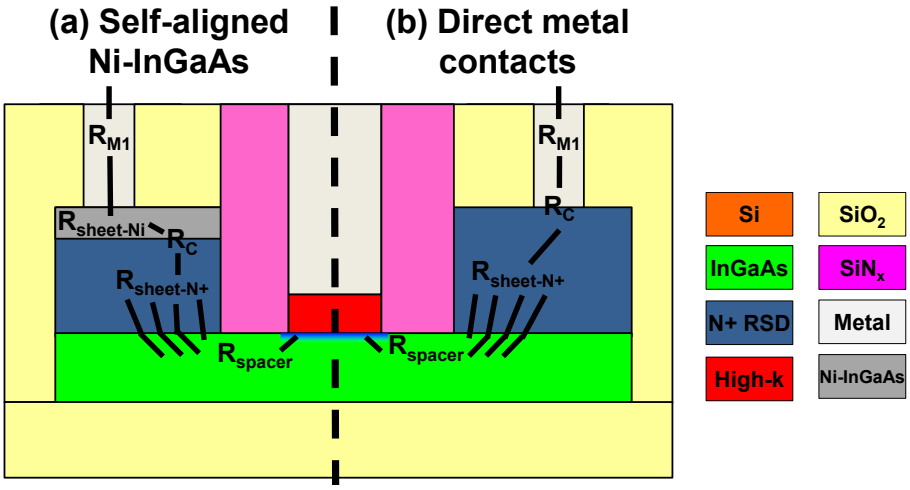



**Figure 3.10:** Schematic of a GF MOSFET with RSD and (a) Ni-InGaAs or (b) direct metal contacts with emphasis on the various contributions to external series resistance.

resistance and sheet resistance of the Ni-InGaAs layer. The resistance originating from the spacer region is beyond the scope of this chapter as it can only be investigated with fully-processed MOSFETs. It consists of a spreading resistance from the highly-doped RSD region to lowly-doped channel material and a sheet resistance beneath the spacers. It will be shown in Chapter 4 that it is the main source of external resistance for devices presented in this work.

### 3.3.1 Raised Source/Drain

High-performance scaled MOSFETs require an ultra-thin body under the gate for ideal electrostatic control as well as ultra-low series resistance originating from the S/D regions. Raised S/D (RSD) are typically used to thicken the channel material in the S/D regions to help reducing its resistance (as in Fig. 3.10). MOVPE is an excellent platform for the selective epitaxy of *in-situ* doped InGaAs RSD as is provides a high selectivity to oxides (see Chapter 2, section 2.3) and nitrides. In addition, it accommodates a wide-range of growth temperatures (from 450°C to 650°C for InGaAs) and n-type doping species (silicon, tin, tellurium, sulfur, among others). As any epitaxy technique, it requires a pristine crystalline surface for the growth of high-quality material, which can be challenging in S/D regions as the InGaAs surface sees numerous processing steps associated with the formation of the gate and spacers.

Firstly, a method is proposed to recover an "epi-ready" InGaAs surface after the gate and spacers patterning of a self-aligned GF MOSFET flow (see Chapter 4, section 4.2).

Then, the formation of highly-doped InGaAs RSD is studied for different doping species and temperatures.

#### 3.3.1.1 Raised S/D process

Two types of test wafers are processed in parallel to study the S/D regions process: gate-patterned wafers are used to demonstrate self-alignment of the final structure, highlight integration issues and test transistors; on the other hand, un-patterned characterization wafers are used to reproduce the process conditions seen by S/D regions during a regular transistor process. Characterization wafers serve to extract physico-chemical, structural and electrical properties of the S/D regions. In the next paragraph, typical process conditions are given for a GF flow as they are necessary to explain the chemical analysis of the surface prior RSD epitaxy (see Chapter 4 section 4.2, in particular Fig. 4.1 and Fig. 4.2 for further details).

Two sets of 2 inches "epi-ready" (100)-oriented semi-insulating InP wafers are loaded in a MOVPE system. After native oxide desorption under tributylphosphine (TBP) over-pressure, a 150 nm thick buffer of $In_{0.52}Al_{0.48}As$ and a 50 nm thick NID $In_{0.53}Ga_{0.47}As$ channel are grown at 600°C. The HK stack is then formed by ALD, followed by 30 nm of sputtered tungsten. The gate metal is capped by 50 nm of $SiN_x$ deposited by plasma-enhanced chemical vapor deposition (PECVD). At this point, gate lithography is performed only on the gate-patterned wafers. The $SiN_x$ gate cap is then dry etched by reactive ion etching (RIE) using a mixture of trifluoromethane ($CHF_3$) and oxygen oxygen ($O_2$). The gate metal is dry etched in the same RIE tool using hexafluoride ($SF_6$) and nitrogen ($N_2$). 15 nm of $SiN_x$ is deposited by PECVD and dry-etched in a mixture of $CHF_3$ and oxygen $O_2$ to form the spacers. Finally, the remaining damaged HK layer is removed in DHF. The InGaAs surface is now expected to be contaminated by fluorocarbon species, residual oxides and other organic contaminants which have to be properly cleaned to recover an "epi-ready" surface. The wafers are first cleaned in acetone, isopropanol and deionized (DI) water for 2 minutes each. Carbon contaminants are removed by a 4 minutes exposure to an ozone-rich (10 $g.m^{-3}$) DI water. An hydrophobic surface is then recovered after a DHF step which removes any oxide contaminants from the surface, with a good selectivity to the $SiN_x$ spacers and gate capping layer. An additional 4 minutes exposure to ozone-rich DI water is done to build up a thin native oxide, which is then stripped in diluted HCl (1:5 in water). The cleaned wafers are transferred in the MOVPE system for the RSD epitaxy. After native oxide thermal desorption under TBA, 50 nm of *in-situ* doped $In_{0.53}Ga_{0.47}As$ is grown selectively to the $SiN_x$ spacers and gate capping layer.

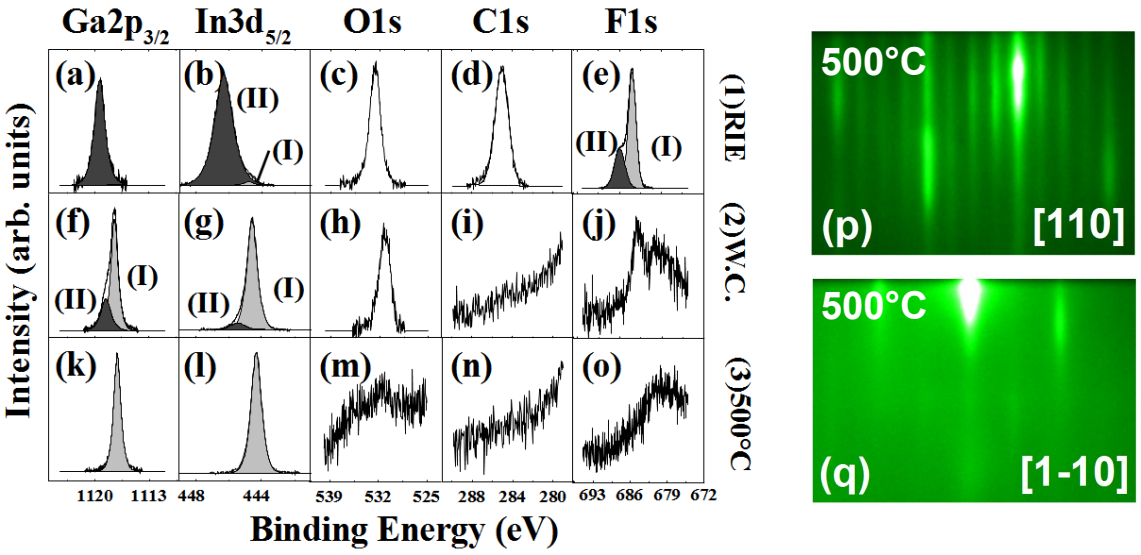



**Figure 3.11:** (a-o) XPS core levels of $Ga2p_{3/2}$, $In3d_{5/2}$, O1s, C1s and F1s recorded after different process steps. (1) Gate stack RIE, (2) Wet cleaning and (3) in-situ annealing at 500°C for 5 minutes. (p,q) (4×2) surface reconstruction recorded by RHEED along the (p) [110] and (q) [1-10] azimuths of $In_{0.53}Ga_{0.47}As$ (001), after in-situ annealing at 500°C for 5 minutes.

#### 3.3.1.2 Pre-epitaxy surface cleaning

XPS measurements and RHEED patterns are acquired on the characterization wafer after different process steps. Figure 3.11 displays the XPS core levels of $Ga2p_{3/2}$, $In3d_{5/2}$, O1s, C1s and F1s recorded after (1) gate RIE, (2) wet cleaning and (3) in-situ annealing at 500°C to reproduce the oxide desorption conditions seen by the wafer in the MOVPE system prior to RSD epitaxy.

The XPS analysis acquired after RIE process shows the presence of residual oxygen (Fig. 3.11(c)), carbon (Fig. 3.11(d)), and fluorine (Fig. 3.11(e)) at the top surface due to the $SF_6$:$N_2$ or $CHF_3/O_2$ gas mixtures used to etch the W gate metal and $SiN_x$ cap/spacers. One single peak is observed for O1s and C1s at binding energy (BE) 532.7 eV and 285 eV respectively. The F1s core level (Fig. 3.11(e)) can be decomposed into two peaks, one in light gray (I) related to fluorine bonded with InGaAs elements at 685.6 eV BE and one in dark gray (II) related to F-C bonds at 687.9 eV BE. These fluorine InGaAs bonds are also observed in the $Ga2p_{3/2}$ and $In3d_{5/2}$ core levels (Fig. 3.11(a) and (b)). The decomposition of the $Ga2p_{3/2}$ spectrum shows one single peak in dark gray at 1119.34 eV BE corresponding to Ga-F bonds, while the decomposition of the In3d5/2 signal shows two peaks denoted (II) in dark gray at 446.3 eV BE related to In-F bonds and (I) in light gray at 444.8 eV BE related to a weak indium signal from the bulk $In_{0.53}Ga_{0.47}As$. At this stage, no As2p peak is detected (not shown) indicating that the top surface layer

is mainly composed of Ga-F and In-F species. No RHEED pattern could be measured pointing out the presence of an amorphous, contaminated surface not suitable for epitaxy.

The XPS spectrum of the characterization wafer after wet cleaning confirms that carbon and fluorine species are efficiently removed (Fig. 3.11(i) and (j)). A very small peak of F above the noise level is only observed in the F1s spectrum. The $Ga2p_{3/2}$ (Fig. 3.11(f)), $In3d_{5/2}$ (Fig. 3.11(g)) and $As2p_{3/2}$ (not shown) peaks display the presence of strong signal related to $In_{0.53}Ga_{0.47}As$ bulk denoted (I) in light gray at 1117.45 eV BE for the $Ga2p_{3/2}$ and at 444.57 eV BE for $In3d_{5/2}$. Additional small components are observed after decomposition shifted at higher BE from the bulk peak, denoted (II) in dark gray at 1118.5 eV for $Ga2p_{3/2}$ and 444.5 eV for $In3d_{5/2}$ related to $In_{0.53}Ga_{0.47}As$ native oxides, ($Ga_2O$, $Ga_2O_3$) and ($In_2O_3$) respectively [93]. The $As2p_{3/2}$ core level (not shown) is decomposed in three components, one intense related to the $In_{0.53}Ga_{0.47}As$ bulk at 1322.87 eV BE and two additional shifted by 0.63 eV and 3.35 eV to higher BE from the bulk peak related to As-As bonds and $As_2O_3$ oxide respectively. A slight diffraction could be observed in the RHEED pattern (not shown) indicating a thin oxide coverage of the semiconductor crystal. An annealing in UHV at 500°C for 5 minuntes followed by *in-situ* XPS analysis is performed to confirm that a high-quality contamination-free "epi-ready" surface can be recovered. Figures 3.11(m), (n) and (o) show that the carbon and fluorine concentrations are reduced below detection limit of the instrument while a very small peak, just above the noise level, is however observed in the O1s spectrum. Only one component remains for the $Ga2p_{3/2}$ and $In3d_{5/2}$ peaks attributed to $In_{0.53}Ga_{0.47}As$ bulk as shown in Fig. 3.11(k), (l). $In_{0.53}Ga_{0.47}As$ native oxides are no more stable at this temperature. The RHEED patterns after annealing measured along the [110] and [1-10] directions (Fig. 3.11(p) and (q)) present a streaky bright (4×2) surface reconstruction indicating that the surface is smooth, well ordered and stabilized by group-III elements [94].

Those results confirm that a pristine "epi-ready" surface can be recovered in the S/D regions after the gate and spacers fabrication without any channel recess. From that point, several InGaAs RSD modules are developed with different doping species and processing temperatures. Details are given in the next paragraph.

#### 3.3.1.3 Highly doped $n^+$ InGaAs source/drain

The selective growth of $In_{0.53}Ga_{0.47}As$ RSD is investigated for different dopant species and growth conditions. The growth of 100 nm $In_{0.53}Ga_{0.47}As$ on semi-insulating InP is carried out with trimethylgallium (TMGa) and trimethylindium (TMIn) as group-III precursors in TBA over-pressure, with a V/III ratio of 20. The default growth temperature is 600°C.

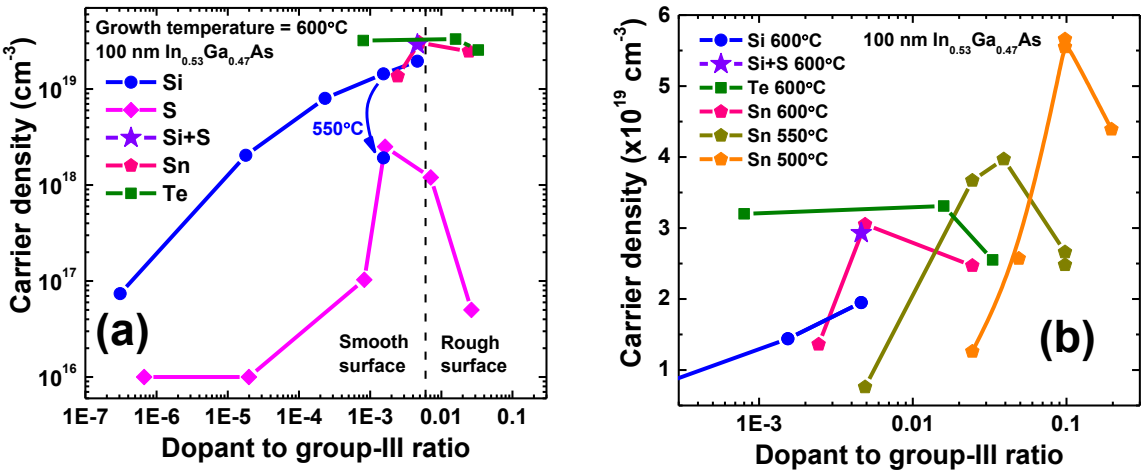



**Figure 3.12:** (a) Hall electron density versus dopant to group-III flux ratio for *in-situ* doped 100 nm thick $In_{0.53}Ga_{0.47}As$ grown at 600°C with different n-type dopant species. The blue arrow indicates a Si doped sample grown at 550°C. (b) Magnified Hall electron density versus dopant to group-III flux ratio focusing on the high doping region, for different dopant species and growth temperatures.

The n-type dopant precursors are disilane ($Si_2H_6$), hydrogen sulfide ($H_2S$), diethyl telluride (DETe) and tetraethyltin (TESn). The samples are characterized by Hall measurements in Van der Pauw configuration.

Firstly, samples are prepared at 600°C with $Si_2H_6$ or $H_2S$ as dopant precursors and dopant molar fluxes varying over 5 decades. The resulting Hall electron density is presented in Fig. 3.12(a). In the case of $Si_2H_6$, the electron density is steadily increasing with dopant flux up to $10^{19}$ $cm^{-3}$, then starts to saturate as a 10-fold increase in dopant flux yields a 2-fold increase in carrier concentration. Further increasing the $Si_2H_6$ flux results in a large degradation of the InGaAs morphology. Si, as a group-IV element, is an amphoteric dopant in III-V materials. Although it preferentially incorporates on group-III sites thus acting as n-type dopant, it might incorporate onto group-V sites at high dopant concentration thus acting as p-type dopant. Such self-compensation effect is a possible limiting factor to achieve higher Si active doping in InGaAs [95]. At too high fluxes, the InGaAs morphology is degraded as Si probably reaches its solubility limit in InGaAs at 600°C. A possible way to increase the incorporation of Si is to reduce the growth temperature which increases the solubility limit. A sample is grown at 550°C with a $Si_2H_6$ flux corresponding to a carrier concentration of $1.5\times10^{19}$ $cm^{-3}$ at 600°C. The resulting carrier concentration at 550°C drops by an order of magnitude down to $1.7\times10^{18}$ $cm^{-3}$ as the cracking efficiency of $Si_2H_6$ decreases significantly. Higher fluxes are thus required at lower growth temperature, not achievable in our MOVPE system.

In the case of $H_2S$ (Fig. 3.12(a)), only the background doping is detected for the first 3 decades of dopant flux, followed by a sharp increase up to $2.5\times10^{18}$ cm$^{-3}$ and a sharp decrease as the InGaAs surface became rough. Those results indicate that sulfur incorporation into the crystal lattice is difficult to control and that the maximum achievable doping is rather limited. As a group-VI element, sulfur is not amphoteric and preferentially incorporated on group-V sites. Therefore, combining silicon and sulfur doping might promote Si incorporation on group-III sites and thus increase the active carrier density for the same density of Si atoms. Similar concept was proposed with Tin and Tellurium in [96]. A sample is grown at 600°C with a nominal Si doping of $1.9\times10^{19}$ cm$^{-3}$ and a sulfur doping of $2.5\times10^{18}$ cm$^{-3}$ resulting in an active carrier concentration of $2.93\times10^{19}$ cm$^{-3}$. The achieved carrier concentration is higher than the simple sum of expected Si and sulfur doping confirming that the presence of $H_2S$ promotes Si incorporation on group-III sites. It appears to be difficult to increase this doping level further as it results in undesirable roughening of the InGaAs surface.

With DETe and TESn for Te and Sn doping, high active carrier concentrations above $3\times10^{19}$ cm$^{-3}$ are successfully achieved but they appears to saturate at higher doping flux. Several samples are prepared with varying TESn doping fluxes and reduced growth temperatures of 550°C or 500°C (Fig. 3.12(b)). For each temperature, the active carrier concentration versus dopant flux presents the same trend: an increase up to a peak concentration and then a decrease associated with a degradation of the InGaAs morphology. Lowering the growth temperatures strongly increases the peak carrier concentration while it shifts to higher fluxes. A maximum electron concentration of $5.7\times10^{19}$ cm$^{-3}$ is reached at 500°C. The trend versus growth temperature is attributed to an increase of the solubility limit of Sn in InGaAs as the growth temperature reduces.

For integrated InGaAs n-MOSFETs presented in Chapter 4, the RSD module is either a 600°C Si-doped (as this is the first module which has been developed) or a 500°C Sn-doped InGaAs (for devices made after this development). Besides the simple improvement of contact and sheet resistances of S/D regions, the low temperature Sn-doped RSD module is highly beneficial for a reduced $D_{it}$ in GF MOSFETs (Chap. 4, section 4.3.2) as well as maintained performance of bottom silicided p-MOSFETs in a 3D monolithic CMOS integration scheme (Chap. 5, section 5.3).

### 3.3.2 Ni-InGaAs: Self-aligned silicide-like contacts

The formation of self-aligned Ni-InGaAs contacts (see Fig. 3.13) requires to deposit Ni on a clean InGaAs surface such that alloying reaction can occur, control the alloying depth

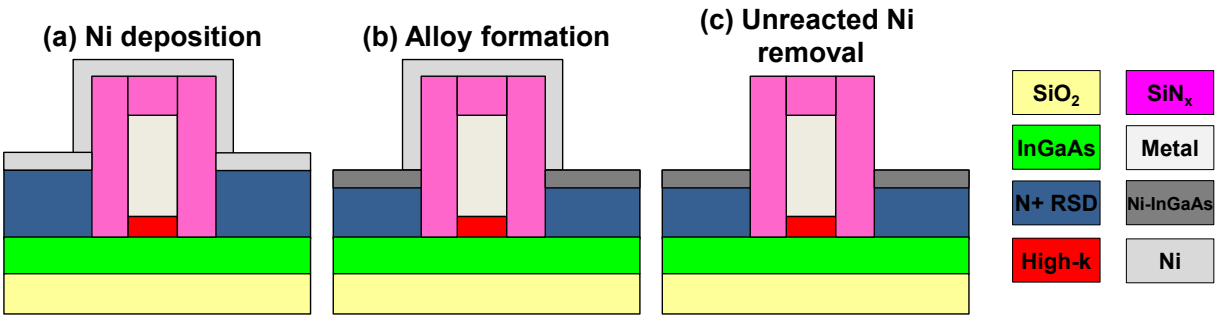



**Figure 3.13:** Schematic of InGaAs MOSFETs at various stage of the self-aligned Ni-InGaAs contact formation process: (a) after Ni deposition, (b) after alloy formation by annealing and (c) after selective wet etching of unreacted Ni.

and Ni lateral diffusion, and selectively etch the unreacted Ni from the formed Ni-InGaAs alloy, as proposed in [90]. The resulting self-aligned contact should be characterized for its sheet resistance and contact resistance to the RSD, and should have a high enough thermal stability to enable BEOL processing.

For that purpose, the following sections will present a study of the Ni-InGaAs process in terms of thermal budget and wet chemistries, electrical characterization through transfer length method (TLM) structures, physical characterization by secondary ion mass spectrometry (SIMS) and integration details into a MOSFET flow.

#### 3.3.2.1 Ni-InGaAs baseline process

Two types of samples are prepared: blanket samples used for characterization of sheet resistances, and TLM samples to extract the specific contact resistivity of Ni-InGaAs to $n^+$ RSD. 50 nm thick Si-doped (at $2\times10^{19}cm^{-3}$) $In_{0.53}Ga_{0.47}As$ layers are grown at 600°C on semi-insulating InP wafers and loaded in a sputtering system where the surface native oxide is removed by a 1 minute exposure to an argon plasma. Subsequently, 10 nm of Ni are deposited without breaking vacuum, either as a blanket film or as contact pads. A mesa-isolation step of the TLM structures is performed by wet etching of $In_{0.53}Ga_{0.47}As$ down to the InP wafer. The Ni-InGaAs alloy is formed by a vacuum anneal for 5 minutes at different temperatures ranging from 230°C to 500°C. SEM cross-sections revealed that with 10 nm of fully reacted Ni, a 25 nm thick Ni-InGaAs alloy is formed. Unreacted Ni is then selectively wet etched for 1 minute in diluted HCl (1:10 in water) at 70°C, or 1.5 minutes in diluted nitric acid ($HNO_3$) (1M in water) at room temperature, or 1 minute in a commercial sulfuric acid ($H_2SO_4$) based Ni etchant at 50°C stabilized to be selective to GaAs.

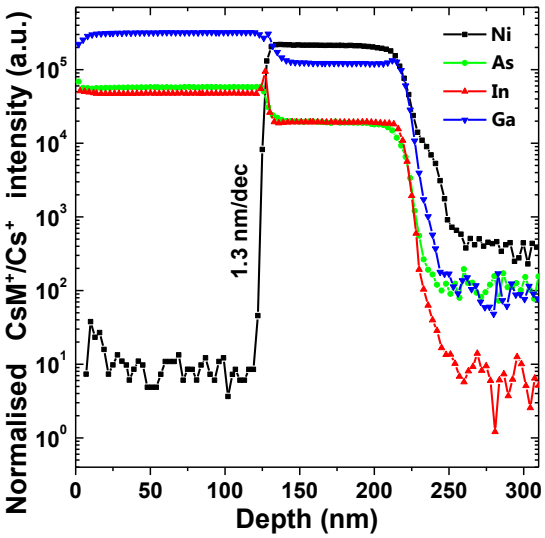



**Figure 3.14:** Back-side SIMS profile for 220 nm of $In_{0.53}Ga_{0.47}As$ on InP after deposition of 50 nm Ni, annealed at 350°C for 5 minutes.

Those samples are then characterized electrically. Results are presented in a following paragraph. Firstly, physical characterization by SIMS are shown to asses the alloying front uniformity and composition profile.

#### 3.3.2.2 Physical characterization

An additional sample is prepared in order to evaluate the composition profile in the Ni-InGaAs alloy by SIMS analysis. It consists of 220 nm of $In_{0.53}Ga_{0.47}As$ on InP grown by MOVPE, followed by sputtering deposition of 50 nm of Ni. This sample is annealed at 350°C for 5 minutes in vacuum to drive the alloy formation to completion. In order to avoid artificial tailing of the alloy/III-V interface because of beam-induced topography, a back-side SIMS preparation procedure is followed. The wafer is transferred to a carrier wafer by epoxy-bonding and subsequently thinned down to about 25 $\mu$m using a silicon-carbide grinding paper. The remaining InP substrate is wet etched in HCl-based chemistry which features a high InP etch rate (several $\mu$m per minutes) and a high selectivity to $In_{0.53}Ga_{0.47}As$.

The acquired back-side SIMS profile (Fig. 3.14) reveals the presence of a Ni-InGaAs quaternary alloy with constant composition over 90 nm. The Ni-profile shows the absence of any significant Ni diffusion in the underlying $In_{0.53}Ga_{0.47}As$ together with a very abrupt leading edge of 1.3 nm/decade indicating a highly uniform Ni-InGaAs thickness, as a result of a highly uniform alloying reaction. This is an important result as it confirms that the to-

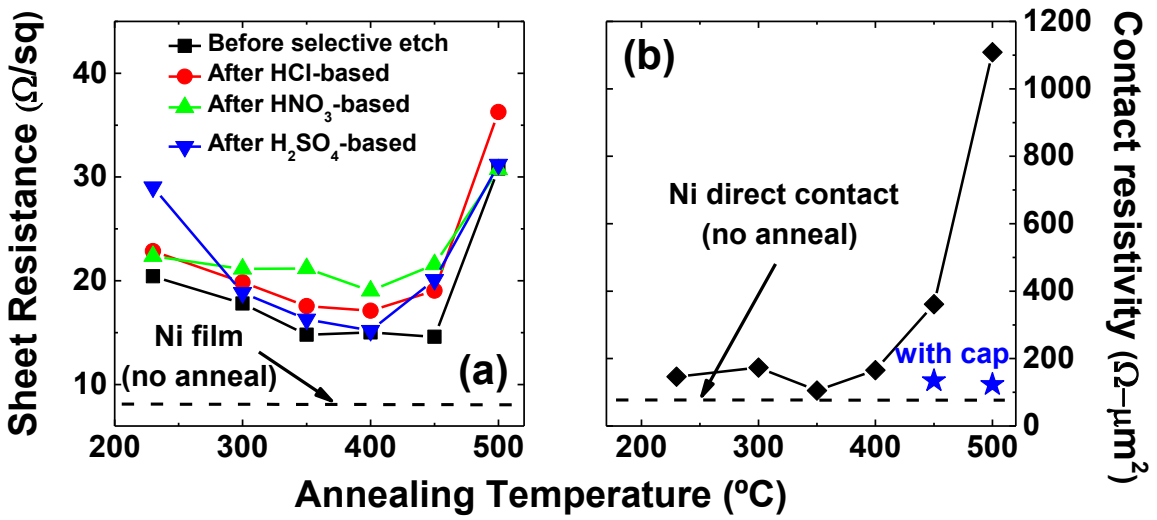



**Figure 3.15:** (a) Sheet resistance ($R_{sheet}$) of Ni-InGaAs alloy (with 10 nm Ni deposition) as a function of annealing temperature for 5 minutes in vacuum; before and after selective wet etching of unreacted metal. (b) Specific contact resistance ($\rho_C$) of Ni-InGaAs to RSD as a function of annealing temperature, extracted on TLM structures on samples with (blue stars) and without (black diamond-shaped dots) annealing $SiO_2$ cap.

tal alloy thickness can be accurately controlled down to the scaled thicknesses required for high-performance CMOS applications. Furthermore, back-side In-profile reveals the presence of an In-rich InGaAs (significantly above 53% of In) phase at the Ni-InGaAs/InGaAs interface. As high In-content InGaAs features a lower bandgap, this effect could contribute to reducing the Schottky barrier height (SBH) at the metal/semiconductor interface, which should improve the contact resistance [97].

#### 3.3.2.3 Electrial characterization

4-probes sheet resistance ($R_{sheet}$) measurements on the Ni-InGaAs alloy as a function of annealing temperature for various selective wet etching agents are reported in Fig. 3.15(a). Firstly, the as-deposited Ni film is characterized as a reference for unreacted Ni on InGaAs, showing a $R_{sheet}$ of 7.4 Ω/sq. Around 230°C, the Ni-InGaAs alloy starts to form leading to an increase in the $R_{sheet}$ to 20.4 Ω/sq. With raising temperatures up to 350°C, Ni is partially consumed leading to a progressive decrease of $R_{sheet}$ down to 14.8 Ω/sq. The formed phase is thermally stable between 350°C and 450°C with a constant $R_{sheet}$. At 500°C, $R_{sheet}$ starts to degrade rising to 30.8 Ω/sq while higher temperatures lead to sample failure attributed to III-V desorption in the absence of a capping layer. Comparing $R_{sheet}$ after etching the Ni in different solutions reveals that $HNO_3$-based etching agents leads to the worst selectivity as highlighted by the largest variation in $R_{sheet}$ before and

after etch. The $H_2SO_4$-based etching solution gives the best selectivity, as indicated by a low $R_{sheet}$ of 15.2 Ω/sq at 400°C, which is only twice more resistive than as-deposited Ni. This obtained sheet $R_{sheet}$ is notably better than reported in [90] (25 Ω/sq for 30 nm deposited Ni, corresponding to about 75 nm thick Ni-InGaAs), which is attributed to a significant reduction of the Ni-InGaAs degradation during selective etching of unreacted Ni thanks to the improved wet etch selectivity in the $H_2SO_4$-based solution.

The specific contact resistance ($\rho_C$) vs annealing temperature derived from TLM structures on the characterization wafer is shown in Fig. 3.15(b). A rather low $\rho_C$ of 86 $\Omega\mu m^2$ is measured before annealing on Ni direct contacts. After annealing, $\rho_C$ jumps to 146 $\Omega\mu m^2$ at 230°C and stays rather constant up to 400°C. At 450°C and above, $\rho_C$ largely increases up to 1108 $\Omega\mu m^2$ at 500°C in absence of capping layer, also attributed to thermal degradation of the III-V layer. Additional contact resistivity measurements are performed on samples where a 100 nm thick $SiO_2$ capping layer is deposited by PECVD before annealing (Fig. 3.15(b)), showing a $\rho_C$ in the range of 120-130 $\Omega\mu m^2$ for 450°C and 500°C respectively. This result tends to confirm that the degradation of the electrical properties of the Ni-InGaAs alloy above 400°C is linked to the thermal desorption of III-V materials, but not to a physical change of the material properties like a phase transition as for nickel silicide [98]. It should then be noted that with a capping layer, this nickel alloy shows a very stable $\rho_C$ of about 100-150 $\Omega\mu m^2$ over the whole range of tested temperatures up to 500°C making it suitable for CMOS standard BEOL processing. This later $\rho_C$ value is 2 orders of magnitude better than reported value in [90] (about $10^{-3}$ $\Omega cm^2$), probably owing to the more uniform alloying front which leads to indium pill-up at the alloy/InGaAs interface. Nevertheless, it is still two to three orders of magnitude higher than required for CMOS applications (1 $\Omega\mu m^2$ to 0.1 $\Omega\mu m^2$).

Further improvements are expected by increasing the $n^+$ doping to $5\times10^{19}$ $cm^{-3}$ or more (with Sn-based RSD) and by carefully adjusting InGaAs composition to minimize the SBH at the metal/semiconductor interface [97].

#### 3.3.2.4 Ni-InGaAs integration on MOSFETs

Figure 3.16(a) presents a SEM cross-section at the gate-edge region of gate-patterned test wafer. It shows the 50 nm thick RSD layer with its Ni-InGaAs alloyed metal contact self-aligned to the gate. The nickel alloy, formed at 350°C for 5 minutes, is very uniform far from the gate area and is 22 nm thick. Ni is found to be the diffusing species during the alloying process, which allows an accurate control of the resulting film thickness by adjusting the amount of deposited Ni. This phenomenon is also observed on Si and enables

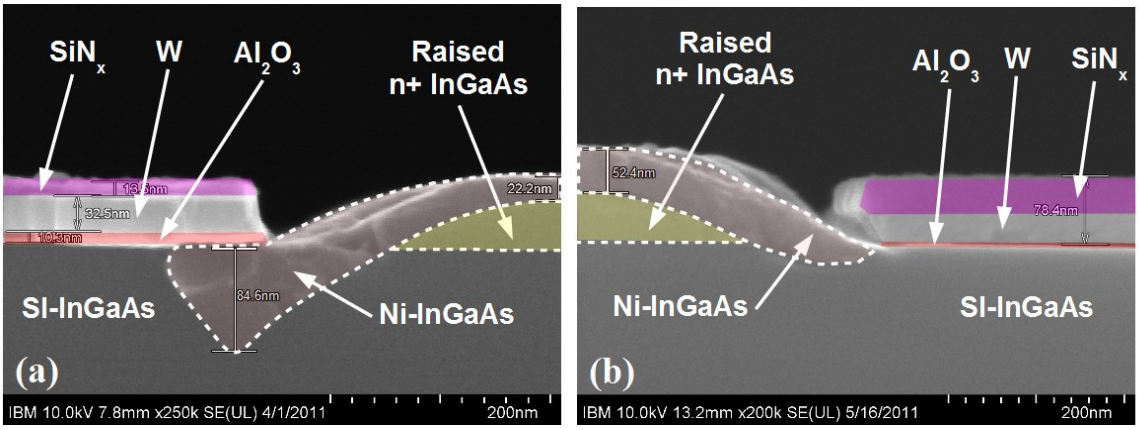



**Figure 3.16:** SEM cross-section of a gate-patterned wafer after RSD epitaxy, Ni-alloying and unreacted Ni removal; showing Ni-InGaAs alloy and RSD self-aligned to the gate: (a) 10 nm Ni on 50 nm RSD annealed at 350°C for 5 minutes, (b) 25 nm Ni on 100 nm RSD with migration-optimized double-step anneal process.

down scaling the alloyed contact thickness to CMOS requirements.

However, a severe increase of the alloy thickness (up to 85 nm) near the gate area is observed originating from Ni migration from the top of the gate to the S/D regions. This problem is solved by a two-step annealing in order to minimize Ni migration. Firstly, an annealing if performed at low temperature to complete Ni reaction with InGaAs while minimizing Ni diffusion on top of the gate. Secondly, the unreacted Ni is selectively etched. Finally, a second annealing step is performed at higher temperature to reach the optimum $R_{sheet}$-$\rho_C$ combination. Figure 3.16(b) presents a SEM cross-section in the gate-edge region after this two-steps anneal process which clearly demonstrates a uniform film thickness up to the gate-edge, without any Ni pile-up close to the gate. It should be noted that in this case, the RSD thickness is 100 nm and the Ni thickness is 25 nm, resulting is 50 nm of Ni-InGaAs alloy.

Self-aligned Ni-InGaAs contacts are successfully developed, can be integrated into MOSFETs and show promising sheet and contact resistance values with a good thermal stability. Nevertheless, the best specific contact resistivity obtained (105 $\Omega\mu m^2$) is still two to three orders of magnitude too high to enable the formation of S/D regions smaller than 50 nm for densely integrated CMOS circuits. Therefore, the next section will evaluate the use of direct metal contacts to RSD as it might be preferable if it provides a better $\rho_C$.

### 3.3.3 Direct metal contacts

Direct metal contacts were replaced by self-aligned silicided contacts in CMOS existing technologies. The self-alignment of the metal contact to the gate edge yielded a significant reduction of the series resistance as the silicide $R_{sheet}$ is much lower than that of highly doped Si. In modern CMOS technologies, silicided contacts are still used as they are the industry standard process although they might no longer be required. Indeed, the metal plug contacts are placed by lithography at only 20 nm or less from the gate edge meaning that most of the S/D resistance is governed by the metal/semiconductor contact resistance and the sheet resistance of the RSD to the channel, not anymore by the sheet resistance of the metal.

In the case of InGaAs, the choice between Ni-InGaAs or similar alloyed contacts versus direct metal contacts is still open as self-alignment is no longer a differentiating factor. The final choice will probably be based on the best resulting $\rho_C$ rather than on the possibility to achieve self-alignment. The purpose of this section is to benchmark direct metal contacts on $In_{0.53}Ga_{0.47}As$ RSD to Ni-InGaAs, in order to guide the final choice for integrated MOSFETs.

#### 3.3.3.1 Benchmarking of different metals

In theory, forming an ohmic contact requires to have metals with a work-function lower than the electron affinity of $In_{0.53}Ga_{0.47}As$ (4.5 eV [99]). A large spread exists in literature for metal work-functions due to the dependence on crystal lattice orientation, grain size or roughness. The obtained work function is therefore very dependent on the exact deposition process. Nevertheless, available metals which were reported to have work-functions lower than 4.5 eV [100], are selected. The metals investigated are: Al, V, Ti, Ta, Mo, W.

Fabricating contact test structures requires several levels of lithography and processing steps. This processing can change the surface chemistry of InGaAs, induce damages or introduce contaminating species. In order to probe the intrinsic specific contact resistivity between a metal and InGaAs, it is important to make sure that processing is restricted to an absolute minimum before the formation of the metal/semiconductor contact. Therefore, a dedicated process is proposed which starts by the deposition of the contact metal on InGaAs to form the critical interface - postponing all the rest of the processing to a later stage. Only a gentle surface clean is performed between the InGaAs epitaxy and the metal deposition. All transfer times in air are minimized. The process starts with the epitaxy of 100 nm Si-doped $In_{0.53}Ga_{0.47}As$ on an $In_{0.52}Al_{0.48}As$ buffer on semi-insulating InP wafers. The carrier concentration in InGaAs is measured to be $2\times10^{19}$ $cm^{-3}$. Upon

**Table 3.1:** $\rho_C$ obtained from TLM measurements for different metals on 100 nm thick Si-doped $In_{0.53}Ga_{0.47}As$ at $2\times10^{19}$ $cm^{-3}$.

| Metal | Specific contact resistivity ($\Omega\mu m^2$) |
|---|---|
| Mo | 7.9 ± 2.3 |
| W | 46.5 ± 1.7 |
| Al (*in-situ*) | 50.5 ± 6.3 |
| Ti | 65.9 ± 20.2 |
| V | 68.3 ± 2.1 |
| Al (*ex-situ*) | 124.6 ± 8.6 |
| Ta | 22546 ± 595 |

unloading the wafer from the MOVPE chamber, a gentle surface clean is performed (similar to reported in section 3.3.1) followed by the deposition of a 20 nm thick contact metal (Al, V, Ti, Ta, Mo or W). For Al, a sample is prepared with *in-situ* deposition of Al inside the III-V growth chamber in order to avoid any oxidation/damage of the surface during air transfer, and another one with *ex-situ* deposition as for other contact metals. Then, thick metal pads (400 nm) are deposited by lift-off to form the future electrical probe contacts. After lift-off, the blanket contact metal is etched using the thick metal pads as etch mask. Finally, InGaAs mesa are wet etched.

All the samples exhibit an ohmic behavior for the probed range of current (± 0.5 mA/$\mu$m). A systematic extraction of $R_{sheet}$, contact resistance ($R_C$) and $\rho_C$ is performed. The $\rho_C$ results are summarized in Table 3.1. Molybdenum yields the best results achieving a $\rho_C$ of 7.9 $\Omega\mu m^2$. Tungsten gives the second best result of 46.5 $\Omega\mu m^2$, close to aluminium (*in-situ*), vanadium and titanium. The results obtained with *in-situ* Al are not better than other refractory *ex-situ* metals. Tantalum and aluminium (*ex-situ*) yield poorer results due to their oxidation during the fabrication process.

For MOSFETs fabrication, Mo and W are the preferred choice because they yield the best $\rho_C$, they have a high thermal stability and are CMOS compatible. Compared to Ni-InGaAs, direct metal contacts offer a reduced process complexity as well as a 2 to 10-fold improvement in $\rho_C$. Therefore, most devices fabricated in Chapter 4 have direct metal contacts instead of self-aligned Ni-InGaAs alloyed contacts. Among direct metal contact options, it is decided to focus on W since this is the industry-standard metal contact for Si-based CMOS technology and simpler to integrate than Mo. It will be shown in Chapter 4 section 4.2.4 that a $\rho_C$ of 10 $\Omega\mu m^2$ could be obtained with W on integrated devices. Nevertheless, it is still at least an order of magnitude too high for CMOS requirements.

## 3.4 Conclusion and Outlook

The introduction of an a-Si interlayer between the HK layer and InGaAs channel enables the formation of MOS stacks without the formation of any InGaAs oxides, and an improved thermal stability up to 650°C. Scaled CET down to 12.7 Å are demonstrated on MOSCAPs and 13 Å on transistors. A high $\mu_{eff}$ up to 1270 $cm^2/V.s$ is achieved. Nevertheless, it will be shown in the next Chapter 4 section 4.2 that the extracted low $D_{it}$ numbers by the high-low frequency method are probably not valid and that direct HKMG gate stacks result in steeper SS.

The remote oxygen scavenging mechanism is explained and its applicability to InGaAs is proposed. CET scaling of 2 Å is achieved on gate stacks containing a-Si through the scavenging of the $SiO_2$ interlayer confirmed by XPS. On gate stacks having a direct HK/InGaAs interface, oxygen scavenging is shown to yield a large reduction in CET and $D_{it}$ for moderate temperatures below 450°C. Above this temperature, thermal desorption of InGaAs oxides and elements is restricting the applicability of the method.

Finally, an optimized PEALD gate stack is presented. It relies on the *in-situ* plasma cleaning of the InGaAs surface prior to HKMG deposition, the use of a TiN metal electrode for remote oxygen scavenging and an optimized $H_2$/Ar post-metalization anneal. A CET of 15.5 Å is obtained with a minimum $D_{it}$ of approximately $5\times10^{11}cm^{-2}.eV^{-1}$. In the future, further attention should be paid to the reliability of the MOS stacks on InGaAs as it currently appears to be one of the main limitation for CMOS applications.

The surface recovery and preparation prior to the formation of RSD is characterized by RHEED, AFM and XPS. Various RSD modules are developed at different temperatures and with different dopant species. Two modules are subsequently integrated in MOSFETs: high-temperature (600°C) Si-doped InGaAs with a doping of $2\times10^{19}cm^{-3}$, or low-temperature (500°C) Sn-doped InGaAs reaching a doping of $5.5\times10^{19}cm^{-3}$.

Self-aligned Ni-InGaAs alloyed contacts are obtained with an optimum formation temperature of 350°C to 450°C and a sulfuric-acid based wet etchant for the removal of unreacted Ni. It reaches a $\rho_C$ of 105 $\Omega\mu m^2$ stable up to 500°C provided that a $SiO_2$ capping layer is used during annealing. A dual-anneal process is proposed and successfully tested to control the lateral diffusion of the Ni-InGaAs alloy at the gate edge.

Finally, several CMOS compatible metals are evaluated as direct metal contacts to highly-doped InGaAs. Excellent $\rho_C$ values are obtained down to 7.9 $\Omega\mu m^2$ for Molybdenum contacts and 46.5 $\Omega\mu m^2$ for Tungsten contacts. Those results are notably better than for Ni-InGaAs alloyed contacts. A comparison of alloyed and direct metal contacts is carried out on transistors in Chapter 4 section 4.2.1.

Future work should focus on increasing even more the n-type doping in InGaAs RSD and improving the metal/semiconductor contact resistance as the currently obtained $\rho_C$ values are still an order of magnitude too high for CMOS applications whose metal contact size are expected to be approximately 30 nm wide.

All modules developed in this thesis are tested and benchmarked on devices. Some might finally not be the leading options for high performance devices (such as a-Si-based gate stacks or Ni-InGaAs contacts), but there were still presented as their development is part of the overall learning process.

# Chapter 4

# Devices: Self-aligned CMOS-compatible InGaAs MOSFETs

## 4.1 Introduction

This chapter describes the fabrication and characterization of CMOS-compatible self-aligned InGaAs MOSFETs. It reviews the evolution of the device architecture as new process modules are successfully developed and progressively introduced. The gate-first (GF) planar architecture is the simplest self-aligned device structure thus it serves as the main platform for the development of InGaAs MOSFETs and concentrates most of the device work (section 4.2). Transistors are fabricated on bulk InP as well as on insulator on Si, with an a-Si-based gate stack or direct HK/InGaAs interface, with or without Ni-InGaAs self-aligned metal contacts. Then, non-planar fin-based MOSFET (FinFET) are pursued to enable further performance improvement at scaled dimensions (section 4.3). Junction-less (JL) GF devices are used as a test vehicle for the development of InGaAs fins formation and fins cleaning prior to the MOS stack deposition. A replacement metal-gate (RMG) process is then established and compared to GF FinFETs. Finally, GF InGaAs FinFETs are fabricated on selectively grown InGaAs on Si and compared to their bonded InGaAs-OI counter part.

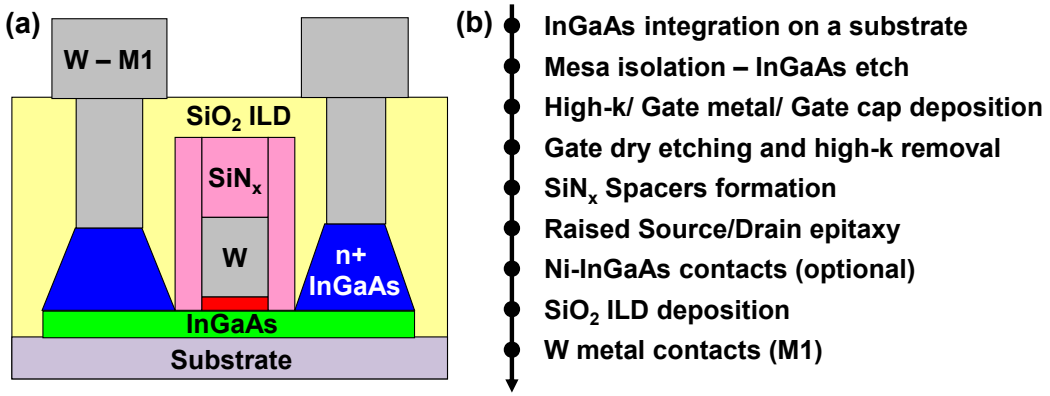



**Figure 4.1:** (a) Schematic of a self-aligned GF InGaAs MOSFET integrated on a generic substrate. (b) Corresponding baseline GF process flow.

## 4.2 Gate-first Planar MOSFETs

All GF MOSFETs presented in this chapter share the same baseline process flow, presented in Fig. 4.1. The InGaAs channel is integrated on a substrate which can either be an $In_{0.52}Al_{0.48}As$ buffer on InP for "bulk" MOSFETs, or a BOX on Si obtained by DWB (see section 2.2) or by selective epitaxy in empty cavities (see section 2.3). The InGaAs channel is etched to form active regions isolated from each other through the non-intentionally doped (NID) wider bandgap buffer or through the BOX layer. The channel surface is prepared for HKMG deposition of an a-Si-based stack or a direct HK/InGaAs stack followed by an optional TiN deposition. 30 nm of W are then deposited to complete the formation of the gate metal and provide a robust contact for future interconnects. The gate metal is capped by 30 nm of $SiN_x$ such that the top of the gate metal is not later exposed to the MOVPE of InGaAs RSD which would lead to non selective growth on W. The gate lines are defined by electron beam lithography (EBL) and dry etched down to the HK layer in a two step RIE process with $CHF_3$:$O_2$ and $SF_6$:$N_2$. The HK layer is removed in DHF followed by the PECVD or ALD deposition of a $SiN_x$ layer. An RIE step with a $CHF_3$:$O_2$ gas mixture is performed to etch back the $SiN_x$ layer and form the sidewall spacers.

The thickness of the $SiN_x$ layer is chosen to be 1.5 times thicker than the desired sidewall spacer thickness as a result of the RIE process. The achievable lower limit of spacer thickness is mostly defined by the ability to deposit a very conformal $SiN_x$ layer on a gate profile as vertical as possible. Owing to the intrinsic anisotropy of PECVD, it appeared to be impossible to scale the spacer thickness below 25 nm as, for layers thinner than 40 nm, no $SiN_x$ could deposit at the gate foot corner leading to shorts with

the S/D regions. The introduction on an ALD $SiN_x$ deposition module enables spacer thickness scaling down to 10 nm, limited by the gate profile which cannot be 90 degrees when formed in W. After spacer formation, the InGaAs surface in S/D regions is wet cleaned and highly doped $In_{0.53}Ga_{0.47}As$ RSD are grown (see section 3.3.1). Most devices are fabricated with Si-doped RSD grown at 600°C, some better optimized devices are also fabricated with Sn-doped RSD grown at 500°C.

Optionally, self-aligned Ni-InGaAs contacts can be formed as described in section 3.3.2. Ni-InGaAs contacts are used on devices where the formation of the metal electrodes for device testing are defined by optical lithography, thus being separated by 7.5 $\mu$m from the gate edge. For such devices, the contribution of the sheet resistance from the metal contact to the gate edge dominates compared to the metal/semiconductor contact resistance which motivates the use of Ni-InGaAs having much lower sheet resistance than RSDs. Finally, the devices are covered with 100 nm of $SiO_2$ acting as interlayer dielectric (ILD). Contact holes are dry etched in the $SiO_2$ ILD by RIE in a $CHF_3$:$O_2$ gas mixture down to the RSD or Ni-InGaAs. A wet cleaning is performed to remove native oxides and RIE damages in the contact regions, followed by the deposition of W acting as M1. The W layer is patterned by dry etching to form the final probing electrodes.

Figure 4.2 presents 3 types of GF devices which are fabricated and characterized: "bulk", "on-insulator" and "optimized on-insulator". Those architectures do not correspond to a design of experiment, but rather to the device architecture evolution followed during the course of this work. New modules are gradually introduced with the target to improve electrostatic integrity and external resistance: starting from devices on InP to develop the baseline process, then moving to on-insulator structures on Si for better electrostatics, finally on-insulator on Si with higher S/D doping and thinner spacers for better on-performance.

- Firstly, "bulk" devices (Fig. 4.2(a)) with a 10 nm thick $In_{0.53}Ga_{0.47}As$ channel on a NID $In_{0.52}Al_{0.48}As$ buffer on semi-insulating InP wafers are fabricated. They feature an a-Si-based gate stack (see Chapter 3, section 3.2.1), comprising 1 nm a-Si/ 1 nm $Al_2O_3$/ 2 nm $HfO_2$ with W as a gate metal. Spacers are formed by PECVD and are 25 nm thick. High temperature (600°C) Si-doped RSD are used with a doping level of $2\times10^{19}cm^{-3}$. Those devices have metal contacts defined by optical lithography, therefore some devices are fabricated with Ni-InGaAs contacts, some with direct metal contacts.

- Secondly, the same fabrication process is applied to realize "on-insulator" devices (Fig. 4.2(b)) on an InGaAs-OI substrate comprising a 10 nm thick $In_{0.53}Ga_{0.47}As$

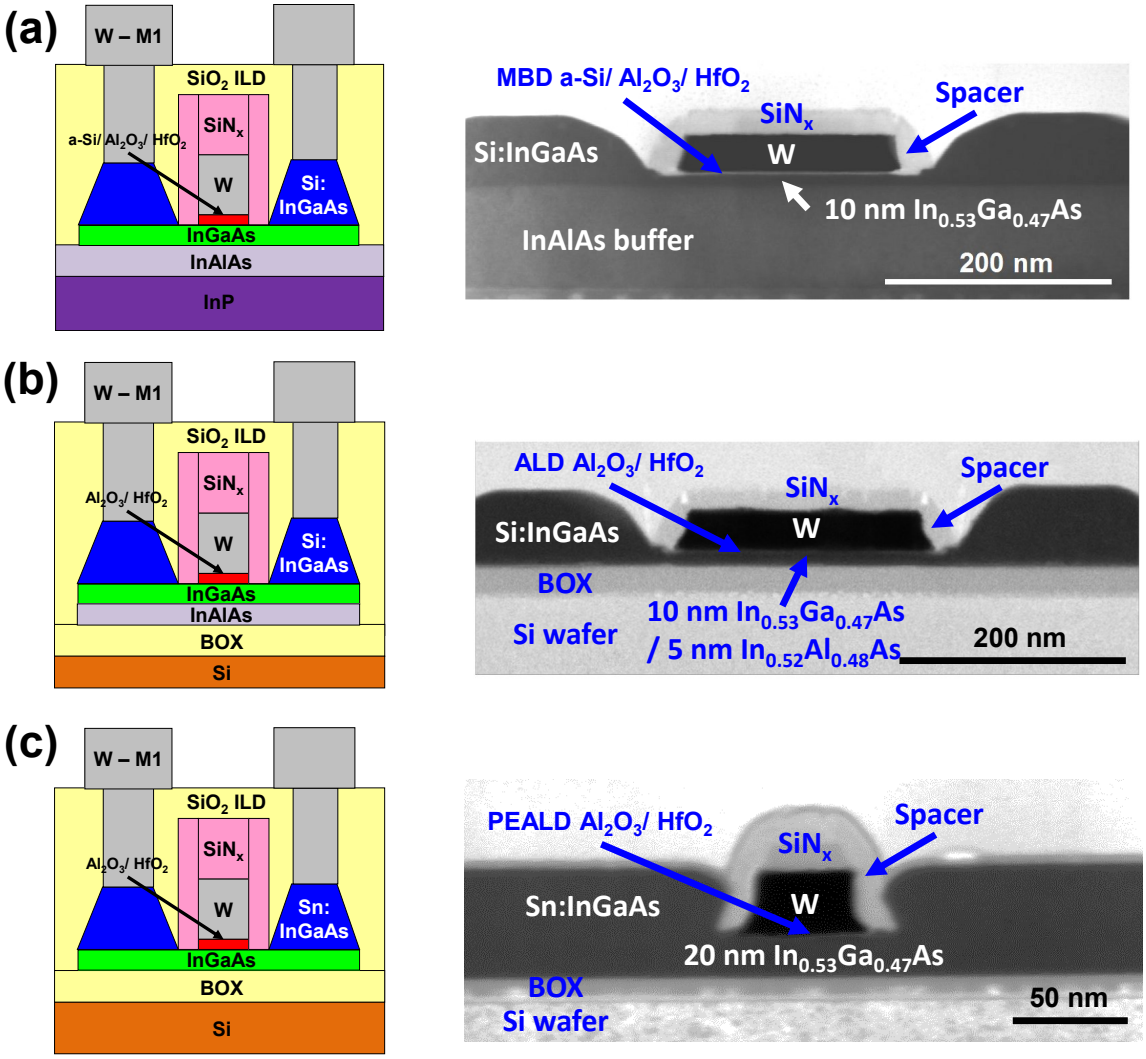



**Figure 4.2:** Schematic and TEM cross-sectional view of 3 types of self-aligned GF $In_{0.53}Ga_{0.47}As$ MOSFETs: (a) "bulk" devices with $t_{ch}$ = 10 nm, 1 nm a-Si/ 1 nm $Al_2O_3$/ 2 nm $HfO_2$ gate stack, Si-doped RSD, with or without Ni-InGaAs contacts ; (b) "on-insulator" devices with $t_{ch}$ = 10 nm on 5 nm InAlAs, 1 nm $Al_2O_3$/ 3 nm $HfO_2$ gate stack, Si-doped RSD ; (c) "optimized on-insulator" devices with $t_{ch}$ = 20 nm, 0.5 nm $Al_2O_3$/ 3 nm $HfO_2$ gate stack, Sn-doped RSD.

channel on a 5 nm thick $In_{0.52}Al_{0.48}As$ buffer on a 30 nm thick BOX on 4 inches Si wafers. The a-Si-based gate stack is not used here as the 4 inches InGaAs-OI substrates cannot be loaded in the UHV MBD chamber. Instead, a 1 nm $Al_2O_3$/ 3 nm $HfO_2$ thermal ALD bi-layer gate stack is used (see Chapter 3, section 3.2.2.2). Spacer thickness and RSD are nominally identical to the "bulk" devices. The metal contacts are defined by EBL so only direct metal contacts are used.

- Thirdly, "optimized on-insulator" devices (Fig. 4.2(c)) are fabricated with a 20 nm thick $In_{0.53}Ga_{0.47}As$ channel on a 25 nm BOX on Si substrates. A thicker channel is used as fin-based MOSFETs are fabricated on the same wafer (see section 4.3). The optimized PEALD gate stack is used with hydrogen-plasma clean and 0.5 nm $Al_2O_3$/ 2 nm $HfO_2$ (see Chapter 3, section 3.2.3). Scaled ALD-based $SiN_x$ spacers are formed with a final thickness around 10 nm. Low temperature (500°C) Sn-doped RSD are used with a nominal doping of $5\times10^{19}cm^{-3}$. Here as well, metal contacts are defined by EBL so direct metal contacts are used.

### 4.2.1 Impact of Ni-InGaAs contacts on "bulk" devices

As described in Chapter 3 section 3.3.2, self-aligned Ni-InGaAs mostly provide a lowered $R_{sheet}$ but an increased $\rho_C$ compared to direct metal contacts. The first set of devices fabricated in this work are long-channels "bulk" InGaAs MOSFETs defined by optical lithography. It implies that the metal contact to gate edge separation is 7.5 $\mu$m on each side of the gate. Thus, the current flows through 15 $\mu$m of S/D material which can contribute to a significant part of the total external resistance of the devices.

The total on-resistance extracted at $V_g = 1$ V in linear regime (drain-to-source voltage ($V_{ds}$) = 50 mV) is plotted against the gate length in Fig. 4.3. The results are normalized to 10 k$\Omega$.$\mu$m, meaning that an on-resistance of 1 on the graph corresponds to 10 k$\Omega$.$\mu$m. The linear extrapolation at zero gate length indicates the external resistance ($R_{ext}$) which comprises the metal to S/D contact resistance, the S/D sheet resistance from the contact to the gate edge and the resistance originating from the spacer region (from the doped RSD to the gate-controlled channel).

The extracted $R_{ext}$ for devices with and without self-aligned Ni-InGaAs contacts are 2.9 k$\Omega$.$\mu$m and 3.7 k$\Omega$.$\mu$m respectively. It corresponds to a 22% reduction of $R_{ext}$ with Ni-InGaAs contacts. $R_{sheet}$ of RSD and Ni-InGaAs layers extracted on TLM test structures are 70 $\Omega/\square$ and 15 $\Omega/\square$ respectively. As the contact are separated by 7.5 $\mu$m on each side of the gate, the total contribution of $R_{sheet}$ to $R_{ext}$ is approximately 115 $\Omega$.$\mu$m with Ni-InGaAs and 525 $\Omega$.$\mu$m for InGaAs RSD only. Assuming specific contact resistivities

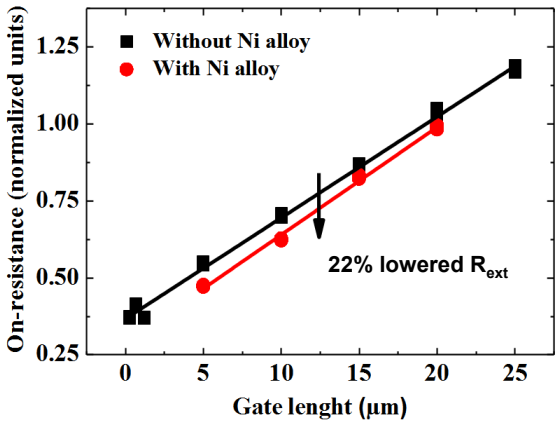



**Figure 4.3:** On-resistance versus gate length obtained on "bulk" MOSFETs with or without Ni-InGaAs contacts. The on-resistance is extracted from the drain current at $V_g$ = 1 V and $V_{ds}$ = 50 mV, normalized to 10 kΩ.$\mu$m.

of 100 Ω.$\mu$m$^2$ and 50 Ω.$\mu$m$^2$ for Ni-InGaAs to RSD contacts and W to RSD contacts respectively (see Chapter 3, section 3.3.2 and 3.3.3), $R_C$ is estimated to be 85 Ω.$\mu$m with Ni-InGaAs and 60 Ω.$\mu$m without Ni-InGaAs. Therefore, the total contribution of S/D regions to $R_{ext}$ is 380 Ω.$\mu$m with Ni-InGaAs contacts and 1170 Ω.$\mu$m with direct metal contacts. Those calculations are in good agreement with the measured $R_{ext}$ assuming that the resistance originating from the spacer region is 2.5 kΩ.$\mu$m.

The positive impact of self-aligned Ni-InGaAs contacts is clearly visible for devices with a large separation between metal contacts and gate edge. Nevertheless, it appears that most of $R_{ext}$ does not originate from the S/D regions, but rather from the region beneath the spacers. Indeed, as no implantation is used in the fabrication process, the region beneath spacers is nominally undoped. Hall measurements performed on several NID 10 nm thick InGaAs on 100 nm InAlAs on semi-insulating InP wafers reveal a background carrier density of 2-3×10$^{16}$cm$^{-3}$ with a Hall mobility of 4000-4500 cm$^2$/V.s. Assuming a 25 nm thick spacer on each side of the gate, it corresponds to a resistance comprised between 2.2 and 3.8 Ω.$\mu$m, in good agreement with the 2.5 kΩ.$\mu$m estimated above by deconvolution of the S/D contribution to $R_{ext}$.

As a consequence, all following devices are fabricated with EBL-defined direct metal contacts with a separation to the gate edge lower than 200 nm. In this way, the $R_C$ contribution of direct metal contacts and the $R_{sheet}$ contribution of RSD are limited to approximately 60 Ω.$\mu$m and 5 Ω.$\mu$m, respectively. Those values are negligible compared to the contribution of the spacer regions. Most of the on-performance improvement in the following sections originates from spacer thickness scaling.

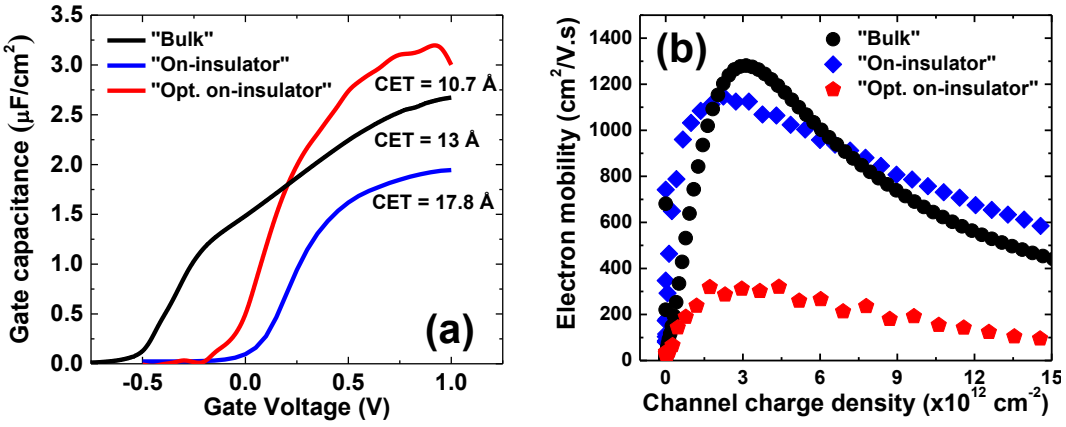



**Figure 4.4:** (a) Split C-V characteristics for the three GF device types measured at 1 MHz on MOSFETs with gate length ($L_G$) = 10 $\mu$m. (b) Effective mobility versus channel charge density for the corresponding devices.

### 4.2.2 Split C-V and Effective mobility

Long-channel MOSFETs ($L_G$ = 10 $\mu$m) are first characterized to extract the split C-V characteristics and effective mobility curves. "Bulk" devices have an a-Si-based gate stack while the two "on-insulator" devices have an $Al_2O_3$/ $HfO_2$ bi-layer. The extracted CET values are respectively 13 Å, 17.8 Å and 10.7 Å for "bulk", "on-insulator" and "optimized on-insulator" devices (Fig. 4.4(a)). The two bi-layer gate stacks present a very similar behavior besides their different scaling (in terms of $V_T$ or stretch-out). In contrast, the a-Si-based gate stack presents a much larger stretch-out which seem to indicate the presence of a higher density of traps. This finding is not in agreement with the $D_{it}$ values presented in Chapter 3 section 3.2.1. It might indicate the different nature of traps in the a-Si-based gate stack which have much shorter time constants than traps of a direct HK/ InGaAs interface, and thus seem to be largely responding to the *a.c* signal at 1 MHz. Therefore, the $D_{it}$ extraction with the high-low frequency method might be largely underestimated as it assumes that no traps respond at the high frequency. It is confirmed in the next paragraph through SS roll-off characteristics (section 4.2.3).

Figure 4.4(b) shows the effective mobility data. The extracted peak $\mu_{eff}$ values are respectively 1270 $cm^2$/V.s, 1150 $cm^2$/V.s and 320 $cm^2$/V.s for "bulk", "on-insulator" and "optimized on-insulator" devices. This is in agreement with the peak field effect mobility obtained from transconductance in linear regime. First comparing the two samples on-insulator having a bi-layer gate stack, a 3-fold reduction of $\mu_{eff}$ is observed. The large difference in CET could partly explain the reduction of $\mu_{eff}$. $HfO_2$ is known to lead to large mobility degradation on Si through remote Coulomb scattering as it gets close to

the channel by scaling the $SiO_2$ interlayer [82]. It is also shown in Chapter 3 section 3.2.1 that $HfO_2$ thickness has a strong influence on the electron mobility, attributed to remote Coulomb scattering. In this case, the CET scaling is due to 5 Å reduction of the $Al_2O_3$ layer and 1 nm reduction of the $HfO_2$ layer. The thinner $HfO_2$ improves the mobility as it reduces the number of scattering centers but the thinner $Al_2O_3$ reduces the distance between the channel and the $HfO_2$ layer which degrades the mobility through an increased interaction with scattering centers. The net resulting effect is an increased scattering rate as the Coulomb scattering potential is exponentially increasing with decreasing distances [101]. Similarly, $HfO_2$ is known to create a much stronger remote phonon scattering potential than $Al_2O_3$ [102] leading to mobility degradation as it gets closer the channel. Finally, another possible cause of mobility degradation is the different contribution from the back-side channel/BOX interface. "On-insulator" devices have a 5 nm $In_{0.52}Al_{0.48}As$ barrier layer between the InGaAs channel and the BOX which confines carriers away from the back-side BOX interface. "Optimized on-insulator" devices do not have such barrier layer and might suffer from extra remote Coulomb scattering originating from charged interface states or fixed charges at the InGaAs/BOX interface.

The "bulk" and "on-insulator" $\mu_{eff}$ present relatively similar peak values despite the different nature of their gate stacks. It is surprising to see that the MBD deposited a-Si-based gate stack which seems to contain a high density of fixed charges and interface traps (owing to its $V_T$ shift (Chapter 3 section 3.2.1) and strong stretch-out) results in such a high $\mu_{eff}$, compared to the ALD deposited bi-layer stack which appears to have a low density of fixed charges and a lower $D_{it}$. Furthermore, if the 1 MHz split C-V characteristic of the "bulk" device contains a strong response of interface traps, it implies that the effective mobility at low charge density could be underestimated. The 1 nm thick a-Si and $Al_2O_3$ layers could be confining the carriers further away from $HfO_2$ thus improving $\mu_{eff}$, although C-V measurements from Chapter 3 section 3.2.1 indicates that the accumulation layers most likely form at the a-Si/ $Al_2O_3$ interface. Lastly, the absence of BOX layer in "bulk" samples is another possible factor improving the mobility.

### 4.2.3 Short-channel devices and roll-off characteristics

Transfer characteristics of short-channel devices having a similar gate length ($L_G$ of 60 to 70 nm) are presented in Fig. 4.5 on the same scale, for a $V_{ds}$ of 50 mV and 0.5 V for all three device architectures. All devices reach an off-current below the 100nA/$\mu$m target for high-performance MOSFETs, not being limited by gate leakage at high drain bias but could rather be limited by gate-induced drain leakage (GIDL) [21, 103]. The on-current

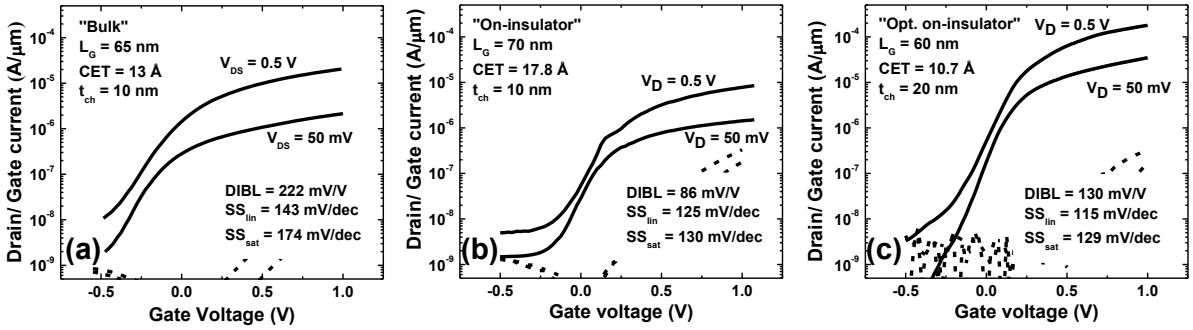



**Figure 4.5:** Drain (full lines) and Gate (dashed lines) currents versus gate voltage for GF short-channel MOSFETs of similar gate length for the three device architectures: (a) "bulk", (b) "on-insulator" and (c) "optimized on-insulator".

reduces from the "bulk" to "on-insulator" device as $R_{ext}$ increases by a factor 10 because of the full depletion of the ultra-thin-body NID InGaAs-OI beneath the spacers. Scaling spacers from 25 nm down to 10 nm leads to a large improvement in on-current on the "optimized on-insulator" devices, up to a maximum drain current of 180 $\mu$A/$\mu$m at $V_g$ = 1 V and $V_{ds} = 0.5$ V. As expected, clearly improved SS and DIBL are observed for devices on-insulator compared to bulk.

SS in saturation ($V_{ds} = 0.5$ V) and DIBL roll-off characteristics are presented in Fig. 4.6 for the three device architectures. "Bulk", "on-insulator" and "optimized on-insulator" long-channel devices exhibit SS of 107 mV/V, 98 mV/V and 95 mV/V respectively. The significantly lower SS for devices with a bi-layer gate stack than with the a-Si-based gate stack confirms the large difference in $D_{it}$ between the two stacks. Results from Chapter 3 section 3.2.1 are thus largely underestimated due to a strong response of traps in the 1 MHz C-V curve. Although a $D_{it}$ optimized PEALD bi-layer gate stack is used on the "optimized on-insulator" devices, the thermal budget of the RSD module brings it back to the same level as the thermal ALD bi-layer stack. In the next section 4.3.2, a RMG process is presented allowing to deposit the HK layer at the end of the process, after the high temperature steps, which yields a significant improvement in $D_{it}$.

SS dependence on gate length is mostly dominated by $D_{it}$ leading to a similar roll-off behavior for the two types of devices on insulator and a degraded roll-off for "bulk" devices. In contrast, DIBL dependence on gate length is mostly influenced by electrostatics leading to a clear improvement for devices on insulator compared to "bulk". The "optimized on-insulator" devices have slightly worse DIBL at short channel lengths probably due to the thicker channel (10 nm vs 20 nm). "Bulk" devices with better roll-off behavior are obtained by introducing a $2\times10^{17}$cm$^{-3}$ p-type doping in the InAlAs buffer compared to

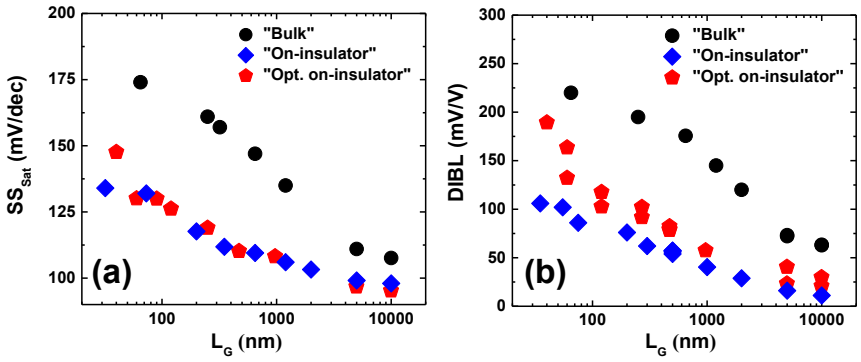



**Figure 4.6:** (a) SS at $V_{ds}$ = 0.5 V and (b) DIBL versus $L_G$ for "bulk", "on-insulator" and "optimized on-insulator" devices.

the 2-3×$10^{16}$cm$^{-3}$ n-type doping obtained for NID layers (not shown). This p-type doping in the buffer yields depletion of carrier beneath spacers resulting in a very large $R_{ext}$. It is not a viable solution in absence of doped extensions beneath the spacers.

### 4.2.4 Tight-pitch InGaAs MOSFETs

Electrical characterization of resulting direct W metal contacts to RSD is performed with TLM structures fabricated on-chip along with the "optimized on-insulator" MOSFETs, having contact length ($L_C$) varying from 50 nm to 5 $\mu$m. Total resistance versus contact separation curves are obtained and fitted to extract the corresponding $R_{sheet}$, $R_C$ and transfer length ($L_t$) as a function of $L_C$. Those results are shown in Fig. 4.7. For all $L_C$, a RSD $R_{sheet}$ of 124 $\Omega/\square$ is consistently obtained. It is low enough such that the $R_{sheet}$ contribution to $R_{ext}$ can be neglected. $R_C$ is measured to be comprised between 25 $\Omega.\mu$m and 40 $\Omega.\mu$m for all $L_C$ larger than 300 nm and then rises up to 200 $\Omega.\mu$m for 50 nm long contacts. Indeed, the extracted $L_t$ from TLM structures having $L_C$ above 1 $\mu$m indicates a transfer length of 275 nm which explains the increased $R_C$ as the contact length gets below the transfer length. Finally, a resulting $\rho_C$ of 10 $\Omega.\mu$m$^2$ is extracted. It is notably better than previous results obtained on direct contact test samples in Chapter 3 section 3.3.3, pointing to the improved doping level of RSD and robustness of the developed full-scale MOSFETs process.

Tight-pitch GF MOSFETs are fabricated on the "optimized on-insulator" wafer as shown in Fig. 4.8(a). The smallest devices have a gate length of 30 nm with 10 nm spacers on each side, contact holes of 50 nm and a contact pitch of 120 nm. It leaves only 10 nm alignment tolerance on each side of the gate which is the most aggressive design realized on an InGaAs MOSFET. It is only possible thanks to the use of a fully

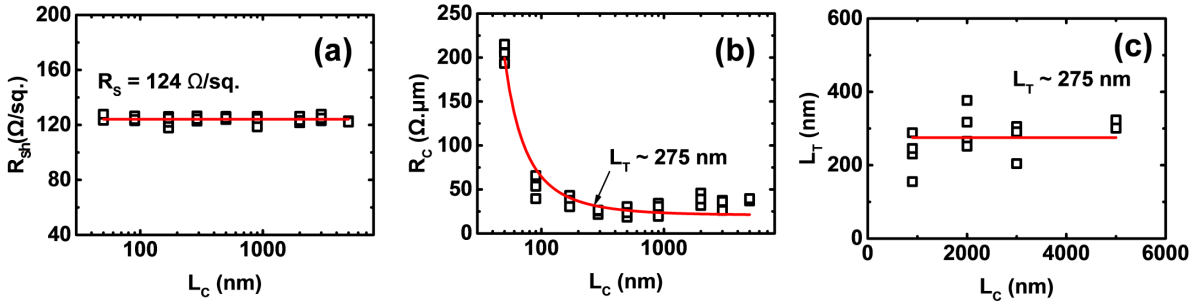



**Figure 4.7:** (a) $R_{sheet}$, (b) $R_C$ and $L_t$ versus contact size $L_C$ extracted from TLM structures of different contact size and spacing.

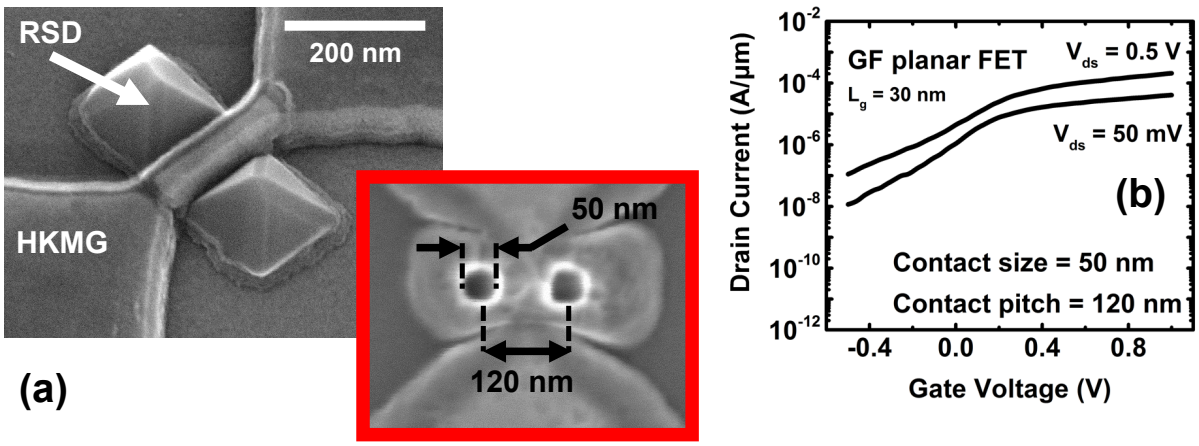



**Figure 4.8:** (a) Tilted and top view SEM of a tight-pitch "optimized on-insulator" GF MOSFET featuring a gate length of 30 nm, contact size of 50 nm and contact pitch of 120 nm. (b) Corresponding transfer characteristics of the device.

self-aligned device architecture and of well optimized fabrication processes. The resulting transfer characteristics highlight a properly operating device with a high on-current of 215 $\mu$A/$\mu$m at $V_g = 1$ V and $V_{ds} = 0.5$ V. This is actually higher than the device presented in Fig. 4.5(c) despites the scaled 50 nm contacts. In fact, although the resulting $R_C$ is around 200 $\Omega.\mu$m per contact, it is still a fraction of the total on-resistance of 2.3 k$\Omega.\mu$m. Therefore small contacts are not yet a problem on those devices as their $R_{ext}$ is still dominated by the region beneath spacers, but $\rho_C$ still needs to be reduced by at least one order of magnitude to match the targeted metrics for high-performance CMOS circuits. SS and DIBL are degraded compared to Fig. 4.5(c) owing to the twice smaller gate length.

## 4.3 Non-planar MOSFETs

In the previous section 4.2, all the required process modules to fabricate self-aligned InGaAs MOSFETs are integrated and tested on the simplest device architecture: GF planar devices. Those developments led to selection of best process modules and converged to the "optimized on-insulator" device architecture making use of PEALD gate stack with an *in-situ* clean of the InGaAs surface, scaled ALD-based $SiN_x$ spacers for improved $R_{ext}$, low-temperature Sn-doped RSD for higher doping level in S/D regions and finally, direct W metal contacts to RSD.

Further developments can be made to reduce the high resulting $D_{it}$ after RSD and to improve on the poor short-channel SS and DIBL of planar devices. For that purpose, two major changes in the fabrication process are proposed and developed in this section.

Firstly, a transition from planar MOSFETs to FinFETs is made to improve electrostatic control on the channel. It requires the development of a high-resolution low-damage InGaAs dry etch process, and a proper surface cleaning post-etch prior to the HK deposition. Ideally, the resulting $D_{it}$ or long-channel SS should be identical on planar or fin-based MOSFETs. To develop this process, junction-less (JL) devices are used as a short-loop test vehicle. They have a doped channel meaning that direct metal contacts to the channel can be made in S/D regions. It eliminates the need for spacers and RSD but still allows to benchmark the MOS interface quality. These results are presented in section 4.3.1.

Secondly, a transition from GF devices to RMG devices is proposed. The concept of RMG devices is to complete the fabrication of MOSFETs with a dummy gate and a dummy HK. Once the process is finished, the dummy gate and dummy HK are removed and replaced with final optimized HKMG stack. In this way, the MOS interface does not see the high thermal budget from the RSD module which implies that the low $D_{it}$ levels reported in Chapter 3 section 3.2.3 can be obtained on MOSFETs with a full-scale process. Such process is developed, characterized and compared to GF devices in section 4.3.2.

Finally, a transition from InGaAs-OI channels obtained by DWB to selectively grown InGaAs is pursued. DWB is an ideal platform for device development as it offers a perfect crystal quality if InP donor wafers are used, and it is relatively simple to prepare. Although it is possible to fabricate large-scale InGaAs-OI wafers for industrial needs (see Chapter 2 section 2.2.4), the possibility to selectively grow InGaAs, directly from the Si substrate where it is needed, is very appealing for industrial applications and needs to be benchmarked. For that purpose, GF FinFET are fabricated on CELO grown InGaAs as described in Chapter 2 section 2.3. These results are presented in section 4.3.3.

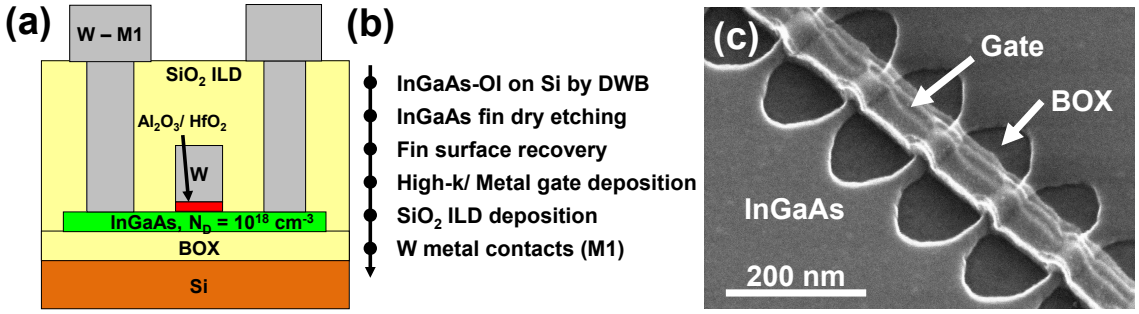



**Figure 4.9:** (a) Schematic of a JL InGaAs MOSFET on insulator on Si. (b) Corresponding JL process flow. (c) Tilted SEM image of a JL device after gate patterning on InGaAs fins.

### 4.3.1 Junction-less FinFETs

Recently, the multigate JL MOSFET using SOI has attracted significant attention due to its simplified fabrication process and excellent short-channel performance [104, 105]. For high drive current, a multigate JL device requires a high channel doping along with a short channel length, while for good electrostatic integrity a small fin width $W_{fin}$, low $D_{it}$ and a small EOT are required.

JL devices have a normally-on channel thanks to the high channel doping, which gets fully depleted by the gate in off-state as long as the body thickness is small enough. Outside of the gate region, the channel material remains very conductive and ensures a reasonably low $R_{ext}$. Direct metal contacts can be made to the S/D regions without any need for implantation or RSD. Therefore, it results in a device architecture which is simple to fabricate while being very sensitive to the good electrostatic control of the gate over the channel: an ideal candidate for the development of low $D_{it}$ gate stack on fins.

#### 4.3.1.1 Junction-less fabrication

Schematic of the targeted JL devices and corresponding process flow are presented in Fig. 4.9(a) and (b). JL devices are fabricated on a n-type $In_{0.53}Ga_{0.47}As$ on $Al_2O_3$ BOX on Si wafers, obtained by DWB. The n-$In_{0.53}Ga_{0.47}As$ layer is 20 nm thick and Si-doped to $1\times10^{18}cm^{-3}$. Firstly, InGaAs fins are formed by EBL and dry etching through a $SiN_x$ hard mask, which is removed after formation of the fins. Dry etching of InGaAs is achieved in an inductively-coupled plasma (ICP) RIE reactor by a cyclic plasma etching process. It results in a smooth low-damage etching of InGaAs, with $W_{fin}$ varying from 50 nm to 200 nm. The $SiN_x$ hardmask is removed by RIE and a pristine surface is recovered by wet etching 3 nm of InGaAs using a digital wet etch process. Firstly, the fins are exposed to an oxidant to form a self-limiting chemical oxide on the InGaAs surface, which is removed

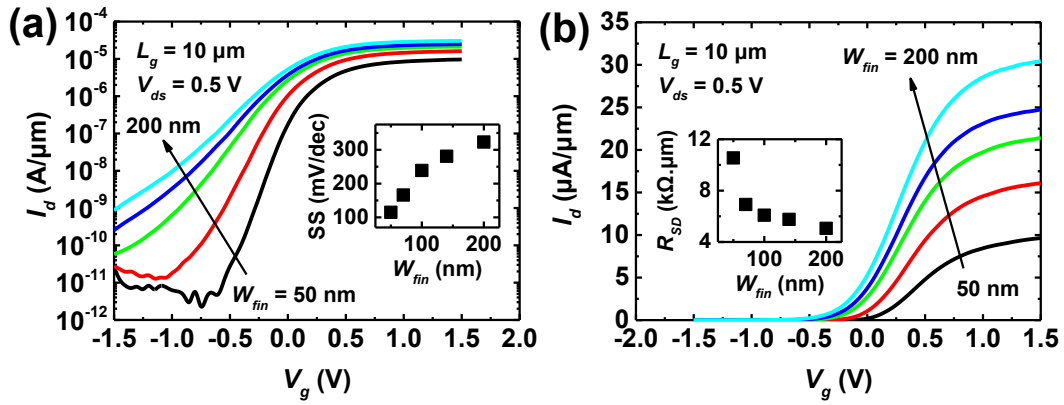



**Figure 4.10:** Transfer characteristics measured at $V_{ds}$ = 0.5 V, on devices featuring a $L_G$ of 10 $\mu$m, $H_{fin}$ = 20 nm and $W_{fin}$ ranging from 50 to 200 nm. Plotted in (a) log scale with SS vs $W_{fin}$ in inset and (b) linear scale with source and drain series resistance ($R_{SD}$) vs $W_{fin}$ in inset.

in a second step, selectively to the InGaAs crystal. Each cycle results in the removal of 1 nm of InGaAs. The PEALD gate stack is then deposited. Only 3.5 nm $Al_2O_3$ is used, no $HfO_2$, to simplify the HK removal in S/D regions. The W gate is deposited by sputtering. Gates of 100 nm to 10 $\mu$m length are formed by EBL and RIE. A tilted SEM image after gate patterning is presented in Fig. 4.9(c). The devices are encapsulated in a $SiO_2$ ILD deposited by PECVD prior to the formation of the W source and drain (S/D) contacts. The gate-to-source and gate-to-drain separations (main source of $R_{ext}$ in JL devices) are 150 nm.

#### 4.3.1.2 Electrical characterization: Impact of $W_{fin}$ and $H_2$/Ar anneal

Figure 4.10(a) and (b) show the impact of $W_{fin}$ on the transfer characteristics plotted in log and linear scales, respectively. A large on/off ratio of over 6 decades is achieved for $W_{fin}$ = 50 nm and degrades through an increase of SS for wider fins as expected with JL devices. From the inset of Fig. 4.10(a), it is clear that the gate control over the channel improves with the scaling of $W_{fin}$, as the SS reduces from 323 mV/dec at $W_{fin}$ = 200 nm to 108 mV/dec at $W_{fin}$ = 50 nm. However, a degradation of the drive current with $W_{fin}$ scaling is also observed due to an increase in source and drain series resistance ($R_{SD}$), which raises from 5 kΩ.$\mu$m at $W_{fin}$ = 200 nm to 10.5 kΩ.$\mu$m at $W_{fin}$ = 50 nm (inset Fig. 4.10(b)). Those results point to the usual compromise of JL devices where a smaller body is required to improve subthreshold characteristics, while scaling the body size largely increases the series resistance.

The negative or close to zero $V_T$ and the high minimum SS of 108 mV/V indicates

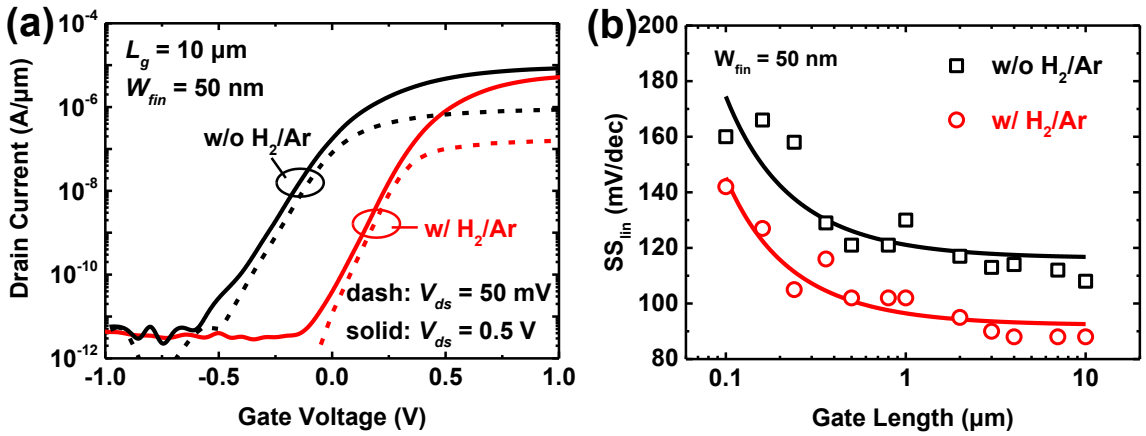



**Figure 4.11:** (a) Transfer characteristics measured at $V_{ds}$ of 50 mV and 0.5 V on long-channel (10 $\mu$m) tri-gate InGaAs-OI JL MOSFETs before and after $H_2$/Ar anneal. (b) SS at $V_{ds}$ = 50 mV versus $L_G$ roll-off characteristic before and after $H_2$/Ar anneal.

the presence of a high density of fixed charges and $D_{it}$. From Chapter 3 section 3.2.3, it appears that an annealing step in $H_2$/Ar is very efficient in reducing fixed charges and $D_{it}$. Figure 4.11(a) compares the transfer characteristics before and after $H_2$/Ar anneal in a long-channel ($L_G$ = 10 $\mu$m) device. A strong $V_T$ shift from -0.1 V to 0.25 V ($\Delta V_t$ = 0.35 V) following $H_2$/Ar is observed. The SS also reduces by about 20 mV/dec across all $L_G$ following $H_2$/Ar anneal, as reported in Fig. 4.11(b). For $L_G$ over 3 $\mu$m, a SS value of 88 mV/dec is obtained corresponding to an integrated $D_{it}$ of $4\times10^{12}$cm$^{-2}$eV$^{-1}$, given the measured CET of 29 Å. If the CET would be scaled down to sub 15 Å with the same interface quality ($D_{it}$), very competitive SS below 75 mV/dec would be expected which would correspond to a substantial improvement compared to devices presented in section 4.2. It points to the fact that the InGaAs etched surface on the sides of fins seem to be properly cleaned and have a low $D_{it}$ as best electrostatics are obtained for smallest fin widths where the side surfaces are becoming predominant to overall transport and electrostatics.

Devices with excellent subthreshold characteristics and high on-current can be achieved if this gate stack process on fins can be preserved with a low thermal budget, and combined with highly doped RSD to overcome the $R_{SD}$ limitation of JL devices. This is the purpose of the next section 4.3.2 which introduces the RMG process.

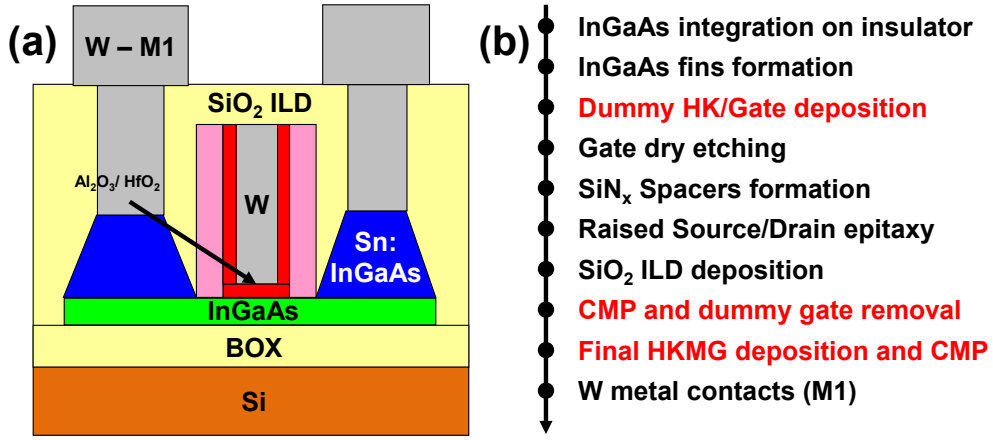



**Figure 4.12:** (a) Schematic of a self-aligned RMG InGaAs-OI MOSFET and (b) corresponding baseline RMG process flow. Highlighted in red are the major steps which differ from the baseline GF process shown in Fig. 4.1.

### 4.3.2 Replacement-gate FinFETs on Silicon

In today's modern industrial offering of CMOS technologies at advanced nodes, two major routes co-exist for the integration of the HKMG stack [106]: GF and RMG. In the GF scheme, the HK layer is present during the high temperature steps of the formation of S/D regions. Such high thermal budget can lead to interlayer regrowth limiting CET scaling as well as undesirable $V_T$ shifts. In the RMG scheme, a dummy-gate is used during the fabrication of the high temperature S/D regions, later removed and replaced by the final HKMG stack. In this way, the HK layer does not see the high thermal budget so that interfacial layer regrowth is minimized enabling very aggressive CET scaling, and provides an accurate control of $V_T$. The main drawback of RMG is a largely increased process complexity involving several very critical oxide and metal CMP steps.

For Si technology, numerous solutions were found to address the above mentioned challenges such that there is finally no clear benefit for one integration scheme over the other one [78, 107], resulting in both offerings on the market [108, 109]. For an InGaAs-based CMOS technology, it can be expected that RMG will lead to a significant performance improvement over GF. Indeed, it was shown in Chapter 3 section 3.2.2.2 and in sections 4.3.1 and 4.2 of this chapter that the thermal stability of the MOS stack is very limited.

This section presents results on the development of CMOS-compatible self-aligned InGaAs FinFETs featuring a RMG process and achieving significantly improved performance over previously discussed devices.

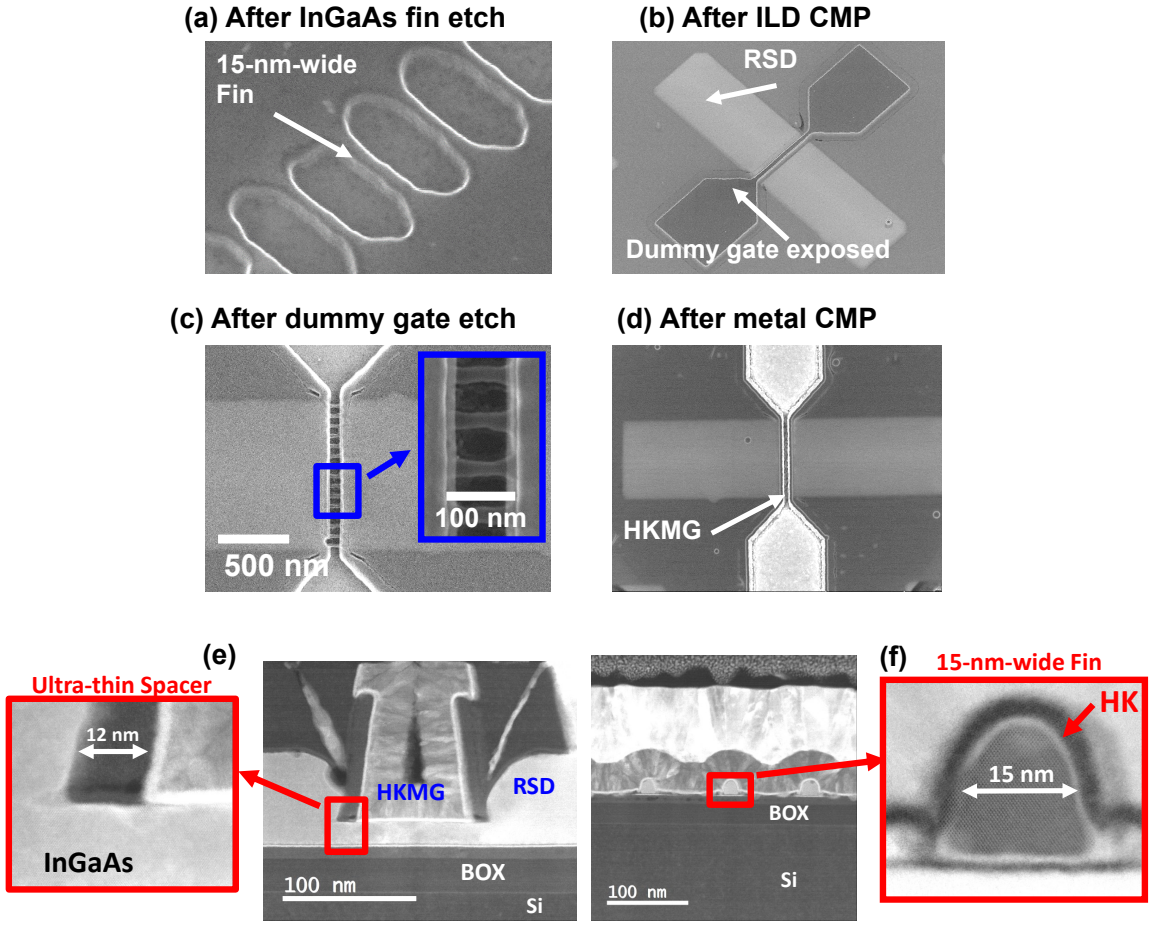



**Figure 4.13:** (a, b, c, d) SEM views taken at different critical stages of the RMG process: (a) after InGaAs fin patterning, (b) after $SiO_2$ ILD CMP exposing the top of the dummy gates, (c) after removal of the dummy gate and dummy HK, (d) after final HKMG deposition, W fill and metal CMP. (e, f) Cross sectionnal TEM image of a RMG InGaAs-OI MOSFET taken (e) across and (f) along the gate. Side insets show the scaled 12 nm thick $SiN_x$ spacers and 15 nm wide InGaAs fins.

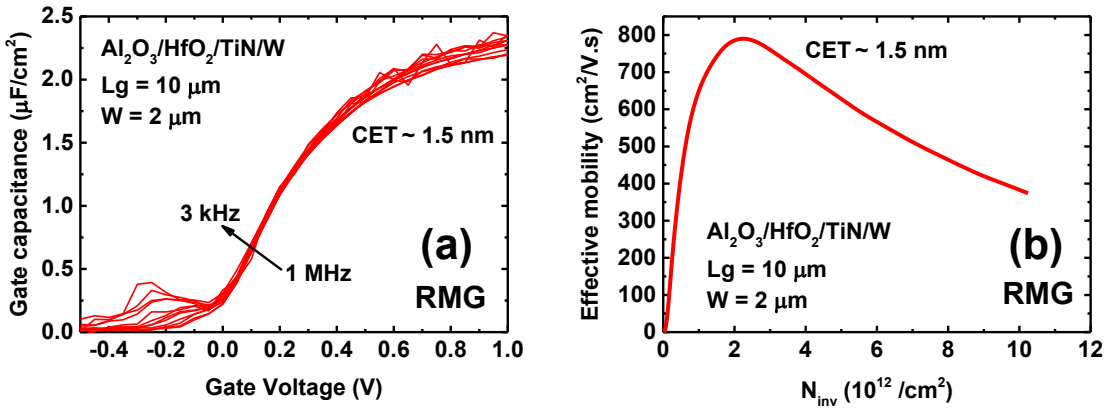



**Figure 4.14:** (a) Split C-V characteristics for a planar RMG MOSFET measured from 1 MHz down to 3 kHz. (b) Effective mobility versus channel charge density for the corresponding devices.

#### 4.3.2.1 RMG integration flow

The CMOS-compatible RMG fabrication flow and schematic of InGaAs-OI FinFETs are presented in Fig. 4.12. SEM and TEM images are shown in Fig. 4.13. It follows the "optimized on-insulator" GF process flow from section 4.2 with some modifications highlighted in red in Fig. 4.12(b). The InGaAs-OI structure is obtained by DWB as described in Chapter 2 section 2.2. The $In_{0.53}Ga_{0.47}As$ channel thickness is 20 nm, and BOX thickness is 25 nm $SiO_2$, 10 nm $Al_2O_3$ and 2 nm of PEALD HK stack. Devices with $W_{fin}$ scaled down to 15 nm are obtained (Fig. 4.13(a,f)) by EBL and a combination of dry etching and controlled wet etching (as discussed in section 4.3.1). Following dummy gate deposition and patterning, 12-nm-thick $SiN_x$ spacers are formed by ALD and RIE dry etching (Fig. 4.13(e)). Low temperature (500°C) Sn-doped 50 nm thick RSD are formed by selective MOVPE regrowth. A 250 nm thick $SiO_2$ ILD is deposited by PECVD and planarized using a controlled CMP process to open the dummy gate (Fig. 4.13(b)). After dummy gate removal (Fig. 4.13(c)), the final optimized PEALD HKMG stack is deposited, featuring a scaled CET of 15 Å. The HKMG is immediately capped with a 300 nm thick W layer. The W layer is planarized by CMP (Fig. 4.13(d,f)) prior to $SiO_2$ encapsulation and M1 metal contacts formation. A $H_2$/Ar anneal is performed for HKMG optimization in terms of density of $D_{it}$ and density of fixed charges.

#### 4.3.2.2 Split C-V and Effective Mobility

For the split C-V characterization and $\mu_{eff}$ extraction, planar MOSFETs are used as it is not possible with this process to fabricate a large number of fins in parallel which are

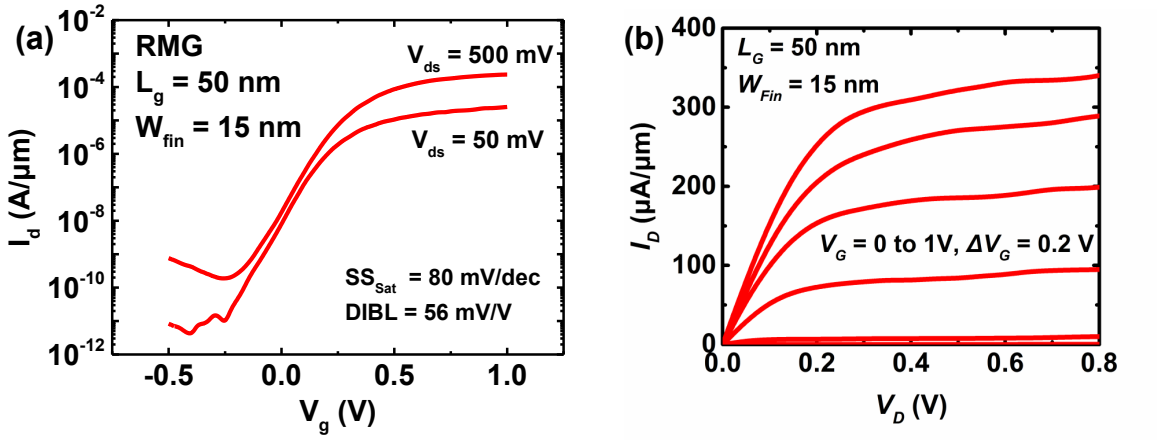



**Figure 4.15:** (a) Transfer and (b) characteristic of an InGaAs RMG FinFET featuring $L_G = 50$ nm, $W_{fin} = 15$ nm and $H_{fin} = 20$ nm.

long enough to provide a measurable C-V response. The multi-frequency split C-V of a device with $L_G = 10$ $\mu$m and W = 2 $\mu$m is shown in Fig. 4.14(a). Frequencies below 3 kHz are not shown as the signal is too noisy owing to the too small probed gate area. A CET of 15 Å is observed together with a very small frequency dispersion in the transition region from depletion ($V_g = 0$ V) to accumulation ($V_g = 0.5$ V) indicating a low $D_{it}$ below the conduction band edge, where the device operates. A larger frequency response is observed in depletion with a peak at $V_g$ = -0.3 V, very similar to what is reported on MOS capacitors in Chapter 3 section 3.2.3. It demonstrates that the full-scale self-aligned RMG MOSFET process is properly optimized as it yields comparable interface quality and capacitance scaling as simple test MOSCAPs. The extracted $\mu_{eff}$ peaks at 790 cm$^2$/V.s is significantly higher than in corresponding GF devices (see Fig. 4.4(b)) which can be a consequence of the higher CET and lower $D_{it}$. This peak $\mu_{eff}$ value might not be representative of the electron mobility in narrow fins but is a good indication of the improvements obtained with the RMG process over the GF process.

#### 4.3.2.3 Short-channel devices, roll-off characteristics, on-current benchmark

Transfer and output characteristics are obtained on an InGaAs-OI FinFET featuring a $L_G$ of 50 nm and $W_{fin}$ of 15 nm. The device reaches an off-current of 1 nA/$\mu$m and 5.5 decades of on/off ratio. It features a nearly ideal $V_T$ in saturation of approximately 0.25 V along with an ON-resistance of 568 $\Omega.\mu$m and a peak transconductance in saturation of 615 $\mu$S/$\mu$m. Excellent subthreshold performance is obtained with an SS in saturation (at $V_{ds} = 0.5$ V) of 80 mV/dec over 3 decades of drain current and a DIBL of 56 mV/V.

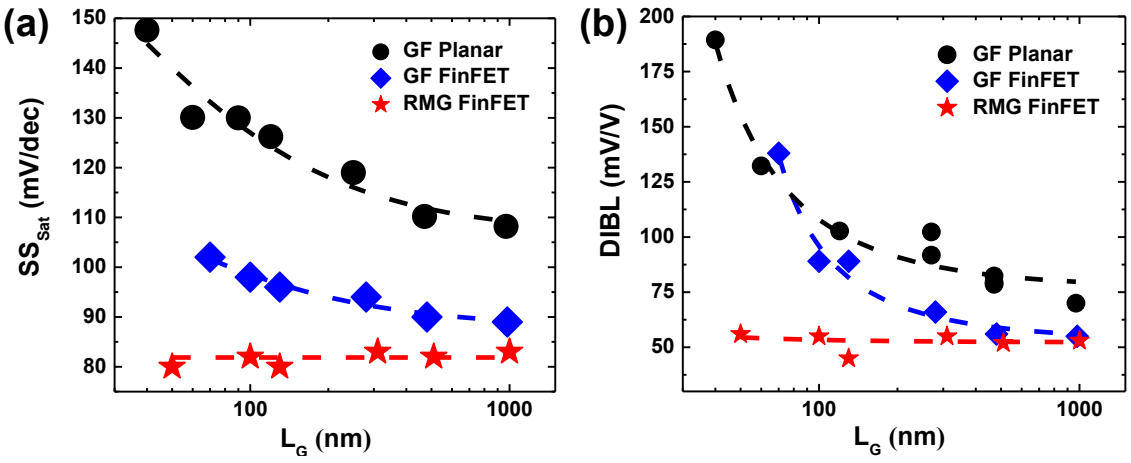



**Figure 4.16:** (a) SS in saturation ($V_{ds}$ = 0.5 V) and DIBL versus $L_G$ roll-off characteristics for GF planar MOSFETs, GF FinFETs and RMG FinFETs.

SS and DIBL roll-off characteristics are presented in Fig. 4.16 where GF planar "optimized on-insulator" MOSFETs from section 4.2 are compared to GF FinFETs on the same wafer and RMG FinFETs. The transition from planar to fin-based devices yields a substantial improvement in both SS and DIBL. GF FinFETs reach the same minimum SS and DIBL floor as GF planar devices, but at $L_G$ = 1 $\mu$m instead of 5-10 $\mu$m. The transition from GF FinFETs to RMG FinFETs leads to a clear improvement in electrostatics as SS close to 80 mV/dec are obtained and no $L_G$ dependence is seen down to $L_G$ = 50 nm on both SS and DIBL. It points to a reduced $D_{it}$ as anticipated from the split C-V data presented in the previous section.

In order to properly benchmark the resulting performance of RMG InGaAs FinFETs to other InGaAs devices in literature and to Si devices, the on-current ($I_{on}$) metrics at fixed off-current ($I_{off}$) and fixed operating voltage ($V_{DD}$) is used. A high $I_{on}$ combines the ability of the device to reach a certain targeted $I_{off}$ with the need for a good SS and a low $R_{ext}$. The impact of $W_{fin}$ on the $I_{on}$ versus $L_G$ trend obtained for the fabricated RMG FinFETs is presented in Fig. 4.17(a) for devices with the best $I_{on}$ at each $L_G$ (which are not necessarily the ones having the best SS). For $W_{fin} > 35$ nm, $I_{on}$ increases linearly with $L_G$ down to $L_G$ = 130 nm. However, a marked drop in $I_{on}$ is observed for $L_G < 130$ nm due to insufficient short-channel effect control (degradation of SS at short $L_G$). The SS vs $W_{fin}$ inset in Fig. 4.17(a) shows that for $L_G$ = 50 nm, SS in saturation remains at approximately 112 mV/dec for $W_{fin} > 45$ nm, suggesting a planar-like electrostatic control of the channel set by the InGaAs thickness. However, as $W_{fin}$ scales down from 45 nm to 15 nm, SS in saturation reduces linearly from 112 mV/dec to 93 mV/dec, confirming

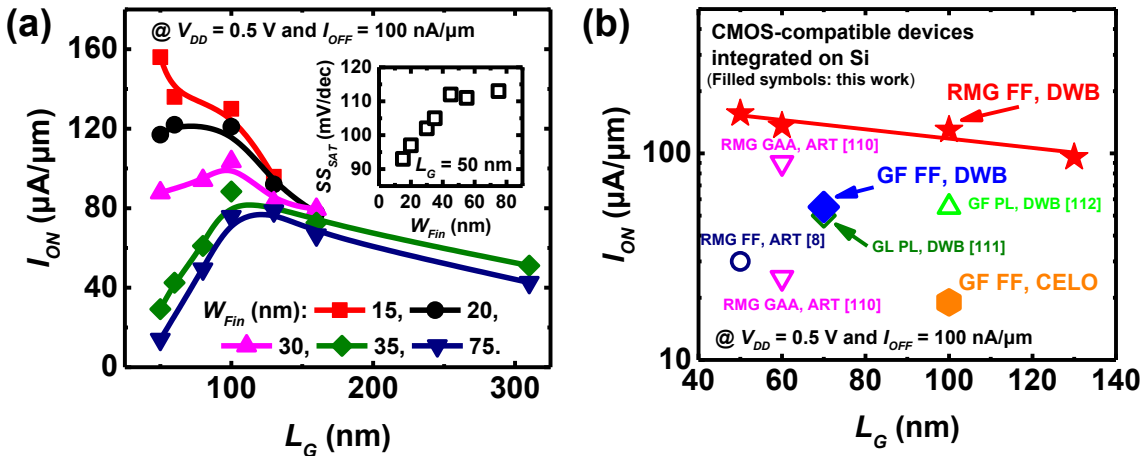



**Figure 4.17:** (a) On-current ($I_{on}$) at fixed off-current ($I_{off}$) = 100 nA/$\mu$m and operating voltage ($V_{DD}$) = 0.5 V versus $L_G$ for different $W_{fin}$ varying from 15 nm to 75 nm. (b) Best $I_{on}$ at fixed $I_{off}$ = 100 nA/$\mu$m and $V_{DD}$ = 0.5 V versus $L_G$ for FinFETs reported in this study (filled symbols) (RMG by DWB (red stars), GF by DWB (blue diamond) and GF by CELO (orange hexagon)) benchmarked against CMOS compatible InGaAs MOSFETs on Si in litterature (open symbols) [8, 110–112] having different architectures ((GF, RMG or gate-last (GL) ; FinFET, planar (PL) or gate-all-around (GAA))).

improved short-channel effect control at scaled $W_{fin}$ due to electrostatic contribution of the sidewalls. As a result, the InGaAs-OI FinFET with $L_G$ = 50 nm and $W_{fin}$ = 15 nm exhibits an $I_{on}$ of 156 $\mu$A/$\mu$m, extracted at fixed $I_{off}$ = 100 nA/$\mu$m and fixed $V_{DD}$ = 0.5 V. Figure 4.17(b) shows an $I_{on}$ versus $L_G$ benchmark, where the presented RMG InGaAs-OI FinFETs with $L_G$ ranging from 50 nm to 130 nm and $W_{fin}$ = 15 nm are compared to other InGaAs MOSFETs or FinFETs integrated on a CMOS-compatible Si platform [8, 110–112]. The figure indicates the InGaAs integration method (DWB, ART or CELO - refering to next section 4.3.3) and the device architecture (GF, RMG or gate-last (GL) ; FinFET (FF), planar (PL) or gate-all-around (GAA)). The presented RMG FinFETs feature the best $I_{on}$ at each $L_G$. However, although the $I_{on}$ of 156 $\mu$A/$\mu$m at $L_G$ = 50 nm represents the highest value reported to date for InGaAs MOS devices integrated on a CMOS-compatible Si platform, an increase by factor 2.3 is required needed to match the $I_{on}$ of state-of-the-art Si MOSFETs at $V_{DD}$ = 0.5 V [3]. A factor 3 reduction in ON-resistance of is required and could be reached by further decreasing the spacer thickness and/or introducing S/D extensions beneath spacers.

Those excellent RMG devices are used in Chapter 5 section 5.3, combined with state-of-the-art SiGe FinFETs in a 3D monolithic integration scheme for the realization of CMOS circuit demonstrators.

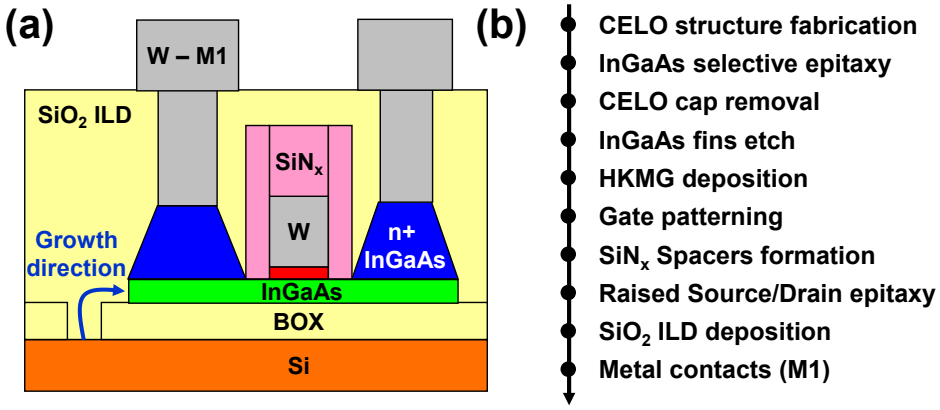



**Figure 4.18:** (a) Schematic of a self-aligned GF InGaAs-OI FinFET integrated on Si by the CELO technique and (b) corresponding baseline process flow.

### 4.3.3 Gate-first FinFETs on selectively grown InGaAs on Silicon

All InGaAs devices on Si presented so far are based on InGaAs-OI obtained by DWB. In Chapter 2 section 2.3, a method to directly integrate InGaAs on Si by selective epitaxy in empty $SiO_2$ cavities (CELO) was presented. In this section, devices are fabricated on selectively grown InGaAs, and characterized. The GF FinFET process is used, despite the better performance of RMG, to simplify the fabrication by avoiding CMP steps.

#### 4.3.3.1 Device fabrication

The schematic of the targeted device architecture and its corresponding process flow are presented in Fig. 4.18. The only nominal difference with GF FinFETs from the previous section 4.3.2 is the fact that a 25 nm thick $In_{0.7}Ga_{0.3}As$ channel is used, grown laterally from a Si seed as indicated by the blue arrow in Fig. 4.18(a). The optimized PEALD gate stack from Chapter 3 section 3.2.3 and low-temperature Sn-doped $In_{0.53}Ga_{0.47}As$ RSD from Chapter 3 section 3.3.1 are used.

Several SEM and TEM images are presented in Fig. 4.19 to illustrate the fabrication process. Firstly, Fig. 4.19(a) shows a tilted SEM image of two InGaAs FinFETs after dry etching of the spacers. The initial Si crystalline seed is clearly visible between the two devices, from which two $\mu$m-sized InGaAs active regions are grown. The SEM image in Fig. 4.19(b) shows a magnified view of the fin/gate region where the overgrown RSD are clearly visible. In the cross-sectional TEM image taken along the channel in Fig. 4.19(c), the (111)-faceted initial Si seed can be observed on the left. In the center of the image, the GF gate is seen, identical to reference GF gates shown in Fig. 4.2(c). A magnified TEM

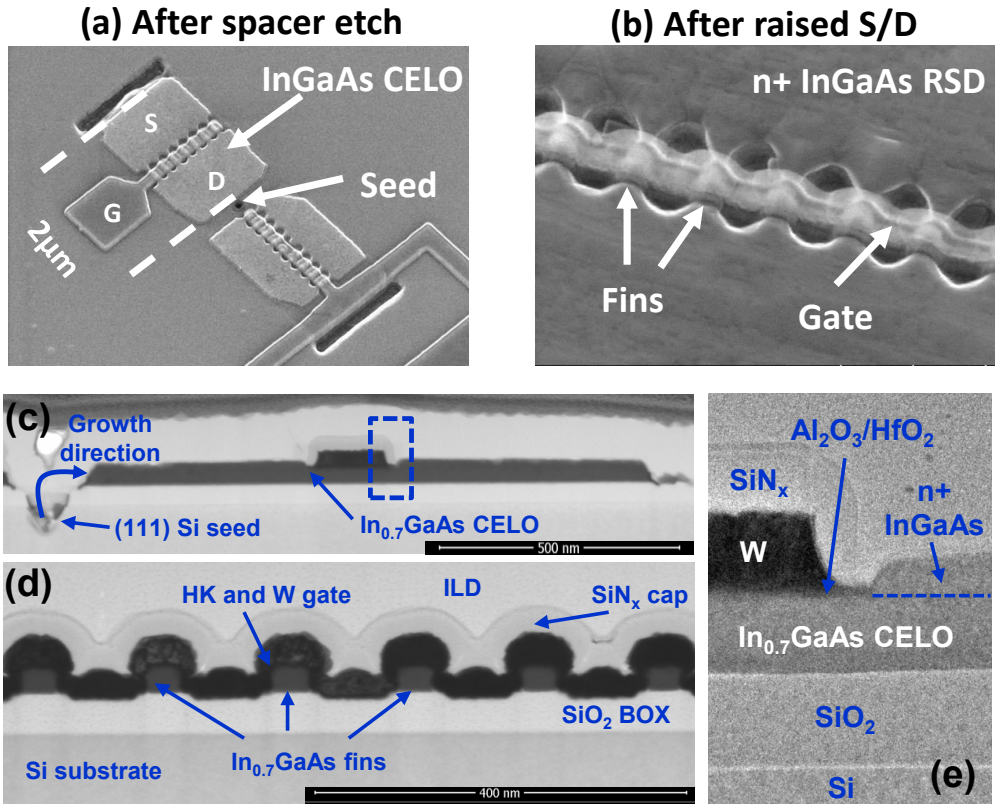



**Figure 4.19:** (a, b) Tilted SEM images of GF FinFETs with $W_{fin}$ = 35 nm (a) after spacer etch and (b) after RSD. (c, d, e) Corresponding cross-sectional TEM images (c, e) across the gate and (d) across the 25 nm x 35 nm fins.

cross-sectional view on the gate edge is presented in Fig 4.19(e) where the presence of thin ALD $SiN_x$ spacers and RSD is clearly visible. Finally, the cross-sectional TEM image taken along the gate in Fig. 4.19(d) highlights the 35 nm wide fins with a conformal deposition of the HK/ W/ $SiN_x$ gate stack. A problem occurred during the digital wet etching of the InGaAs fins prior to HK deposition, leading to a degraded and rough InGaAs surface. This problem is associated to the size of the sample which is too small and does not get properly cleaned and dried between half-cycles of the digital etch process, leading to some undesirable mixture of both oxidant and oxide etch chemicals. It is largely mitigated in a following CMOS run presented in Chapter 5 section 5.2.2, resulting in improved SS, comparable to reference devices on InGaAs-OI obtained by DWB.

#### 4.3.3.2 Electrical characterization

InGaAs FinFETs are obtained on wafers with and without RSD. Data are presented for 25 nm thick fins with $W_{fin}$ of 50 nm. Devices without RSD (Fig. 4.20(a)) exhibit

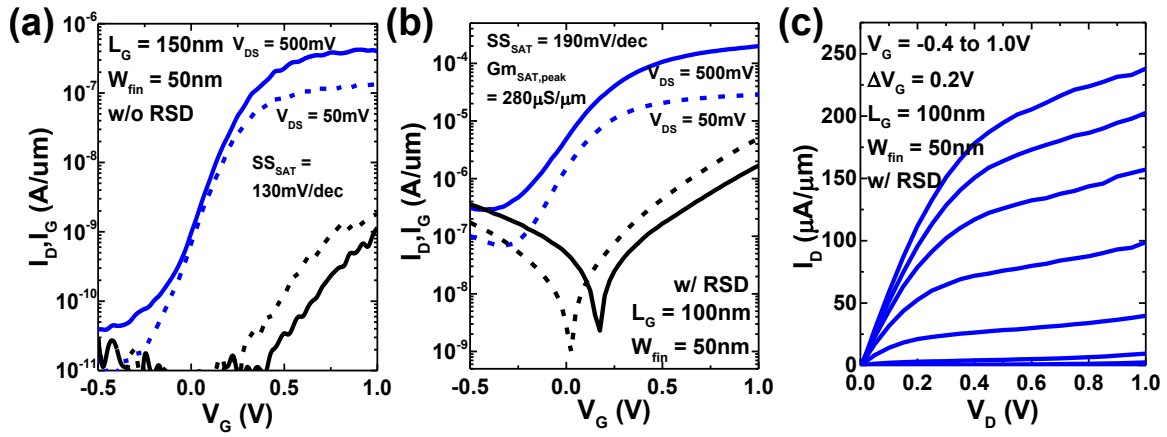



**Figure 4.20:** (a,b) Transfer characteristics of two InGaAs GF FinFET integrated on Si by CELO (a) without or (b) with RSD. (c) Output characteristics of the corresponding device with RSD. $L_G$ = 50 nm, $W_{fin}$ = 50 nm and $H_{fin}$ = 25 nm.

a reasonable SS of 130 mV/dec at $L_G$ = 150 nm. As no RSD are used, the thermal budget is equivalent to the one of RMG devices. A much better SS is therefore expected as it is obtained on RMG reference devices (see section 4.3.2). This difference in SS is attributed to a degraded HK/InGaAs interface, consequence of the above mentioned wet cleaning problem which occurred before HK deposition. Devices with the same process are fabricated as part of a full CMOS flow and presented in Chapter 5 section 5.2.2. There, the wet cleaning problem is reduced and devices are reaching SS as low as 95 mV/dec.

An on/off ratio of 4 orders of magnitude is reached. It confirms the absence of threading dislocations which might create parallel conduction channels from source to drain, and the low background doping of the InGaAs crystal. Devices with RSD (Fig. 4.20(b,c)) demonstrate a better on-performance, reaching a drain current of 0.2 mA/$\mu$m at $V_g$ = 1 V and $V_{ds}$ = 0.5 V, attributed to a largely reduced series resistance. A much higher gate leakage after RSD limits however the off-state current and SS. SS of 190 mV/dec is obtained, higher than without RSD pointing to an increased $D_{it}$ due to the high thermal budget or limited by the higher gate leakage. Nevertheless, it is similar to what is reported in [8] on InGaAs RMG FinFETs integrated on Si by the ART technique.

Combining CELO-integrated InGaAs with the optimized RMG process flow and solving the wet cleaning issue prior to HK deposition should result it largely improved device performance similar to what is obtained on DWB material in section 4.3.2. Owing to the simplicity of the process, GF CELO devices are used as part of a full CMOS flow in Chapter 5 section 5.2.2, co-integrated with SiGe MOSFETs to demonstrate the fabrication of dense circuits.

## 4.4 Conclusion and Outlook

Several device architecture are developed and characterized. They follow the successive introduction of newly developed process modules. Firstly, GF planar devices are studied. Comparing devices with and without self-aligned Ni-InGaAs contacts reveals that direct metal contacts are superior as long as metal contacts are positioned close to the gate edge. In this case, contact resistance dominates over sheet resistance of the metal, which is in favor of direct metal contacts as they have a lower $\rho_C$ to InGaAs RSD. Bi-layer gate stacks show better CET scaling, SS and short-channel effect control than gate stacks containing a-Si which points to the presence of a higher $D_{it}$ than expected in those stacks. Nevertheless, a-Si provides the best effective mobility, which appears to be limited by remote Coulomb scattering. Devices on-insulator present better roll-off characteristics owing to the improved electrostatic control provided by the ultra-thin body. Finally, nano-scaled GF planar MOSFETs are fabricated with 50 nm wide contacts and 120 nm contact pitch.

Non-planar devices are then studied to further improve the electrostatic control at short channel lengths. JL devices are first used to benchmark the fin dry etch module and wet cleaning process. SS of 88 mV/dec is obtained for a CET of 29 Å, with PEALD gate stack processed at a maximum temperature of 300°C. JL MOSFETs suffer from excessive $R_{ext}$ due to a limited doping in S/D regions. Therefore, a RMG process is proposed and developed to integrate the optimized PEALD gate stack on self-aligned FinFETs while maintaining a low thermal budget on the gate stack. SS of 80 mV/dec and DIBL of 56 mV/V are obtained on RMG FinFETs with $L_G = 50$ nm and $W_{fin} = 15$ nm. A record $I_{on}$ of 156 $\mu$A/$\mu$m at fixed $I_{off} = 100$ nA/$\mu$m and fixed $V_{DD} = 0.5$ V is reached owing to the good subthreshold performance, high mobility of 790 cm$^2$/V.s and low $R_{ext}$ in the 500-600 $\Omega\mu$m range. Finally, GF FinFETs are fabricated on InGaAs selectively grown on Si in empty $SiO_2$ cavities. Promising results are obtained in terms of on-current and on/off ratio pointing to the good channel material quality.

Future work should focus on reducing $R_{ext}$ even further, down to at least 150 $\Omega\mu$m. $SiN_x$ spacers need to be scaled down to 5 nm and doping should be introduced beneath spacers.

# Chapter 5

# Circuits: Hybrid InGaAs/SiGe CMOS

## 5.1 Introduction

In this Chapter, hybrid InGaAs/SiGe CMOS circuits are fabricated using different material integration methods and architectures, in order to address the numerous co-integration challenges mentioned in Chapter 1 section 5.1. Two circuit architectures are explored: 2D co-planar and 3D monolithic integrations.

For the 2D co-planar architecture, InGaAs and SiGe devices are processed at the same level, in parallel, like for an industry-standard CMOS technology. This approach is the most cost-efficient in terms of number of processing steps, but is largely constrained by the incompatibility of thermal budgets, wet chemistries and integration density. In a first section 5.2.1, hybrid dual-channel substrates presented in Chapter 2 section 2.2.5 are used to fabricate CMOS inverters with a low-temperature process in order to address the process integration challenges associated with the different chemical properties of the two channel materials.

Then, in section 5.2.2, dense hybrid InGaAs/SiGe 6-transistors (6T)-SRAM arrays are fabricated with CELO-integrated InGaAs and using the GF "optimized on-insulator" MOSFET process from Chapter 4 section 4.2. Emphasis is put on the integration density, cell-sizes down to $0.45\mu m^2$ are demonstrated which corresponds to the 45 nm CMOS node, at the limit of the fabrication facilities available for this work.

In the last section 5.3, a 3D monolithic architecture is explored. It allows an independent optimization of each device layer provided that the thermal budget of the upper layer is compatible with the lower layer. A bottom layer of state-of-the-art p-type GF SiGe MOSFETs from [25] is integrated with an upper layer of RMG InGaAs FinFETs as in Chapter 4 section 4.3.2. 3D inverters are demonstrated without any degradation of n- or p-MOSFETs which highlights that each device layer can be independently optimized.

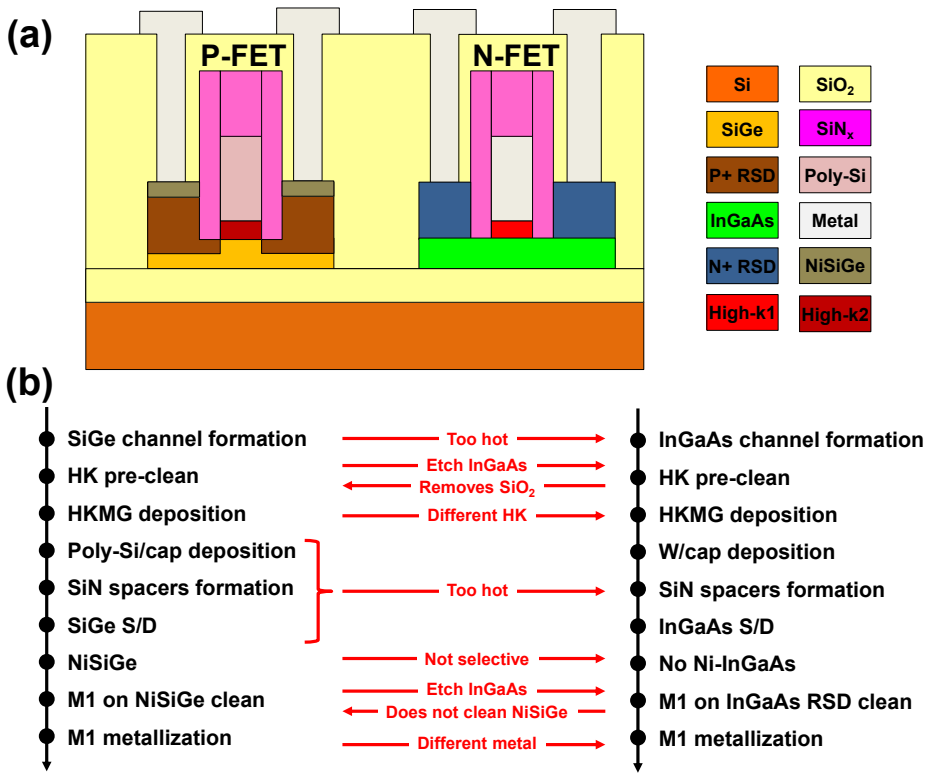



**Figure 5.1:** (a) Schematic and (b) process flow description of an ideal 2D hybrid InGaAs/SiGe CMOS technology with representative best-known process for n- and p-MOSFETs. Non-compatible process modules are highlighted in red in the process flow description.

## 5.2 2D Co-planar CMOS Technology

Figure 5.1(a) illustrates the co-integration challenges with a schematic of an ideal 2D co-planar hybrid InGaAs/SiGe technology, with representative best-known processes for n- and p-MOSFETs. GF integration is used as an example but the challenges remain the same for all integration schemes. Process flows for individual n- and p-MOSFETs are reported (Fig. 5.1(b)) to highlight the process incompatibilities (in red) between the key modules. Clearly, such a technology cannot be manufactured as it is proposed due to numerous SiGe-related steps with a too high thermal budgets, or non-compatible wet cleans which cannot apply for both channel materials.

In the coming sections, two 2D co-planar CMOS technologies are presented with the target to address most of the integration challenges mentioned in Fig. 5.1. Firstly, DWB is used as a development platform to establish a joint CMOS process where SiGe and InGaAs devices are processed together, mostly addressing wet and dry processing issues. Secondly, circuits are fabricated with InGaAs integrated by local selective epitaxy (with

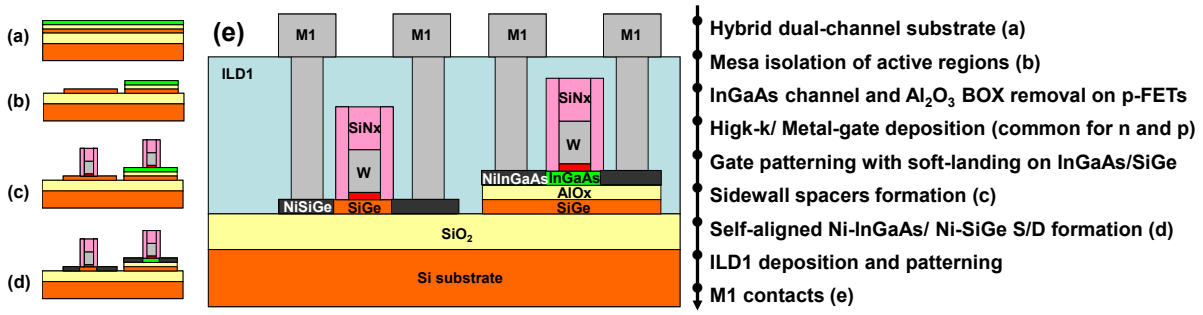



**Figure 5.2:** Process flow description for the 2D co-planar co-integration of InGaAs n-MOSFETs and SiGe p-MOSFETs with a common front-end (a,b,c,d,e) based on hybrid dual-channel substrates obtained by DWB.

the CELO method) as a potential path towards a more industrial solution (since it is inherently compatible with manufacturing on 300/450mm wafers). The used integration scheme is more complex, using the "optimized on-insulator" GF InGaAs process from Chapter 4, and the fabricated circuits are targeting very dense designs. No solution is demonstrated regarding the thermal budget incompatibility between InGaAs and SiGe RSD modules, but possible paths are discussed based on literature.

### 5.2.1 2D InGaAs/SiGe CMOS based on DWB

DWB is the first InGaAs integration method which resulted in the successful co-integration of InGaAs and Ge devices on the same Ge substrate [28], but not on Si. A thin layer of InGaAs was transfer on a Ge substrate with a thin BOX. Very large ($100\times20\mu m^2$) n- and p-MOSFETs were fabricated next to each other with a low-temperature process yielding poor $V_T$ matching and subthreshold performance which made impossible the operation of CMOS circuits.

It is proposed to use a similar approach to demonstrate scaled CMOS inverters based on InGaAs and SiGe self-aligned GF planar MOSFETs on a Si platform. For that purpose, hybrid dual-channel substrates containing ultra-thin InGaAs and SiGe channels on Si are combined with a simplified GF process where RSD are omitted and replaced by Ni-alloyed contacts (see section 5.2.1.1). Electrical characterization of individual devices is performed and the effect of substrate biasing is explored (see section 5.2.1.2). Finally, CMOS inverters are characterized (see section 5.2.1.3).

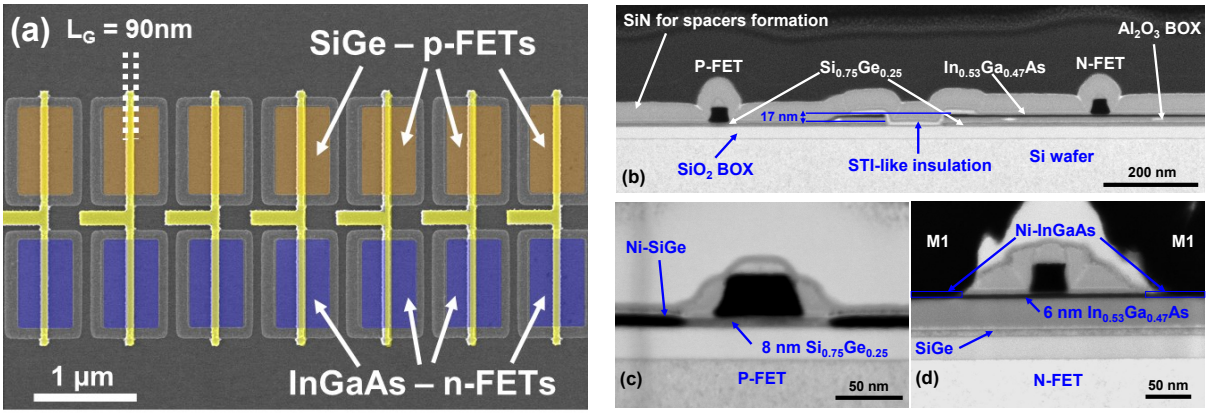



**Figure 5.3:** (a) Top-view SEM micrograph of a dense inverter chain after gate patterning. (b, c, d) TEM cross-sections of n- and p-MOSFETs at different stages of the process: (b) n- and p-MOSFETs before spacer formation (Fig. 5.2(c)), (c) p-MOSFET with $L_G$ = 65 nm after the front-end (Fig. 5.2(d)), (d) n-MOSFET with $L_G$ = 40 nm after M1 (Fig. 5.2(e)).

#### 5.2.1.1 Circuit fabrication

The fabrication process is illustrated in Fig. 5.2 with schematics at different stages of the process, and the corresponding process flow. The starting hybrid dual-channel substrate consists of 6 nm $In_{0.53}Ga_{0.47}As$ on 10 nm $Al_2O_3$ BOX on 8 nm SiGe (25%-Ge) on 25 nm $SiO_2$ BOX on a Si wafer (Fig. 5.2(a), see Chapter 2 section 2.2.5). Firstly, the n- and p-active regions are defined and isolated from each other by the dry etching of mesas in the InGaAs and SiGe layer, similar to an ETSOI process flows [5]. Then, the InGaAs channel and its $Al_2O_3$ BOX are selectively removed where p-MOSFETs need to be fabricated, as illustrated in Fig. 5.2(b). It implies that the n- and p-channel materials are not at the exact same height. A small step corresponding to the sum of the $Al_2O_3$ BOX and InGaAs thickness exists, which is about 17 nm in this case. It is not a show-stopper for manufacturing as long as this step remains within the depth of focus of lithography steppers which is on the order of 40 nm, although it is preferable to minimize it.

The rest of the fabrication process is adapted from the GF process from Chapter 4 section 4.2, with a thermal ALD $Al_2O_3/HfO_2$ gate stack as in Chapter 3 section 3.2.2.2. For the sake of simplicity, a common HKMG stack is used, although independently optimized gate stacks could be used as for standard ETSOI CMOS technology. The gates are patterned by dry etching, stopping on the HK layer which is removed by wet etching. $SiN_x$ spacers are deposited by PECVD and dry etched selectively to SiGe and InGaAs, in two steps (Fig. 5.2(c)). Spacers on p-MOSFETs are dry etched first followed by the formation of p-type S/D regions. Then, spacers on n-MOSFETs are dry etched and n-

type S/D regions are realized. For S/D regions on both types of devices, self-aligned contacts are fabricated using Ni-alloy metal source and drain contacts: Ni-SiGe is used for p-MOSFETs, Ni-InGaAs for n-MOSFETs (Fig. 5.2(d)). The dual-spacer process used here is not required in principle as both Ni-SiGe and Ni-InGaAs could be formed in the same step. Nevertheless, it is developed to allow fabricating different S/D regions for each device type in the future. For instance, in the next section 5.2.2, Sn-doped InGaAs RSD for n-MOSFETs and Ni-SiGe for p-MOSFETs are used. Finally, a $SiO_2$ ILD is deposited and patterned to form EBL defined contact holes combined with direct M1 W contacts (Fig. 5.2(e)).

As the bonding process for the fabrication of the initial hybrid dual-channel substrate occurs at full wafer scale, no constraint exist on the placement, size and density of InGaAs and SiGe transistors. This design flexibility is highlighted in Fig. 5.3(a) which presents a top view SEM image of a dense inverter chain taken after gate patterning where n- and p-MOSFETs are spaced by only 250 nm. An overview TEM cross-sections of n- and p-MOSFETs after spacer deposition is presented in Fig. 5.3(b). It shows the dual-channel structure of the substrate as evidenced by the presence of the SiGe channel below the InGaAs channel. The small height difference of 17 nm between the InGaAs and SiGe channels is also apparent. Magnified TEM cross-sectional views of p- and n-MOSFETs after finishing the FEOL process are also shown in Fig. 5.3(c, d). The observed difference in spacer thickness between both types of devices is due to the dual-spacer process to allow a different contacting scheme on p- and n- devices. In this case, the large spacer thicknesses (chosen to maximize yield) should result in a large difference of access resistance between both types of devices.

#### 5.2.1.2 Characterization of isolated devices

The transfer characteristics acquired on short-channel devices ($L_G$ of 40 nm and 65 nm for n- and p-MOSFET respectively) show well-behaved operation with on/off drain current ratios above $10^4$ (Fig. 5.4(a, b)). The maximum drain current on the n-MOSFET is lower than on p-MOSFET due to the difference in access resistance as highlighted above. Both device types exhibit poor subthreshold performance, as well as a strong negative $V_T$ shift only for n-MOSFETs. As evidenced in the TEM cross-sections presented in Fig. 5.3(c, d), the same gate stack is used for both device types meaning that no $SiO_2$ interlayer is present to improve the MOS interface quality of p-MOSFETs. It will be shown in the next section 5.2.2 that the use of an $SiO_2$ interlayer largely improves the subthreshold performance of p-type devices. For n-type devices however, a better SS was expected.

As both device types have the same gate stack and only n-MOSFETs are subjected to a

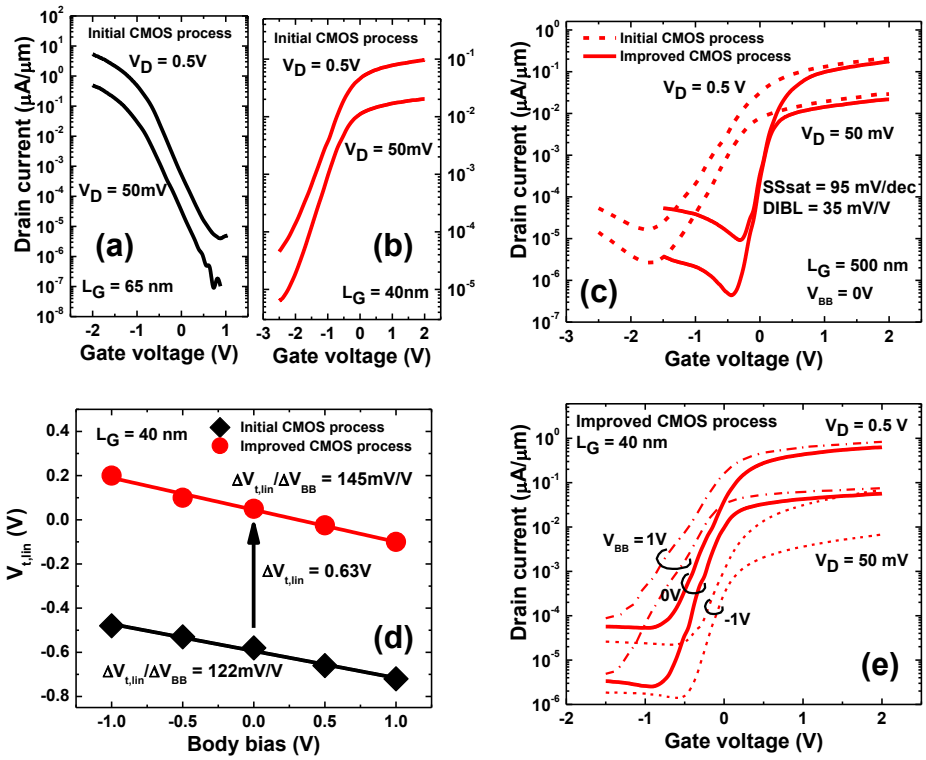



**Figure 5.4:** (a, b) Transfer characteristics obtained on isolated SiGe and InGaAs MOSFETs from the initial CMOS process for: (a) short-channel SiGe p-MOSFET with $L_G = 65$ nm and (b) short-channel InGaAs n-MOSFET with $L_G = 40$ nm. (c) Transfer characteristics obtained on isolated InGaAs n-MOSFETs with $L_G = 500$ nm, comparing the initial and improved CMOS process. (d) $V_T$ vs body bias in linear regime on short-channel InGaAs p-MOSFETs with $L_G = 40$ nm, comparing the initial and improved CMOS process. (e) Transfer characteristics versus body bias obtained on an isolated InGaAs MOSFETs with $L_G = 40$ nm.

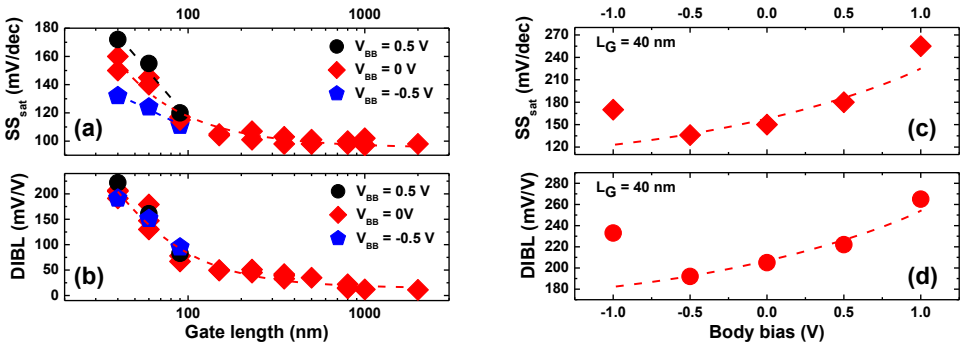



**Figure 5.5:** (a) SS in saturation and (b) DIBL versus $L_G$ for InGaAs n-MOSFETs of the improved CMOS process, some devices are reported for different body bias. (c) SS in saturation and (d) DIBL versus body bias for an InGaAs n-MOSFET with $L_G = 40$ nm.

strong $V_T$ shift, it indicates that the $Al_2O_3$ BOX contains a high density of fixed charges and presents a high $D_{it}$. This problem is largely mitigated by a less aggressive BOX deposition and introduction of $H_2$/Ar anneal. The improvements obtained on transfer characteristics for n-MOSFETs are presented in Fig. 5.3(c) where two identical devices are compared with the initial and improved CMOS process. A large improvement in SS and DIBL is observed, with 500 nm long devices reaching 95 mV/dec and 35 mV/V respectively. Improved devices also exhibit a positive $V_T$ shift of approximately 0.63 V owing to the removal of $6\times10^{12}$cm$^{-2}$ of fixed charges. No significant changes are observed on p-MOSFETs. The large $V_T$ shift observed on n-MOSFETs is further highlighted in Fig. 5.4(d) where $V_T$ in linear regime ($V_{ds}$ = 50 mV) is plotted versus the body bias. Despite the complex stack between the InGaAs channel and the substrate (comprised of $SiO_2$/ SiGe/ $Al_2O_3$), large body bias induced $V_T$ shifts (body factor) of 122 mV/V and 145 mV/V are extracted on initial and improved short-channel n-MOSFETs. The impact of body-biasing on transfer characteristics of a short-channel n-MOSFET with 50-nm-long gate length is shown in Fig. 5.4(e). $V_T$ shift is achieved together with an undesirable access resistance modulation: body-biasing accumulates or depletes carriers below the spacers which largely modulates the access resistance.

SS and DIBL roll-off curves for n-MOSFETs of the improved CMOS process show a very similar behavior as GF "on-insulator" devices from Chapter 4 section 4.2, with a slightly improved DIBL owing to the thinner channel (Fig. 5.5(a, b)). A negative body bias improves SS for short-channel devices which can be attributed to an increased gate control as the centroid of charges shifts towards the gate. Body biasing has a more moderate impact on DIBL. SS and DIBL dependence on body bias on a 40 nm long n-MOSFET are summarized in Fig. 5.5(c, d). The off-trend increase of SS and DIBL at a body bias of -1 V is attributed to the low on/off ratio where off-state leakage starts to play a significant role (see Fig. 5.4(e)).

#### 5.2.1.3 CMOS inverters

CMOS inverters fabricated with the initial and improved CMOS process were characterized. Functional inverters down to $L_G$ = 60 nm and $V_{ds}$ = 0.2 V are obtained for both processes. The large negative $V_T$ shift of n-MOSFETs and the mismatch in on-current with the initial CMOS process yield inverters whose switching voltages occur for negative input voltage ($V_{in}$) values. In addition, inverters featuring very short-channels require a $V_{in}$ sweep larger than $V_{DD}$ to switch from on-state to off-state. Properly operating CMOS inverters should present an output voltage ($V_{out}$) switch from $V_{DD}$ to 0 V for a $V_{in}$ sweep restricted to 0V to $V_{DD}$. All inverters from the initial CMOS process as well as all short-

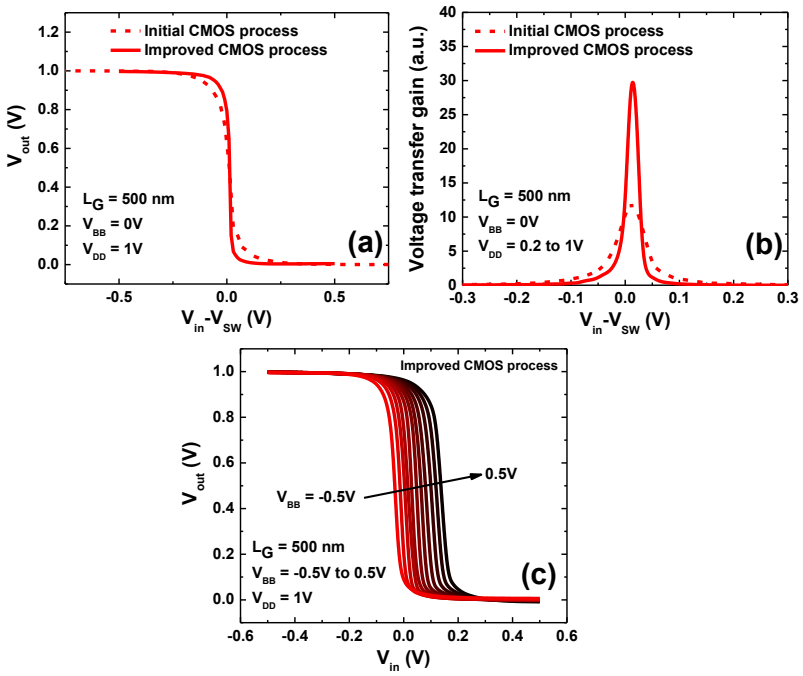



**Figure 5.6:** (a) Comparison of voltage transfer characteristics and (b) voltage transfer gain for inverters built with the initial or improved CMOS process. (c) Voltage transfer characteristics versus body bias for an inverter built with the improved CMOS process.

channel inverters from the improved CMOS process do not fulfill those proper operation conditions.

Figure 5.6(a) presents the voltage transfer characteristics for inverters from the initial and improved CMOS process with $L_G = 500$ nm. For better comparison, $V_{in}$ is shifted to match switching voltage ($V_{SW}$) of both inverter. The better $V_T$ and on-current matching of the improved CMOS process results in a steeper transition at $V_{SW}$. It results in a 2.5-fold increase in the voltage transfer gain (Fig. 5.6(b)).

The voltage transfer characteristics of an inverter from the improved CMOS process with $L_G = 500$ nm are shown for different body-bias in Fig. 5.6(c). For a $V_{DD}$ of 1 V, $V_{SW}$ should ideally be close to 0.5 V. Here, it is shifted to $V_{in}$ between 0 V and 0.2 V depending on body-bias, indicating a still unbalanced pull-down current from the n-MOSFET. The $V_{SW}$ modulation with body bias is a joint consequence of the $V_T$ and $R_{ext}$ modulation presented above. Those inverters can be interconnected to build more complex circuits where one inverter can drive another since switching from on-state to off-state is achieved in a fixed $V_{DD}$ operating window. This initial demonstration paves the way towards the fabrication of ring-oscillators and SRAM cells.

### 5.2.2 2D InGaAs/SiGe CMOS based on CELO

The hybrid InGaAs/SiGe CMOS technology demonstrated in the previous section 5.2.1 represents a step forward for the understanding of the co-processing of such dissimilar n- and p-MOSFETs. This technology implementation remains very complicated for industrial applications as: 1) it implies to collaborate with a wafer supplier which could provide hybrid dual-channel substrates on large wafer scale, 2) it is more challenging to realize FinFETs and 3) the presence of the unused floating-body SiGe channel beneath the InGaAs channel might represent a significant source of reliability degradation.

An industrial CMOS manufacturer might largely prefer to have the possibility to simply grow InGaAs where required, directly in its standard circuit cells, only with slight modification of its baseline process. In order to evaluate the potential of a technology, dense 6T-SRAM arrays are usually realized to demonstrate the density and process control (variability) while ring-oscillators serve to benchmark the technology performance.

In this section, it is proposed to use the CELO technique presented in Chapter 2 section 2.3 to co-integrate InGaAs MOSFETs with SiGe devices on a Si platform by selective epitaxy. Such a technology is inherently compatible with any wafer size and would represent the first demonstration of InGaAs/SiGe CMOS circuits where InGaAs is selectively grown on Si. Dense 6T-SRAM arrays are designed and fabricated to assess the applicability of this technique for standard circuit cells. The minimum cell size is pushed to the fabrication limits of the available facilities for this work.

#### 5.2.2.1 Circuit fabrication

Figure 5.7 presents the integration concept for dense hybrid InGaAs/SiGe CMOS circuits on Si. Selectively grown InGaAs can be combined with SiGe obtained by any preferred industry-standard integration process (bulk/on-insulator, planar/fins). For this demonstration, a 8 nm thick SiGe channel with 25%-Ge on 25 nm BOX (Fig. 5.7(a)) is obtained from ETSOI substrates by Ge condensation (as explained in Chapter 2 section 2.2.5).

Firstly, p-MOSFETs active regions (mesas or fins) are formed by dry etching. Small openings are dry etched in the BOX down to the Si substrate which acts as a crystalline seed for subsequent InGaAs epitaxy (Fig. 5.7(b)). Then, a sacrificial material is deposited and patterned into a shape that comprises the final shape of n-MOSFETs active regions and overlaps with the Si seeds (Fig. 5.7(c)). A $SiO_2$ capping oxide is deposited and openings are formed down to the sacrificial material, which is etched away resulting in empty $SiO_2$ cavities (Fig. 5.7(d)). The wafers are cleaned from organic contaminants and wet etched to form a pristine (111)-faceted Si surface in the seed regions. In an

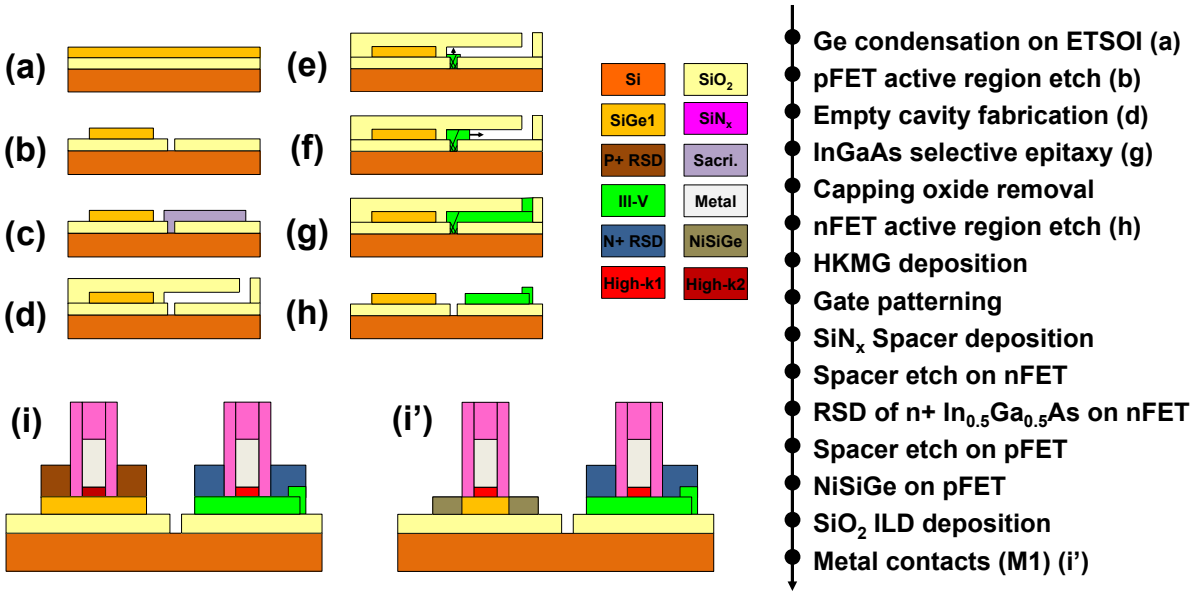



**Figure 5.7:** Process flow schematic and description for the 2D co-planar co-integration of InGaAs n-MOSFETs and SiGe p-MOSFETs with a common front-end based on selective epitaxy of InGaAs in empty $SiO_2$ cavities.

MOVPE reactor, $In_{0.7}Ga_{0.3}As$ is selectively grown to refill the empty $SiO_2$ cavities. A 30 nm thick $In_{0.7}Ga_{0.3}As$ channel is chosen to allow the fabrication of both planar MOSFETs and FinFETs. The epitaxy starts vertically from the Si seeds (Fig. 5.7(e)) and continues laterally towards the cavity openings (Fig. 5.7(f)). This way, defect filtering is handled with minimal area penalty, while the lateral growth direction is used for defining the active channel material. Once the cavity is filled (Fig. 5.7(g)), the capping oxide is removed and the n-MOSFETs active regions are formed by dry etching (mesas or fins) (Fig. 5.7(h)). The InGaAs n-MOSFETs and SiGe p-MOSFETs can be processed with independently optimized HKMG and RSD (Fig. 5.7(i)). It is proposed to simplify the integration scheme by having a common PEALD HKMG in a GF scheme, with Sn-doped low-temperature $In_{0.53}Ga_{0.47}As$ RSD for n-MOSFETs and Ni-SiGe alloyed contacts for p-MOSFETs (Fig. 5.7(i')). The HKMG process is slightly adapted, compared to the previous section 5.2.1, to enable the selective formation of an $SiO_2$ interlayer on SiGe without forming a native oxide on the InGaAs surface.

Top view SEM images taken at different stages of the FEOL on dense 6T-SRAM arrays with cell sizes comprised between 0.4 $\mu m^2$ and 0.45 $\mu m^2$ are presented in Fig. 5.8. They illustrate how empty $SiO_2$ cavities can be fabricated in standard cell designs and used to densely integrate InGaAs-OI layers by selective epitaxy next to SiGe. The complete fabrication process comprises 12 levels of EBL which requires very strict alignment toler-

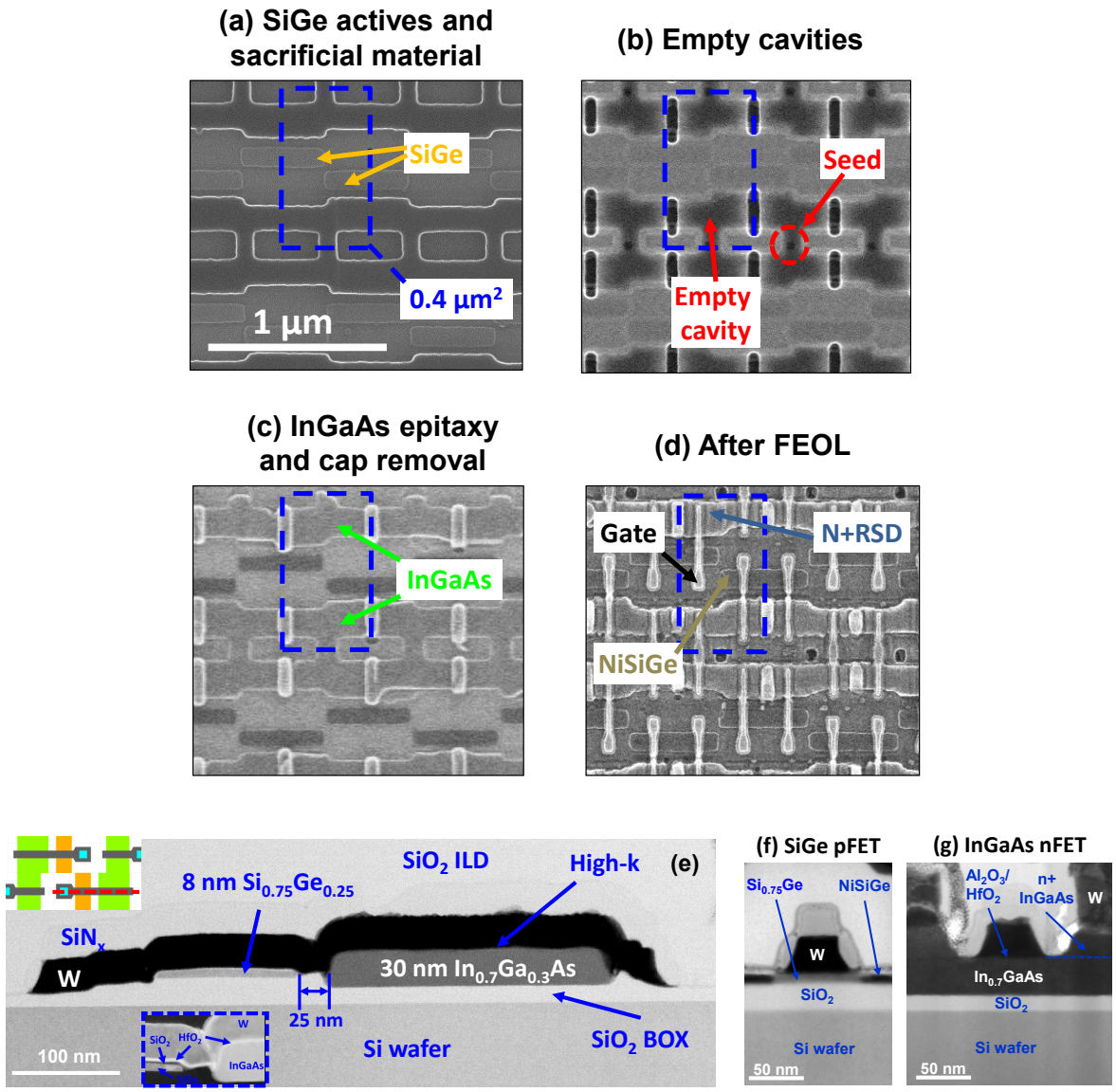



**Figure 5.8:** (a, b, c, d) Top view SEM images of dense 6T-SRAM arrays at various stages of the hybrid InGaAs/SiGe CMOS fabrication process: (a) after sacrificial material patterning, (b) after the formation of empty cavities, (c) after decaping selectively grown InGaAs and (d) after completing the FEOL process. All images are taken on dense SRAM arrays having a cell size below 0.45 $\mu m^2$. (e) TEM cross-sectional image taken along the gate of an inverter of a dense SRAM cell (red-dashed line in SRAM layout shown in the top-left inset). Dashed blue rectangular inset (bottom left): High-resolution dark-field TEM image with emphasis on HK layers. (f, g) TEM cross-sectional images taken across the gates ($L_G$ = 55 nm) for GF (f) SiGe p-MOSFET and (g) InGaAs n-MOSFET.

ances. Given the achieved overall alignment accuracy of about 25 nm, it is not possible to yield 6T-SRAM cells smaller than 0.4 $\mu m^2$. Still, it enables the fabrication of four n-MOSFETs and two p-MOSFETs in about 460 nm $\times$ 860 nm which is straightforward for CMOS manufacturing lines but a great challenge in a research environment.

The tight integration of InGaAs, SiGe and Si is further illustrated in the TEM cross-sectional view along the gate of an inverter of an SRAM cell shown in Fig. 5.8(e), where those three heterogeneous semiconductors are integrated within a 25 nm spacing. In the inset acquired at higher resolution in dark-field, the presence of a 1.5 nm thick $SiO_2$ layer between the SiGe channel and the HK layers is clearly visible, it is used to improve the $D_{it}$ on p-MOSFETs. In the contrary, this inset did not reveal the presence of any native oxide at the HK/InGaAs interface. It shows a path towards independently optimized gate layers for each channel type, in a selective manner.

TEM cross-sectional views across the gates of p- and n-MOSFETs with $L_G = 55$ nm are presented in Fig. 5.3(f, g). The two devices appear to be very similar to the p-MOSFET from Fig. 5.3(c) and the n-MOSFET from Fig. 4.19(c), as expected.

#### 5.2.2.2 Characterization of isolated devices

The transfer and output characteristics acquired on short-channel SiGe p-MOSFET and InGaAs n-MOSFET with $L_G = 35$ nm are shown in Fig. 5.9(a-d). The SiGe p-MOSFET present a good electrostatic integrity with SS in linear regime of 138 mV/dec and DIBL of 85 mV/V owing to the 8 nm thick SiGe channel. It is notably better than what was obtained on p-MOSFETs in the previous section 5.2.1. This improvement is attributed to the presence of a thin $SiO_2$ interlayer which reduces $D_{it}$. However, the p-MOSFETs on-current is limited by the large series resistance of the Ni-SiGe layer. The fabrication of high-performance SiGe p-MOSFETs at a low process temperature (below 700°C) is an active field of research and might be a necessary condition to the successful co-integration with InGaAs. For instance, better p-MOSFETs performance could be obtained with low-temperature B-doped SiGe RSD [113] or low-temperature activated S/D extensions by solid phase epitaxial regrowth [114].

The presence of Sn-doped InGaAs RSD on n-MOSFETs result in better on-current with 100 $\mu A/\mu m$ at $V_g = 1$ V and $V_{ds} = 0.5$ V. It is lower than in similar devices from Chapter 4 section 4.3.3. Comparing Fig. 4.19(e) and Fig. 5.8(g), it appears that although the $SiN_x$ spacers should nominally be the same, the resulting spacer thicknesses are different as devices shown in Fig. 4.19(e) have a more pronounced gate footing which effectively reduces the spacer size at the gate foot. Owing to the 30 nm thick InGaAs body, 35 nm $L_G$ n-MOSFETs suffer from severe short-channel effects resulting in degraded SS and DIBL.

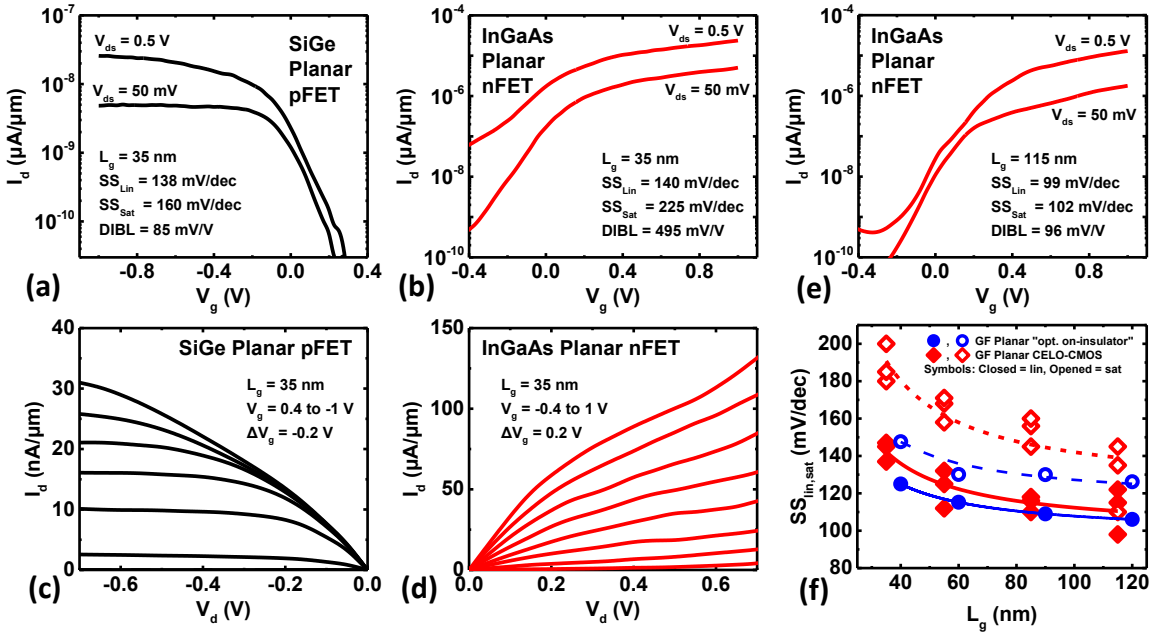



**Figure 5.9:** (a, b) Transfer and (c, d) output characteristics of short-channel (a, c) SiGe p-MOSFET and (b, d) InGaAs n-MOSFET with $L_G$ = 35 nm. (e) Transfer characteristic of a long-channel InGaAs n-MOSFET with $L_G$ = 115 nm. (f) SS versus $L_G$ plots in linear and saturation regime.

Comparing n- and p-MOSFETs with $L_G$ = 35 nm, it clearly appears that it is not possible to obtain working CMOS circuits as the on-current of the p-type device is equivalent of the off-current of the n-type device. The p-MOSFET will not be able to pull-up the output voltage of an inverter. Switching to longer-channel devices improves the situation as n-MOSFETs with $L_G$ = 115 nm have a more attractive SS and DIBL of 102 mV/dec and 96 mV/V respectively. It is notably better than what is reported in Chapter 4 section 4.3.3 owing to an improved interface quality as the wet cleaning problem before HKMG is now minimized (compared to Chapter 4 section 4.3.3). This improvement in electrostatic control for $L_G$ = 115 nm brings the off-state current of n-type devices about a decade lower than the on-current of p-type devices. In this situation, CMOS circuit operation is possible although it will be difficult for p-MOSFETs to pull-up $V_{out}$ to $V_{DD}$.

Finally, Fig. 5.9(f) reports the n-MOSFETs SS vs $L_G$ characteristics in linear and saturation regime, compared to those of reference GF planar MOSFETs from Chapter 4 section 4.2. Reference devices have a 20 nm thick $In_{0.53}Ga_{0.47}As$ channel while the CMOS n-MOSFETs have a 30 nm thick $In_{0.7}Ga_{0.3}As$ channel. SS in linear regime is almost identical on both reference and CMOS devices which tends to indicate that the different In-content and the possible difference in material quality does not influence the quality

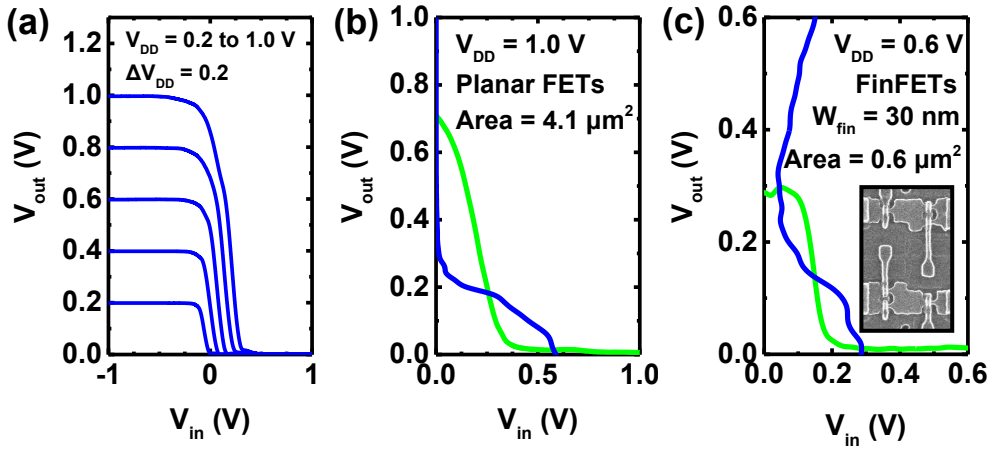



**Figure 5.10:** (a, b, c) Voltage transfer characteristics of hybrid InGaAs/SiGe CMOS (a) planar inverter with $L_G$ = 115 nm, (b) large SRAM cell in "hold" state with planar MOSFETs and cell area of 4.1 $\mu$m$^2$, (c) dense SRAM cell in "hold" state with FinFETs cell area of 0.6 $\mu$m$^2$ (inset: SEM top view of the small FinFET-based SRAM cell).

of the MOS interface. In the contrary, the difference of SS in saturation is much larger owing to the thicker channel thickness.

#### 5.2.2.3 CMOS circuits

Hybrid InGaAs/SiGe CMOS inverters and SRAM cells are fabricated and characterized. The voltage transfer characteristic of an inverter with planar MOSFETs ($L_G$ = 115 nm) is reported in Fig. 5.10(a). As expected from the electrical characterization of individual p- and n-MOSFETs, the characteristic is unbalanced due to a too weak pull-up. For this inverter, a low input results in $V_{out}$ almost reaching $V_{DD}$ logic level (within 50 mV), but many other inverters do not fully reach $V_{DD}$ (not shown). The switching voltages occur at too low $V_{in}$ for all $V_{DD}$, but still above 0 V for $V_{DD}$ of 0.4 V and above. Therefore, SRAM operation is possible although the characteristic is expected to be quenched towards 0 V with a low static noise margin. Inverters which $L_G$ shorter than 80 nm do not work due to the too high off-state leakage on n-MOSFETs.

Figure 5.10(b) presents the voltage transfer characteristic of a large SRAM cell consisting of planar MOSFETs (cell area of 4.1 $\mu$m$^2$), acquired at $V_{DD}$ = 1 V in "hold" state. It is clearly apparent that on both inverters, the pull-up is too weak to reach the high logic level. One inverter reaches 0.7 V, the other one 0.55 V. It means that the drive current of the p-MOSFETs is only a factor 1.5 to 3 higher than the off-current of the n-MOSFETs. Nevertheless, the presented SRAM cell shows the characteristic "butterfly" behavior, but with a poor static noise margin of only 82 mV. SRAM cells with planar

devices and smaller area do not operate due to high off-state leakage on n-MOSFETs.

FinFETs with $L_G$ smaller than 50 nm are also fabricated on this wafer but because of a problem during the fin etch module, the isolated devices are not operational. All FinFET-based SRAM cells were still characterized and, surprisingly, a few of them did show a butterfly characteristic. It is believed that the improved electrostatics at short gate length with the fin architecture reduces the off-state leakage of the n-MOSFETs such that the p-MOSFETs drive current is strong enough to act as pull-up. Figure 5.10(c) shows the example of a small SRAM cell with $W_{fin} = 30$ nm and a cell area of 0.6 $\mu$m$^2$. Both high and low logic levels are hardly reached on the two inverters, pointing to p- and n-MOSFETs having similar current levels but a small on-off ratio. The resulting static noise margin is limited to 53 mV at $V_{DD} = 0.6$ V.

Future work should focus on improving the p-MOSFETs process to boost their on-current, which would greatly improve the SRAM characteristics. Nevertheless, this work represents the first demonstration of InGaAs/SiGe CMOS circuits on Si, obtained by local selective epitaxy of InGaAs. It is using only standard CMOS-compatible process modules and is inherently compatible with 300 mm or 450 mm wafers. Furthermore, the density of integration is comparable to the 45 nm technology node which is a major achievement given the current state of reported InGaAs-based hybrid CMOS technologies. It represents a significant step forward towards the high volume manufacturing of a low power CMOS technology based on high mobility channel materials on Si, but also highlights the challenges associated to the fabrication of InGaAs and SiGe devices at the same level.

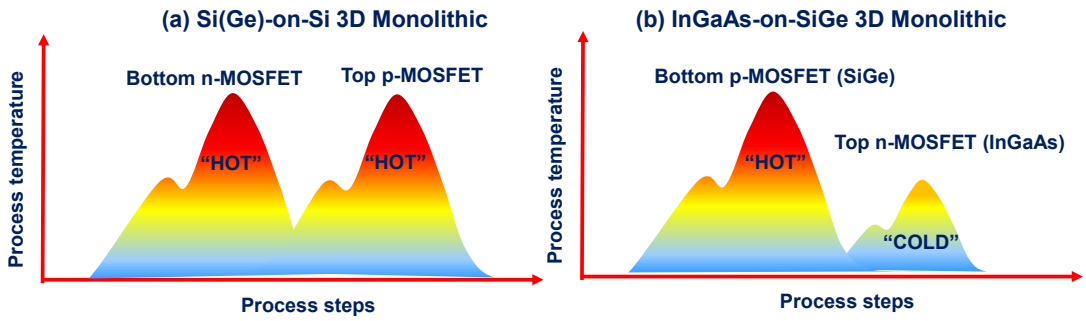



**Figure 5.11:** Illustration of thermal budget evolution versus processing steps for 3D monolithic integration of (a) SiGe or Si MOSFETs on top of Si MOSFETs and of (b) InGaAs MOSFETs on top of SiGe or Si MOSFETs.

## 5.3 3D Monolithic CMOS technology

Scaled hybrid InGaAs/SiGe circuits have already been demonstrated in the previous section 5.2 with a 2D co-planar integration scheme based on DWB or CELO approaches and GF MOSFETs. However, until now, such demonstrations of hybrid CMOS (with InGaAs and SiGe/Ge) have been limited only to silicided S/D contacts. This is primarily due to high thermal budget for standard B-doped RSD module on SiGe, which is currently beyond allowable temperature range for InGaAs (below 600°C) without creating significant material degradation. Therefore, only demonstrations involving low temperature Ni-alloyed contacts have been made. However, it is essential to have RSD on both device layers to achieve a high performance hybrid CMOS technology, as highlighted in the previous section 5.2.2.3. This necessitates that both InGaAs and SiGe devices have their processes independently optimized.

3D monolithic integration has been shown previously to enable independent optimization of different device layers [115, 116]. As the process involves monolithic stacking of semiconducting layers, it provides an opportunity to choose a bottom layer with higher thermal budget and a top layer which requires a lower thermal budget, without degrading the performance of the bottom layer. Besides, 3D monolithic integration has also been proposed to provide significant circuit density increase (about 60%) compared to the standard 2D co-planar integration [116].

The realization of 3D monolithic CMOS circuits based on two layers of Si MOSFETs is extremely challenging. Indeed, the thermal budget required to process the upper Si layer is too high under standard processing conditions, which deteriorates the performance of underlying Si MOSFETs on the bottom layer (Fig 5.11(a)). Although tremendous progress have been recently reported to achieve high-performance top Si n-MOSFETs with a lower

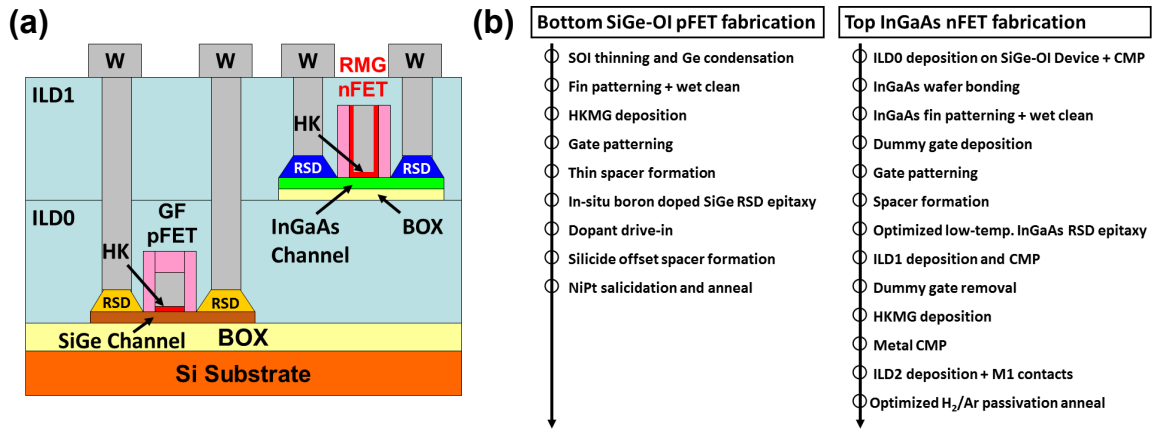



**Figure 5.12:** (a) Schematic and (b) process flow description for the 3D monolithic co-integration of "hot" bottom GF SiGe p-MOSFETs and "cold" top RMG InGaAs n-MOSFETs on a Si substrate by DWB.

thermal budget [114], stacking Si on Si might not properly exploit the full potential of this technology. Instead, stacking can prove to be an excellent choice for realizing hybrid CMOS circuits with a bottom SiGe layer (with high temperature steps) and top InGaAs layer (with lower thermal budget) (Fig 5.11(b)). Such a stacking can be obtained by DWB and has been shown for InGaAs/Ge on Ge substrate [29] and InGaAs/SiGe on Si substrate [30]. However, those demonstrations do not properly highlight the real benefits of thermal budget management and independent optimization of each device layer, as the authors only used low-temperature Ni-alloyed contact for both n- and p-MOSFETs.

In this section, it is proposed to realize hybrid InGaAs/SiGe CMOS circuits on Si by 3D monolithic integration using only CMOS-compatible self-aligned MOSFET architectures with their respectively best available process. A "hot" bottom layer of SiGe p-MOSFETs is realized using a deeply optimized GF FinFET process proven to achieve record performance [25]. A "cold" upper layer of InGaAs n-FinFETs is co-integrated by DWB, using the RMG "optimized on-insulator" FinFET process reported in Chapter 4 section 4.3.2 to give the best performance among CMOS-compatible InGaAs MOSFETs. In this 3D monolithic demonstration, the n- and p-MOSFETs processes are strictly identical to their best known integration routes.

### 5.3.1 Circuit fabrication

Figure 5.12 shows a schematic and the corresponding fabrication flow of the 3D monolithic CMOS stack featuring a RMG InGaAs n-FinFETs layer on a GF SiGe on-insulator p-FinFETs layer. The detailed fabrication flow of the SiGe p-FinFETs is similar to that

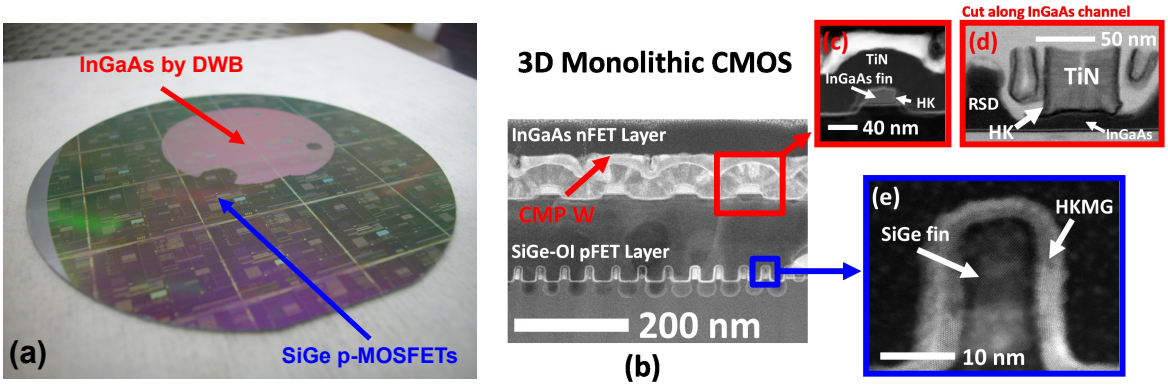



**Figure 5.13:** (a) Photograph of InGaAs bonded on top of processed SiGe devices for 3D monolithic CMOS circuits. (b, c, d, e) Cross-section TEM images of: (a) InGaAs n-FinFET layer on SiGe p-FinFET layer seen along the stacked p- and n-gates, (b) zoom-in on an 8 nm wide SiGe fin, (c) a 30 nm wide InGaAs fin, and (d) cross section along InGaAs channel.

reported in [25]. An SOI substrate is thinned down to the desired thickness and the SiGe 25%-Ge channel is obtained by Ge condensation (as described in Chapter 2 section 2.2.5). Further, a GF integration follows including optimized HKMG/poly-Si gate stack, high-temperature CVD $SiN_x$ spacers, selective epitaxial of B-doped SiGe RSD, B-implantation and Ni-SiGe self-aligned contacts. It yields devices featuring $W_{fin}$ down to sub-10 nm and $L_G$ down to sub-20 nm. Electrical tests are performed at this stage on p-MOSFETs, later compared to the same electrical tests on the same devices after the 3D monolithic integration of InGaAs n-MOSFETs.

The integration of the InGaAs channel above the pre-existing p-MOSFETs layer is achieved using DWB (as described in Chapter 2 section 2.2). After deposition and CMP of a first $SiO_2$ ILD, the transfer of a 20 nm thick $In_{0.53}Ga_{0.47}As$ layer is performed. Then a RMG process is carried out for n-MOSFETs fabrication. It starts with the formation of a dummy gate and thin ALD $SiN_x$ spacers. A key feature of the n-MOSFET fabrication flow is the use of the low-temperature Sn-doped RSD (see Chapter 3 section 3.3.1). This is critical for the thermal stability of bottom p-MOSFETs Ni-SiGe regions. Subsequently, a second $SiO_2$ ILD is deposited and planarized by CMP to expose the top of the dummy gates, which are then removed and replaced by the optimized PEALD gate stack (see Chapter 3 section 3.2.3). Follows a W deposition and metal CMP to complete the formation of the final gates. Finally, contact vias are dry etched down to both device layers, and W M1 interconnects are formed. Post-bonding, this fabrication process requires a selective epitaxy step at 500°C and two CMP steps, highlighting the robustness of the bonded interface between the p- and n-MOSFETs levels.

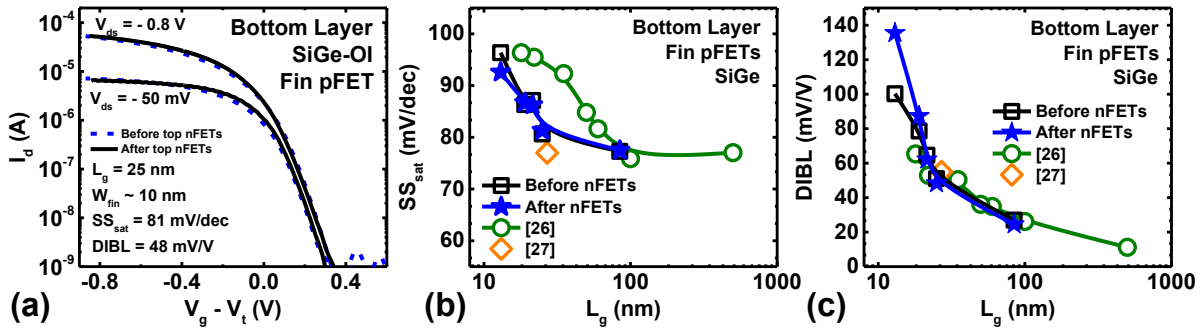



**Figure 5.14:** (a) Transfer characteristics, (b) SS and (c) DIBL roll-off curves versus $L_G$ for SiGe p-FinFETs before and after top n-MOSFETs fabrication. Roll-off characteristics are also compared to previous reports on similar devices [26, 27].

A photograph showing the InGaAs channel bonded on top of the processed SiGe devices is shown in Fig. 5.13(a). An excellent bonding uniformity is obtained owing to the good planarization, low particle count and low surface roughness obtained after the CMP process. A cross-sectional TEM view taken along the stacked p- and n-gates is presented in Fig. 5.13(b). It highlights the presence of tight pitch narrow SiGe fins at the bottom level and larger InGaAs fins with relaxed pitch on top. The characteristic structure of the planarized W/TiN/HK RMG gate can also be observed. Smallest fabricated fins have $W_{fin}$ sub-10 nm for SiGe and approximately 30 nm for InGaAs (see Fig. 5.13(c, e)). Finally, Fig. 5.13(d) presents a cross-sectional TEM view across the n-gate where the typical U-shaped HKMG of the RMG process is seen in the gate, as well as the presence of InGaAs RSD. Some HKMG residues are present on each side of the gate due to the formation of voids during the second $SiO_2$ ILD deposition by PECVD. Nevertheless, it does not compromise the device operation.

### 5.3.2 Impact of nFETs fabrication on pFETs performance

As mentioned above, p-MOSFETs are characterized after completion of their FEOL process and after the full 3D monolithic fabrication. Those electrical data are compared on identical devices to track the influence of the InGaAs n-MOSFETs fabrication on the performance of the underlying p-MOSFETs. The most critical aspect is the impact of the 500°C InGaAs RSD module on the Ni-SiGe alloyed contacts which might negatively impact the $R_{ext}$ of p-MOSFETs. The p-MOS gate stack might also get degraded which would result in worst SS and on-current.

The transfer characteristics of an aggressively scaled p-FinFET with $L_G$ = 25 nm and $W_{fin}$ = 10 nm are shown in Fig. 5.14(a) before and after the fabrication of the top

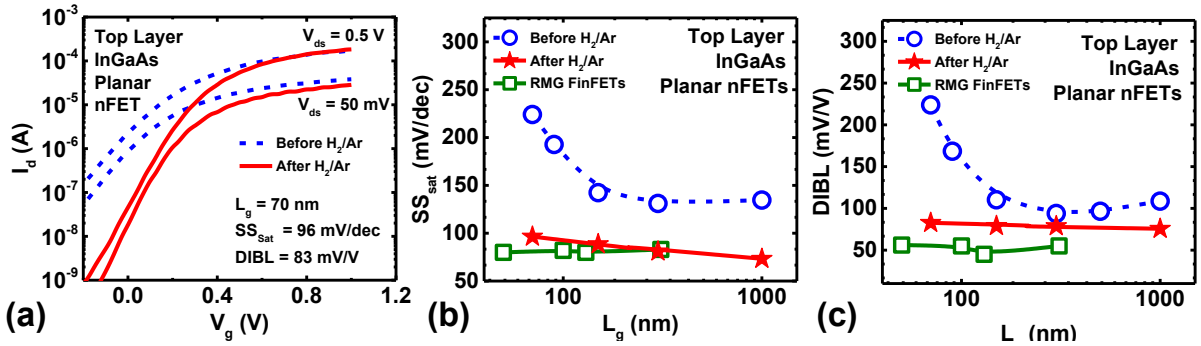



**Figure 5.15:** (a) Transfer characteristics, (b) SS and (c) DIBL versus $L_G$ for planar InGaAs n-MOSFETs on the top layer, before and after an $H_2$/Ar anneal. Roll-off characteristics are compared to optimized InGaAs RMG FinFETs from Chapter 4 section 4.3.2.

n-MOSFETs. A very short-channel device is selected as its performance is dominated by its $R_{ext}$ and short-channel effects control. A small degradation of Ni-SiGe contacts or $D_{it}$ would become clearly apparent. After the full 3D monolithic CMOS fabrication, no degradation can be observed on the linear or saturation current pointing to stable Ni-SiGe contacts and doping profile (although dopant diffusion is not expected given the n-MOSFET thermal budget). Excellent SS and DIBL are obtained, of 81 mV/dec and 48 mV/V respectively with $L_G$ = 25 nm. Comparing SS and DIBL roll-off characteristics before and after the top n-MOSFET process (Fig. 5.14(b, c)) reveals no modification in the subthreshold performance or $D_{it}$. They are identical or better compared to previously published data obtained on p-MOSFETs-only wafers [26, 27].

Those results are very encouraging as they confirm that with a proper thermal budget management, 3D monolithic integration enables co-integrating SiGe p-MOSFETs and InGaAs n-MOSFETs with their respective best known process without compromising on the bottom layer performance.

### 5.3.3 InGaAs n-MOSFETs and 3D CMOS inverters

Both planar MOSFETs and FinFETs are present on the wafer but as in the previous section 5.2.2.3, no isolated FinFETs are operational because of a problem during the fin etch module. The transfer characteristic of a RMG planar MOSFET is reported before and after the $H_2$/Ar anneal carried out at the end of the BEOL (Fig 5.15(a)). A substantial improvement in subthreshold performance is obtained after $H_2$/Ar anneal with SS in saturation and DIBL of 96 mV/dec and 83 mV/V at $L_G$ = 70 nm.

SS and DIBL versus $L_G$ curves are presented in Fig. 5.15(b, c), comparing the 3D monolithic planar RMG MOSFETs before and after $H_2$/Ar anneal with the reference

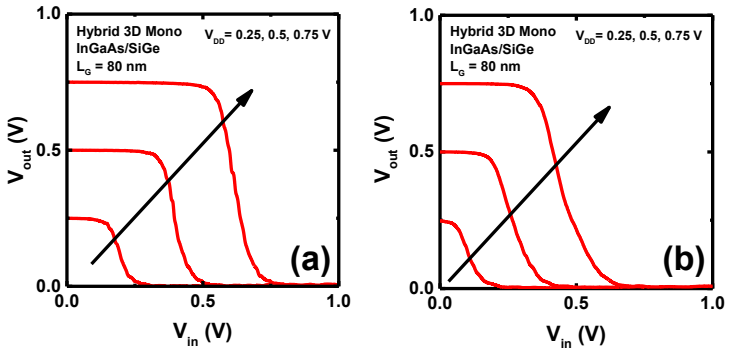



**Figure 5.16:** (a, b) Voltage transfer characteristics of hybrid 3D monolithic InGaAs/SiGe CMOS inverters with p-$L_G$ = 30 nm and (a) n-$L_G$ = 80 nm or (b) n-$L_G$ = 30 nm.

RMG FinFETs from Chapter 4 section 4.3.2. The $H_2$/Ar anneal largely improves the long-channel SS down to 74 mV/dec at $V_{ds}$ = 0.5 V and $L_G$ = 1 $\mu$m, slightly better than on long-channel reference RMG FinFETs and in good agreement with what is expected based on the initial results on JL devices from Chapter 4 section 4.3.1. Weak short-channel effects are seen down to $L_G$ = 70 nm, almost as good as reference FinFETs devices which show no SS degradation down to $L_G$ = 50 nm. Those results confirm that 3D monolithic CMOS integration of "cold" InGaAs devices on "hot" SiGe devices enables maintaining the same level of performance on each device layer.

Finally, hybrid 3D monolithic InGaAs/SiGe inverters are characterized. Figure 5.16 presents the voltage transfer characteristics of scaled 3D inverters at various $V_{DD}$ for different $L_G$ matching: one inverter with n-$L_G$ = 80 nm and p-$L_G$ = 30 nm, another one with both $L_G$ = 30 nm. The large enough on/off ratios and reasonable current matching between n- and p-MOSFETs result in high and low logic levels which are properly reached within $V_{DD}$ limits. Nevertheless, it is clear that the more robust performance of p-FinFETs yields a sharper pull-up than pull-down at small $L_G$, owing to SS degradation by short-channel effects on the n-MOSFET (Fig. 5.16(b)).

Compared to previous reports [29, 30], this is the first demonstration of scalability of 3D monolithic hybrid CMOS with state-of-the-art CMOS process featuring RSD, scaled CET, RMG for n-MOSFETs and short $L_G$ for both p- and n-MOSFETs. This technology is not only promising for future CMOS applications, but is a real platform for monolithic integration of multiple functionalities on-chip to sustain the growing demand for System-on-Chip applications. Possible interesting novel functionalities are III-V RF devices on top of advanced CMOS circuits, or III-V light-sources on top of Si photonics and CMOS for optical interconnects or optical sensors.

## 5.4 Conclusion and Outlook

2D co-planar CMOS architectures are first investigated. Based on hybrid dual-channel InGaAs/SiGe substrates fabricated by DWB, InGaAs n-MOSFETs and SiGe p-MOSFETs are co-integrated on the same Si wafer. A simplified GF planar process is used, with Ni-alloyed metal S/D regions. The resulting devices present a proper $V_T$ and on-current matching yielding operational CMOS inverters in a fixed $V_{DD}$ window.

Selective epitaxy of InGaAs in empty $SiO_2$ cavities is used to fabricate dense 6T-SRAM arrays with 45 nm node ground rules. A more complex MOSFET fabrication flow is demonstrated, with optimized PEALD gate stack, scaled spacers, RSD on n-MOSFETs and NiSiGe alloyed contacts on p-MOSFETs. P-type devices are largely limited by their high $R_{ext}$ owing to the absence of SiGe RSD. N-type devices show promising subthreshold performance with similar SS in linear regime than reference GF devices from Chapter 4. Operational inverters and SRAM cells are obtained as the first demonstration of hybrid InGaAs/SiGe CMOS circuits on Si integrated by selective epitaxy. Furthermore, the achieved density of integration represents a major achievement compared to the current state of reported InGaAs-based CMOS technologies, or even InGaAs MOSFETs in general.

Finally, 3D monolithic integration is explored as a possible route to co-integrate InGaAs and SiGe devices with independently optimized fabrication processes. GF SiGe FinFETs are realized on a bottom layer, while RMG InGaAs MOSFETs are fabricated on a top layer without degrading the performance of underlying SiGe p-FinFETs. 3D CMOS inverters are finally demonstrated.

Future work on 2D co-planar integration should focus on improving the p-MOSFETs process to include low-temperature SiGe RSD. The 3D monolithic platform should be further developed towards RF device integration on top of CMOS circuits as well as III-V lasers on top of Si photonics.

# Chapter 6

# Conclusion

The aim of this study was to assess the possibility of introducing a hybrid InGaAs/SiGe technology platform for CMOS applications. It is addressing the different material and integration challenges associated with its realization, in the context of a potential future high-volume manufacturing.

From the scientific point of view, this topic can largely impact the semiconductor research community as it covers a broad range of fields such as material science, physics and chemistry of interfaces, as well as complex atomistic and quantum transport simulations. From the industrial point of view, it is seen as one of the main candidates for extending the CMOS technology roadmap but it is not yet clear if it will fulfill its promises and be an economically-viable solution.

We hope that our study contributed to advance the development and understanding of this technology by proposing different paths towards a technologically viable industrial solution. In the next paragraphs, the results presented in this work will be aggregated to provide further insights into three of the most relevant open questions in this field and propose associated directions for future research:

- Can we really take full advantage of the low effective mass of electrons in InGaAs to build reliable and scalable InGaAs n-type transistors showing a significant improvement over strained Si ?

- Is it possible to co-integrate InGaAs and SiGe with a high-quality and high-yield on large-scale Si wafers, while fulfilling the CMOS requirements ?

- Can we fabricate CMOS circuits based on InGaAs and SiGe transistors, while maintaining their respective optimum performance and exceeding Si CMOS metrics ?

**• Reliable and scalable InGaAs MOSFETs exceeding strained-Si metrics**

One of the major advancements of InGaAs MOSFETs technology in the past few years was the demonstration of InGaAs-based devices exceeding the performance of industry-standard strained-Si n-MOSFETs [20]. It proved that the expected performance gain envisioned by simulations could translate in real hardware matching those expectations.

As discussed in Chapter 1, these high-performance devices cannot be directly integrated into hybrid circuits as their architecture does not scale down to the density requirements of advanced CMOS chips. In Chapters 3 and 4, technology developments were presented converging towards the realization of high-performance CMOS-compatible InGaAs MOSFETs. It was shown that InGaAs-OI FinFETs with a replacement metal-gate (RMG) process, with a gate stack having a direct HK/InGaAs interface deposited on an *in-situ* cleaned channel surface, with scaled $SiN_x$ spacers, highly-doped raised S/D (RSD) and direct metal contacts seem to be the most promising CMOS-compatible option to outperform strained-Si. Those devices combined high $I_{on}$, low $I_{off}$ and excellent SS.

Although the achieved performance exceeded that of other CMOS-compatible InGaAs MOSFETs on Si, it is still behind that of best reported InGaAs devices on native III-V substrates. It was shown that the main limiting factor is the high series resistance associated with the undoped region beneath the gate sidewall spacers. The introduction of extension regions is necessary in order to take full advantage of the excellent channel transport properties [117]. *Based on those developments, it appears that no major show-stoppers exist which might hinder the realization of CMOS-compatible InGaAs MOSFETs showing significant performance improvements over strained-Si.*

Nevertheless, two major potential roadblocks are still on the way to a reliable and scalable technology. Firstly, the best specific contact resistance ($\rho_C$) achieved to date to highly-doped InGaAs S/D regions is too high (by an order of magnitude) to enable scaling the contact size below 30 nm, as envisioned for advanced CMOS technologies. This issue is not exclusively limited to InGaAs since $\rho_C$ values on Si are also too high, but the problem is more severe on InGaAs as the maximum achievable doping seems to be limited to below $10^{20}$ $cm^{-3}$. Secondly, although it appears that $D_{it}$ and CET scaling of MOS stacks on InGaAs showed tremendous progress and is now almost good enough for advanced CMOS technologies, the reliability of the gate stack remains an open field of research. The extraction methods and targets to assess the gate stack reliability need to be adapted to InGaAs as it appears that, unlike the case of Si, most of the bias temperature instability (BTI) is recoverable on InGaAs. The implications in terms of circuit operation (which might take advantage of this effect), yield and performance, as well as on the projection of product life time are unclear.

**• High-quality and high-yield integration of InGaAs and SiGe on Si**

As discussed in Chapter 1, an advanced CMOS technology based on high-mobility channel materials will most likely integrate InGaAs and SiGe MOSFETs together with Si devices on a Si platform. Owing to the difference is thermal budget, SiGe will be integrated first (by epitaxy, Ge condensation or wafer bonding), followed by the integration of InGaAs.

This InGaAs integration can be realized in the form of blanket layers or local selectively grown films, by a plurality of techniques. The choice of the integration method is primarily guided by the obtained material quality, the compatibility of the technique with dense large-scale CMOS integration, its cost and the final system design. Indeed, depending on whether InGaAs devices are only used in the high-performance logic core or also for the cache memory arrays and I/O devices, it might be preferable to use blanket layers or local selective epitaxy.

Based on the methods and results presented in Chapter 2 about high-quality 200 mm InGaAs-OI substrates obtained by DWB and controlled micron-sized InGaAs islands formed by CELO, it appears possible to realize CMOS-compatible InGaAs substrates by using industry-standard processes. In Chapter 5, the potential of these integration techniques for the fabrication of InGaAs/SiGe CMOS circuits was explored. It was shown that the chosen method has implications in the final circuit architecture in the form of a height difference between n- and p-type transistors (see Chapter 5 section 5.2.1 and section 5.3) or by introducing additional mask levels which might impact the density of integration (see Chapter 5 section 5.2.2). Nevertheless, it was possible to fabricate InGaAs/SiGe CMOS circuits by using DWB or CELO, including dense 6T-SRAM arrays designed with 45 nm ground rules. *Those demonstrations give confidence that the proposed material integration techniques enable the co-integration of InGaAs and SiGe on a Si platform for CMOS applications.*

The lowest reported defect densities in InGaAs on Si are in the low $10^8$ $cm^{-2}$ (see Chapter 2 section 2.2.4, or [55]), which is two orders of magnitude higher than what is expected to be acceptable for CMOS applications. The real impact of those crystalline defects in the active device layer on the transistors performance is not yet fully clear. As long as it does not provide a direct leakage path from source to drain, it does not seem to degrade the carrier mobility or subthreshold performance in large devices where the impact of defects is averaged (see Chapter 4 section 4.3.3 and Chapter 5 section 5.2.2). Therefore, the main implications of defective material on dense CMOS circuits might mostly translate into an increased variability and decreased yield. A very controlled fabrication environment is required to investigate such variability and yield issues which might only be addressable by R&D groups.

**• InGaAs/SiGe CMOS circuits outperforming Si CMOS technology**

In Chapter 1, it was shown that the fabrication of n- and p-MOSFETs based on InGaAs and SiGe channel materials is very challenging owing to the heterogeneous properties of those materials (thermal budget, etch and clean chemistries, oxide interfaces). The realization of hybrid InGaAs/SiGe CMOS circuits which could outperform Si-based chips implies that the best possible performance can be simultaneously obtained for each device type. It was stated a few paragraphs above that no technical show-stoppers can hinder the fabrication of CMOS-compatible InGaAs MOSFET exceeding the performance of strained-Si devices. This statement becomes much more challenging when it is considered in the context of co-integration with an optimized SiGe p-MOSFET.

The developments presented in Chapter 5 intended to address this co-integration issue. It was demonstrated that by using a 3D monolithic integration scheme (see section 5.3), the different thermal budgets could be managed and it was possible to form CMOS circuits for which each device type is realized with its independently optimized process. Although 3D monolithic circuits might be advantageous for future density scaling, 3D technology is not yet considered as a fully viable approach for CMOS manufacturing. In contrast, 2D co-planar integration is preferred, where both n- and p-type devices are co-processed at the same level. Mainly, it implies that thermal budgets should be matched, that different surface preparation have to be used for MOS stacks and dissimilar S/D modules are required on n- and p-MOSFETs. In Chapter 5 section 5.2, some of those issues were addressed. It was shown that it is possible to realize hybrid InGaAs/SiGe CMOS circuits (inverters and 6T-SRAM arrays) with n- and p-MOSFETs having different HK/channel interfaces (with $SiO_2$ interlayer on p- and without InGaAs-oxides on n-type devices) and different S/D regions (RSD on n- and NiSiGe alloyed contacts on p-type transistors). It has not been possible to integrate RSD on p-type devices as the necessary equipments were not available. *Overall, those results on 2D and 3D hybrid InGaAs/SiGe CMOS circuits support a significant advancement of the knowledge and understanding about this technology, which is today still far from approaching the performance of advanced Si CMOS.*

The main roadblock for the 2D architecture is the management of the thermal budget discrepancy between a high-performance InGaAs and SiGe MOSFET processes. Two possible paths forward are (i) the use of ultra-fast anneals to obtain the high temperatures required for SiGe with the potential that it might be short enough such that InGaAs does not deteriorate, and/or (ii) the use of low-temperature processes to form the S/D regions of p-MOSFETs [113, 114]. For the 3D architecture, the use of InGaAs and SiGe is perfectly suited and more mature, but the overall 3D concept needs to become more convincing for industrial applications.

## Final thoughts

In spite of the common belief that a hybrid InGaAs/SiGe technology platform is too complex and not practical for industrial CMOS applications, this study contributed to demonstrate that there are no more major technical show-stoppers to transform this scientifically appealing concept into an industrial solution. It was shown that CMOS-compatible InGaAs MOSFETs have the potential to outperform strained-Si at low operating voltage, that those devices could be densely integrated on large-scale Si substrates, and processed into more complex circuits than ever reported before. Some efforts should still be devoted to lower even further the contact resistance to S/D regions ; understand the implications of gate stack reliability and channel defect density on product operation, yield and lifetime ; and to focus on increasing the performance of n- and p- MOSFETs when they are jointly processed at the same level. Taking the risk to conclude this work on a more "down-to-earth" statement, we should not underestimate the market environment and the competitive landscape. Although this engineering and scientific "dream" appears to be more attainable than ever, its realization in the near future will be more governed by the laws of economics rather than by those of physics.

# Appendix A

# List of Publications

Publications are grouped in three categories: publications related to III-V CMOS, invited talks and other publications. In each group, they are sorted by year, and for each year, by relevance for this thesis.

## List of Publications related to III-V CMOS

L. Czornomaz, V. Djara, V. Deshpande, E. O'Connor, M. Sousa, D. Caimi, K. Cheng, and J. Fompeyrine, "First Integration of InGaAs/SiGe Channels into Dense SRAM Arrays with sub-0.45$\mu$m$^2$ Cell Size Fabricated Using Standard CMOS Processes," *VLSI Technology (VLSI Technology), 2016 Symposium on*, p. submitted, 2016.

L. Czornomaz, V. Djara, V. Deshpande, D. Caimi, L. Pirro, C. Cristoloveanu, and J. Fompeyrine, "Fabrication and Characterization of InGaAs-on-insulator Lateral N+/n/N+ Structures," *Ultimate Integration on Silicon (EUROSOI-ULIS), 2016 Joint International EUROSOI Workshop and International Conference on*, p. accepted, 2016.

L. Pirro, L. Czornomaz, H. J. Park, I. Ionica, M. Bawedin, V. Djara, V. Deshpande, and C. Cristoloveanu, "Volume and interface conduction in InGaAs junctionless transistors," *Ultimate Integration on Silicon (EUROSOI-ULIS), 2016 Joint International EUROSOI Workshop and International Conference on*, p. accepted, 2016.

L. Czornomaz, E. Uccelli, M. Sousa, V. Deshpande, V. Djara, D. Caimi, M. Rossell, R. Erni, and J. Fompeyrine, "Confined Epitaxial Lateral Overgrowth (CELO): A Novel Concept for Scalable Integration of CMOS-compatible InGaAs-on-insulator MOSFETs on Large-Area Si Substrates," *VLSI Technology (VLSI*

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V. Djara, V. Deshpande, M. Sousa, D. Caimi, L. Czornomaz, and J. Fompeyrine, "CMOS-compatible Replacement Metal Gate InGaAs-OI FinFET With $I_{ON}$ = 156 $\mu$A/$\mu$m at $V_{DD}$ = 0.5 V and $I_{OFF}$ = 100 nA/$\mu$m," *Electron Device Letters, IEEE*, p. accepted, 2015.

V. V. Deshpande, V. Djara, D. Caimi, E. O'Connor, M. Sousa, L. Czornomaz, and J. Fompeyrine, "(Invited) Material and Device Integration for Hybrid III-V/SiGe CMOS Technology," *ECS Transactions*, vol. 69, no. 10, pp. 131–142, 2015. [Online]. Available: http://ecst.ecsdl.org/content/69/10/131.abstract

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L. Czornomaz, V. Djara, V. Deshpande, E. Uccelli, N. Daix, D. Caimi, C. Rossel, M. Sousa, H. Siegwart, , and J. Fompeyrine, "(Invited) InGaAs on Si technology platform for high-mobility dual-channel CMOS: from materials to devices and circuits," *Insulating Films on Semiconductors, 19th Conference on*, 2015.

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# Appendix B

# Contributions to this work

All the work shown in this thesis was performed at IBM Research - Zürich, under the guidance of my academic supervisor Sorin Cristoloveanu from IMEP-CNRS and my supervisor at IBM, Jean Fompeyrine. This section briefly highlights my contribution to the results and indicates where my colleagues provided strong support.

All III-V growth developments and most samples by metal-organic vapor phase epitaxy (MOVPE) were performed by myself, with some back-up from Emanuele Uccelli for few samples. In contrary, all III-V growth experiments by molecular beam epitaxy (MBE) (strain-relaxed buffer (SRB) on silicon (Si), 200 mm wafers, in-situ Al-contacts) were done mainly by Emanuele Uccelli, with support from Mirja Richter and Christian Gerl. The maintenance on MOVPE and MBE chambers was operated by Heinz Schmid and Heinz Siegwart, respectively.

I initiated the direct wafer bonding activity and developed the initial process, which was later elaborated in strong collaboration with Nicolas Daix (splitting, 200 mm). The bonding energy measurement setup was designed by Christophe Rossel and used by Nicolas Daix. Once the process was stable, Daniele Caimi realized most layer transfers. 200 mm III-V chemical-mechanical polishing (CMP) was performed in IBM Yorktown by Mahadevaiyer Krishnan's team.

I proposed the confined epitaxial lateral overgrowth (CELO) concept, developed the fabrication process in collaboration with Daniele Caimi and optimized the epitaxy conditions for indium-phosphide (InP) and indium-galium-arsenide (InGaAs).

Material characterizations (atomic force microscopy (AFM), x-ray diffraction (XRD), ellipsometry) were shared between Marilyne Sousa, Nicolas Daix, Jean Fompeyrine and myself, with varying relative loads along the years. I performed most transmission electron microscopy (TEM) sample preparation and scanning TEM (STEM) images in the focused ion beam (FIB) presented in this work, with support from Marilyne Sousa in the last year.

All high-resolution TEM images and analysis were performed by Marilyne Sousa, Marta Rossell, Nicolas Daix and Rolf Erni.

The H-plasma cleans, amorphous silicon (a-Si) depositions, reflection high-energy electron diffraction (RHEED) measurements and most X-ray photoemission spectroscopy (XPS) analysis in the MBE chamber, were realized by Mario El Kazzi, with support from Chiara Marchiori and Jean Fompeyrine. I performed all associated metal-oxide-semiconductor capacitor (MOSCAP) process development, fabrication, electrical characterization and analysis.

All gate stack developments, results and analysis based on thermal atomic layer deposition (ALD) bi-layers were performed on my own. I co-supervised with the cleanroom staff the purchase of the plasma ALD tool with the concept to develop a full *in-situ* high-k metal-gate (HKMG) stack, featuring a plasma cleaning of the surface, plasma-controlled oxidation and oxygen scavenging gate metal. Then, I collaborated with Vladimir Djara and Éamon O'Connor who carried on most of the development of the plasma-assisted ALD gate stack, with support from Nikola Đorđević.

The development of the raised source and drain (S/D) (RSD) modules and self-aligned nickel-indium-galium-arsenide (Ni-InGaAs) contacts were realized mostly on my own with support from Daniele Caimi for Ni wet etching, Christophe Rossel who design the Hall setup and carried on some of the measurements, and Marco Hopstacken from IBM Yorktown for secondary ion mass spectrometry (SIMS) profiling. The study of direct metal contacts was performed by Philipp Mächler under my supervision.

I designed and co-developed the gate-first (GF) self-aligned metal-oxide-semiconductor field-effect transistor (MOSFET) process with Daniele Caimi. Later, Veeresh Deshpande introduced plasma ALD spacers and Vladimir Djara initiated the work on InGaAs junction-less (JL) and fin-based MOSFETs (FinFETs). The four of us developed the replacement metal-gate (RMG) process, and actively shared the fabrication of numerous wafers in the cleanroom. I created a programmable complementary metal-oxide-semiconductor (CMOS) mask design environment in IPKISS on the advice and initial training of Stefan Abel. I then designed most mask layouts with the help of Veeresh Deshpande and Vladimir Djara. I developed the alignment mark process for the electron beam lithography (EBL) tool and ran all EBL exposures which is a very critical process since CMOS wafers need up to 14 EBL levels with 25 nm alignment accuracy. Finally, I developed an automatic and generic measurement routine which allows wafer-scale electrical testing of devices, parameters extraction and trends plotting. Therefore, MOSFET electrical analysis was mostly realized with my automatic test platform, with support from Christophe Rossel, Veeresh Deshpande and Vladimir Djara.

I introduced the concept of 2D co-planar CMOS based on wafer bonding and on CELO, while Jean Fompeyrine initiated the effort on 3D monolithic CMOS integration. Silicon-germanium (SiGe) on insulator wafers for 2D CMOS were provided by Kangguo Cheng from IBM Albany and fully-processed SiGe p-MOSFETs were realized by Pouya Hashemi from IBM Yorktown. I designed all 2D CMOS circuits, while Veeresh Deshpande took care of the 3D CMOS layouts. All CMOS fabrication runs were followed by myself, Veeresh Deshpande and Vladimir Djara, with a strong support from Daniele Caimi. CMOS circuit electrical characterization was shared between Veeresh Deshpande, Vladimir Djara, Éamon O'Connor and myself.

# Appendix C

# Acknowledgements

This work could not have been possible without the contribution and guidance of many persons sharing their time, expertise and passion: the people creates a unique stimulating atmosphere at IBM Research - Zurich.

I would like to first thank Jean Fompeyrine who took the risk to believe in me right from the beginning while my profile was not exactly what he was looking for. Over the years, he efficiently guided me on a scientific and personal level to overcome my limits and develop my professional skills. Having the opportunity to collaborate with him is probably the kind of chance which does not happen often in a lifetime. Similarly, I would also like to thank Sorin Cristoloveanu who also trusted in me as soon as we met and accepted to become my PhD supervisor. His guidance on the scientific work and in the scientific community has always been efficient and insightful. Next, I would like to thank the committee members who spent their precious time to review this PhD work and give extremely valuable suggestions to improve the quality: Francis Balestra, Alexander Zaslavsky, Luca Selmi, Siegfried Mantl and Maud Vinet. Finally, the last acknowledgment for the supervision of this work goes to the local and US management who gave strong support to this work and enabled to create the right environment for success.

Many collaborators from IBM Research - Zurich and other institutes deserve special acknowledgments. First, the initial Advanced Functional Materials team who welcomed me at the very beginning : Mario El Kazzi who started in the same time and mentored me through the jungle of the scientific world, Daniele Caimi with whom we spent countless extra hours developing every single piece of module required for this work , Stefan Abel for his steady enthusiasm about innovation and science, Heinz Siegwart for his expertise and devotion in maintaining all the UHV tools to their best condition, Chiara Marchiori for her expertise in chemistry and interfaces, Mirja Richter and Christian Gerl who introduced me to the parallel reality of MBE growth, Marilyne Sousa for her kindness and never

ending willingness to support, Dave Webb without whom I might not have been able to stay long enough at IBM to finish this work, and finally, President Christophe Rossel who so many times could also have been called Inspector Gadget for his problem solving skills. Next, special acknowledgments are deserved for the people who joined this collaborative effort and all had a strong impact by bringing their ideas and skills to push the limits of this technology: Emanuele Uccelli who successfully managed to master the big beast on a large scale, Nicolas Daix who proved to everybody that he is the real-life James Bond, Vladimir Djara who managed to "junction-lessly" bridge the gap between self-aligned MOSFETs and high performance, Éamon O'Connor for his infinite dedication to engage in scrums with interfacial defects, and Veeresh Deshpande who definitely proved that there is plenty of room at the top. As well, Nikola Đorđević, Luca Pirro, Patrik Ogsnach, Philipp Mächler and Pirmin Weigele stayed a short time but left a long lasting positive impact to this project. Finally, I would like to thank Kangguo Cheng and Pouya Hashemi from IBM Albany and Yorktown as well as Jean-Michel Hartmann from LETI who believed in our crazy ideas and greatly helped to push the limits of co-integration ; the MIND and BRNC groups in Zurich as well as the III-V and CMP teams in Yorktown for their limitless support.

I will always be grateful to my parents, my sister and my (not so little) wife Marion who were an infinite source of inspiration, comfort, motivation and support through all the sometimes beautiful or hard life moments which led to the conclusion of this work.

# Appendix D

# French Summary

## D.1 Introduction

Les materiaux à forte mobilité comme l'InGaAs et le SiGe sont considérés comme des candidats potentiels pour remplacer le Si dans les circuits CMOS futurs. De nombreux défis doivent être surmontés pour transformer ce concept en réalité industrielle. Cette thèse couvre les principaux challenges que sont l'intégration de l'InGaAs sur Si, la formation d'oxydes de grille de qualité, la réalisation de régions source/drain auto-alignées de faible résistance, l'architecture des transistors ou encore la co-intégration de ces matériaux dans un procédé de fabrication CMOS. Les solutions envisagées sont proposées en gardant comme ligne directrice l'applicabilité des méthodes pour une production de grande envergure.

Le chapitre 2 aborde l'intégration d'indium-galium-arsenide (InGaAs) sur silicon (Si) par deux méthodes différentes. Le chapitre 3 détaille le développement de modules spécifiques à la fabrication de transistors auto-alignés sur InGaAs. Le chapitre 4 couvre la réalisation de différents types de transistors auto-alignés sur InGaAs dans le but d'améliorer leurs performances. Enfin, le chapitre 5 présente trois méthodes différentes pour réaliser des circuits hybrides complementary metal-oxide-semiconductor (CMOS) à base d'InGaAs et de silicon-germanium (SiGe).

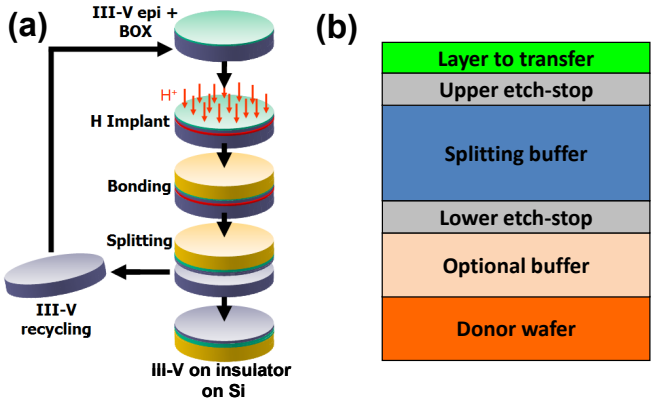



**Figure D.1:** (a) Procédé de fabrication de substrats InGaAs-on-insulator (InGaAs-OI) sur Si par DWB en utilisant la séparation induite par implantation d'hydrogène pour recycler le substrat donneur. (b) Schéma fonctionel de la structure du substrat donneur.

## D.2 Substrats : Intégration d'InGaAs sur Si

L'intégration d'InGaAs sur Si est envisagée sous forme de couches pleines plaques réalisées par collage (direct wafer bonding (DWB)) ainsi que sous forme d'îlots micrométriques crû de manière sélective dans des cavités d'oxyde (confined epitaxial lateral overgrowth (CELO)).

Dans un premier temps, grâce à la technique du collage pleine plaque (DWB) et à la structure fonctionnelle innovante introduite par la Fig. D.1, des substrats d'InGaAs sur isolants (InGaAs-OI) sur 200 mm ont pu être réalisés avec une densité de défauts inférieure à $3\times10^{8}$ $cm^{-2}$. Le recyclage de la plaque donneuse est démontré par une séparation thermique des plaques induite par une implantation préalable d'hydrogène.

Dans un second temps, la surcroissance épitaxiale latérale confinée (CELO) d'InGaAs et d'InP dans des cavités d'oxyde est proposée comme une nouvelle solution pour l'intégration locale de matériaux III-V sur Si. Elle peut être appréhendée comme une analogie à l'échelle micrométrique de la méthode de Czochralski [63] pour la fabrication de substrat monocristallins. La croissance selective du semiconducteur III-V débute à partir d'une petite zone de nucléation sur Si, puis se propage dans une cavité 3D faite de silicon-oxide ($SiO_2$) qui permet un filtrage dans toutes les directions des défauts cristallins au niveau de la région de nucléation, puis l'expansion controlée du cristal jusqu'à atteindre sa forme et taille finale souhaitée (Fig.D.2).

Ces deux techniques (DWB et CELO) sont utilisées dans les chapitres suivants pour la réalisation de transistors et de circuits hybrides CMOS.

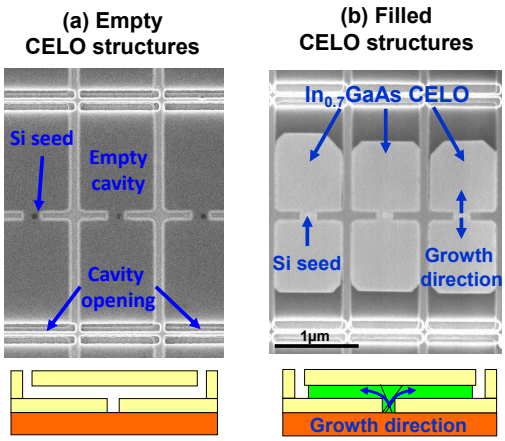



**Figure D.2:** Vue scanning electron microscopy (SEM) du dessus et schémas associés de structures CELO (a) avant et (b) après la croissance séléctive d'InGaAs (with 70% of indium) ($In_{0.7}Ga_{0.3}As$) par metal-organic vapor phase epitaxy (MOVPE).

## D.3 Modules : Empilement de grille et régions S/D

Ce chapitre met l'accent sur le développement de modules spécifiques à la fabrication de transistors auto-alignés sur InGaAs: l'empillement de grille et la formation de régions source and drain (S/D) permettant une faible résistance d'accès.

Premièrement, des empilements de grille à forte stabilité thermique, contenant une couche intermédiaire de silicium amorphe entre le diélectrique de grille et le canal d'InGaAs sont étudiés. Ils démontrent une épaisseur de capacité équivalente (capacitance-equivalent thickness (CET)) inférieure à 14 Å mais semblent contenir une densité élevée de défauts d'interface ($D_{it}$).

Deuxièmement, le phénomène de récupération d'oxygène à distance appliqué aux oxydes natifs d'InGaAs est utilisé pour améliorer la stabilité thermique des empilements de grille sur InGaAs dans couche intermédiaire. Cette technique permet d'obtenir une réduction jusqu'à 5 Å de CET associée à une réduction de la $D_{it}$.

Finalement, basé sur ces résultats, un empilement de grille optimisé à base de déposition atomique assistée par plasma (PEALD) est présentée (Fig. D.3). Cette empilement n'utilise pas de couche intermediaire ni de préparation chimique de la surface. Il comprend une préparation par plasma d'hydrogène de la surface *in-situ*, une bi-couche d'$Al_2O_3/HfO_2$ et une grille métallique in-situ de TiN riche en Ti permettant d'utiliser la technique de récupération d'oxygène à distance. Cette empilement démontre une CET de 15.5 Å ainsi qu'une $D_{it}$ minimale inférieure à $5\times10^{11}$ $eV^{-1}cm^{-2}$ dans la partie haute de la bande interdite.

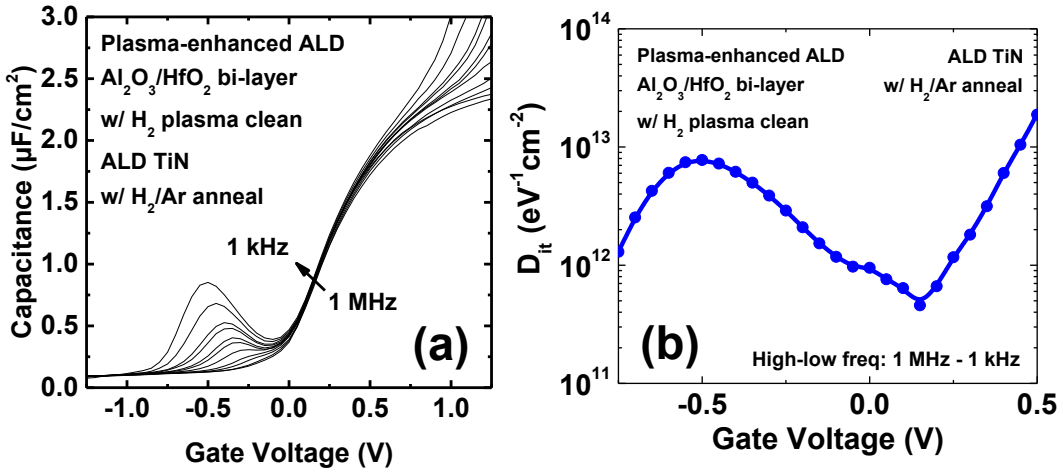



**Figure D.3:** (a) Caractéristique capacitance-voltage (C-V) multi-fréquence (de 1 MHz à 1 kHz) d'un metal-oxide-semiconductor capacitor (MOSCAP) avec un empilement de grille optimisé réalisé par plasma-enhanced atomic layer deposition (ALD) (PEALD), comprenant un nettoyage in-situ de la surface par plasma d'hydrogène, une bi-couche d'aluminum-oxide ($Al_2O_3$)/hafnium-oxide ($HfO_2$) et une grille métallique in-situ de titanium nitride (TiN) riche en Ti recuit sous atmosphère de $H_2$/Ar. (b) Profile de density of interface traps ($D_{it}$) vs tension de grille extrait par la méthode de la haute et basse fréquence entre 1 MHz et 1 kHz.

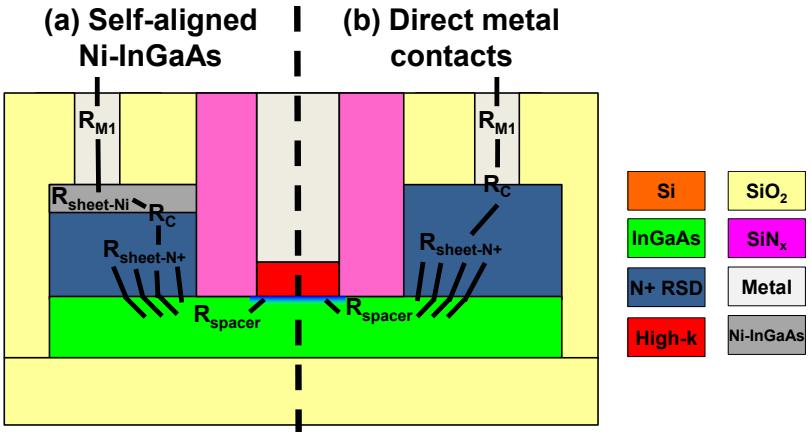



**Figure D.4:** Schéma d'un gate-first (GF) metal-oxide-semiconductor field-effect transistor (MOSFET) avec raised S/D (RSD) et (a) nickel-indium-galium-arsenide (Ni-InGaAs) ou (b) contacts métalliques directs avec la description des différentes contributions à la résistance série extrinsèque.

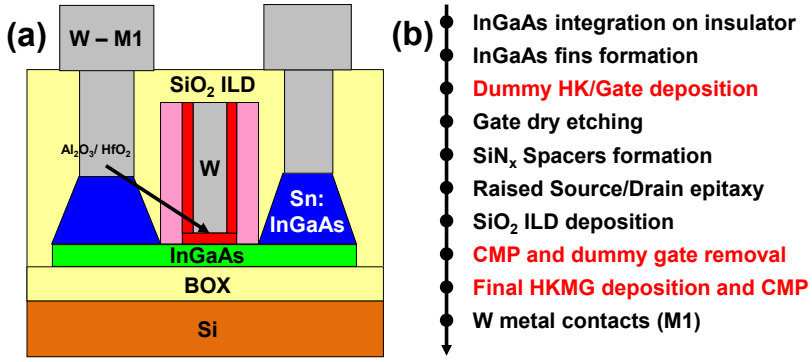



**Figure D.5:** (a) Schéma d'un replacement metal-gate (RMG) InGaAs-OI MOSFET et (b) procédé de fabrication RMG correspondant. En route sont représentées les étapes majeures qui diffèrent du procédé GF.

Différentes stratégies pour la réalisation de régions source/drain auto-alignées sont proposées (Fig. D.4). Elles se basent d'abord sur la croissance sélective de régions semi-conductrices fortement dopées (RSD). Les conditions de croissances sélective de ces régions sont explorées avec différents dopants. Le meilleur compromis est trouvé pour un dopage à l'etain à faible température, résultant en une densité volumique d'électrons supérieure à $5\times10^{19}$ cm$^{-3}$ obtenu à 500 °C.

Ces régions recrues (RSD) sont ensuite combinées avec un alliage de Ni-InGaAs auto-aligné, et comparé avec des contacts métalliques directs. Les meilleurs résultats sont obtenus avec l'utilisation de contacts métalliques directs à base de Mo et de W.

## D.4 Composants : Transistors auto-alignés compatibles CMOS à base d'InGaAs

Des transistors d'InGaAs auto-alignés et compatibles CMOS avec différentes architectures sont comparés : composants sur substrat massif vs sur isolant, planaire vs triple grille, grille en premier vs grille de remplacement, empilement de grille avec ou sans silicium amorphe, alliage Ni-InGaAs ou contacts métalliques directs. Des composants triple grille InGaAs sur Si optimisés avec une grille de remplacement, un empilement de grille déposé par couche atomique assistée par plasma et contacts métalliques directs (Fig. D.5) présentent des performances records (Fig. D.6).

Avec une longueur de grille de 50 nm et une largeur de fin de 15 nm, une pente sous le seuil de 80 mV/dec est obtenue avec un courant ON de 156 $\mu$A/$\mu$m à courant OFF fixé à 100 nA/$\mu$m et tension d'opération fixée à 0.5 V. L'utilisation d'une grille de remplacement

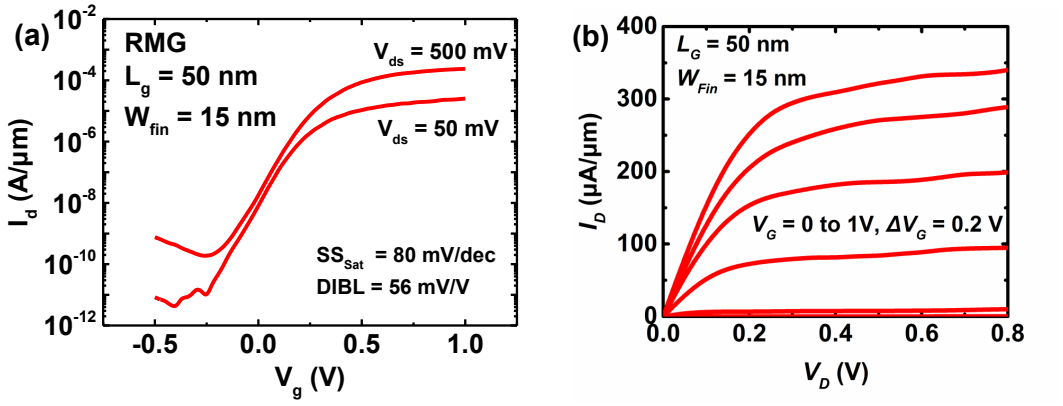



**Figure D.6:** Caractéristiques de (a) transfert et de (b) sortie d'un InGaAs RMG fin-based MOSFET (FinFET) ayant les dimensions suivantes : gate length ($L_G$) = 50 nm, $W_{fin}$ = 15 nm et $H_{fin}$ = 20 nm.

permet d'éviter que l'empillement de grille soit exposé au procédé de formation des RSD qui se déroule à haute température, ayant pour conséquence de dégrader la qualité de l'interface entre l'empilement de grille et le canal, tout en conservant la nature auto-alignée de l'architecture du composant.

## D.5 Circuits : Technologie CMOS hybride InGaAs/SiGe

La réalisation de circuits hybrides CMOS à base d'InGaAs et de SiGe présente de nombreux défis, illustrés dans la Fig. D.7: incompatibilité des budgets thermiques de fabrication idéaux, incompatibilités chimiques lors de nombreuses étapes de fabrication, et difficulté d'intégration de ces deux matériaux sur une même plateforme de Si.

Grâce aux techniques de collage pleine plaque (DWB) ou de surcroissance épitaxiale latérale confinée (CELO) introduites au chapitre 2, des circuits 2D coplanaire hybrides à base d'InGaAs et SiGe sont démontrés. Des inverseurs CMOS ainsi que des cellules mémoire de type 6T-SRAM sont obtenues avec succès (Fig. D.8), ce qui représente la première démonstration de circuits CMOS coplanaires hybrides InGaAs/SiGe sur Si.

Finalement, l'intégration monolithique 3D est proposée pour intégrer une couche "chaude" inférieure de transistors P en SiGe avec une couche "froide" supérieure de transistors N en InGaAs ; chaque couche faisant appel au procédé de fabrication optimisé respectif à chaque type de composant. Des performances excellentes sont obtenues pour chaque type de composants. De même, des inverseurs CMOS 3D sont démontrés.

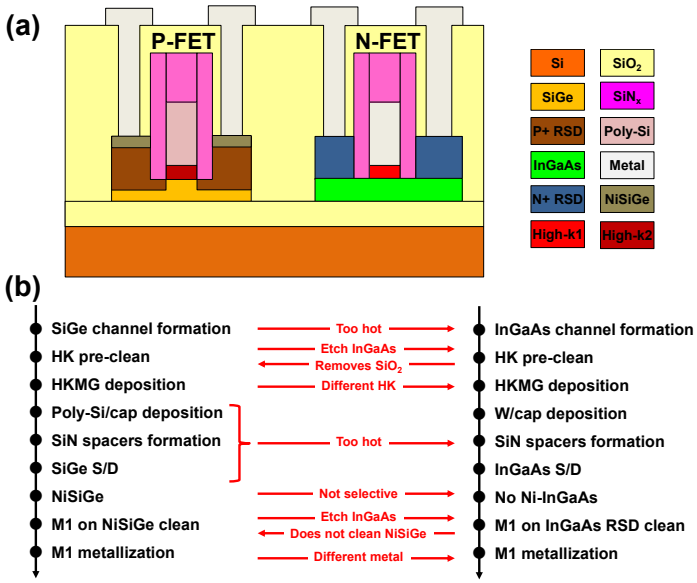



**Figure D.7:** (a) Schéma et (b) description du procédé de fabrication d'une technologie idéale CMOS hybride 2D à base d'InGaAs et de SiGe avec les meilleures conditions connues de fabrication pour les MOSFETs de type n et p. Les incompatibilités entre ces conditions idéales de fabrication pour chaque type de composants sont mises en évidence en rouge.

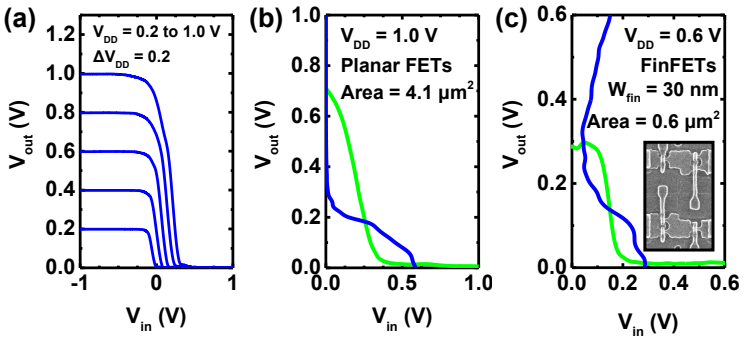



**Figure D.8:** (a, b, c) Caractéristiques de transfert en tension de circuits CMOS 2D hybrides à base d'InGaAs et de SiGe : (a) inverseur planaire avec $L_G = 115$ nm, (b) cellule static random access memory (SRAM) large en état de rétention avec des MOSFETs planaires et une taille de cellule de 4.1 $\mu m^2$, (c) cellule SRAM dense en état de rétention avec des FinFETs et une taille de cellule de 0.6 $\mu m^2$ (insert: Vue SEM du dessus d'une petite cellule SRAM avec des FinFET).

## D.6 Conclusion

En couvrant de manière transverse les aspects matériaux, modules, composants et circuits, ce travail entend faire avancer le développement et la compréhension de la technologie hybride CMOS à base d'InGaAs et de SiGe. Les solutions proposées aux problèmes posés tiennent compte des contraintes de production de masse requise pour une potentielle commercialisation de cette technologie à l'avenir.

Ce travail a montré qu'il n'y a plus de blocage techniques à la réalisation de transistors à base d'InGaAs dont les performances excèdent celles de transistors Si ; qu'il est désormais possible de co-intégrer de l'InGaAs et du SiGe sur Si pour la réalisation de circuits CMOS ; et que différentes méthodes sont possibles pour la démonstration de circuits hybrides CMOS se fondant sur ces matériaux.

À l'avenir, il comviendra de continuer à améliorer la résistance spécifique de contact entre le métal et les régions RSD ; de comprendre les implications de la fiabilité des empilements de grille sur InGaAs sur le fonctionnement des circuits ; d'étudier l'influence des défauts cristallins dans le canal d'InGaAs sur la variabilité des composants ; et d'améliorer la compatibilité des budgets thermiques pour la réalisation des composants de type n et de type p.

# List of Figures

1.1 Overview of different methods to integrate InGaAs on Si substrates. Images taken from: blanket and bonding [7], aspect ratio trapping (ART) from [8], epitaxial lateral overgrowth (ELO) from [9] and nanowire (NW) from [10]. 5

1.2 Transmission electron microscopy (TEM) cross-sectional view of GF fully-depleted silicon on insulator (FDSOI) n- and p-MOSFETs taken from [24]. 8

2.1 (a) Schematic process flow of the fabrication of ultra-thin body and buried oxide (BOX) (UTBB) InGaAs-OI substrates (1 to 5) and InGaAs regrowth module for S/D regions (6). (b) Picture of an InGaAs-OI substrate. . . . . 14

2.2 Ellipsometry thickness mapping of a 7 nm InGaAs (with 53% of indium) ($In_{0.53}Ga_{0.47}As$) active layer on a 10 nm BOX on Si after etch-stop removal. 15

2.3 (a) Calculated $2\theta$ (004) diffraction angle in high-resolution x-ray diffraction (XRD) for InGaAs of varying indium-content when fully relaxed (black squares) or fully strained to the lattice constant of indium-phosphide (InP) (red circles). (b) Magnified plot of (a) around the lattice matched conditions to InP. . . . . 17

2.4 High-resolution XRD $\omega - 2\theta$ scans on the (004) reflection of InGaAs-OI substrates with a high indium-content and various nominal thickness. The diffractometer is aligned to the InGaAs reflection which explains the low amplitude of the Si signal. . . . . 18

2.5 Bonding energy versus post-bonding annealing temperature for $Al_2O_3$-Si, $Al_2O_3$-$Al_2O_3$ and $SiO_2$-Si bonded pairs of wafers. No Plasma activation of the surface is done before DWB. For comparison, $SiO_2$-Si bonding energy data reported by SOITEC are included [51]. The red dashed line indicate the empirical minimal bonding energy required to enable device processing up to 600°C. . . . . 19

2.6 (a) Critical thickness in thermodynamic equilibrium [50] of InGaAs-OI on Si vs processing temperature. The strain is estimated from the processing temperature through thermal expansion mismatch assuming no relaxation in the BOX or at the bonding interface. (b) High resolution XRD $\omega - 2\theta$ scans on the (004) reflection of InGaAs-OI after layer transfer and (c) after about 50 nm in-situ Si doped $In_{0.53}Ga_{0.47}As$ regrowth by MOVPE at 600°C. 20

2.7 Atomic force microscopy (AFM) scans in tapping mode on the InGaAs surface after (a) growth on the donor wafer, (b) transfer to Si, (c) annealing at 600°C under tertiarybutylarsine (TBA) and (d) about 50 nm $In_{0.53}Ga_{0.47}As$ regrowth at 600°C. . . . . 21

2.8 (a) Process flow for the fabrication of InGaAs-OI on Si substrates by DWB using hydrogen-induced thermal splitting to release the donor wafer and enable its recycling. (b) Schematic of the functional structure of the donor wafer. . . . . 22

2.9 (a) SRIM [53] simulation of hydrogen dose implanted at 27 KeV in the III-V epi-stack. (b) Cross-sectional TEM image of the corresponding InP donor wafer with indium-aluminum-arsenide (InAlAs) (with 52% of indium) ($In_{0.52}Al_{0.48}As$) buffer, $In_{0.53}Ga_{0.47}As$ active layer and $Al_2O_3$ BOX layer after hydrogen implantation. . . . . 23

2.10 AFM scans in tapping mode on the surface of (a) the donor wafer after epitaxy, (b) target wafer after splitting, (c) target wafer after wet etching of the damaged splitting buffer, (d) after 600°C anneal of the transferred InGaAs-OI substrate, (e) donor wafer after splitting and (f) donor wafer after wet etching of the damaged splitting buffer and subsequent regrowth of the bonding stack. . . . . 24

2.11 (a) XRD $\omega - 2\theta$ scans on the (004) reflections of (i) the donor wafer as grown, (ii) 15 nm thick transferred InGaAs-OI after splitting and wet cleaning and (iii) after annealing at 600°C in TBA. (b) XRD $\omega - 2\theta$ scans on the (004) reflections of (iv) the donor wafer as grown (same as (i)), and (v) after splitting, cleaning and regrowth of the initial epitaxy stack. . . . . 25

2.12 (a) Schematic of the strain-relaxed buffer (SRB) donor wafer structure and process flow for the fabrication of large-scale InGaAs-OI substrates from Si donor wafers. (b) Photograph of a 200 mm InGaAs-OI on Si obtained by this method. . . . . 26

2.13 XRD $\omega-2\theta$ scans aligned on the (004) reflection of the InGaAs active layer after growth on Si (a), after bonding and etching of the Si donor wafer and of the Ge layer (b) and after removal of the galium-arsenide (GaAs) buffer and InAlAs grading buffer (c). XRD rocking curve ($\omega$ scans) of the (004) reflection of a finalized 200 mm InGaAs-OI substrate compared to a reference scan acquired on a InGaAs-OI layer bonded from an InP wafer. . 27

2.14 (a) AFM surface topography and corresponding roughness of the InGaAs-OI layer after growth and (b) after III-V CMP. (c) Spectroscopic ellipsometry thickness map on a nominally 30 nm thick 200 mm InGaAs-OI substrate. . . . . 28

2.15 (a) Schematic of the targetted hybrid dual-channel InGaAs/SiGe substrate. (b) Fabrication flow and (c) photograph of a final dual-channel substrate with a 6 nm thick InGaAs channel on a 10 nm $Al_2O_3$ BOX on a 8 nm thick SiGe channel on a 25 nm $SiO_2$ BOX on Si. . . . . 29

2.16 AFM scans on (a) the initial SiGe surface and on (b) the InGaAs layer of the hybrid dual-channel substrate. (c) XRD $\omega-2\theta$ scan aligned on Si (004) of the dual-channel substrate comprising both InGaAs and SiGe channels. Grey dashed lines represent theoretical peak positions for InGaAs with 53% Indium and SiGe with 25% Germanium. The inset shows the InGaAs diffraction pattern on the same wafer but aligned on the InGaAs (004) reflection to resolve the finite-size oscillations. . . . . 29

2.17 Schematic of the CELO integration scheme. (a) An empty $SiO_2$ cavity on Si is formed which defines the final shape and thickness of the III-V layer. (b) III-V epitaxy starts vertically from the Si seed and (c) continues laterally towards the cavity openings. (d) Once the cavity is filled, (e) $SiO_2$ top layer is removed and the III-V layer is patterned into final n-MOSFET active regions. . . . . 32

2.18 Process flow for the fabrication of empty $SiO_2$ cavities on Si fulfilling the requirements of the CELO integration scheme. . . . . 34

2.19 Top view SEM image and associated schematic of CELO structures (a) before and (b) after $In_{0.7}Ga_{0.3}As$ selective epitaxy by MOVPE. . . . . 35

2.20 Cross-sectional TEM (a) along and (b) across the growth direction on 30 nm thick InP grown from a (111) Si seed on a 30 nm thick $SiO_2$ BOX. The inset cartoon presents the cutting direction as a blue dashed line. . . . . 36

2.21 (a) High-resolution TEM image on the seed region of the sample shown in Fig. 2.20(a). Blue arrows indicates the position of planar defects. (b) High-resolution scanning TEM (STEM) image of the Si/InP interface corresponding to the small blue dashed square in (a). (c) Highly magnified STEM image of a microtwin (MT). (d) Lattice mismatch map obtained by geometrical phase analysis (GPA) in the vincinity of the Si/InP interface. . 37

2.22 High-resolution STEM images (a) on the region corresponding to the onset of lateral growth (large blue dashed square in Fig. 2.21(a)) and (b) magnified view of the crystal structure. (c) Electron diffraction pattern acquired with a 50 nm apperture on a region away from the seed containing an InP/BOX/Si stack. . . . . 38

2.23 (a) STEM overview on a 30 nm thick and 2.5 $\mu$m long $In_{0.7}Ga_{0.3}As$ crystal grown from a (100) Si seed. (b) In- and Ga-content measured from energy dispersive X-ray spectroscopy (EDX) line scan on the L$\alpha$ line of In and K$\alpha$ line of Ga (white dashed scan line shown in (a)). (c) AFM scan on the surface of the sacrificial material as deposited and (d) on the InGaAs surface after growth and oxide cap removal. . . . . 39

3.1 (a) Energy band diagram of an InGaAs metal-oxide-semiconductor (MOS) stack summarizing the presence of interface states, border traps and fixed charges. (b, c, d) C-V characteristics at high (HF, full lines) and low (LF, dashed lines) frequencies for an ideal MOS interface (black curves), compared with an MOS stack containing (b) interface states, (c) border traps and (d) fixed charges. . . . . 44

3.2 Ga3p, Si2p and Al2p core level X-ray photoemission spectroscopy (XPS) spectra after (a) hydrogen plasma, (b) 1 nm Si, (c-d) 1 nm $Al_2O_3$, (e-g) 2 nm $HfO_2$, (h) post-metallization anneal at 550°C in Ar for 30 min. . . . . 47

3.3 (a) C-V characteristics of a W/2 nm $HfO_2$/1 nm $Al_2O_3$/1 nm amorphous silicon (a-Si)/$In_{0.53}Ga_{0.47}As$ MOS capacitor annealed at 550°C in Ar for 30 minutes and measured at 25°C in the dark from 1 kHz to 1 MHz. 100 kHz and 1 MHz curves are plotted with forward and reverse sweep. (b) $D_{it}$ versus gate voltage extracted by the high-low frequency method [77]. (c) CET measured at 1 MHz versus annealing temperature in Ar for 30 minutes. 48

3.4 (a) Split C-V characteristics of W/$HfO_2$/1 nm $Al_2O_3$/1 nm a-Si/$In_{0.53}Ga_{0.47}As$ MOSFETs with $HfO_2$ of nominally 5 nm and 2 nm annealed at 600°C for 15 minutes in the MOVPE system and measured at 25°C in the dark from 10 kHz to 1 MHz. (b) Effective mobility ($\mu_{eff}$) versus inversion-charge density ($N_{inv}$) for the same MOSFETs. The channel is 10 nm thick and non-intentionally doped (NID), on NID $In_{0.52}Al_{0.48}As$ on InP. . . . . 49

3.5 Gibbs free energy of oxidation per Oxygen atom plotted at 1 atm versus temperature for InGaAs oxides, high-k dielectrics ($HfO_2$, $Al_2O_3$), $SiO_2$, W oxides and titanium-oxide ($TiO_2$). Values calculated based on thermodynamic properties in [79, 80]. . . . . 51

3.6 (a) Ga3p and Si2p core level XPS spectra after (i) hydrogen plasma and 1 nm a-Si deposition, (ii) 1.3 nm $Al_2O_3$ and 2.4 nm $HfO_2$ deposition, (iv) post-metallization anneal at 525°C in Ar for 30 min. (b) MOSCAPs C-V characteristics at 1 MHz with two different gate metals (TiN and W). . . . 53

3.7 Multi-frequency C-V characteristics of MOSCAPs with (a) W and (b) TiN gate metal on 2 nm $HfO_2$/ 0.5 nm $Al_2O_3$/ n-type $In_{0.53}Ga_{0.47}As$, annealed at 425°C in Ar for 30 minutes. Measurements acquired at room temperature between 1 MHz and 2 kHz. . . . . 54

3.8 (a) CET versus annealing temperature in Ar for 30 minutes on MOSCAPs with W or TiN gate metal on 2 nm $HfO_2$/ 0.5 nm $Al_2O_3$/ n-type $In_{0.53}Ga_{0.47}As$. (b) $D_{it}$ versus annealing temperature for MOSCAPs with W or (c) TiN as gate electrode. . . . . 55

3.9 (a) Multi-frequency C-V characteristics from 1 MHz to 1 kHz of a MOSCAP with an optimized PEALD stack comprising an in-situ hydrogen-plasma surface clean, an $Al_2O_3/HfO_2$ bi-layer and in-situ Ti-rich TiN gate metal annealed in $H_2$/Ar. (b) Corresponding $D_{it}$ versus gate voltage profile extracted by the high-low frequency method between 1 MHz and 1 kHz. . . . 57

3.10 Schematic of a GF MOSFET with RSD and (a) Ni-InGaAs or (b) direct metal contacts with emphasis on the various contributions to external series resistance. . . . . 60

3.11 (a-o) XPS core levels of $Ga2p_{3/2}$, $In3d_{5/2}$, O1s, C1s and F1s recorded after different process steps. (1) Gate stack reactive ion etching (RIE), (2) Wet cleaning and (3) in-situ annealing at 500°C for 5 minutes. (p,q) (4×2) surface reconstruction recorded by reflection high-energy electron diffraction (RHEED) along the (p) [110] and (q) [1-10] azimuths of $In_{0.53}Ga_{0.47}As$ (001), after in-situ annealing at 500°C for 5 minutes. . . . . 62

3.12 (a) Hall electron density versus dopant to group-III flux ratio for *in-situ* doped 100 nm thick $In_{0.53}Ga_{0.47}As$ grown at 600°C with different n-type dopant species. The blue arrow indicates a Si doped sample grown at 550°C. (b) Magnified Hall electron density versus dopant to group-III flux ratio focusing on the high doping region, for different dopant species and growth temperatures. . . . . 64

3.13 Schematic of InGaAs MOSFETs at various stage of the self-aligned Ni-InGaAs contact formation process: (a) after Ni deposition, (b) after alloy formation by annealing and (c) after selective wet etching of unreacted Ni. 66

3.14 Back-side secondary ion mass spectrometry (SIMS) profile for 220 nm of $In_{0.53}Ga_{0.47}As$ on InP after deposition of 50 nm Ni, annealed at 350°C for 5 minutes. . . . . 67

3.15 (a) Sheet resistance ($R_{sheet}$) of Ni-InGaAs alloy (with 10 nm Ni deposition) as a function of annealing temperature for 5 minutes in vacuum; before and after selective wet etching of unreacted metal. (b) Specific contact resistance ($\rho_C$) of Ni-InGaAs to RSD as a function of annealing temperature, extracted on transfer length method (TLM) structures on samples with (blue stars) and without (black diamond-shaped dots) annealing $SiO_2$ cap. 68

3.16 SEM cross-section of a gate-patterned wafer after RSD epitaxy, Ni-alloying and unreacted Ni removal; showing Ni-InGaAs alloy and RSD self-aligned to the gate: (a) 10 nm Ni on 50 nm RSD annealed at 350°C for 5 minutes, (b) 25 nm Ni on 100 nm RSD with migration-optimized double-step anneal process. . . . . 70

4.1 (a) Schematic of a self-aligned GF InGaAs MOSFET integrated on a generic substrate. (b) Corresponding baseline GF process flow. . . . . 76

4.2 Schematic and TEM cross-sectional view of 3 types of self-aligned GF $In_{0.53}Ga_{0.47}As$ MOSFETs: (a) "bulk" devices with $t_{ch}$ = 10 nm, 1 nm a-Si/ 1 nm $Al_2O_3$/ 2 nm $HfO_2$ gate stack, Si-doped RSD, with or without Ni-InGaAs contacts ; (b) "on-insulator" devices with $t_{ch}$ = 10 nm on 5 nm InAlAs, 1 nm $Al_2O_3$/ 3 nm $HfO_2$ gate stack, Si-doped RSD ; (c) "optimized on-insulator" devices with $t_{ch}$ = 20 nm, 0.5 nm $Al_2O_3$/ 3 nm $HfO_2$ gate stack, Sn-doped RSD. . . . . 78

4.3 On-resistance versus gate length obtained on "bulk" MOSFETs with or without Ni-InGaAs contacts. The on-resistance is extracted from the drain current at gate voltage ($V_g$) = 1 V and drain-to-source voltage ($V_{ds}$) = 50 mV, normalized to 10 k$\Omega$.$\mu$m. . . . . 80

4.4 (a) Split C-V characteristics for the three GF device types measured at 1 MHz on MOSFETs with $L_G = 10$ $\mu$m. (b) Effective mobility versus channel charge density for the corresponding devices. . . . . 81

4.5 Drain (full lines) and Gate (dashed lines) currents versus gate voltage for GF short-channel MOSFETs of similar gate length for the three device architectures: (a) "bulk", (b) "on-insulator" and (c) "optimized on-insulator". 83

4.6 (a) subthreshold swing (SS) at $V_{ds} = 0.5$ V and (b) drain-induced barrier lowering (DIBL) versus $L_G$ for "bulk", "on-insulator" and "optimized on-insulator" devices. . . . . 84

4.7 (a) $R_{sheet}$, (b) contact resistance ($R_C$) and transfer length ($L_t$) versus contact size contact length ($L_C$) extracted from TLM structures of different contact size and spacing. . . . . 85

4.8 (a) Tilted and top view SEM of a tight-pitch "optimized on-insulator" GF MOSFET featuring a gate length of 30 nm, contact size of 50 nm and contact pitch of 120 nm. (b) Corresponding transfer characteristics of the device. . . . . 85

4.9 (a) Schematic of a junction-less (JL) InGaAs MOSFET on insulator on Si. (b) Corresponding JL process flow. (c) Tilted SEM image of a JL device after gate patterning on InGaAs fins. . . . . 87

4.10 Transfer characteristics measured at $V_{ds} = 0.5$ V, on devices featuring a $L_G$ of 10 $\mu$m, $H_{fin} = 20$ nm and $W_{fin}$ ranging from 50 to 200 nm. Plotted in (a) log scale with SS vs $W_{fin}$ in inset and (b) linear scale with source and drain series resistance ($R_{SD}$) vs $W_{fin}$ in inset. . . . . 88

4.11 (a) Transfer characteristics measured at $V_{ds}$ of 50 mV and 0.5 V on long-channel (10 $\mu$m) tri-gate InGaAs-OI JL MOSFETs before and after hydrogen ($H_2$)/Ar anneal. (b) SS at $V_{ds} = 50$ mV versus $L_G$ roll-off characteristic before and after $H_2$/Ar anneal. . . . . 89

4.12 (a) Schematic of a self-aligned RMG InGaAs-OI MOSFET and (b) corresponding baseline RMG process flow. Highlighted in red are the major steps which differ from the baseline GF process shown in Fig. 4.1. . . . . 90

4.13 (a, b, c, d) SEM views taken at different critical stages of the RMG process: (a) after InGaAs fin patterning, (b) after $SiO_2$ interlayer dielectric (ILD) chemical-mechanical polishing (CMP) exposing the top of the dummy gates, (c) after removal of the dummy gate and dummy high-k (HK), (d) after final high-k metal-gate (HKMG) deposition, W fill and metal CMP. (e, f) Cross sectionnal TEM image of a RMG InGaAs-OI MOSFET taken (e) across and (f) along the gate. Side insets show the scaled 12 nm thick silicon-nitride ($SiN_x$) spacers and 15 nm wide InGaAs fins. . . . . 91

4.14 (a) Split C-V characteristics for a planar RMG MOSFET measured from 1 MHz down to 3 kHz. (b) Effective mobility versus channel charge density for the corresponding devices. . . . . 92

4.15 (a) Transfer and (b) characteristic of an InGaAs RMG FinFET featuring $L_G$ = 50 nm, $W_{fin}$ = 15 nm and $H_{fin}$ = 20 nm. . . . . 93

4.16 (a) SS in saturation ($V_{ds}$ = 0.5 V) and DIBL versus $L_G$ roll-off characteristics for GF planar MOSFETs, GF FinFETs and RMG FinFETs. . . . . 94

4.17 (a) On-current ($I_{on}$) at fixed off-current ($I_{off}$) = 100 nA/$\mu$m and operating voltage ($V_{DD}$) = 0.5 V versus $L_G$ for different $W_{fin}$ varying from 15 nm to 75 nm. (b) Best $I_{on}$ at fixed $I_{off}$ = 100 nA/$\mu$m and $V_{DD}$ = 0.5 V versus $L_G$ for FinFETs reported in this study (filled symbols) (RMG by DWB (red stars), GF by DWB (blue diamond) and GF by CELO (orange hexagon)) benchmarked against CMOS compatible InGaAs MOSFETs on Si in litterature (open symbols) [8, 110–112] having different architectures ((GF, RMG or gate-last (GL) ; FinFET, planar (PL) or gate-all-around (GAA))). . . . . 95

4.18 (a) Schematic of a self-aligned GF InGaAs-OI FinFET integrated on Si by the CELO technique and (b) corresponding baseline process flow. . . . . 96

4.19 (a, b) Tilted SEM images of GF FinFETs with $W_{fin}$ = 35 nm (a) after spacer etch and (b) after RSD. (c, d, e) Corresponding cross-sectional TEM images (c, e) across the gate and (d) across the 25 nm x 35 nm fins. . . . . 97

4.20 (a,b) Transfer characteristics of two InGaAs GF FinFET integrated on Si by CELO (a) without or (b) with RSD. (c) Output characteristics of the corresponding device with RSD. $L_G$ = 50 nm, $W_{fin}$ = 50 nm and $H_{fin}$ = 25 nm. . . . . 98

5.1 (a) Schematic and (b) process flow description of an ideal 2D hybrid InGaAs/SiGe CMOS technology with representative best-known process for n- and p-MOSFETs. Non-compatible process modules are highlighted in red in the process flow description. . . . . 101

5.2 Process flow description for the 2D co-planar co-integration of InGaAs n-MOSFETs and SiGe p-MOSFETs with a common front-end (a,b,c,d,e) based on hybrid dual-channel substrates obtained by DWB. . . . . 102

5.3 (a) Top-view SEM micrograph of a dense inverter chain after gate patterning. (b, c, d) TEM cross-sections of n- and p-MOSFETs at different stages of the process: (b) n- and p-MOSFETs before spacer formation (Fig. 5.2(c)), (c) p-MOSFET with $L_G$ = 65 nm after the front-end (Fig. 5.2(d)), (d) n-MOSFET with $L_G$ = 40 nm after M1 (Fig. 5.2(e)). . . 103

5.4 (a, b) Transfer characteristics obtained on isolated SiGe and InGaAs MOSFETs from the initial CMOS process for: (a) short-channel SiGe p-MOSFET with $L_G$ = 65 nm and (b) short-channel InGaAs n-MOSFET with $L_G$ = 40 nm. (c) Transfer characteristics obtained on isolated InGaAs n-MOSFETs with $L_G$ = 500 nm, comparing the initial and improved CMOS process. (d) threshold voltage ($V_T$) vs body bias in linear regime on short-channel InGaAs p-MOSFETs with $L_G$ = 40 nm, comparing the initial and improved CMOS process. (e) Transfer characteristics versus body bias obtained on an isolated InGaAs MOSFETs with $L_G$ = 40 nm. . . . . 105

5.5 (a) SS in saturation and (b) DIBL versus $L_G$ for InGaAs n-MOSFETs of the improved CMOS process, some devices are reported for different body bias. (c) SS in saturation and (d) DIBL versus body bias for an InGaAs n-MOSFET with $L_G$ = 40 nm. . . . . 105

5.6 (a) Comparison of voltage transfer characteristics and (b) voltage transfer gain for inverters built with the initial or improved CMOS process. (c) Voltage transfer characteristics versus body bias for an inverter built with the improved CMOS process. . . . . 107

5.7 Process flow schematic and description for the 2D co-planar co-integration of InGaAs n-MOSFETs and SiGe p-MOSFETs with a common front-end based on selective epitaxy of InGaAs in empty $SiO_2$ cavities. . . . . 109

5.8 (a, b, c, d) Top view SEM images of dense 6-transistors (6T)-SRAM arrays at various stages of the hybrid InGaAs/SiGe CMOS fabrication process: (a) after sacrificial material patterning, (b) after the formation of empty cavities, (c) after decaping selectively grown InGaAs and (d) after completing the front-end-of-line (FEOL) process. All images are taken on dense SRAM arrays having a cell size below 0.45 $\mu m^2$. (e) TEM cross-sectional image taken along the gate of an inverter of a dense SRAM cell (red-dashed line in SRAM layout shown in the top-left inset). Dashed blue rectangular inset (bottom left): High-resolution dark-field TEM image with emphasis on HK layers. (f, g) TEM cross-sectional images taken across the gates ($L_G$ = 55 nm) for GF (f) SiGe p-MOSFET and (g) InGaAs n-MOSFET. . . . . 110

5.9 (a, b) Transfer and (c, d) output characteristics of short-channel (a, c) SiGe p-MOSFET and (b, d) InGaAs n-MOSFET with $L_G = 35$ nm. (e) Transfer characteristic of a long-channel InGaAs n-MOSFET with $L_G$ = 115 nm. (f) SS versus $L_G$ plots in linear and saturation regime. . . . . 112

5.10 (a, b, c) Voltage transfer characteristics of hybrid InGaAs/SiGe CMOS (a) planar inverter with $L_G = 115$ nm, (b) large SRAM cell in "hold" state with planar MOSFETs and cell area of 4.1 $\mu m^2$, (c) dense SRAM cell in "hold" state with FinFETs cell area of 0.6 $\mu m^2$ (inset: SEM top view of the small FinFET-based SRAM cell). . . . . 113

5.11 Illustration of thermal budget evolution versus processing steps for 3D monolithic integration of (a) SiGe or Si MOSFETs on top of Si MOSFETs and of (b) InGaAs MOSFETs on top of SiGe or Si MOSFETs. . . . . 115

5.12 (a) Schematic and (b) process flow description for the 3D monolithic co-integration of "hot" bottom GF SiGe p-MOSFETs and "cold" top RMG InGaAs n-MOSFETs on a Si substrate by DWB. . . . . 116

5.13 (a) Photograph of InGaAs bonded on top of processed SiGe devices for 3D monolithic CMOS circuits. (b, c, d, e) Cross-section TEM images of: (a) InGaAs n-FinFET layer on SiGe p-FinFET layer seen along the stacked p- and n-gates, (b) zoom-in on an 8 nm wide SiGe fin, (c) a 30 nm wide InGaAs fin, and (d) cross section along InGaAs channel. . . . . 117

5.14 (a) Transfer characteristics, (b) SS and (c) DIBL roll-off curves versus $L_G$ for SiGe p-FinFETs before and after top n-MOSFETs fabrication. Roll-off characteristics are also compared to previous reports on similar devices [26, 27]. . . . . 118

5.15 (a) Transfer characteristics, (b) SS and (c) DIBL versus $L_G$ for planar InGaAs n-MOSFETs on the top layer, before and after an $H_2$/Ar anneal. Roll-off characteristics are compared to optimized InGaAs RMG FinFETs from Chapter 4 section 4.3.2. . . . . 119

5.16 (a, b) Voltage transfer characteristics of hybrid 3D monolithic InGaAs/SiGe CMOS inverters with p-$L_G$ = 30 nm and (a) n-$L_G$ = 80 nm or (b) n-$L_G$ = 30 nm. . . . . 120

D.1 (a) Procédé de fabrication de substrats InGaAs-OI sur Si par DWB en utilisant la séparation induite par implantation d'hydrogène pour recycler le substrat donneur. (b) Schéma fonctionel de la structure du substrat donneur. . . . . 141

D.2 Vue SEM du dessus et schémas associés de structures CELO (a) avant et (b) après la croissance séléctive d'$In_{0.7}Ga_{0.3}As$ par MOVPE. . . . . 142

D.3 (a) Caractéristique C-V multi-fréquence (de 1 MHz à 1 kHz) d'un MOSCAP avec un empilement de grille optimisé réalisé par PEALD, comprenant un nettoyage in-situ de la surface par plasma d'hydrogène, une bi-couche d'$Al_2O_3$/$HfO_2$ et une grille métallique in-situ de TiN riche en Ti recuit sous atmosphère de $H_2$/Ar. (b) Profile de $D_{it}$ vs tension de grille extrait par la méthode de la haute et basse fréquence entre 1 MHz et 1 kHz. . . . . 143

D.4 Schéma d'un GF MOSFET avec RSD et (a) Ni-InGaAs ou (b) contacts métalliques directs avec la description des différentes contributions à la résistance série extrinsèque. . . . . 143

D.5 (a) Schéma d'un RMG InGaAs-OI MOSFET et (b) procédé de fabrication RMG correspondant. En route sont représentées les étapes majeures qui diffèrent du procédé GF. . . . . 144

D.6 Caractéristiques de (a) transfert et de (b) sortie d'un InGaAs RMG FinFET ayant les dimensions suivantes : $L_G$ = 50 nm, $W_{fin}$ = 15 nm et $H_{fin}$ = 20 nm. . . . . 145

D.7 (a) Schéma et (b) description du procédé de fabrication d'une technologie idéale CMOS hybride 2D à base d'InGaAs et de SiGe avec les meilleures conditions connues de fabrication pour les MOSFETs de type n et p. Les incompatibilités entre ces conditions idéales de fabrication pour chaque type de composants sont mises en évidence en rouge. . . . . 146

D.8 (a, b, c) Caractéristiques de transfert en tension de circuits CMOS 2D hybrides à base d'InGaAs et de SiGe : (a) inverseur planaire avec $L_G$ = 115 nm, (b) cellule SRAM large en état de rétention avec des MOSFETs planaires et une taille de cellule de 4.1 $\mu$m$^2$, (c) cellule SRAM dense en état de rétention avec des FinFETs et une taille de cellule de 0.6 $\mu$m$^2$ (insert: Vue SEM du dessus d'une petite cellule SRAM avec des FinFET). . . . . 146

# List of Tables

3.1 $\rho_C$ obtained from TLM measurements for different metals on 100 nm thick Si-doped $In_{0.53}Ga_{0.47}As$ at $2\times10^{19}$ $cm^{-3}$. . . . . 72

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# Abstract / Résumé


## Title: Hybrid InGaAs/SiGe Technology Platform for CMOS Applications

High-mobility channel materials such as indium-galium-arsenide (InGaAs) and silicon-germanium (SiGe) alloys are considered to be the leading candidates for replacing silicon (Si) in future low power complementary metal-oxide-semiconductor (CMOS) circuits. Numerous challenges have to be tackled in order to turn the high-mobility CMOS concept into an industrial solution. This thesis addresses the majors challenges which are the integration of InGaAs on Si, the formation of high-quality gate stacks and self-aligned source and drain (S/D) regions, the optimization of self-aligned transistors and the co-integration of InGaAs and SiGe into CMOS circuits. All investigated possible solutions are proposed in the framework of very-large-scale integration requirements.

Chapter 2 describes two different methods to integrate InGaAs on Si. Chapter 3 details the developments of key process modules for the fabrication of self-aligned InGaAs metal-oxide-semiconductor field-effect transistors (MOSFETs). Chapter 4 covers the realization of various types of self-aligned MOSFETs towards the improvement of their performance. Finally, chapter 5 demonstrates three different methods to make hybrid InGaAs/SiGe CMOS circuits.

## Titre: Filière Technologique Hybride InGaAs/SiGe pour Applications CMOS

Les materiaux à forte mobilité comme l'InGaAs et le SiGe sont considérés comme des candidats potentiels pour remplacer le Si dans les circuits CMOS futurs. De nombreux défis doivent être surmontés pour transformer ce concept en réalité industrielle. Cette thèse couvre les principaux challenges que sont l'intégration de l'InGaAs sur Si, la formation d'oxydes de grille de qualité, la réalisation de régions source/drain auto-alignées de faible résistance, l'architecture des transistors ou encore la co-intégration de ces matériaux dans un procédé de fabrication CMOS. Les solutions envisagées sont proposées en gardant comme ligne directrice l'applicabilité des méthodes pour une production de grande envergure.

Le chapitre 2 aborde l'intégration d'InGaAs sur Si par deux méthodes différentes. Le chapitre 3 détaille le développement de modules spécifiques à la fabrication de transistors auto-alignés sur InGaAs. Le chapitre 4 couvre la réalisation de différents types de transistors auto-alignés sur InGaAs dans le but d'améliorer leurs performances. Enfin, le chapitre 5 présente trois méthodes différentes pour réaliser des circuits hybrides CMOS à base d'InGaAs et de SiGe.