



HAL
open science

Etude et amélioration de l'électromigration pour améliorer la durée de vie des interconnexions des technologies CMOS

Giulio Marti

► **To cite this version:**

Giulio Marti. Etude et amélioration de l'électromigration pour améliorer la durée de vie des interconnexions des technologies CMOS. Autre. Université Grenoble Alpes, 2016. Français. NNT : 2016GREAI111 . tel-01844256

HAL Id: tel-01844256

<https://theses.hal.science/tel-01844256>

Submitted on 19 Jul 2018

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

THÈSE

Pour obtenir le grade de

DOCTEUR DE LA COMMUNAUTÉ UNIVERSITÉ GRENOBLE ALPES

Spécialité : **Matériaux, Mécanique, Génie civil, Electrochimie**

Arrêté ministériel : 7 août 2006

Présentée par

Giulio MARTI

Thèse dirigée par **Yves WOUTERS** et
codirigée par **Lucile ARNAUD**

préparée au sein du **Laboratoire SiMaP**
dans l'**École Doctorale IMEP²**

Interconnections: Copper and Low K Dielectrics - lifetime optimisation by improvement of electromigration understanding

Thèse soutenue publiquement le « **2 Décembre 2016** »,
devant le jury composé de :

M. Michel PONS

Directeur de Recherche CNRS, SIMAP

(Président)

Mme Helene FREMONT

Ingénieur Docteur à IMS,

(Rapporteur)

M. Roland FORTUNIER

Professeur, ENISE,

(Rapporteur)

M. Yves WOUTERS

Professeur, SIMAP,

(Directeur de thèse)

Mme. Lucile ARNAUD

Ingénieur Docteur à CEA-Leti,

(Co-encadrant)

M. David Ney

Ingénieur à STmicroelectronics

(invité)



CONTENTS

1 INTRODUCTION	1
1.1 CONTEXT	1
1.2 INTERCONNECT STRUCTURES IN MICROELECTRONICS	2
1.3 COPPER BASED INTERCONNECTION FABRICATION	4
1.4 FAILURE MECHANISM IN INTERCONNECT	5
1.5 ELECTROMIGRATION INDUCED FAILURES	6
1.6 HISTORIC OUTLINE OF ELECTROMIGRATION	7
1.6.1 <i>Black's equation</i>	7
1.6.2 <i>Blech effect</i>	9
1.7 OUTLINE OF THIS THESIS	12
2 ELECTRICAL CHARACTERIZATION ERROR! BOOKMARK NOT DEFINED.	
2.1 OBJECTIVES	35
2.2 ELECTRICAL CHARACTERIZATION	35
2.3 TEST STRUCTURES.....	38
2.3.1 <i>Single standard via</i>	40
2.3.2 <i>Local sense structure description</i>	42
2.4 BLACK PARAMETERS EXTRACTION.....	46
2.5 RESISTANCE LOWERING FITTING	48
2.5.1 <i>R_{slopes} of heat treated and not heat treated devices</i>	51
2.6 FOCUSED DESIGN STUDY	52
2.6.1 <i>1st Study: Microstructure study of the line width transition [BS vs TS]</i>	53

2.6.2	<i>2nd Study: Local Blech effect [BS vs CS]</i>	56
2.6.3	<i>3rd Study: width influence on lifetime [BS]</i>	59
2.6.4	<i>Conclusions</i>	59
2.7	EFFECTIVE CHARGE EXPERIMENTAL EVALUATION	60
3	PHYSICS OF ELECTROMIGRATION	35
3.1	THE ELECTROMIGRATION DRIVING FORCE	15
3.2	DIFFUSIVITY PATHS	17
3.3	ELECTROMIGRATIONS INDUCED MATERIAL TRANSPORT	19
3.4	ELECTROMIGRATION AND MECHANICAL STRESS (BLECH EFFECT)	22
3.5	BLECH EFFECT	23
3.6	MODELS OF STRESS BUILD-UP DUE TO ELECTROMIGRATION	25
3.7	VOID NUCLEATION	29
3.8	VOID EVOLUTION	31
4	SIMULATIONS STUDIES OF ELECTROMIGRATION	65
4.1	THE ELECTRO-THERMAL PROBLEM	66
4.2	MATERIAL TRANSPORT EQUATIONS	67
4.3	ELECTROMIGRATION INDUCED STRESS	68
4.3.1	<i>Strain due to Vacancy Migration</i>	69
4.3.2	<i>Strain due to Vacancy Generation/Annihilation</i>	70
4.3.3	<i>Total Electromigration Strain</i>	70
4.4	MECHANICAL DEFORMATION	71
4.5	MODEL SIMPLIFICATIONS	73
4.6	MODEL SUMMARY	73
4.7	MODEL NUMERICAL IMPLEMENTATION	74
4.8	SIMULATION STUDIES OF ELECTROMIGRATION	77
4.9	MATERIAL AND SIMULATION PARAMETERS	77
4.10	SITES OF VOID NUCLEATION	78
4.11	CRITICAL STRESS OF VOID FORMATION EXTRAPOLATION	79
4.12	FOCUSED DESIGN TEST STRUCTURES	80
4.13	INITIAL CONCENTRATION IMPACT	84
5	CONCLUSIONS	88
	REFERENCES	92

LIST OF TABLES

TABLE 3-1: PERCENTAGE TO CATCH ELECTRICALLY A VOID IN FUNCTION OF THE DISTANCE OF THE VOLTAGE VIA AND TEMPERATURE.....	45
TABLE 3-2: ENERGY ACTIVATION E_A AND CURRENT ACCELERATION FACTOR N.....	48
TABLE 3-3: SLOPES AT 300 °C OF SSV SAMPLES HEAT TREATED (BAKED FOR 800 H AT 300°C) AND NOT HEAT TREATED.	51
TABLE 3-4: SUMMARY GEOMETRICAL TEST STRUCTURES PARAMETERS AND THE RELATIVE MEAN TIME FAILURE (MTTF) AND MEAN OF R_{SLOPE}	53
TABLE 3-5: GEOMETRICAL TEST STRUCTURES PARAMETERS OF 1ST STUDY.....	54
TABLE 3-6: MTF AND MEAN OF RSLOPE OF BS1 AND TS	56
TABLE 3-7: GEOMETRICAL TEST STRUCTURES PARAMETERS OF 2ND STUDY ORDERED ACCORDING L1 ASCENDING.	56
TABLE 3-8: GEOMETRICAL TEST STRUCTURES PARAMETERS OF 3RD STUDY.....	59
TABLE 3-9: MTF AND MEAN R_{SLOPE} OF BS1 AND BS3, SAME L1 AND L2 (10 μ M) WITH A WIDTH OF 3 W1 AND 2 W1 RESPECTIVELY.....	59
TABLE 3-10: SUMMARY OF VOLUMES OF SATURATION V_{SAT} AND RELATIVES CHARGE EFFECTIVES Z^* FOUND.	62
TABLE 4-1: THE TOTAL VACANCY FLUX IS THE SUM OF FOUR CONTRIBUTORS	67
TABLE 4-2: MODEL SUMMARY.....	74
TABLE 4-3: DEFORMATION AND MECHANICAL STRESS	74

LIST OF FIGURES

FIGURE 1-1: CROSS-SECTION OF BACK-END STRUCTURE, SHOWING INTERCONNECTS, CONTACTS AND VIAS, SEPARATED BY DIELECTRIC LAYERS.	3
FIGURE 1-2: SINGLE AND DUAL DAMASCENE STRUCTURE [6].	5
FIGURE 1-1-3: THE TWO FORCE OF EM.	6
FIGURE 1-4: SCHEMATIC DESIGN OF A COMSOL TOOL FOR EM SIMULATION.	12
FIGURE 2-1: DIFFUSION PATHS OF LATTICE, GRAIN BOUNDARIES, MATERIAL INTERFACES AND DISLOCATIONS FOR A DUAL-DAMASCENE INTERCONNECT	18
FIGURE 2-2: EVOLUTION OF THE INCREMENT OF THE VACANCY CONCENTRATION ($C_V/C_{V0}-1$) AT $x=0$ WITH C_V AS THE VACANCY CONCENTRATION AND C_{V0} THE INITIAL VACANCY CONCENTRATION.	26
FIGURE 2-3: STRESS BUILD-UP AT $x = 0$ ACCORDING TO KORHONEN'S MODEL.....	28
FIGURE 2-4: STRESS BUILD-UP ALONG THE INTERCONNECT AT DIFFERENT TIMES.	29
FIGURE 2-5: SCHEMATIC OF VOID NUCLEATION AT AN INTERFACE SITE OF WEAK ADHESION.	30
FIGURE 3-1: EXAMPLE OF ESTIMATION OF TTF DISTRIBUTION IN OPERATIVE CONDITIONS KNOWING THE ENERGY OF ACTIVATION (E_A) AND THE FACTOR OF CURRENT (N).....	36
FIGURE 3-2: RESISTANCE VERSUS TIME CURVE OF CLASSIC STRUCTURE (SSV) THAT IS SUBJECTED TO ELECTROMIGRATION STRESS. DIFFERENT PHASES OF THE DEGRADATION PROCESS, REPRESENTING THE EVOLUTION OF THE DEGRADATION OF THE TEST LINE, ARE SHOWN.	37
FIGURE 3-3: TEST LINE SCHEME.	38
FIGURE 3-4: IN THE EXAMPLE IS SHOWN A CROSS SECTION TEM ANALYSIS CENTERED ON THE CATHODE VIA ON THE TECHNOLOGY DUAL DAMASCENE CU LINE EMBEDDED IN LOW-K DIELECTRIC OF THE CMOS 28NM TECHNOLOGY PROCESS, WHICH INCLUDES A CUMN SEED LAYER. IN THE FIGURE, IT IS POSSIBLE TO CLEARLY DISTINGUISH THE SiCN BARRIER AND Ta/TaN BARRIER.....	39
FIGURE 3-5: TEST LINE SCHEME SEEN ABOVE SHOWING THE EXTRUSION DETECTORS.	40
FIGURE 3-6: SINGLE STANDARD VIA (SSV) DUAL DAMASCENE CU LINE DOWNSTREAM CONFIGURATION.	41
FIGURE 3-7: ELECTROMIGRATION DEGRADATION DURING THE STRESS IS FOLLOWED BY MONITORING THE RESISTANCE EVOLUTION OF THE LINE WITH TIME. THE FAILURE TIME (TTF) IS RECORDED FOR EACH TESTED LINE AT THE RESISTANCE STEP INCREASE	

OF 5% OF THE INITIAL RESISTANCE. THE JUMP STEP OF RESISTANCE IS PROPORTIONAL TO THE LENGTH OF THE VOID.	41
FIGURE 3-8: EXPERIMENTAL GRAPHICAL EXAMPLE THAT SHOWS THE METHODOLOGY TO CALCULATE R_{SLOPE} AND V_D	42
FIGURE 3-9: TEST STRUCTURE USED A) STANDARD SINGLE-VIA (SSV) EM-STRUCTURE AND B) LOCAL SENSE STRUCTURE (LSS) TEST STRUCTURE WITH VOLTAGE-SENSES CLOSER TO THE VIA.	43
FIGURE 3-10: COMPARATIVE GRAPH OF RESISTANCE VERSUS STRESS TIME FOR A SINGLE STANDARD VIA (SSV) AND LOCAL SENSE STRUCTURE (LSS).	43
FIGURE 3-11: EXAMPLE OF A RESISTANCE VERSUS TIME CURVE FOR LSS 1, 2, 3: SAMPLES WITH THE TERMINAL OF POTENTIAL AT 0.35 μM FROM THE ANODE 4,5,6: SAMPLES WITH THE TERMINAL OF POTENTIAL AT 0.7 μM	44
FIGURE 3-12: TEM OF LSS AFTER EM TEST A) SAMPLE WITHOUT VOID BETWEEN THE VOLTAGE SENSES B) SAMPLE WITH VOID BETWEEN THE VOLTAGE SENSES.	44
FIGURE 3-13: TEM OF LSS AFTER EM TEST STOPPED JUST AFTER A SMALL POSITIVE VARIATION OF RESISTANCE.	45
FIGURE 3-14: CHEN IRPS2015 [84] TEST STRUCTURE SCHEME. THIS STRUCTURE ALLOWS FOLLOWING THE EVOLUTION OF RESISTANCE LOCALLY BETWEEN 2 VOLTAGE TAPS.	46
FIGURE 3-15: TIME TO FAILURE (TTF) AND TIME OF NUCLEATION (TN) CALCULATED RESPECTIVELY WITH THE SSV AND THE LSS AT ACCELERATED AT CONSTANT CURRENT CONDITIONS FOR 300 °C AND 330 °C.	47
FIGURE 3-16: TIME TO FAILURE (TTF) AND TIME OF NUCLEATION (TN) CALCULATED RESPECTIVELY WITH THE SSV AND LSS AT ACCELERATED CONDITIONS AT CONSTANT TEMPERATURE WITH CURRENTS $J_2 > J_1$	48
FIGURE 3-17: EXAMPLE OF RESISTANCE VERSUS TIME (NO CURRENT) FITTED BY DECREASING EXPONENTIAL LAW.	49
FIGURE 3-18: CUMULATIVE FUNCTION DISTRIBUTION (CFD) OF AMPLITUDE (A) IN ABSENCE OF CURRENT ($J=0$) AND WITH CURRENT = J_1), LINES REPRESENT THE 90 % CONFIDENCE LEVEL (C.L.) OF THE DATA.	50
FIGURE 3-19: CUMULATIVE FUNCTION DISTRIBUTION (CFD) OF CONSTANT DECAY VALUE (T_c) IN ABSENCE OF CURRENT ($J=0$) AND WITH CURRENT = J_1	50
FIGURE 3-20: EXAMPLE OF RESISTANCE VERSUS STRESS TIME FOR A SSV HEAT TREATED AND NOT HEAT TREATED STRUCTURE TEST LINE.	51
FIGURE 3-21: TEST STRUCTURE USED A) CONSTANT REFERENCE STRUCTURE (CS) EM-	

STRUCTURE USED TO HAVE TIME TO FAILURE FOR THE REF B) BOTTLE STRUCTURE BS	
C) TRIDENT-STRUCTURE TS	53
FIGURE 3-22: 1 ST STUDY: CUMULATIVE FUNCTION DISTRIBUTION (CFD): A) TIME TO FAILURE (TTF) CALCULATED WITH BS1 AND TS RESPECTIVELY.B) R_{SLOPE} COMPARISON OF BS1 AND TS.	54
FIGURE 3-23: [83] (STEM TOP) MICROSTRUCTURE DESCRIPTION IN A BS SAMPLE. THE POLYCRYSTALLINE PROFILE IS SEEN IN THE NARROWER REGION WHILE THE BAMBOO PROFILE IS OBSERVED IN THE WIDER SEGMENT (55 NM NODE SAMPLE). (VERY LOW ANGLE ANNULAR DARK FIELD VLAADF BOTTOM) EVIDENCE OF A VOID LOCATED IN THE POLYCRYSTALLINE REGION BELOW VIA OF A BS SAMPLE. THE COLOR ALLOWS QUALITATIVE STUDY OF VOID SIZE DISTRIBUTION (VERTICAL RED LINE MARKS THE TRANSITION)	55
FIGURE 3-24: 2 ND STUDY: TIME TO FAILURE (TTF) CALCULATED RESPECTIVELY WITH THE BS2, BS3, BS4, CS1 AND CS2 (ON THE TOP). R_{SLOPE} COMPARISON (AT THE BOTTOM).	57
FIGURE 3-25: 2 ND STUDY: MEAN TIME TO FAILURE (MTTF) CALCULATED RESPECTIVELY WITH THE CS2, BS2, BS3, BS4 AND CS1 AND FITTED WITH AN EXPONENTIAL DECREASING LAW. THE MTTF SHOWS A REMARKABLE INCREASE IF $L1$ IS SMALLER THAN 10 μ M, WITH THE ERROR BAR THAT REPRESENTS THE STANDARD DEVIATION.	58
FIGURE 3-26: 2 ND STUDY: MEAN OF R_{SLOPE} CALCULATED RESPECTIVELY WITH THE CS2, BS2, BS3, BS4 AND CS1 AND FITTED WITH EXPONENTIAL ASYMPTOTIC LAW. IF $L1$ IS INCREASED THE R_{SLOPE} CONVERGES TO THE VALUE OF THE CONSTANT NARROW STRUCTURE CS1, WITH THE ERROR BAR THAT REPPRESENT THE STANDARD DEVIATION.	58
FIGURE 3-27: RESISTANCE VERSUS TIME EXAMPLES OF SOME BLECH TEST LINES FITTED WITH AN EXPONENTIAL DECREASING LAW. SOME OF THESE LINES WERE SUBSEQUENTLY ANALYZED BY TEM TO CONFIRM THE PRESENCE OF A VOID (FIGURE 3-28). THE EXAMPLES SHOWN DID NOT FAIL DUE TO THE SHORT LENGTH EFFECT....	60
FIGURE 3-28: TEM CROSS-SECTIONS OF 2 SAMPLES OF THE BLECH-TEST STRUCTURE STRESSED FOR 1800 H. THESE ANALYSES CONFIRM THE PRESENCE OF A FULLY FORMED VOID UNDETECTABLE WITH USUAL EM-TESTS.	61
FIGURE 4-1: DUAL-DAMASCENE INTERCONNECT STRUCTURE.	65
FIGURE 4-2: EFFECT OF A VACANCY IN AN IDEAL CRYSTAL LATTICE. (A) INITIAL LATTICE. (B) DEFORMED LATTICE.	69

FIGURE 4-3: EXAMPLE OF HYDROSTATIC STRESS ON A 2D CUT SOLUTION ALONG THE DIRECTION X ZOOMED ON THE CATHODE.....	79
FIGURE 4-4: TIME OF NUCLEATION (TN) EVALUATED WITH THE LSS [79] AT THE SAME CONDITIONS OF THE SIMULATIONS I.E. AT 0.1 MA AND 300°C	79
FIGURE 4-5: EXAMPLE TEM CROSS-SECTION OF LSS DETECTED ELECTRICALLY. THIS ANALYSIS CONFIRMS THE PRESENCE OF A VOID FULLY FORMED UNDETECTABLE WITH CONVENTIONAL EM-TEST STRUCTURES. FURTHERMORE, THE DISTANCE OF THE VOLTAGE TAP FROM THE CATHODE IS SHOWN.	79
FIGURE 4-6: EVOLUTION OF THE HYDROSTATIC STRESS ALONG THE X DIRECTION AT THE TN FOUND EXPERIMENTALLY FOR EVERY EFFECTIVE CHARGE. THIS ALLOWED THE EVALUATION OF THE HYDROSTATIC STRESS ON THE CATHODE AT 0 NM AND AT 500 NM	80
FIGURE 4-8: BOTTLE STRUCTURES INTERCONNECT HYDROSTATIC STRESS DISTRIBUTION	81
FIGURE 4-9: HYDROSTATIC STRESS ALONG THE X DIRECTION AT THE TN FOUND EXPERIMENTALLY OF 106H FOR THE BS1.	82
FIGURE 4-10: TRIDENT STRUCTURE INTERCONNECT HYDROSTATIC STRESS DISTRIBUTION	82
FIGURE 4-11: HYDROSTATIC STRESS ALONG THE X DIRECTION AT THE TN FOUND EXPERIMENTALLY OF 106H FOR THE TRIDENT STRUCTURE.....	83
FIGURE 4-12: EVOLUTION OF THE INCREMENT OF VACANCY CONCENTRATION ($C_V/C_{V0}-1$) AT $x=0$ FOR C_{V0} (BLUE CURVE), $2C_{V0}$ (GREEN CURVE) AND $3C_{V0}$ (RED CURVE). WHERE C_V IS THE VACANCY CONCENTRATION AND C_{V0} THE INITIAL VACANCY CONCENTRATION.....	85
FIGURE 4-13: EVOLUTION OF THE HYDROSTATIC STRESS AT $x=0$ (AT THE CATHODE) FOR C_{V0} (BLUE CURVE), $2C_{V0}$ (GREEN CURVE) AND $3C_{V0}$ (RED CURVE) WITH C_V AS THE VACANCY CONCENTRATION AND C_{V0} THE INITIAL VACANCY CONCENTRATION.....	85

ACRONYMS

3D	Three-dimensional
AFD	Atomic flux divergence
BS	Bottle structure
CMOS	Complementary Metal-Oxyde-Semiconductor
CVD	Chemical vapour deposition
EM	Electromigration
FEM	Finite element method
IC	Integrated circuit
ILC	Inter level dielectric
IVD	Inter via dielectric
LSS	Local sense structure
MFD	Mass flux divergence
MTF	Mean time to failure
PDE	Partial differential equation
PECVD	Plasma enhanced CVD
SEM	Scanning electron microscopy
SVV	Single standard via
TEM	Transmission electron microscopy
TN	Time nucleation
TS	Trident structure
TTF	Time to failure

ABSTRACT

Electromigration induced failure is one of the main reliability issues for the microelectronics industry. The continuous scaling of the interconnect dimensions leads to higher operating current densities and temperatures, which accentuates the electromigration failure. As a consequence, electromigration still poses challenges for the development of the new technological nodes. In industry semi-empirical models with parameters of fitting calculated by distribution of experimental data obtained by accelerated test are conventionally used to estimate the lifetime of interconnections. More recently, it has been shown that these models are not reliable and moreover degradation depends also on the wire topological parameters and the interconnection network configuration. The study of the physical phenomena behind EM damage has become more and more important, since it can provide a deeper knowledge basis to anticipate the EM effect. In this context, experimental characterization coupled with mathematical modeling becomes a convenient way to understand the EM-induced failure. Therefore, the Mathematical modeling has become a fundamental tool for explaining numerous experimental observations and, ultimately, can deliver a stronger basis for design and production of reliable metallizations. The aim of this work is to merge the two different domains: one hand side the experimental characterization of interconnect structures conventionally done in industry and on other hand side the development of mathematical models, suitable for the implementation in COMSOL, a tool for numerical simulations, as these two domains are often too disconnected. This original approach has brought excellent results and it has allowed to confirm hypothesis formulated by experimental analysis. Moreover, it is proposed an original methodology to evaluate the critical stress of nucleation, parameter hard to estimate with conventional methods.

1 INTRODUCTION

1.1 Context

When an interconnect metal is traversed by a sufficiently strong electric current, there is a diffusive motion of atoms along to the current flow and of vacancies in the opposite direction. This phenomenon is named electromigration (EM)[1]. Though it had been observed previously, the study of EM became of fundamental importance in the late 1960's, when semiconductor companies observed failures in integrated circuits (ICs) by EM. From this point on, failure due to EM has been one of the main concerns regarding reliability in ICs [2]. The principal objective of device scaling is to increase the operating speed. Though, interconnects pose a significant delay to signal propagation in chips. Consequently, device scaling should be accompanied by improvements in the interconnect operation. In order to moderate the delay, low interconnect resistance and capacitance is essential, which demands high conductivity metals and interlayer materials with low permittivity.

At the same time, new integration processes have been developed and many materials have been investigated to produce adequate characteristics and, eventually, reduce the EM effect. These considerations contributed for example to the replacement of aluminum in a interconnect metal to aluminum-copper alloys, and later to pure copper [2]. Copper has a much lower electrical resistivity than aluminum and, furthermore, is more resistant to EM failure. The introduction of copper metallization

posed several defies, which ultimately resulted in the damascene fabrication process [3]. The interconnect structure is arranged in several levels of metallization with thousands of inter-level connections such as vias, so that the density of on-chip interconnects has increased from generation to generation of modern integrated circuits. This requires a decrease in interconnect width and thickness and, consequently, the operating current densities increase. Due to the continuous shrinking of interconnect dimensions, high current densities and temperatures are unavoidable. Therefore, EM failure is likely to be even more problematic for the next ICs generations, and the prediction of the long term interconnect behavior is a major necessity.

Traditionally ICs are manufactured by mounting a single die in a package. Thus, bigger dies in terms of space are needed to realize more complex circuits for a given technology node. This approach leads to higher length interconnects. In contrast to the transistors the propagation velocity of interconnects does not increase by scaling, leading to higher signal propagation times.

The aim of this thesis is to improve the electromigration mechanism understanding by the implementation of EM degeneration model in the simulation tool COMSOL before the void nucleation, supported by innovative electrical characterization and methodologies. Thereby, the localization of the areas with the highest failure probability are addressed. Furthermore, the results of simulations based on the finite elements method (FEM) coupled with the electrical and physical characterization allowed finding parameters that are difficult to calculate classically, allowing the prediction of problems for next ICs generation and the improvement of the reliability of CMOS 28nm interconnections.

1.2 Interconnect Structures in Microelectronics

Interconnect structures are responsible for the transmission of signals within electronic circuits. The active devices and regions once manufactured have to be electrically coupled to each other to make circuits. They are also connected to the outside world through their inputs and outputs on bonding pads. Making these connections is the role of contacts, vias and interconnects. Separating the interconnects from each other is the function of dielectric layers. These components are part of the metallization or back-end structure. The Figure 1-1 is a schematic cross-section showing these components in a standard integrated circuit (IC) structure. Recently the relative importance of the back-

end structures has significantly increased, and will likely continue as IC technology progresses.

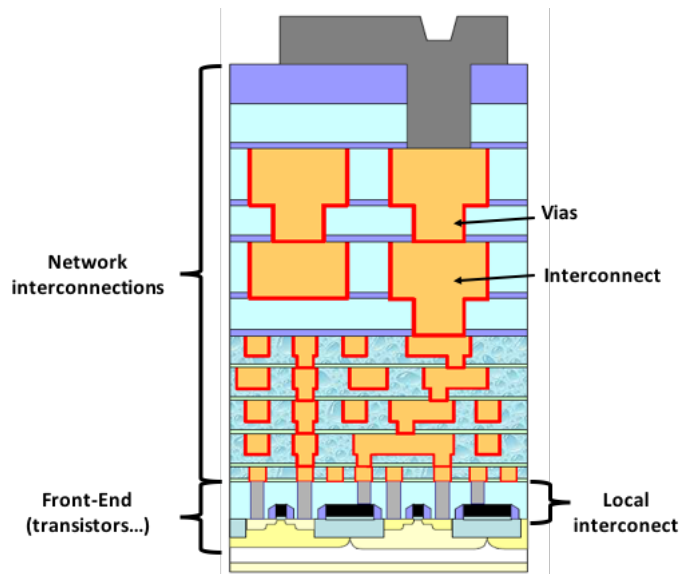


Figure 1-1: Cross-section of back-end structure, showing interconnects, contacts and vias, separated by dielectric layers.

The first structures in use were single wire connections between the active, such as electronic tubes and transistors, and passive elements like resistors, capacitors, and inductors found for example in old days radios. The next step was the development of printed circuit boards. These boards consist of copper layers laminated on polymeric substrates. By etching lithographically developed patterns into the copper, conductive tracks are obtained. This planar structure connecting the electric components exhibits low aspect ratios and allows the application of low cost wet etching techniques [4].

In integrated circuits the active components are placed in the substrate, usually silicon, whereon planar interconnect structures are grown. Besides the conducting lines several other layers are placed between them such as dielectric, etch stop, anti-reflective coating, diffusion barriers, and plugs realizing vertical connections, and thereby realizing multiple metallization layers.

The function of interconnection in integrated circuit is the distribution of the clock signals, the power, and the transmission of signals over the chip connecting various system functions. Due to the desired development of fast integrated circuits the interconnects have to meet the high-speed requirements for the clocks, the signals, as well as the downscaling of sizes. A typical parameter for interconnect speed is the RC time delay given by the product of the resistance and the capacitance of the line. To minimize this delay the interconnect structures have to be properly designed and material systems

with conducting materials exhibiting low resistance as well as isolation materials between the lines with low permittivity (low-k) have to be developed and implemented [4]. The conducting materials should further fulfill the following requirements:

- Low resistance
- High thermal conductivity
- High melting temperature
- Compatibility to the dielectric, the barrier, and capping layers
- Compatibility to the back-end-of-line process

1.3 Copper based interconnection fabrication

IBM began to develop metallization technologies based on copper in the 1990s. One benefit is the reduced resistance compared to aluminum of about 40%. The process of fabrication had to be modified as there is no reactive ion etching process for mass-production, contrary to aluminum [4]. After the deposition of the silicon oxide a second oxide layer is grown. This oxide is covered with a photoresist, which in turn is exposed to UV light for the pattern transfer from the mask and subsequently dissolved. After the etching process the oxide remains only at those locations where no copper should be located and the copper is deposited into the trenches and forms a layer at the top of the wafer. By chemical-mechanical polishing the top layer is removed and only the filled trenches remain. For the isolation another oxide layer is deposited and the steps described are repeated until the last metallization layer is formed [4]. Therefore, the processes forming the vias and the lines are very similar which enables the reduction of the process steps by saving one isolation oxide deposition, diffusion barrier, copper deposition, and planarization step [5]. The dual-damascene process takes advantage of the possibility to omit several process steps and is explained in the following. First an inter-level dielectric (ILD) layer is deposited on the wafer, followed by a photolithographic pattern transfer, the dissolution of the exposed photoresist, and etching of the vias holes. By depositing another photoresist and exposing it to UV light masked by the line patterns the structure of the lines is transferred. After dissolution of the photoresist and etching, the trenches of the lines are etched into the ILD and the vias holes are further etched to the bottom of the layer. The last steps are a deposition of the

barrier layer Ta/TaN and the copper, filling the vias and trenches, as well as forming a layer at the top of the wafer which is removed by chemical-mechanical polishing and covered by a non-conductive diffusion-barrier layer (i.e. SiCN) [5]. Figure 1-2 compares the single to the dual-damascene structure. In the dual-damascene structure the inter-via dielectric (IVD) layer is missing giving an idea of the reduction of the fabrication steps.

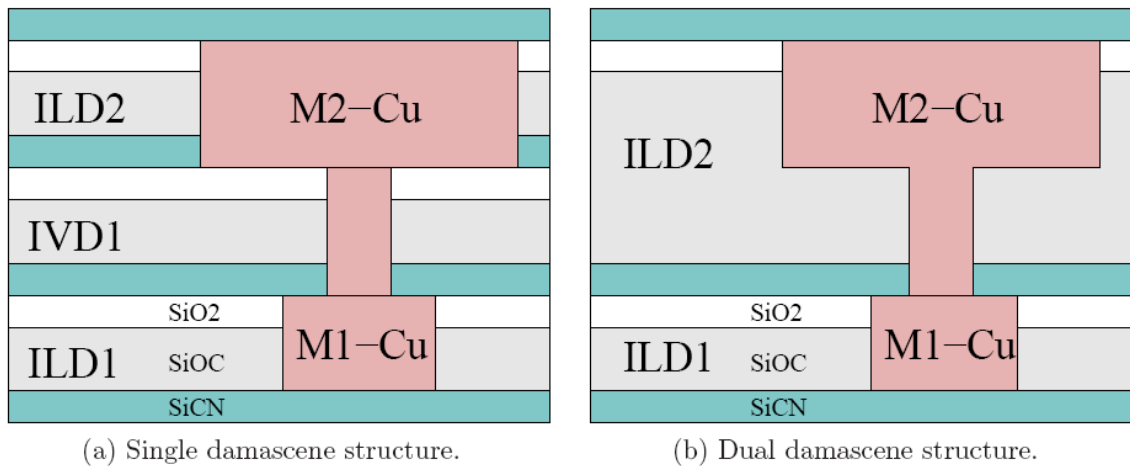


Figure 1-2: Single and dual damascene structure [6].

1.4 Failure mechanism in interconnect

In interconnects, failures are the variation of parameters beyond critical values which prevents the designated function of integrated circuits. The typical parameters are the resistance of the interconnect and the resistive and capacitive isolation to neighboring components like interconnects, devices, or to the bulk. Differences between the experienced parameters and the designed parameter can be caused by defect-related problems or by wear-out. The fabrication process causes defect related problems. Missing process steps and especially dirt contamination can be responsible for regions where the conducting material is missing, leading to higher resistance than designed. Furthermore, the isolating layers can be thinner than engineered, leading to higher leakage currents and capacitive coupling into other system parts, affecting their function [7]. Wear-out, in contrast, is a failure phenomenon, which occurs or evolves under the operation of the devices. This occurs under normal operating conditions. Wear-out phenomena are for example material diffusion from the metal into the semiconductor or the isolation/dielectric leading to a change in the electrical characteristics, or temperature induced phenomena leading to stress induced failure (e.g.

cracking or delamination) [7].

1.5 Electromigration induced failures

One of the processes leading to wear-out degeneration in interconnect structures is EM, the directed transport of atoms under the influence of an electric field acting as one force and a resulting electric current leading to a second force. The electric field force (called direct force F_{direct}) is a result of the ionic character of atoms in a metallic lattice as the valance electrons responsible for the electric conductivity are not bound to their atom anymore. Furthermore, the conducting electrons driven by the electric field are scattered at the atoms exerting a force on them, which is the so-called wind force (F_{wind}). Figure 1-1-3 shows these circumstances.

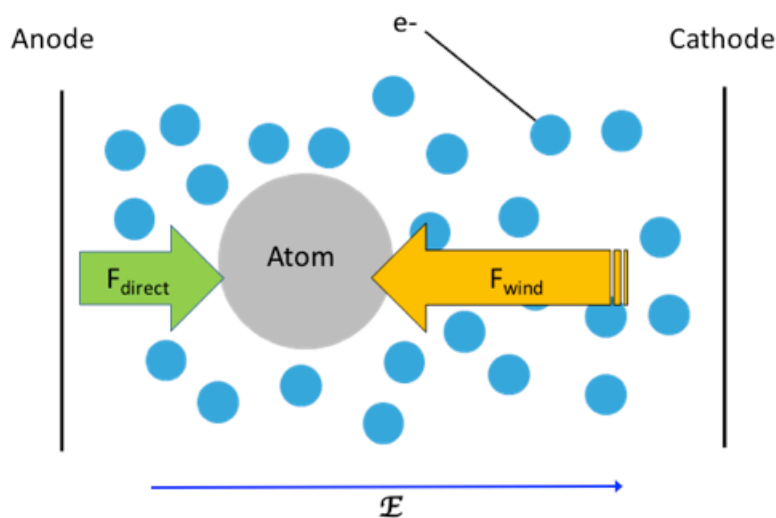


Figure 1-1-3: The two force of EM.

Beside this phenomenon, other material transport inducing phenomena are acting inside metals. Some are uncorrelated to the EM induced flux, e.g., thermal migration [8], and some are compensating partially the EM flux [9], e.g., diffusion. The transport of material in interconnect structures is leading to a mechanical stress build-up in the structures. These stresses can be tensile, when material is transported away; causing cracking or void formation and thereby leading to degradation as the conducting cross-sections are reduced. In the worst case an open circuit failure can be observed. The stress can also be compressive, which can crack the passivation and isolation layers between interconnects or other devices and cause the formation of a hillock. This leads to a reduction of the isolation gaps and thus degrades or even destroys the desired function

of an IC. Therefore, ICs have to be checked against these phenomena [10]. For these assessment tests under accelerated test conditions are carried out and the results are extrapolated to normal operation conditions. An extrapolation of the data is only reasonable, if the phenomenon leading to degeneration under accelerated conditions is the same as under normal operation conditions. Therefore, these tests have to be designed very carefully. Typical accelerated conditions are increased electric current densities and elevated temperatures. Due to this and the long times needed for experimental tests, numerical simulations are the method of choice to give designers a tool for pretesting or even testing.

1.6 Historic outline of electromigration

Electromigration was first discovered by the French physicist M. Gerardin in 1861 [11]. In the 1960s electromigration was recognized as one of the main failure phenomena leading to the development of different failure criteria and physically based models [12]. The subject first became of practical interest in 1966 when the first IC became commercially available. The main observation of electromigration in thin films was made by I. Blech [13]. Research in this field was pioneered by a number of investigators throughout the fledgling semiconductor industry. As already mentioned EM lifetimes acquired under accelerated tests have to be extrapolated to operating conditions. This extrapolation has to appropriately take into account relevant EM physical parameters and, consequently, it is normally performed based on empirical and semi-empirical expressions.

1.6.1 Black's equation

While working for Motorola in the 1960s, James R. Black was involved in the understanding of the “cracked stripe” problem [14]. This phenomenon was found to be electromigration induced. He carried out a systematic investigation and derived a model for the failure time prediction [15]. The model is based on the concept that a failure criterion is reached, if a structure specific mass is transported away.

$$TTF \cdot \dot{M}_r \propto 1 \qquad \text{Equation 1-1}$$

\dot{M}_r is the mass transported per time. This leads to the inverse proportionality of the time

to failure (TTF) to the rate of mass transport.

$$TTF \propto 1/\dot{M}_r \quad \text{Equation 1-2}$$

This rate \dot{M}_r is modeled by the proportionality

$$\dot{M}_r \propto n_e \Delta p N_a \quad \text{Equation 1-3}$$

with n_e being the conducting electron concentration, Δp the impulse transferred from the electrons to the atoms while scattering, and N_a the density of thermal activated atoms. The first two variables n_e and p are proportional to the current density J and N_a the density of activated atoms is modeled by the Arrhenius law [16].

$$N_a \propto \exp\left(-\frac{E_a}{k_b T}\right) \quad \text{Equation 1-4}$$

with the activation energy E_a , the Boltzmann constant k_b and the temperature T . The combination of **Equation 1-2**, **Equation 1-3** and **Equation 1-4** leads to Black's equation.

$$TTF \propto \frac{A}{J^2} \exp\left(-\frac{E_a}{k_b T}\right) \quad \text{Equation 1-5}$$

The constant A comprises the material properties as well as the geometry and must be empirically determined [15], [17]. The inverse J^2 dependence is a special case, which can be extended to the generalized Black's equation.

$$TTF \propto \frac{A}{J^n} \exp\left(-\frac{E_a}{k_b T}\right) \quad \text{Equation 1-6}$$

By substituting the exponent 2 by a second parameter n called the factor of current. The correct value for this parameter was extensively debated [18], [19]. According to Clement [20], lifetime models can be roughly classified into two groups. Void growth models, where the failure is triggered by the growth of a void over a critical size and nucleation models, where the failure is triggered by the stress build-up in the structure exceeding a critical value. For the void growth model the current exponent is found to be 1, because the mass transported is proportional to the current resulting in an inverse relation to the TTF [21]. Models based on the nucleation show an exponent of 2 as in the original Black equation due to the stress induced back flow flux [22].

For the prediction of the TTF the generalized Black equation is used to extrapolate the results from accelerated test conditions with increased currents and elevated temperatures to normal operation conditions. Measurements reported in the literature show values for n ranging from slightly greater than 1 to 6 [23]. Values above two are explained by the improper treatment of the Joule heating. Values in the range between one and two are interpreted as a failure based on a mixture of the two models, where a

void is first nucleated and followed by a growth phase [17].

1.6.2 Blech effect

Ian A. Blech from the Technion in Israel carried out a study, where he deposited golden islands onto a refractory underlay made out of titanium nitride. In his experiments, he stressed the film with high current densities [13]. Due to the much higher resistivity of the underlayer, the current mainly passed through the gold in the gold covered regions. By observing the movement of the islands he discovered a length dependent behavior. For long islands the edge, where the electrons pass into the gold, moved in the direction of the stripes with the velocity v_e .

$$v_e \propto \frac{D_a |Z^*| e p j}{k_b T} \quad \text{Equation 2-7}$$

where D_a is the self-diffusion coefficient, Z^* the effective charge, e the unit charge, the specific electrical resistance, and j the current density. At the other side of the island, extrusions were formed. For islands short enough the movement of the ends was not observed. For islands in between, the side, where the electrons entered, also moved with v_e but stopped after a certain time, when a critical length was reached. At the other end, no extrusion was formed. Blech discovered a critical value for the product of current density j and the length l of the islands under which electromigration does not occur. This finding leads to the concept of the Blech length as a critical value for a given current density.

The explanation for this phenomenon was found in the fact that different densities of mass in the island lead to a mechanical back stress working against the electromigration force. This compression stress has to be below the critical value of extrusion forming. While the islands are in steady state, the back flux induced by the stress gradient is totally compensating the EM flux. This back flux is proportional to the gradient of the tensile stress. Therefore, the maximum stress divided by the island length l is proportional to the back flux. With the fact that the EM flux is proportional to the current j the following can be deduced.

$$\frac{\sigma}{l} \propto j \rightarrow \sigma \propto (jl) \quad \text{Equation 1-8}$$

By taking a critical stress value into account a critical product $(jl)_c$ follows [24] [25]. As the stress build-up due to electromigration in microelectronic structures is highly depending on the surrounding materials, on the physical design and on the fabrication

process, the Blech length or product can hardly be pre-determined.

1.7 Experimental Lifetime Estimation

EM tests are carried out operating simple test structures and stress conditions which accentuate the EM degradation. This can be done by stressing an interconnect line at considerably higher current density and temperature than those found at operative condition. Classically, current densities in the order of 1 to 10 MA/cm² are used, and the test temperature is situated in the range from 170 to 350 C [26]. Under such conditions, interconnect failure is found much faster than it would be possible at use conditions. An significant matter here is that the results from the EM experiments have to be correlated to the real operating conditions, which means that the lifetimes found from the accelerated tests have to be extrapolated to the operative conditions. Additionally, only a limited quantity of interconnect structures are tested, whereas often hundreds of millions of interconnects exist on a chip. Consequently, the extrapolation needs to take into account, how to evaluate on-chip reliability from the EM sample test lines structures. Lately, the use of 1/f noise measurements has been explored for the purpose of finding faster techniques for electromigration (EM) Black's parameter extraction with excellent results [27].

In copper interconnects EM failures are primarily caused by void nucleation and growth at the cathode end of the line [28]. As the void grows, the electric current is forced to pass across the highly resistive barrier layer (TaN/Ta), which leads to a rise of the test line resistance. When this rise reaches a given threshold value (commonly more than 5% of the initial resistance), the line is considered to have failed. In this way, the EM lifetime of a given interconnect structure is obtained by monitoring its resistance change [29]. Because of the statistical character of EM lifetimes, it is indispensable to carry out EM experiments on a certain number of test structures, 32 samples for temperature-current condition is considered sufficient. The time to failure (TTF) or lifetimes obtained from these electricals characterizations are statistically analyzed and commonly presented in probability plots following a certain distribution which is characterized by a mean time to failure (MTF) and standard deviation [30].

EM lifetimes are normally described using a lognormal distribution. However, it has been discussed whether this choice is the most appropriate one [31], and it is debated

that EM lifetimes are more appropriately described by a multi-lognormal distribution[32]. This has been recently confirmed by several EM experiments [33] [34]. It should be pointed out that the understanding of the electromigration phenomenon is crucial to interpret the lifetime distribution for a correct evaluation of lifetime to real operating conditions.

1.8 COMSOL for Electromigration Simulation

Since the 1960s, numerous models have been suggested to describe electromigration. Mathematical modeling can meaningfully contribute to the understanding of EM failure mechanisms. It is an essential tool for explaining several experimental observations and, ultimately, it can deliver an improved basis for design and production of reliable metallizations. The principal problem is that EM is influenced by an extensive variety of physical phenomena and differs on a large number of intrinsic and extrinsic effects. Furthermore, the intricate interconnect geometries and technological process-related features of modern interconnects, such as a typical dual-damascene line, make modeling even more puzzling.

Numerous of the available models are founded on simplifying assumptions so that analytical solutions can be found. Though, as the development and improvement of diverse experimental techniques has permitted a deeper analysis of the EM failure, the complexity of the models has progressively increased, in order to be able to reproduce these experimental observations. Such intricate models cannot be analytically solved and, therefore, numerical solutions are now required. At the same time, the development of computational methods and resources has permitted to model complex systems and carry out numerical simulations in a proficient way. Therefore, the use of numerical solver tools for EM simulation in interconnect lines has become more common. As previously mentioned, EM failures can typically be described by a void nucleation and a void evolution phase. Due to the fact that each of these phases are related to different physical phenomena, it is suitable to treat them separately. A schematic design of such tool for EM simulation is then shown in Figure 1-4. In this thesis the modeling problem before “the void nucleation” has been addressed, while the modeling of void growth

has been studied previously through 2D modeling [35], and recently through 3D modeling [36].

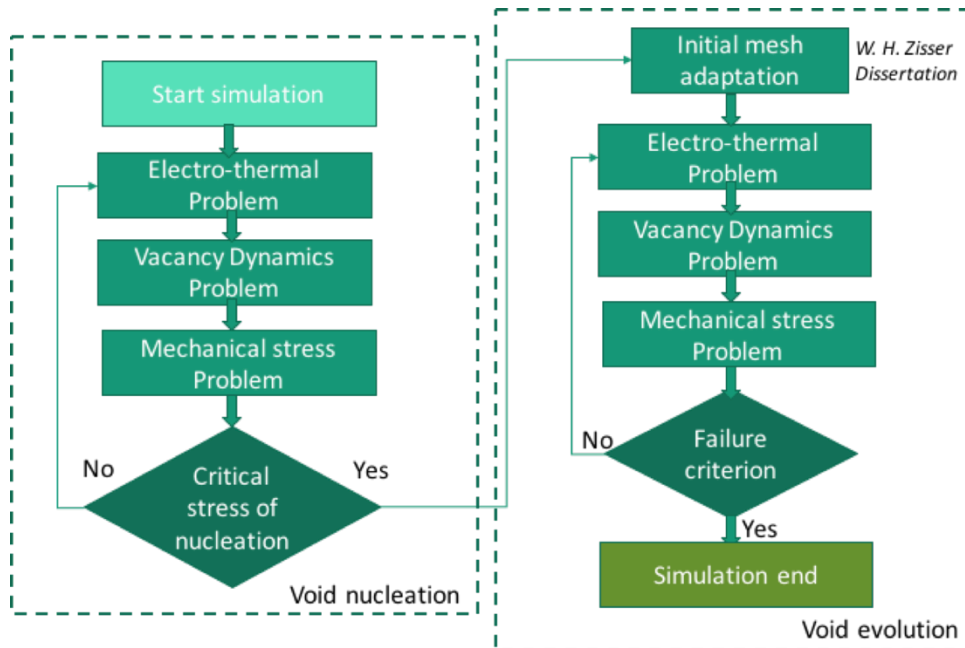


Figure 1-4: schematic design of a COMSOL tool for EM simulation.

1.9 Outline of this thesis

The main aim of this dissertation is to investigate the CMOS 28 nm backend technology regarding EM failure. This investigation includes experimental characterization and numerical analysis. In order to cover the full range of failure development, several experimental characterizations and simulations with the numerical model implemented in the software COMSOL have been carried out. The validity of the implemented model is demonstrated. This accomplishment is the basis for the EM failure assessment of interconnects structures taking also voiding into account.

This thesis is logically structured into 3 mainly chapters more introduction and conclusion. Chapter 2 gives a historic outline of the discovery of EM and the development of its modeling originating from the compact model developed by Black [15] relating current densities and lifetime. This is followed by Blech's findings [13], a critical length times current product for the occurrence of EM-induced voiding and hillock development. After the description of these simple models more advanced and

complex models are introduced, where the impact of the vacancy dynamics and the stress build-up is gradually incorporated, finally resulting in the state of the art model for EM. The typical characteristic of EM-induced vacancy accumulation featuring a three-phase behavior in time is used as an initial verification and is therefore discussed subsequently. In Chapter 3, the different test structures and methodologies used to characterize the electromigration are shown. The first part of the chapter is devoted to explain the electrical characterization; their relative test structures used and statistical studies carried out. A new experimental time has been defined; the time nucleation (TN), and the relative test structure that allowed this explained extensively. Morphological analysis necessary to gain complementary information and for further investigations are presented. Subsequently, the different relevant parameters and their relative statistical analysis are shown in detail. Complementary, the study of special structures that reproduce crucial aspects of interconnect design is shown. Finally, it is presented in detail how the calculation of the effective charge (Z^*) is performed with the morphological analysis together with the electrical characterization.

In Chapter 4 the full mathematics of the model PDE and the connecting quantities are presented in detail. To describe EM failure a variety of different physical phenomena have to be considered, resulting in the need to simulate a Multiphysics problem. This includes in bulk regions the electro-thermal problem, as the current is the driving force for EM, the vacancy dynamics, and the continuum mechanical model. Subsequently discuss the entire assessment of an interconnect structure with simulation results and their implications such as the sites of void formation at high hydrostatic stress. A new method to extrapolate the critical stress of void formation is proposed elaborating the data gathered experimentally. The special structures for focused design study have been reproduced to confirm the experimental data interpretation. Finally, some meaningful simulation to anticipate problems of the future technologies will be shown. Lastly, the thesis is concluded giving an outline for possible further improvements by taking atomistic and microstructural properties into account.

Chapter 1:Introduction

2 PHYSICS OF ELECTROMIGRATION

2.1 The electromigration driving force

Electromigration is a process of current induced atomic transport; which in a metal leads to void formation and so damages metal lines. This phenomenon, mainly activated by current stress and temperature, is explained by the collision between the conduction electrons in the metallic line and the metal ions [37]. It leads to the drift of the vacancies and so the ions. At the local scale, a divergence of the ions flux creates micro-voids at the cathode side and hillocks at the anode side. The force produced by this momentum transfer from the electron to the atom ion is the so-called “wind force”.

Classically, atomic diffusion is an arbitrary process, in the sense that there is no favorite direction of atomic jumps. However, during an atomic jump, when the atom is out of the lattice equilibrium position, it is subject to a greater electron scattering, in this way the momentum transfer from the electron to the atom affect the atomic jump in the direction of the electron flow [38], [39].

Huntington and Grone [1] represent the wind force using a semi-classical ballistic model of scattering:

$$\vec{F}_{wind} = -\frac{np_d m_o}{n_d p m^*} e \vec{E} \quad \text{Equation 2-1}$$

Where n and n_d are respectively the density of conduction electrons and the density of defects, p_d and p are the defect resistivity and the metal resistivity, m_o is the free-electron mass and m^* is the effective electron mass. Following e as the elementary charge, and \vec{E} is the macroscopic electric field. Huntington and Grone derived this equation assuming that the electrons are scattered only by the atomic defects and that the defects are decoupled from the lattice. A general expression for the wind force is given by the following equation of quantum mechanics theory [5]:

$$\vec{F}_{wind} = \sum_k \delta f(\vec{k}) \int |\psi(\vec{k})|^2 \nabla_{\vec{r}} V d\vec{r} \quad \text{Equation 2-2}$$

where the electron-point defect interaction potential is V and the electron scattering wave function for an electron incident upon the defect complex is $\psi(\vec{k})$, the perturbed electron distribution function caused by the applied field is $\delta f(\vec{k})$, which has the form [40]:

$$\delta f(\vec{k}) = e\tau\vec{E} \cdot \vec{v} \frac{\partial f(\epsilon)}{\partial \epsilon} \quad \text{Equation 2-3}$$

Where the transport relaxation time is τ , the velocity is \vec{v} , and the energy of an electron is ϵ .

Furthermore to the wind force, the so-called "direct force" [41] is the second contribution to the force acting on an atom. This force is due to the direct action of the macroscopic electric field on the migration ion. So, the sum of the direct force and the wind force represents the whole driving force acting on a metal ion:

$$\vec{F} = \vec{F}_{direct} + \vec{F}_{wind} = (Z_{direct} + Z_{wind})e\vec{E} \quad \text{Equation 2-4}$$

where the direct valence is Z_{direct} , the wind valence is Z_{wind} . The direct valence Z_{direct} is the nominal valence of the metal, when screening effects are neglected. Though, considerable controversy has emerged, when screening effects are taken into account. In fact, Z_{wind} represents the magnitude and direction of the momentum exchange between the conducting electrons and the metal ions. It is convenient to write **Equation 2-4** as

$$\vec{F} = Z^*e\vec{E} \quad \text{Equation 2-5}$$

where $Z^* = (Z_{direct} + Z_{wind})$ is named effective charge or valence. So, the microscopic, quantum mechanical effects of the electromigration phenomenon are included in the effective valence parameter, which can be theoretically evaluated and experimentally measured [42], [43], see also G.Marti IRPS 2016 [44].

Using the Nernst-Einstein relation, the drift velocity, \vec{v}_d , of metal atoms and the atomic flux due to electromigration are calculated, respectively, by

$$\vec{v}_d = \frac{D_a}{kT} \vec{F} = \frac{D_a}{kT} Z^* e \vec{E} \quad \text{Equation 2-6}$$

And

$$J_a = C_a \vec{v}_d = \frac{D_a C_a}{kT} Z^* e \vec{E} = \frac{D_a C_a}{kT} Z^* e p \vec{j} \quad \text{Equation 2-7}$$

Where D_a is the atomic diffusion coefficient, C_a is the atomic concentration, k is Boltzmann's constant, and T is the temperature. Regarding the current density \vec{j} , (since $\vec{E} = p\vec{j}$), the last equality in **Equation 2-7** is written.

From 2-6 and 2-7 one can see that the sign of the effective valence determines the direction of atomic migration. Thus, a negative effective charge means that the atoms diffuse in the same direction of the electron flow, i.e. a direction opposite to current density or the external electric field. Moreover, the mass flow is directly proportional to \vec{j} and to D_a . This means that the whole material transport due to electromigration is a function of the accessible atomic diffusivity paths.

2.2 Diffusivity paths

There are some possible diffusivity paths in an interconnect line, so the entire material transport is determined by the summation of the mass transport resulting along each of these paths. Generally, an effective diffusion coefficient of the form **Equation 2-8**, [3], [45] is taken into account to evaluate the material flux through these paths.

$$D_{eff} = D_l + f_{gb} D_{gb} + f_i D_i + f_c D_c \quad \text{Equation 2-8}$$

Where D_{eff} is the effective diffusion coefficient, the diffusion coefficients for diffusion through the lattice are: D_l lattice, D_{gb} grain boundary, D_i material interfaces, D_c dislocation cores (“pipe diffusion”). The correlative fractions of atoms diffusing along these paths are: f_{gb} grain boundary, f_i interface, f_c dislocation core.

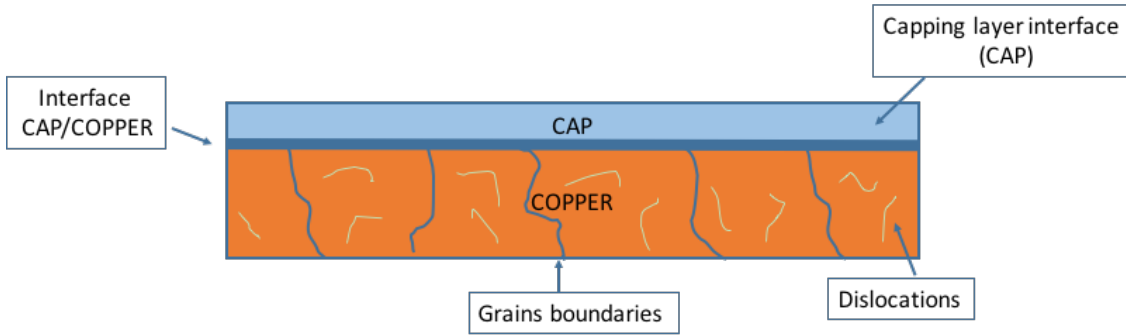


Figure 2-1: diffusion paths of lattice, grain boundaries, material interfaces and dislocations for a dual-damascene interconnect

For a classic dual-damascene interconnect the effective diffusivity is given by [46]

$$D_{eff} = D_l + \delta_{gb} \frac{(w - d)}{wd} D_{gb} + \delta_i \frac{2(w + h)}{wh} D_i + p_c a_c D_c \quad \text{Equation 2-9}$$

Where δ_{gb} , δ_i are the grain boundary and interfaces thicknesses, respectively, d is the average grain diameter, p_c is the dislocation density, a_c is the cross-sectional area of a dislocation core, w is the line width, and h is the line height. The Arrhenius law expresses the diffusion coefficients

$$D = D_0 \exp \left(-\frac{E_a}{kT} \right) \quad \text{Equation 2-10}$$

Where D_0 is the pre-exponential factor and E_a is the activation energy. From these equations, it is possible to realize that the fastest diffusivity path (i.e. the dominant diffusion mechanism) settles the effective diffusivity. The fastest diffusivity path revolves around several factors, as the temperature, the microstructure, and the quality of the interface between the metal, the capping layer adjacent and metallic barrier. Typically, lattice or bulk diffusion has the highest activation energy, being the slowest path for mass transport. Instead, the activation energy for diffusion along grain boundaries and interfaces is rather lower. Generally, surface interfaces have the lowest values, being the fastest diffusivity paths. **Equation 2-9** allows examining the relative influence of each path on the material transport due to electromigration. For example, when the line width is larger than the grain size, $w > d$, it is probable that grain boundaries constitute a continuous path in a way that grain boundary diffusion might meaningfully contribute to the total mass transport along the line. Instead, interfacial diffusion becomes more important, when the line width is less than the average grain size, $w < d$ (“bamboo-like structures”), because there is no continuous path for atomic transport along grain boundaries.

For example, in aluminum interconnects, the activation energy for grain boundary

diffusion is considerably lower than that for interfacial diffusion. This is credited to the formation of a stable native oxide on the aluminum surface, which reduces the interfacial diffusivity [3]. Therefore, for polycrystalline lines diffusion along grain boundaries is likely to be the main transport mechanism. For a bamboo-like structure the interfacial diffusion becomes the dominant path, as mentioned previously.

Therefore, the activation energy for interfacial diffusion in copper seems to be lower than for diffusion along the grain boundary [47], [48]. Accordingly, the interface between copper and surrounding layers is the main diffusivity path, for both polycrystalline and bamboo lines. However, it has been suggested that there should be a important influence of grain boundary diffusion to the entire electromigration induced mass transport in copper polycrystalline lines [49], [50]. This may become a main issue for the new technological nodes (28 nm and below), since the copper lines are expected to have polycrystalline structures at such nanometric dimension [49].

2.3 Electromigrations induced material transport

Though electromigration refers to the transport of material produced by the momentum transfer from conducting electrons to metal atoms [16], the total atomic migration is influenced by other physical mechanisms. Electromigration is a diffusion-convection problem, where atomic transport along the interconnect line occurs due to a combination of numerous driving forces. Because the atomic migration occurs via a vacancy exchange mechanism, the material transport can be, in general, described in terms of vacancies as

$$\vec{J}_v = \frac{D_v C_v}{kT} (\nabla \mu_v + |Z^*| e p \vec{j}) \quad \text{Equation 2-11}$$

\vec{J}_v is the vacancy flux, D_v is the vacancy diffusivity, C_v is the vacancy concentration, and μ_v is the chemical potential of vacancies. In sites of flux divergence vacancies can accumulate or disappear depending on the sign of the divergence, and the material balance is specified by the usual continuity equation

$$\frac{\delta C_v}{\delta t} = -\nabla \cdot \vec{J}_v + G \quad \text{Equation 2-12}$$

Where G is the generation or annihilation term. Equations 3-11 and 3-12 are the basic

continuum equations which describe the total mass transport along an interconnect line due to electromigration and associated driving forces.

Shatzkes and Lloyd proposed this model [16], it was the first that rigorously derived the interconnect lifetime with an inverse square dependence on current density. Only the influence of diffusion and electromigration on the vacancy flux is taken into account. The continuity **Equation 2-12** along the interconnect length direction can be written as

$$\frac{\delta C_v}{\delta t} = D_v \frac{\partial^2 C_v}{\partial x^2} - \frac{D_v |Z^*| e p j}{kT} \frac{\partial C_v}{\partial x} \quad \text{Equation 2-13}$$

Here, the source term $G = 0$ is used. For a semi-infinite line under the boundary conditions:

$$C_v(-\infty, t) = C_{v0} \text{ and } \vec{j}_v(0, t) = 0 \quad \text{Equation 2-14}$$

Which has the meaning that the vacancy concentration at $x = -\infty$ is fixed at an initial equilibrium value, C_{v0} , and that there is a perfect blocking boundary ($\vec{j}_v = 0$) at $x = 0$, the solution of 3-13 at the blocking boundary is given by Laplace transformation [16]:

$$\frac{C_v(0, t)}{C_{v0}} = 1 + \text{erf}(\beta) + 2 \left\{ \beta^2 [1 + \text{erf}(\beta)] + \frac{\beta}{\sqrt{\pi}} \exp(-\beta^2) \right\} \quad \text{Equation 2-15}$$

Where

$$\beta = \frac{|Z^*| e p j}{kT} \sqrt{D_v t} \quad \text{Equation 2-16}$$

And

$$\text{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x \exp(-x^2) dt \quad \text{Equation 2-17}$$

is the error function. Presuming that the failure happens, when the vacancy concentration reaches a certain critical value C_{vf} significantly higher than the initial equilibrium value C_{v0} , and that $\beta \gg 0$, then **Equation 2-15** is approximated [16] by:

$$\frac{C_{vf}}{C_{v0}} \approx 4\beta^2 = \left(\frac{|Z^*| e p j}{kT} \right)^2 D_v t_f \quad \text{Equation 2-18}$$

Since the diffusion the Arrhenius law expresses coefficient:

$$D_v = D_{v0} \exp\left(-\frac{E_a}{kT}\right) \quad \text{Equation 2-19}$$

Where D_{v0} is the pre-exponential factor for vacancy diffusivity, **Equation 2-18** yields the mean time to failure of the form:

$$MTF = \frac{AT^2}{J^2} \exp\left(-\frac{E_a}{kT}\right) \quad \text{Equation 2-20}$$

This equation is alike to the original Black's equation (**Equation 1-6**) [15], excluding the multiplying term T^2 , and it also predicts a mean time to failure with an inverse square current density dependence. This is a result of the statement that the failure takes place, when the vacancy concentration reaches a specified critical value, which corresponds, in fact, to a void nucleation condition. A comparable model to **Equation 2-13** had already been proposed by Rosenberg and Ohring [51] including a source term, so that

$$\frac{\delta C_v}{\delta t} = D_v \frac{\partial^2 C_v}{\partial x^2} - \frac{D_v |Z^*| e p j}{kT} \frac{\partial C_v}{\partial x} - \frac{C_v - C_{v0}}{\tau} \quad \text{Equation 2-21}$$

Where C_{v0} is the equilibrium vacancy concentration and τ is the characteristic vacancy relaxation time. The last term of this equation represents a source function which models vacancy annihilation/generation. This means that vacancies are annihilated, if their concentration is greater than the equilibrium value, or its are produced, if their concentration is smaller than the equilibrium one. The vacancy relaxation time, τ , characterizes the effectiveness of the sites acting as sinks/sources. In fact, smaller values of τ result in shorter times for the vacancy concentration to reach the steady state condition, and vice versa. As outcome, high vacancy supersaturation cannot be achieved near vacancy sinks, since vacancies are extinguished as rapidly as the local vacancy concentration gets higher than its equilibrium value.

The above-mentioned models, where material transport only due to gradients of concentration and due to electromigration itself is considered, have two main inadequacies: First, the time scale to reach the steady state vacancy supersaturation is of the order of minutes, which is a too short time related to the characteristic failure times. Second, the maximum vacancy supersaturation is very low. In this way, the energy barrier for void formation would be extremely high. This would impede void formation by vacancy condensation mechanism and, therefore, a critical vacancy concentration cannot be used to conclude the failure of the interconnect [52]. In the following will be shown that with the inclusion of mechanical stress in the model equations these inadequacies have been solved.

2.4 Electromigration and mechanical stress (Blech effect)

There are three primary sources of mechanical stress in interconnect lines. The first is the thermal stress, consequential to the difference in thermal expansion between the dielectric, the capping layer and metal upon cooling from high deposition temperatures. Metallization processing can expose an integrated circuit to temperatures of more than 400 °C. The second source of stress is non-equilibrium film growth. As wafer curvature measurements have shown, this source of stress is even more important than the thermal stress. The third major source of stress is the electromigration itself. Though the measurements significantly contribute to the understanding of thin film stresses, they are, most of the time, limited to simple test structures. Moreover, the full stress distribution within a material cannot be experimentally determined. For the dual-damascene technology high tensile stresses at interfaces, such as in the metal/capping layer interface, are generally critical, and electromigration can increase (anode) or reduce (cathode) this local tensile stress.

The adoption of passivating film material and corresponding process technology origins tensile or compressive stress in the interface between the metal test line and the passivating film. Interfacial compressive stress diminishes electromigration along interfaces by reducing the diffusivity [53]. Although, numerous experimental observations have shown that tensile stress in the interface increases the possibility of failure [53]. Elevated thickness and rigidity of the capping layer impede relaxation of both electromigration and thermally induced stress, which outcomes in dielectric cracking and metal extrusion.

The development of mechanical stress in interconnects lines depends on vacancies that can be created or annihilated such that their equilibrium is retained. For mechanical stresses to develop, there must be both a volume expansion and contraction of the line with complying to the surrounding material and a mechanical constraint due to the surrounding material. Because atoms swap places with vacancies and travel in the direction of the anode, there is a flow of vacancies in the opposite direction towards the cathode end. In the absence of vacancy sources and sinks, this would result in a vacancy supersaturation on the cathode end and an absence at the anode end. Since there is a small relaxation of the lattice surrounding a vacancy, vacancy accumulation would produce volume contraction at the cathode. Instead, the depletion of vacancies would produce volume expansion at the anode end. But, due to the constraints imposed by the

surrounding layers i.e. the passivation, the barrier layer and the capping layer of the dual-damascene interconnects, these volumetric variations cannot be accommodated, which origins the development of mechanical stress in the test line. Tensile stress is developed at the cathode end, while compressive stress develops at the anode end of the test line. Afterward, it is shown, that the stress gradient acts as further driving force for material transport and must be taken into account in the vacancy flux equation. Moreover, mechanical stress is a crucial parameter for the void nucleation condition.

2.5 Blech effect

Blech [13], [54], [55] designed an experiment where conductor islands were deposited upon a titanium nitride (TiN) film and stressed at a large current density. Considering the conductor resistivity was considerably lower than that of the TiN layer, the conductor stripe would transmit most of the current and the resulting movement of the ends of the stripe could be estimated. So, the electromigration induced drift velocity is determined by

$$v_d = \frac{D_a |Z^*| e p j}{kT} \quad \text{Equation 2-22}$$

Blech observed that only the upstream end (about the electron flow) of the line moved according to **Equation 2-22**, and that the upstream end stopped moving, when the test line was shortened to a certain length. Additionally, he observed that no drift could be detected below a threshold current density.

These observations can be explained by considering the flux due to electromigration and the gradient of the chemical potential via a gradient of mechanical stress [13], [54], [55] according to:

$$\vec{j}_v = \frac{D_v C_v}{kT} \left(|Z^*| e p \vec{j} - \Omega \frac{\partial \sigma}{\partial x} \right) \quad \text{Equation 2-23}$$

where the atomic volume is Ω , and the hydrostatic stress is σ . This equation indicates that a gradient of mechanical stress acts as driving force against electromigration. Therefore, electromigration stops, when the opposing stress gradient, generally referred to as “Blech stress”, equals the electromigration driving force, so that $\vec{j}_v = 0$. This steady-state condition is called “Blech Condition”, given by:

$$\frac{\partial \sigma}{\partial x} = \frac{|Z|^* e p \vec{j}}{\Omega} \quad \text{Equation 2-24}$$

Integrating over the length of the interconnect line yields:

$$\sigma(x) = \sigma_0 + \frac{|Z|^* e p \vec{j}}{\Omega} x \quad \text{Equation 2-25}$$

where σ_0 is the stress at $x = 0$. This equation shows that the stress varies linearly along the line, when the backflow flux equals the electromigration flux.

Assumed that the maximum stress the conductor line can tolerate is σ_{th} , a critical product for electromigration failure can be stated as:

$$(jL)_c = \frac{\Omega(\sigma_{th} - \sigma_0)}{|Z|^* e p} \quad \text{Equation 2-26}$$

This is the so-called ‘‘Blech Product’’. The critical product furnishes a measurement of the interconnect resistance against electromigration failure and numerous experimental works have disclosed that the critical product for modern copper interconnects is in the range from 2000 to 10000 A/cm [28], [56]. From the above equation, for a given current density, j , a critical line length can be identified, so that shorter lines will not fail due to electromigration. This is well known as ‘‘Blech Length’’, given by:

$$l_B = \frac{\Omega(\sigma_{th} - \sigma_0)}{|Z|^* e p j} \quad \text{Equation 2-27}$$

Similarly, for a given line length, L , the maximum current density that can be applied for which electromigration failure does not occur is:

$$j_c = \frac{\Omega(\sigma_{th} - \sigma_0)}{|Z|^* e p L} \quad \text{Equation 2-28}$$

A significant consequence of the Blech effect is that the jL product during electromigration tests have to be significantly higher than the critical product $(jL)_c$ for the corresponding test structure. Otherwise, the test structure might fail at a later time than it would normally do, giving a false sense of safety[57]. Another point to be evocated is that the presence of residual stresses from the fabrication process. In fact, it has been shown by Lloyd [57], that the stress produced by electromigration in order to reach the maximum value which a line can endure, can be reduced by the residual stress. So it means, that smaller values for the Blech length and smaller maximum operating current density than that given by **Equation 2-27** and **Equation 2-28** are obtained indeed.

2.6 Models of Stress Build-up due to Electromigration

Though Blech had shown that electromigration transport was closely related to mechanical stress development, the first model that related the rate of stress generation to electromigration was proposed by Kirchheim [58]. In the total vacancy flux equation, he added the gradient of mechanical stress as a driving force, as follow:

$$\vec{J}_v = -D_v \left(\frac{\partial C_v}{\partial x} - \frac{|Z^*|epj}{kT} + \frac{f\Omega}{kT} C_v \frac{\partial \sigma}{\partial x} \right) \quad \text{Equation 2-29}$$

Where $f = \Omega_v/\Omega$ and Ω_v is the vacancy volume. Thus, the continuity equation can be written as

$$\frac{\partial C_v}{\partial t} = -\frac{\partial}{\partial x} \left[-D_v \left(\frac{\partial C_v}{\partial x} - \frac{|Z^*|epj}{kT} + \frac{f\Omega}{kT} C_v \frac{\partial \sigma}{\partial x} \right) \right] - \frac{C_v - C_{veq}}{\tau} \quad \text{Equation 2-30}$$

The generation/annihilation function is the last term, similar to that suggested by Rosenberg and Ohring [51], (see **Equation 2-21**). Though, Kirchheim used the more general expression for the equilibrium vacancy concentration in a grain boundary

$$C_{veq} = C_{v0} \exp \left[\frac{(1-f)\Omega\sigma}{kT} \right] \quad \text{Equation 2-31}$$

which relates the equilibrium vacancy concentration with mechanical stress. The following equation represents the volumetric strain in a grain produced by the generation of vacancies [58]

$$\frac{\Delta V}{V} = (1-f)\Omega \frac{\delta}{d} \Delta C_v \quad \text{Equation 2-32}$$

where $(1-f)\Omega$ is the volume change due to lattice relaxation, when a vacancy is treated as a substitutional atom with smaller volume ($0 < f < 1$), δ is the grain boundary thickness, d is the grain diameter, and ΔC_v is the generated vacancy concentration. Thus, the strain rate is given by [58]:

$$\frac{1}{V} \frac{\partial V}{\partial t} = (1-f)\Omega \frac{\delta}{d} \frac{C_v - C_{veq}}{\tau} \quad \text{Equation 2-33}$$

which together with Hooke's law yields [58]

$$\frac{\partial \sigma}{\partial t} = B(1-f)\Omega \frac{\delta}{d} \frac{C_v - C_{veq}}{\tau} \quad \text{Equation 2-34}$$

where B is the rigid modulus of the test line.

This equation indicates that the stress build-up is connected to the deviation of the vacancy concentration from its equilibrium value and τ can have a substantial impact on the stress development. It is central to highlight that this model consents different

mechanisms of vacancy annihilation or generation to be defined. In fact, it is sufficient to set different τ for the different characteristic zone of an interconnect line, such as grain boundaries, bulk, interface between capping layer and the metal. This leads to smaller values for grain boundaries and interfaces and to larger values for the bulk of the line.

Equation 2-30 and **Equation 2-34** compose a non-linear system of differential equations, which has to be solved numerically. However, Kirchheim derived analytical solutions for some limiting cases and identified three main phases for vacancy and stress evolution [58], as shown in Figure 2-2. The first phase corresponds to a short period of time, where the initial stress is very low. Consequently, the equilibrium vacancy concentration remains unaffected and the vacancy concentration grows until a quasi steady-state condition is reached. The quasi steady-state phase is relatively long, and the vacancy concentration does not change very much, while the stress grows linearly with time. It continues until the stress becomes large enough to affect the equilibrium vacancy concentration. Next, a non-linear growth of stress with time is detected and the vacancy concentration almost follows the development of the equilibrium vacancy concentration. This means, that vacancies and stresses are in equilibrium and the true steady-state condition has been reached, (more details in [52]).

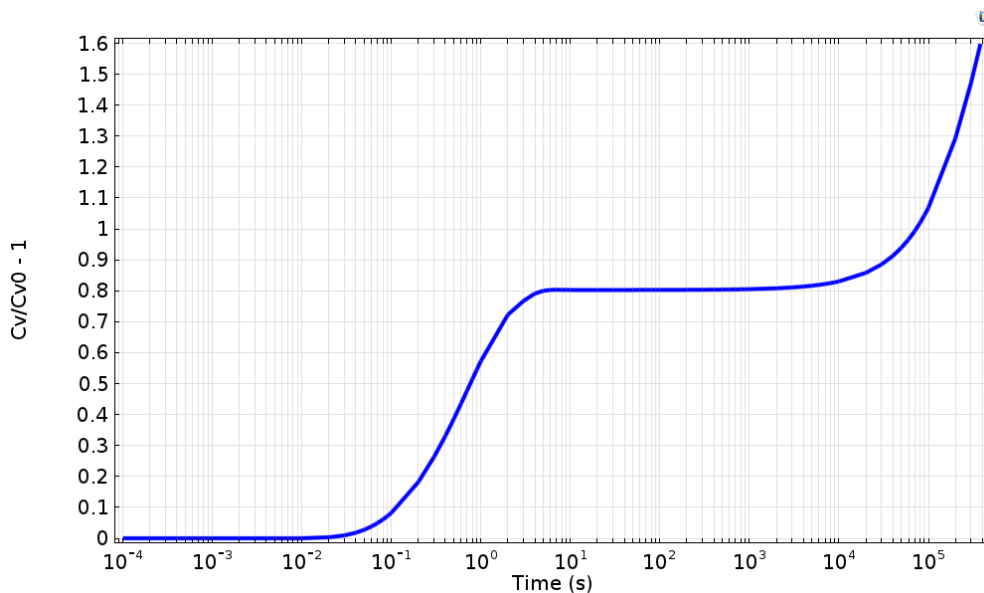


Figure 2-2: Evolution of the increment of the vacancy concentration ($C_v/C_{v0} - 1$) at $x=0$ with C_v as the vacancy concentration and C_{v0} the initial vacancy concentration.

Additionally, Kirchheim [58] disclosed that, if the electromigration lifetime is set by the time to reach a certain critical stress. The current density exponent of Black's equation depends on the magnitude of the stress and ranges from $n = 1$ at low stresses (the time

to failure is determined by the quasi steady-state period, see Figure 2-2) to $n = 2$ for higher critical stresses (the time to reach the true steady-state condition determines the lifetime).

Korhonen *et al.* derived a rather simplified model for the stress development in a interconnect subject to electromigration [59]. The generation/recombination is considered by them a dislocation climb mechanisms either in grain boundaries or at lattice dislocations. This cause changes to the concentration of lattice sites, C_L , producing stress according to Hooke's law:

$$\frac{dC_L}{C_L} = \frac{d\sigma}{B} \quad \text{Equation 2-35}$$

Using the source term [46], [60]:

$$G = \frac{\partial C_L}{t} \quad \text{Equation 2-36}$$

the vacancy continuity equation can be written as:

$$\frac{\partial C_v}{\partial t} = \frac{\partial J_v}{\partial x} - \frac{C_L}{B} \frac{\partial \sigma}{\partial t} \quad \text{Equation 2-37}$$

Assuming that the vacancy concentration is in equilibrium with the mechanical stress via [61]:

$$C_v = C_{veq} = C_{v0} e^{\left(\frac{\Omega\sigma}{kT}\right)} \quad \text{Equation 2-38}$$

Equation 2-37 becomes:

$$\left(\frac{C_v B \Omega}{C_L k T} + 1\right) \frac{C_L}{B} \frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x} \left[\frac{D_v C_v}{k T} \left(\Omega \frac{\partial \sigma}{\partial x} - |Z^*| e \rho j \right) \right] \quad \text{Equation 2-39}$$

when J_v from **Equation 2-23** is used.

Korhonen *et al.* observed that $(C_v B \Omega)/(C_L k T) \ll 1$ at typical electromigration test conditions. The meaning of this is that most of the transported vacancies initiate climbing dislocation which produce mechanical stress, while only a small number of vacancies is needed to keep the local equilibrium concentration [59]. Therefore, the above approximation lead to:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x} \left[\frac{D_a B \Omega}{k T} \left(\frac{\partial \sigma}{\partial x} - \frac{|Z^*| e \rho j}{\Omega} \right) \right] \quad \text{Equation 2-40}$$

where $D_a = D_v C_v / C_L$.

Following the same approach as Korhonen *et al.*, Clement *et al.*, derived an equivalent equation in terms of vacancies, [46], [59]:

$$\frac{\partial C_v}{\partial t} = \frac{D_a B \Omega}{k T} \left(\frac{\partial^2 C_v}{\partial x^2} - \frac{|Z^*| e \rho j}{k T} \frac{\partial C_v}{\partial x} \right) \quad \text{Equation 2-41}$$

This equation has the same form as **Equation 2-13** the Shatzkes and Lloyd formulation, but with D_v replaced $(D_a B\Omega)/kT$. Since it was assumed that vacancies are in equilibrium with stress, the stress can be calculated from **Equation 2-38** as

$$\sigma(x, t) = \frac{kT}{\Omega} \ln \left[\frac{C_v(x, t)}{C_{v0}} \right] \quad \text{Equation 2-42}$$

where $C_v(x, t)$ is determined by the solution of **Equation 2-41**.

Assuming that the electromigration failure is determined by the time to reach a given critical stress, the above models can predict void nucleation time.

Figure 2-3 shows the stress development with time at $x = 0$ according to Korhonen's solution, **Equation 2-42**. This demonstrates the concern of taking into account the mechanical stress in the model, along with the stress dependence in the generation/annihilation term term of the continuity equation. In Figure 2-4, the stress distribution along the line for some representational times is presented. At steady-state the stress changes linearly, as predicted by Blech [13], [54], [55]. It is clear that high stress can develop in the interconnect line, which is a necessary requirement for void nucleation [62], [63].

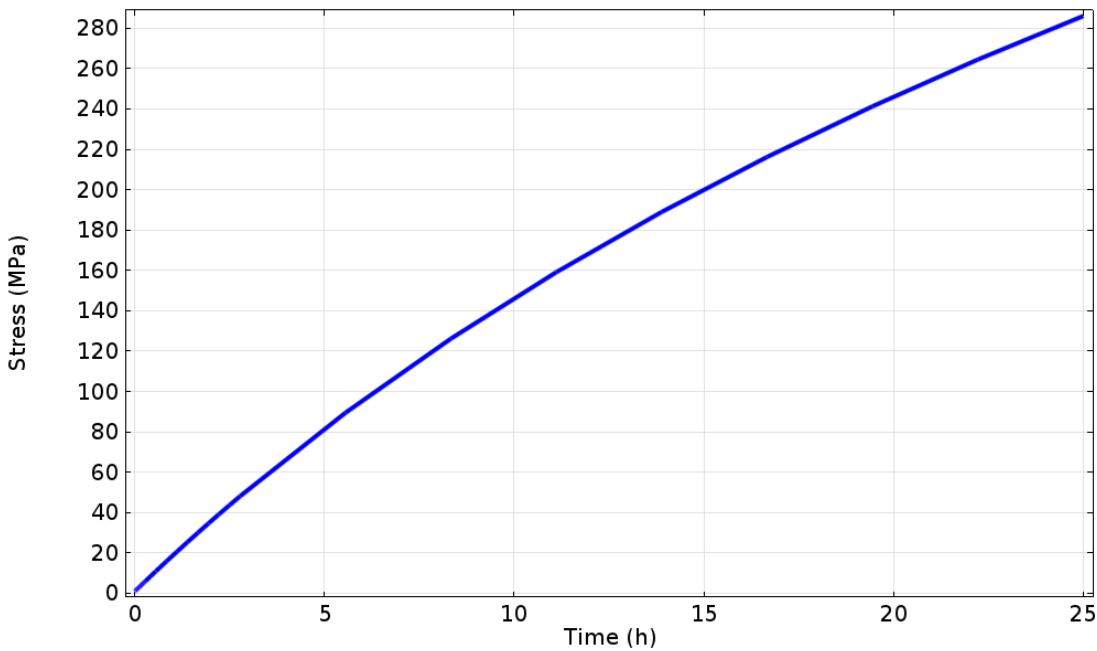


Figure 2-3: Stress build-up at $x = 0$ according to Korhonen's model.

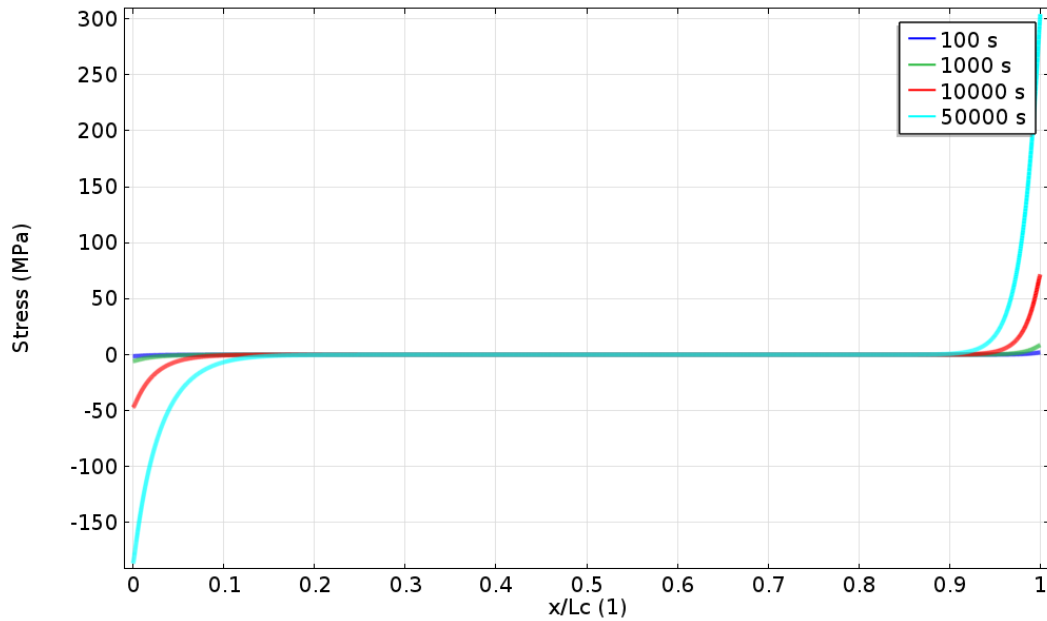


Figure 2-4: Stress build-up along the interconnect at different times.

These models were very acknowledged in explaining the origin of mechanical stress and calculating the hydrostatic stress which develops in a metal test line due to electromigration. Though, they are based on numerous simplifying assumptions and are applicable to elementary interconnect lines only. For example, the modulus B taken into account all the mechanical properties of the line and the effect of the constraints imposed by the surrounding materials. Consequently, a more general description of the problem is mandatory, in order to better find out the distribution of mechanical stress and its effects on the interconnect structures.

2.7 Void nucleation

Originally, void nucleation was imputed to the accumulation of vacancies at sites of flux divergence induced by their drift due to electromigration. At the time that the vacancy concentration at a particular site reached a certain critical amount, vacancy condensation would cause to the formation of a void [28,] [64], [65]. Though, an unrealistically high vacancy supersaturation would be needed for spontaneous void formation by vacancy condensation [51]. So, according to classical thermodynamics homogeneous, void nucleation by a vacancy condensation mechanism cannot be sustained under electromigration.

In the meanwhile, several works investigated the impact of mechanical stress on void nucleation under various conditions [66], [67]. The relevance of mechanical stress build-up in an interconnect line under electromigration was acknowledged, so that the development of a critical stress emerged as the main criterion for void formation “nucleation” [58], [59], [68]. However, the stress threshold value is still an open issue, varying from work to work, in Chapter 4 a new methodology is proposed to evaluate the critical stress of nucleation.

Voids are commonly observed to nucleate at the metal/capping layer interface intersected by a grain boundary [69]. Flinn [62] evocated that a void could form at a pre-existing free surface. Free surfaces can result from contamination during the line fabrication process, which impedes the bonding of the surrounding layer to the metal surface. Then, assuming a circular flaw of radius R_c and the surface free energy of the metal γ_s the critical stress σ_{th} for void nucleation is given by [62]:

$$\sigma_{th} = \frac{2\gamma_s}{R_c} \quad \text{Equation 2-43}$$

Clemens *et al.* [70] presented that the above equation is valid as long as the void grows in the contaminated region. Therefore, it is possible that the void extends beyond the flaw area, as shown by, once the equilibrium contact angle, θ_c , is attained. The equilibrium contact angle is calculated by interfacial energy balance, and lies in the range $0 < \theta_c < 90^\circ$. In this circumstance, the threshold stress is given by [63], [70]:

$$\sigma_{th} = \frac{2\gamma_s \sin \theta_c}{R_c} \quad \text{Equation 2-44}$$

which may exhibit a small decrease in the nucleation energy barrier compared to Equation 2-43.

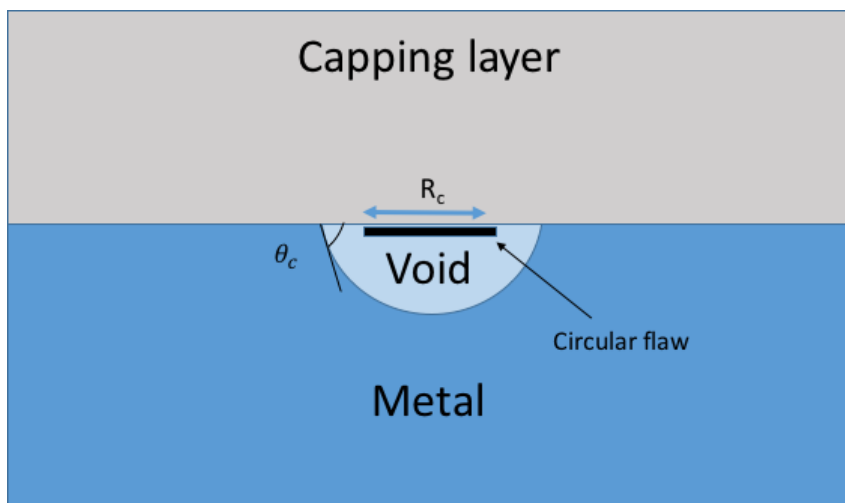


Figure 2-5: Schematic of void nucleation at an interface site of weak adhesion.

The critical stress is meaningfully reduced as the flaw area increases. For instance, for a flaw radius as small as 10 nm the critical stress is $\sigma_{th} \approx 340$ MPa [68]. Because of the contaminated region can extend through the whole line width, for a 100 nm wide line the critical stress becomes $\sigma_{th} \approx 70$ MPa. Experimental works have reported values of critical stress for void nucleation of about the same order of magnitude [44], [71]. Similar stress value is rather low and can be easily obtained in an interconnect line under electromigration.

2.8 Void evolution

The development of fatal voids (i.e. voids that trigger the line failure) is the ultimate cause for the electromigration induced interconnect failure [28], [30]. The failure criterion is typically set as a maximum resistance increase tolerated (generally 5% or 10% more than the initial resistance) for the corresponding interconnect. Once a void is nucleated it can grow, until it causes a substantial resistance increase or even completely separates the line.

The void evolution phase can include several processes: a void can drift along the interconnect [72], interact with the local microstructure [50] and grow, or even heal in certain conditions [73], before it definitely causes interconnect failure. Additionally, multiple voids can form in a line, so that their migration and agglomeration at a certain critical site can be the mechanism chargeable for the interconnect failure [72][74].

The void surface acts as an additional path for atomic migration. The chemical potential of an atom on the void surface is given by [75]:

$$\mu_s = \mu_0 + \Omega(w - \gamma_s k) \quad \text{Equation 2-45}$$

where μ_0 is a reference chemical potential, $w = (\sigma : \varepsilon)/2$ is the elastic energy density of the material adjacent to the void, γ_s is the surface free energy, and k is the curvature of the void surface. Therefore, the atomic flux on the void surface due to gradients in chemical potential plus electromigration has the form:

$$\vec{J}_s = -\frac{D_s \delta_s}{kT} (\nabla_s \mu_s + e |Z^*| \vec{E}_s) \quad \text{Equation 2-46}$$

where D_s is the diffusion coefficient on the surface, δ_s is the surface thickness, \vec{E}_s is the electric field tangential to the void surface, and ∇_s denotes the gradient along the

surface. The normal velocity at any point on the surface by mass conservation is given by the following [75]:

$$v_n = -\nabla_s \cdot \vec{J}_s \quad \text{Equation 2-47}$$

Void evolution due to electromigration is a complex dynamic process, for which modeling is a challenging task due to difficulty for tracking the shape of the void changing during the experience. Then, demands the application of numerical methods and special techniques for tracking the void during the growth.

The most generally used numerical method is based on sharp interface models [76] [36], which demands an accurate tracking of the void surface and, therefore, a continuous remeshing procedure. As the void drifts, grows, and changes shape this precise tracking becomes very tough. Then, it can be reasonably applied only for simple two-dimensional cases and cannot be further extended. This inadequacy can be overcome with the introduction of the level set method [35]. The main advantage of these methods is that the void is indirectly represented by a field parameter or level set function, so that void evolution is indirectly determined by the calculation of these functions. Therefore, the tough direct void surface tracking can be avoided, detailed information can be found in the ref [77] .

2.9 Conclusions

In this Chapter all the main physical phenomena related to electromigration have been described in detail. The following points are necessary for the understanding of the whole document:

- The electromigration driving force as a result of the action of the "wind force" has been derived and the origin of the charge effective Z^* explained.
- The role of the several paths for atomic migration in an interconnect line is discussed and the material transport equations are presented, highlighting the fact that only the diffusion paths of metal/capping and grains boundaries really contribute to the electromigration process.
- The Blech-effect has been explained in detail and why if $jL < (jL)_c$ the line is defined "immortal", leading designer to project power grids interconnection respecting these limits when it is possible.
- Several earlier continuum models of electromigration have been then described. Here, the impact of mechanical stress is explained. These are the basis for the developing of the actual 3D model of this document.
- The void nucleation condition is discussed in detail and, finally, the basic void evolution equations and associated numerical methods are briefly presented.

Chapter 0:

3 CHARACTERIZATION OF ELECTROMIGRATION

3.1 Objectives

In the following Chapter, the different test structures and methodologies used to characterize the phenomenon of the electromigration are shown. The first part of the chapter is devoted to explaining the electrical characterization, its relative test structures used and statistical studies carried out. The lifetime test electrical characterization is the principal experimental method used by the community to gather information about the reliability of the different technologies and designs of the interconnect network. A new designed test structure that allowed finding the time at which the first degradation occurs in the test line is shown, defined as “time nucleation” TN. Morphological analysis necessary to gain complementary information and for further investigations have been done. Subsequently, the different relevant parameters are shown and their relative statistical analysis is detailed. Finally, it is shown in detail how the calculation of the effective charge (Z^*) is performed with the morphological analysis together with the electrical characterization.

3.2 Electrical characterization

The lines are tested until all or most of them have failed. Usually, the median failure

conditions to operating time and the standard deviation of the assumed lognormal failure distribution are then estimated to characterize the sample reliability. Tests are performed at higher temperatures and current densities compared to operating conditions to obtain lifetime distributions in a reasonable time. As a consequence, extrapolations from EM stressing conditions according to the following equation [15] are necessary

$$TTF_o = MTTF_s \left(\frac{j_s}{j_o} \right)^n \exp \left[\frac{E_a}{k} \left(\frac{1}{T_o} - \frac{1}{T_s} \right) \right] \quad \text{Equation 3-1}$$

where TTF is the time of failure, MTTF the median lifetime, j the current density, n the factor of current, Ea the activation energy, k the Boltzmann's constant, T the temperature, an example is shown in the Figure 3 1. The subscripts o and s correspond to mean operative conditions and accelerated conditions, respectively. The result of EM in copper interconnects is void that span the whole line width and height. The main way to analyze these phases is the observation of the behavior of the resistance on which we base all our suppositions. Figure 3-2 shows the typical resistance versus time in accelerated conditions (high current density and high temperature) using a single standard via structure.

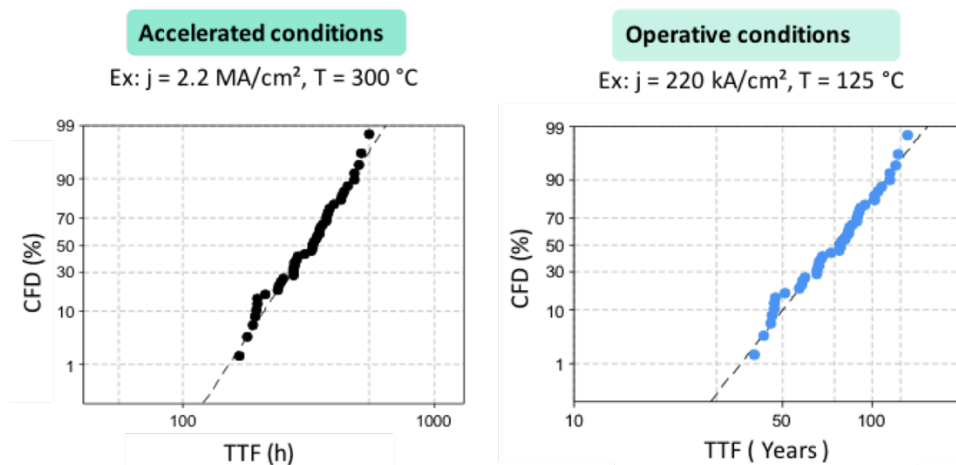


Figure 3-1: example of estimation of TTF distribution in operative conditions knowing the Energy of activation (E_a) and the factor of current (n)

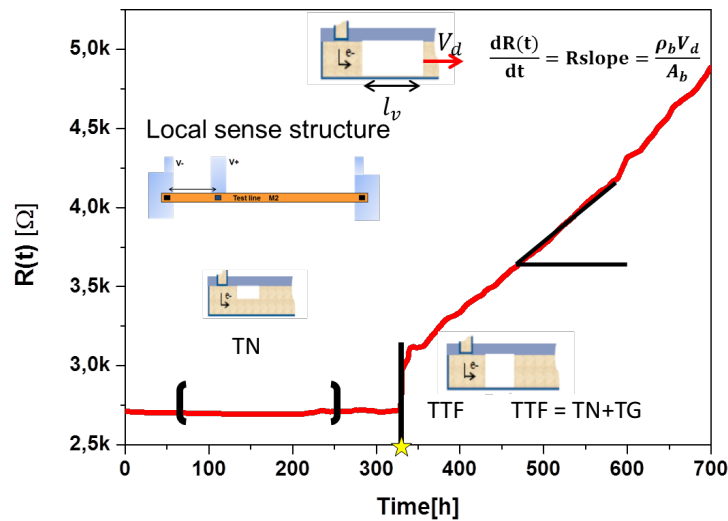


Figure 3-2: Resistance versus time curve of classic structure (SSV) that is subjected to electromigration stress. Different phases of the degradation process, representing the evolution of the degradation of the test line, are shown.

Three phases of resistance evolution have been observed in an EM test conducted with a classic structure (Figure 3-2). In the first phase, the voltage increase cannot be individuated with classic structures (SSV = single standard via). This is the “plateau” of a typical EM test, the phase less explored in the literature [78], where our analysis has been focused in order to define an experimental time of void formation (TN). The abrupt change of resistance corresponds to the second phase used to record the failure time TTF, currently the time that matches to an increment of 5% of initial resistance to facilitate the gathering of data; it’s possible to evaluate size and form of the void proportional to the jump step [28]. The time that the void takes to reach the metallic barrier is called TG, so $TTF = TN + TG$ [17]. In phase 3 is observed a linear increasing of resistance as a function of the time R_{slope} . This increase is linked to void growth. Quite a lot of literature exists about the drift velocity in metal liner after fully void formation [28]. In the usual method single-via, as the resistance increase caused by void formations is very small less than 1% of the resistance initial, EM systems are not able to detect any resistance change below this value, so void formation cannot be electrically detected. Herein an innovative structure the local sense structure LSS [78] has been characterized that allows measuring void formation through a design artifice, detailed afterward.

Moreover, with the normal structure, we individuated a phenomenon of resistance lowering in the plateau that we have studied and characterized. This phenomenon

suggests us that the EM result can also give information about the evolution of the strain in the line. The aim is to have a complete modelization of physics mechanism during electromigration.

3.3 Test structures

In the industrial context, the electromigration test is usually based on lifetime tests. The objective is to analyze the evolution of the resistance to evaluate time to failure, recently “time of nucleation” [78], [79] and drift velocity. Herein, all the test structure are dual damascene Cu line embedded in low-k dielectric of the 28 nm node CMOS technology process, that includes a CuMn seed layer [80], that decreases of one order of magnitude the drift velocity of copper (see Chapter 2) [81]. The line is surrounded bottom and side walls by a thin TaN/Ta diffusion barrier of few nanometers because very resistive and capped with SiCN. The ILD is in porous carbon silicon dioxide SiOC to reduce the parasitic capacitance. The line is ended at each extremity by one via where the electrons flow in the line (cathode via) or out the line (anode via) respectively. All the electromigration test structure used have the following characteristics in common:

- The width of the test line if no specifically detailed is 45nm (W_{min}) and the height 90 nm. The via side on the test line have a length of 60 nm and a width of 45 nm.
- Two current ports supplying the current into the test structure and two voltage taps sensors to evaluate the electrical potential difference allowing the calculation of the resistance (Figure 3-3).

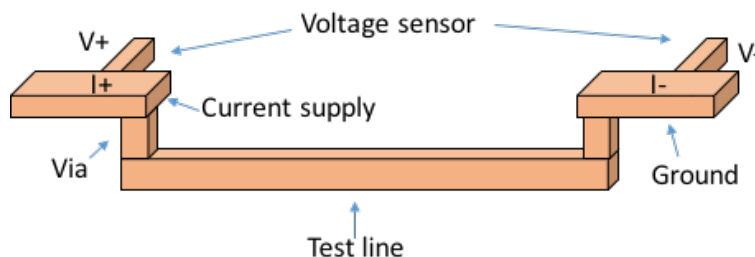


Figure 3-3: Test line scheme.

- The current taps and the voltage tap have to be at different positions of the test line under investigation to not interfere with EM process. The connection between the line, the current taps, and the voltage taps is done by via (Figure 3-4)
- This is recommended to isolate the line by the insulators that can act as a reservoir of copper as it happens for mono-level test structure (copper reservoir). The current injector has to be large enough to avoid electromigration in it.

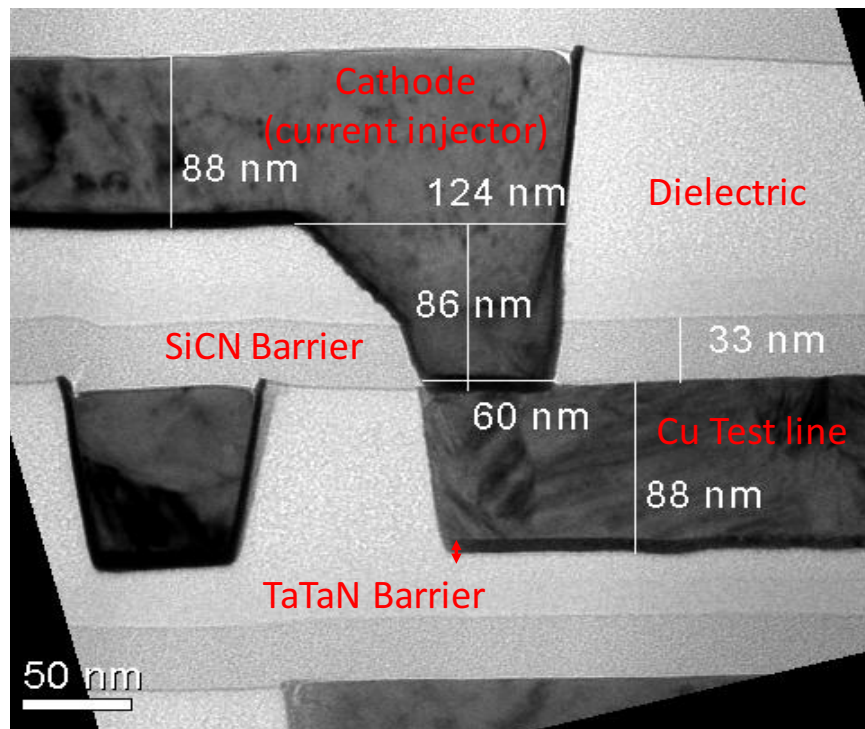


Figure 3-4: In the example is shown a cross section TEM analysis centered on the cathode via on the technology dual damascene Cu line embedded in low-k dielectric of the CMOS 28nm technology process, which includes a CuMn seed layer. In the figure, it is possible to clearly distinguish the SiCN barrier and Ta/TaN barrier.

- Detectors of extrusion have to be positioned around the copper line undergoing the electromigration, as shown in Figure 3-5. In the eventuality of an extrusion a leakage current can be detected thanks to these parallel copper lines.

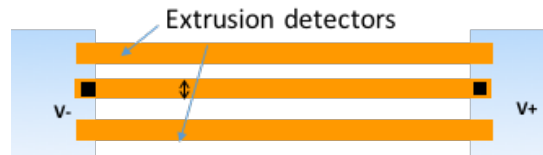


Figure 3-5: Test line scheme seen above showing the extrusion detectors.

Electromigration tests are conducted in accelerated conditions i.e. higher density current and higher temperature than operative conditions. This is done to have results in reasonable time imposed by industry, constraints some hundreds of hours. However, much high current can induce significant heat generation by Joule effect. An excessive self-heating leads to a failure by thermic gradient that it is not representative of a failure in operative condition. So generally the current is chosen to limit the joule effect under 5 °C. In order to respect these requirements, the silicon wafer is cut and every chip containing the test structure is then bonded and packaged.

The assembly of the structures brings additional time in comparison with other tests carried out directly on wafer. This is the main inconvenient of this technic. The test structures are then placed in the adapted test machines that allow setting current (generally between 0.1 and 0.3 mA) and temperatures (temperature generally between 250 and 300 °C). The interest of this method is the possibility to test groups of structures (in this case 16 test structures each oven) at fixed current and temperature. The lines are tested until all or most of them have failed. The median failure time and the standard of deviation of the assumed lognormal failure time (TTF) distribution are then estimated to characterize the sample reliability.

3.3.1 Single standard via

The single test structure is the most commonly used in industry to evaluate the reliability of each technology. The line is ended at each extremity by one via where the electrons flow in the line (cathode via) or out the line (anode via) respectively. The line can be tested in upstream or downstream configurations (see Figure 3-6). All the structures investigated in this paper are in downstream configuration.

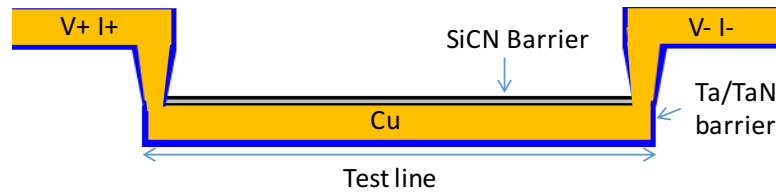


Figure 3-6: Single standard via (SSV) dual damascene Cu line downstream configuration.

The SSV was used also in order to characterize the phenomenon of resistance lowering in the plateau detailed in [82]. The evolution of resistance in this first phase can be fitted with decreasing exponential laws that give complementary kinetics information, phenomenon analyzed subsequently in this chapter (see paragraph 3.5).

Frequently this corresponds to an abrupt change of resistance since the void arrives at the bottom of the line on the metallic barrier and so the only metallic barrier with much higher resistivity ensure the passage of the current (see Figure 3-7). This structure allows the observation of phase 3 where currently a linear increasing of resistance as a function of the time is observed. This increase is linked to void growth ([28] Doyen) as shown in Figure 3-8. For the sake of simplification, only the predominant contribution of the metallic barrier to the total increment of resistance for interconnection is considered, so the drift velocity (V_d) of the void front can be calculated as shown in Figure 3-8.

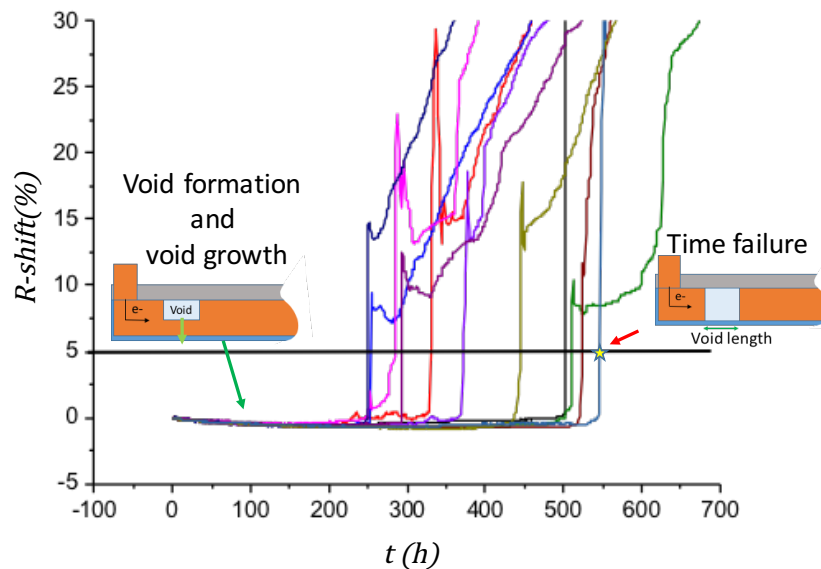


Figure 3-7: Electromigration degradation during the stress is followed by monitoring the resistance evolution of the line with time. The failure time (TTF) is recorded for each tested line at the resistance step increase of 5% of the initial resistance. The jump step of resistance is proportional to the length of the void.

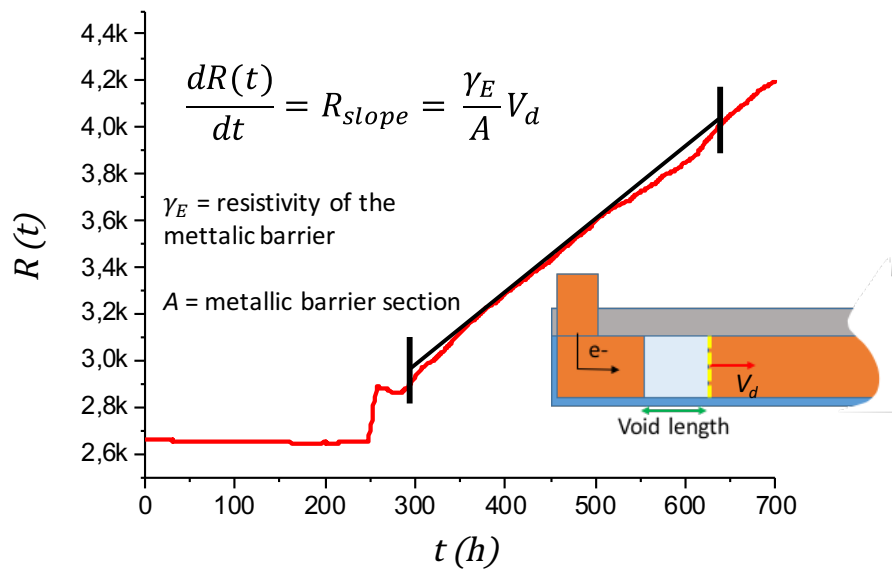


Figure 3-8: Experimental graphical example that shows the methodology to calculate R_{slope} and V_d

3.3.2 Local sense structure description

The new structure LSS presents the same characteristic of the standard single-via structure, but the anode voltage terminal is put much closer to the cathode via [78] (see Figure 3-9). This design artifice allows the measurement of the resistance of a smaller part of the line without influencing the conditions of EM, analyzing a zone where the void appears the most of the time frequently [73], confirmed by simulations and experimental data previously in literature and in this work. Thus considering that the precision of the electrical characterization tool is less than 1%, the sensitivity to resistance changes of “void nucleation” (TN) is increased. Since voids are typically formed within less than 1 micron from the cathode via [83], two LSS with the respective potential terminal V^+ at 0.35 and 0.7 μm from the cathode were studied.

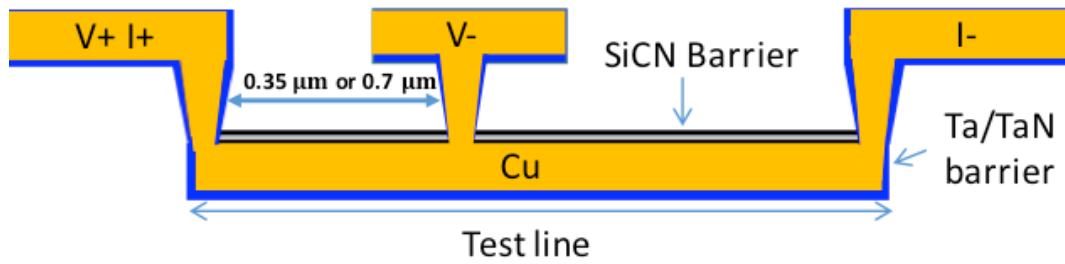


Figure 3-9: Test structure used a) Standard single-via (SSV) EM-structure and b) Local sense structure (LSS) test structure with voltage-senses closer to the via.

In the following, SSV and the LSS are compared and the void formation characteristic time is defined. In Figure 3-10 an example of the resistance evolution as a function of time for both structures is shown. In SSV there is no resistance increase, conversely a slight decrease around 1%, followed by jump, which indicates the full formation of the void (phase2). The time of resistance jump defines the time to failure (TTF). The behavior of resistance with LSS is clarified and gives additional information about the “the plateau” (see Figure 3-2). A smooth resistance increase is observed before the jump. The resistance shift has been considered as a “time of nucleation” (TN), note that the TN as defined here is quite different from the incubation time previously defined in Arnaud 2013 ref [80]. In Figure 3-11 are shown 6 curves of LSS, where the yellow stars indicate the TN. The LSS allows to isolate also a minimal variation of resistance by the fact that initial resistances of this structure is around 100 times smaller than the SSV, and so also variation around 0.1Ω can be detected.

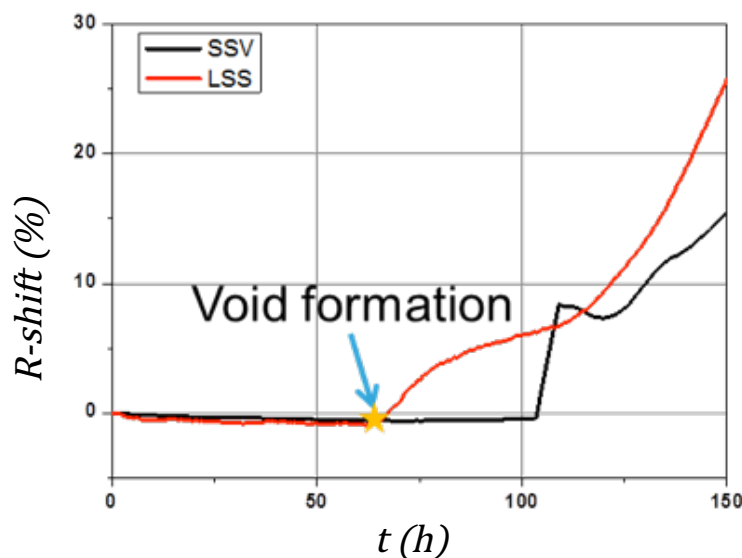


Figure 3-10: Comparative graph of resistance versus stress time for a single standard via (SSV) and local sense structure (LSS).

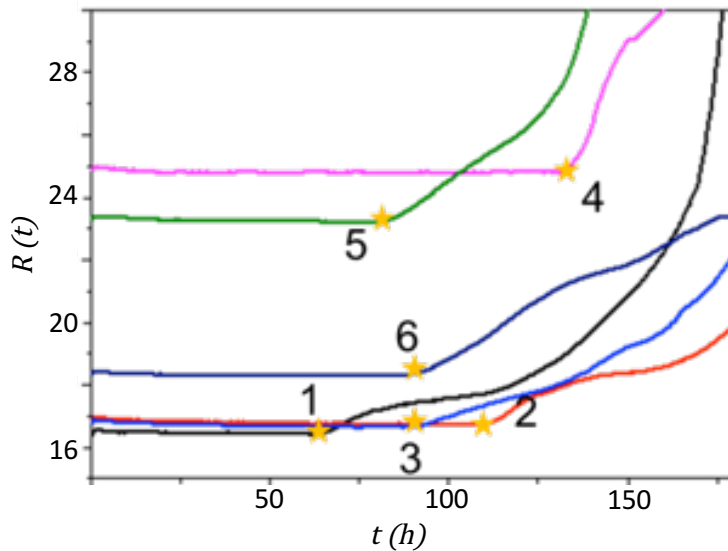


Figure 3-11: Example of a resistance versus time curve for LSS 1, 2, 3: Samples with the terminal of potential at $0.35 \mu\text{m}$ from the anode 4,5,6: samples with the terminal of potential at $0.7 \mu\text{m}$

Firstly, we compared TEM samples with resistance curve of Figure 3-11 and samples that presented a curve straight with no variation of resistance supposed without void. In Figure 3-12 meaningful examples are shown. In Figure 3-12a) the void between the two voltages senses has not been found as expected by electrical characterization (the curve is straight) and in Figure 3-12b) a full formed void has been found as predicted by electrical characterization. This proves that voids are between the voltages senses only when resistance shifts.

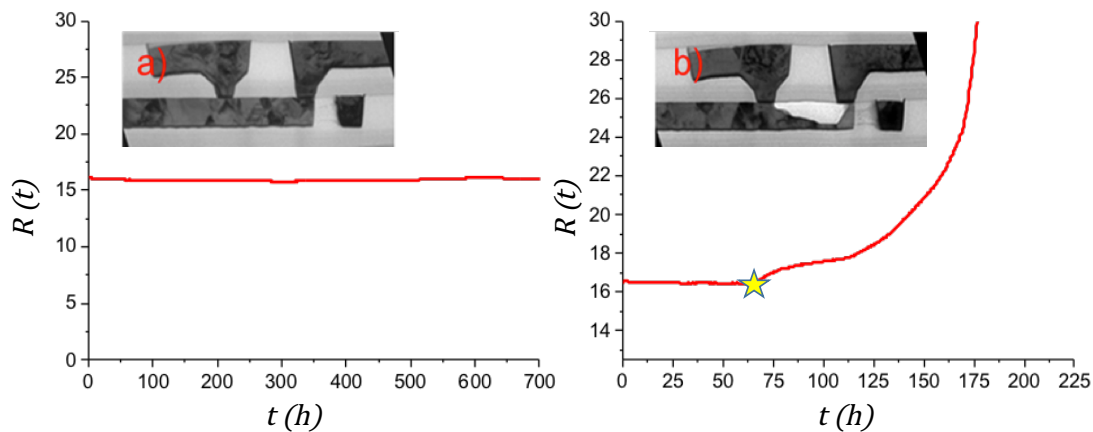


Figure 3-12: TEM of LSS after EM test a) sample without void between the voltage senses b) sample with void between the voltage senses.

To complete the analysis, TEM image of Figure 3-13 shows the void just nucleated as expected by electrical characterization. In details, we stopped the EM test after a positive variation of resistance of 0.1Ω (only possible with the LSS), before the void spans the whole line width and height. In other words, it's possible to know exactly when the void nucleates.

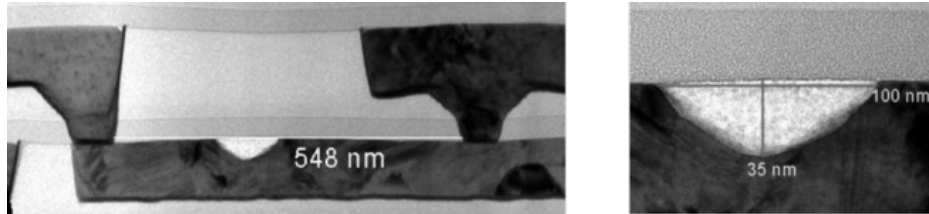


Figure 3-13: TEM of LSS after EM test stopped just after a small positive variation of resistance.

In addition, the LSS can also be used to localize the void, because it is possible electrically to catch the void only when it is between the 2 terminals of potential (see Figure 3-12). Thus, the two LSS (terminal of potential at $0.35 \mu\text{m}$ and $0.7 \mu\text{m}$ from the cathode) structures were compared to evaluate the probability to catch the void for 2 different temperatures and distances. In Table 3-1 the percentage of void nucleated between the 2 distances is shown of a population of 128 samples, 64 for each distance of the terminal of potential and 32 for each temperature. It's clear that is more likely to individuate the void with increasing the distance of the voltage sense from the cathode and lowering the temperature. This suggests the design of new structures with the anode tap at different distances from the cathode [79].

LSS	$0.35 \mu\text{m}$	$0.7 \mu\text{m}$
300 °C	37%	68%
330 °C	18%	50%

Table 3-1: Percentage to catch electrically a void in function of the distance of the voltage via and temperature.

These structures have been designed but unfortunately in STmicroelectronics never produced on Silicon. Moreover, in year 2015 the author Fen Chen IRPS2015 [84] has published a structure with a similar approach concept but with the voltage taps placed to the bottom of the line to avoid to interfere with the physic of electromigration. Considering that the interface between cap layer and copper is the preferential path of diffusion and site of nucleation. Chen's voltage taps are spaced every $5 \mu\text{m}$ and given that the void appears normally no more than $1 \mu\text{m}$ from the cathode, it seems more

interesting to add more voltage taps in this preferential zone close to the cathode. This was the conclusion of my paper IITC2014[79] to map the void spawn electrically and precisely.

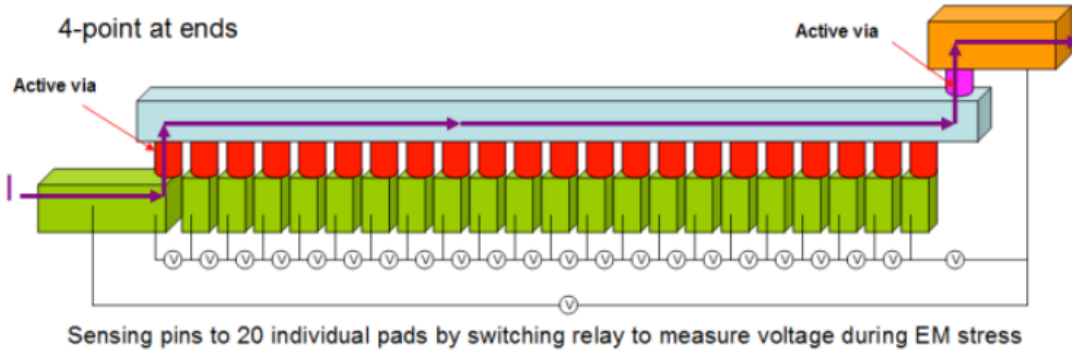


Figure 3-14: Chen IRPS2015 [84] test structure scheme. This structure allows following the evolution of resistance locally between 2 voltage taps.

3.4 Black parameters extraction

The extraction of the Black parameters E_a and n is obtained by lifetime test at different temperatures and current. The Black parameters are obtained by the MTF for every condition. In order to extract these parameters it's necessary at first to linearize the Black law previously shown, as follow:

$$\ln(MTF) = \ln(A_b) - n \ln(J) - E_a/k_b T \quad \text{Equation 3-2}$$

Practically, a series of tests is realized at constant current (J) but for different temperatures for extracting the energy of activation E_a . So the MTF are traced as a function of the corresponding $1/k_b T$, the slope obtained by linear regression gives the E_a value. Similarly, the time to failure obtained for constant temperature is traced for the different densities of current, the slope, in this case, is the n factor. The precision is strictly related to the numbers of samples analyzed, the test conditions chosen, the number of temperatures and currents. Currently, in the industry the Black parameters are extracted from lifetime tests of classical structures (see Figure 3-6), the objectives of this study is to go beyond the standard analysis extracting the same parameters also with the LSS considering the TN instead of the TTF and furthermore considering the R_{slope} calculated with the SSV. We have carried EM experiments for a set of samples with

LSS and SSV at 2 fixed current and two stress temperatures. In Figure 3-14 and Figure 3-15 the distribution of “time to failure”(TTF) and “time of nucleation”(TN) are compared. The distributions of both characteristic times (TTF and TN) lets us calculate activation energy (E_a) (see Table 3-2) and factor of current (n) with the Black equation [15] as explained previously. Moreover, it allows us to calculate the E_a and the n for the R_{slope} (see Figure 3-8) considering it as the inverse of the mean TTF (explained in detail [28] doyen). The values obtained are shown in Table 3-2. The values of E_a are in agreement with a lifetime dominated by time of nucleation. A further demonstration is that the factor of current n obtained with the TTF is around 2, conventionally in literature considered the value to define that the electromigration process is dominated by void nucleation [2], [17], [85], [86]. While for TN and R_{slope} the value obtained for n is around one. Considering the Lloyd theory [17] of the fractional n factor relative to the phase of void formation and void growth these values seems to be coherent, in fact the Black model [15] has been conceived to evaluate the TTF and in this case we extracted n from TN and the inverse of the R_{slope} , as were TTF. Remembering that the TTF is equal to the sum of the TN plus the time necessary for the void to reach the metallic barrier at the bottom of the line, time proportional to the inverse of the R_{slope} .

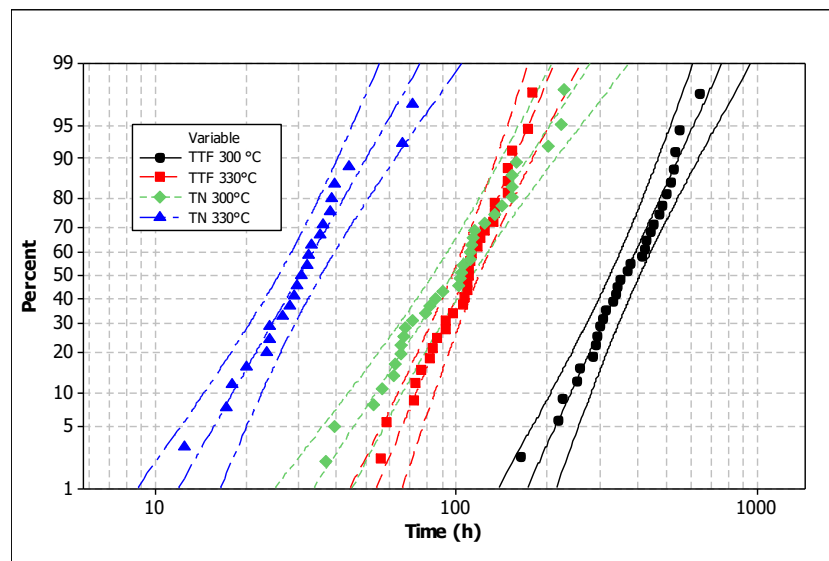


Figure 3-15: Time to failure (TTF) and Time of Nucleation (TN) calculated respectively with the SSV and the LSS at accelerated at constant current conditions for 300 °C and 330 °C.

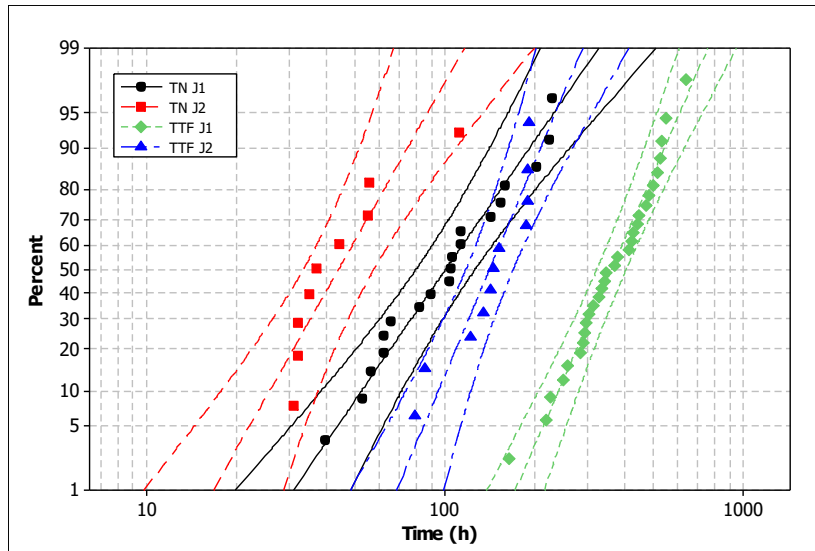


Figure 3-16: Time to failure (TTF) and Time of Nucleation (TN) calculated respectively with the SSV and LSS at accelerated conditions at constant temperature with currents $J_2 > J_1$.

TN		R_{slope}		TTF	
E_a (eV)	n	E_a (eV)	n	E_a (eV)	n
1.2 ± 0.1	1.2 ± 0.1	0.9 ± 0.1	0.8 ± 0.3	0.8 ± 0.3	2.4 ± 0.3

Table 3-2: Energy activation E_a and current acceleration factor n.

In this work the analysis of 2 test structures to study in detail the void nucleation and mechanic relaxation effects by using appropriate electrical measurements is shown. Void nucleation is defined as the degradation before the void spans the whole line width and heights. The accelerated parameters are in agreement with a lifetime nucleation dominated. Furthermore, the Lloyd theory [17] of the fractional n factor relative to the phase of void formation and void growth is confirmed; Moreover the TN nucleation can be used to calibrate models existing based on the critical mechanic stress to have more realistic predictions. Therefore, the comprehension of nucleation and others phenomena is fundamental to the future of interconnects reliability physics and modeling.

3.5 Resistance lowering fitting

In order to characterize the phenomenon of resistance lowering during the phase1 (“the plateau” see Figure 3-2), samples of SSV were baked for 800 hours at 300° C and we

followed the evolution of resistance in this first phase. Figure 3-17 shows an example of fitting the evolution of resistance of the heat treated sample (i.e. no current) with the decreasing exponential function. All samples reached a final resistance that we call Y_0 . Moreover, also the first phase or “the plateau” of all samples was analyzed (see Figure 3-2), considering just the part of the curve before the typical jump of resistance.

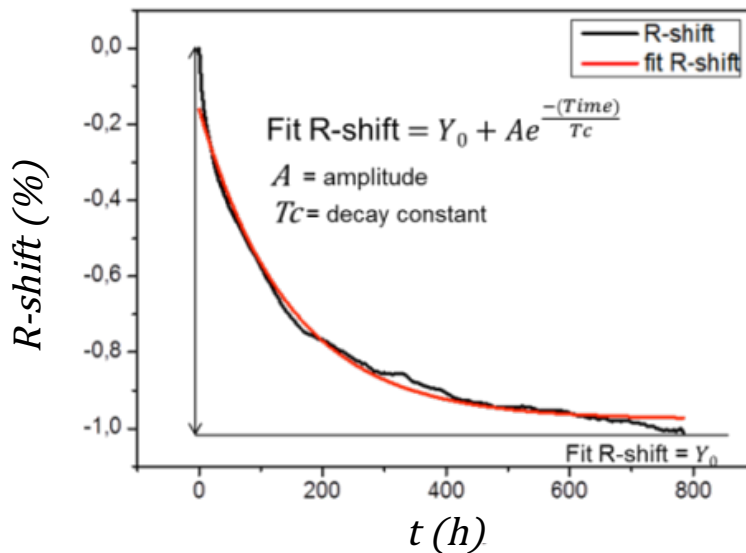


Figure 3-17: Example of resistance versus time (no current) fitted by decreasing exponential law.

In Figure 3-17 the example of resistance lowering fitting is shown. A represent the amplitude i.e. the resistance shift between the initial resistance and final resistance just before the jump for classic EM. Tc is the decay constant and represent the time that takes to recover A reaching the asymptotic value Y_0 . In the following is shown that A and Tc are strongly dependent to temperature and current magnitude. In Figure 3-18 and Figure 3-19 the distribution of the amplitude of *R-shift* (A (%)) and the decay constant (Tc (h)) are compared for a population of 128 samples, 32 for each pair temperature-current condition. The amplitude decreases in presence of current and at higher temperature. The constant decay at higher temperature and in presence of current is clearly smaller; the meaning is that the devices reach the asymptotic value Y_0 in less time. This suggests us that this phenomenon of resistance lowering is closely related to the temperature and density current of the test condition.

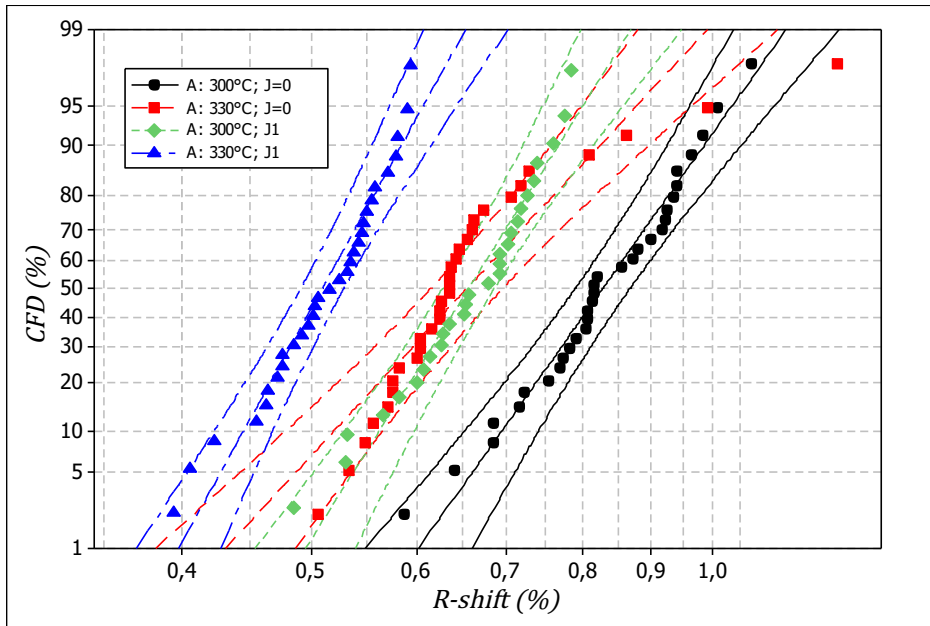


Figure 3-18: Cumulative function distribution (CFD) of Amplitude (A) in absence of current ($J=0$) and with current = $J1$, Lines represent the 90 % confidence level (C.L.) of the data.

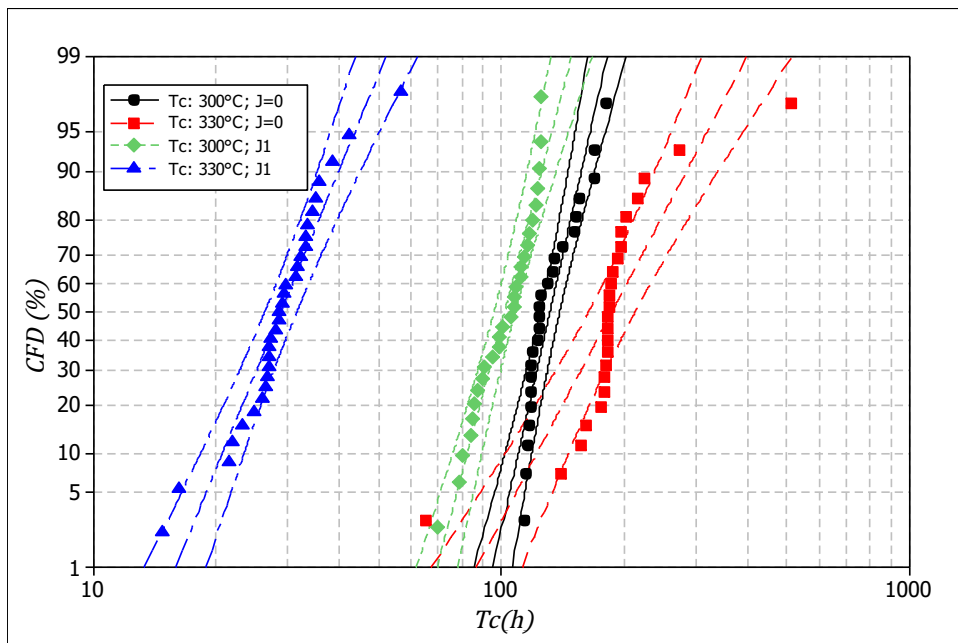


Figure 3-19: Cumulative function distribution (CFD) of constant decay value (Tc) in absence of current ($J=0$) and with current = $J1$

Afterward, all samples treated thermally were tested with current $J1$. It's interesting to see that the treated samples show now the “plateau” perfectly straight, as shown in Figure 3-20. The mean of TTF changes slightly, less than 10% of difference. We think that this resistance lowering is related with relaxation mechanic and/or homogenization of the material. Therefore, it could be interesting to use a similar electrical structure to

monitor also the mechanical properties. Probably the thermal mismatch between copper and cap induces a compression state at the interface (principal site of void creation) that makes the spawn of the void for samples without heat treatment a bit harder. The experimental results allow thinking that the MTF of samples with heat treatment is slightly lower due to mechanical relaxation.

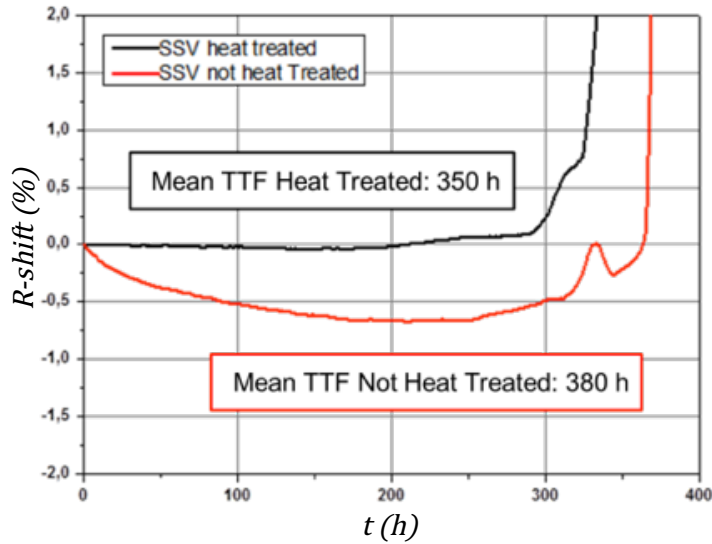


Figure 3-20: Example of resistance versus stress time for a SSV heat treated and not heat treated structure test line.

3.5.1 R_{slopes} of heat treated and not heat treated devices

The slope of heat treated and not heat treated sample is almost the same (see Table 3-3). So the heat treatment does not seem to modify the preferential diffusivity paths [10]. In conclusion, heat treatment seems to affect only the mechanism of nucleation.

Mean R_{slope}	
Heat treated (Ohm/h)	Not heat treated (Ohm/h)
3.8±0.9	3.8±1.2

Table 3-3: Slopes at 300 °C of SSV samples heat treated (baked for 800 h at 300°C) and not heat treated.

3.6 Focused design study

More recently, it has been shown that EM degradation depends also on the wire topological parameters and the interconnection network configuration. For instance, B. Ouattara [87] shows that redundant paths have significant effect in Power Grid lifetime increase. On the other hand, F. Bana [83] shows that Cu line with a narrow to wide line width transition can provide an increase of lifetime up to a ratio of 40 in comparison to a constant narrow line. R.G. Filippi introduces an equivalent length function for the structures with the width variation that depends on the width and length of each region [88]. Herein, two different structures that also reproduce crucial aspects of interconnect design (Figure 3-21 b) and c)) are studied extensively. The purpose is to evaluate the effect of these configurations on the electromigration degradation in order to provide lifetime quantitative design rules.

The standard reference structures are single standard via that for convenience have been called: constant structure (CS) of Figure 3-21a because has the same width all along the line. The trident-structure (TS) of Figure 3-21b and the bottle-structures (BS1, BS2, BS3 and BS4) of Figure 3-21c present substantial geometrical differences versus the CS. For the TS metal line splits into three parallel branches at L_1 distance from the cathode with the same width everywhere ($W_1=W_2$) and each line is ended with a single via. The BS structures show line width transitions at a distance L_1 from the cathode from W_1 to W_2 either with $W_2=2W_1$ or $W_2=3W_1$.

The purpose is to evaluate the effect of these configurations on the electromigration degradation in order to provide lifetime quantitative design rules. Taking into account these configurations will increase the accuracy of reliability prediction at the design level and help designers to deal with high current density needs.

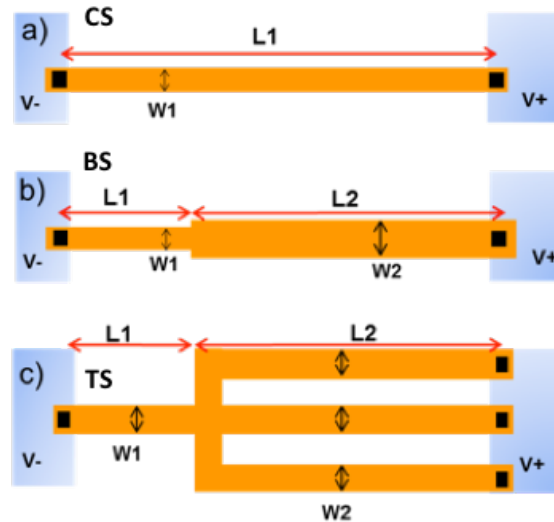


Figure 3-21: Test structure used a) constant reference structure (CS) EM-structure used to have time to failure for the Ref b) Bottle structure BS c) trident-structure TS

We have carried EM experiments with a fixed stress current and temperature for all designed structures with a sampling of 32 test structures by type except for the CS1 for which 64 test structures have been used. The detailed structure geometries used for these studies are summarized in the following Table 3-4 with their relative mean time failures and mean resistance slope (R_{slope}). For reasons of clarity Table 3-5, Table 3-7 and Table 3-8 show the test structures and the relative geometrical parameters for each specific study.

	L1 (μm)	L2 (μm)	W1 (μm)	W2 (μm)	MTTF (h)	Mean R_{slope} (Ohm/h)
CS1	200	0	0.045	-	346	3.6
CS2	0	200	-	0.09	1467	0.8
TS	10	190	0.045	0.045	1038	2.3
BS1	10	190	0.045	0.0135	1046	1.2
BS2	5	195	0.045	0.09	1001	1.6
BS3	10	190	0.045	0.09	456	1.8
BS4	20	180	0.045	0.09	497	3.2

Table 3-4: Summary geometrical test structures parameters and the relative mean time failure (MTTF) and mean of R_{slope} .

3.6.1 1st Study: Microstructure study of the line width transition [BS vs TS]

The purpose of this study is to evaluate if the microstructure has any effect on the phenomenon of degradation. In this first study, the length of the narrow cathode part of

the line is kept constant for both structures TS and BS1. Then the width of the second part of BS1 is varied with $W2=3W1$ as shown in the Table 3-5. It follows that TS and BS1 have an equivalent section as shown in Figure 3-21 but different microstructures in the transition narrow section ([83]), TS is supposed to have the same microstructure of the CS1 in each branch.

1 st Study	BS1	TS
L1	10 μm	10 μm
L2	190 μm	190 μm
W1	0.045 μm	0.045 μm
W2	0.135 μm	0.045 μm

Table 3-5: Geometrical test structures parameters of 1st study.

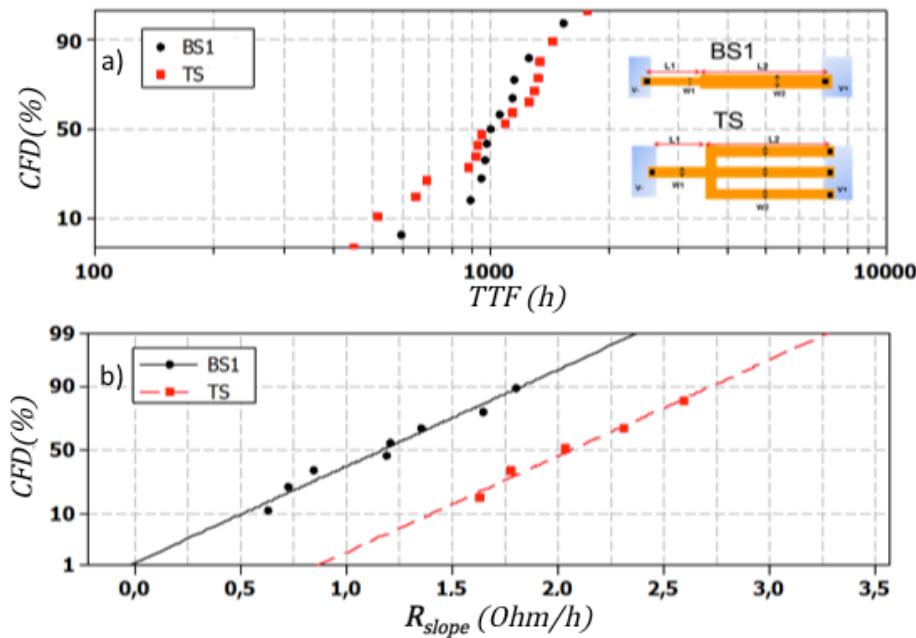


Figure 3-22: 1st Study: Cumulative function distribution (CFD): a) Time to failure (TTF) calculated with BS1 and TS respectively. b) R_{slope} comparison of BS1 and TS.

In Figure 3-22a the distribution of lifetimes (TTF) is shown. It should be noticed that similar distributions are obtained for both structures with line width transitions. The comparison with the reference structure (CS) with a unique narrow line width shows an increase of TTF for both line width transition structures. Such lifetime increase for line with line width transition has already been reported [8]. Indeed, F. Bana *et al.* have demonstrated that increasing line width results in better bamboo microstructure with

fewer grain boundaries (Figure 3-23).

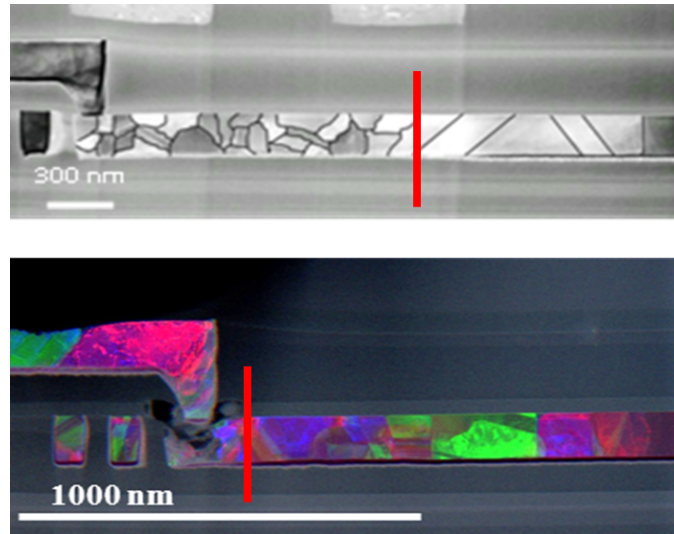


Figure 3-23: [83] (STEM Top) Microstructure description in a BS sample. The polycrystalline profile is seen in the narrower region while the bamboo profile is observed in the wider segment (55 nm node sample). (Very Low Angle Annular Dark Field VLAADF Bottom) Evidence of a void located in the polycrystalline region below via of a BS sample. The color allows qualitative study of void size distribution (vertical red line marks the transition)

Then they explained that bamboo like microstructure in the wide section slow down Cu atoms diffusion resulting in a local effect similar to the Blech short length effect. On the contrary in the present study, experimental results mean that increasing the line section provides the same increase in TTF whatever the microstructure (see Table 3-6). In addition, we have addressed the Cu drift velocity through the evolution of resistance slope (R_{slope}). Comparison of both structures is given in Figure 3-22. In agreement with the previous study [83], the Cu drift velocity is larger for the narrow line width case (TS structure) where the density of preferential diffusion paths is assumed to be the largest. Actually, one can assume that TTF is the sum of a nucleation time (TN) and a growth time (TG)[17], [28] so it means that similar TTF for both TS and BS1 structures but different TG, need to have the largest TN for the structure with the smallest TG. Because it is straightforward that the smallest TG is due to the largest Cu drift ($\approx R_{slope}$) and is obtained for the structure with the narrow line width.

We believe that the distribution of stress in the TS at the cathode reaches the critical stress later to allow the void nucleation time increase. Simulations and characterizations were be done with the multiphysics model of electromigration developed to confirm the stress effect. The void location is assumed very close to the cathode or below the via i.e. the void formation is always in the L1 segment. When the void appears below the via

the electric characteristic has an abrupt increase of resistance and it is not possible to measure the R_{slope} . In the ref [83] is shown that is likely to have this kind of failure (Figure 3-23) with such a structure. This explains why only few samples were available to evaluate the R_{slope} .

BS1 vs TS	BS1	TS
MTF (h)	1046	1038
R_{slope} (Ohm/s)	1.2	2.3

Table 3-6: MTF and mean of R_{slope} of BS1 and TS

In conclusion, BS1 and TS they have similar TTF, but different R_{slope} with the TS one around 2 times greater. This suggested that the TN in this structure has to be necessarily greater to compensate the sum $TTF = TN + TG$. Numerical analysis will be shown in Chapter 4 to confirm this hypothesis.

3.6.2 2nd Study: Local Blech effect [BS vs CS]

In the second study, the lengths of the narrow anode part (L1) of the BS type are varied, while all the other geometrical dimensions are kept similar for both structures. We consider for convenience, the reference structure CS1 and CS2 as BS with L1 respectively equal to 200 μm and zero. The aim is to rate the effect of the distance of narrow transition.

2 nd Study	CS2	BS2	BS3	BS4	CS1
L1	0 μm	5 μm	10 μm	20 μm	200 μm
L2	200 μm	195 μm	190 μm	180 μm	0 μm
W1	—	0.045 μm	0.045 μm	0.045 μm	0.045 μm
W2	0.09 μm	0.09 μm	0.09 μm	0.09 μm	—

Table 3-7: Geometrical test structures parameters of 2nd study ordered according L1 ascending.

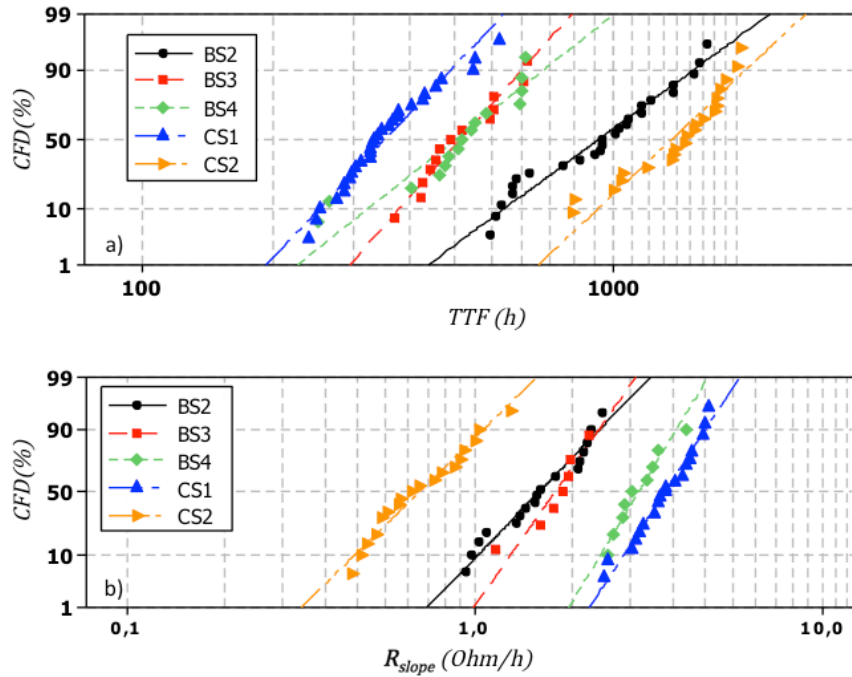


Figure 3-24: 2nd Study: Time to failure (TTF) calculated respectively with the BS2, BS3, BS4, CS1 and CS2 (on the top). R_{slope} comparison (at the bottom).

In Figure 3-24 let us move to the distribution of lifetime (TTF). In this case, the lifetime distribution of each BS is between CS1 with the shortest lifetime and CS2 with the longest lifetime. We obtained for the BS2 structure with the shortest L1 a lifetime 3 times greater than the reference CS1. But when the length of the narrow line width portion is increased the lifetimes of BS structures reaches the lifetime of the constant narrow structure CS1. Figure 3-25 shows the mean TTF as a function of L1. Qualitatively when L1 overcomes 10 μm , it does not provide a considerable lifetime increase. The drift velocity is similar for both BS2 and BS3 (see Figure 3-26) structures where microstructure of the W2 line width part is assumed to be similar. But for BS4 with $L1 = 20 \mu m$, the behavior is closer to the reference structure CS1 with $L1 \gg 0 \mu m$ more grain boundaries are contributing to the Cu diffusion because of the narrow line width.

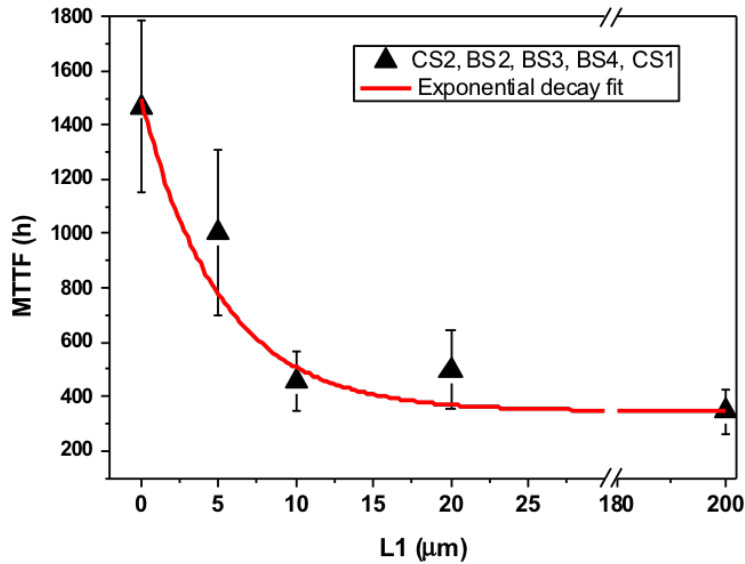


Figure 3-25: 2nd Study: Mean Time to failure (MTTF) calculated respectively with the CS2, BS2, BS3, BS4 and CS1 and fitted with an exponential decreasing law. The MTTF shows a remarkable increase if L1 is smaller than 10 μm, with the error bar that represents the standard deviation.

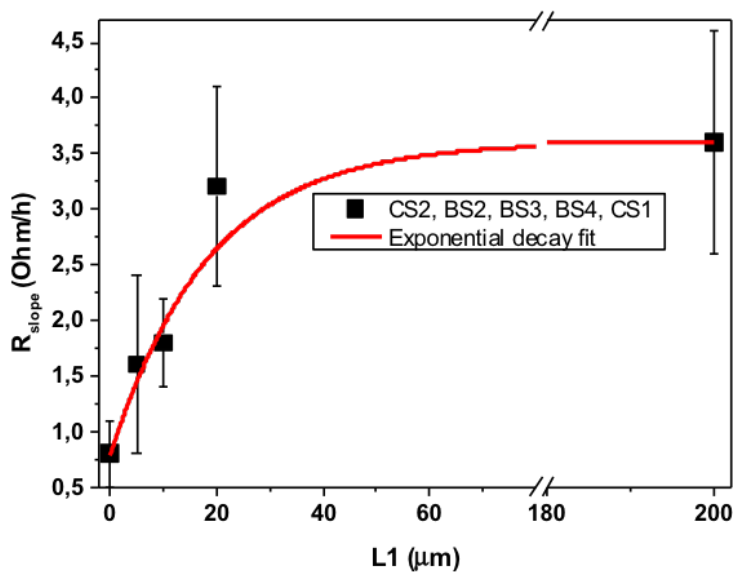


Figure 3-26: 2nd Study: Mean of R_{slope} calculated respectively with the CS2, BS2, BS3, BS4 and CS1 and fitted with exponential asymptotic law. If L1 is increased the R_{slope} converges to the value of the constant narrow structure CS1, with the error bar that represents the standard deviation.

In conclusion, the effect of the variation of the length L1 in the bottle structure has been analyzed. It is shown that if L1 is less than 10 μm the lifetime shows a remarkable increase that makes think to a Local Blech effect. And that also the R_{slope} reduces drastically with the reduction of L1.

3.6.3 3rd Study: width influence on lifetime [BS]

In the third study about BS type (Table 3-8), L1 is kept the same (10 μm) but different W2 are considered i.e. BS1 and BS3. In the order to evaluate if also, the narrow width (W2) has an important effect on the lifetime.

3 rd Study	BS1	BS3
L1	10 μm	10 μm
L2	190 μm	190 μm
W1	0.045 μm	0.045 μm
W2	0.135 μm	0.09 μm
MTTF	1046 h	456 h

Table 3-8: Geometrical test structures parameters of 3rd study.

In addition, in the third study the lifetime of BS1 is 2 times greater than BS3 (see Table 3-9), so we can assume that also the narrow width (the only geometrical difference) has an important effect on the lifetime.

BS vs BS	BS1	BS3
MTF (h)	1046	456
R_{slope} (Ohm/s)	1.2	1.8

Table 3-9: MTF and mean R_{slope} of BS1 and BS3, same L1 and L2 (10 μm) with a width of 3 W1 and 2 W1 respectively.

3.6.4 Conclusions

Interconnect lifetimes are increased in complex test structures using line width transitions or splitting the line into many branches. This lifetime increase is not only due to the microstructure, where fewer grains helps in lowering the Cu diffusion path. A mechanical stress effect is suspected to be added. Then the lifetime increase effect is limited to a fixed line length of about 10 μm here. These results can be applied to product design responding to specific requests that need more in-depth analysis than the classical electromigration test structure. Taking into account these configurations will increase the accuracy of reliability prediction at design level and help designers with high current density needs.

3.7 Effective charge experimental evaluation

For this study Blech structures has been used. These structures SSV are short enough to activate the condition of immortality defined as $JL = JL_c$, with J the density of current and L_c the critical length explained in the previous section, to which the structures are no more subjected to degradation by electromigration.

We have carried out EM experiments with a fixed stress current and temperature on a population of 16 Blech structures 10 μ m long with a section of 4500 nm² for 1800 h at 0.1 mA and 300 °C (larger test time than usual for standard EM test). As expected most of the structures did not fail due to the short length effect as shown in Figure 3-27.

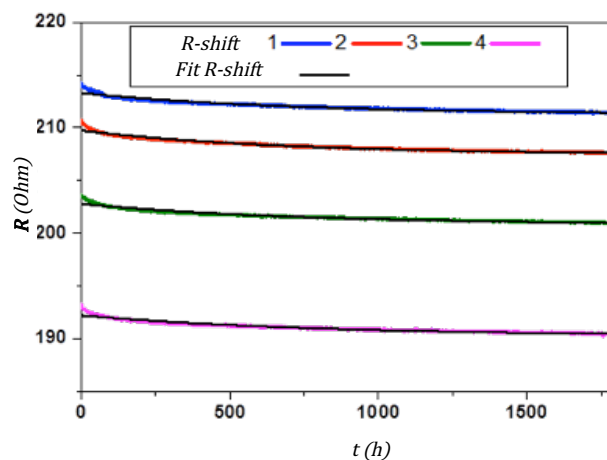


Figure 3-27: Resistance versus Time examples of some Blech Test lines fitted with an exponential decreasing law. Some of these lines were subsequently analyzed by TEM to confirm the presence of a void (Figure 3-28). The examples shown did not fail due to the short length effect.

The objective is to have a fully void formed under effect of electromigration that cannot grow up anymore due to the directionally opposite flux of Blech, as explained previously. It has been hypothesized, that this equilibrium condition has been reached before the characteristic jump of the resistance; and then a void was necessary fully formed to reach this equilibrium condition causing the immortality of the test structure, the mainly difference with the study of Lamontagne [89] is that the void stop to grow before reaching the metallic barrier. Then, morphological analysis are necessary to confirm that actually a void is fully formed in the line at the cathode as shown in Figure 3-28 and these morphological analysis allowed us especially to quantify this volume of saturation for 2 samples. This evaluation classically is done evaluating the size of the jump of the resistance[90], [29].

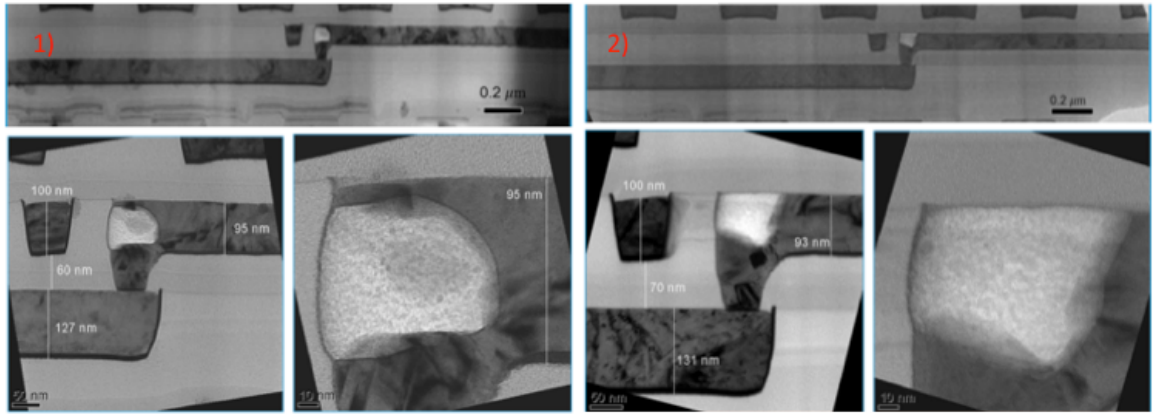


Figure 3-28: TEM cross-sections of 2 samples of the Blech-Test structure stressed for 1800 h. These analyses confirm the presence of a fully formed void undetectable with usual EM-tests.

The void volume calculation was done by a graphical method that allows isolating the portion of the line with void from the rest of the line and then calculating the void area. From the void area then it is possible to calculate either an equivalent spheroidal (S_v) and parallelepipedal (P_v) volume, as follows:

$$P_v = Area * d \quad S_v = \frac{4}{3} \pi r_a^3 \quad \text{Equation 3-3}$$

Where $Area$ is the area calculated from morphological analysis TEM Figure 3-28, d the depth of the copper line (here = 50nm); and r_a is the radius calculated from $Area$ considering this as the area of an equivalent circle. Finally, every TEM analysis allows the calculation of two volumes of saturation (V_{sat}) and then of two Z^* with the following equation:

$$Z^* = \frac{\Omega V_{sat} 2B}{Ae\rho} \frac{1}{JL^2} \quad \text{Equation 3-4}$$

Where B is the elastic effective module, A the section of the line considering only the copper section, e the charge of an electron, ρ the resistivity of Cu, J the current density, Ω the atomic volume of copper ($1.18 \times 10^{-23} \text{cm}^3$ [52]) and L the length of the line. The elastic effective module was calculated with the correct geometry and mechanical properties of the experimental test structures used. Detailed information about the formula can be found in [90]. The effective charge found with this method are coherent with Z^* found in other works (e.g. [52] [43]).

Parameter	Pv		Sv	
V _{sat}	2.66e5nm ³	2.83e5nm ³	2.91e5nm ³	3.21e5nm ⁵
Z*	-2.85	-3.04	-3.12	-3.44

Table 3-10: Summary of volumes of saturation V_{sat} and relative charge effectiveness Z* found.

3.8 Conclusion

In this Chapter, the SSV the classic methodology to evaluate the reliability of a technology by analyzing the distribution of lifetime for different condition is shown. Then, the LSS structure is presented and compared to the SSV. This structure allows calculating experimentally the “void nucleation”. Complementary morphological analysis have been shown to demonstrate the validity of this test structure. This characteristic new time calculated experimentally represents the first damage of the line measured.

Then, the fundamental parameters of this technology are extracted: n and E_a by using classically the SSV and originally the LSS. It is interesting to highlight that the factor of current calculated from LSS (TN distribution) is around one, the explanation is that TN is considered as TTF that certainly does not present an “incubation time” [80], in fact the n factor around one is obtained the lifetime is dominated by growth.

Morphological analysis necessary to gain complementary information and for further investigations have been done. Subsequently, the different relevant parameters are shown and their relative statistical analysis is detailed. Finally, it is shown in detail how the calculation of the effective charge (Z*) is performed originally with the morphological analysis together with the electrical characterization.

Chapter 0:

4 SIMULATIONS STUDIES OF ELECTROMIGRATION

In the previous section, the different physical phenomena related to electromigration were described and meaningful physically based models were shown. The majority of these models are based on several simplifying assumptions in order to obtain analytical expressions, or they can be applied exclusively for simulation of simple interconnect geometries. Thus, they cannot handle with the complex modern interconnect structures, as that shown in Figure 4-1. In this Chapter, a universal electromigration model for implementation in a COMSOL tool for simulation of realistic three-dimensional interconnects structures is developed.

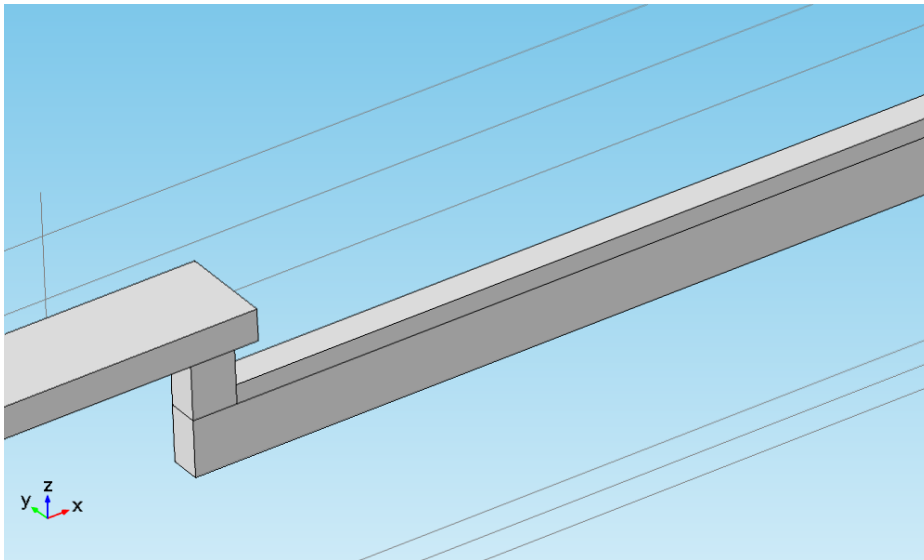


Figure 4-1: Dual-damascene interconnect structure.

The electromigration simulation necessitates a Multiphysics approach. Thus the model equations can be most opportunely divided into smaller blocks. At first, the electro-thermal problem, the distributions of electric potential, electric field, current density,

and temperature in the interconnect are shown. Then, the material transport equations are presented. The mechanical equations, which define the deformation and the resultant hydrostatic stress evolution in the line, are explained. Subsequently, a concise model overview is given, where the summary of equations is presented i.e. the equations which have to be resolved to perform electromigration simulations. Finally, several electromigration simulation examples according to the model discussed are presented and a new methodology to calculate the critical stress of “void formation”. Then, the special structures described in the second chapter are reproduced and analyzed to confirm assumptions previously done. Finally, the initial concentration impact on the time of nucleation is addressed.

4.1 The electro-thermal problem

Representing the electric potential at any point in the line by φ and the electrical conductivity by γ_E , the current density \vec{j} can be calculated from Ohm's law as:

$$\vec{j} = \gamma_E \vec{E} = -\gamma_E \nabla \varphi \quad \text{Equation 4-1}$$

where the electric field \vec{E} is related to the electric potential by:

$$\vec{E} = -\nabla \varphi \quad \text{Equation 4-2}$$

Because the electric charge should obviously be conserved:

$$\nabla \cdot \vec{j} = 0 \quad \text{Equation 4-3}$$

which together with **Equation 3-3** yields an equation written for the electric potential,

$$\nabla \cdot (\gamma_E \nabla \varphi) = 0 \quad \text{Equation 4-4}$$

Note that **Equation 4-4** reduces to the Laplace equation (if the electrical conductivity is constant along the line):

$$\nabla^2 \varphi = 0 \quad \text{Equation 4-5}$$

The solution of the thermal problem determines the temperature distribution:

$$\nabla \cdot (\gamma_T \nabla T) = \rho_m c_p \frac{\partial T}{\partial t} - p \quad \text{Equation 4-6}$$

where γ_T is the material thermal conductivity, ρ_m is the mass density, and C_p is the specific heat. Here, p is the electrical power loss density, given by:

$$p = \gamma_E E^2 = \gamma_E (\nabla \phi)^2 \quad \text{Equation 4-7}$$

Which accounts for the Joule heating and couples the electrical with the thermal problem. Together, the electrical and thermal conductivity are treated as temperature dependent parameters, with the following form:

$$\gamma(T) = \frac{\gamma_0}{1 + \alpha(T - T_0) + \beta(T - T_0)^2} \quad \text{Equation 4-8}$$

Where γ_0 is the conductivity for a given reference temperature T_0 . The linear and quadratic temperature coefficients are respectively: α and β . The equations **Equation 4-4** and **Equation 4-6**, together with **Equation 4-7** and **Equation 4-8**, compose a non-linear system, whose solution gives the voltage, electric field, current density, and temperature distributions in an interconnect line. It should be emphasized that particular attention must be taken in setting the thermal boundary conditions. In order to appropriately consider the effect of Joule heating, an appropriate portion of dielectric surrounding must be included in the simulation. The thermal reservoir has been implemented by a Dirichlet boundary condition for the temperature.

4.2 Material transport equations

The whole atomic transport which occurs in an interconnect line during electromigration is the sum of the various driving forces for atomic migration activated by temperature, hydrostatic stress, electrical potential and vacancy concentration. As in copper metallization, atomic migration happens via vacancy diffusion mechanisms, the total material transport can be equivalently written in terms of vacancies. Therefore, the combination of the driving forces leads to the total vacancy flux of the form [58][91]:

$$\vec{J}_v = \sum J_i = J_1 + J_2 + J_3 + J_4 \quad \text{Equation 4-9}$$

In this equation the first term J_1 describes a diffusional effect “The Fickian term”, the second term J_2 represents the electromigration, the third term J_3 accounts for the atomic migration caused by gradients of mechanical stress, and the last term J_4 illustrates the material transport which occurs due to thermal gradients in the interconnect. Mathematic expressions of these terms are summarized in Table 4-1 [92] [93].

Table 4-1: The total vacancy flux is the sum of four contributors

The vacancy flux components		
J_1	Fick's Law	$-D_v \nabla C_v$
J_2	EM term	$-\frac{D_v C_v}{KT} Z^* e \nabla \varphi$
J_3	Mech. Grad.	$-\frac{D_v C_v}{KT} f \Omega \nabla \sigma$
J_4	Therm. Grad.	$-\frac{D_v C_v}{KT} \frac{Q^*}{T} \nabla T$

Two mainly mechanisms contribute to a local variation in vacancy concentration. In the first one vacancies accumulate or disappear due to the existence of flux divergences. In the second, the generation or annihilation of vacancies in the presence of source/sink mechanisms alters the vacancy concentration. Accordingly, material balance is described by the continuity equation:

$$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J}_v + G \quad \text{Equation 4-10}$$

Where G is a function which models vacancy generation/annihilation processes. Vacancy generation or annihilation is related to the change of lattice sites. Then, this term is active only at the appropriate interfaces, like grain boundaries and material interfaces [94]. In order to calibrate the model with the standard electrical characterization available explained in section 3 an equivalent G for the whole line has been used.

4.3 Electromigration Induced Stress

Considering an ideal crystal lattice as shown in Figure 4-2 (a), the effect of introducing a vacancy is schematically presented in Figure 4-2 (b). It shows that the volume of a vacancy occupied is different from the volume of the atom. In fact, a vacancy occupies less volume than an atom inducing relaxation in the lattice. Consequently, a change in vacancy concentration induces strain in the lattice due to its relaxation in a confined environment. Because in a typical interconnect structure the metal line is completely embedded in a passivation layer, this strain field cannot be accommodated. Then this lead to the development of mechanical stress.

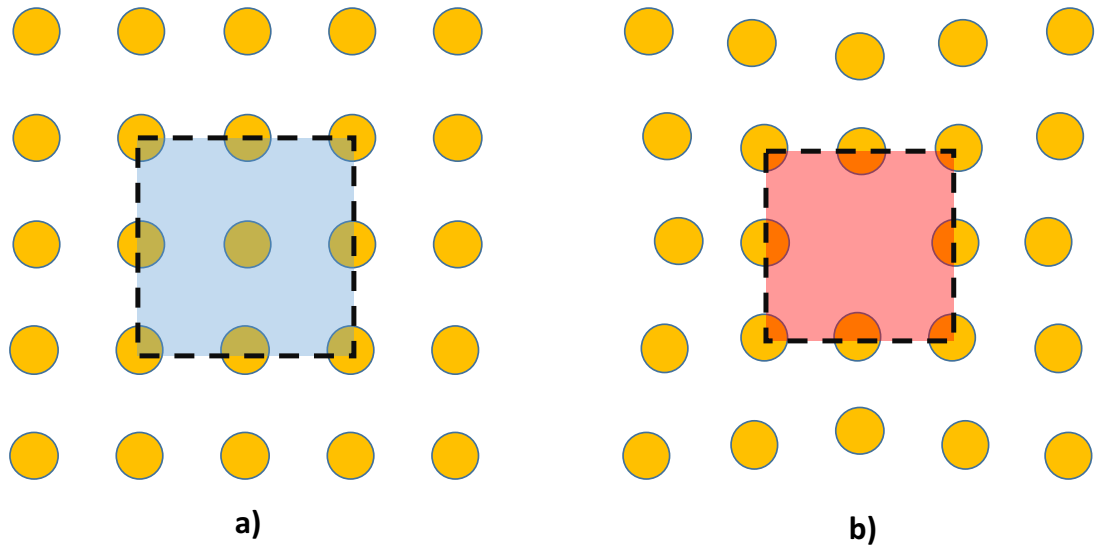


Figure 4-2: Effect of a vacancy in an ideal crystal lattice. (a) Initial lattice. (b) Deformed lattice.

As previously described in Chapter 3, the variation in vacancy concentration at any point of an interconnect happens either by a vacancy-atom exchange mechanism or, at interfaces, by the production or annihilation of vacancies with source/sink mechanism. This signifies that the strain induced by electromigration has two input: a migration component related with the vacancy-atom exchange process, and a component associated to vacancy production/annihilation.

4.3.1 Strain due to Vacancy Migration

When an atom is replaced for a vacancy, the adjacent atoms relax, leading to a total volume change given by:

$$\Delta V = \Omega_v - \Omega = (1 - f)\Omega. \quad \text{Equation 4-11}$$

For a volume V (Ω_v, Ω respectively vacancy volume and atomic copper volume), the relative volume change associated with a change in vacancy concentration ΔC_v is [95]:

$$\frac{\Delta V}{V} = -(1 - f)\Omega\Delta C_v \quad \text{Equation 4-12}$$

so the volumetric strain has the form:

$$\frac{\Delta V}{V} = \varepsilon_{11}^m + \varepsilon_{22}^m + \varepsilon_{33}^m = 3\varepsilon^m = -(1 - f)\Omega\Delta C_v \quad \text{Equation 4-13}$$

where ε^m indicates to the migration strain.

Taking the time derivative of the previous equation is obtained:

$$\frac{\partial \varepsilon^m}{\partial t} = -\frac{1}{3}(1-f)\Omega \frac{\partial C_v}{\partial t} \quad \text{Equation 4-14}$$

and, since for the test volume the atom-vacancy exchange is governed by the continuity equation.

$$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{J}_v \quad \text{Equation 4-15}$$

the components of the migration strain rate is given by:

$$\frac{\partial \varepsilon_{ij}^m}{\partial t} = \left[\frac{1}{3}(1-f)\Omega \nabla \cdot \vec{J}_v \right] \delta_{ij} \quad \text{Equation 4-16}$$

4.3.2 Strain due to Vacancy Generation/Annihilation

The generation/annihilation of vacancies is accompanied by a change in the concentration of lattice sites, so that $\Delta C_v = \Delta C_L$ [94]. Therefore, the relative volume change of a given test volume due to the addition or removal of lattice sites through a change in the local vacancy concentration ΔC_v by means of generation/annihilation processes is [95]:

$$\frac{\Delta V}{V} = f\Omega \Delta C_v \quad \text{Equation 4-17}$$

where $f\Omega$ accounts for the vacancy volume. Following the same procedure as described above, the strain rate is given by:

$$\frac{\partial \varepsilon^g}{\partial t} = \frac{1}{3}f\Omega \frac{\partial C_v}{\partial t} \quad \text{Equation 4-18}$$

where ε^g refers to the strain produced due to vacancy generation/annihilation processes. Since the variation in vacancy concentration C_v is given, in this case, only by generation or annihilation developments:

$$\frac{\partial C_v}{\partial t} = G \quad \text{Equation 4-19}$$

which leads to the generation/annihilation strain rate components:

$$\frac{\partial \varepsilon_{ij}^g}{\partial t} = \left[\frac{1}{3}f\Omega G \right] \delta_{ij} \quad \text{Equation 4-20}$$

4.3.3 Total Electromigration Strain

The electromigration total strain induced is given by the sum of the vacancy migration and vacancy generation/annihilation components:

$$\varepsilon_{ij}^v = \varepsilon_{ij}^m + \varepsilon_{ij}^g \quad \text{Equation 4-21}$$

Taking the time derivative of **Equation 4-21**, and using **Equation 4-16**, the total strain rate produced by electromigration is given by:

$$\frac{\partial \varepsilon_{ij}^v}{\partial t} = \frac{1}{3} \Omega [(1-f) \nabla \cdot \vec{J}_v + fG] \delta_{ij} \quad \text{Equation 4-22}$$

Since ε_{ij}^v is a diagonal tensor with equal entries, one can write **Equation 4-22** in terms of the trace of the strain tensor:

$$\frac{\partial \varepsilon^v}{\partial t} = \Omega [(1-f) \nabla \cdot \vec{J}_v + fG] \quad \text{Equation 4-23}$$

Specified the dependence of the EM-induced strain on the source function G , the modeling approach for mechanisms of generation/annihilation of vacancies becomes of central importance.

4.4 Mechanical Deformation

The material transport due to electromigration yields local strain, which causes to the deformation of the interconnect line. This deformation is defined by the displacement field, \vec{u} , of points in the line with respect to a stress-free initial configuration. Assuming that the displacements from the reference configuration are small, the line deformation is characterized by the total strain [96]:

$$\varepsilon_{ij} = \frac{1}{2} \left(\frac{\partial u_i}{\partial u_j} + \frac{\partial u_j}{\partial u_i} \right), \quad i, j = 1, 2, 3 \quad \text{Equation 4-24}$$

which can be written in matrix notation as:

$$\varepsilon = S u \quad \text{Equation 4-25}$$

with

$$\varepsilon = [\varepsilon_{11} \ \varepsilon_{22} \ \varepsilon_{33} \ \gamma_{12} \ \gamma_{23} \ \gamma_{31}]^T \quad \text{Equation 4-26}$$

Where symmetry of the strain tensor is assumed and the engineering shear strains are used:

$$\gamma_{ij} = 2\varepsilon_{ij}, \quad i \neq j \quad \text{Equation 4-27}$$

The strain operator S is given by:

$$S = \begin{pmatrix} \frac{\partial}{\partial x_1} & 0 & 0 \\ 0 & \frac{\partial}{\partial x_2} & 0 \\ 0 & 0 & \frac{\partial}{\partial x_3} \\ \frac{\partial}{\partial x_2} & \frac{\partial}{\partial x_1} & 0 \\ 0 & \frac{\partial}{\partial x_3} & \frac{\partial}{\partial x_2} \\ \frac{\partial}{\partial x_3} & 0 & \frac{\partial}{\partial x_1} \end{pmatrix} \quad \text{Equation 4-28}$$

The total strain has contributions from different sources: the elastic distortion of the line, the thermal strain, and the strain induced by variations in vacancy concentration. Therefore, we can write, respectively:

$$\boldsymbol{\varepsilon} = \boldsymbol{\varepsilon}^e + \boldsymbol{\varepsilon}^{th} + \boldsymbol{\varepsilon}^v \quad \text{Equation 4-29}$$

Where the thermal matrix of strain is:

$$\boldsymbol{\varepsilon}^{th} = \alpha(T - T_0)I \quad \text{Equation 4-30}$$

and the EM-induced matrix of strain is (with ε^v determined by **Equation 4-23**):

$$\boldsymbol{\varepsilon}^v = \frac{1}{3}\varepsilon^v I \quad \text{Equation 4-31}$$

Assuming an elastic deformation of the interconnect, which means that Hooke's law applies, the stress is related to the elastic strain by:

$$\boldsymbol{\sigma} = C\boldsymbol{\varepsilon}^e \quad \text{Equation 4-32}$$

which together with **Equation 4-29**:

$$\boldsymbol{\sigma} = C(\boldsymbol{\varepsilon} - \boldsymbol{\varepsilon}_0) \quad \text{Equation 4-33}$$

Where

$$\boldsymbol{\varepsilon}_0 = \boldsymbol{\varepsilon}^{th} + \boldsymbol{\varepsilon}^v \quad \text{Equation 4-34}$$

represents the total inelastic strain. Here, the stresses should satisfy the mechanical equilibrium equations:

$$\nabla \cdot \boldsymbol{\sigma} = \mathbf{0} \quad \text{Equation 4-35}$$

since it is assumed that there are no external forces acting on the line during electromigration.

4.5 Model simplifications

In a first approach we tried to reproduce this phenomenon in a detailed way as the work of De Orio [52] including: grain boundaries, dislocations and interfaces that can act as sinks and sources for vacancies in metals. But subsequently a compactness of the model has been preferred as explained subsequently in this Chapter. Due to the difficulty to find out experimentally certain fundamental parameters with standard characterization available during the project and furthermore due to the excessive time of simulations and their instability it has been preferred to simplify the model. If, on the one hand, has been lost a bit of precision in the representation of the physical phenomena of electromigration, on the other hand, this has allowed having results in a reasonable time. But this approach has been chosen principally to calibrate the model with sensible time and few standard test. This methodology will allow using the same approach and model for futures technologies. Moreover, the metallic barrier of the test line of only few nm has not been reproduced for the sake of stability of the simulations.

4.6 Model summary

The developed electromigration model contains several submodels. The conservative mass balance **Equation 4-10** is solved by coupling the corresponding Laplace's current equation, **Equation 4-4**, the mechanical equilibrium equation, **Equation 2-35**, and the Fourier's thermal equation, **Equation 4-6**. The four equations are solved simultaneously in transient state.

Balance conservative equation	Laplace's current equation	Mechanical equilibrium equation	Fourier's thermal equation
$\frac{\partial C_v}{\partial t} = -\nabla \cdot \vec{j}_v + G$	$\nabla \cdot (\gamma_E \nabla \varphi) = 0$	$\nabla \cdot \sigma = 0$	$\nabla \cdot (\gamma_T \nabla T) = \rho_m c_p \frac{\partial T}{\partial t} - p$

Table 4-2: Model summary

The electromigration strain rate part has two origins: the first one is the vacancy flux divergence and the second is the vacancy generation/annihilation. For this model the generation/annihilation or source term G Sarychev model [91] has been used:

$$G = \frac{C_v - C_{v0} \frac{\Omega \sigma}{k_b T}}{\tau} \quad \text{Equation 4-36}$$

With C_{v0} as the initial concentration. The **Equation 4-22** expresses the diagonal tensor of the total electromigration strain. The resulting line deformation and mechanical stress is determined by the set of equations shown in the Table 4-3 (respectively **Equation 4-25, Equation 4-35, Equation 4-33**):

Total strain	Mechanical equilibrium equation	Hooke's law
$\varepsilon = Su$	$\nabla \cdot \sigma = 0$	$\sigma = C(\varepsilon - \varepsilon_0)$

Table 4-3: deformation and mechanical stress

The solution of these equations permits a complete cycle of simulation of electromigration in general three-dimensional interconnect structures.

4.7 Model numerical implementation

Very frequently the mathematical description of physical phenomena consists of partial differential equations (PDE's) defined in a limited domain of interest. These equations can be analytically resolved only for simple problems. Therefore, for complicated geometries and problems, involving variable material properties and general boundary conditions, numerical methods have to be applied.

Considering the model proposed in this chapter, the finite element method (FEM) has been chosen as numerical solving, developed on COMSOL simulation tool. FEM grants a solid mathematical formulation for solving several types of PDE's and can handle intricate geometries with different types of boundary conditions. Furthermore, since it was originally conceived for solving mechanical problems, it is adequately convenient for the model implementation. A severe mathematical treatment is outside the scope of this thesis and can be found elsewhere [96]. Since electromigration constitutes a multi-physics problem, it is convenient to divide it into smaller sub-problems and to solve each one separately. The electro-thermal problem is directed by partial differential equations for the electric potential, φ , and for the temperature, T . The variable of concern for the vacancy dynamics is the vacancy concentration, C_v . The mechanical problem is expressed in terms of the displacement field, \vec{u} , nevertheless, the mechanical stress found from the solution of the mechanical problem is the variable of interest here. Each sub-problem is solved for the corresponding variable, while the variables of the other sub-problems are fixed. In order to obtain an appropriate resolution for vacancy dynamics close to the cathode (zone of major interest for the “void nucleation”) of the interconnect metal with the surrounding layers, an appropriately fine FEM mesh has to be provided at these locations. Therefore, a simple local mesh refinement procedure was implemented. The procedure first detects the elements with nodes connected to more than one segment. If the tetrahedron volume is larger than a given value, the corresponding tetrahedron is refined. This procedure can be executed recursively, until all tetrahedrons connected to the interface have a volume smaller than the specified one. A compromise has been necessary found between simulation time, refining solution and stability of the simulation. First, the solution of the electro-thermal problem establishes the electric potential and temperature distribution in the modeled test line. These quantities are then used to obtain the vacancy concentration change due to the whole mass transport happening under electromigration and accompanying driving forces. The rate of change of vacancy concentration due to generation/annihilation processes is found. The variation in vacancy concentration establishes the induced strain, which loads the mechanical problem. The solution of the mechanical system produces the deformation of the test line, consequently that the mechanical stress can be estimated. If the size of the developed stress gets the threshold value for “void nucleation”, the simulation procedure is ended and the resultant time for void nucleation can be estimated, or else the time of nucleation could be set to evaluate the stress at that time.

Since the electric potential and temperature distribution reach a steady state condition on a time scale much smaller than that for the vacancy concentration and mechanical stress, the electro-thermal problem is classically solved only for a few initial time steps.

4.8 FEM complementary platform for the prediction of EM failure

The introduction of coupling of experimental observation and numerical simulations is clearly necessary, as shown in many parallels and previous works. This eventually even allows to disprove semi-empirical models used for more than 60 years, as the n factor recently demonstrated be more linked to the residual stress, current and temperature [97], than the dominant lifetime mechanism of degradation (i.e. “void nucleation or void growth”). Furthermore, It has been shown the importance to consider the hydrostatic stress in the power-grid and not only the density of current to have a correct evaluation of EM lifetime [98]. Other works were focused on the study of the atomic flux divergence or mass flux divergence AFD or MFD, as representative of the zone at high risk of degradation with good results, at circuit levels [99] and for “highly robust design” structures [100], [101]; the authors demonstrated being able to predict the zone that will be damaged for first with simulations evaluating the AFD, and confirming with the morphological analysis subsequently. Some efforts to prepare models that account the statistical nature of the EM phenomenon due to a random grain size distribution were done also [102]. However, the approach of using the simulations as a complementary tool needs to be adjusted case to case. This will allow to formulate routines (as in this document) that consent to extract delicate parameters, evaluate eventually the lifetime, calibrate the model, confirm the experimental data etc. etc. For example herein the test lines modeled do not have complex geometries, as e.g. at circuit level with many edges sources of divergences. And also the density of current and the temperature for almost the simulation are constant. Consequently it is more appropriate to study the cause origin of the void nucleation, i.e. the amount of hydrostatic stress, taking advantage of the fact that we were able to find experimental parameters as the Z^* used as simulation material parameter, and the TN used to evaluate the state of hydrostatic stress at that characteristic time.

4.9 Simulation Studies of Electromigration

In this Chapter, several electromigration simulation studies according to the model discussed are presented. First, the materials considered in the simulations are introduced. The vacancy dynamics behavior is analyzed it is clearly shown the importance of the stress effect on the electromigration failure development. The sites where the void is likely to spawn are addressed. It is shown a new methodology how to calculate a critical parameter for design as the critical stress of nucleation, taking into account the experimental data previously exposed in Chapter 3. This enables to explain several features of failure development commonly observed in experiments, for which the simple effective diffusion models cannot handle with. Then, the special structures used for focused design of an interconnect are presented. Finally, the influence of the initial concentration on the electromigration has been studied parametrically.

4.9.1 Material and Simulation Parameters

The following simulations are focused on copper dual-damascene interconnect structures of the 28nm technology nodes that includes a CuMn seed layer. The commonly materials used in such interconnects are: as conductor metal copper (Cu), as barrier layers at the sides and bottom of the lines tantalum based (TaN/Ta), as capping layers silicon nitride based (SiN/SiCN), and as low-k interlevel dielectrics SiCOH.

The Annex presents the materials parameters for the electro-thermal, vacancy dynamics and mechanical deformation problem. Many of these parameters were obtained experimentally the rest was chosen from the literature. Because electromigration just takes place in the conductor line, the parameters related to the material transport equations are presented only for copper.

Electromigration experiments executed under accelerated test conditions as shown in Chapter 3, which means that the interconnect lines are commonly tested at a higher temperature and higher current than that found at use conditions. Consequently, the simulations results presented in the next sections follow this trend. The test lines have the same geometries of test structures used for experimental characterization i.e. are 100

μm long with a height of the copper of 90 nm and a width of 45 nm. A current of 0.1 mA has been used (around $2,2 \text{ MA}/\text{cm}^2$) and a temperature of $300 \text{ }^\circ\text{C}$, as a boundary condition on the external surfaces of the SiOC box. The dielectric box has a height and width of $1 \mu\text{m}$ and a length of $102 \mu\text{m}$. The test line simulated has been positioned exactly in the middle of the box. The objective is to reproduce as accurately as possible the same conditions of the experimental characterization conducted.

4.9.2 Sites of Void Nucleation

Figure 4-3 shows the vacancy distribution in an interconnect via. The current flows from anode to cathode, driving vacancies towards the via. Vacancies accumulate at this site, since the barrier layer blocks additional vacancy diffusion into the upper metal line. Therefore, the maximum vacancy concentration is situated beneath the via and so also the maximum hydrostatic stress. Nevertheless, as previously pointed out, grain boundaries also act as weak spot. Consequently, it is usual to have void formation at sites away from the anode end of the line. Void nucleation detected at the copper/capping layer away from the cathode end is only possible if there is an available site where flux divergence happens and/or is a site of weak adhesion. Grain boundaries are the unique feature, which can provide such sites. Because triple points formed by the intersection of grain boundaries with the copper/capping layer interface are natural region of flux divergence and also weak adhesion [103].

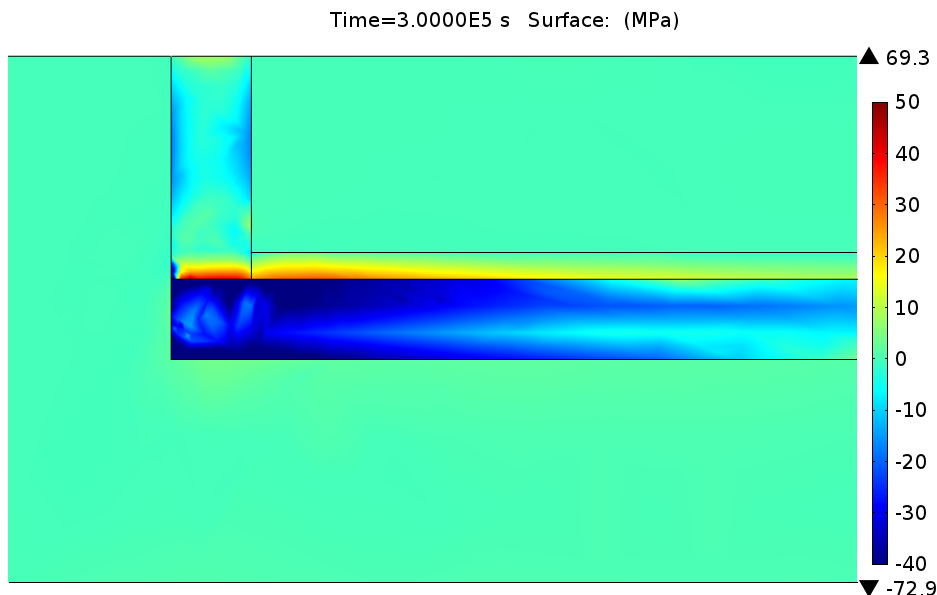


Figure 4-3: Example of Hydrostatic stress on a 2D cut solution along the direction x zoomed on the cathode.

4.9.3 Critical stress of void formation extrapolation

A new method to extrapolate the critical stress of void formation is proposed. In section 2 has been shown how to find experimentally the effective charge from the volume of saturation and the mean nucleation time (TN) experimentally for the same conditions used in the simulations. This new method consists of isolating the model solution that corresponds to the mean TN experimentally found. Then considering that the void is always really close to the cathode, it is possible to evaluate the critical stress with the assumption that the void is likely to appear not farther than 500 nm from the cathode; as shown e.g. in Figure 4-5.

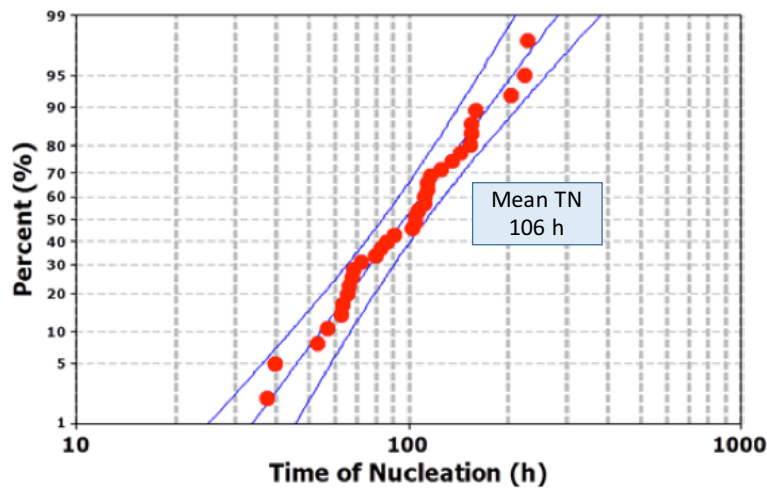


Figure 4-4: Time of nucleation (Tn) evaluated with the LSS [79] at the same conditions of the simulations i.e. at 0.1 mA and 300°C

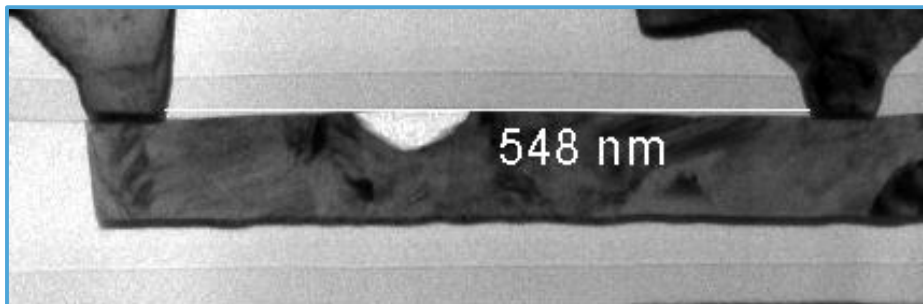


Figure 4-5: Example TEM cross-section of LSS detected electrically. This analysis confirms the presence of a void fully formed undetectable with conventional EM-test structures. Furthermore, the distance of the voltage tap from the cathode is shown.

Assuming realistically (see Chapter 3) that the void does not spawn more than 500nm from the cathode, the range of possible critical stress depends only on the distance from the cathode as shown in Figure 4-6. Therefore, knowing the distance range allows to find the real critical stress of void nucleation for this technology from the solutions of the simulations.

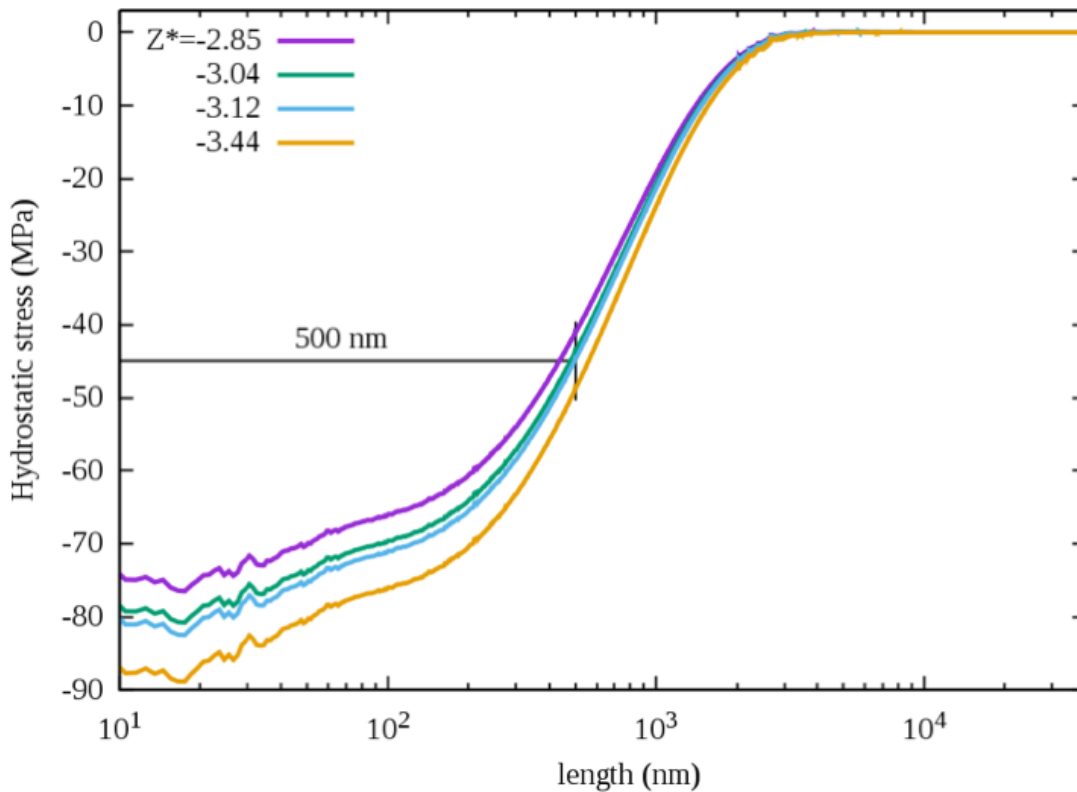


Figure 4-6: Evolution of the hydrostatic stress along the x direction at the TN found experimentally for every effective charge. This allowed the evaluation of the hydrostatic stress on the cathode at 0 nm and at 500 nm

4.9.4 Focused design test structures

In order to design reliable interconnects against electromigration, a big effort has been put into investigating materials, which produce preferable properties. However, another strategy which is commonly used to improve the interconnect resistance against

electromigration is the introduction of specific geometrical features, such as material reservoirs [83] and redundant vias [87]. In this paragraph some simulation results for the bottle structure and the trident structure, are presented. In this way, the impact of these geometries on the interconnect behavior regarding electromigration can be analyzed to confirm previous experimental results.

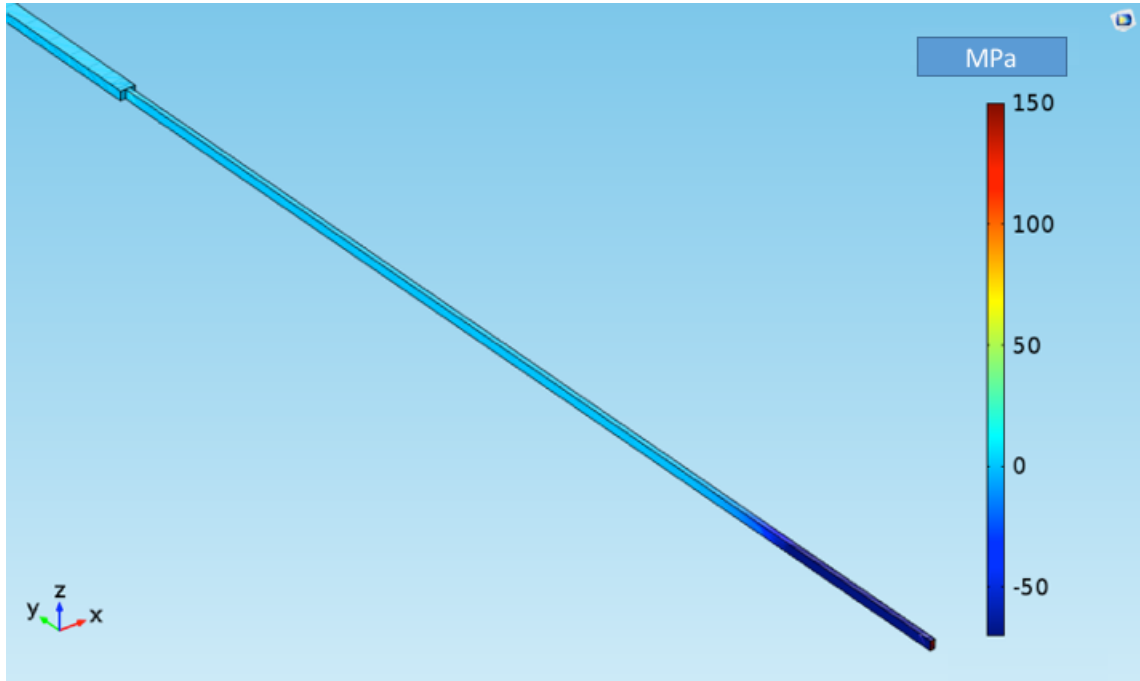


Figure 4-7: Bottle structures interconnect hydrostatic stress distribution

Figure 4-7 shows the hydrostatic stress distribution in the bottle structure. The maximum hydrostatic stress measured at 106h (the TN found for the same technology, see Figure 4-4) is on the cathode, as shown in Figure 4-8, and it is around 55 MPa. The stress developed in the interconnect with the bottle structure design via is smaller than that developed in the single via structure, see Figure 4-6. The introduction of an enlargement reduces the overall interconnect resistance. As the current applied at the terminals of the interconnect is the same, the reduction of the interconnect resistance leads to a decrease of the voltage. Consequently, the driving force for material transport along the line is decreased, and fewer vacancies concentrate under the cathode via, producing a smaller stress.

In Chapter 2 has been demonstrated the benefit to use this design structure, about increasing of lifetime. The model results actually confirm that the hydrostatic stress reached in the same time is significantly less as expected. So that means that the time of

nucleation and the lifetime is larger for this design.

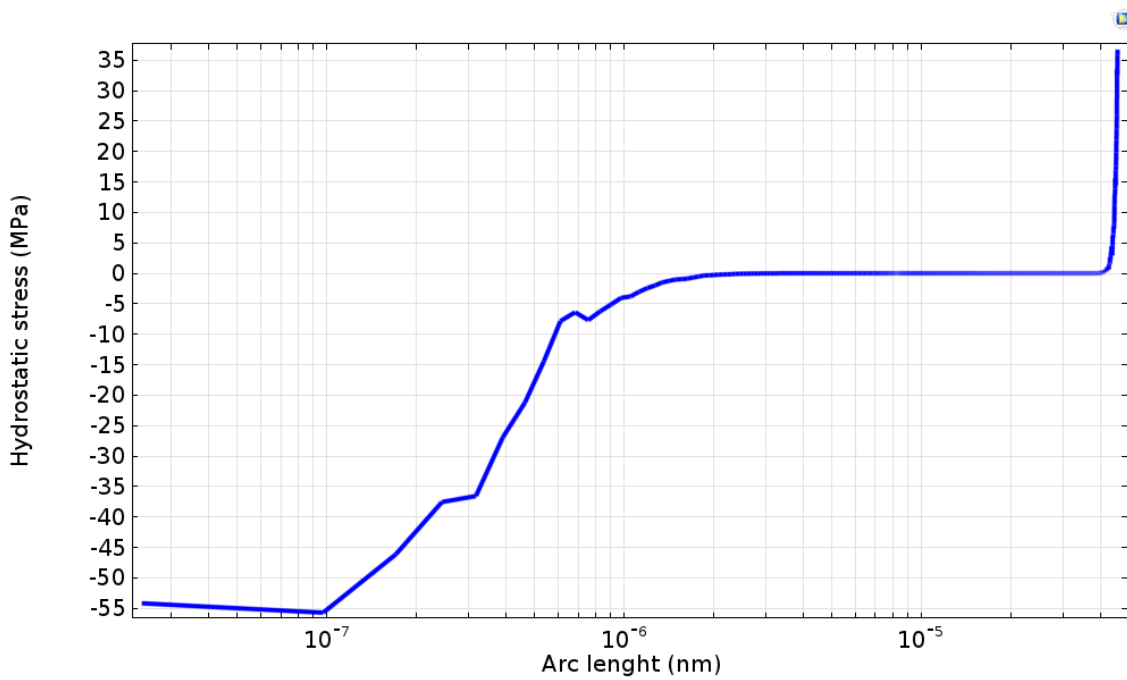


Figure 4-8: hydrostatic stress along the x direction at the TN found experimentally of 106h for the BS1.

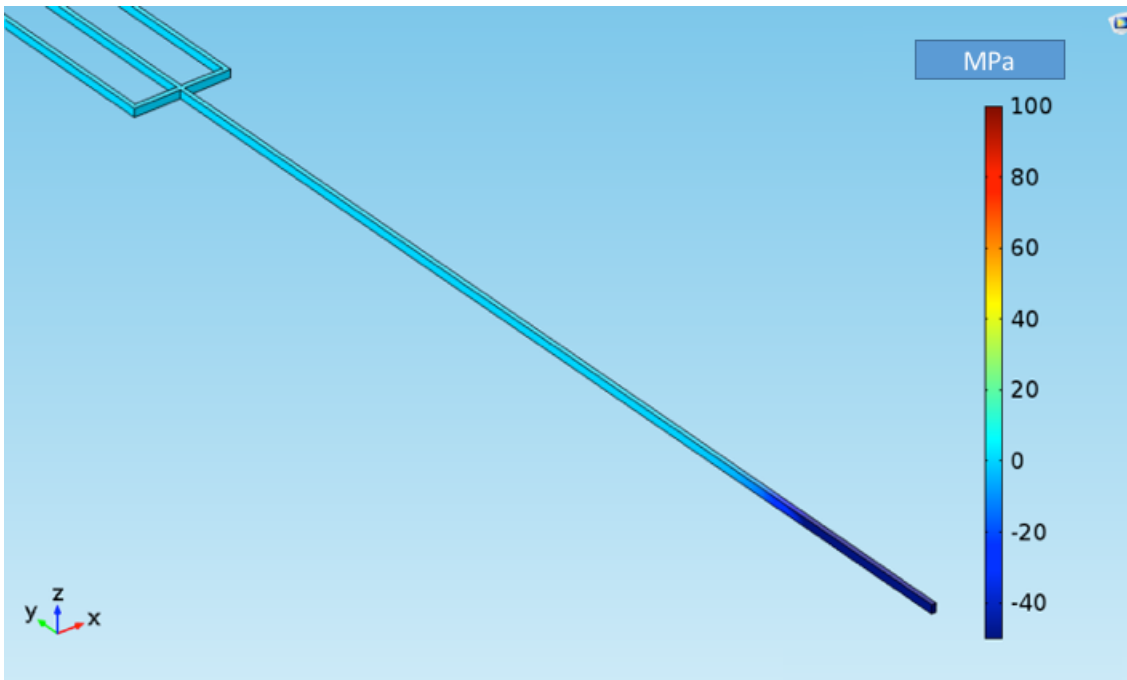


Figure 4-9: Trident structure interconnect hydrostatic stress distribution

Similarly to the bottle structure also the trident structure has been reproduced for simulation, as shown in Figure 4-9. The simulation was carried out for the same

conditions. The hydrostatic stress distribution in the interconnect is similar to the bottle structure, only slight smaller. In fact, in Figure 4-10 the hydrostatic stress along the test line on is shown, the cathode, as expected, show off the maximum hydrostatic. For the same time the stress reached is around 40 MPa. The introduction of the split of the three lines reduces the overall interconnect resistance, and as for the bottle structure fewer vacancies concentrate under the cathode via, producing a smaller stress.

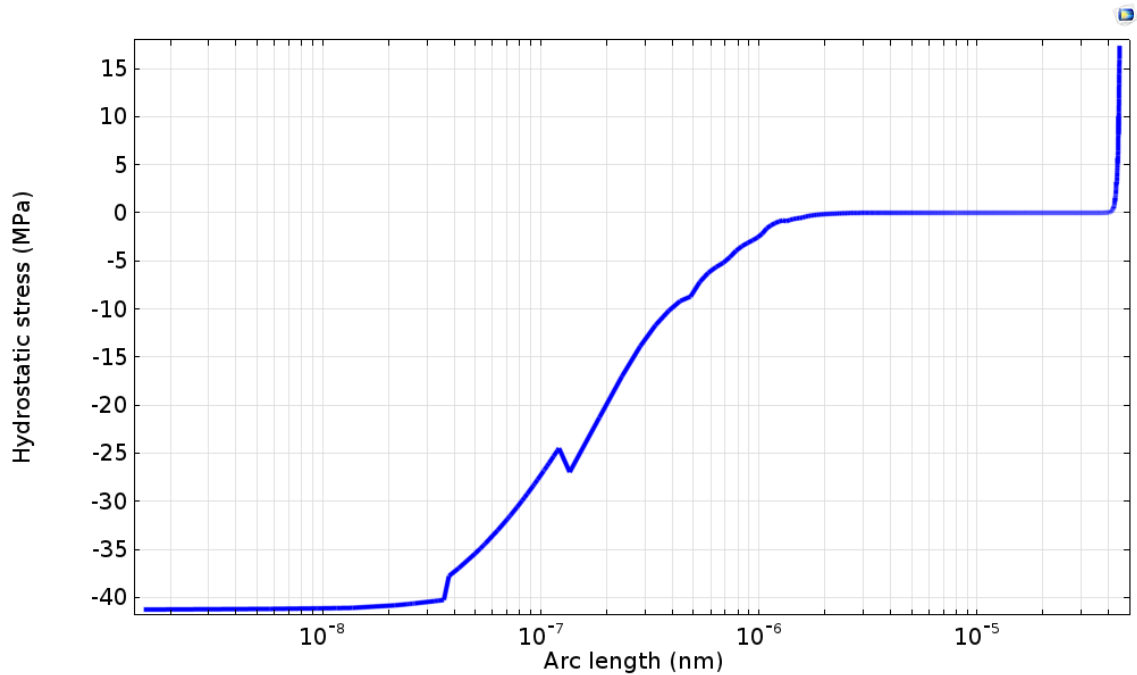


Figure 4-10: hydrostatic stress along the x direction at the TN found experimentally of 106h for the trident structure.

In Chapter 2 has been shown that the two structures have the same time to failure, but the R_{slope} (proportional to the drift velocity of the vacancies) much higher for the trident structure. For remembering, the time failure is the sum of the time of nucleation (TN) and the time growth (Tg), and the Tg is proportional to $1/R_{slope}$. Therefore, the TN has to be large enough to compensate the “full” time of failure. These simulations confirm the hypothesis announced in Chapter 3 about a larger TN for the trident structure, showing that the stress behavior, although similar, is weakened for this configuration.

4.9.5 Initial concentration impact

The influence of the initial concentration, which could be related to the density of the grains and/or eventual future materials and/or process of massive production is addressed. In Figure 4-11 it is shown a parametric study of the initial concentration. Three initial concentrations have been used for these simulations: C_{v0} , $2C_{v0}$, $3C_{v0}$ with $C_{v0} = 1e16/cm^3$. The aim of the study is to show the developing on the vacancy concentration C_v and hydrostatic stress evolution in function of the initial concentration. The evolution of the C_v has similar behavior until 2000 seconds. After this time the typical third phase starting is visible for all three initial parameters with the blue curve for C_{v0} , green for $2C_{v0}$ and red for $3C_{v0}$. In the third phase, for remembering the phase at high mechanical stress, the source term G of the transport equation i.e. is highly dominated by the initial concentration, as shown in **Equation 4-36**. In fact, fixed the final concentration increment $(C_v/C_{v0}-1)$ to 1.6, that corresponds to the time nucleation i.e. 106 hours; the same concentration for $2C_{v0}$ and $3C_{v0}$ is obtained in less time, respectively 55 and 33.3 hours. This means that the initial C_{v0} highly impact on the C_v evolution. And so, all the efforts done to reduce it can improve substantially the EM robustness of the test line. In Figure 4-12: is shown the evolution of the hydrostatic stress on the cathode. Likewise the C_v , also the hydrostatic stress is strictly correlated to the initial concentration and the same results fixing the critical stress of nucleation at 97 MPa, as expected, are obtained.

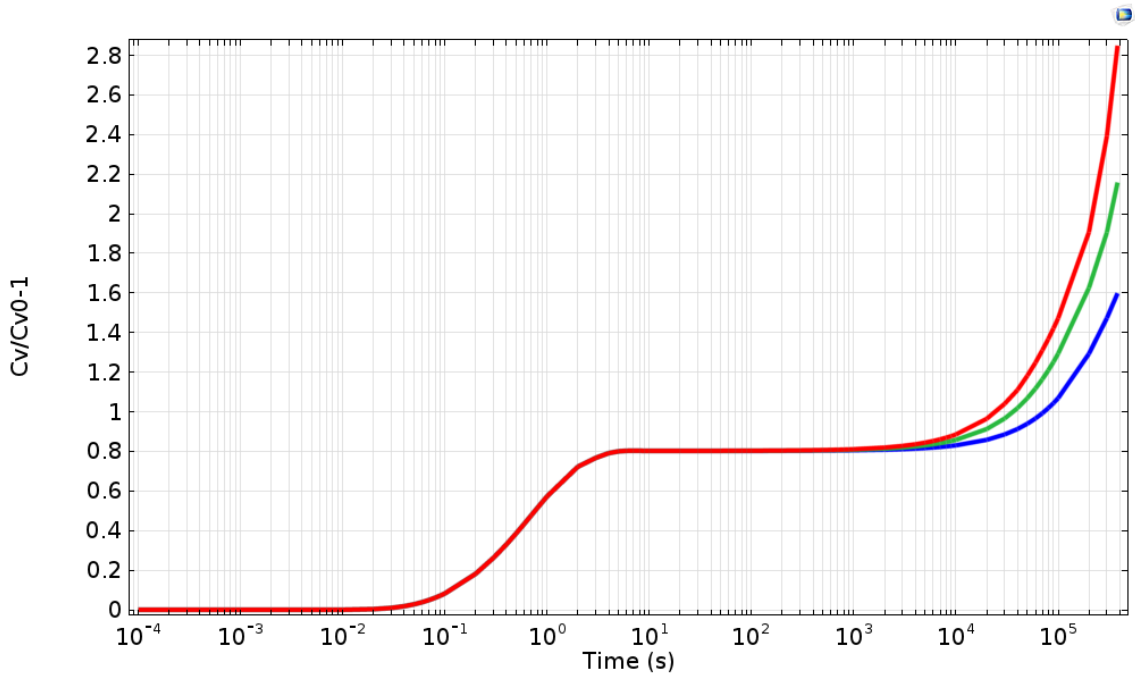


Figure 4-11: Evolution of the increment of vacancy concentration ($C_v/C_{v0} - 1$) at $x=0$ for C_{v0} (blue curve), $2C_{v0}$ (green curve) and $3C_{v0}$ (red curve). Where C_v is the vacancy concentration and C_{v0} the initial vacancy concentration.

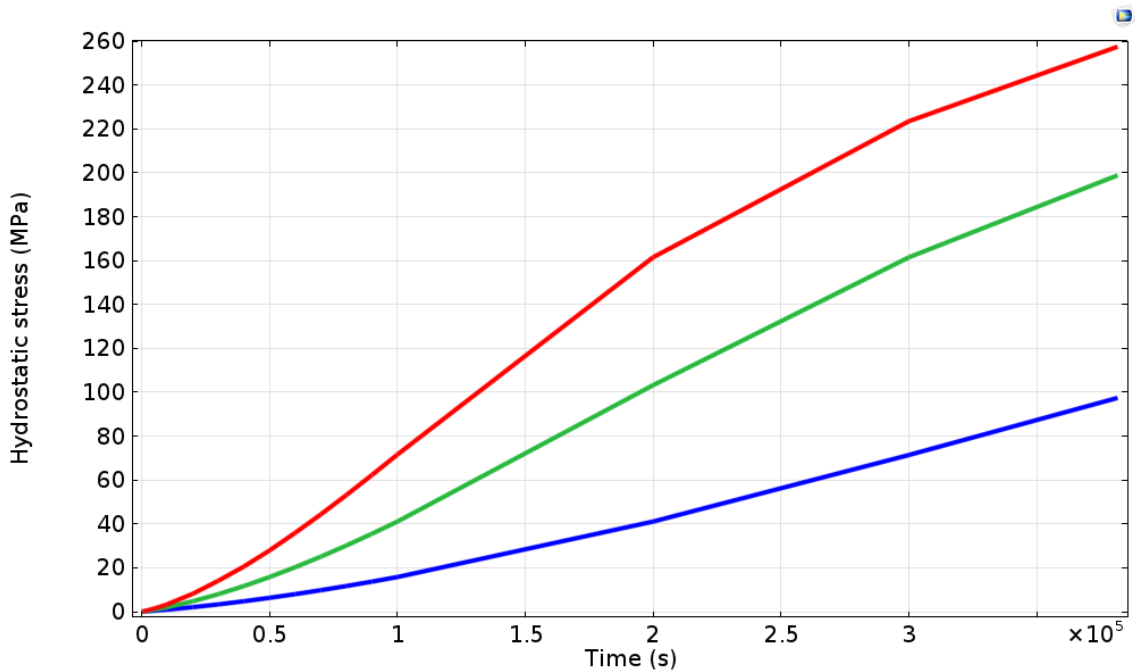


Figure 4-12: Evolution of the hydrostatic stress at $x=0$ (at the cathode) for C_{v0} (blue curve), $2C_{v0}$ (green curve) and $3C_{v0}$ (red curve) with C_v as the vacancy concentration and C_{v0} the initial vacancy concentration.

4.10 Conclusions

In this Chapter, a universal electromigration model for implementation in a COMSOL tool for simulation of realistic three-dimensional interconnects structures is developed. It has been shown that the electromigration simulation necessitates a multiphysics approach. The equations of the model can be conveniently divided in smaller block or sub-problems:

1. The electro-thermal problem is directed by partial differential equations and the solution allow to obtain the electric potential, φ , and for the temperature, T , in the test line
2. Then, the material transport equations are presented the solution of this equation allow to obtain the variable of concern for the vacancy dynamics is the vacancy concentration, C_v .
3. The mechanical problem is expressed in terms of the displacement field, \vec{u} , nevertheless, the hydrostatic stress found from the solution of the mechanical problem is the variable of interest here.

Each sub-problem is solved for the corresponding variable, while the variables of the other sub-problems are fixed in order presented, and iterated for the time of simulation. When the electric potential and temperature distribution reach a steady state only the transport equations and mechanical problem are iterated.

The variation in vacancy concentration is the cause of the induced strain considering that the test line is in a confined environment and that the volume occupied by an atom of copper is bigger than the volume occupied by a vacancy. So the electromigration strain rate and the mechanical stress are generated by the movement or the generation/annihilation of vacancies in the line. Electromigration simulation studies according to the model discussed were presented:

- The maximum vacancy concentration is situated beneath the via and so also the site maximum hydrostatic stress. This condition is necessary for the “void nucleation” and as expected is close to the cathode because already observed experimentally.
- A new method to extrapolate the critical stress of void formation is proposed. The time of simulation has been fixed to the time of “void nucleation” and the Z^* found experimentally has been used. This allowed to obtain the critical stress of nucleation, parameter hard to obtain conventionally.

Chapter 4: Simulations studies of electromigration

- The focused design test structures were been reproduced and simulated for the same condition. The simulation carried out shown a clear difference regarding the maximum stress reached already predicted experimentally. In fact, the trident structure for the same time of simulation reaches a stress smaller than the bottle structure i.e. it will reaches the critical stress of nucleation later, so it has a bigger TN.
- The initial concentration impact has been addressed conducting a parametric study of the initial concentration. The aim of the study is to show the developing on the vacancy concentration C_v and hydrostatic stress evolution in function of the initial concentration. The results is that increasing the initial concentration accelerate the mechanical stress developed and so, all the efforts done to reduce it can improve substantially the EM robustness of the test line.

5 CONCLUSIONS

The EM induced failure has been one of the main reliability issues for the microelectronic industry since its discovery as a potential damage mechanism in metallization of integrated circuits. Since then, new fabrication process and materials, which have suitable properties, have been introduced. Furthermore, the design of specific geometrical features allowed the production of more EM resistant interconnections.

The continuous downscaling of devices demands an ongoing reduction of the metal line dimensions, due to a density increase of interconnections in modern integrated circuits. Consequently, the interconnect lines have to operate at higher temperatures and carry higher current densities, emphasizing the EM-induced transport. As a result, electromigration remains to be a challenge for the development of robust back-end of line. In fact, the lifetime of interconnects has decreased from generation to generation, even though a lot of knowledge was gained and efforts were made within the last 50 years.

The study of the physical phenomena behind EM damage has become more and more important, since it can provide a deeper knowledge basis to anticipate the EM effect. In this context, experimental characterization coupled with mathematical modeling becomes a convenient way to understand the EM-induced failure. In the past years, several new test structures and continuum as well as semi-empirical models have been proposed. They have been able to explain partially numerous features of EM-induced damage and predict the lifetimes of different technologies.

The aim of this work was to merge the two different domains: one hand side the

experimental characterization of interconnect structures and on other hand side the development of mathematical models, suitable for the implementation in COMSOL, a tool for numerical simulations, as these two domains are often too disconnected. In the second chapter, a detailed study of the previously available models is shown, recognizing their main weaknesses and, at the same time, their main strengths. Founded on this analysis, these models were extended and further developed by taking into account the most pronounced effects for EM. In the third chapter, the different test structures and methodologies used to characterize EM have been shown. Among which, the local sense structure allowed the experimental detection of void formation, enabling the access to fundamental data (i.e. the experimental time of nucleation) and the focused design structures to reproduce crucial aspects of the interconnections design. As a result, in the 4th chapter, a multi-physical 3D model is proposed, which links the EM material transport problem with the electro-thermal and mechanical problem in any arbitrary interconnect structure. The model, calibrated with the CMOS technology of 28nm node, has shown benefits to predict the behaviors in certain crucial aspects of the design and for futures technologies, as shown in the perspectives of chapter 4. Therefore, the activation energies of diffusion, calculated from accelerated tests, are probably incorrect, posing a significant problem for the extrapolation of lifetimes to regular operating conditions. An essential feature of the proposed model is the calibration with experimental data. Instead of considering the effective charge (Z^*) found in the literature for copper, this relevant parameter has been extracted experimentally in Chapter 3 and employed in the model in Chapter 4 allowing the calculation of a further crucial parameter for design and modeling which is the critical stress of nucleation.

To sum up, a complex and robust COMSOL EM model was developed, which takes into account a wide diversity of physical phenomena and calibrated with standard experimental characterization, doable in the semiconductor industry. Many numerical simulations of realistic 3D interconnect structures were performed and several valuable predictions have been done and will be done. Nevertheless, there are still many points, which should be enhanced, and its are recommendations for future works. In upcoming studies, the residual stress emerging from the fabrication process, which has a significant impact on the device reliability, should be taken into account. Therefore, this stress must also be evaluated and included in the simulations. As this stress is not only dependent on the metal line itself, but also on the surrounding structures and materials,

the variability of the material properties has to be considered as well. The influence of the process variability on the device performance is usually modeled using statistical approaches. Therefore, the microstructure of the metallization (e.g. bamboo structure) and the surrounding interfaces can impact the EM behavior significantly and should be also taken into account. Furthermore, the effective charge Z^* is currently treated as a material-dependent, but geometry independent constant. Due to an increased number of scattering sources, such as at a rough metal interface for decreased metallization lines, Z^* will likely need to be adjusted according to the metal thickness or grain sizes, i.e. has to be evaluated for each technology. Therefore, it is necessary to design complementary test structures with different geometries to evaluate if and how Z^* has a geometry dependence. And also from a technical point of view, a 3D EM simulation of the entire structure using the finite element approach is only manageable with a relatively coarse mesh, reducing the accuracy of the results.

A logical extension of this work is to couple this modeling approach with a void evolution model suitable for the implementation in COMSOL for 3D structures; the achievement of this task is an ongoing work with Dr. W. H. Zisser from TU Wien. This is a really challenging task, because the void evolution problem necessitates the consideration of additional physical phenomena and particular numerical techniques for tracking the void surface as it evolves, e.g. the phase field method. The main idea is to be able to predict precisely the time of nucleation and the time to failure with a unique general model, which can be calibrated with experimental data.

Chapter 0:

REFERENCES

- [1] H. B. Huntington and A. R. Grone, “Current-induced marker motion in gold wires,” *J. Phys. Chem. Solids*, vol. 20, no. 1, pp. 76–87, Jun. 1961.
- [2] J. R. Lloyd, “Electromigration failure,” *J. Appl. Phys.*, vol. 69, no. 11, pp. 7601–7604, Jun. 1991.
- [3] C.-K. Hu and J. M. E. Harper, “Copper interconnections and reliability,” *Mater. Chem. Phys.*, vol. 52, no. 1, pp. 5–16, Jan. 1998.
- [4] K. Wetzig and C. M. Schneider, “Metal based thin films for electronics,” *CERN Document Server*, 2006. [Online]. Available: <http://cds.cern.ch/record/1609927>. [Accessed: 07-Oct-2016].
- [5] S. Wolf, *Silicon processing for the VLSI era*, vol. volume 4-deep-submicron process technology. Sunset Beach, 2012.
- [6] S. Holzer, “Optimization for Enhanced Thermal Technology CAD Purposes,” TU Wien, 2007.
- [7] A. W. Strong and E. Y. Wu, *Reliability wearout mechanisms in advanced CMOS technologies*, vol. Vol. 12. John Wiley & Sons, 2009.
- [8] Y. Naka, *Introduction to VLSI process engineering*. Springer Science & Business Media, 1993.
- [9] D. N. Bhate, A. Kumar, and A. F. Bower, “Diffuse interface model for electromigration and stress voiding,” *J. Appl. Phys.*, vol. 87, no. 4, pp. 1712–1721, Feb. 2000.
- [10] M. Datta, T. Osaka, and J. . Schultze, *Microelectronic packaging*. CRC press, 2004.
- [11] A. S. Nowick and J. J. Burton, *Diffusion in solids: Recent developments*. Academic Press. New York: Academic Press, 1975.
- [12] K. N. Tu, “Recent advances on electromigration in very-large-scale-integration of interconnects,” *J. Appl. Phys.*, vol. 94, no. 9, pp. 5451–5473, Nov. 2003.
- [13] I. A. Blech, “Electromigration in thin aluminum films on titanium nitride,” *J. Appl. Phys.*, vol. 47, no. 4, pp. 1203–1208, Apr. 1976.
- [14] J. E. Barwin, A. A. Joshi, B. Li, and M. R. Ouellette, “Integrated circuit design method and system,” US8656325 B2, 18-Feb-2014.
- [15] J. R. Black, “Electromigration #8212;A brief survey and some recent results,” *IEEE Trans. Electron Devices*, vol. 16, no. 4, pp. 338–347, Apr. 1969.
- [16] V. Sukharev, A. Kteyan, and E. Zschech, “Physics-Based Models for EM and SM Simulation in Three-Dimensional IC Structures,” *IEEE Trans. Device Mater. Reliab.*, vol. 12, no. 2, pp. 272–284, Jun. 2012.
- [17] J. R. Lloyd, “Black’s law revisited—Nucleation and growth in electromigration failure,” *Microelectron. Reliab.*, vol. 47, no. 9–11, pp. 1468–1472, Sep. 2007.

- [18] R. Kirchheim and U. Kaeber, "Atomistic and computer modeling of metallization failure of integrated circuits by electromigration," *J. Appl. Phys.*, vol. 70, no. 1, pp. 172–181, Jul. 1991.
- [19] J. R. Lloyd, "Reliability modelling for electromigration failure," *Qual. Reliab. Eng. Int.*, vol. 10, no. 4, pp. 303–308, Jan. 1994.
- [20] J. J. Clement, "Reliability analysis for encapsulated interconnect lines under dc and pulsed dc current using a continuum electromigration transport model," *J. Appl. Phys.*, vol. 82, no. 12, pp. 5991–6000, Dec. 1997.
- [21] M. Shatzkes and J. R. Lloyd, "A model for conductor failure considering diffusion concurrently with electromigration resulting in a current exponent of 2," *J. Appl. Phys.*, vol. 59, no. 11, pp. 3890–3893, Jun. 1986.
- [22] C. Basaran, M. Lin, and H. Ye, "A thermodynamic model for electrical current induced damage," *Int. J. Solids Struct.*, vol. 40, no. 26, pp. 7315–7327, Dec. 2003.
- [23] D. G. Pierce and P. G. Brusius, "Electromigration: A review," *Microelectron. Reliab.*, vol. 37, no. 7, pp. 1053–1072, Jul. 1997.
- [24] M. Shatzkes and Y. Huang, "Characteristic length and time in electromigration," *J. Appl. Phys.*, vol. 74, no. 11, pp. 6609–6614, Dec. 1993.
- [25] S. Thrasher *et al.*, "Blech effect in single-inlaid Cu interconnects," in *Interconnect Technology Conference, 2001. Proceedings of the IEEE 2001 International*, 2001, pp. 177–179.
- [26] L. Cao, P. S. Ho, and P. Justison, "Electromigration reliability of Mn-doped Cu interconnects for the 28 nm technology," in *Reliability Physics Symposium (IRPS), 2013 IEEE International*, 2013, p. EM.5.1-EM.5.4.
- [27] S. Beyne, K. Croes, I. De Wolf, and Z. Tókei, "1/f noise measurements for faster evaluation of electromigration in advanced microelectronics interconnections," *J. Appl. Phys.*, vol. 119, no. 18, p. 184302, May 2016.
- [28] L. Doyen, E. Petitprez, P. Waltz, X. Federspiel, L. Arnaud, and Y. Wouters, "Extensive analysis of resistance evolution due to electromigration induced degradation," *J. Appl. Phys.*, vol. 104, no. 12, p. 123521, Dec. 2008.
- [29] L. Doyen, "Caractérisation électrique de l'endommagement par électromigration des interconnexions en cuivre pour les technologies avancées de la microélectronique," Thesis, Université Joseph Fourier, 2009.
- [30] M. Hauschildt *et al.*, "Statistical analysis of electromigration lifetimes and void evolution," *J. Appl. Phys.*, vol. 101, no. 4, p. 43523, 2007.
- [31] J. R. Lloyd and J. Kitchin, "The electromigration failure distribution: The fine-line case," *J. Appl. Phys.*, vol. 69, no. 4, p. 2117, 1991.
- [32] F. L. Bana, "Dégradation par électromigration dans les interconnexions en cuivre : étude des facteurs d'amélioration des durées de vie et analyse des défaillances précoces," École Doctorale IMEP2, 2013.
- [33] B. Li, C. Christiansen, J. Gill, R. Filippi, T. Sullivan, and E. Yashchin, "Minimum Void Size and 3-Parameter Lognormal Distribution for EM Failures in Cu Interconnects," in *2006 IEEE International Reliability Physics Symposium Proceedings*, 2006, pp. 115–122.
- [34] S. c Lee and A. S. Oates, "Identification and Analysis of Dominant Electromigration Failure Modes in Copper/Low-K Dual Damascene Interconnects," in *2006 IEEE International Reliability Physics Symposium Proceedings*, 2006, pp. 107–114.
- [35] F. Cacho, V. Fiori, L. Doyen, C. Chappaz, C. Tavernier, and H. Jaouen, "Electromigration induced failure mechanism: Multiphysics model and correlation with experiments," in *International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Micro-*

- Systems, 2008. EuroSimE 2008, 2008, pp. 1–6.*
- [36] W. H. Zisser, H. Ceric, J. Weinbub, and S. Selberherr, “Electromigration induced resistance increase in open TSVs,” in *2014 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, 2014, pp. 249–252.
- [37] R. S. Sorbello, “Microscopic Driving Forces For Electromigration,” in *Symposium K – Advanced Metallization for Future ULSI*, 1996, vol. 427.
- [38] J. R. Lloyd, “Electromigration in thin film conductors,” *Semicond. Sci. Technol.*, vol. 12, no. 10, p. 1177, 1997.
- [39] K. N. Tu, “Electromigration in stressed thin films,” *Phys. Rev. B*, vol. 45, no. 3, pp. 1409–1413, Jan. 1992.
- [40] R. S. Sorbello, A. Lodder, and S. J. Hoving, “Finite-cluster description of electromigration,” *Phys. Rev. B*, vol. 25, no. 10, pp. 6178–6187, May 1982.
- [41] R. S. Sorbello, “Theory of the direct force in electromigration,” *Phys. Rev. B*, vol. 31, no. 2, pp. 798–804, Jan. 1985.
- [42] P. R. Rimbey and R. S. Sorbello, “Strong-coupling theory for the driving force in electromigration,” *Phys. Rev. B*, vol. 21, no. 6, pp. 2150–2161, Mar. 1980.
- [43] A. Lodder and J. P. Dekker, “The Electromigration Force in Metallic Bulk,” *ArXivcond-Mat9803172*, pp. 315–328, 1998.
- [44] G. Marti, W. H. Zisser, L. Arnaud, and Y. Wouters, “Electromigration: Multiphysics model and experimental calibration,” in *2016 IEEE International Reliability Physics Symposium (IRPS)*, 2016, p. IT-3-1-IT-3-4.
- [45] E. T. Ogawa, K.-D. Lee, V. A. Blaschke, and P. S. Ho, “Electromigration reliability issues in dual-damascene Cu interconnections,” *IEEE Trans. Reliab.*, vol. 51, no. 4, pp. 403–419, Dec. 2002.
- [46] J. J. Clement, “Electromigration modeling for integrated circuit interconnect reliability analysis,” *IEEE Trans. Device Mater. Reliab.*, vol. 1, no. 1, pp. 33–42, 2001.
- [47] C.-K. Hu, L. Gignac, and R. Rosenberg, “Electromigration of Cu/low dielectric constant interconnects,” *Microelectron. Reliab.*, vol. 46, no. 2–4, pp. 213–231, Feb. 2006.
- [48] E. Liniger, L. Gignac, C.-K. Hu, and S. Kaldor, “In situ study of void growth kinetics in electroplated Cu lines,” *J. Appl. Phys.*, vol. 92, no. 4, pp. 1803–1810, Aug. 2002.
- [49] C. K. Hu, L. Gignac, B. Baker, E. Liniger, R. Yu, and P. Flaitz, “Impact of Cu microstructure on electromigration reliability,” in *International Interconnect Technology Conference, IEEE 2007*, 2007, pp. 93–95.
- [50] L. Arnaud, T. Berger, and G. Reibold, “Evidence of grain-boundary versus interface diffusion in electromigration experiments in copper damascene interconnects,” *J. Appl. Phys.*, vol. 93, no. 1, pp. 192–204, Jan. 2003.
- [51] R. Rosenberg and M. Ohring, “Void Formation and Growth During Electromigration in Thin Films,” *J. Appl. Phys.*, vol. 42, no. 13, pp. 5671–5679, Dec. 1971.
- [52] R. L. de Orio, “Electromigration Modeling and Simulation,” Technischen Universität Wien, 2010.
- [53] J. R. Lloyd and J. J. Clement, “Electromigration in copper conductors,” *Thin Solid Films*, vol. 262, no. 1–2, pp. 135–141, Jun. 1995.
- [54] I. A. Blech and C. Herring, “Stress generation by electromigration,” *Appl. Phys. Lett.*, vol. 29, no. 3, pp. 131–133, Aug. 1976.
- [55] I. A. Blech and K. L. Tai, “Measurement of stress gradients generated by electromigration,” *Appl. Phys. Lett.*, vol. 30, no. 8, pp. 387–389, Apr. 1977.

- [56] D. Ney, X. Federspiel, V. Girault, O. Thomas, and P. Gergaud, “Stress-induced electromigration backflow effect in copper interconnects,” *IEEE Trans. Device Mater. Reliab.*, vol. 6, no. 2, pp. 175–180, Jun. 2006.
- [57] J. R. Lloyd, “Electromigration and mechanical stress,” *Microelectron. Eng.*, vol. 49, no. 1–2, pp. 51–64, Nov. 1999.
- [58] R. Kirchheim, “Stress and electromigration in Al-lines of integrated circuits,” *Acta Metall. Mater.*, vol. 40, no. 2, pp. 309–323, Feb. 1992.
- [59] M. A. Korhonen, P. Botgesen, K. N. Tu, and C.-Y. Li, “Stress evolution due to electromigration in confined metal lines,” *J. Appl. Phys.*, vol. 73, no. 8, p. 3790, 1993.
- [60] J. J. Clement and C. V. Thompson, “Modeling electromigration-induced stress evolution in confined metal lines,” *J. Appl. Phys.*, vol. 78, no. 2, pp. 900–904, Jul. 1995.
- [61] R. O. Simmons and R. W. Balluffi, “Measurement of Equilibrium Concentrations of Vacancies in Copper,” *Phys. Rev.*, vol. 129, no. 4, pp. 1533–1544, Feb. 1963.
- [62] P. A. Flinn, “Mechanical Stress in VLSI Interconnections: Origins, Effects, Measurement, and Modeling,” *MRS Bull.*, vol. 20, no. 11, pp. 70–73, Nov. 1995.
- [63] R. J. Gleixner, B. M. Clemens, and W. D. Nix, “Void Nucleation in Passivated Interconnect Lines: Effects of Site Geometries, Interfaces, and Interface Flaws,” *J. Mater. Res.*, vol. 12, no. 8, pp. 2081–2090, Aug. 1997.
- [64] V. Sukharev, R. Choudhury, and C. W. Park, “Physically-based simulation of the early and long-term failures in the copper dual damascene interconnect,” in *Integrated Reliability Workshop Final Report, 2003 IEEE International*, 2003, pp. 80–85.
- [65] D. Dalleau, K. Weide-Zaage, and Y. Danto, “Simulation of time depending void formation in copper, aluminum and tungsten plugged via structures,” *Microelectron. Reliab.*, vol. 43, no. 9–11, pp. 1821–1826, Sep. 2003.
- [66] D. Hull and D. E. Rimmer, “The growth of grain-boundary voids under stress,” *Philos. Mag.*, vol. 4, no. 42, pp. 673–687, Jun. 1959.
- [67] J. P. Hirth and W. D. Nix, “Analysis of cavity nucleation in solids subjected to external and internal stresses,” *Acta Metall.*, vol. 33, no. 3, pp. 359–368, Mar. 1985.
- [68] H. Ceric, R. L. de Orio, J. Cervenka, and S. Selberherr, “A Comprehensive TCAD Approach for Assessing Electromigration Reliability of Modern Interconnects,” *IEEE Trans. Device Mater. Reliab.*, vol. 9, no. 1, pp. 9–19, Mar. 2009.
- [69] Z.-S. Choi, R. Mönig, and C. V. Thompson, “Dependence of the electromigration flux on the crystallographic orientations of different grains in polycrystalline copper interconnects,” *Appl. Phys. Lett.*, vol. 90, no. 24, p. 241913, 2007.
- [70] B. M. Clemens, W. D. Nix, and R. J. Gleixner, “Void Nucleation on a Contaminated Patch,” *J. Mater. Res.*, vol. 12, no. 8, pp. 2038–2042, Aug. 1997.
- [71] A. S. Oates and M. H. Lin, “Electromigration Failure Distributions of Cu/Low-Dual-Damascene Vias: Impact of the Critical Current Density and a New Reliability Extrapolation Methodology,” *IEEE Trans. Device Mater. Reliab.*, vol. 9, no. 2, pp. 244–254, Jun. 2009.
- [72] A. V. Vairagar, S. G. Mhaisalkar, and A. Krishnamoorthy, “Electromigration behavior of dual-damascene Cu interconnects—Structure, width, and length dependences,” *Microelectron. Reliab.*, vol. 44, no. 5, pp. 747–754, May 2004.
- [73] L. Arnaud, F. Cacho, L. Doyen, F. Terrier, D. Galpin, and C. Monget, “Analysis of electromigration induced early failures in Cu interconnects for 45 nm node,” *Microelectron. Eng.*, vol. 87, no. 3, pp. 355–360, Mar. 2010.
- [74] A. V. Vairagar *et al.*, “In situ observation of electromigration-induced void

- migration in dual-damascene Cu interconnect structures,” *Appl. Phys. Lett.*, vol. 85, no. 13, p. 2502, 2004.
- [75] D. N. Bhate, A. F. Bower, and A. Kumar, “A phase field model for failure in interconnect lines due to coupled diffusion mechanisms,” *J. Mech. Phys. Solids*, vol. 50, no. 10, pp. 2057–2083, Oct. 2002.
- [76] A. F. Bower and S. Shankar, “A finite element model of electromigration induced void nucleation, growth and evolution in interconnects,” *Model. Simul. Mater. Sci. Eng.*, vol. 15, no. 8, p. 923, 2007.
- [77] W. H. Zisser, “Electromigration in Interconnect Structures,” TU Wien, Wien, 2016.
- [78] K. Croes *et al.*, “Study of void formation kinetics in Cu interconnects using local sense structures,” in *Reliability Physics Symposium (IRPS), 2011 IEEE International*, 2011, p. 3E.5.1-3E.5.7.
- [79] G. Marti, L. Arnaud, and Y. Wouters, “Study of void formation in Cu interconnects using local sense and standard singlevia structure,” in *Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC), 2014 IEEE International*, 2014, pp. 121–124.
- [80] L. Arnaud, P. Lamontagne, F. Bana, Y. Le Friec, and P. Waltz, “Study of electromigration void nucleation time in Cu interconnects with doping elements,” *Microelectron. Eng.*, vol. 107, pp. 145–150, Jul. 2013.
- [81] M. H. Lin and A. S. Oates, “Electromigration in Dual-Damascene CuMn Alloy IC Interconnects,” *IEEE Trans. Device Mater. Reliab.*, vol. 13, no. 1, pp. 330–332, Mar. 2013.
- [82] G. Marti, L. Arnaud, and Y. Wouters, “Study of EM void nucleation and mechanic relaxation effects,” *Microelectron. Reliab.*, vol. 54, no. 9–10, pp. 1692–1696, Sep. 2014.
- [83] F. Bana, D. Ney, L. Arnaud, and Y. Wouters, “Microstructure local effect for electromigration reliability improvement and Cu damascene lines design rules relaxation,” in *Reliability Physics Symposium (IRPS), 2013 IEEE International*, 2013, p. 2C.2.1-2C.2.6.
- [84] F. Chen *et al.*, “Diagnostic electromigration reliability evaluation with a local sensing structure,” in *2015 IEEE International Reliability Physics Symposium*, 2015, p. 2D.4.1-2D.4.7.
- [85] M. Hauschildt *et al.*, “Electromigration early failure void nucleation and growth phenomena in Cu and Cu(Mn) interconnects,” in *Reliability Physics Symposium (IRPS), 2013 IEEE International*, 2013, p. 2C.1.1-2C.1.6.
- [86] S. Yokogawa and H. Tsuchiya, “Scaling Impacts on Electromigration in Narrow Single-Damascene Cu Interconnects,” in *AIP Conference Proceedings*, 2004, vol. 741, pp. 124–134.
- [87] B. Ouattara, L. Doyen, D. Ney, H. Mehrez, and P. Bazargan-sabet, “Power grid redundant path contribution in system on chip (SoC) robustness against electromigration,” *Microelectron. Reliab.*, vol. 54, no. 9–10, pp. 1702–1706, Sep. 2014.
- [88] R. G. Filippi, P.-C. Wang, A. T. Kim, B. Redder, and C.-K. Hu, “Interconnects exhibiting enhanced electromigration short-length effects by line width variation,” in *Reliability Physics Symposium, 2014 IEEE International*, 2014, p. 5A.3.1-5A.3.7.
- [89] P. Lamontagne, D. Ney, and Y. Wouters, “Effect of reservoir on electromigration of short interconnects,” in *2010 IEEE International Integrated Reliability Workshop Final Report*, 2010, pp. 46–50.
- [90] P. Lamontagne, “Caractérisation électrique et modélisation de la cinétique

- d'endommagement par électromigration pour la fiabilité des interconnexions des technologies avancées de la microélectronique,” Université Grenoble, 2011.
- [91] M. E. Sarychev, Y. V. Zhitnikov, L. Borucki, C.-L. Liu, and T. M. Makhviladze, “General model for mechanical stress evolution during electromigration,” *J. Appl. Phys.*, vol. 86, no. 6, p. 3068, 1999.
- [92] X. Zhu *et al.*, “Multi-physics computer simulation of the electromigration phenomenon,” in *2011 12th International Conference on Electronic Packaging Technology and High Density Packaging*, 2011, pp. 1–5.
- [93] C.-U. Kim, *Electromigration in Thin Films and Electronic Devices: Materials and Reliability*. Elsevier, 2011.
- [94] K. Garikipati, L. Bassman, and M. Deal, “A lattice-based micromechanical continuum formulation for stress-driven mass transport in polycrystalline solids,” *J. Mech. Phys. Solids*, vol. 49, no. 6, pp. 1209–1237, Jun. 2001.
- [95] H. Ceric, R. Heinzl, C. Hollauer, T. Grasser, and S. Selberherr, “Microstructure and Stress Aspects of Electromigration Modeling,” in *AIP Conference Proceedings*, 2006, vol. 817, pp. 262–268.
- [96] O. C. Zienkiewicz and R. L. Taylor, *The Finite Element Method for Solid and Structural Mechanics*. Butterworth-Heinemann, 2005.
- [97] V. Sukharev, A. Kteyan, and X. Huang, “Postvoiding Stress Evolution in Confined Metal Lines,” *IEEE Trans. Device Mater. Reliab.*, vol. 16, no. 1, pp. 50–60, Mar. 2016.
- [98] P. Gibson, M. Hogan, and V. Sukharev, “Electromigration analysis of full-chip integrated circuits with hydrostatic stress,” in *2014 IEEE International Reliability Physics Symposium*, 2014, p. IT.2.1-IT.2.7.
- [99] C. M. Tan, “Electromigration simulation at circuit levels,” in *2014 IEEE International Reliability Physics Symposium*, 2014, p. 5A.1.1-5A.1.9.
- [100] K. Weide-Zaage, Kludt, M. Ackermann, V. Hein, and M. Erstling, “Life time characterization for a highly robust metallization,” in *2015 16th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems*, 2015, pp. 1–6.
- [101] J. Kludt, K. Weide-Zaage, M. Ackermann, C. Kovács, and V. Hein, “Reliability performance of different layouts of wide metal tracks,” in *2014 IEEE International Reliability Physics Symposium*, 2014, p. IT.4.1-IT.4.4.
- [102] X. Huang, A. Kteyan, S. X. D. Tan, and V. Sukharev, “Physics-Based Electromigration Models and Full-Chip Assessment for Power Grid Networks,” *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 35, no. 11, pp. 1848–1861, Nov. 2016.
- [103] R. Galand *et al.*, “Microstructural void environment characterization by electron imaging in 45 nm technology node to link electromigration and copper microstructure,” *Microelectron. Eng.*, vol. 106, pp. 168–171, Jun. 2013.

ANNEX

In the present annex, all the parameters used for carrying out the simulations are presented. If there is no reference, it means that the parameters have been found experimentally or well known in the literature.

Table a-1: Parameters of the electro-thermal equations.

Parameters		Cu	Ta	SiCN	SiOC	Ref.
Electrical conductivity		1.5e7	3.3e5	/	/	
Linear temperature coefficient	(K ⁻¹)	0.0043	/	/	/	[52]
Quadratic temperature coefficient	(K ⁻²)	0	0	0	0	[52]
Thermal conductivity	(W/mK)	379	53.65	0.8	0.35	[52]
Density	(kg/m ³)	8920	16690	3100	2100	
Specific heat	(J/kgK)	385	140	170	1000	

Table a-2: Parameters of the mechanical equations.

Parameters		Cu	Ta/TaN	SiOCOH	SiCN	Ref
Elastic Module	E (GPa)	130	186	9.2	265	[52]
Poisson coefficient		0.34	0.35	0.16	0.27	[52]
Thermal expansion coefficient	(K ⁻¹)	16.5e-6	6.5e-6	0.68e-6	1.50e-6	[52]

Table a-3: Parameters of vacancy dynamics equations

Parameters		Copper	Ref.
Pre-factor diffusion	Dvo (cm ² /s)	0.52	[52]
Energy activation	Ea (eV)	1.14	
Effective charge	Z*	-3.1 0.2	
Vacancy constant heat	Q* (J)	1.2e-20	[52]
Vacancy volume relaxation	f	0.9	[35]
Atomic copper volume	(cm ³)	1.18e-23	
Initial concentration	Cvo (cm ⁻³)	1.0e-16	
Recombination constant	(s)	1	[52]