Contribution to the development of UWB chipless RFID reader based on IR-UWB approach

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Contribution au développement d'un lecteur RFID sans puce basé sur l'approche ultra large bande impulsionnelle

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Contribution au développement d'un lecteur RFID sans puce basé sur l'approche ultra large bande impulsionnelle.

Mots-clés: *Radio Frequency Identification (*RFID), Chipless, Ulta-Wideband (UWB), Reader, Radar

Résumé: La technologie d'identification radiofréquence (RFID) est aujourd'hui une technologie mature qui est amenée à remplacer le code à barre dans un futur proche. Au milieu de toutes les familles de RFID, la technologie RFID sans puce Ultra Large Bande (ULB) est devenue un sujet incontournable. Au cours de cette thèse, nous avons contribué au développement d'un lecteur de tag RFID sans puce ULB en nous basant sur une approche impulsionnelle.
Deux prototypes de lecteur ont été développés en suivant les limitations d'émissions de la technologie ULB imposées par les normes. Le premier lecteur a permis principalement de valider le principe de la lecture de tags RFID sans puce en utilisant le temps équivalent. Une deuxième version du lecteur plus aboutis a ensuite été développée. En effet, la précision de lecture a été optimisée grâce à la réduction du bruit d'échantillonnage. Le temps de lecture ainsi que le coût du lecteur ont aussi été des paramètres clés qui ont été drastiquement réduits. Pour cela, un générateur d'impulsion faible bruit bas coût ainsi que des antennes ULB et des cartes de front-end RF ont été conçus et optimisés. Enfin, une technique de lecture des tags basée sur la diversité en polarisation est proposée et validée en pratique. L'objectif étant de permettre la lecture de tag dépolarisant indépendamment de leur orientation. Ce point est un aspect très important pour le développement futur de la technologie RFID sans puce car cela lève des contraintes sur la conception des tags.

Contribution to the development of UWB chipless RFID reader based on IR-UWB approach.

Keywords: *Radio Frequency Identification (*RFID), Chipless, Ulta-Wideband (UWB), Reader, Radar

Abstract : The RFID technology is in full development, and is intended to compete with optical barcodes for traceability in the next future. Between all the RFID families, the UWB chipless RFID technology is a major topic nowadays. This work of thesis is focused on the development of UWB chipless RFID readers based on IR-UWB approach.
The international regulations that limit the UWB emission are taken into consideration, and two reader prototypes have been developed. The first was used as proof of concept. The second version represents a full optimized reader in all the key aspects. Between them there are the reading precision, through sampling noise reduction, the reading time, and cost effectiveness. As part of the development of the readers, a low noise and low cost UWB pulse generator prototype was realized, along with UWB antennas and RF front-end boards. As prospective, a reading technique based on polarization diversity is shown with the aim of reading cross-polarized chipless tags independently from their orientation. This approach is valuable because does not give any constraint at the tag design level.

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Introduction

The advent of smartphone and its diffusion have revolutionized the life of billions of people in the last decade. The smartphone combines the advantages of a Personal Computer (PC) with those of a mobile phone. A mobile phone gives you the opportunity to be connected with computers and users, exploiting the public telephone network, using a low power portable device. The PC allows for high computational capability as a result of its dedicated hardware combined with software suites. Today these devices are evolving toward a major connectivity to meet the incessant growing request of exchange of information. The increase of mobility in the era of globalization, and the continuous technologic development are changing our life at hectic pace. The home automation, the autonomy transportation, the robotic, and technology in general need a strong interchange of information where people and machines are all connected together, in a global net that is generally addressed as Internet of Things (IoT).

The IoT uses different technologies involved in Personal Area Network (PAN) wireless communications. Between them: Bluetooth, WIFI, Radio Frequency Identification (RFID), infrared, Ultra-Wideband (UWB), bar-code reading capability, and more. This thesis is focused on the RFID, which is a technique where a reader is able to catch information from a passive transceiver using the Radio Frequency (RF) spectrum. The great potentiality of this technology lies on the possibility to have a totally passive tag (transponder).

The massive use of RFID started in the nineties, and up to date, there are diverse kinds of RFID tags that are working at different RF bandwidths. All are in accordance with industrial standards, national and international regulations. The RFID tags incorporate intelligence, they are able to execute hand-shaking protocols, elaborate information, and can be interconnected with sensors. Consequently, RFID tags can be used as part of Wireless Sensor Networks (WSNs). The major use of RFID technology is in the identification of goods

with tracking and tracing ability, in smart logistic, access control, and recently have being incorporated in credit cards.

In the other hand, the most worldwide spread identification technology is still the barcode, where the labels are printed directly on objects or on paper substrate, and are read with optic technique. The barcode was conceived in 1948 from two students of the University of Drexel, Norman Joseph Woodland and Bernard Silver, and its diffusion started only in 1974 by reason of recent optical technology improvements. The barcode labels may be mono or bi-dimensional with many different symbologies. The chipless RFID is born to play an intermediate role between barcode and classical RFID. It is based on the interrogation of a label (tag) with UWB signals, and the subsequent decoding of the tag Identification (ID) based on its Radar Cross Section (RCS) signature. The tags are totally passive and do not present any electronic device attached on its surface, therefore they do not have intelligence or non-linear modulation ability. Thereby, the tags are expected to be printed on paper substrate with metallic ink.

Chipless RFID technology can be placed in-between barcode and classical RFID, where it takes in minor part the advantages of both to be used in industry. Because directly printable on paper, the chipless RFID tags may have a realization cost comparable with barcode labels, and with the use of RF they can be read in a no ling-of-sight condiction. At present there is not a real use of chipless RFID technology in industry apart from Surface Acustic Wave (SAW) devices. However the SAW tags are printed on piezoelectric substrate and they are costly compared to paper, hence they may not be seen as a potential real alternative to barcode. Apart from SAW, the chipless RFID is a young technology born at the beginning of the new century where was first published in 2002 by Richard Ribon Fletcher with its PhD dissertation, at Massachusetts Institute of Technology.

There is an increasing of interest on chipless RFID, and many researchers are redirecting their studies toward this technology. Up to date there is a prominent request in the direction of increasing chipless RFID tag coding capacity, which is hardily higher than 40 bits. Not less important ameliorations are demanded from the reader point of view. The chipless RFID technology needs a reader which is cheap, compliant with UWB regulation, small in size, and preferable integrated inside a smartphone such as for the others PAN communications techniques starting from barcode. The aim of this thesis is to improve the UWB chipless

RFID reader technology. **The duration of the thesis was of three years**, and all the aspects involving the design of a reader for chipless RFID are given in this manuscript**.**

The chapter 1 of this manuscript is an introduction of RFID technology more focusing in all the aspects concerning the chipless RFID. The different characteristics of RFID, barcode, and chipless RFID are discussed. The principle of operation of UWB chipless tags are given in detail, along with their reading techniques.

The chapter 2 presents the state of the art concerning UWB chipless RFID reader. All the proposed readers in literature are based on Frequency-Modulated Continuous-Wave (FMCW) and Stepped-Frequency Continuous-Wave (SFCW) approaches. These technologies are compared with Impulse-Radio UWB (IR-UWB) in terms of UWB regulations, and reading time.

The chapter 3 introduces the first designed IR-UWB chipless RFID reader during the thesis. It is based on equivalent time approach to reduce its realization cost, while maintaining high acquisition performance.

A second reader version was developed and is presented in chapter 4. The objective was to obtain a lower reading time and sampling noise. After a theoretical introduction to sampling noise and quantization noise, the reader hardware architecture is deeply exposed. Compared to the version in chapter 3, it also allows for flexibility in terms of equivalent sampling rate, acquisition frame length and position.

The chapter 5 discusses the design of a tunable low jitter UWB pulse generator, and of UWB planar antennas. The pulse generator could be used with the proposed readers as emission stage and radiative elements to decrease the reader realization cost. Simulation results along with characterizations are shown.

The chapter 6 presents a novel reading technique based on polarization diversity. This approach may be used to read cross-polarization based tags (i.e. chipless tags known to be robust in term of detection in real environment) independently from their orientation. After a theoretical introduction, the approach is validated first with test equipment, and after with the updated reader presented in chapter 4.

1

Introduction to Chipless RFID Technology

1. Introduction

In this chapter the Chipless Radio Frequency Identification (RFID) technology is introduced. After a brief discussion of classical RFID systems, the chapter is focusing on the chipless RFID. A comparison of these two technologies with barcode is given. This thesis work is focusing on the reader part of the chipless technology that interests the Ultra-wideband (UWB). Thus, the principle of operation of UWB chipless tags will be given more in detail. The chapter is organized as follows:

- Section 2 does a general introduction to RFID technology, and its main features are compared with barcode.
- Section 3 presents the chipless RFID technology in UWB. The principle of work of time-coded and frequency-coded tags is given.
- Section 4 draws the conclusion of the chapter.

2. Introduction to RFID

2.1 Introduction

The RFID is among the most widespread technologies concerning the identification of objects and animals (humans are in this category). It is practice to date the origin of the RFID technology in 1945, with the well-known Léon Theremin espionage equipment to retrieve the conversation inside the office of the US ambassador in Moscow. The *thing* was totally passive and able to modulate its backscattered signal, once illuminated by an external electromagnetic source, according to the acoustic waves produced inside the ambassador office. Today a RFID system retains the same principle of work except for the absence of the

modulating acoustic waves, which is substituted with the smartness of an Application Specific Integrated Circuit (ASIC) that performs the modulation.

During its long evolution, RFID systems have been evolving towards numerous directions, due to the lack of standardization for many years, and the huge number of distinct application requirements. Up to date the most employed RFID systems may be classified according to their frequency band as: Low Frequency (LF), High Frequency (HF), Ultra High Frequency (UHF), and Super High Frequency (SHF). Apart from LF, the others use the unlicensed Industrial, Scientific and Medical (ISM) bands.

2.2 Passive, semi-passive and active transponder

Essentially a RFID system is composed of a reader, and a bunch of transponders inside the reading volume. The transponder may be passive, semi-passive or active. A passive transponder does not have a battery. Its chip is energized by harvesting from the reader transmission Electromagnetic (EM) wave, i.e. reader interrogating signal. For the most of passive transponder the transmission of information is performed in a passive way. Once energized, the chip is able to vary the load impedance connected to its antenna, generally between two different values. It modulates the amplitude of the impinging reader signal (down-link), which is backscattered toward the reader (up-link) ensuring the communication between the two actors. This is called load modulation and is summarized in figure 1.1.

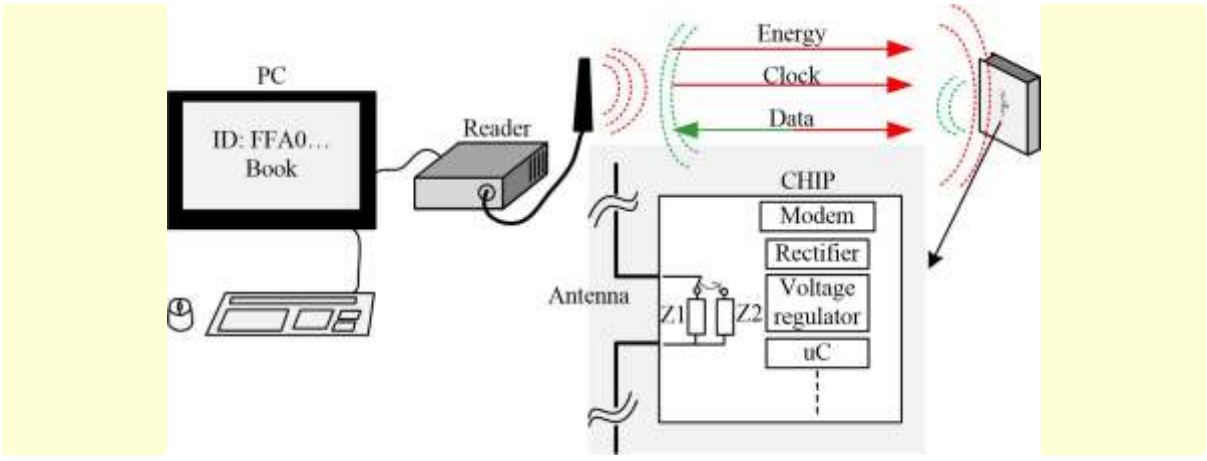


Figure 1.1. *Schematic of a RFID system, the reader interrogates the transponder providing energy to wake up the ASIC (Chip), clock for synchronization purposes, and data as request code (down-link). After, the chip replies modulating the antenna load impedance between two values, providing a backscattering modulation to the reader (up-link).*

Usually the reader adopts either an Amplitude Shift Keying (ASK) or a Frequency Shift Keying (FSK) modulation with a dual objective. First, to optimize the bandwidth available according to international regulations, and second, to retain the transponder chip well energized to accomplish the communication. Conversely the transponder can respond modulating the amplitude and the phase of the reflected carrier wave by changing the chip impedance between two states. It can adopt modulation schemes with subcarrier generation such as Binary Phase Shift Keying (PSK), Amplitude Shift Keygen (ASK), and Frequency Shift Keying (FSK). These schemes have a robust implementation at the expense of a reduced communication throughput. In a direct modulation scheme, each bit is associated with one reflecting carrier wave amplitude variation with a fixed bit period. It ensures the fastest communication at the expense of low noise immunity [MIC 02].

According to figure 1.1, the transponder chip presents an analog part involved directly in the communication, and a mixed part represented by a microcontroller. The analog part is formed of a modulator and demodulator (modem), a voltage rectifier to harvest the energy from the carrier wave, and a voltage regulator to provide the correct voltage to the chip. The digital part is a hard-core microcontroller that may embed memories, Inter-Integrated Circuit (IC2) and Serial Peripheral Interface (SPI), and analog sensor interfaces. The read-range of a passive UHF transponder is lower than 10 m (short range), and limited by the harvester efficiency that is around 20% [LE 008].

A semi-passive or active transponder is equipped with a battery to provide energy at the chip, and eventually at peripherals. The communication retains the load modulation scheme, while the part of the chip in charge of the modulation is energized directly from the battery. The transponder can be waked up, in a cooperative way, from the battery and the harvested reader interrogating signal. Thus, the transponder is read at distances up to 100 m for a UHF semi-passive transponder (moderate range). An active transponder has a Radiofrequency (RF) transmitter block used to communicate with readers, and also with other transponders. Its read-range is of several hundred of meters (long range) [DOB 12].

The RFID is a narrowband technology regulated in Europe by the European Telecommunications Standards Institute (ETSI), and by the Federal Communications Commission (FCC) in the United States of America (USA). The LF RFID applications and standards use mostly the frequencies of 125 kHz and 134 kHz, while the HF the 6.78 MHz

and 13.56 MHz. The UHF interests 433.92 MHz and 869 MHz in Europe (915 MHz in USA), and 2.45 GHz, while the SHF is for 5.8 GHz. Several standards have been proposed from the physical to the software application level, where some are international as ISO/IEC, and others are proprietary. The standardization helps the manufacturer to realize product with high level of interoperability. For instance, the ISO 18000 series is taking care of the air interface protocol (frequency, data modulation, …) for systems, to be used to track goods in the supply chain for RFID, in all the aforementioned frequency bands [VIOL 05]. Some of the currently used standards are shown in figure 1.2 [SAT 12,DOB 05].

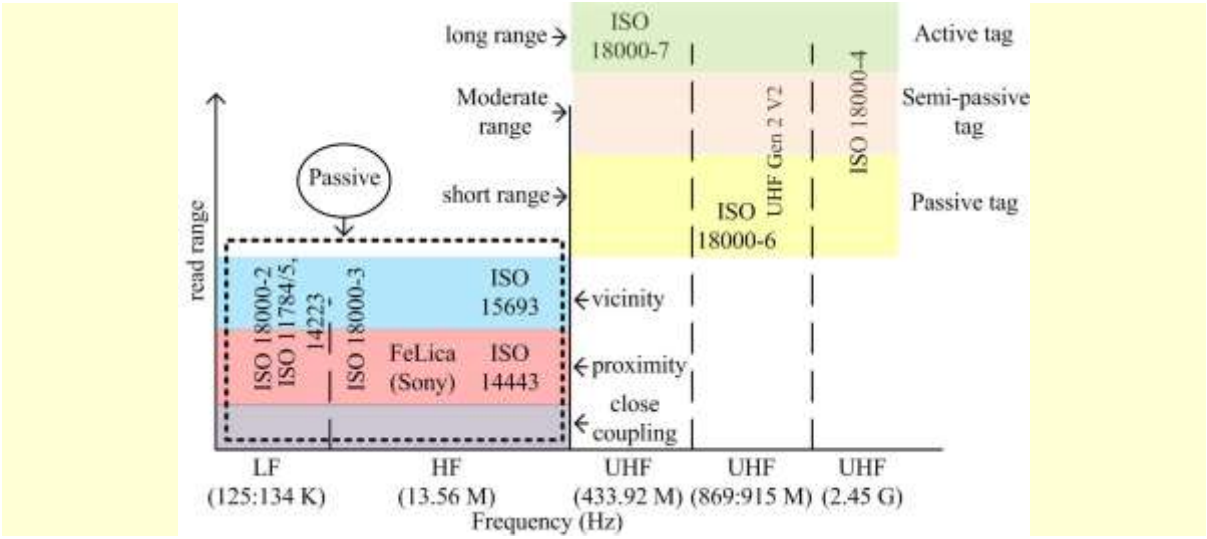


Figure 1.2. *A reduced collection of RFID standard. From international organizations (ISO, GS1), to private enterprises, such as Sony.*

2.3 RFID vs barcode

As a result of its minimal label cost, the barcode technology is more employed than RFID in item identification. Nowadays the realization cost of a barcode label is orders of magnitude lower than a passive RFID transponder. A barcode can be printed on paper substrate with not-conductive ink because based on optic reflection. Due to the use of RF, a conductive ink is needed in RFID to generate surface currents. It is used in HF RFID to print out the antenna in label tag (transponder) for transport ticketing. It is also a subject of study for passive UHF tags for tracking item applications and for wearable electronics [BJO 16- RIZ 16]. The conductive ink is more expensive than the not-conductive ink; hence a RFID tag cannot compete with barcode label in term of cost, where the cost of the chip can be prominent. The cost of a RFID transponder is varying depending on its characteristics. It ranges from few tens of euro-cents for inlay EPC GEN2 tags, to hundreds of euros for sophisticated long life

active transponders. A barcode label may worth less than 0.5 euro-cents, even lesser if the barcode is directly printed on items.

A barcode label substrate may be composed of almost each type of solid material, and the label color has to be as much pale as possible. It is common to print the barcode motive out directly on item surface to save from substrate cost. For a printed UHF RFID transponder, the substrate can affect considerably the reading performance. Thus, it is hardly possible to print the transponder antenna directly on not-characterized tracking items. The relative permittivity of the substrate may vary the antenna operating frequency.

With the exception of cost, the RFID technology offers many advantages compared with barcode. It is smart (chip), has a higher read-range, and data bit capacity. It does not need a direct-line-of-sign to be read thanks to the use of RF, as so the transponder can be hided and made not visible. It may also work in harsh environment and be water-proof.

3. Chipless RFID

3.1 Principle of operation

The chipless RFID technology is born at the beginning of the new century, and is dated with the Richard Ribon Fletcher PhD dissertation published in 2002 [FLE 02]. After in 2005, Michael Pettus patented a chipless RFID system, where the tag was composed of a multitude of RF antennas, each providing different orientation and phase characteristics as so to encode the tag identification (ID). In this system the reader scans an area, and using radar imaging techniques, can retrieve the tag information [PET 05]. Since then, the chipless technology is gaining a continuous growth of interest world-wide, most from university. It is a technique of identification where the tag does not have any electronic component attached on its surface and relays on its EM property for the identification.

A chipless RFID reading system is shown in figure 1.3. The tag is commonly composed of a pattern (like in barcode) made of conductive material, created upon a substrate with etching or printing technique. The principle of work is similar to that of a radar application where non Radar Cross Section (RCS) modulation is expected. Contrarily to RFID, the reader transmits a wide-band signal to the environment, and the tag backscattered signal is measured and analyzed, in time and frequency domain, to retrieve the desired information.

The total absence of a chip denied the opportunity of any signal modulation therefore the chipless RFID technology is not compatible with narrow band identification utilizations such as classic RFID, and needs to be wideband.

A chipless RFID tag can be seen has a passive filter, where the information is coded based on its impulsive response: larger available bandwidth means higher coding capacity. A chipless RFID system needs to comply with (UWB) regulations in the band 3.1-10.6 GHz. The UWB at bigger frequency is reserved for different applications. The chipless technology is developing also in extremely high frequency [POP 16] and terahertz [HAM 12], where a sort of two dimensional imaging (2-D) encoding technique may be employed. Anyway, these latter two frequency bands are not subject of study in this thesis.

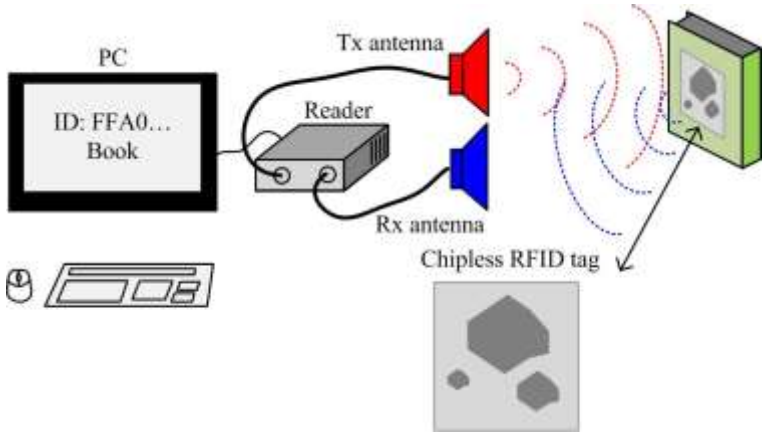


Figure 1.3. *Schematic of a chipless RFID system.The reader interrogates the transponder with a UWB signal, then the backscattered signal from the tag is analyzed to retrieve the tag ID.*

3.2 Chipless RFID in-between RFID and Barcode

The chipless RFID technology may be located between the conventional RFID and the barcode. The absence of electronic devices with their package may represent a significant abatement of tag realization cost. Thus, a chipless RFID tag may be cheaper than a RFID tag, and perhaps comparable with a barcode [VEN 13a]. Up to date the cost comparison is a hard topic. Despite the absence of electronic devices the label pattern may have a total surface area larger than a passive UHF RFID tag on a costly substrate. Thus most of chipless tag prototypes have a realization cost higher than UHF RFID tag [PRE 10]. However, it is possible to find in literature miniaturized single layer chipless RFID tags for UWB compatible with ultra-low cost realization techniques. For instance, in [VEN 13a], chipless tags printed with conductive ink, using flexography, are presented. In [VEN 12], the

authors present a miniaturized chipless RFID tag of 2 cm × 2 cm, with 10 bits. The tag was realized on a rigid FR-4 substrate with etching technique, and was read with expensive laboratory equipment.

In comparison with barcode, a chipless RFID tag adds the opportunity to be read without direct line-of-sign. This is a strong advantage because the tag may be hided and read through objects. It opens to a plenty of applications for chipless RFID where barcode may not be used, such as discretion for luxury package and security. Contrarily to barcode, a chipless RFID tag may offer sensor capabilities [TED 13]. In [FEN 15] the authors present a printed chipless RFID tag on paper substrate designed as humidity sensor, with interdigital capacitor implementation. In [SCH 14] a time domain coded chipless temperature sensor was proposed. It was realized with screen-printing technology on a substrate of Allumina, with a central frequency of 7 GHz, and a -10 dB bandwidth of 2 GHz.

The chipless read-range is often considered higher than barcode, and absolutely lower than passive UHF RFID tags. This may be debatable, in fact for the chipless RFID tag the read range is also correlated with its coding capacity in terms of bits number. Some chipless RFID tags, based on time-domain reflectometry (TDR), may have a read-range over 1 m, but with a scarce number of bits, usually lower than 10. Most of the time, they are realized on high cost and RF performing substrate [RAM 11]. Higher bit capacity chipless RFID tags have a reduced read-range in order of few tens of centimiters.

The read-range depends not only on the tag characteristics but also on the reader performance, and its power emission (UWB regulations). In literature are often claimed read-range, bit capacity, and in general chipless RFID tag with high performance, but using expensive laboratory equipment as reader, in anechoic environment, and slighting taking into consideration the UWB regulations.

Multipath effects are present in chipless RFID, and they may affect the reading capability. Conversely, in barcode, the interrogating optical reader signal can be well focused on the tag, that allows for reducing multipath effects. In addition, a barcode label needs to be read with direct line-of-sign, as so the reading optic signal cannot go behind the label, and eventual reflective perturbing signals are not present. In literature is common to find tables that compare barcode, chipless RFID, and UHF RFID in terms of tag performances and realization cost [PER 14]. Almost all of them give the best place for all the parameters,

except for tag realization cost, to UHF RFID. Then chipless RFID outdo barcode in reading range, with comparable realization cost, and lower bit capacity. From our experience in the field, up to date the battle between barcode and chipless RFID for reading performances did not give a net vanquisher. For tag realization cost, the barcode is today the winner, but the match between passive UHF RFID tag and chipless RFID tag is still open.

3.3. UWB chipless RFID

The chipless RFID technology has to comply with international regulations as all electronic communication systems. A chipless RFID system works with UWB because the tag bit-capacity increases with the frequency bandwidth. The UWB technology is referred to systems which employ large band and low power to exchange or retrieve information. The American FCC regulation concerning UWB is in *Part 15* of Title *47* [FCC 17], and grants the band 3.1 - 10.6 GHz for communication systems in indoor applications such as chipless RFID. The ETSI regulation, in terms of UWB systems, is stricter compared with FCC. It allows for the same band of FCC, but with lower power between the band 6 – 8.5 GHz [ETS 04 - ETS 10]. This work of thesis is concerning the readers for UWB chipless RFID tags that may be classified in time-coded and frequency-coded based tags.

3.3.1 UWB time-coded chipless RFID tag

An UWB time-coded chipless RFID tag, in its most simple representation, is composed of one UWB antenna connected to a transmission line, along which some impedance mismatchings are created. A schematic example of a 4 reflections based tag is shown in figure 1.4 (a). Once interrogated with a UWB reader, the tag reflected signal may be analyzed in time domain, and the delays between the different reflections can be estimated. The values of these delays encode the tag information. The tag response in time is composed of a tag structural mode and an antenna or tag mode. The former is due to the specular reflection of the tag assemblage. The latter is the tag behavior where the antenna is transferring energy to the transmission line, and all the reflections due to impedance mismatchings occur. The antenna (tag) mode is the essential information in chipless technology, and is exploited in copious manner with signal processing. In case of time-coded chipless tag, the structural mode is also useful. It gives information about the tag distance, and also is exploited to calculate the relative delays of the reflections to decode the tag ID. An example of encoding technique is shown in figure 1.4 (b), corresponding to the tag in (a). The time domain is divided in 4 areas, where each is referred to one reflection of the 4 that

compose the tag mode. Based on the position of the reflection inside the area, a different binary code is assigned. In the figure the tag ID is 01001110_2 that correspond to 8 bits of information.

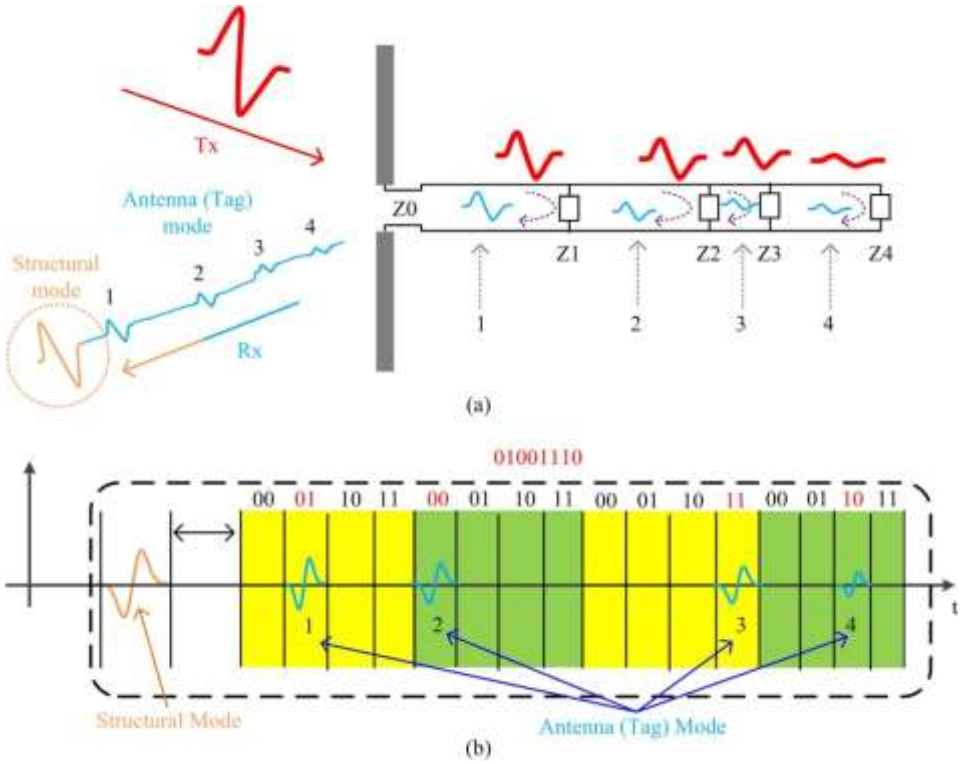


Figure 1.4. *(a) Exemplification of a UWB chipless RFID tag based on a time-coded approach. The tag has 4 impedance mismatchings (Z_i) that originate 4 main reflections toward the reader. (b) The tag information is encoded with the temporal distances between the structural mode, and the various reflections in the antenna (tag) mode.*

The figure 1.4 is overly simplified because the impedances Z_n generate multiple-reflections. For instance, the first reflected signal by Z_2, before reaching the antenna, will be in part reflected back by the impedance Z_1, and so on. These effects will create disturbances in the reader receiving signal, and the low energy reflected signals will be decoded with more difficulty.

The major drawback of a time-coded tag is represented by the transmission line length that may be substantial. Considering a Gaussian monocycle interrogating signal with a pulse full-width of about 500 ps, then the minimum registered distance between reflections in the tag response should be of at least 500 ps. It corresponds to 250 ps transmission line delay

between two impedances (2 ways). If the tag transmission line has a relative permittivity ε_r of around 4.4 (FR-4), then the wave speed inside the line v_L is approximately,

$$v_L = \frac{v_0}{\sqrt{\varepsilon_r}}. \qquad [1.1]$$

Where v_0 is the speed of light in a vacuum environment, which was estimated at about 3×10^8 m/s. In such configuration, v_L is of about 1.43×10^8 m/s, and multiplying it by 250 ps returns to a minimum distance between two reflectors of 3.5 cm. Hence, a UWB time-coded chipless RFID tag may have a significant dimension. It can be reduced using less number of reflective elements (lower bit-capacity), higher permittivity materials, and bending techniques.

In a chipless RFID tag, all the impedances Z_i have to be realized with layout techniques (Chipless). To reduce as much as possible the loss of the transmission line, the impedance elements Z_i should have zero resistivity. This leads to the realization of pure imaginary discontinuities. However they are known to be narrow band in its simpler realization (stub). Consequently in literature is possible to find UWB time-coded chipless RFID tags which are not really *chipless,* because the impedances are realized with discrete components [ZHA 06-SCH 09].

The use of Surface Acoustic Wave (SAW) technology is not recent, and in electronics is employed in a variety of applications, such as filters design, oscillators, and sensors. They are based on acoustic waves instead of electromagnetic waves, which have a speed in free space of about 10^5 times lower than the speed of light. This feature can be exploited to create much smaller RF devices. A SAW component needs two Interdigitated Transducer (IDT), and a piezoelectric substrate that can transduce between electrical and mechanical energy. Time-coded chipless RFID SAW tags are a reality nowadays, and are produced by numerous enterprises. These tags are working in the ISM band at 2.45 GHz (narrow band). The bit capacity may exceed 128 bits with a tag dimension of about 10 mm for side not considering the antenna [HAR 02]. The major drawback of a SAW tag is the realization cost caused by the need of piezoelectric substrates, and also by the use of etching techniques for metallic layer deposition. It may not represent a competitor neither for barcode, nor for UHF RFID passive technology.

In 2008 a patent about the use of cellulose substrate to propagate acoustic wave was deposited [KIM 08]. The tag was characterized by the presence of an antenna, a SAW based IDT, and a plurality of reflectors for reflecting the surface acoustic wave. All was mounted on

cellulose substrate that would help to reduce the tag substrate cost. However other challenges need to be faced, such as the printability of the tag and the immunity against environmental condition.

3.3.1.1 Single line discontinuity UWB time-coded chipless RFID tag

A UWB time-coded chipless RFID tag with only one discontinuity line can be readily designed. It needs to have either a zero impedance (short circuit) or infinitive impedance (open circuit) to reflect as much energy as possible in the direction of the antenna. It is simple to realize a large band open circuit with layout technique, while for a short circuit it may depend from the transmission line technology. In microstrip a short circuit needs a via, while for coplanar it does not. This approach pays in terms of coding capacity, but gains in read-range, and dimensions. The principle schematic of a single reflector UWB time-coded chipless RFID tag, and a reading process with a bi-static reader, is shown In figure 1.5.

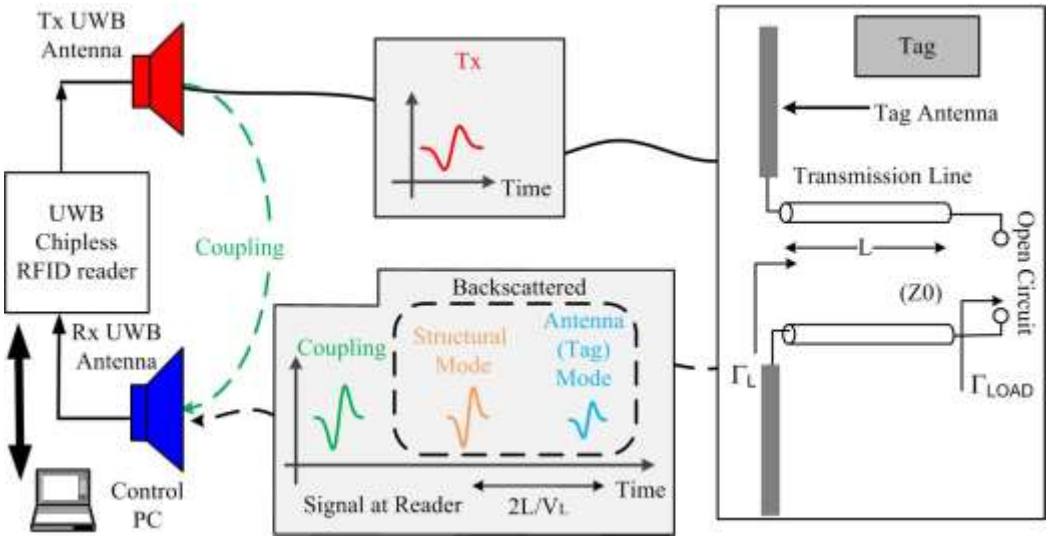


Figure 1.5. *Exemplification of an UWB chipless RFID tag based on a time-coded approach using only one line discontinuity (open circuit load). A bi-static UWB chipless RFID reader is used.*

In case of bi-static configuration the coupling between the two reader antennas is reduced (green dashed line on figure 1.5) compared to mono-static configuration. However it is omnipresence in short-range radar based applications such as chipless. If the coupling of the reader antennas and the tag are not influencing each other, the coupling effect can be removed from one tag identification process in post-processing. Two measurements are

necessary, one without the tag and subsequently another one with the tag (background subtraction [RAM 11]).

A typical bi-static co-polarization measurement results, of a time-coded chipless tag at several distances up to 2 m in practical environment [RAM 12], is shown in Figure 1.6. It uses known detection methods (background subtraction and Continuous Wavelet Transform (CWT)) [LAZ 11]. As it can be observed, both the structural and antenna (tag) modes can be detected. The tag layout along with its measured and simulated reflection coefficient is shown in Figure 1.7. The tag consists of a microstrip-fed UWB monopole [WHY 08] fabricated on Rogers RO4003C substrate.

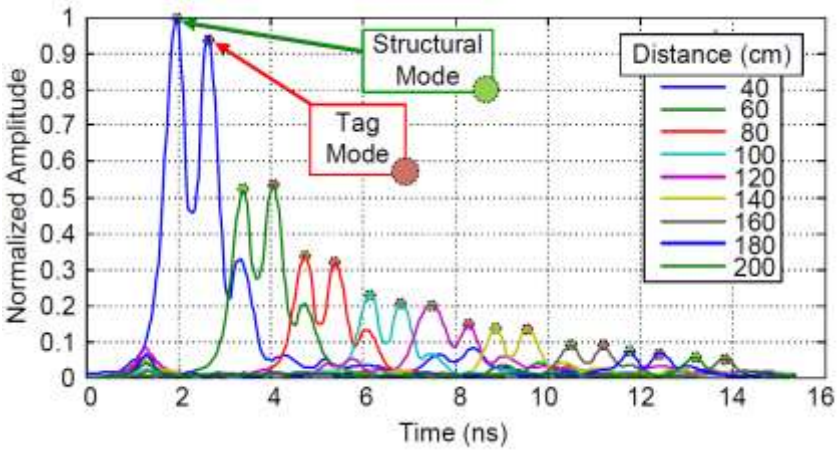


Figure 1.6. *Normalized result measurement after background subtraction (top) and CWT, for the monopole tag at several tag-reader distances in practical environment. Original figure in [RAM 12].*

The obtained read range of 2 m is remarkable, and also the tag reduced dimension of 5.3 cm × 4.3 cm makes it smaller than a credit card size, which is of 8.560 cm × 5.398 cm according to [ISO/IEC 7810 ID-1]. The tag information capability depends also from the reader performances and post processing power. A value lower than 10 bits is reasonable, hence, this kind of UWB chipless RFID tag is more suitable for sensing and localization applications rather than identification [RAM 11, RAM 13].

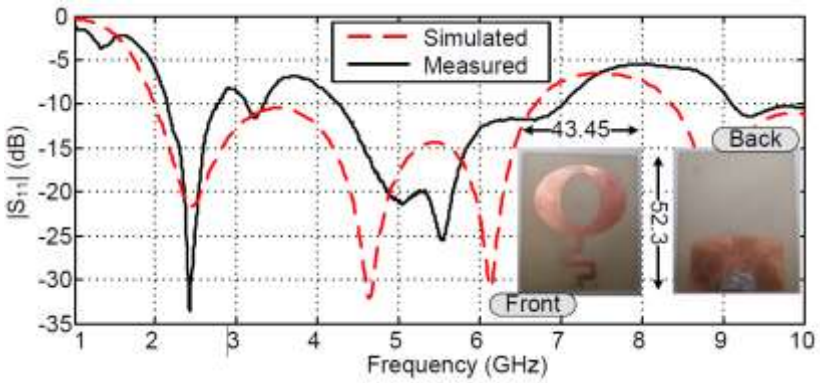


Figure 1.7. *Layout of the microstrip-fed UWB monopole tag with dimensions in millimeters, and its measured and simulated tag reflection coefficient. Original figure in [RAM 12].*

3.3.2 UWB frequency-coded chipless RFID tag

A UWB frequency-coded chipless RFID tag uses an approach based on its spectral response to encode information. The tag geometry is modified to account for specific amplitude and phase characteristics over the frequency band of interest. A well-known structure of such tag is composed of two UWB antennas (one for transmission and the other for reception), and between them a passive filter realized with distributed elements as shown in figure 1.8 (a).

If the passive distributed filter of figure 1.8 is considered lossless, part of its input signal will be reflected, and part transmitted to the other antenna. The antennas are linear polarized with a cross-polarization configuration (in perpendicular direction). If a reading approach similar to figure 1.5 (UWB bi-static) is used to read the tag, the reader antennas have to be lined up with the tag antennas, to read successfully the tag. The cross-polarization configuration allows for measuring only the part of the UWB reader interrogating signal that crosses the tag filter, and therefore the part of the signal where is encoded the tag ID.

In figure 1.8(a) are represented two examples of passive filters compatible with microstrip technology. One based on notch spiral resonators, and the other one on parallel open circuit stubs. The first solution applied to chipless technology was proposed in [PRE 09]. The spiral filters were placed along with the microstrip line, each resonator introduced a diverse band-stop resonance. It was designed in the band 3.1 - 7 GHz, and realized in Taconic TLX-0 with dimensions of 8.8 cm × 6.5 cm. The information is encoded in the amplitude part of the

spectrum reaching 35 bit of information. Varying the dimension of the spirals their first mode resonant frequency will change accordingly, as so the filter characteristics.

In [NIJ 12] the solution represented in figure 1.8 (a) using parallel open circuit stubs was proposed. The tag has a limited 8 bit capacity, and the coding is yet trusted on spectrum amplitude. The antennas are two cross-polarized monopoles, and the tag measures 5.0 cm × 3.0 cm not considering the antennas. The bandwidth of interest is between 2 - 4 GHz and the substrate is high performance from Rogers. In [NAI 16] the authors presented a UWB frequency domain chipless RFID tag where only the filter section was implemented and characterized with laboratory equipment. Instead of focusing on the amplitude of the response, they took care of the phase through the group delay. The filter was composed of cascaded commensurate C-sections which length determines the frequency with higher group delay variation. To retain a small filter dimension, a folding approach is proposed. As yet, the proposed architecture of a UWB frequency-coded chipless RFID tag presents a discrete bit capacity of around 40 bits. On the other side, it expects a reader in bi-static configuration, with two cross-polarized antennas, and the tag needs to be aligned with the reader antennas for maximum performance.

3.3.2.1. Join antennas and filter

The frequency-coded chipless RFID tags proposed in [PRE 09 - NIJ 12] are based on spectrum amplitude modulation, using a set of independent notch filters, in an absence/presence encoding sort (see figure figure 1.8). In [TED 12] an exhaustive overview of UWB chipless encoding technique is given.

Using the RF Encoding Particle (REP) approach introduced in [PER 14, VEN 16], it is possible to obtain the requested spectrum amplitude modulation of the tag, in a smaller structure [VEN 11- VEN 12]. This structure is composed of several resonant scatterers (particles), in which the two antennas and the filter are enclosed. For instance the tag proposed in [NIJ 12], which is composed of parallel open circuit stubs used as Band-Stop Filter (BSF), can be translated in an equivalent tag based on REP approach. It is shown in figure 1.9 where for simplicity only three resonators of [NIJ 12] are shown.

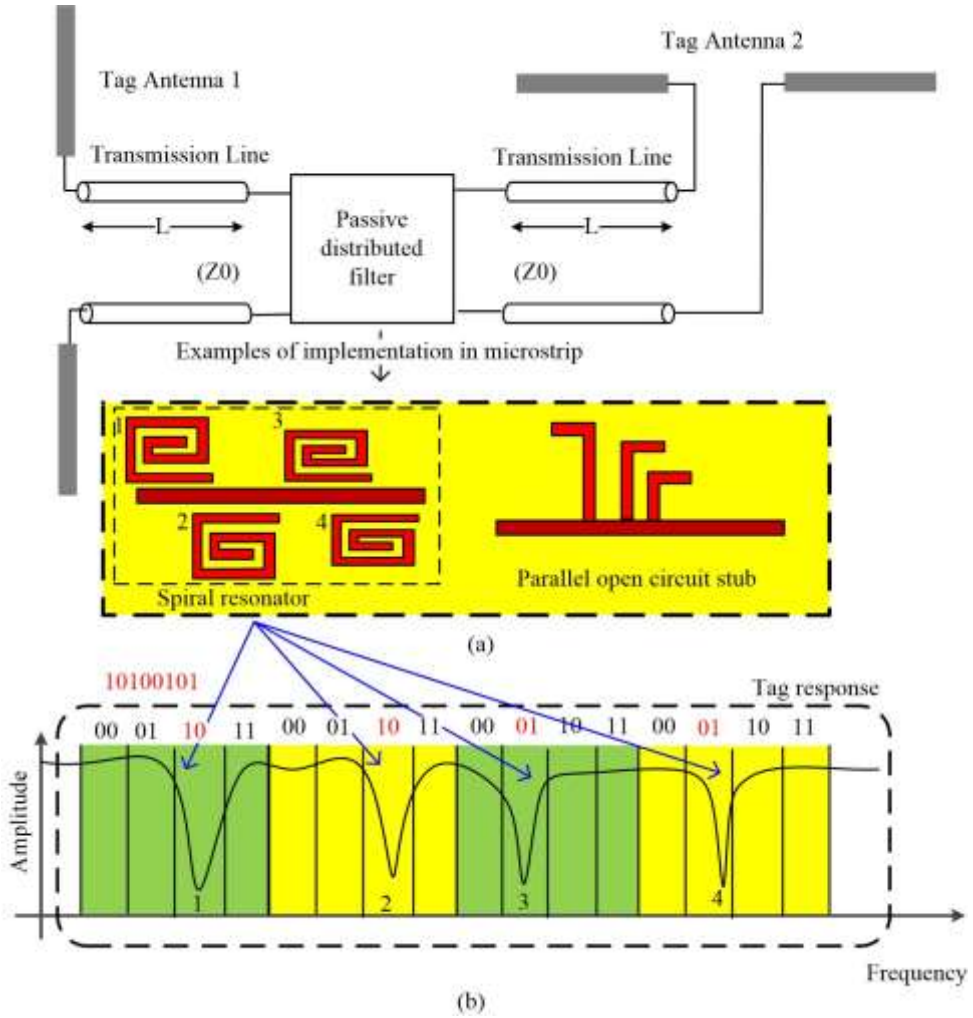


Figure 1.8. *Schematic of a frequency-coded UWB chipless RFID tag based on cross-polarization. Two examples of passive distributed filters are shown, one based on spiral resonator [PRE 09], and the other on parallel open circuit stubs [NIJ 12].*

The REP approach is a complex subject, form a theoretical point of view, one interest is that a REP chipless tag can be seen like a radar target. The specificity here is that the tag (target) is designed to have a known number of resonant frequencies. From the Singularity Expansing Method these frequencies, which are related to the tag mode, are independent from the reading method. Thus, they can be used to encode the information [BAU 91], [REZ 13].

The study of the behavior of a loaded antenna, constructed with linear reciprocal materials, is fundamental to better understand the complexity of REP from both, analytical and physical approach. In [GRE 63] the author presents a study about the prediction of the

backscattering property of a loaded antenna with some minimal measurements. Once exited with an impinging electromagnetic field, two different scattering processes occur, one load independent and the other fully dependent. As previously explained, the first is due to the immediate reflection that occurs on the metallic part of the antenna, through the formation of surface currents (structural mode scattering). Instead the second is concerning the radiative property of the antenna connected at that specific load (antenna mode scattering). This can be seen as the property of the antenna to convey the incoming electromagnetic field towards the load, which is responsible of its dissipation. The tag of figure 1.9 with REP approach is composed of three scatterers. Each scatterer has its structural and antenna (tag) mode scattering, and then can be seen as an antenna connected to a complex load.

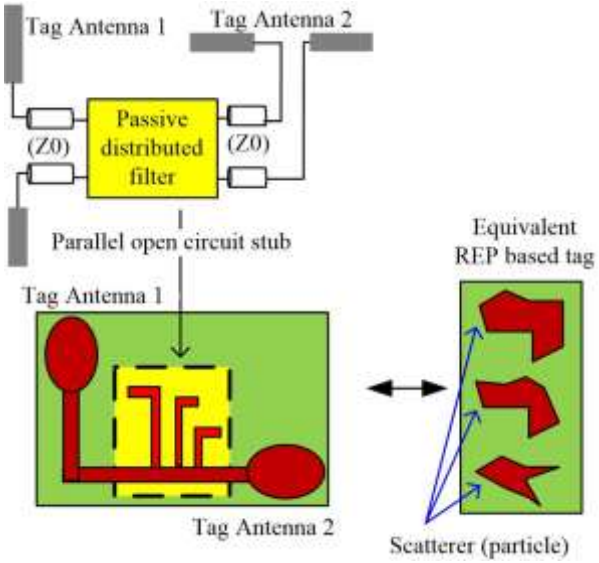


Figure 1.9. *Representation of a UWB frequency coded tag based on microstrip with two UWB disc monopole antennas, and three parallel open circuit stubs similar to [NIJ 12]. The tag can be realized with three resonant scatterers using the REP approach, with similar performance than the original tag.*

One of the first use of the REP approach on chipless RFID was in [JAL 05]. The authors realized a barcode type chipless tag composed of 5 scatterers. Each scatterer was considered as a short circuited dipole antenna and not yet strictly speaking as REP scatterer, the concept was introduced later [PER 4]. Each scatterer was composed of a strip with different length, in microstrip technology. It was designed in the bandwidth 5.4 - 6 GHz on Taconics TLY-5, and shown a 5 bit capacity, and a read range of tens of centimeters. The measurement was performed with a Vector Network Analyzer (VNA) in co-polarization, and shows a band rejection effect of the tag at the strip first resonance frequency ($\lambda/2$). This was

due to the destructive effect between the scatterer structural mode and the antenna (tag) mode.

Since [JAL 05] remarkable progresses have occurred on this approach for chipless, and many works are publishing by worldwide laboratories. The bit capacity of this kind of tag has been increased using more elaborated scattering particles, with magnitude and also phase coding information, and using mainly cross-polarization reading approach with a more elaborate post processing treatment. In [VEN 11] a tag based on C-like resonators (scatterers) is presented, it was realized on one metallic layer in a low cost FR-4 substrate with permittivity of 4.6. Using a coding based on frequency resonant position and phase characteristic of C-like resonators, the coding capacity was increased up to 22.9 bits, with a tag size of 2 cm × 4 cm, where the tag bandwidth was 2-7 GHz. The use of only one layer represents a significant reduction of the tag development cost, with the possibility to realize the tag by using printing techniques.

The reading process in anechoic chamber and in cross-polarization of a depolarizing REP tag introduced in [VEN 13b], is shown in figure 1.10 (a). The tag was realized in Roger R04003 with a ground plane, and was based on eight resonators composed each of five coupled dipoles in short circuit with the first resonant mode in between the band 3-7 GHz. The Agilent N9918A was used as VNA with 0 dBm of emission power. The dual access Satimo QH2000 was employed, and the tag was placed at 15 cm. The detection process used was the background subtraction. The measurement results are shown in figure 1.10 (b), where the eight resonant frequencies correspond to the visible eight peaks. The coding is based on the position of the resonances.

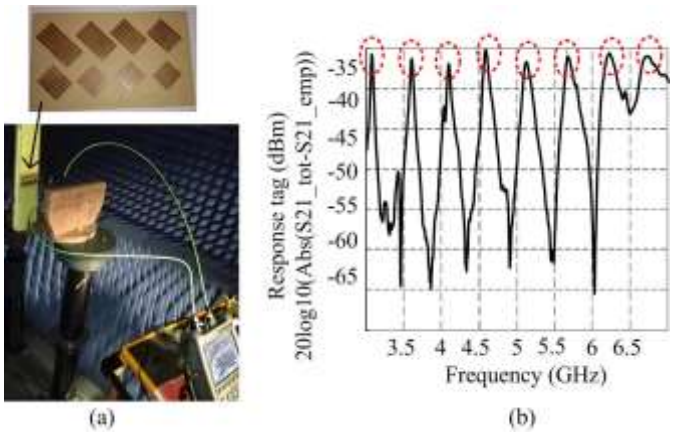


Figure 1.10. *Measurement in cross-polarization of the frequency-coded UWB REP chipless RFID tag proposed in [VEN 13b], inside an anechoic chamber. (a) Photo of the test bench and the measured tag. The Agilent N9918A was used to measure the S-parameter (S21), with an averaging factor of 10. The tag was placed at 15 cm from the dual-access dual polarization Satimo QH2000 antenna. In (b) the tag response where the positions of the eight resonant frequencies are underlined (read circles).*

4. Conclusion

In this chapter the chipless RFID technology that interests the UWB was introduced. The chipless may be placed in-between the more advanced RFID and the barcode. It may represent a cheaper identification solution than RFID preserving the not direct-line-of-sign in reading process, and the possibility to embed sensor capabilities. These two characteristics represent significant advantages compared to barcode. On the other side a UWB chipless tag, in comparison with barcode, has lower bit capacity, lower multipath immunity, and higher realization cost. The latter is most due to the cost of conductive ink in case of printable tags. A UWB chipless tag may be classified in time-coded and frequency-coded, where the letter uses the REP technology to reduce its dimension.

The chipless RFID technology is based on a radar approach, where the backscattering energy from an object through its RCS, is the heart of all the radar applications. Thus, the performance of the reader has an important impact on the reading capability. Parameters such as: the read range, the impact of different tag orientations, and tag bit capacity, are strongly dependent on the reader. In the next chapter, the state of the art of chipless reading technology is reviewed.

5 References

[BAU 91] C. E. BAUM, E. J. ROTHWELL, K. CHEN, et al. “The singularity expansion method and its application to target identification,” Proccedings of the IEEE, vol. 79, no. 10, pp. 1481–1492, 1991.

[BJO 16] BJORNIEN T., SUIKKOLA J., UKKONEN L. *et al.*, "Testing and modeling the performance of stretchable screen printed UHF RFID tag under strain," *2016 IEEE International Symposium on Antennas and Propagation (APSURSI)*, Fajardo, pp. 465-466, 2016.

[DOB 05] DOBKIN D. M., “A Radio-Oriented Introduction to RFID-Protocols, Tags and Application”, *High Frequency Electronics, Aug*. 2005.

[DOB 12] DOBKIN D.M., *The RF in RFID, Second Edition: UHF RFID in Practice*, Newnes Newton, MA, USA, 2012.

[ETS 04] ETSI TR 101 994-1 V1.1.1 ("Electromagnetic compatibility and Radio spectrum Matters (ERM); Short Range Devices (SRD); Technical characteristics for SRD equipment using Ultra Wide Band technology (UWB) Part 1: Communications applications”, *European Telecommunication Institute (ETSI),* Janu. 2004.

[ETS 10] ETSI EN 302 065 V1.2.1 "Electromagnetic compatibility and Radio spectrum Matters (ERM); Short Range Devices (SRD) using Ultra Wide Band technology (UWB) for communications purposes; Harmonized EN covering the essential requirements of article 3.2 of the RTTE Directive”, *European Telecommunication Institute (ETSI),* Oct. 2010.

[FCC 17] Title 47 Telecommunication chapter 1 subchapter A Part 15 subpart F-Ultra-wideband operation, online available at : www.FCC.org.

[FEN 15] FENG Y., XIE L., CHEN Q. et al., ”Low-Cost Printed Chipless RFID Humidity Sensor Tag for Intelligent Packaging,” in *IEEE Sensors Journal*, vol.15, no.6, pp. 3201-3208, June 2015.

[FLE 02] FLETCHER R.R., “Low-Cost Electromagnetic Tagging: Design and Implementation,” Ph.D. dissertation, Massachusetts Institute of Technology, Cambridge, MA, 2002.

[GRE 63] GREEN R.B., “The general theory of antenna scattering”, Ph.D. dissertation, Ohio State University, 1963.

[HAM 12] HAMDI M., GARET F., DUVILLARET L. P. et al., "New approach for chipless and low cost identification tag in the THz frequency domain," *2012 IEEE International Conference on RFID-Technologies and Applications (RFID-TA)*, indipendentiNice, 2012, pp. 24-28.

[HAR 02] HARTMANN C. S., "A global SAW ID tag with large data capacity," 2002 IEEE Ultrasonics Symposium, Proceedings., 2002, pp. 65-69 vol.1.

[JAL 05] JALALY I. "RF barcodes using multiple frequency bands," *IEEE MTT-S International Microwave Symposium Digest (IMS), pp. 139-142, 2005*.

[KIM 08] KIM J., Saw based chipless passive RFID tag using cellulose paper as substrate and method for manufacturing the cellulose paper (2008), Patent WO/2008/056,848.

[LAZ 11] LAZARO A., RAMOS A., GIRBAU D. et al., “Chipless UWB RFID Tag Detection Using Continuous Wavelet Transform,” *IEEE Antennas Wireless Propagation Letters*, Vol. 10, 520-523, 2011.

[LE 008] LE T., MAYARAM K., FIEZ T., "Efficient Far-Field Radio Frequency Energy Harvesting for Passively Powered Sensor Networks," in *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1287-1302, May 2008.

[MIC 02] MICROCHIP, microID 125 kHz RFID System Design Guide, Application Note AN680, 2004.

[NAI 16] NAIR R. S., PERRET E., "Folded Multilayer C-Sections With Large Group Delay Swing for Passive Chipless RFID Applications," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4298-4311, Dec. 2016.

[NIJ 12] NIJAS C. M., DINESH R., DEPPAK D., et al., "Chipless RFID Tag Using Multiple Microstrip Open Stub Resonators," in *IEEE Transactions on Antennas and Propagation*, vol. 60, no. 9, pp. 4429-4432, Sept. 2012.

[PER 14] PERRET E., Radio Frequency Identification and Sensors – from RFID to Chipless RFID, ISTE Press – Elsevier, 1st Edition, 2014.

[PET 05] PETTUS M., RFID system utilizing parametric reflective technology (2005), patent US20050280539 A1.

[POP 16] POPPERL M., ADAMETZ J., VOSSIEK M., "Polarimetric Radar Barcode: A Novel Chipless RFID Concept With High Data Capacity and Ultimate Tag Robustness," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 11, pp. 3686-3694, Nov. 2016.

[PRE 09] PRERADOVIC S., BALBIN I., KARMAKAR N. C., et al., "Multiresonator-Based Chipless RFID System for Low-Cost Item Tracking," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 5, pp. 1411-1419, May 2009.

[PRE 10] PRERADOVIC S., KARMAKAR N. C., "Chipless RFID: Bar Code of the Future," in *IEEE Microwave Magazine*, vol. 11, no. 7, pp. 87-97, Dec. 2010.

[RAM 11] RAMOS A., LAZARO A., GIRBAU D., et al., "Time-domain Measurement of Time-coded UWB Chipless RFID tag", *Progress in Electromagnetics*, vol 116, pp.313-331, 2011.

[RAM 12] RAMOS A., GIRBAU D., LAZARO A., "Influence of materials in time-coded chipless RFID tags characterized using a low-cost UWB reader," *42nd European Microwave Conference*, Amsterdam, 2012, pp. 526-529.

[RAM 13] RAMOS A., LAZARO A., GIRBAU D. et al., "Time-coded chipless RFID temperature sensor with self-calibration based on a Vivaldi antenna," *IEEE MTT-S International Microwave Symposium Digest (IMS)*, 1-4, 2013.

[REZ 13] REZAIESARLAK R., MANTEGHI M., "Short-time matrix pencil method for chipless RFID detection applications," IEEE Transaction on Antennas and Propagation, vol. 61, no. 5, pp. 2801–2806, May 2013.

[RIZ 16] RIZWAN M., KUTTY A.A., KGWADI M., *et al.*, "Comparative study of inkjet and thermal printing for fabrication of passive UHF RFID tags," *2016 10th European Conference on Antennas and Propagation (EuCAP)*, Davos, pp. 1-5, 2016.

[SAT 12] SATTLEGGER K., DENK U., "Navigation your way through the RFID jungle", Texas instrument white paper, Feb. 2012.

[SCH 09] SCHÜßLER M., MANDEL C., MAASCH M., et al., "Phase modulation scheme for chipless RFID- and wireless sensor tags", *Asia Pacific Microwave Conference*, Singapore, 2009, pp. 229-232.

[SCH 14] SCHUSSLER M., KOHLER C., WIENS A., et al., "Screen printed chipless wireless temperature sensor tag based on Barium Strontium Titanate thick film capacitor," in *SENSORS*, pp. 2223-2226, 2-5 Nov. 2014.

[TED 12] TEDJINI S., PERRET E.., VENA A., et al., " Mastering the electromagnetic signature of chipless RFID system," in Chipless and Conventional Radio Frequency Identification: Systems for Ubiquitous Tagging, KARMAKAR N. C., IGI global, 2012, pp. 146-174.

[TED 13] TEDJINI S., KARMAKAR N., PERRET E., et al., "Hold the Chips: Chipless Technology, an Alternative Technique for RFID," in *IEEE Microwave Magazine*, vol. 14, pp. 56-65, July 2013.

[VEN 11] VENA A., PERRET E., TEDJINI S., "Chipless RFID Tag Using Hybrid Coding Technique," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 12, pp. 3356-3364, Dec. 2011.

[VEN 12] VENA A., PERRET E., TEDJINI S., "Design of Compact and Auto-Compensated Single-Layer Chipless RFID Tag," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 9, pp. 2913-2924, Sept. 2012.

[VEN 13a] VENA A., PERRET E., TEDJINI S. et al., "Design of Chipless RFID Tags Printed on Paper by Flexography," in *IEEE Transactions on Antennas and Propagation*, vol. 61, Issue 12, pp. 5868-5877, 2013.

[VEN 13b] VENA A., PERRET E., TEDJINI S., "A Depolarizing Chipless RFID Tag for Robust Detection and Its FCC Compliant UWB Reading System," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 8, pp. 2982-2994, Aug. 2013.

[VIOL 05] VIOLINO B., "A summary of RFID standards", in *RFID journal,* jan. 2005.

[ZHA 06] ZHANG L., RODRIGUEZ S., TENHUNEN H. et al., "An innovative fully printable RFID technology based on high speed time-domain reflections," *Conference on High Density Microsystem Design and Packaging and Component Failure Analysis*, Shanghai, 2006, pp. 166-170.

[WHY 08] WHYTE G., DARBARI F., MCGREGOR I. et al., "Different Feeding Geometries for Planar Elliptical UWB Dipoles, and the Excitation of Leakage Current," *38th European Microwave Conference*, 1382-1385, 2008.

[VEN 16] VENA A., PERRET E., TEDJINI S., *Chapter 4: Design of Chipless RFID Tags*, Chipless RFID based on RF Encoding Particle, ISTE Press – Elsevier, 1st Edition, pp. 98 – 122, 2016.

2

UWB Chipless RFID Reader: State of the Art

1. Introduction

In the chapter 1 the chipless RFID technology that involves the UWB was introduced. Its main peculiarities, compared with classical RFID and barcode, were underlined. The aim of this thesis is the development of a low cost reader for UWB chipless RFID tags, which is compliant with international regulations with a reduced reading time. This chapter introduces the current state of the art for chipless readers involving the UWB between 3.1 – 10.6 GHz.

All the proposed readers in literature are based on frequency domain with either a Stepped-Frequency Continuous Wave (SFCW) or a Frequency-Modulated Continuous-Wave (FMCW) approach. Both provide a transmitting signal sweeping in between the tag bandwidth to retrieve the desired information. A SFCW reader has a higher sweep time compared with a FMCW where the transmitted CW instantaneous frequency is varying with a stair case function as shown in figure 2.1(a). The transmitting and receiving instantaneous frequency, respectively f'(Tx) and f'(Rx), have a small offset and no beat frequency is generated. This approach is also used in commercial Vector Network Analyzer (VNA) and is suitable to read both frequency-based and time-based chipless RFID tag. A FMCW approach is typically used in radar application where a beat frequency is generated due to the offset Δf between f'(Tx) and f'(Rx) as shown in figure 2.1(b). This approach allows for a reduced sweep time compared with SFCW and both RFID chipless tags topology can be read. However the reading of a frequency-coded tag with FMCW is low accurate and requires a complex post processing algorithm that may involve the Hilbert transform.

The chapter is organized as follows:

- Section 2 introduces two SFCW reader architectures characterized by two mixers in reception, and an IQ demodulation scheme.

- Section 3 details the readers based on FMCW architecture and their capability of reading frequency-based tags is demonstrated.

- Section 4 introduces a reading technique based on Impulse-Radio UWB (IR-UWB) as shown in figure 2.1(c). It represents a time domain approach, and up to date no IR-UWB chipless RFID readers are available in literature. A comparison between SFCW, FMCW and IR-UWB architectures, in relation with UWB regulations, is given. Finally a link-budget involving the three different approaches with a typical frequency-coded tag as target is proposed

- Section 5 draws the conclusion of the chapter.

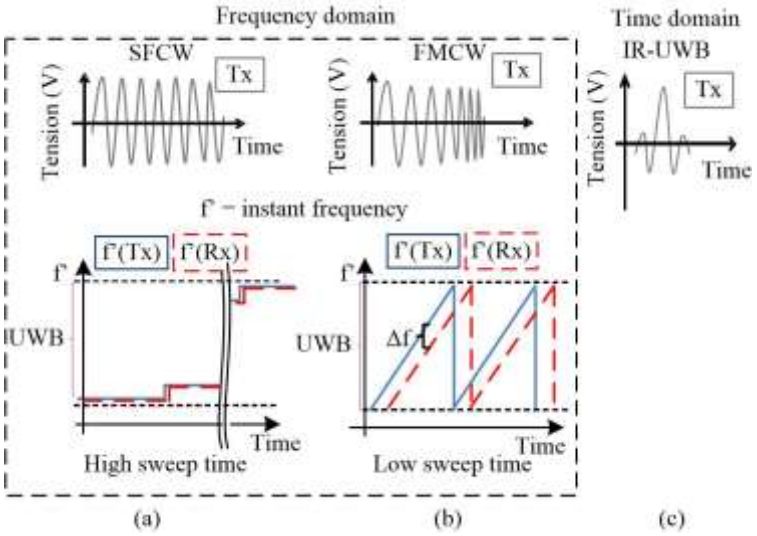


Figure 2.1. *(a) Transmitting and receiving signals of a UWB chipless RFID reader based on SFCW. It shown a high sweep time and is ideal to read frequency-coded chipless tag. (b) Transmitting and receiving signals of a UWB chipless RFID reader based on FMCW. It has a reduced sweep time and is most employed to read time-based chipless tag. (c) Transmitting signal of a UWB chipless RFID reader based on IR-UWB approach.*

2. SFCW approach

A block schematic of a bi-static SFCW reader is shown in figure 2.2. In transmission a Phase Locked Loop (PLL) is used to generate the CW interrogating signal whose instantaneous frequency f'(Tx) is controlled by the digital and control unit. In the receiving front-end is used an I/Q demodulation scheme to recover the amplitude and phase difference between the reader transmitting and receiving signal. The generation of a beat frequency is not needed with this solution, and the sweep time of the PLL can be as long as desired. In

any case the sweep time must not be excessively long to avoid unbearable reading time. With this approach is possible to characterize the impulsive response of the tag in the band of interest, and thus decode both chipless RFID tag topologies.

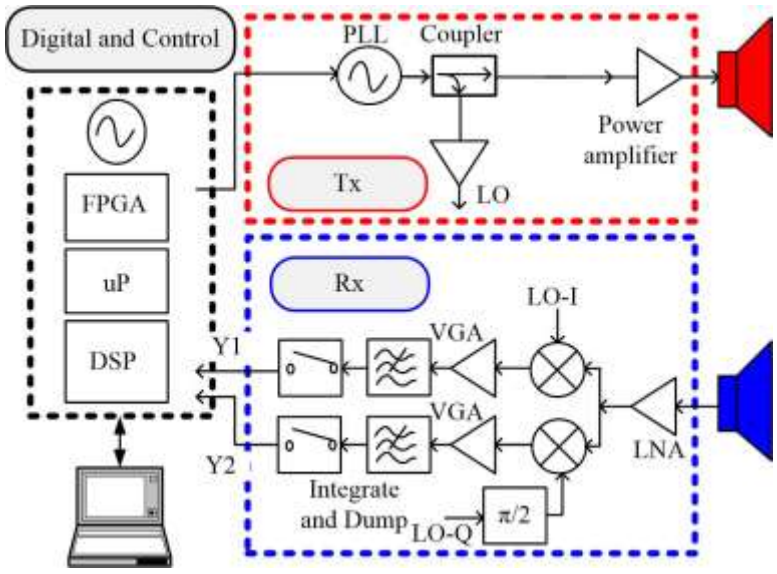


Figure 2.2. *UWB chipless RFID reader based on FMCW approach and I/Q demodulation. Thanks to the use of two mixers, a beat frequency is not required.*

A reader for UWB chipless RFID tags based on SFCW implementation was proposed in [PRE 10]. It was designed to work between 5 and 9 GHz, and a wideband Yttrium Iron Garnet sphere (YIG) Voltage Controlled Oscillator (VCO) was used in transmission. The reader schematic is based on a heterodyne configuration with the generation of an Intermediate Frequency (IF) signal to reduce the effect of flicker noise. The reader block schematic is shown in figure 2.3.

The two outputs of the low-pass filters (LPF), Y_1 and Y_2, go through the AD8302 from Analog Devices. It is a gain-phase detector, which is able to measure the phase and amplitude difference between two signals. Considering that the amplitude of Y_2 depends also from the amplitude of the tag response, an IF amplifier was needed after the LPF. This to compensate for the higher power present at the output of the coupler, compared with the input signal of the reader, where the tag response is present. The reader bandwidth was between 5 - 9 GHz, and its hardware cost, not including the antennas, was of 4500 € (2010). It was tested in anechoic environment with an 8 bit frequency-coded tag at few tens of centimeters. The emitted VCO output power was of 16 dBm.

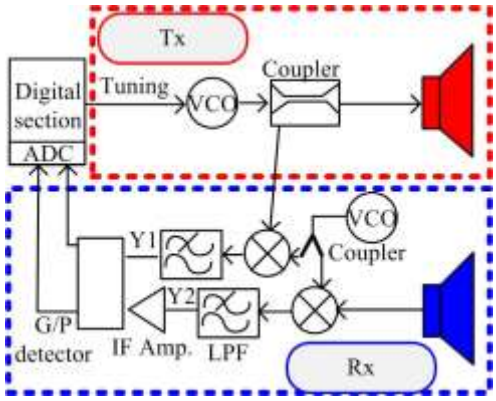


Figure 2.3. *Schematic of the UWB chipless RFID reader presented in [PRE 10].It is based on SFCW approach with a heterodyne configuration. The use of a heterodyne configuration helps to reduce the flicker noise effects due to the active devices.*

3. FMCW approach

In this section, the main FMCW UWB chipless RFID readers proposed in literature are introduced. The proposed readers were designed around specific tag's families, from frequency-coded in [KOS 12] to time-coded in [POP 16]. Both readers have the same architecture, with the use of different components that grant for diverse reader performance.

In a FMCW approach the instantaneous frequency of the transmitting and receiving signal have an offset Δf which is proportional to the distance of the tag. This generate a beat signal in reception where is encoded the tag ID as demonstrated in the next sub-section 3.1.1. [CHA 00].

3.1. Frequency-coded tag reader

In [KOS 12], the authors proposed a UWB chipless RFID reader based on chirp signal interrogation. This reader was optimized for frequency-coded tags, and its hardware architecture may be considered invariant with respect to a bi-static UWB FMCW radar. A photo of the proposed reader with the tag used as proof of concept, and its schematic representation, are shown in figure 2.4. The reader is composed of two boards, one for the digital processing and the other one, on top, for the analog circuitry. The analog board was realized on Taconic TLX-0 which has a relative permittivity of 2.45, and a thickness of 0.5 mm. The reader works in the bandwidth 4 - 8 GHz, and is used with two UWB monopole antennas, with a bandwidth of 3.6 - 7 GHz. The tag was a frequency coded with 9 bits having

two cross-polarized UWB antennas, and spiral resonators as notch filters. The coding technique was based on a presence/absence approach.

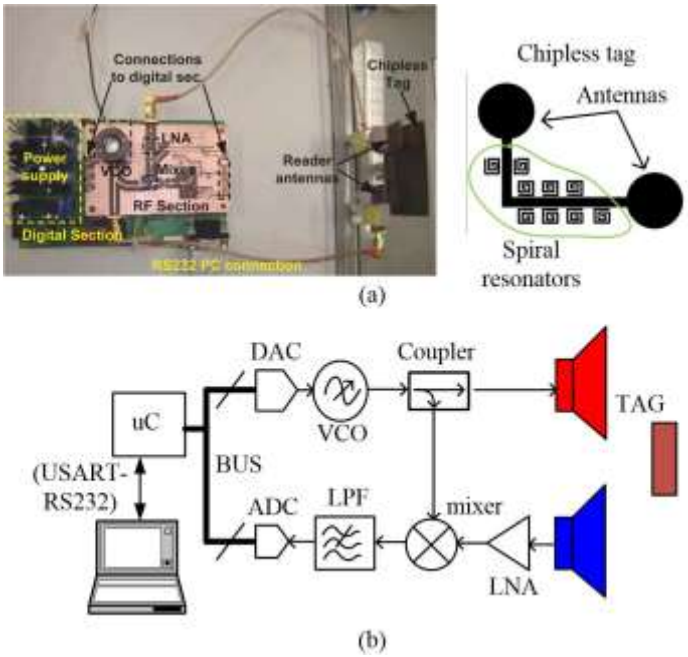


Figure 2.4. *(a) UWB chipless RFID reader proposed in [KOS 12] with a photo of the frequency-coded tag used as proof of concept. (b) Architecture of the reader, it presents the same hardware structure of a FMCW radar in bi-static configuration.*

3.1.1. Limitation on reading frequency-coded tag

To stress the limitations of a UWB FMCW chipless RFID reader to read frequency-coded tag an analytical analysis is proposed. The equations are partially based on [KOS 12], and [CHA 00]. The tag is supposed to be interrogated with a linear frequency modulated signal as shown in figure 2.1(b). The interrogation starts at t = 0 s from the minimum frequency of the VCO, called f_0, to the maximum frequency equals to $f_0 + BW$. The VCO is modulated with a saw tooth signal of repetition frequency f_p. The transmitting signal (VCO output) $X_t(t)$ toward the tag can be approximated with the equation [2.1].

$$X_t(t) = \cos(2\pi \int_0^t (f_0 + BW f_p t')dt') \qquad [2.1]$$

For simplicity the four antennas, two of the reader and two of the tag, are considered as ideal irradiators where the signal is only attenuated. T_{path} is the time that the VCO output signal takes to travel all the way to the RF input of the receiving mixer crossing the tag, the antennas, the RF cables, the PCB components, and the free space. This signal will be varied

in amplitude, $TM(f)$, and in phase, $T\theta(f)$, according with the tag transfer function. The objective of the reading process is to obtain the amplitude $TM(f)$, and the phase, $T\theta(f)$ of the transfer function of the tag. In the proposing case of study, the instant frequency of $X_t(t)$ is not constant as for CW, and therefore in first approximation, $TM(f)$ and $T\theta(f)$ may be inserted in the time domain expression of the equation [2.1] resulting in the equation [2.2].

$$Y_r(t) = TM(f^i)cos\left(2\pi \int_0^{t-T_{path}} (f_0 + BWf_p t')dt' - T\theta(f^i)\right) \quad [2.2]$$

$Y_r(t)$ is the signal at the RF input of the mixer, and f^i represents approximately the instantaneous frequency of the transmitting signal at the time $t - T_{path}$. The output of the mixer after the LPF can be expressed as:

$$\begin{aligned} &Y_{ADC}(t) = TM(f^i)cos\left(\left(2\pi \int_0^t (f_0 + BWf_p t')\right)dt' - 2\pi \int_0^{t-T_{path}} (f_0 + BWf_p t')dt' - \right. \\ &\left. T\theta(f^i)\right) = TM(f^i)cos\left(\left(2\pi \int_{t-T_{path}}^t (f_0 + BWf_p t')\right)dt' - T\theta(f^i)\right) \\ &= TM(f^i)cos\left(\left(2\pi(f_0 T_{path} + \frac{f_p {T_{path}}^2 BW}{2} + f_p T_{path} BWt\right) - T\theta(f^i)\right) \approx \\ &TM(f^i)cos\left(\left(2\pi(f_0 T_{path} + f_p T_{path} BWt\right) - T\theta(f^i)\right) \end{aligned} \quad [2.3]$$

The instantaneous frequency of the transmitting signals is known and equals to $f_0 + BWf_p t$ (from equation [2.1]). Once $Y_{ADC}(t)$ is digitalized, it is possible to obtain the two components $TM(f^i)$ and $T\theta(f^i)$, using the Hilbert transform. The possibility to obtain the two information separately, is due to the generation of the beat frequency $f_p T_{path} BW$ equals to Δf of figure 2.1(b). The equation [2.3] is the results of many approximations. The influence of the antennas, and the coupling and the echoes from the environment, were not considered.

3.1.2. Influence of the VCO sweep time on the reading performance

The accuracy that can be reached using a FMCW reader depends also from the product BWf_p. A small value means that the chirp interrogating signal is sweeping slowly around the tag bandwidth. The tag output will reach its stable state according to the input instantaneous frequency. On the other side, the beat signal frequency ($f_p T_{path} BW$) will be excessively small, making complex the estimation of the amplitude, and the phase components ($TM(f^i), T\theta(f^i)$) separately.

Increasing BWf_p means a VCO with a higher input bandwidth so a reduced sweep time. The beat frequency ($f_p T_{path} BW$) will be increased, and the application of the Hilbert transform more effective. However the approximation made in the time domain, with the

introduction of the components $TM(f^i)$ and $T\theta(f^i)$, will not worth anymore. Thus, the measured signals $TM(f^i)$ and $T\theta(f^i)$ will be a kind of mean in a bigger bandwidth, and they will not be referred to the precise instantaneous input frequency resulting in a less accurate estimation of the tag spectral characteristic.

3.1.3. Simulation result

This sub-section shows the effect of a variable sweep-time on the reading accuracy of a frequency-coded tag. A Matlab Simulink model of a FMCW UWB chipless RFID reader is shown in figure 2.5. It was used to read a tag based on one resonator in cross-polarization. All the components are ideal, and the attenuations of the reader cables, the antennas, the free space loss and the tag antennas were not taken into consideration. The propagation delay between the VCO output in transmission and the mixer RF input in reception, were modelled with two ideal transport delay blocks. The tag was interrogated with a CW signal whose instantaneous frequency was varying linearly between 2 and 6 GHz, with a saw tooth modulating signal. Different simulations were performed varying the sweep time $(1/f_p)$ between 100 ns and 100 us, where the BW was fixed at 4 GHz according to [KOS 12]. The tag resonator was modelled with a RLC series circuit terminated with a 50 Ω load. Its resonant frequency was at 4 GHz with a quality factor of 100 that is consistent with REP based resonant particles [VEN 16].

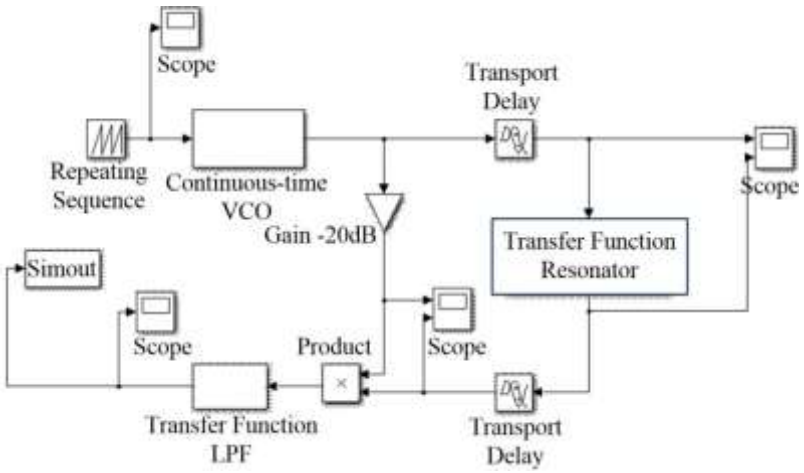


Figure 2.5. *Matlab Simulink model of a FMCW UWB chipless RFID reader. The tag is a solely scatterer based on REP principle, and represented with its transfer function. The delay introduced by the cables and the devices are represented with the two transport delay blocks. The transfer function of the tag is the tag mode response of a resonator at the frequency of 4 GHz with a quality* factor of 100.

The simulation results of the model of figure 2.5 are shown in figure 2.6 for a sweep time of 100 ns, 1 us, and 10 us. The modules of the analytical receiving signal obtained with the Hilbert transform is shown in figure 2.6 (a). All the curves were normalized with respect to the most favorable sweep time of 10 μs. The normalized module of the transfer function of the tag is shown in green dotted line on the figure.

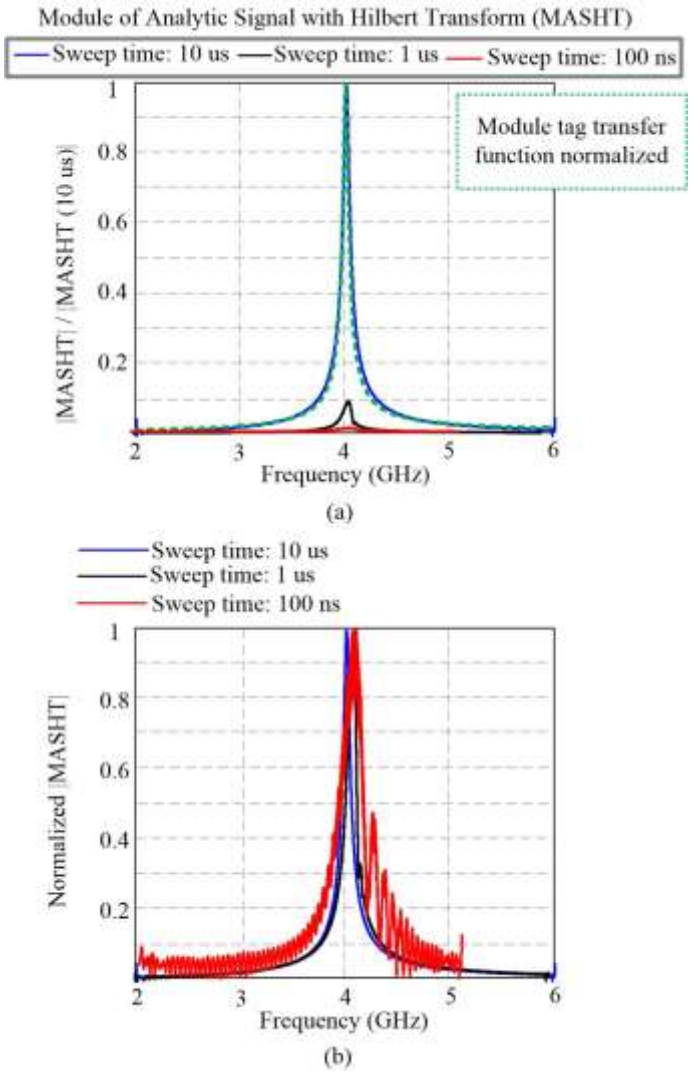


Figure 2.6. *Simulation results of the model in figure 2.5 for the sweep time of 100 ns, 1 us, and 10 us. (a) Module of the analytical receiving signal obtained with the Hilbert transform. All the curves were normalized with respect to the more favorable case represented by the bigger sweep time of 10 us. In the figure in green dotted line is also shown the normalized module of the transfer function of the tag. (b) The normalized three sweep time cases of (a).*

From figure 2.6 (a) the module of the analytical signal, obtained with the Hilbert transform, matched perfectly the response of the tag for a sweep time of 10 μs. At a shorter sweep time

corresponds a smaller energized signal [KEY 16], as shown in figure 2.6 (a). The three sweep time cases normalized results are shown in figure 2.6 (b). From simulation, the phase variation $T\theta(f^i)$ introduced by the transfer function, was excessively small to be effectively detected. In equation [2.3], $T\theta(f^i)$ represents a phase variation corresponding to the high frequency chirp interrogating signal, and not to the smaller beat frequency $f_p T_{path} BW$. In case the tag has the information coded only with the tag phase characteristics, a shorter sweep time is advisable to increase the beat frequency, otherwise a compromise needs to be found.

3.1.4. Conclusion

From [KOS 12] and the proposed simulation model, a frequency-coded tag may be read with a reader architecture close to a FMCW radar. The sweep time of the transmitting VCO plays a fundamental role to retrieve the tag transfer function characteristics ($TM(f^i)$, $T\theta(f^i)$). A short sweep time allows for a better implementation of the Hilbert transform, and the retrieve of tag phase characteristics $T\theta(f^i)$. However, it shows lower analytic module signal amplitude as shown in figure 2.6 (b). A long sweep time produces a small beat frequency $f_p T_{path} BW$, hence the estimation of $T\theta(f^i)$ is more difficult, but it allows for a higher analytic module signal amplitude, and thus a better $TM(f^i)$ estimation.

In the sub-next section will be demonstrated how the reading of a time-coded tag using a FMCW approach is easier than a frequency-coded tag, and less error-prone.

3.2. Time-coded tag

3.2.1. Time-coded tag as collection of steady targets

A time-based UWB chipless RFID tag may be seen as a different number of steady targets located in the direction of the reader [GIR 13]. This implies the absence of any Doppler effects that may complicate the reading. For simplicity, a time-coded tag with only one reflector is considered. It may be seen as two ideal targets, the closer responsible for the tag structural mode, and the farer for the antenna (tag) mode. If the two targets are not influencing each other during a reading process, then the equation [2.3] can be applied at each of them independently, giving the equation [2.4] for the tag structural mode, and equation [2.5] for the antenna (tag) mode.

$$Y_{ADC}(t) \approx TM_S(f^i) cos\left(\left(2\pi(f_0 T_{path-S} + f_p T_{path-S} \mathrm{BW} t\right) - T\theta_S(f^i)\right) \qquad [2.4]$$

$$Y_{ADC}(t) \approx TM_T(f^i)cos\left(\left(2\pi(f_0T_{path-T} + f_pT_{path-T}\mathrm{BW}t\right) - T\theta_T(f^i)\right) \quad [2.5]$$

$TM_S(f^i)$ and $T\theta_S(f^i)$ are referred to the reflective characteristic of the tag structural mode, and $TM_T(f^i)$ with $T\theta_T(f^i)$ for that of the antenna (tag) mode. Because the tag is approximated with two ideal reflective targets, the aforementioned parameters may be considered invariant with frequency. T_{path-S} and T_{path-T} are the total propagation delay between the VCO output and the mixer RF input, respectively for the signal reflected back from the structural mode, and for the antenna (tag) mode.

In a time-based tag the information is coded on the timing distances between the different targets, and from equations [2.4]-[2.5], it may be retrieved measuring the difference between the two beat frequencies $f_pT_{path-S}\mathrm{BW}$ for the structural mode, and $f_pT_{path-T}\mathrm{BW}$ for the antenna (tag) mode. The difference between T_{path-T} and T_{path-S} depends on the propagation delay between the two targets. A time based UWB chipless RFID tag is supposed to have resolution in the orders of ns, it brings to a frequency difference of:

$$f_{diff} = f_p\mathrm{BW}1ns \quad [2.6]$$

From equation [2.6], the difference between the two beat frequency depends linearly from the bandwidth of the reader BW, and from the sweep time with f_p. A fast FMCW with a high bandwidth will read the time-based tag with a better timing resolution increasing the tag bit capacity. The reader proposed in [KOS 12] and analyzed in this section may be used to read time-based tags, where the Hilbert transform is substituted with a spectral analysis of the ADC output to retrieve the distances between all the generated beat frequencies.

3.2.2. Low cost solution

The lack of interest in retrieving the transfer function of a time-based tag with $TM(f^i)$ and $T\theta(f^i)$, opens for a low cost reader design reducing the band of interest BW. This principle was exploited in [POP 16], where a low-cost FMCW reader for time-based tags is proposed. The reader block schematic and a photo of its RF front-end are shown in figure 2.7. The transmitting signal is generated by a VCO whose frequency is stabilized with a fractional synthesizer PLL. As a result of the VCO (10 dBm) high power output, and the gain of the transmitting and receiving antennas (20 dBi), the reader does not need an output power amplifier. The demodulating block is composed of a mixer and a LPF, with a coupler realized directly on layout. The tag, also shown in figure 2.7, has been optimized to work in co-

polarization, where the reading was performed in an anechoic chamber at a distance of 50 cm. The hardware implementation without the antennas was around 250 € in 2016.

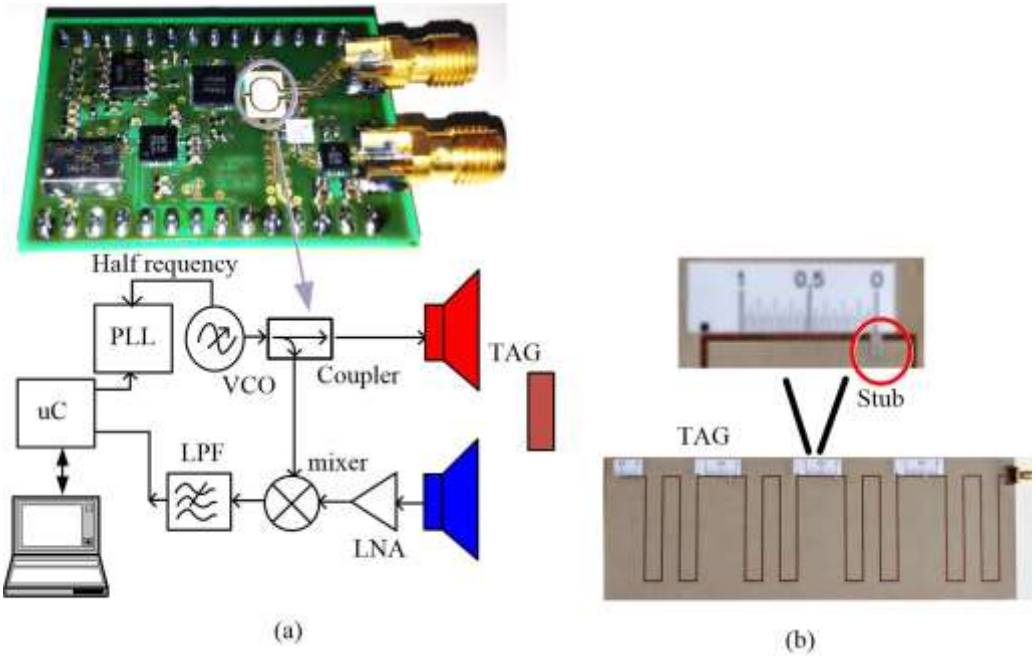


Figure 2.7. *(a) Analog board photograph of the UWB chipless RFID reader proposed in [POP 16] and its architecture. It is similar to [KOS 12]. Its lower cost is due to its limited bandwidth. (b) The time coded tag is composed of four scatterers with stub loads.*

The tag was realized on Rogers RT/duroid 6006 substrate and presents four scatterers realized with parallel stubs. The tag dimensions are prominent and of about 23.7 cm × 8.2 cm. The measurement process in [POP 16] uses a calibration tag to remove multiple reflections outside that of the tag reflectors. The tag was successfully tested, whereas no results in practical environment are reported.

The cost of the VCO can be a strong handicap towards the design of a wideband reader. In [POP 16] it has a limited bandwidth of 1.25 GHz centered at 7.825 GHz representing an inexpensive solution. The PLL Analog Devices HMC703LP4E is provided with a frequency sweep mode, and is used to control the VCO Analog Devices HMC508LP5E in feedback loop. The VCO has two outputs, one is the higher frequency called RF output, and the other one is at half frequency, and is connected with the PLL to form the loop. In reception after the usual LPF, the microcontroller STM32F407 from STMicroelectronis provides the digital

conversion. This solution is the solely designed around time-coded tag on literature, and represents the cheapest UWB chipless RFID reader currently available.

4. SFCW-FMCW vs IR-UWB

4.1. Introduction

A UWB chipless RFID reader based on IR-UWB uses sub-nanoseconds UWB pulses to characterize the tag and therefore represents a time based solution as shown in figure 2.1. A schematic of an IR-UWB UWB chipless reading system, which employs laboratory equipment, is shown in figure 2.8. A pulse generator triggers the Digital Signal Oscilloscope (DSO), and transmits a sub-nanosecond UWB pulse towards the tag. Then the DSO measures the backscattered signal from the environment, in a bi-static configuration. In alternative, a diplexer can be used to obtain a mono-static reader. The IR-UWB configuration helps to send an interrogating signal with the maximum instantaneous power compared with SFCW and FMCW, which interrogates the tag for a longer period of time.

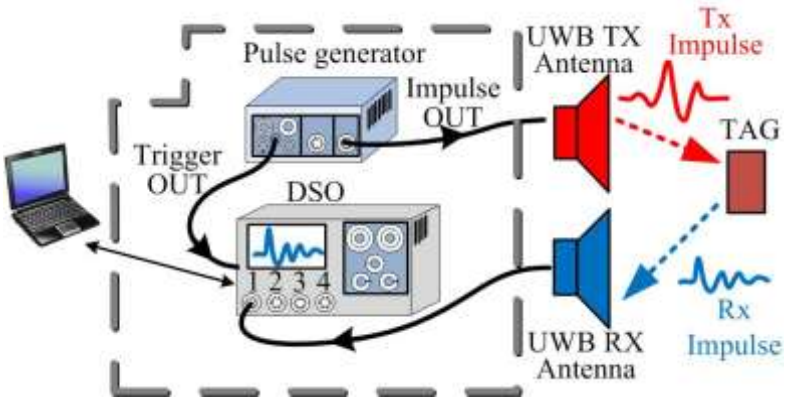


Figure 2.8. *Bi-static chipless reading system based on IR-UWB approach consisting of laboratory equipment. A pulse generator, which triggers the Digital Signal Oscilloscope (DSO), sends a sub-nanosecond UWB signal toward the tag, and then the DSO measures the backscattered signal from the environment.*

An IR-UWB approach shows a reduced reading time due to the absence of a sweep in frequency domain. The sweep time of a frequency domain solution is directly proportional to the bandwidth of the reader. In [KOS 12] it is equal to 500 ms, and for an estimation of a row reading time, all the post processing treatment, and an eventual data transfer to a central unit should be added. Moreover, if a sweep averaging process is used, the reading time could reach several tens of seconds. In [POP 16], the sweep time is limited to 10 ms, however its

bandwidth is of only 1.25 GHz as so the proposed reader may hardly be employed to read high bit capacity tags (frequency-coded tag).

4.2. UWB regulations

In 2002 the FCC issued its first radio-regulation for UWB [FCC 17], subsequently Europe followed with the ETSI [ETS 04-ETS 10]. The UWB is an unlicensed bandwidth and therefore free to be used. It is characterized by low power transmission, where the limitations depend on the applications.

Both FCC and ETSI define limits for the maximum average power spectral density, and the maximum peak power. The maximum peak power is defined over a bandwidth of 50 MHz around the maximum measured average spectral density. The latter is measured with a resolution of 1 MHz. The FCC and ETSI masks for the maximum peak power and maximum average power spectral densities are shown in figure 2.9. An IR-UWB reader has a higher instantaneous transmitted power than a frequency domain reader. Thus, the maximum peak power mask represents the major constraint for the IR-UWB solution, while is the maximum average power mask for SFCW and FMCW readers.

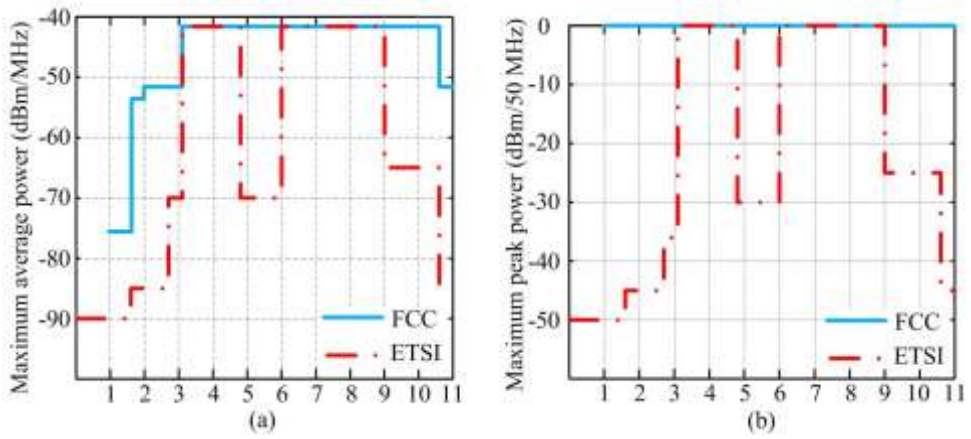


Figure 2.9. *FCC and ETSI mask for communication application with the respective most favorable case. a) Maximum average power. b) Maximum peak power.*

4.3. Link budget

A study of the link budget in the case of a chipless RFID systems taking into account the regulations is proposed. The equation [2.7] is the radar equation (Friis), where G_T is the gain

of the transmitting antenna, G_R is the gain of the receiving antenna, σ is the RCS of the tag for that frequency, λ is the wave length of the carrier frequency, R is the distance of the tag, P_T is the transmitting reader power, and finally P_R the reader receiving power.

$$P_R = \frac{P_T G_T G_R \lambda^2}{(4\pi)^3 R^4}\sigma \qquad [2.7]$$

For a frequency domain reader, the frequency of the carrier is sweeping between a minimum and a maximum value. Thus, the receiving power from the reader is also sweeping in frequency during the same period of time depending on the period of the modulating signal. The maximum average power between 3.1-10.6 GHz, for the most favorable case, is of -41.3 dBm/MHz as shown in figure 2.9 (a). It is equivalent to the instantaneous power transmitted by the reader in case its sweep time is bigger than the sweep time of the Signal Analyzer (SA) used to check the compliant with the maximum average power mask. From regulations, the sweep time of the SA is maximized by 1 ms/ MHz. If the reader has a shorter sweep time, it may have a maximum average power higher than -41.3 dBm/MHz. Substituting -41.3 dBm/MHz to $P_T G_T$ the equation [2.8] shown in dB, is obtained.

$$P_R = -41.3\ dBm + 10log10(\frac{G_R \lambda^2}{(4\pi)^3 R^4}\sigma) \qquad [2.8]$$

In case of IR-UWB approach the reader transmits all the energy of its UWB pulse concentrated in a small fraction of time, while in a frequency domain reader it is distributed in time. Thereby the equation [2.7] can be integrated around the band of interest, which is the frequency resolution of the IR-UWB reader (RBW), giving the equation [2.9].

$$P_R = \frac{G_R \lambda^2 \int_{fa}^{fb} P_T G_T df}{(4\pi)^3 R^4}\sigma \qquad [2.9]$$

In equation [2.9], the product $P_T G_T$ needs to be defined according with the masks. For an IR-UWB approach, the most restrictive mask is the maximum peak power, which in the worst case is of -34 dBm/MHz according to equation [2.10].

$$Peack_{Imp}(RBW_{New}) = Peack(RBW_{50MHz}) + 20log_{10}(\frac{RBW_{New}}{50\ MHz}) \qquad [2.10]$$

Where $Peack(RBW_{50MHz})$ is the maximum of peak power in figure 2.9 (0 dBm/(50 MHz)), and $20log_{10}(\frac{RBW_{New}}{50\ MHz})$ is the scale factor to express $Peack(RBW_{50MHz})$ for the new resolution of 1 MHz. The equation [2.9] may be expressed in dB as shown in equation [2.11].

$$P_R(dBm) = -34\ \text{dBm} + 10log10(f_b - f_a\ (MHz)) + 10log10(\frac{G_R\lambda^2}{(4\pi)^3R^4}\sigma) \quad [2.11]$$

Comparing the results of equations [2.8] (SFCW-FMCW) and [2.11] (IR-UWB), the case of IR-UWB appears more favorable, especially for time-coded tags where the spectral characteristics of the tag are not concerned, and then $f_b - f_a$ may be as big as possible. As example, if a frequency-coded tag is measured with a frequency resolution of 50 MHz, the equation [2.11] (IR-UWB) becomes,

$$P_R = -17\ \text{dBm} + 10log10(\frac{G_R\lambda^2}{(4\pi)^3R^4}\sigma) \quad [2.12]$$

Comparing the equation [2.8] and [2.12], the case of IR-UWB shows a receiving power P_R of about 24 dB bigger than the case of frequency domain. To increase P_R the reader should have a short sweep time, which is the case for a FMCW reader. This will decrease the measured maximum mean PSD over the specified interval of time for 1 MHz (1 ms for FCC, 1 us -1 ms for ETSI). However a FMCW approach shows difficulties to read frequency-coded tag as demonstrated in section 3. Other ways of increasing the transmit power to the tag are compression power methods such as pulsed frequency modulation (PFM) that have never being proposed for chipless RFID reader.

Compared with IR-UWB a frequency domain reader has a lower input noise bandwidth due to the presence of the IF filter, it will result in a reader with higher sensitivity that may compensate for the lower receiving P_R. A reader based on IR-UWB has a higher noise bandwidth due to its wide-band receiver, which is translated into high sampling noise.

Numerous works in literature exploit the IR-UWB advantages for chipless applications. They use commercial IR-UWB radar to perform reading of time-coded tags. In [RAM 16], a Time Domain PulsON P400 MRM was used to read a time-coded UWB chipless RFID tag with a read range in practical environment 5 m. In case of all the frequency domain reader proposed in literature, the read range was lower than 1 m with measurement in anechoic environment. The only reader tested in practical environment was [KOS 12] at a distance of 10 mm. In [RAM 11], the Geozondas GZ6EVK IR-UWB radar evaluation kit, composed of the GZ6E sampler converter and the impulse generator GZ1120ME-50EV, was employed to read time coded tag at 50 cm in practical environment. In [RAM 12], a Novelda NVA610 evaluation kit IR-UWB radar was used in bistatic configuration with two tapered slot Vivaldi antennas. It was able to read a time-coded tag in practical environment at a distance of 130

cm. As analytically demonstrated, a reader based on IR-UWB is preferable than a frequency domain reader when the UWB regulations are taken into consideration. It shows bigger power in reception, and reduced reading time. If the UWB regulations are not taken into account, the study of link-budget does not worth anymore.

4.4. Conclusion

A FMCW solution with reduced sweep time found not only hardware difficulty, because of the UWB VCO limited speed, but also from the tag characteristics. Indeed a frequency-coded tag implemented with REP technique, is no more than a bunch of parallel passive filters. If the sweep in frequency is excessively fast, then they will not have the time to charge themselves and reach the stable state, and the response will be lower in amplitude. This was demonstrated in [KEY 16]. A SFCW reader may be used to read both, time and frequency-based tag where the reduced P_R may be compensated by higher sensitivity compared with IR-UWB. On the other side the high sweep time will translate in high reading time especially in presence of sweep averaging [KOS 12]. An IR-UWB architecture is preferable to design a UWB Chipless RFID reader compliant with international regulations, and which is capable to read both, time-coded and frequency-coded tags. It has higher P_R and a reduced reading time for the absence of any frequency sweeping in transmission that makes it ideal for a real time application. The hardware design of an IR-UWB reader has to be optimized to reduce its sampling noise (high input noise bandwidth).

5. Conclusion

In this chapter the state of the art of UWB chipless RFID readers has been reviewed. The totalities of the proposed solution are based on SFCW [PRE 10] or FMCW [KOS 12 - POP 16] and their main characteristics shown in table 2.1. Both frequency domain approaches are able to read time-coded and frequency-coded tags, with their main characteristics shown in table 2.1. The SFCW solution provides better reading for frequency-coded tags while the FMCW is ideal for time-coded tags and low cost reader design. The tag reading time exceeds readily 1 s depending on the VCO sweep time and averaging.

The IR-UWB architecture has been introduced, it grants for faster reading because no sweep frequency process in transmission is needed. The international UWB regulations have been introduced, and based on that a link-budget was proposed. It took into consideration both, frequency domain and IR-UWB reader approach, where the IR-UWB shown higher

receiving power. However its hardware architecture has to be optimized to reduce the sampling noise.

	SFCW	FMCW	
	[PRE 10]	[KOS 12]	[POP 16]
VCO Sweep time	No info	500 ms	10 ms
Bandwidth (GHz)	5 - 9	4 - 8	1.25
Components cost estimated (€)	4,500	650	250

Table 2.1. *Main characteristics of major UWB chipless RFID readers presented in literature, all the readers are based on frequency approach. The cost estimation is not considering the antennas used for the shown measurement results.*

In the next chapter will be discussed the first reader version designed during the thesis period. Since the results of this chapter, it was designed around the IR-UWB approach.

6. References

[CHA 00] CHANG K., *Chapter 7: Radar and Sensor Systems*, RF and Microwave Wireless Systems: John Wiley & Sons, 2000, pp. 212-222.

[ETS 04] ETSI TR 101 994-1 V1.1.1 ("Electromagnetic compatibility and Radio spectrum Matters (ERM); Short Range Devices (SRD); Technical characteristics for SRD equipment using Ultra Wide Band technology (UWB) Part 1: Communications applications", *European Telecommunication Institute (ETSI),* Janu. 2004.

[ETS 10] ETSI EN 302 065 V1.2.1 "Electromagnetic compatibility and Radio spectrum Matters (ERM); Short Range Devices (SRD) using Ultra Wide Band technology (UWB) for communications purposes; Harmonized EN covering the essential requirements of article 3.2 of the RTTE Directive", *European Telecommunication Institute (ETSI),* Oct. 2010.

[FCC 17] Title 47 Telecommunication chapter 1 subchapter A Part 15 subpart F-Ultra-wideband operation, online available at : www.FCC.org.

[GIR 13] GIRBAU D., RAMOS A., LÁZARO A., et. al., "UWB time-coded RFID sensors: A comparison between passive and semi-passive approaches," ICECom 2013, Dubrovnik, 2013, pp. 1-4.

[KEY 16] KEYSIGHT TECHNOLOGIES, "Spectrum Analysis Basics", Application Note 150, 2016.

[KOS 12] KOSWATTA R.V., KARMAKAR N.C., "A Novel Reader Architecture Based on UWB Chirp Signal Interrogation for Multiresonator-Based Chipless RFID Tag Reading," in *IEEE Transaction on Microwave Theory and Technique, vol. 60, no. 9*, pp. 2925-2933, Sept. 2012.

[POP 16] POPPERL M., CARLOWITZ C., VOSSIEK M., et. al.,"An ultra-wideband time domain reflectometry chipless RFID system with higher order modulation schemes," in German Microwave Conf (GeMiC), pp. 401-404, 2016.

[PRE 10] PRERADOVIC S., KARMAKAR N.C.,"UWB Chipless Tag RFID Reader Design," in *IEEE International conference on RFID-Technology and Applications*, Jun. 2010.

[RAM 11] RAMOS A., LAZARO A., GIRBAU D. et al., "time-domain measurement of time-coded uwb chipless rfid tags", in *Progress In Electromagnetics Research*, Vol. 116, 313-331, 2011.

[RAM 12] RAMOS A., LAZARO A., GIRBAU D. et al., "IR-UWB radar system and tag design for time-coded chipless RFID," in *6th Eurpean Conference on Antennas and Propagation (EUCAP)*, pp. 2491 - 2494, march 2012.

[RAM 16] RAMOS A., LAZARO A., GIRBAU D. et al., "Signal processing techniques for chipless UWB RFID thermal threshold detector detection," in *IEEE Antennas and Wireless Propagation Letters*, vol. 26, pp. 618-621, 2016.

[VEN 16] VENA A., PERRET E., TEDJINI S., *Chapter 4: Design of Chipless RFID Tags*, Chipless RFID based on RF Encoding Particle, ISTE Press – Elsevier, 1st Edition, pp. 98 - 122.

3

IR-UWB Chipless RFID Reader Design

1. Introduction

In this chapter is presented the first version of the IR-UWB Chipless RFID reader designed during the first part of the thesis. It is a fully working reader, and the first custom published chipless RFID reader based on IR-UWB approach. The chapter is organized as follow:

- Section 2 introduces an IR-UWB reader system based on test equipment and used to read frequency-coded UWB chipless RFID tags. It is a real time system with a realization cost and overall dimensions not suitable for a commercial solution.
- Section 3 introduces the sequential equivalent time principle, which helps to design low cost electronic systems. Thus, all the proposed designed readers on this thesis are based on sequential equivalent time.
- Section 4 shows the first fully working reader developed before the beginning of the thesis.
- Section 5 describes the hardware architecture of the integrated reader version designed during the first part of the thesis. It shows a substantial retail cost reduction on its hardware components, and better performance. The reader characterization stressed possible ameliorations in the design for a more performing reader.
- Section 6 shows some frequency-coded tag measurement with the reader introduced in section 5.
- Section 7 draws the conclusion of the chapter.

2. IR-UWB reading system based on test equipment

The IR-UWB approach has been introduced in the second chapter. The transmitting signal is a sub-nanosecond UWB pulse that may be used to read both, time-coded and frequency-coded tags.

The reading scenario of a UWB chipless RFID tag is shown in figure 3.1 (a). The reader is composed of a pulse generator, a device to measure the tag response in time domain such

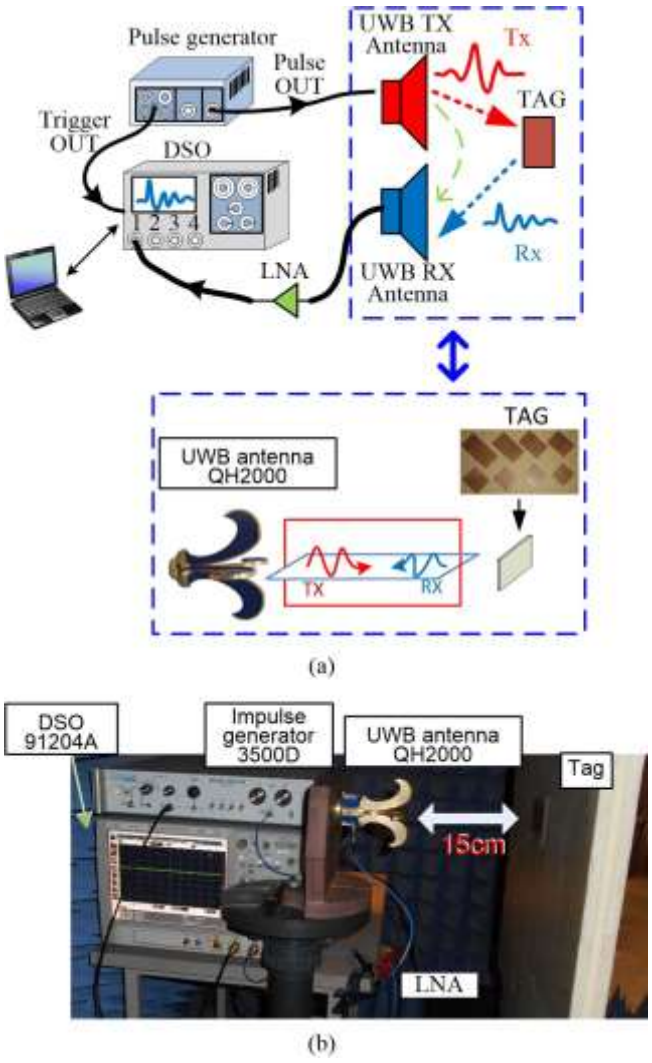


Figure 3.1. *Bi-static chipless reading system based on IR-UWB approach, and composed of test equipment. (a) Schematic of the actual reading system employed. The reading was performed in cross-polarization using the dual access Satimo QH2000 antenna. (b) Photo of the test bench in anechoic chamber. The tag was the depolarizing REP tag introduced in [VEN 13], and already presented in chapter 1. It was placed at 15 cm from the antenna.*

as a DSO, and a PC that may be used as control and post processing unit. A Low Noise Amplifier (LNA) can be connected at the input of the DSO. The pulse generator triggers the DSO during the acquisitions. The corresponding test bench used to read chipless tags is shown in figure 3.1(b). The DSO was the Agilent 912004A, which features an analog bandwidth of 12 GHz, and a sampling rate of 40 GSa/s. The pulse generator was the Picosecond 3500D, it produces pulses with 65 ps of Full Width at Half Maximum (FWHM), and amplitude of 8 V on a 50 Ω load. The tag was the depolarizing REP tag introduced in [VEN 13], and already presented in chapter 1. The tag was placed at 15 cm from the end (the closer point to the tag) of the dual access Satimo QH2000 antenna. The measurements were performed in anechoic chamber to reduce has much as possible external EM disturbances. The PC was connected to the UWB slave port of the DSO, where a Graphical User Interface (GUI) was developed and described in Appendix I to control the DSO.

The tag was read in cross-polarization configuration as shown in figure 3.1 (a), and read with the background subtraction technique introduced in chapter 1. The latter consists in two measurements, one with the tag (tag measurement), and another without the tag (background measurement). After in post processing, a subtraction between the two results in time domain is performed to isolate the tag contribution from the measured signals. The measurement with the tag is shown in figure 3.2 (a), and the subtraction result is shown in figure 3.2 (b). The tag contribution is the less powerful part of the signal, while the most significant one it is represented by the direct coupling between the antenna ports (even if they are characterized by an isolation of around 40 dB). It represents the leakage of the presenting reading system, and is shown in figure 3.1 (a) with the dashed green line. To retrieve the tag ID, it is sufficient to analyze the signal of figure 3.2 (b) in frequency domain, and the correct frequency resonant positions (peak in spectrum) as shown in figure 3.2 (c).

3. Sequential equivalent time approach

The reading system shown in figure 3.1 is a real time implementation, thanks to the DSO high sampling rate of 40 Sa/s. The objective of this thesis is the design of a reader which is also low cost, therefore an equivalent time reading approach has to be used. In a sequential equivalent time approach, the reader transmits the same interrogating signal towards the tag, at intervals corresponding to the Pulse Repetition Frequency (PRF) period. Subsequently, the reader samples only few points of each backscattered signal from the tag to reconstruct

the entire signal. This is possible as long as the reading scenario is stationary between the different interrogations. Note also that a measurement is composed of many contributions, such as the response from the tag, the environmental contribution and the coupling between the antennas (leakage). This procedure is performed with a much lower sampling frequency than the one required in a real time approach, which follows the Nyquist-Shannon sampling theorem.

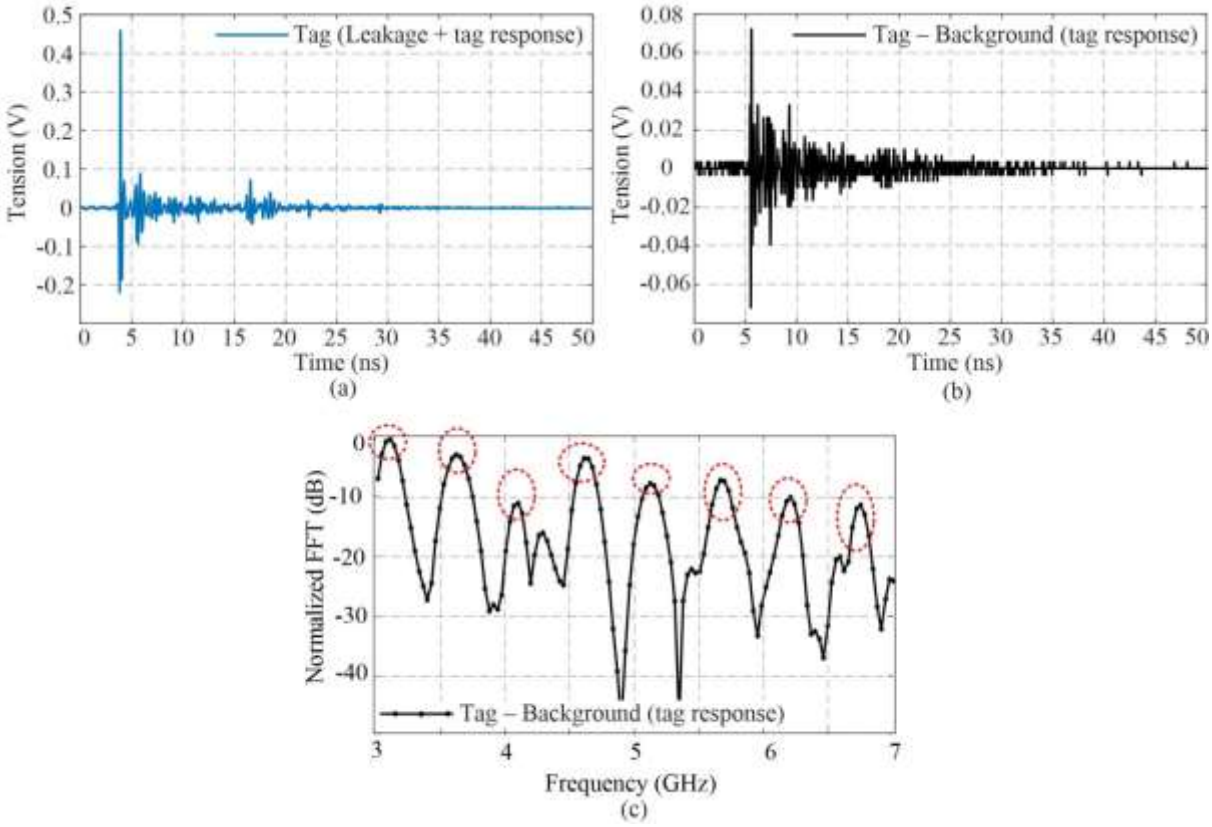


Figure 3.2. *Measurement results in time domain of the test bench presented in figure 3.1. (a) Tag measurement where the tag contribution and antenna leakage are part of the signal. (b) Background subtraction measurement to isolate the tag contribution from antenna leakage. (c) Frequency analysis of tag contribution (b); in read dotted circles, the position of the eight tag resonant frequencies (ID).*

The sequential equivalent time algorithm is summarized in figure 3.3, where the left-side shows the sampling process, whereas the right-side the subsequent tag response reconstruction. Between the distinct acquisitions, the sampling clock is shifted of few picoseconds ΔT, to take all the points corresponding to the measuring signal. Each acquisition starts after a trigger event, which is usually generated by the reader control unit or pulse generator. Finally, in the reconstruction process, all the samples in the reader memory are rearranged together to retrieve the measuring signal. The equivalent sampling frequency

of the system is therefore 1/ ΔT. With this approach the reader can emulate a high speed sampling system, such that in figure 3.1. The reading procedure can be executed with an averaging by repeating the tag interrogation sequence. It is useful to improve the Signal-to-Noise Ratio (SNR), and to avoid outside disturbances from other EM signals [VEN 14]. In the next section the IR-UWB reader designed before the beginning of the thesis is presented.

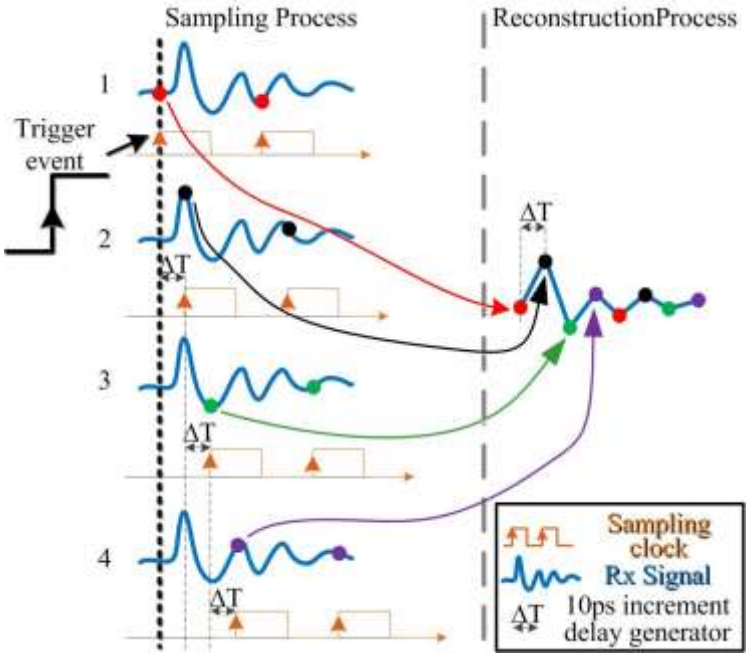


Figure 3.3. *Sequential equivalent time principle. The signal of interest (Rx impulse), is sampled with a low sampling frequency (Sampling clock), that does not respect the Nyquist-Shannon theorem. As so, only few points of the response of the tag are acquired. Different pulses are sent to the tag, and for each response the sampling clock is shifted with steps of few picoseconds, ΔT. The synchronization is entrusted on a trigger event.*

4. Reader developed previous the start of the thesis

The thesis started in February 2014, and before that a first fully working reader version was developed during the two years of the project called *Gravit*, which kick-off was in December 2010. In this section is first detailed the schematic of the prototype, and after it will be put in relation with the figure 3.3 to explain the hardware implementation of the sequential equivalent time algorithm.

4.1 Schematic

The retail cost of the evaluation boards and hardware components that compose the reader prototype was of about 5,638 € after tax (see table 3.1), where the antennas are not considered. The block diagram of the reader is shown in figure 3.4. The hardware was conceived for a bi-static implementation to reduce the leakage between the transmitting and receiving hardware parts. The pulse generator is triggered by the digital section, and its output is directly connected with the transmitting UWB antenna. In reception the RF front-end is made of a LNA in series with a sample and hold amplifier, hereafter just called S/H amplifier, and afterword an Analog to Digital Converter (ADC), whose output is connected with the digital section.

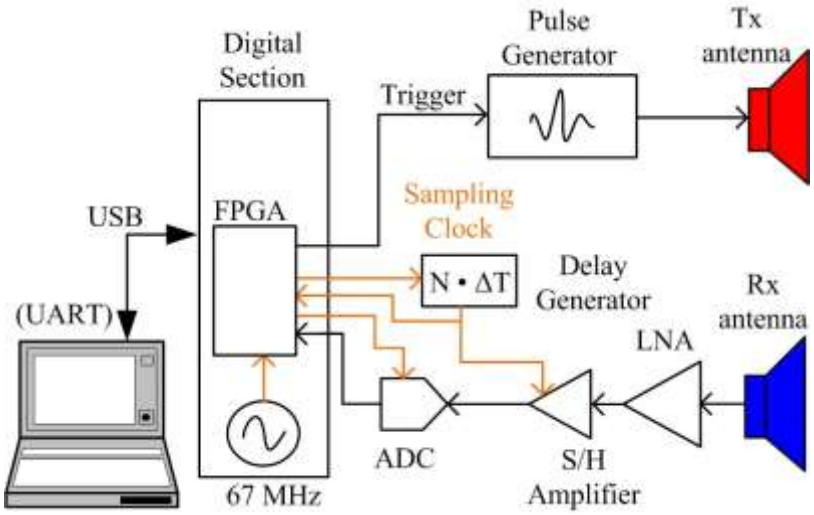


Figure 3.4. *Architecture of the fully-working designed reader during the project Gravit. It has a bi-static configuration, and it is composed of three parts: an UWB pulse generator, a digital section, and the receiving RF front-end.*

A photo of the reader is show in figure 3.5. The LNA was the Miteq AMF-4D-00101200-34-13P, it has a gain of 40 dB, and a bandwidth of 0.1 – 12 GHz. The maximum noise figure is of 3.4 dB and the minimum output 1 dB compression point is of 13 dBm. It needs a supply voltage of 15 V and 325 mA of current. The S/H amplifier was the Inphi 1321TH on its evaluation board; it has an input bandwidth of 0 - 13 GHz, and a maximum sampling clock of 2 GSa/s. The differential output of the S/H amplifier was connected to the analog input of a home designed four layers board, on FR-4 substrate that is part of the reader RF front-end. Its main components are the ADC, and the delay generator.

The ADC was the low cost AD9215 from Analog Devices, it has a vertical resolution of 10 bits. The ADC input is supposed differential and may be 1 or 2 V_{P-P}. It shows an input bandwidth of 300 MHz and a maximum sampling clock of 80 MSa/s. The delay generator was implemented with two chips (MC100EP196 from ON Semiconductor) connected in series, where each has an input digital bus of 10 lines to set up the internal delay. They are able to delay a 50 % duty cycle clock signal between 2.4 ns and 12.4 ns, with a minimum step ΔT of 10 ps (see figure 3.3). The sampling clock period of the reader is of about 15 ns (67 MHz), therefore the use of two chips was indispensable.

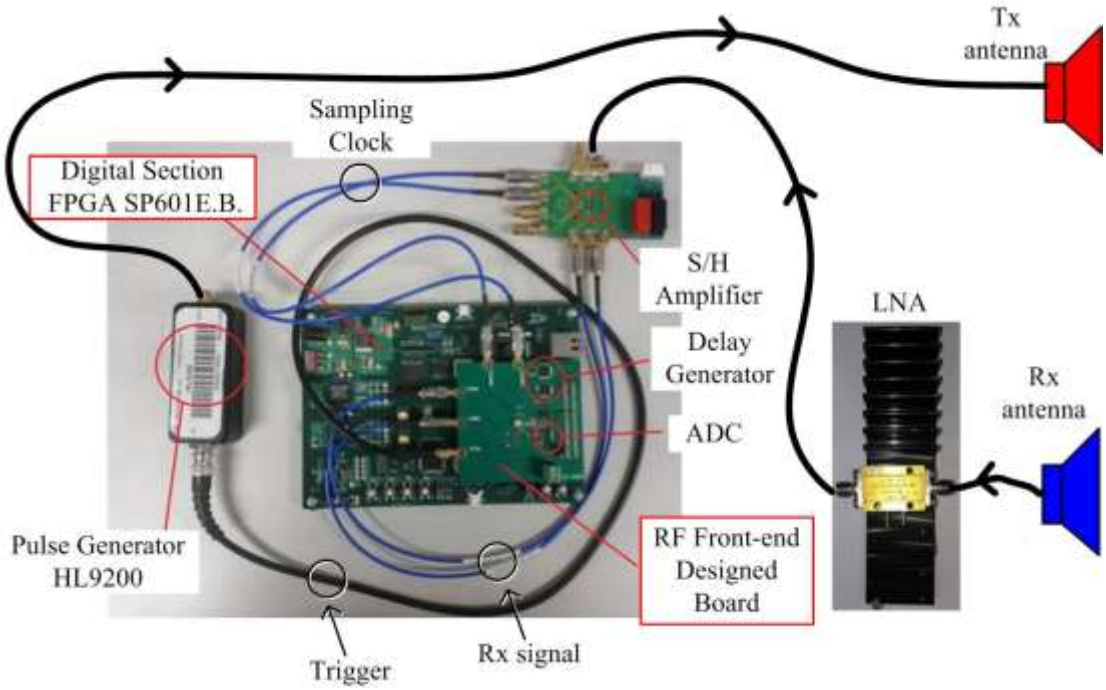


Figure 3.5. *Photo of the fully-working designed reader during the project Gravit. The pulse generator was the HL9200 from Hyperlabs. The digital section was enclosed in a Xilinx SP601 evaluation board for the FPGA Spartan 6 XC6SLX16. The four layers RF front-end board was realized on FR-4 substrate. The LNA is the Miteq AMF-4D-00101200-34-13P. The sampling and holding amplifier was the Inphi 1321TH on its evaluation board.*

The digital section was enclosed in a Xilinx SP601 evaluation board for a FPGA Spartan 6 XC6SLX16. The pulse generator was the HL9200 from Hyperlabs. It can generate a wide-spectrum pulse in the frequency domain extended into UWB. The generated pulse has a rise and fall time of 50 ps, a pulse width of 70 ps, and an amplitude of 2 V on a 50 Ω load with a

random jitter of 3 ps Root-Mean-Square (RMS). The required supply voltage is of 9 V, with a current consumption of 200 mA.

4.2 Implementation of the sequential equivalent time principle

The aim of the reader was to perform UWB chipless RFID tag measurement according to the sequential equivalent time principle summarized in figure 3.3. The FPGA is the controller of the acquisition, it triggers the pulse generator, sets up the value of the delay generator, and memorizes the ADC output. It is controlled by a PC, with a Matlab program in Windows environment, which selects the averaging and retrieves the measured signal in time domain. At the delay generator resolution of 10 ps (ΔT) corresponds an equivalent sampling clock of 100 GSa/s (1/ ΔT). The S/H amplifier is able to sample an UWB input signal and output a constant signal for an entire sampling clock period. It gives the time to the ADC to convert the S/H amplifier output in digital symbols. The trigger event of the pulse generator is synchronized with the sampling clock of the S/H amplifier, at the input of the delay generator. It means that during the acquisition process the delay generator internal delay is varying with step of ΔT, as shown in figure 3.3, to accomplish with the sequential equivalent time principle. Indeed the delay between the pulse generator trigger event and the S/H amplifier sampling clock, have to vary with step of ΔT.

The application software for the PC was written in Matlab, and is based on different scripts called by the Graphical User Interface (GUI). It expects the execution of a tag measurement according with the background subtraction technique. The GUI was designed to read the frequency coded tag presented in [VEN 13], based on coupled short-dipoles with REP and cross-polarization approach shown in figure 3.1. The tag was characterized in chapter 1 section 3, and shown in figure 1.10. The Matlab program uses a Fast Fourier Transform (FFT) approach to retrieve the tag ID. The Matlab GUI is described more in detail in Appendix II.

This first fully working reader version demonstrated the feasibility of the project, where no optimizations were taken into account. Reading of tag with the same antenna Satimo QH2000 were accomplished, and the reader was able to decode the tag information until 5 GHz, which corresponds to the first four resonant frequencies over eight. In table 3.1 are shown the main characteristics of the reader.

Reader retail cost after tax	
Component	**Retail Cost after tax (2013)**
LNA (Miteq AMF-4D-00101200-34-13P)	2,619 €
S/H amplifier (Inphi 1321TH E.B.)	1,469 €
Realized board components	≈200 €
Digital board (Xilinx SP601 E.B.)	350 €
Pulse generator (Hyperlabs HL9200)	1,000 €
Total cost	5,638 €
Reading performance	
PRF	1.04 MHz
Input bandwidth	0.1 – 12 GHz
Acquisition frame duration	120 ns
Frame position	Fixed
Equivalent sampling period (ΔT)	10 ps
Averaging	[1 – 128]
Reading time	≈ 12.3 s + Averaging factor × 0.5 s
S/H Amplifier sampling clock period jitter	13.22 ps RMS (115.67 ps p-p) over 1k cycles

Table 3.1. *Components retail cost after tax of the fully working designed reader during the project Gravit (not considering the antenna), and performance specification.*

The reader most expensive components is the LNA with its 2,619 €, after the S/H amplifier and the pulse generator. The reader input bandwidth is between 0.1 and 12 GHz, and the PRF of 1.04 MHz. The acquisition frame position is fixed, and the acquisition equivalent sampling period of 10 ps (ΔT). The reading time is of 12.3 s plus 0.5 s multiplied for the averaging factor, which maximum is of 128.

From figure 3.3, if the sampling clock is affected by random jitter, the acquisition will be affected by sampling noise. The power of the generated sampling noise increases with the reading signal frequency [GEN 08], therefore its reduction in UWB chipless RFID reader is essential. From table 3.1, the reader S/H amplifier sampling clock has a random period jitter over 1,000 cycles of 13.22 ps as standard deviation (RMS), and a maximum peak to peak of 115.67 ps. The first reader version realized in this thesis is described in the rest of the chapter.

5. Integrated reader designed

In this section the first reader designed during the thesis is presented. It is composed of three main parts: an RF front-end board, the same Xilinx SP601 evaluation board for the digital section, and the same pulse generator for the emission part. The reader has identical frame length, equivalent sampling period (ΔT), and maximum averaging factor as the previous version (see table 3.1). The main ameliorations are represented by the reduction of the reader realization cost, and the improvement of the reading acquisition. The former was obtained with the integration of a low cost LNA and the S/H amplifier on a unique RF Front-end board. A significant work has been done on the S/H amplifier and ADC connections, and a substantial reduction of sampling clock random period jitter has been obtained.

5.1 Hardware architecture

The reader block schematic is shown in figure 3.6, and is invariant with respect to the previous reader version (see figure 3.4). The reader sampling clock was of 67 MHz and the PRF of about 1 MHz. Comparing the figure 3.5 with figure 3.6 the new version is a more integrated solution, this in order to reduce the reader realization cost and overall reader dimensions.

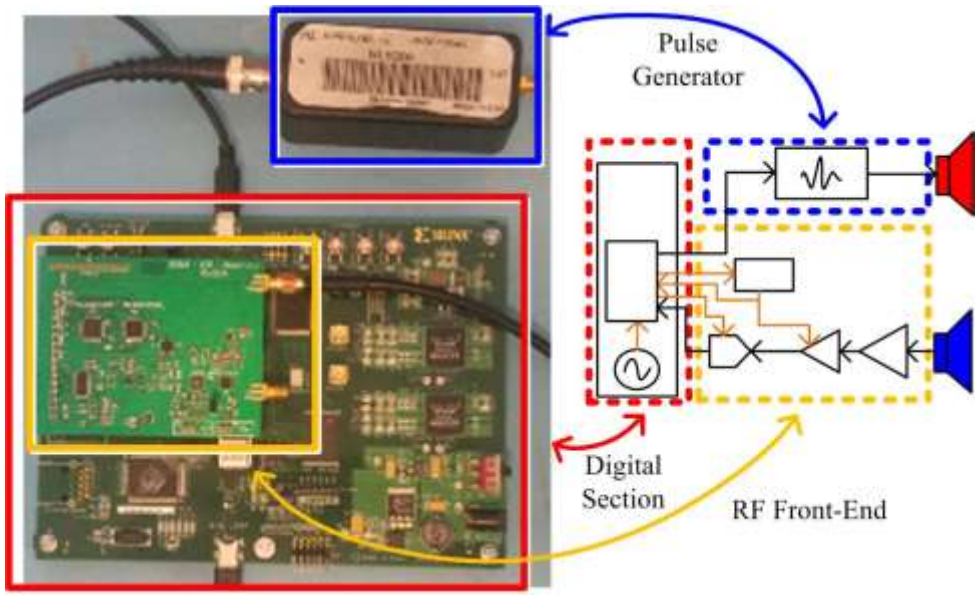


Figure 3.6. *Photograph of the reader. The pulse generator was the HL9200 from Hyperlabs. The digital section is enclosed in a Xilinx SP601 evaluation board for the FPGA Spartan 6 XC6SLX16. The four layers RF front-end board is realized on FR-4 substrate.*

The more performing LNA Miteq AMF-4D-00101200-34-13P was substituted with the HMC754LP4E from Analog Devices. It works in the band 1-11 GHz, and has a gain of 16.5 dB at 6 GHz and of 14 dB at 4 GHz. The noise figure is of 1.5 dB at 4 GHz, and the output compression point is of 18 dBm between 1 to 6 GHz. The AMF-4D-00101200-34-13P costs about 2,619 € (2013), whereas the HMC754LP4E cost is retained inside the 100 € limit. The component integration work was carefully executed to improve as much as possible the reader SNR. This consisted in the use of different components, such as the driver AD4930, the optimization of the RF front-end schematic and layout, and a better implementation of the reader FPGA architecture.

The RF reader front-end board has two SMA connectors, one for triggering the pulse generator, and the other as input for the external UWB receiving antenna. A more detailed photograph of the RF front-end is shown in figure 3.7. The board was realized on four layers with FR-4 substrate, and measures 88 mm × 70 mm (L × H).

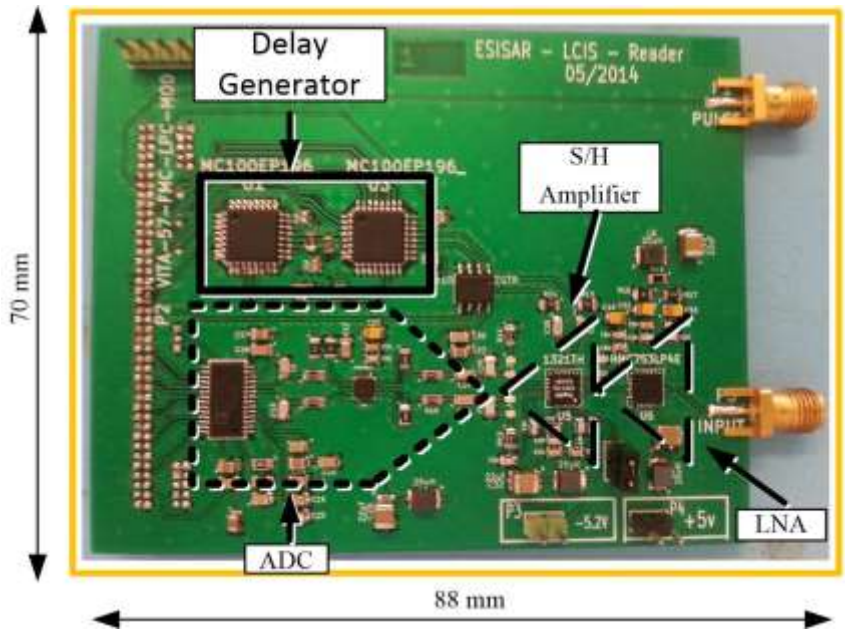


Figure 3.7. *Photograph of the realized RF front-end of the reader in figure 3.6. It is a 4 layers board on a FR4 substrate and measures 88 mm × 70 mm (L × H).*

According to the previous reader version, the delay generator was realized with two MC100EP196 chips connected in series. The input of the first chip is the sampling clock to be delayed (see figure 3.4), and is sourced directly from the FPGA. For both chips the digital control bus, for setting up the delay value, is connected with the FPGA. The output sampling

clock signal of the second chip is connected directly with the sampling clock input of the S/H amplifier, and with the FPGA (see Figure 3.4). To improve signal common noise rejection, the sampling clock connection between the FPGA and the delay generator, and that one between the delay generator and the S/H amplifier are made of balanced signals based on the digital standard Positive Emitter Coupled Logic (PECL). A converter PECL-TTL was employed to have trace of the sampling clock at the output of the delay generator inside the FPGA.

The S/H amplifier input can be an UWB signal, and it is sampled with a sampling clock that in this case is of only 67 MHz (sampling clock). The S/H amplifier varies its output only at the sampling clock event that occur each 15 ns (about 1/67 MHz). It gives the time at the following ADC to convert this low frequency signal, as shown in figure 3.8. The ADC was the low cost AD9215 from Analog Devices, also used in the previous version, which has a vertical resolution of 10 bits. The LNA has a single input/output mode, while the input of the sampler can be driven both in single and differential mode. No balun was employed to convert the LNA output to differential. Actually it is difficult to find commercial available balun that can cover all the UWB between 3.1 and 10.6 GHz, and be at the same time cheap and small in size.

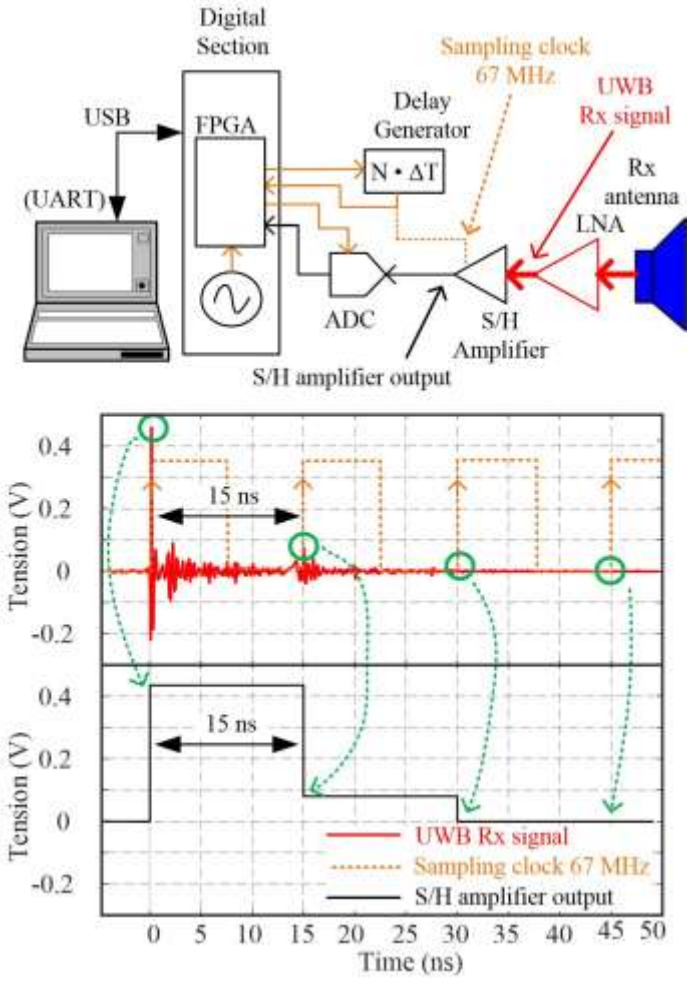


Figure 3.8. *S/H amplifier principle of operation. An UWB input signal (UWB Rx signal) is sampled with a low frequency clock signal (Sampling clock 67 MHz). Thus, its output (S/H amplifier output) is a lower frequency content signal.*

5.2 S/H amplifier - ADC connection improvement

The proper interconnection between the S/H amplifier and the ADC input was a subject of study. Its schematic for the previous reader version of figure 3.5 is shown in figure 3.9. The differential output of the S/H amplifier has an equivalent impedance of 100 Ω, and a dynamic of 1 V_{P-P}. The input impedance of the ADC has a differential resistance of 7 kΩ, and each pin a capacitance referred to the ground of 2 pF. The ADC input needs to have a common voltage of about 1.5 V to work at the maximum performance, which represents half of its analog supply voltage. Thus, the output of the sampler and the input of the ADC must not be connected directly.

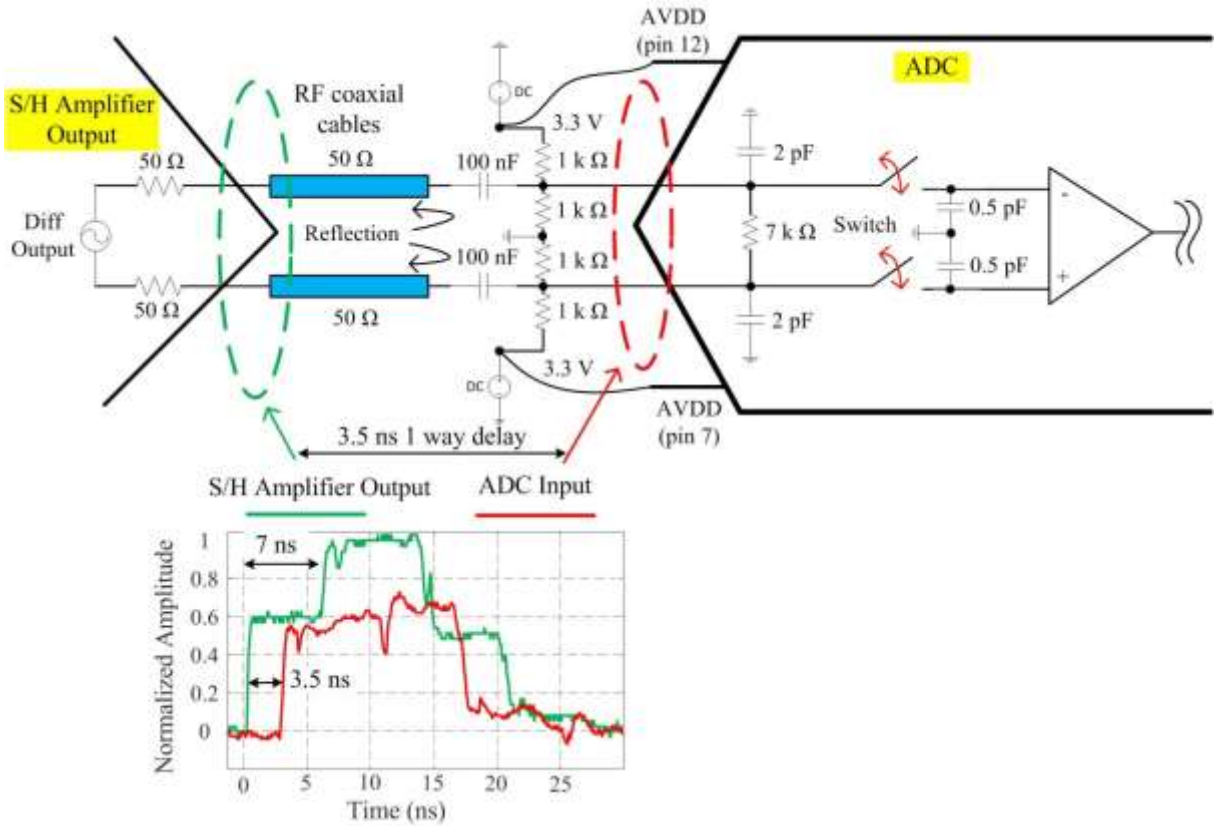


Figure 3.9. *Schematic of the S/H amplifier and ADC interconnection of the first reader version of figure 3.5. The mismatching at the ADC input pins creates important reflections toward the S/H amplifier output, as shown with the plotted curves. The S/H amplifier and the ADC were in two different boards therefore RF coaxial cables were used for their interconnections. The delay between the S/H amplifier output and ADC input was of 3.5 ns. The reader sampling clock period was of 15 ns.*

From figure 3.9, the S/H amplifier and the ADC were located in two distinct boards, therefore RF coaxial cables were used for they interconnections. The sampler and the ADC are AC coupled with two capacitors of 100 nF, and the common voltage of the ADC input is settled with a voltage divider using two resistances of 1 kΩ. This solution is straightforward but has some inconvenient. The voltage divider connects directly the analog supply pins (AVDD pin 12/7) with the ADC analog input. It may represent a low impedance path towards the input of the ADC for the supply noise. The ADC analog input impedance is varying during the acquisition, depending on its state (sampling or holding state). When in sampling state, its analog input impedance decreases because the two switches (see figure 3.9) become closed. It will force output of the sampler to drive the analog input of the ADC. Finally, the output of the sampler is not closed to a proper differential resistance of 100 Ω, creating an impedance mismatching. Its negative effects are underlined in figure 3.9 with the measurement of the sampler output on its evaluation board, and the input of the ADC. From

figure 3.8, the sampler output is expected to be a step signal with interval of about 15 ns, equals to the reader sampling period (1/67 MHz). Instead in figure 3.9, the signal appears not constant with higher interval of about 22 ns. This was caused by the reflected signal, at the aforementioned mismatching, where the two way propagation delay is of about 7 ns (RF coaxial cables, PCB layout and components). It can be seen as the sum of two equals signal of the duration of 15 ns (sampling clock), delayed of 7 ns.

In the new reader version the S/H amplifier, and the ADC are on the same RF front–end board (figure 3.7). To improve the performance of their interconnection, a driver AD4930 from Analog Devices was used. It is a differential amplifier designed to be interfaced with ADC from the same maker. The simplified schematic of the implemented solution is shown in figure 3.10. The driver input pin called V_{OCM} settles the driver output common mode voltage, and with the external two resistors called *Rf*, it is possible to configure a differential gain.

The two capacitors of 10 ps at the output of the S/H amplifier pins, and the two at the ADC analog inputs pins, are used to improve the AD4930 robustness against instability. The sampler output is perfectly matched, and does not need to drive the ADC input in sampling state. The use of the driver also decreases the effect of supply noise at the ADC input [ADA 17]. An evaluation board was realized on FR-4 to study the driver effects on signal acquisition. It is also shown in figure 3.10, and the dimensions of the board are 110 mm × 100 mm (L × H). In the next section the reader FPGA implementation will be detailed.

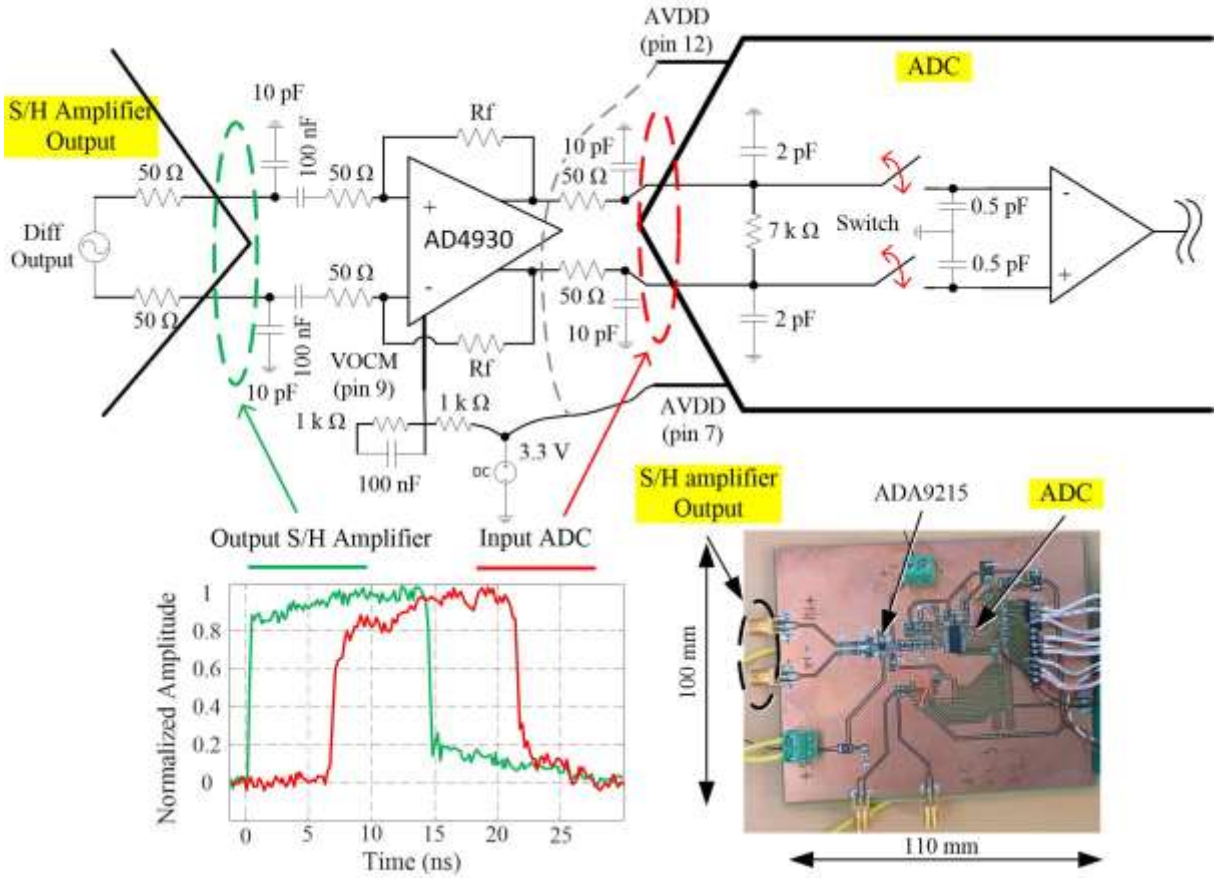


Figure 3.10. *Schematic of the S/H amplifier and ADC interconnection in the newer reader version. The use of the driver AD4930 helped to reduce impedance mismatching, and increases supply noise rejection. An evaluation board was realized.*

5.3. FPGA architecture

The RF front-end is controlled by the digital board SP601 through the FPGA hardware architecture. An FPGA device gives flexibility and also rapidity, fast dedicated hardware blocks can be synthetized with VHSIC Hardware Description Language (VHDL) scripts. In the proposing reader, the FPGA implements a microprocessor based embedded system with the soft-core Microblaze processor version 8.20.a. It is connected to different peripherals, some internal at the chip, and other external such as Double Data Rate 2 (DDR2) memory, Universal Asynchronous Receiver Transmitter (UART), push button, and leds. Between the internal peripherals there are a clock synthesizer, an interrupt controller, and the most important, a custom peripheral called Reader_0. The block Reader_0 was described with VHDL, and is the solely that communicates with the RF front-end. In turn, it is set up by the microprocessor that gives information about the selected averaging. Inside the Reader_0

block is also present a First Input First Output (FIFO) memory to acquire the output of the ADC.

The block schematic of the FPGA embedded system, with the main peripherals of the digital board SP601 used to implement the reader, is shown in figure 3.11. The Xilinx ISE Design Suite 13.2 was used to design, simulate, and debag the FPGA architecture. The suite offers many applications that ease the development process. Between them the ISE Design Tool that is most indicated to implement custom hardware blocks. The Platform Studio to create the real microprocessor embedded system, with the addition of all blocks immediately ready from Xilinx, and Software Development Kit for software development and debugging. Inside the FPGA Spartan 6 XC5SLX16, the Microblaze is connected with local dual ports Block Random Access Memory (BRAM) of 32 kB with two fast Local Memory Bus (LMB), one for data and the other one for instructions, realizing a Harvard memory architecture. Two LMB-BRAM interface controllers are needed to connect the Microblaze with the local BRAM.

A Processor Local Bus (PLB) 4.6 is used to connect the microprocessor with the rest of peripherals, at exception of the clock generator. The PLB provides a bus control unit, a watchdog timer, and separate address, write, and read data path. All the peripherals connected with the Microblaze are accessed with memory mapped, where the address range for LMB and PLB must not overlap.

The LEDs 4 bit GPIO (General Purpose Input/Output) is the interface between the PLB and GPIO to turn on and off 4 leds. They are useful to understand the status of operation of the reader, and also during software debugging. The RS232 uartlite block is able to connect a PLB bus interface with an external device equipped with UART. In this project, it was used to interface the microprocessor with the external PC. The chip CP2103 from Silicon Labs resides on the SP601 board, and is able to interface the Universal Serial Bus (USB) up to version 2.0, with a UART device. All the application software on the PC were developed for the Microsoft operative systems, and work with existing COM port PC applications. The communication with the PC has a Baud Rate (BR) of 460.800 kb/s, with 8 bits for each data frame, and without parity bit. The Spartan 6 presents limited resources in term of available memory, therefore the use of an external memory is somehow necessary. The external DDR2 of 1 Gb is used as principal memory where the application software resides. The interface MCB_DDR2 can connect the DDR2 memory with the PLB bus. This solution is not

optimal for speed, the PLB is not accounted as fast bus, but for this prototype version of the reader the optimization of reading time was not a priority.

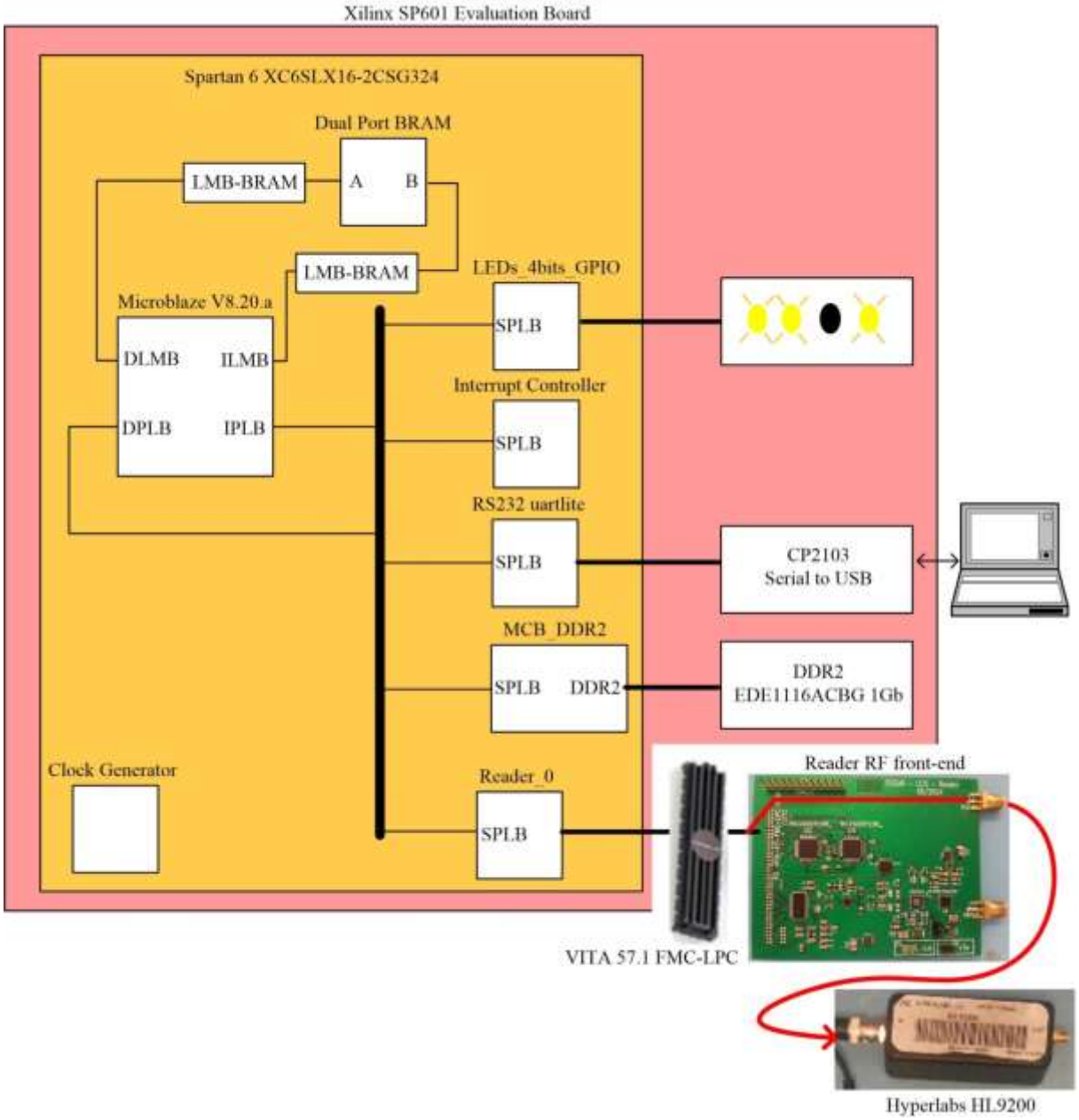


Figure 3.11. *Block schematic of the FPGA embedded system, with the main peripherals of the digital board SP601 used to implement the reader. The custom block Reader_0 is the solely that can communicate with the analog board and trigger the pulse generator.*

The Reader_0 is the custom block developed with ISE Design Tool. It communicates directly with the analog board and also is responsible for triggering the pulse generator. It contains a FIFO memory, which is directly connected with the output of the ADC, a main control unit,

some blocks for synchronization purposes, and a PLB slave interface. The Reader_0 memorizes the ADC output, sets up the internal delay of the delay generator chips, and triggers the pulse generator. A more in depth description of the Reader_0 block is given in Appendix III.

The clock generator exploits the Spartan 6 clock resources, as Phase-Locked Loop (PLL) and Digital Clock Manager (DCM), available inside the Clock Management Tiles (CMTs) to generate different clock signals for the available interfaces. According to the developed project, the FPGA external chip clock input was the on board 200 MHz crystal oscillator SiT9102AI-243N25E200.00000 from SiTimes. From the 200 MHz input, using the clock generator block, a 67 MHz clock and two opposite in phase of 600 MHz clocks were created. The higher were used for the external DDR2 memory and the internal controller MCB_DDR2, the lower for all the rest of components including the block Reader_0. The interrupt controller is able to concentrate multiple interrupt inputs into one single interrupt output. It is interfaced with a PLB slave interface, and presents one output directly connected with the microprocessor interrupt input. The use of an interrupt controller free up the microprocessor from pulling operation.

5.4. Reader specification

The costs and performance of the advanced reader are resumed in table 3.2. Respect with the previous version, it shows a halved retail component cost, from 5,638 € to 2,350 €, and a halved sampling clock period jitter. The latter was obtained by working on the FPGA implementation, with proper utilization of internal intellectual property (IP) such as PLL and delay-locked loop (DLL) [XIL 15a], and with I/O dedicated resources [XIL 15b]. Also the connection between the delay generator chips and S/H amplifier were improved using proper components. Finally the layout design also played an important role. Besides all the ameliorations provided with this reader version, some issues with signal synchronization were still present, as for the previous reader version. They are faced in the developments described in the next chapter.

Reader retail cost after tax	
Component	**Retail Cost after tax (2013*/2014**)**
S/H amplifier (Inphi 1321TH E.B.)	800 € **
Realized board components	≈200 € **
Digital board (Xilinx SP601 E.B.)	350 € *
Pulse generator (Hyperlabs HL9200)	1,000 € *
Total cost	2,350 €
Reading performance	
PRF	1 MHz
Input bandwidth	1 – 11 GHz
Acquisition frame duration	120 ns
Frame position	Fixed
Equivalent sampling period (ΔT)	10 ps
Averaging	[1 – 128]
Reading time	≈ 12.3 s + Averaging factor × 0.5 s
S/H Amplifier sampling clock period jitter	7.34 ps RMS (67.37 ps p-p) over 10k cycles

Table 3.2. *Components retail cost after tax of the presenting fully working designed reader (not considering the antenna) and performance specification.*

6. Tag measurement result

The reader described here was tested using the frequency-coded tag introduced in [VEN 13], and shown in figure 3.12. The two tags have different resonant frequency positions in the bandwidth 3 – 7 GHz. The second tag has the first seven resonant frequencies respectively shifted of 100 MHz in direction of higher frequency (right), while 200 MHz for the eighth. The two tags were first measured in turn in an anechoic chamber with the test equipment of figure 3.1, and after with the proposing reader. The tags were placed at 15 cm from the antenna on a foam support. The dual-access dual polarization Satimo QH2000 antenna, and the dual measurement procedure (background subtraction) were employed, as for section 2. The reference measurement system (test equipment) used the pulse generator HL9200, (the same as in the proposing reader in transmission). In reception, the DSO Agilent 91204A is used as shown in figure 3.1. The measurement bench is shown in figure 3.12.

The measurement results for both test benches in time domain, of the tag 1 and 2, are shown respectively in figure 3.13 (a) and (b). The measurements were executed with an averaging factor of 128 for the reader, and of 64 for the DSO. A calibration process was previously executed to take into account the real delay of the reader delay generator. In fact it is composed of 2 chips in series and the speculation of a tunable delay at an exact step of

10 ps (ΔT) was pretentious. The calibration process was based on a comparison between known measured signals with the DSO and the reader. The calibration results show a ΔT variation between 9 and 11 ps depending on the set up delay of the delay generator.

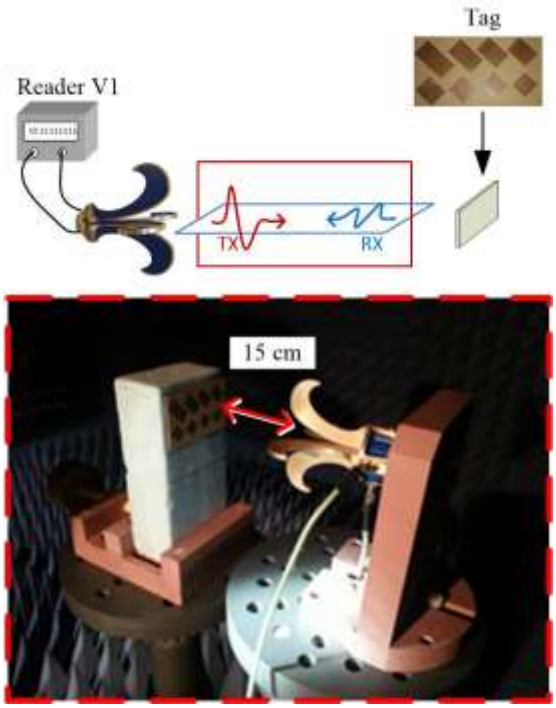


Figure 3.12. *Measurement bench specified to the antennas-tag configuration where the cross-polarization principle was used. The two tags were placed in turn at 15 cm of distance, and measured with a test bench based on a high performance DSO first, and after with the proposing reader.*

The measurements of figure 3.13 represent the tag measurement at which the background measurement was not yet subtracted. The higher voltage contribution at around 1 ns represents the leakage between the antenna ports. It represents the permanent contribution at the reader measurements.

In figure 3.14 (a) is shown the measurement results in frequency domain of tag 1, and in (b) of tag 2, after post processing. In case of tag 1 the proposed reader shows correct measurement for all the resonant frequencies, where the DSO peaks positions coincide with the reader results. While for tag 2, the reader did not decode correctly the information carried on by the sixth and seventh peak. It is worth to note that even if the DSO located correctly the position of these two peaks, a decoding uncertainty is introduced due to the presence of a closer resonance with considerable power.

The obstruction of reading the higher frequency resonances from both test benches could have been outdid reducing the tag distance of few centimeters. In addition, the pulse generator Hyperlabs HL9200 has lower power at higher frequencies as shown in figure 3.15 (b) where the PRF was of 1 MHz. Its response in time domain on a 50 Ω load is shown in figure 3.15 (a).

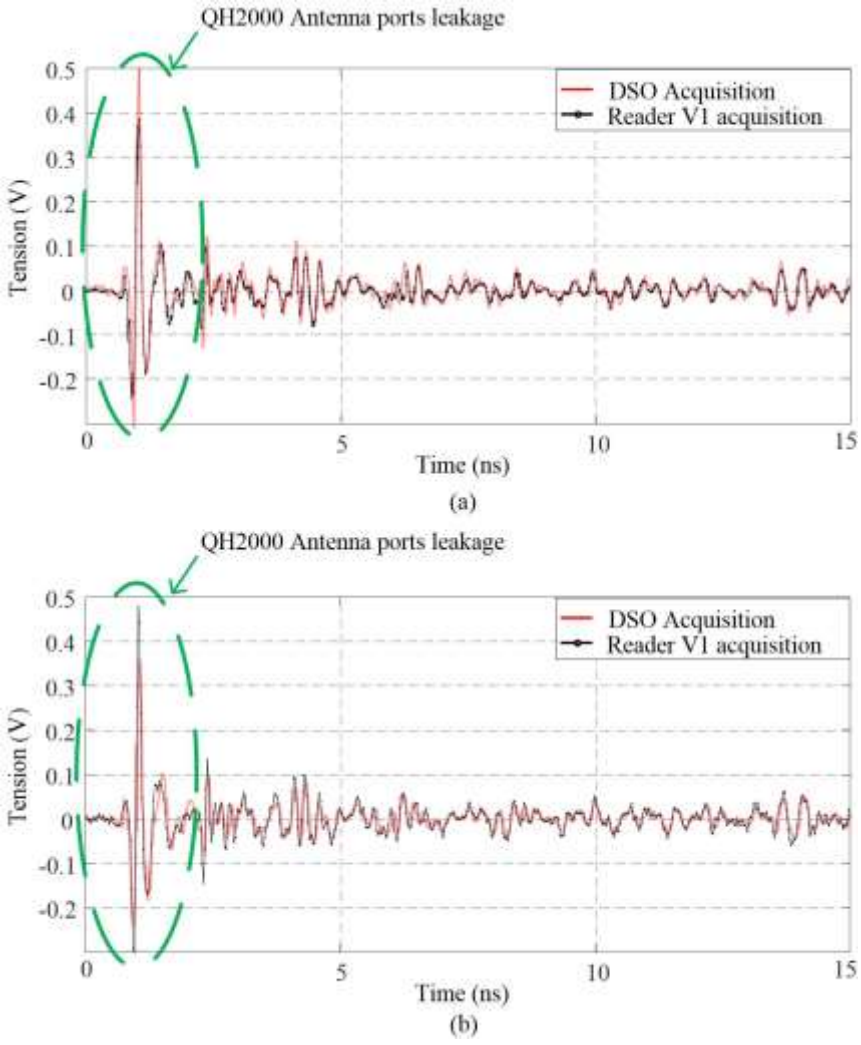


Figure 3.13. *Measurement results in time domain of chipless tag responses (the corresponding measurement bench is shown Fig. 3.13). The DSO measurements were executed with an averaging of 64. The proposing reader measurements were executed with an averaging of 128. (a) Tag 1. (b) Tag 2.*

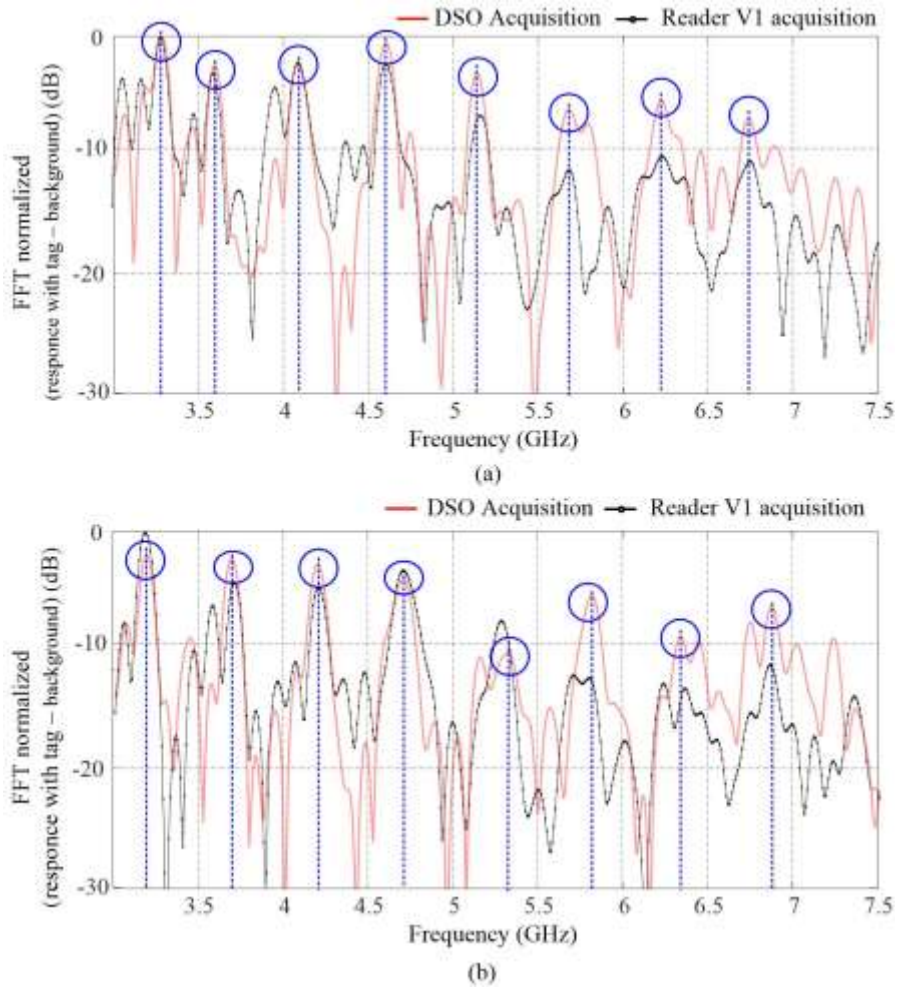


Figure 3.14. *Measurement results in frequency domain of tag responses. (a) Tag 1. (b) Tag 2.*

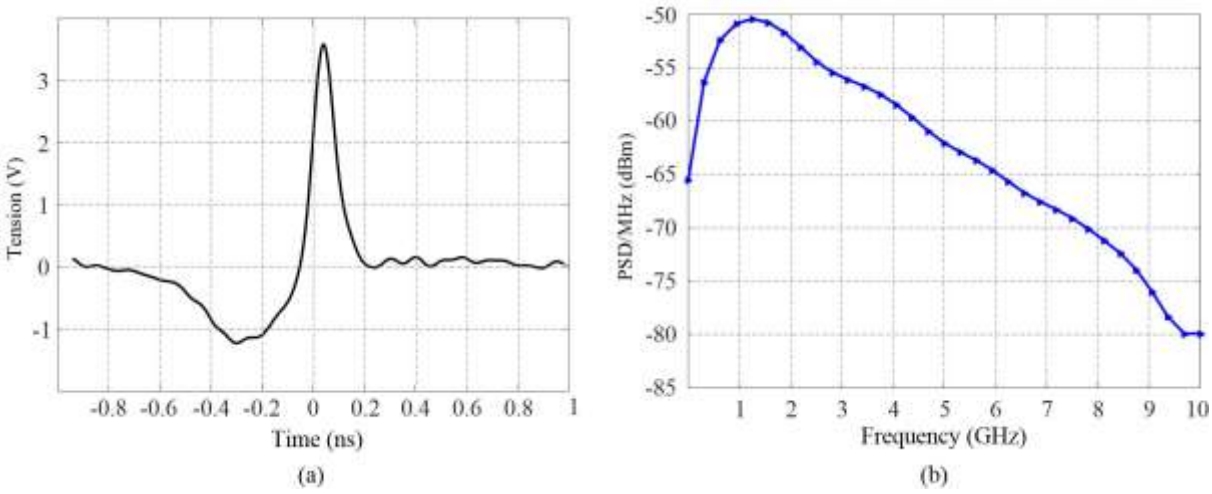


Figure 3.15. *Pulse generator Hyperlabs HL9200 measurement with the DSO in time domain (a), and frequency domain with a PRF of 1 MHz (b).*

7. Conclusion

In this chapter a chipless RFID reader based on IR-UWB approach was presented. It exploits the flexibility of a FPGA with its evaluation board to reduce the reader hardware complexity design. It has a reading time in order of several seconds, strongly depending on the averaging factor. The reader was validated in anechoic chamber with measurements of two frequency coded tags at a distance of 15 cm.

The acquisition suffers from synchronization issues inside the FPGA, which will be faced in the next chapter with the presentation of a second reader version. Several aspects will be optimized such as the reading flexibility (acquisition frame duration, frame position, equivalent sampling period ΔT, averaging), the reading time, and the sampling clock period jitter. The latter aspect is one the main characteristics that needs to be optimized to improve the reading performance.

8 References

[ADA 17] ANALOG DEVICES, ADA4930-1 data sheet, online available at: www.analog.com.

[GEN 08] GENG Z., SIMROCK S.N., “Evaluation of fast ADCs for direct sampling RF field detection for the European XFEL and ILC,” *in 24th Linear Accelerator Conference LINAC08*, Victoria, Canada, Sept. 2008.

[XIL 15a] XILINX, “Spartan-6 FPGA Clocking Resources User Guide UG382 (v1.10),” 2015, online available at: www.xilinx.com.

[XIL 15b] XILINX, “Spartan-6 FPGA SelectIO Resources User Guide UG381 (v1.7),” 2015, online available at: www.xilinx.com.

[VEN 13] VENA A., PERRET E., TEDJINI S., "A Depolarizing Chipless RFID Tag for Robust Detection and Its FCC Compliant UWB Reading System," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 8, pp. 2982-2994, Aug. 2013.

[VEN 14] VENA A., PERRET E., SORLI B., et. al., ”Study on the detection reliability of chipless RFID systems,” in *XXXIth URSI General Assembly and Scientific Symposium (URSI GASS)*, Beijing, China, 2014.

4

Optimized IR-UWB Chipless RFID Reader

1. Introduction

In this chapter an optimized IR-UWB Chipless RFID reader is presented. Compared with the reader version of the previous chapter, its major progresses are represented by the reduction of the reading time, with a factor of around 1,000, and the reduction of sampling noise. It also offers flexibility in term of reading settings, such as acquisition frame position, length, and equivalent sampling rate.

In the first part, a theoretical introduction to sampling noise and quantization noise is given. In the second part, the reader hardware architecture is described more in detail, focusing on the characteristics that improved the reader performance. To facilitate the understanding of the chapter, some particular hardware and software aspects are in Appendix. Finally, measurements of chipless tags in practical environment are shown. The chapter is organized as follow:

- Section 2 does a theoretical introduction at the ADC sampling and quantization noise.
- Section 3 presents the hardware architecture of the reader, and the reduction of its sampling noise compared with the reader version of chapter 3 is demonstrated.
- Section 4 describes the reader FPGA architecture focusing on the techniques employed to reduce the reader reading time, and to resolve the synchronization issues shown in chapter 3.
- Section 5 gives the specifics of the reader.
- Section 6 presents the realized reader power supply board

- Section 7 shows some frequency-coded tag measurements.
- Section 8 compares the reading accuracy of a frequency based reader, with an IR-UWB based reader supposed affected by different levels of jitter.
- Section 9 draws the conclusion of the chapter

2. ADC noise theory

The reader proposed in chapter 3 has an AD conversion block composed of a UWB S/H amplifier followed by a driver and a low cost ADC. The AD conversion block may be seen as a unique ADC presenting at its input an UWB signal. The ADC block of a UWB chipless RFID reader may either have a low frequency signal as input in the case a frequency based approach (see chapter 2) or an UWB signal for the IR-UWB approach.

All the analog to digital conversion processes degrade the SNR ratio at its input. There are different sources of noise that may play a major or a minor role, depending of the ADC characteristics and also of the input signal in terms of voltage range and frequency contents. An ADC can be seen as a S/H amplifier in series with a quantizer as shown in figure 4.1. The S/H amplifier is responsible of the sampling in time domain of the analog input and it is ideally composed of a switch controlled by a clock, and a capacitor to follow the input signal voltage. The switch commutes according to the clock events, rising and falling edges. It closes when falling events occur, and opens with rising events. When the switch is closed, the capacitor follows the analog input signal. At the rising clock event (sampling), the switch opens and the capacitor is in memory state. The tension of the capacitor is constant (holding) until the switch is closed again. During the memory state (holding), the capacitor value is converted in digital symbols by the quantizer, which input/output characteristic can be represented with a stare case function (see figure 4.1).

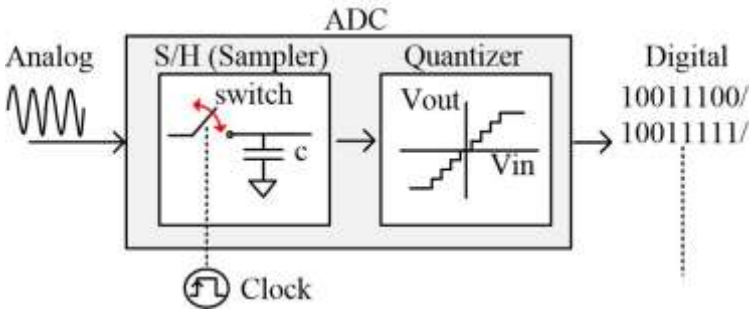


Figure 4.1. *ADC block schematic. It is composed of a S/H amplifier in series with a quantizer. The former is responsible of the sampling noise, and the latter of the quantization noise.*

The output of the ADC has a SNR lower compared to its input. It is most due to the error introduced by the sampling and quantization processes. The sampling process adds sampling noise, which is correlated with the jitter of the sampling clock and the ADC aperture time uncertainty. The quantization process presents a quantizer with a non-linear input/output characteristic, and therefore introduces higher order noise referred with the term quantization noise. In case of frequency based chipless RFID reader, the useful ADC input signal is almost DC and the SNR is most influenced by the quantization effects. An ideal ADC with a staircase quantizer has a maximum SNR output limited to,

$$SNR\ (dB) = 6.02N_{ADC} + 1.76\ dB, \qquad [4.1]$$

where N_{ADC} is the resolution (number of bit) of the ADC. The equation [4.1] assumes: a sinusoidal input signal with an excursion equal to the full-scale ADC input, the ADC clock and the sinusoidal input period with an irrational ratio, and the clock frequency around the Nyquist rate [BEN 48]. The SNR of an ADC can be improved by increasing N_{ADC} (equation [4.1]), and by exploiting techniques such as oversampling and digital filter implementations. In the case of the UWB chipless RFID based on IR-UWB, the ADC input signal is wideband and composed of the coupling between the transmitting and the receiving antennas, and the structural and the antenna (tag) mode. The tag ID is in the tag mode frame for a frequency-coded tag, which is the least powerful part of the ADC input signal. Thus, to reduce the quantization noise referred to the antenna (tag) mode, it is important to select an ADC with a large number of bits and to amplify the antenna (tag) mode ideally to match it with the ADC input full scale range.

The sampling noise depends from the ADC hardware characteristics, the ADC sampling clock jitter, and the ADC input frequency contents. If the input of the ADC is a low frequency signal, then the sampling noise may be negligible. This is the case of the frequency based chipless reader. For an IR-UWB chipless reader approach, the sampling noise can be important because the ADC input is not a low frequency signal anymore. For simplicity, we consider a sinusoidal ADC input, which is the result of the following stationary process,

$$V_{IN}(t) = \sin(\omega t + \phi). \quad [4.2]$$

Where ϕ is a random variable uniformly distributed between [-π, π]. This process is parametric, stationary and ergodic. Once went through the S/H amplifier of the ADC (see figure 4.1), the process becomes,

$$V(k) = \sin(\omega(Tk + \gamma) + \phi). \quad [4.3]$$

Where T is the sampling clock period, and from the central limit theorem, γ is a Gaussian random variable with zero-mean, and k is integer. It takes into account the jitter noise of the ADC clock combined with the ADC aperture uncertainty, which generally has the minimum influence. The error $N(k)$ introduced by the γ can be approximated with,

$$N(k) = \cos(\omega(Tk) + \phi)\omega\gamma. \quad [4.4]$$

This process is stationary, indeed the two random variables ϕ and γ are independent, and can be easily demonstrated that their mean values and autocorrelation is invariant with respect to timing translations. The ratio between the power of the processes in equation [4.4] and in equation [4.3] is equal to,

$$SNR = -10\log_{10}(\omega^2\sigma_t^2). \quad [4.5]$$

Where σ_t^2 is the variance of γ, which may be approximated with the variance of the sampling clock jitter. From equation [4.5], the SNR decays 20dB/dec compared with the input signal frequency. In case of the UWB input signal (IR-UWB chipless reader), the SNR has been calculated in [SMI 17] and is equal to,

$$SNR = -10\log_{10}(4\pi^2\sigma_t^2(f_0^2 + \frac{BW^2}{12})). \quad [4.6]$$

Where f_0 is the central frequency of the UWB input signal and BW is its -3dB bandwidth. In case f_0 > 10 BW the bandwidth of the signal can be neglected.

Only the jitter of the ADC sampling clock has been considered in this analysis. In case of an IR-UWB chipless reader, the pulse generator is triggered by a signal, such as a low frequency clock, which is also affected by a jitter. If its jitter is uncorrelated with that one of the ADC sampling clock, then its variance can be summed to σ_t^2. This is the case of the reader presented in the last chapter and the current presenting optimized version.

In the last reader version presented in chapter 3, the estimated sampling clock period jitter standard deviation was of about 7.34 ps, while the reader input bandwidth between 1 and 11 GHz. Substituting these values into equation [4.6], we obtain a SNR of 10 dB. With respect to the first reader version realized before the kick-off of this thesis, the sampling clock jitter was even bigger and of about 13.22 ps. This standard deviation gives a SNR of about 5 dB, note that at this jitter should be added the one of the pulse generator trigger, resulting in an even worst SNR result.

The averaging process helps to increase the SNR but at the expense of a higher reading time. Much care was spent in the design of the presenting optimized reader to ensure an ultra-low jitter. It may be considered as a cheap manner of improving the reader performance. Indeed, the jitter that affects a signal is directly correlated with the signal integrity. It is caused by different sources of noise: power supply variations, thermal noise, interference between nearby circuits, and loading mismatching [MIT 09]. Thereby, the hardware architecture, the layout of the RF front-end acquisition board and the selection of the components may be optimized without an increasing of reader components cost. For the frequency based chipless reader, the error induced by the ADC can be neglected, on the other hand the VCO phase noise reduces the overall reader performance, decreasing its reading frequency resolution.

The presenting reader is introduced in the next section, and the RF front-end board schematic is described along with the solutions employed to reduce the jitter of the S/H amplifier sampling clock, and the jitter of the pulse generator input trigger.

3. Reduced reader jitter: implemented hardware solution

According to equation [4.5], the sampling noise reduction is fundamental to simplify the reading of the tags information at higher frequencies. In this case, a lower reader averaging factor may be used to read the tags to reduce the reading time.

The block schematic of the proposing optimized reader is shown in figure 4.2 and its photograph in figure 4.3. The schematic shows two clocks, one of 73.333 MHz and the other one of 125 MHz. The 125 MHz clock is used as sampling clock for the S/H Amplifier and also as one input of the ultra-low jitter AND gate. To avoid triggering the pulse generator continuously, the other input of the AND is connected to the FPGA in a clock gating configuration. As it can be seen on figure 4.3, the re-designed RF front-end board holds both the 125 MHz clock generator and the AND gate. The FPGA clock was increased from the 67 MHz to 73.333 MHz to speed up the UART communication with the PC as shortly explained in the sub-section 4.1.1.

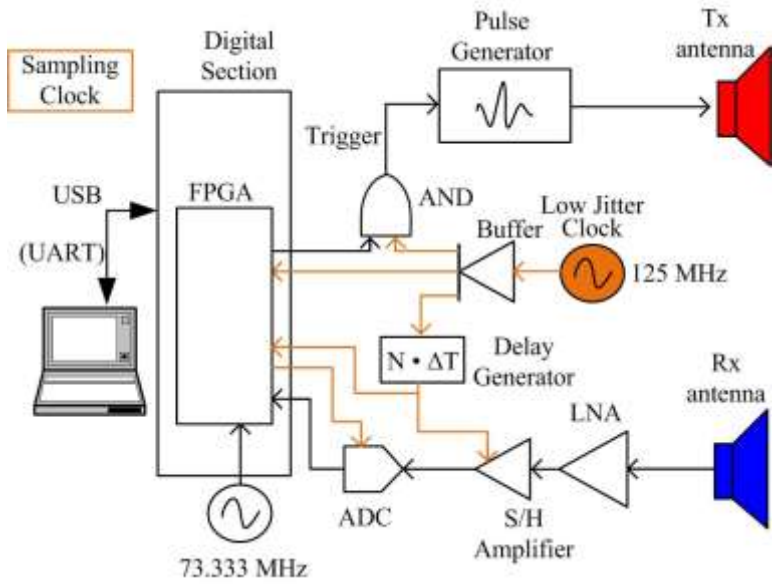


Figure 4.2. *Architecture of the optimized reader. It has a bi-static configuration and it is composed of three parts: an UWB pulse generator, a digital section, and the receiving RF front-end.*

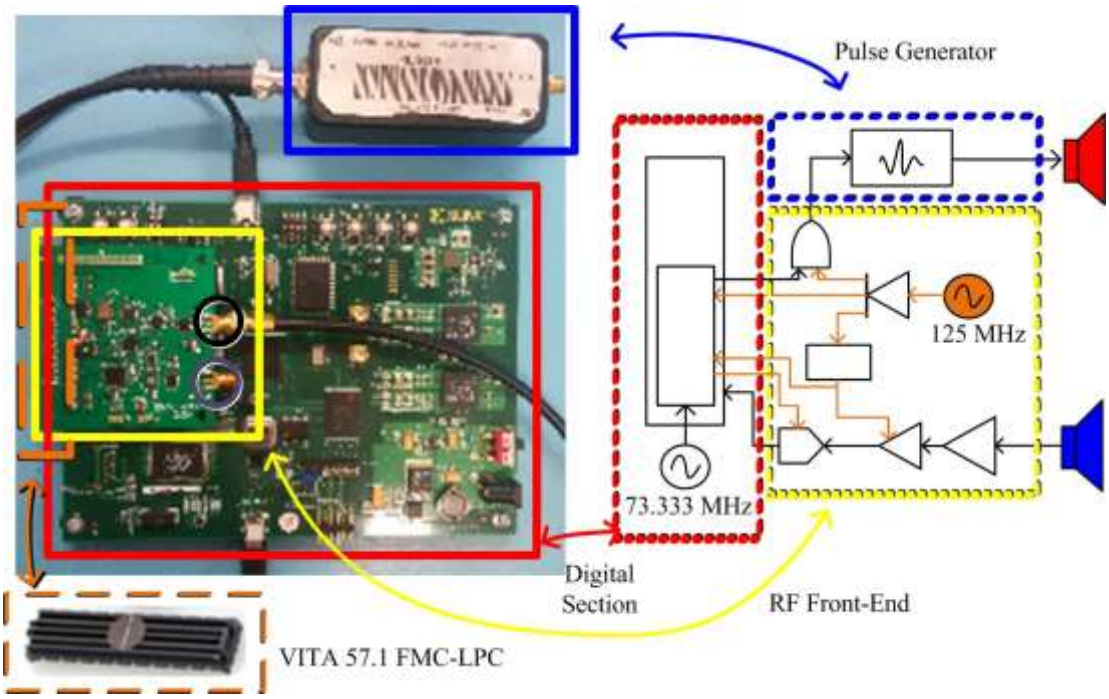


Figure 4.3. *Photograph of the optimized reader. The pulse generator was the HL9200 from Hyperlabs. The digital section is enclosed in a Xilinx SP601 evaluation board for the FPGA Spartan 6 XC6SLX16. The RF front-end board is four layers on FR-4 substrate.*

A photograph of the RF front-end board is shown in figure 4.4 (a), where the main components are underlined. It is a 4 layers board made on a low cost FR4 substrate. Its dimensions are 70 mm × 70 mm. The 125 MHz clock generator is the NBXDPA019 from ON Semiconductor. It is compatible with the PECL digital standard and has a period jitter standard deviation of 2 ps measured over 10 k cycles. The buffer is the CDCLVP2104 eight LVPECL outputs from Texas Instruments. The AND gate is the MC10EP05 from ON Semiconductor, and it has an ultra-low jitter component compatible with both, PECL and NECL (Negative ECL). It has a random clock jitter with a standard deviation of 0.2 ps measured between 1 GHz and 3 GHz state rate variation. The delay generator is the MC100EP196 used also in the first reader version but in a more efficient package, the 32QFN (32 Quad Flat No-leads) instead of the 32LQFP (32 Low profile Quad Flat Package). Because of the new sampling clock of 125 MHz only one chip is needed as delay generator. A single delay generator chip has an internal delay dynamic variation of 10 ns, which is sufficient to cover the 8 ns period of the 125 MHz sampling clock.

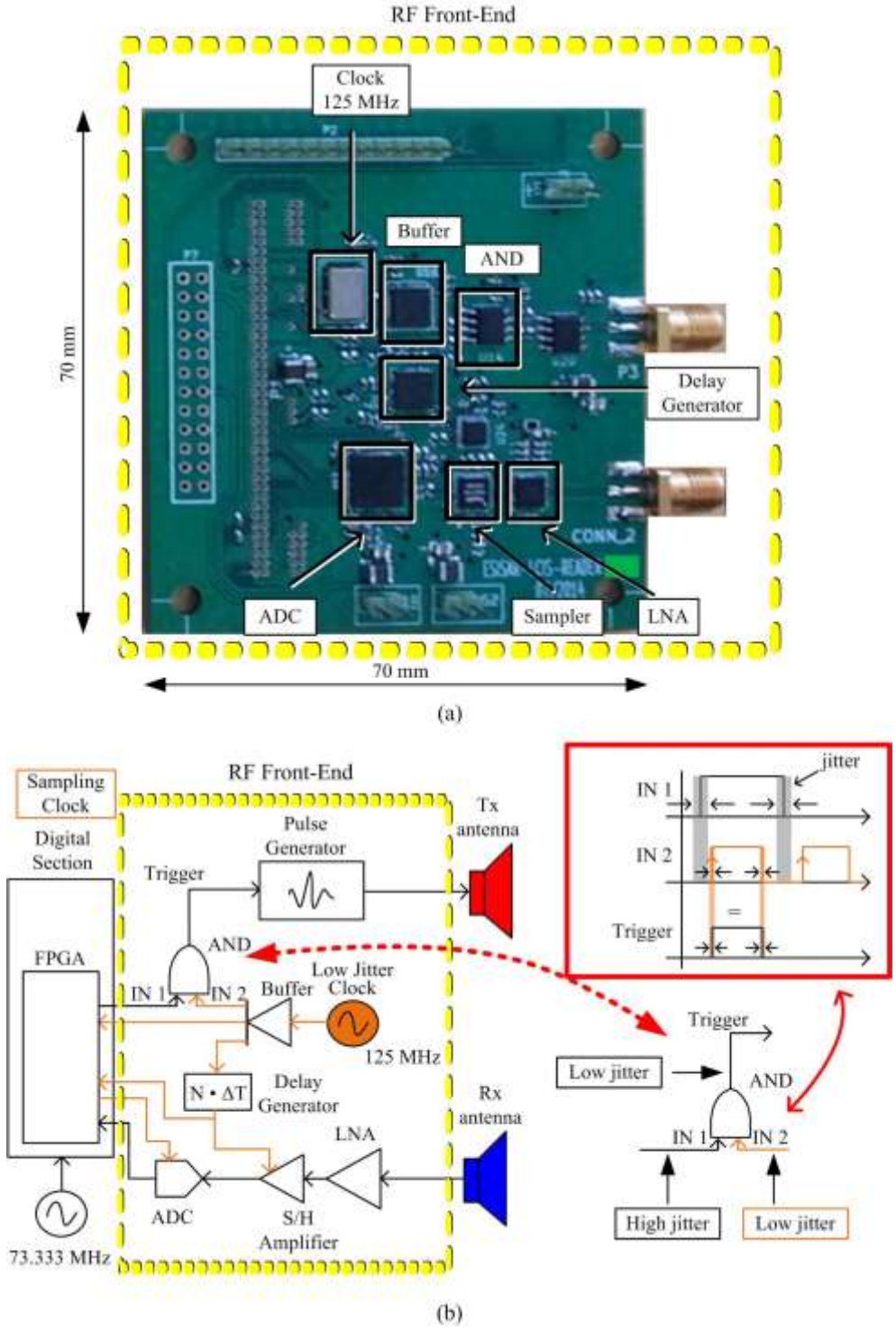


Figure 4.4. *(a) Photograph of the realized analog RF front-end of the optimized reader. It is a 4 layers board on a FR4 substrate, and measures 70 mm × 70 mm. (b) Implemented schematic of the RF front-end board, and AND gate operation.*

The pulse generator trigger input is not compatible with ECL standards, hence a PECL-TTL converter chip was employed after the output of the AND gate. In reception, the LNA (HMC753LP4E) and the S/H amplifier (1321TH) are the same as for the previous reader version, while the ADC is the ADS58B19 from Texas Instruments. It has 9 bit of resolution over 1.5 V_{PP}. It does not need a driver to be interface with the sampler outputs because its differential inputs front-end is composed of two analog buffers, and the common mode voltage is provided directly by the ADC. Thus, the two pins of the sampler output are connected with a resistor of 100 Ω for impedance matching, and are AC coupled with the ADC inputs.

The selected FPGA is low cost and is not designed to provide signals with an extremely low jitter. Moreover the connection between the SP601 evaluation board (digital section) and the designed RF board is made with a VITA 57.1 FMC-LPC connector (see figure 4.3). It is not optimized for RF signal integrity and therefore all those signals generated inside the FPGA, and travelling toward the RF front-end board, have an excessive jitter. This was the case for the previous reader version (chapter 3), with the pulse generator trigger and the S/H amplifier sampling clock signals. In the proposing optimized reader, those two signals are low jitter. This because they are generated directly on the RF front-end board using the 125 MHz clock and the AND gate. The AND gate output is the pulse generator trigger, whereas its input are a high jitter FPGA output called *IN 1,* and the low jitter 125 MHz clock called *IN 2.* The two inputs provide a clock gating configuration. To keep a low jitter AND gate output, it is sufficient to assure the *IN 1* events (rising and falling edges) when the low jitter *IN 2 is stable at* 0_2, as shown in figure 4.4.

The sampling clock period jitter of the S/H amplifier was measured as for the previous reader versions. It has a random period jitter over 1,000 cycles, with 2.45 ps of standard deviation (RMS), and a maximum peak-to-peak of 16.31 ps. It represents a huge improvement compared to the reader versions on chapter 3 (7.34 ps RMS, p-p 67.37 ps). Applying again the equation [4.6] as in paragraph 4.2, at the lower jitter standard deviation of 2.45 ps, a SNR of about 20 dB is obtained. This represents a huge improvement compared with the others reader versions. It was of 10 dB for the reader presented in chapter 3, and 5 dB for the reader version made before the beginning of the thesis. In the next section the reduction of reader sampling noise is demonstrated.

3.1 Temporal characterization of reader RF front-end

To stress the reduction of reader sampling noise, the reader pulse generator output was measured without any averaging, with the previous reader version (chapter three) and with the optimized version. The measurement results for the previous reader version are show in figure 4.5 (a), and in figure 4.5 (b) for the optimized version. Between the pulse output and the RF reader input some attenuators were interposed to avoid the reader front-end saturation. The same measurement performed with the high performance DSO Agilent 91204A is shown in red. The measurement in figure 4.5 (a) demonstrates a higher sampling noise than the figure 4.5 (b), especially in the pulse rise and fall edges (higher slew-rate). This is due to the jitter of the S/H sampling clock, and that of the pulse generator trigger input.

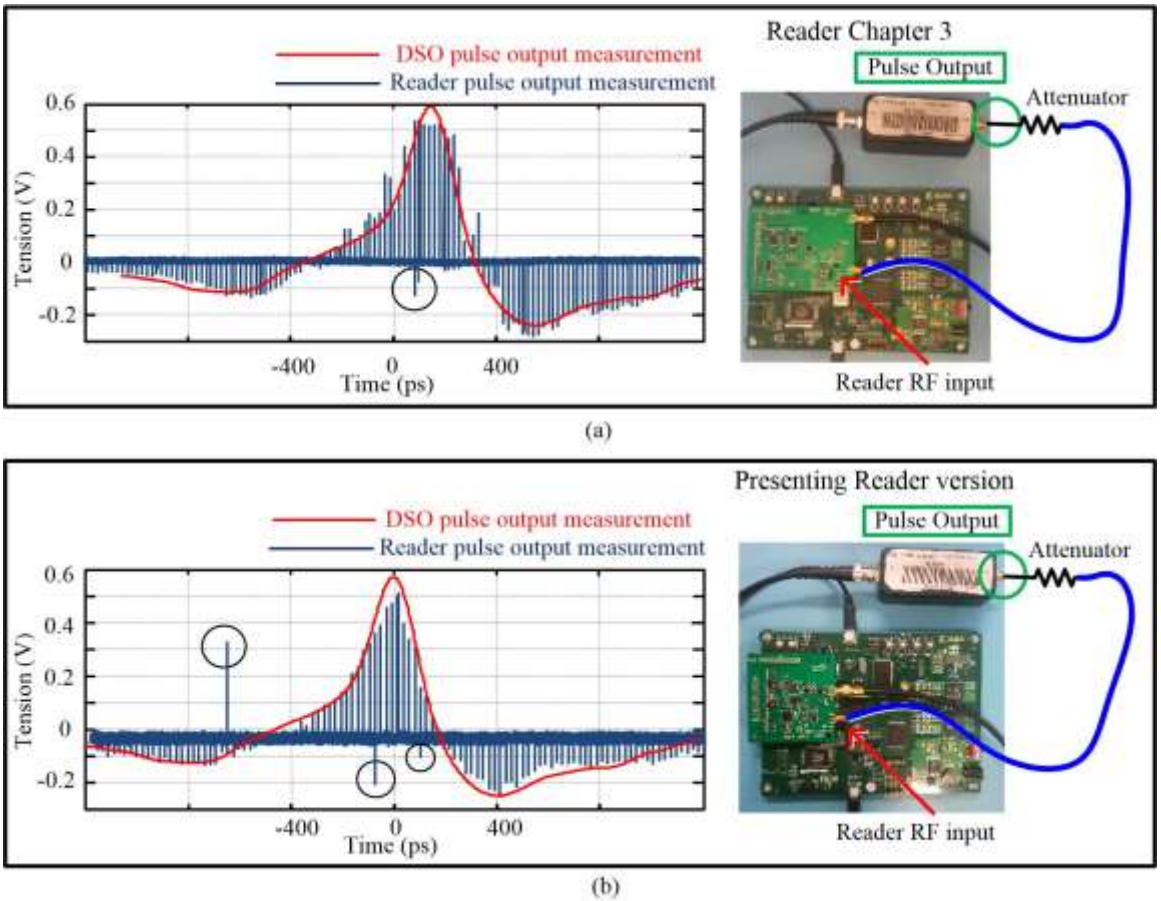


Figure 4.5. *Direct measurement of the pulse generator HL9200 from Hyperlabs, without averaging with reader and the real time DSO Agilent 91204A. (a) Measurement with the reader version presented in the chapter 3. (b) Measurement with the presenting reader (low jitter). The higher sampling noise of (a) is evident, especially where the pulse has the higher slew-rate.*

The sampling noise of figure 4.5 (b) is imperceptible, whereas both versions suffers from synchronization problems during the acquisition. This is shown on the figure plots with black circles, where some acquired points are referred to different timing positions. This kind of problem has been a constant in all prototypes devised so far, and it has been solved working around the FPGA implementation as shown in the next section.

The new architecture of the FPGA will be shown in the next section. The problem of synchronization and the reducing of reading time are correlated with the FPGA internal implementation. The solutions adopted are carefully explained, while particular technical discussions are in Appendix.

4. FPGA architecture

The block schematic of the FPGA embedded system is shown in figure 4.6. Compared with the previous designed reader (Chapter 3), the new version makes use of an external flash memory. The embedded microprocessor system is composed of the Microblaze 8.20a microprocessor connected with an internal BRAM of 32 kB with LMB bus in a Harvard architecture. The PLB bus is used to connect all the other peripherals: the 4 leds GPIO controller, the interrupt controller, the RS232 uartlite controller to transfer information between the reader and the PC, the serial peripheral interface (SPI) for the external flash memory, the external DDR2 memory controller, and finally the Reader_0 custom peripheral to control the reader acquisition. A considerable work has been spent for the optimization of the FPGA architecture, most for the custom block Reader_0 to eliminate synchronization problems during the acquisitions and to reduce the reading time.

The external flash memory allowed for a FPGA self-configuration at the reader start-up. With the previous reader version, the user has to download the bitstream into the FPGA at each start-up. The detail of the use made of the external flash memory is in Appendix IV.

4.1. Reducing reading time

In this reader version the reading time was optimized working around the different aspect of the FPGA implementation. A work has been done around the UART connection to the PC, and the algorithm used to code the reader data to be transferred to the PC was optimized. In

addition low level C functions were employed, and the architecture of the Reader_0 custom peripheral updated with hardware averaging calculation.

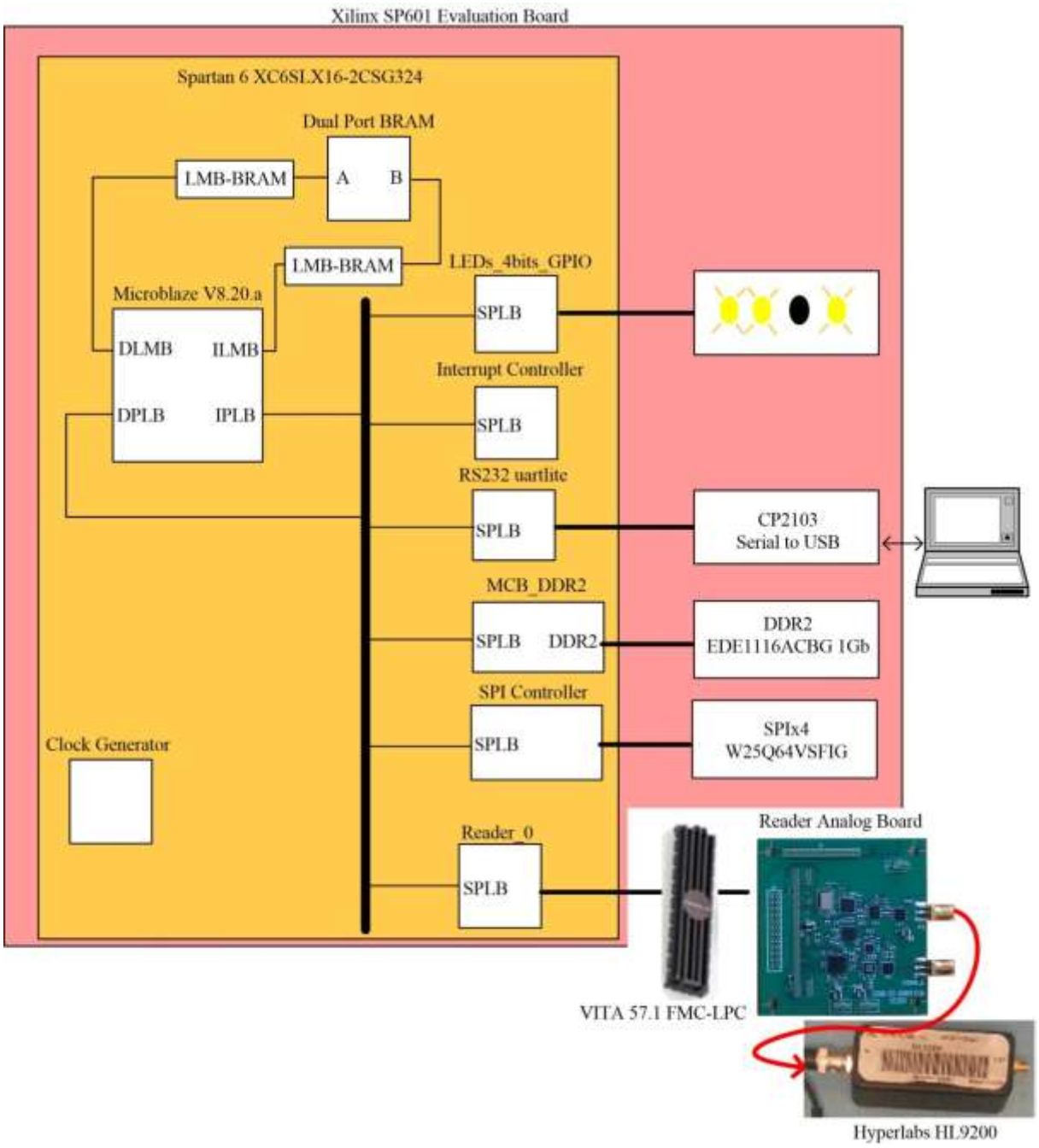


Figure 4.6. *Block schematic of the FPGA embedded system: with the main peripherals of the digital board SP601 used to implement the reader. The custom block Reader_0 is the solely that may communicate with the analog board, and trigger the pulse generator with the clock gating configuration.*

4.1.1 UART optimization

The UART of the first reader version had a BR of 460.800 kb/s. In the new reader version, the BR was first increased from 460.800 to 921.600 kb/s. This modification speeded up the communication but put more constraint on the FPGA internal clock.

From the RS232 uartlite data sheet [XIL 17a], the UART sampling clock is attained using an integer counter at the master clock, therefore compared to the aim of 14.746 MHz (921.600 kb/s × 16), an error is introduced. An UART device may support a sampling clock error in between ±5 % [XIL 17a]. In case of first reader version, the master clock was exactly 66.67 MHz instead of 67 MHz. The objective UART sampling clock was of 7.3728 MHz (460.800 kb/s ***x*** 16) but the real UART sampling clock was of 7.408 MHz (66.67 MHz / 9) with an error of only 0.48 % ((7.408-7.3728)/ 7.3728), which is inside the ±5 % limit. If the same master clock is applied to the bigger BR of 921.600 kb/s, the UART sampling clock will be of 13.334 MHz (66.67 MHz / 5), with an error of 6.1 % ((13.334-14.746) / 14.746) outside the limits of ±5 %. Working with the clock wizard of the Xilinx Platform Studio software, a new Master clock of 73.333 MHz was synthetized. This helps to reduce the error from 6.1 % to only 0.54 % ((14.666-14.746) / 14.746), without violating the clock tolerance of the microprocessor (Microblaze 8.20a), and the attached peripherals. The use of a BR of 921.600 kb/s for the UART, instead of 460.800 kb/s, allows reducing the transfer data time to the main PC of a factor of 2 with respect the first reader version.

4.1.2 Transfer data to PC algorithm optimization

In the first reader version (chapter 3), the ADC output resolution was of 10 bits, and a complete acquisition frame, even with averaging, was composed of samples of 10 bits. Inside the application software that was written in C, the acquired frame was represented with the vector *pulse[i].* For each word of 10 bits of *pulse[i]*, a maximum of 6 bytes was transmitted to the PC using the function *xil_printf* from C Xilinx library. The American Standard Code for Information Interchange (ASCII) was used as character encoding standard. The chunk of code of the application software in charge of it was:

```
for(i = 0; i < num_rcvd; i++)
    xil_printf("%d\r\n", pulse[i]);
```

Where *num_rcvd* was the length of the vector pulse, which is equal to the number of acquired points inside the reader acquisition frame. At 10 bits (ADC resolution) corresponds

an integer number between 0 and $2^{10} - 1$ (0-1023). Each can be represented in ASCII with a number of bytes in between 1 (0-9) to 4 (1000-1023), where each byte represents a digit. Each element of the vector *pulse* is the results of an averaging process. However, because they are integer, they do not have a fractional part, and therefore are still being representable with maximum 4 bytes in ASCII [MIC 17].

The argument of the function *xil_printf* has also the two ASCII characters \r \n, representing respectively carriage return and newline. These two characters were used to simplify the code development in C for the FPGA, and in Matlab for the PC. In fact each element of the *pulse* vector was represented with a variable number of bytes (between 1 and 4) hence, a sort of ASCII character, to inform the Matlab code about the bytes number for each *pulse* element, was needed. In the new reader version, each element of *pulse* vector was represented with the same number of bytes, as so the two ASCII characters \r \n were no more indispensable. The ADC has 9 bits instead of 10 bits, therefore the ADC output is between 0 and 511 ($2^9 - 1$).

In the new reader version each *pulse* vector element (0 - 511) was sent using only two ASCII characters. The *pulse* element was represented with 9 bits, therefore the first ASCII character was in charge of the 6 bits from position 5 to 0, while the second character the last three bits from 8 to 6. Finally the two characters (bytes) were manipulating to avoid transmitting one of the 33 special ASCII characters, which are represented with the bytes with decimal value from 0 to 32.

To transmit the bytes to the PC the function *XUartLite_Send* was used, which is provided with the RS232 UART component driver. It is a function at a lower level compared with *xil_printf,* and so potentially faster. The *XUartLite_Send* function has three arguments, the pointer to the RS232 UART component instance, a pointer to the buffer of data to be transmitted, and finally the number of bytes being sent. This function transmits the specified buffer of data using the UART in either polled or interrupt driven mode. Because it is not a blocking function, it will return before the data has been sent by the UART [XIL 17b] and a sort of timing interval between each called of the function is needed. The function has been used with 8 as third argument because resulting in a faster vector transmission.

4.1.3 Hardware averaging implementation

In the previous version, the averaging process was implemented by software. Considering an averaging factor of *N,* for each of the *N* acquisitions, the content of the Reader_0 internal FIFO memory was transferred to the external DDR2 memory, and finally the microprocessor (Microblaze) was used to perform the averaging. The whole process took different seconds, where only the transfer process of the data from the Reader_0 internal FIFO to the DDR2 counts for 140 ms at each acquisition.

In the newer reader version, a hardware averaging was implemented directly inside the Reader_0 block. The content of Reader_0 memory is transferred to the DDR2 only one time, which is at the end of the acquisition, and no averaging process is required by the microprocessor (Microblaze 8.20a).

The Reader_0 block developed represents a big custom peripheral with its 387 slices over 2278 available, and 8 BRAM (18 kb each) blocks over 32 available. For mater of comparison the microprocessor Microblaze 8.20a, also implemented in the FPGA chip, counts for 882 slices, with the optional Barrel Shifter, integer multiplier, enabling optional Machine Status Register Instructions (MSRI), and pattern comparator. The same peripheral of the first reader version occupied 163 slices, which are less than half slices of the actual peripheral (387). To realize the Reader_0 block, the tool ISE Project Navigator within the Xilinx ISE design Suite 13.2 was employed. It allows for simulation at all the implementation levels, from behavioral to post place and route, and provides a schematic editor quite useful for a complex design. The Reader_0 custom block of the FPGA hardware implementation (see figure 4.8) is composed of a User Logic unit, and a PLB slave interface as for the previous reader version. The User Logic was realized with a hierarchical strategy and is composed of 10 main blocks. A more comprehensive description of the User Logic block is in Appendix V.

To speed up the reading process, the User Logic is composed of three FIFO memories, conversely in the first reader version there was only one. They are: FIFO_FAST_SAMPLE_PACKAGE, FIFO_FRAME_PACKAGE, and FIFO_STORAGE_PACKAGE. The first is a small memory of 32 words of 9 bits, connected directly with the ADC output. The second is capable of 4 k words, while the latter shows the same capacity of 4 k but with words of 20 bits. The use of three memories allows for a fast hardware averaging implementation, and assures a simpler Xilinx bitstream generation.

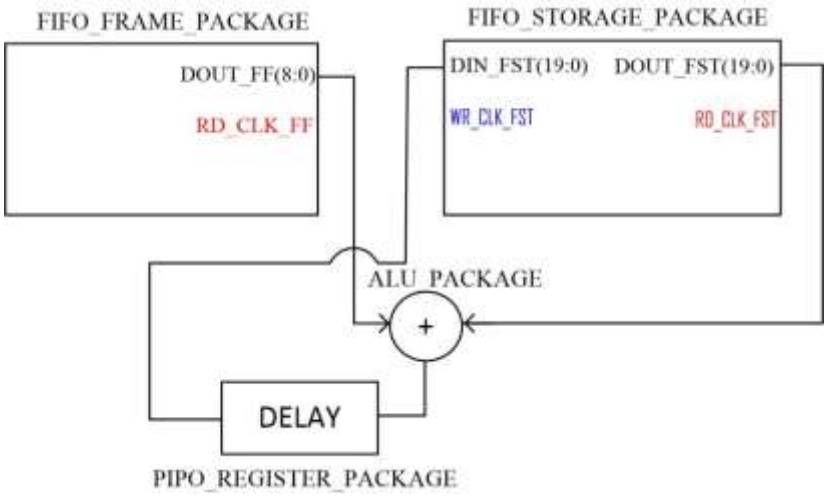


Figure 4.7. *Description of the fast averaging principle. The content of FIFO_FRAME_PACKAGE is added to that of FIFO_STORAGE_PACKAGE N times, where N is the averaging factor. After the FIFO_STORAGE_PACKAGE is downloaded selecting the correct 9 bits over the 20 bits output depending on N, in a shifting position based division.*

The part of the User Logic that takes care of the hardware averaging is shown in figure 4.7. The third memory FIFO_STORAGE_PACKAGE is used in collaboration with the ALU_PACKAGE and PIPO_REGISTER_PACKAGE. For an averaging of N, with N>1, first a tag response measurement is executed and memorized in the FIFO_FRAME_PACKAGE, after its content is transferred to the FIFO_STORAGE_PACKAGE as it is. Then for the N-1 remaining acquisitions, the content of FIFO_FRAME_PACKAGE is added to the content of FIFO_STORAGE_PACKAGE and together memorized in FIFO_STORAGE_PACKAGE. Therefore the FIFO_STORAGE_PACKAGE is at the same time read and written.

The PIPO_REGISTER_PACKAGE is a Parallel Input Parallel Output (PIPO) register [XIL 11a]. It is used as delay block, to compensate for the initial latency between reading and writing processes of the FIFO_STORAGE_PACKAGE, when executed simultaneously [XIL 11b]. The FIFO_STORAGE_PACKAGE memory accounts for words of 20 bits, while of 9 bits for the other two memories. This because during a measurement process, with a predefined averaging of N, each word of FIFO_STORAGE_PACKAGE contains the summation of N words of 9 bits. Thus, the maximum averaging factor depends from the length of FIFO_STORAGE_PACKAGE words. In binary representation, the multiplication of a number for 2 and division for 2 corresponds respectively to its shifting towards the left and the right of one position. The maximum possible averaging factor is therefore equal to 2048 ((2^{20-9})), limited in practice to 512 by software, and restricted to be a power of 2. For instance, if the

averaging factor is of 16, which is equal to 2^4, from each FIFO_STORAGE_PACKAGE world, the 9 bits representing the averaged measurement to transfer to the PC are that from position 4 to 13 (4- 9+4). For more details refer to Appendix V.

4.1.4 Conclusion

The reading time of the presenting reader version accounts for a reducing factor of about 1,000 compared to the previous version. As a result of the flexibility of the proposing reader, the reading time depends from the chosen parameters. The minimum reader time was of about 6 ms without averaging, and of about 50 ms with an averaging of 64.

4.2. Solving acquisition synchronization problems

The connection between the main components of the reader RF front-end board, and the custom block Reader_0 inside the FPGA chip (Spartan 6) is shown in figure 4.8. Compared with the first reader version, it shows a more complex schematic (Appendix III), where two clocks are involved, the master clock inside the FPGA at 73.333 MHz, and the clock of 125 MHz generated from the analog board (RF front-end).

The clock of the ADC is not required to be low jitter because, besides the trigger of the pulse generator, the reader sampling noise depends solely from the clock of the S/H amplifier, as demonstrated in the section 3. The output of the S/H amplifier is a constant value for a complete clock period, as so the fluctuations of the ADC sampling event caused by the jitter do not create error in the acquired signal. From figure 4.8 the Reader_0 block is composed of a PLB slave interface and a User Logic, where the first allows the communication between the User Logic, and all the others peripherals connected with the same PLB bus. The output of the delay generator was connected with the S/H amplifier, as sampling clock, and also with the FPGA through the User Block. The connection with the FPGA was conceived to simplify the design. But finally the User Block was optimized to avoid the use of this signal as underlined in figure 4.8. This optimization may reduce the sampling noise in a future reader version because the buffer at the output of the delay generator won't be needed anymore. It also will reduce the reader realization cost, for the absence of the buffer and also of the digital standard converter PECL-TTL chip. The use of the digital standard converter was essential to increase the dynamic excursion of the signals

crossing the VITA 57.1 FMC-LPC connector to reach the FPGA. The connector is not conceived for high frequency signals, and at 125 MHz they are plenty attenuated.

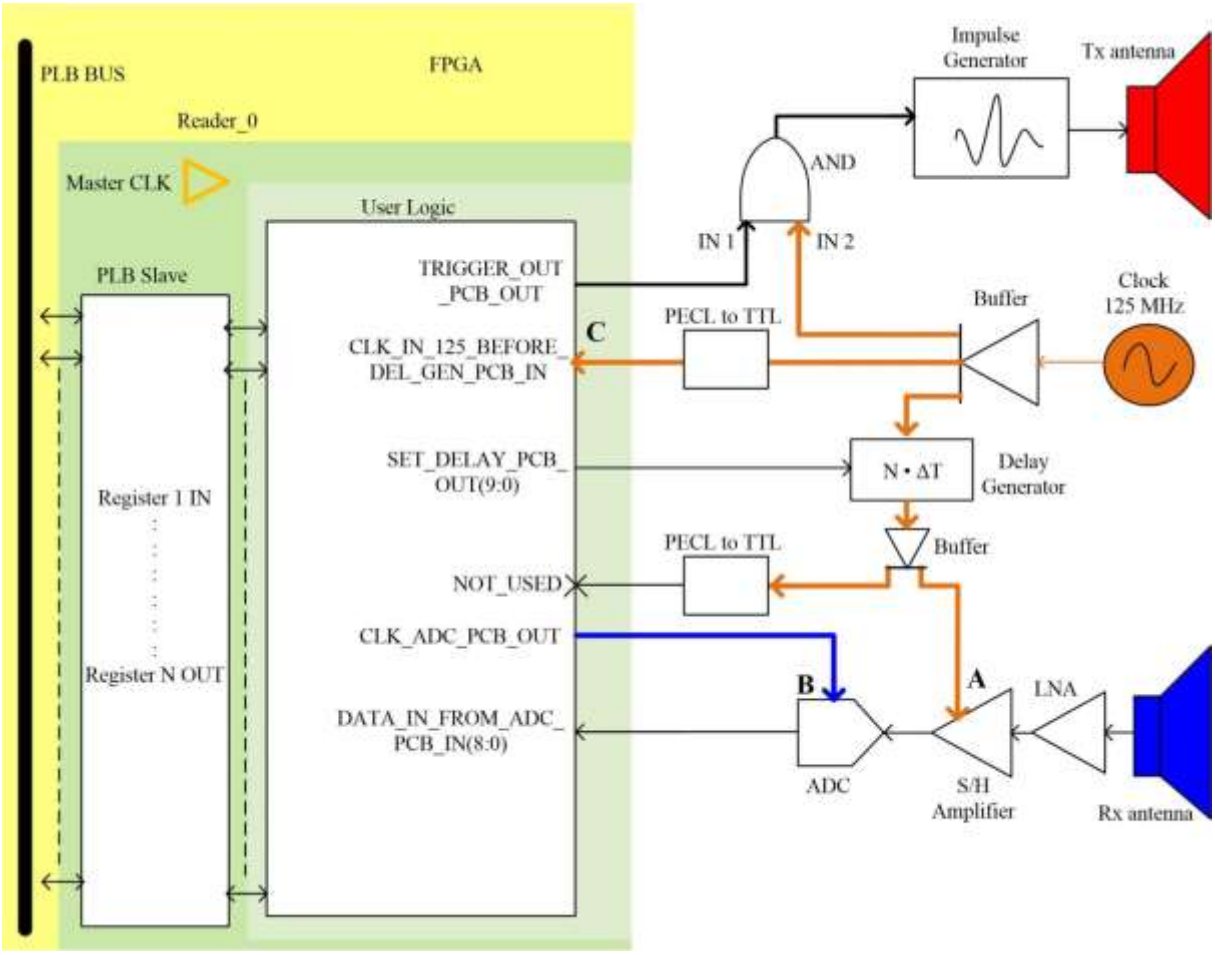


Figure 4.8. *Connection between the main components of the reader RF front-end board, and the custom block Reader_0 inside the Spartan 6 FPGA chip. Compared with the first reader version, it presents many synchronization issues tackled to improve the tag reading quality.*

Contrarily to the previous reader version (chapter 3), many constrains about synchronization of different signals have been added to the new one to improve the reader performance. According to figure 4.4 (b), a precise temporal relation exists between the two AND gate inputs, *IN 1* and *IN 2,* as seen in sub-section 4.3. From figure 4.8 the ADC has the clock sourced by the FPGA, and ideally can sample its analog inputs only when the S/H amplifier output is stable. The ADC output (DATA_IN_FROM_ADC_PCB_IN(8:0)) has to be memorized inside the User Logic memory with a proper clock. As shown in figure 4.5, all these synchronization issues degrade the reader acquisition if not accurately handled.

The cooperation between the digital board (Xilinx SP601) and the RF front-end is notable and the design of the User Logic become quite complex. In addition the delay of the different signals connecting the FPGA with the RF front-end is not characterized caused by the use of a commercial digital board (SP601). However the FPGA provides different resources to help the resolution of synchronization issues such those in this project.

The ADC sampling clock is sourced by the FPGA, and is obtained from the sampling clock of the S/H amplifier before being delayed by the delay generator (see figure 4.8). During an acquisition, the dynamic internal delay of the delay generator is varying with minimum steps of 10 ps (ΔT) to cover the sampling clock period that is of 8 ns (1/125 MHz). Thus, the sampling clock signals of the ADC and of the S/H amplifier have a variable relation of phase during the acquisition. If an acquisition process is supposed, where at the beginning the two clocks are out of phase as shown in figure 4.9 (a), their phase relationship will be modified during the acquisition at each update of the internal delay of the delay generator. As shown in figure 4.9 (b) and (c), for a certain delay generator range values, the two clock rising edges of the ADC and of the S/H amplifier are close, it may result in an ADC not optimal operation acquisition.

Considering the case shown in figure 4.9 (b), where the S/H amplifier sampling clock rising edge happens before that one of the ADC. The output of the S/H amplifier may be considered a step signal. If the two rising edges are excessively close in time, the ADC limited analog input bandwidth cannot follow the sudden S/H amplifier output variation at the sampling clock rising edge event. In this case, an analog ADC data setup time can be defined. The equation [4.7] is the classical step response relationship between filter output rise time (10/90 %) and bandwidth [DEL 98],

$$Rise\ time = \frac{0.35}{Bandwidth}. \qquad [4.7]$$

The ADC input analog bandwidth is of 550 MHz. Therefore from equation [4.7] the analog setup time should be of at least 0.63 ns.

The ADC samples its analog input at the clock rising edge with an aperture delay of about 0.8 ns. This can be translated in a sort of ADC analog data hold time around the ADC clock rising edge, which must not be violated. From the ADC specifications, the recommended analog hold time is of 1.2 ns. The S/H amplifier is able to actualize its output

at each rising edge of its sampling clock, with an aperture delay of only 55 ps. Therefore the S/H amplifier sampling clock rising edge, if subsequent at the ADC sampling clock rising edge, has to respect the ADC analog hold time, as shown in figure 4.9 (c).

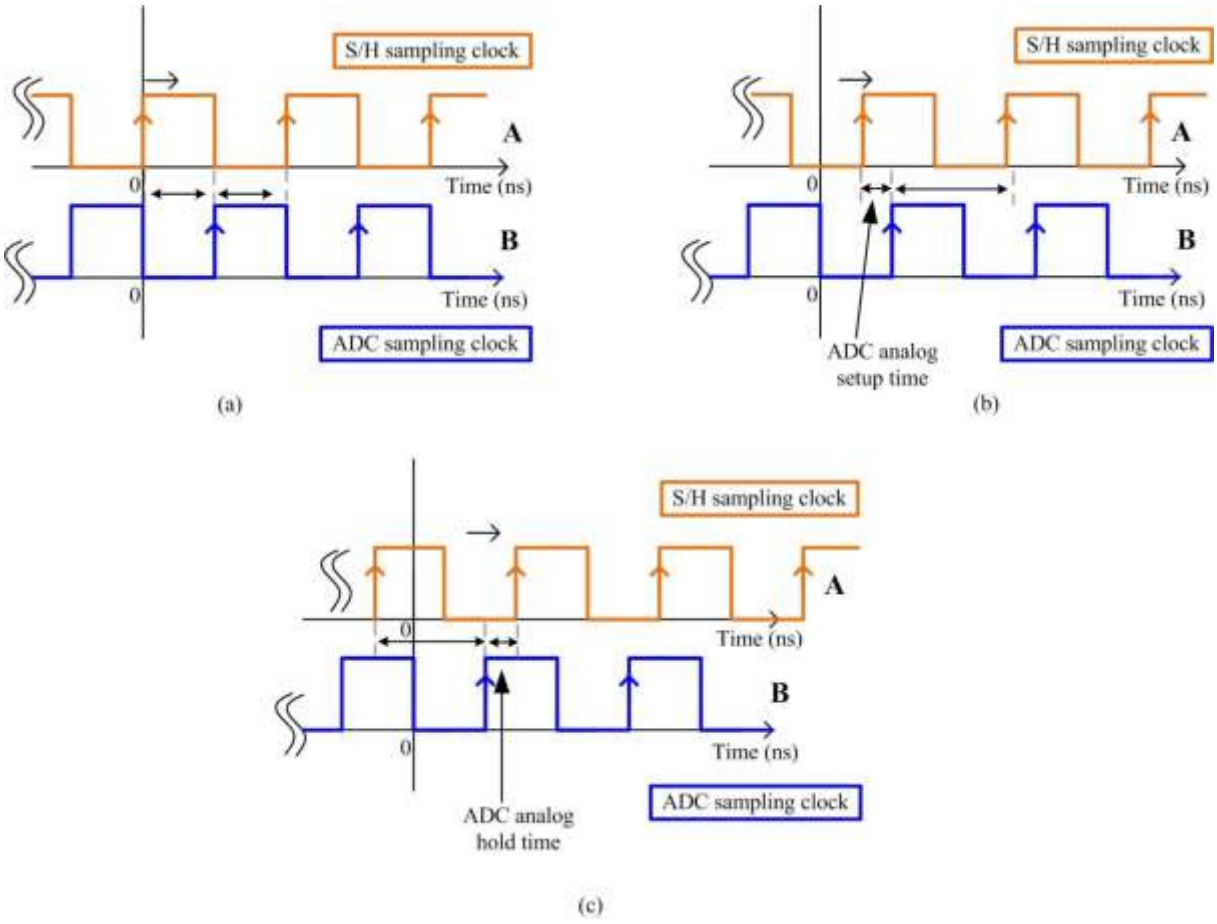


Figure 4.9. *The ADC sampling clock (blue lines), and the S/H amplifier sampling clock (orange lines), have a variable relation of phase during the acquisition process. (a) At the beginning of the reader acquisition the two clocks are out of phase. (b) The S/H amplifier sampling clock event is still anticipating the ADC sampling clock event, but they are closer in time and the ADC analog setup time may be violated. (c) The S/H amplifier sampling clock event is subsequent with respect the ADC sampling clock event. They two events are close and the ADC analog hold time may be violated.*

In the FPGA User Logic implementation, the required dynamic delay of the delay generator (0-8 ns) was divided in three sub-frames: 0 ns - 2.55 ns, 2.55 ns - 6.4 ns, and 6.4 ns - 8 ns. From figure 4.10 (a), at the beginning of the first sub-frame, the ADC clock and S/H amplifier clock were out of phase. After, varying the dynamic delay towards 2.55 ns, their phase relationship changes according to the figure 4.10 (a). To attain their first phase relationship, the FPGA internal PLL utilities where exploited [XIL 15a]. In the first sub-frame,

the minimum analog ADC setup time was of 1.45 ns, and the hold time of 4 ns. It does not violate the ADC setup and hold time just defined (0.63 ns, 1.2 ns).

For the second sub-frame of the dynamic delay of the delay generator (2.55 ns - 6.4 ns), the ADC sampling clock phase was varied of 180 deg using the same PLL, as shown in figure figure 4.10 (b). The minimum analog setup time was of 1.6 ns, and 2.55 ns for the hold time. For the last sub-frame 6.4 ns - 8 ns, shown in figure figure 4.10 (c), the ADC clock was phase shifted again of 180 deg, and the minimum ADC analog setup time and hold time were respectively 4 ns and 2.4 ns.

The division of the dynamic delay generator frame in three sub-frames, with the variation of the ADC sampling clock phase at step of 180 deg, assured lower SNR and reduced synchronization problems. The others synchronization problems were faced in the User Logic block design. The internal memorization of the ADC output was optimized with an IODELAY2 block inside the FPGA, which provides a variable delay generator with step of about 40 ps [XIL 15b]. It was used to properly delay the ADC outputs signal to respect the corresponding User Logic FIFO setup and hold time.

The temporal relation needed between the two AND gate inputs, *IN 1* and *IN 2,* was detailed in section 3 and shown in figure 4.4 (b). To properly gating the on RF front-end board clock generator, for each trigger event, the FPGA *IN 1* signal is high (1_2) for 1 clock cycle that corresponds to a duration of 8 ns. Playing with simple logic gate implementations, its output can be delayed of 4 ns corresponding to a half clock cycle (180 deg), to best fit the low jitter clock (125 MHz) gating requirement of figure 4.4 (b). In the next section the same experiments of section 3.1 was executed, as to show the resolution of the reader synchronization problems during the acquisition.

4.3 Demonstration of the resolution of synchronization problems

The same pulse output measurement on figure 4.5 was executed and the results are shown in figure 4.11. The figure compared the reading performed with the presenting reader version, before and after the resolution of the synchronization issues faced in this paragraph, respectively in figure 11 (a) and figure 11 (b). The measurement with the optimized User Logic on figure 11 (b) does not show any synchronization issue, contrarily to the figure 11 (a) (points with black circles).

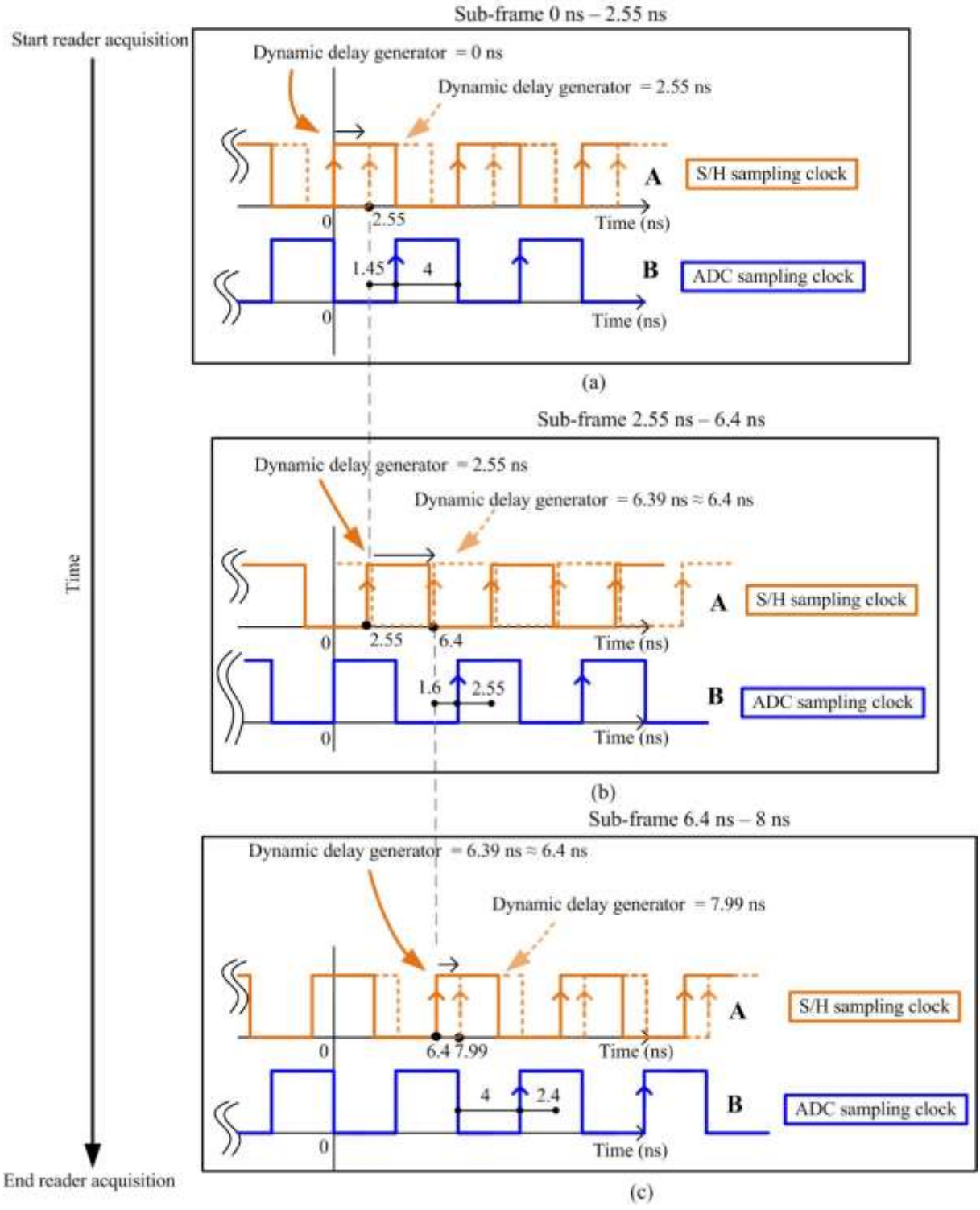


Figure 4.10. *Progress of the ADC sampling clock, and of the S/H amplifier sampling clock during a reader acquisition process. (a) Progression for the delay generator dynamic delay between 0 and 2.55 ns. (b) Delay generator dynamic delay between 2.55 and 6.4 ns. (c) Delay generator dynamic delay between 6.4 and 8 ns.*

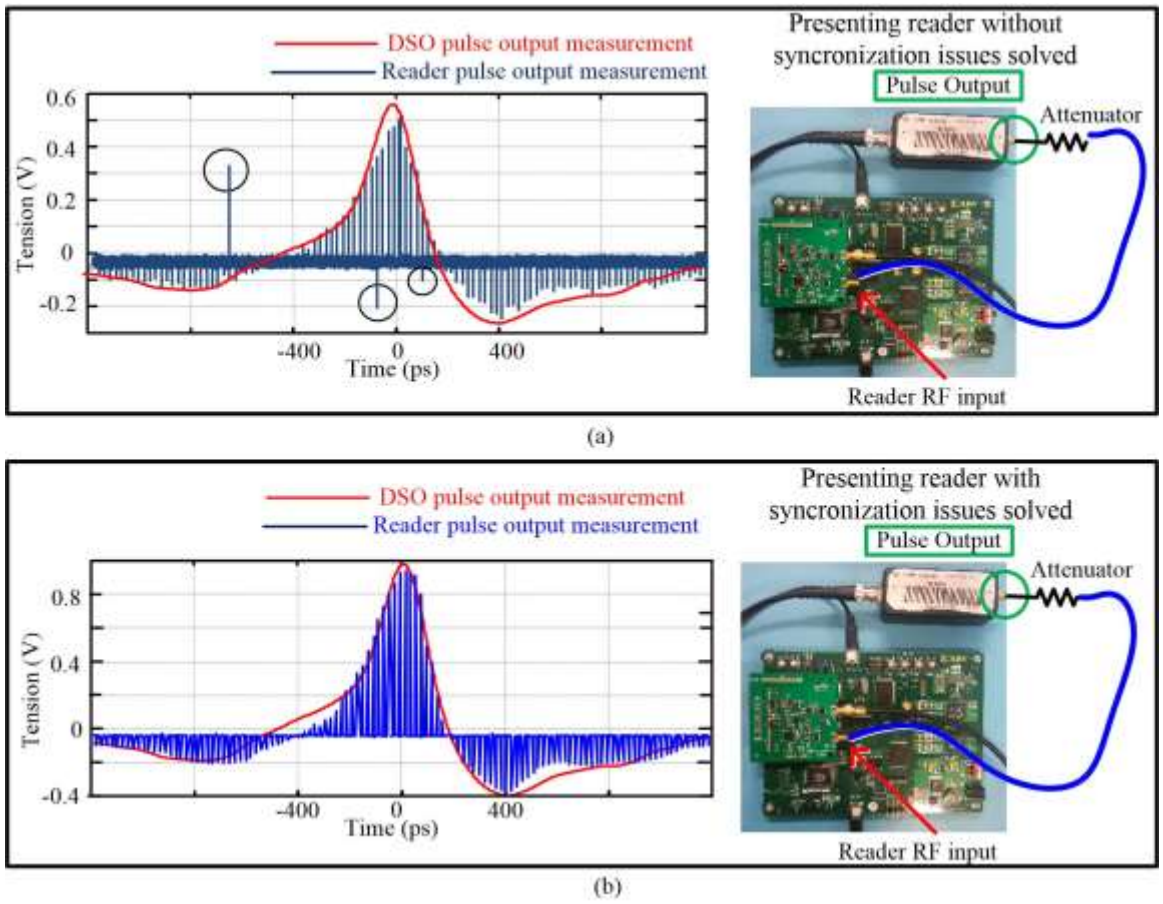


Figure 4.11. *Direct measurement of the pulse generator HL9200 from Hyperlabs without averaging with reader and the real time DSO Agilent 91204A. (a) Measurement with the presenting reader before handling the synchronization issues (black circles). (b) Measurement with the synchronization issues solved.*

5. Reader specification

The reader costs and performance are resumed in table 4.1. Respect with the previous version (table 3.2 chapter 3), it shows a limited reduction of retail cost, from 2,350 € to 2,306 €. Noted that the price of the Xilinx SP601 evaluation board has increased since 2014 of 70 €. The S/H amplifier sampling clock period jitter has a variance reduced of three times. The reader shows flexibility in terms of acquisition frame position, length, and equivalent sampling period (ΔT). This flexibility was obtained working around the FPGA Reader_0 block architecture, and the FPGA application software.

The averaging factor is variable between 1 and 512, with power of 2. The reading time depends from the chosen acquisition parameters but the minimum is of around 6 ms, while

the maximum of around 500 ms. Finally, the reader shows a sensitivity of -60 dBm, this figure can be improved using an ADC with a better resolution at the expense of higher reader cost.

The Matlab application software for the PC is described in Appendix VI. It uses the Short Time Fourier Transform (STFT) algorithm, where in [RAM 16] the STFT for REP based UWB frequency-coded chipless RFID tags is studied.

Reader retail cost after tax	
Component	**Retail Cost after tax (2013*/2017**)**
RF Front-end board components	886 € **
Digital board (Xilinx SP601 E.B.)	420 € **
Pulse generator (Hyperlabs HL9200)	1,000 € *
Total cost	2,306 €
Reading performance	
PRF	1 MHz
Input bandwidth	1 – 11 GHz
Acquisition frame duration	8 ns – 256 ns / step of 8 ns
Frame position	Variable
Equivalent sampling period (ΔT)	10/20/30/40 ps
Averaging	[1 – 512] (Power of 2)
Reading time	from 6 ms to 500 ms
S/H Amplifier sampling clock period jitter	2.45 ps RMS (16.31 ps p-p) over 1k cycles
Reader sensitivity	-60 dBm

Table 4.1. *Components retail cost after tax of the presenting optimized designed reader (not considering the antenna), and performance specification.*

6. Reader power supply board

The reader RF-front end board and pulse generator required diverse power supply points. The FGPA development board provides power pins on the VITA 57.1 FMC-LPC connector. The most useful for reader requirements are the 12 V pins with maximum current of 1 A, the 3.3 V with 3 A, and finally the 2.5 V with 2 A. The required supply voltage for the RF front-end board are 3.3 V for the majority of components, 1.8 V for the ADC, 5 V for the LNA and S/H amplifier, -5.2 V for the S/H amplifier. Finally 9 V is required by the pulse generator HL9200 from Hyperlabs. The 3.3 V was taken directly from the corresponding pins on VITA connector, while the others extracted from the 12 V pins with a developed board. A photograph of the alimentation card mounted on top of the RF front-end is shown in figure

4.12. It is a 2 layer board on a low cost FR4 substrate, the bottom layer is a ground plane without signal traces to reduce interference with the underneath analog board. The board schematic is shown in Appendix VII.

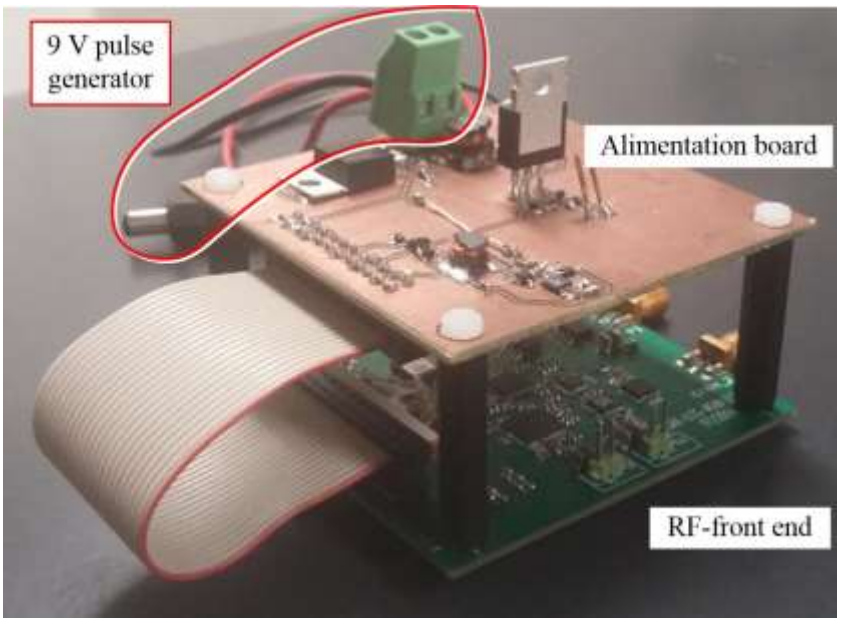


Figure 4.12. *Alimentation board of the reader mounted in top of the RF front-end board.*

7. Reader tag measurement

The reader was tested with intensive tag measurements. For comparison, the same UWB frequency-coded tags, used to test the first reader version in chapter 3 section 6, were employed to test this optimized reader.

The measurements were performed with the reader and the DSO at about 15 cm from the tag. In figure 4.13 is shown a photograph of the measurement bench for the reader case. It consists of a typical office scenario with metallic cabinets, chairs, tables and computers. The Satimo QH2000 dual-access dual-polarization antenna is connected to the reader to have a cross-polarization reading scheme. In reception, the UWB filter Mini-circuits VHF-3100+ was placed to eliminate the out of band noise such as the Wi-Fi at 2.4 GHz. In fact in a real time approach, even with averaging, the out-of-band signals may be filtered by software. In an equivalent time approach, this is not possible and the out-of-band signals may add noise in the frequency band of interest. To clarify this point, it is useful to recall that in this approach, the sampling frequency is very low and of 125 MHz. It does not respect the Nyquist–

Shannon theorem when used to acquire UWB signals that are in the band 3.1 – 10.6 GHz. Therefore for each acquisition, the out of band noise is replicated inside the band of interest. The averaging factor helps to reduce this noise, but because of the low power response of the tags, it is still important. For the DSO, the same setup was employed using the same pulse generator HL9200 from Hyperlabs and the antenna Satimo QH2000. From the figure 4.13, the tag was placed on top of a square wood of few millimeters of thickness with the antenna below. This setup creates a successfully reading process in non ling-of-sight condition, which cannot be possible with barcode technology.

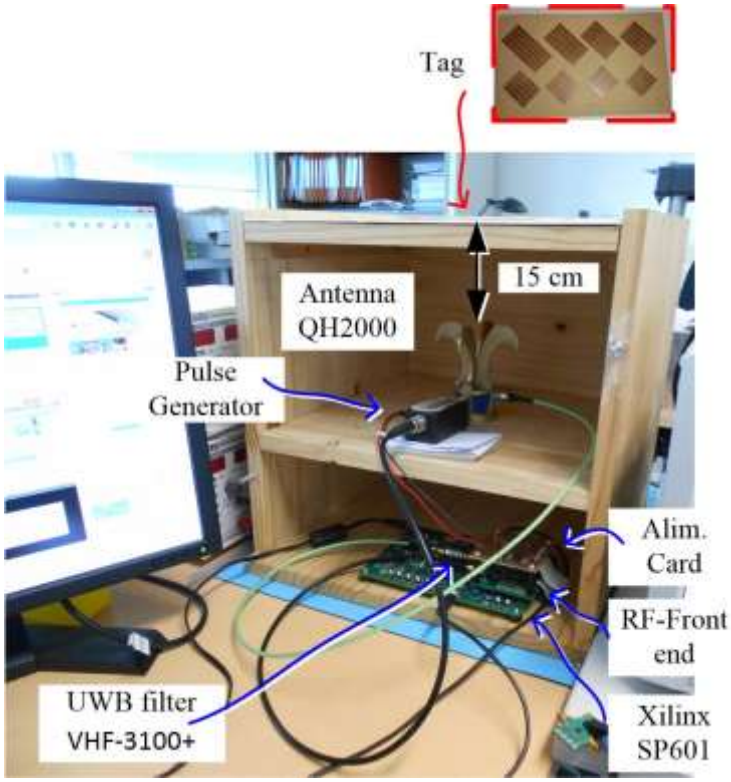


Figure 4.13. *Measurement bench for UWB frequency-coded tags in practical environment for the reader and DSO in a non ling-of-sight condition.*

The measurement results using the STFT algorithm described in [RAM 16] are shown in figure 4.14. The eight resonant frequencies are matching for both tags between DSO and reader. The tags can be decoded without any error.

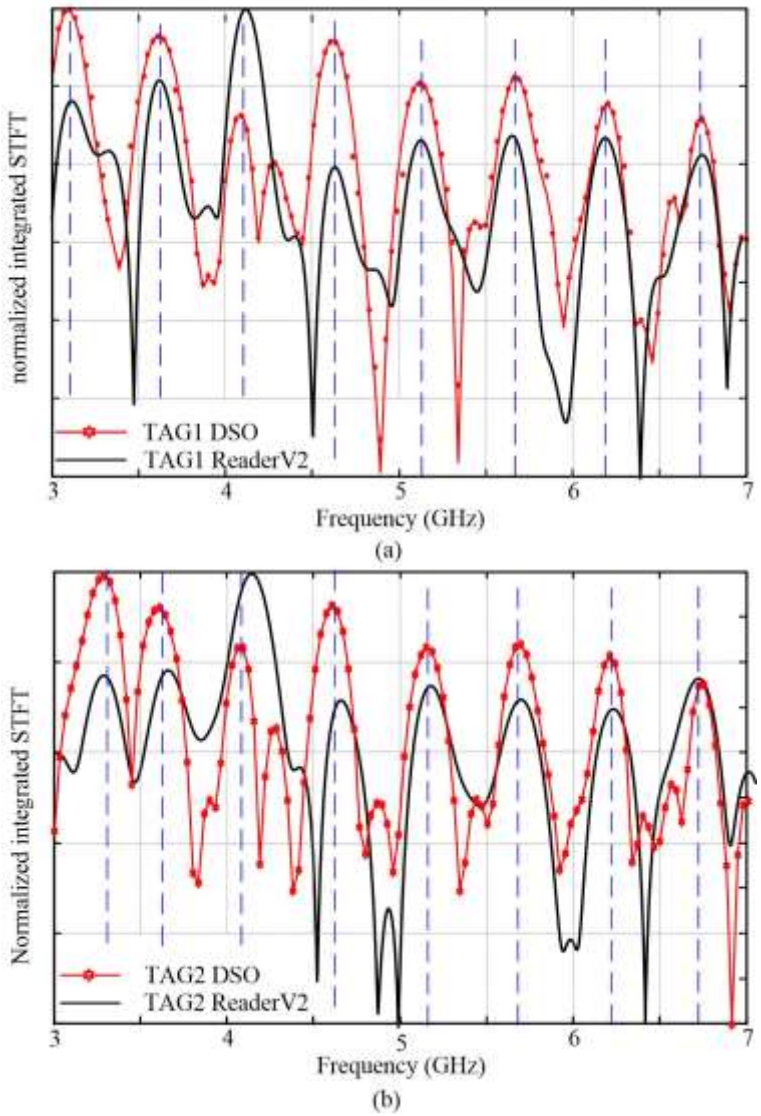


Figure 4.14. *Measurement results of two UWB frequency-coded tags, with reader in black and DSO in read. In (a) the results for the first tag and in (b) for the second one, in both cases the curves indicate the same resonant frequencies as expected.*

The reader was shown in the Drupa 2016 event, in Düsseldorf Germany from 16 June to 25 June, which is a global showroom for printing technologies, and accredited as the biggest showroom in the word. The reader worked without interruptions for 10 hours a day reading printed single layer Powercoat PW230 paper substrate frequency-coded tags. A reader box were designed with the open access FreeCAD software, and realized with a 3D printing machine. A photograph of the reader within its box during the Drupa 2016 is shown in figure

4.15. In the next section the frequency based and the IR-UWB approaches will be studied in terms of reading tag accuracy, where the impact of the jitter for an IR-UWB is underlined.

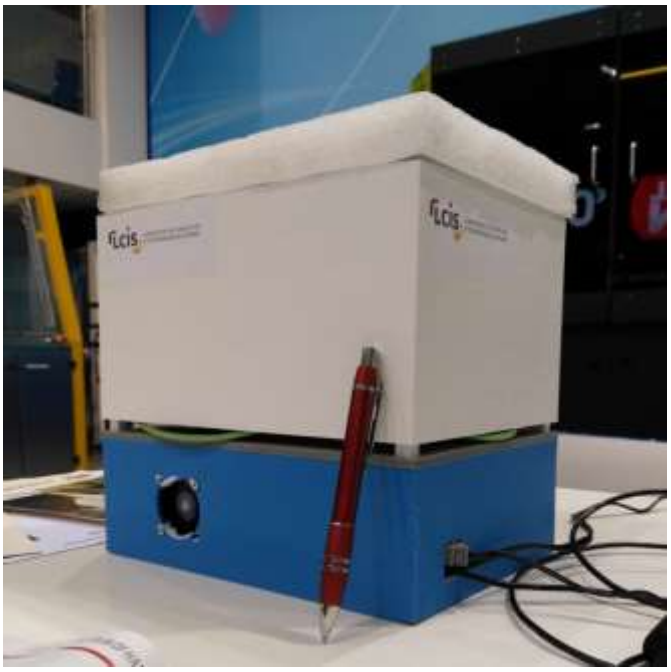


Figure 4.15. *Photograph of the reader within its designed box at the Drupa 2016 event in Düsseldorf (Germany).*

8. Frequency based reader vs IR-UWB with different jitter level

In the first two chapters the two frequency based reader approaches, SFCW and FMCW, used in literature for UWB chipless applications have been introduced. A frequency based approach gives the possibility to perform more accurate measurement compared to an IR-UWB solution. This is because of the higher dynamic range (sensitivity) that can be obtained with such solution. The interrogating signal is sweeping around the frequency band of the tag, where the sweep time is defined at the reader level. Conversely in IR-UWB systems, the interrogating signal is a short pulse in the UWB band, and the tag response lasts notably for only few nanoseconds (around 12 ns) [RAM 16]. Because of the short duration of the tag response, and its amplitude envelope, an IR-UWB can perform tag reading with a limited frequency resolution compared to a frequency based reader. Also, an IR-UWB system is affected by sampling clock jitter and higher input noise bandwidth. According with equation [4.5], the sampling clock jitter impact is more significant at higher frequency, where at small unwanted timing translations of the sampling clock event correspond higher phase variation of the acquiring signal. On the other side, an IR-UWB approach is easier compatible with

UWB regulations as shown in chapter 2, and has a reduced reading time. For instance, the reader presented in this chapter can have a reading time as low as 6 ms, with an input bandwidth between 1 to 10 GHz.

An equivalent time reading system with different parameters has been emulated in Matlab, and the results are shown in figure 4.16. An ideal tag mode response, where the tag is supposed to have eight resonances between 3.2 and 6.7 GHz, has been emulated. The resonators were supposed with an infinitive quality factor. Two different tag response durations (100 ns and 12 ns) have been considered. In case of 12 ns, the reading system was supposed to be affected by a jitter of 0, 7.34, and 40 ps respectively. The 7.34 ps jitter is the jitter of reader in chapter 3, while the 40 ps jitter corresponds to the jitter of the IR-UWB radar for through-wall application introduced in [LIU 13]. Analyzing the effect of the two different signal durations without jitter, the larger one allows for a better reading frequency resolution. It may be translated in the possibility of developing tags with smaller inter-distance between resonances, and therefore higher bit capacity.

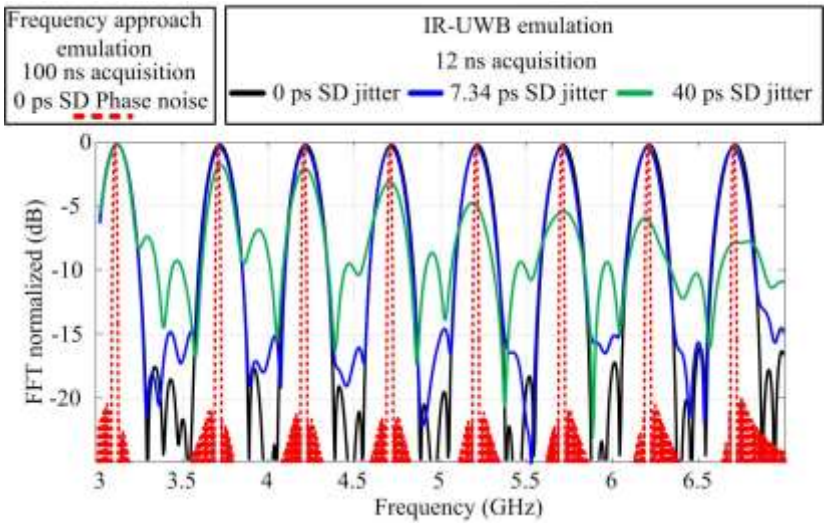


Figure 4.16. *Emulation of the frequency response of a chipless tag read with a frequency based approach, and with an IR-UWB reader working in equivalent time. The IR-UWB reader is affected by 0, 7.34, and 40 ps of jitter. The tag with longer response (100 ns) corresponds to a FMCW approach, where an IF bandwidth in the order of kHz can be obtained. The shorter tag response (12 ns) corresponds to the case of an IR-UWB approach.*

The larger duration corresponds to the case of a frequency based interrogation, where the IF bandwidth can be in orders of kHz. The effect of the jitter variation for the smaller response

duration has also been studied. It represents a real tag signal response in the case of an IR-UWB based interrogation system. The jitter augmentation affects the reading capability as shown in the figure, where the distance between the main lobs of the tag's response (which are located around the tag frequency resonances), and the secondary lobs is smaller. Moreover, the peak apexes corresponding to these main lobs decrease with frequency, and also their frequency value and bandwidth vary especially at high frequency.

A chipless tag acquisition with different reading systems, which are based on SFCW and IR-UWB with different performance in terms of jitter, is shown in Figure 4.17. The frequency-domain chipless tag employed presents eight resonances between 3 and 7 GHz, and is the same used to characterize the readers so far. All the measurements were performed in an anechoic chamber to reduce as much as possible the noise distinct from the jitter system.

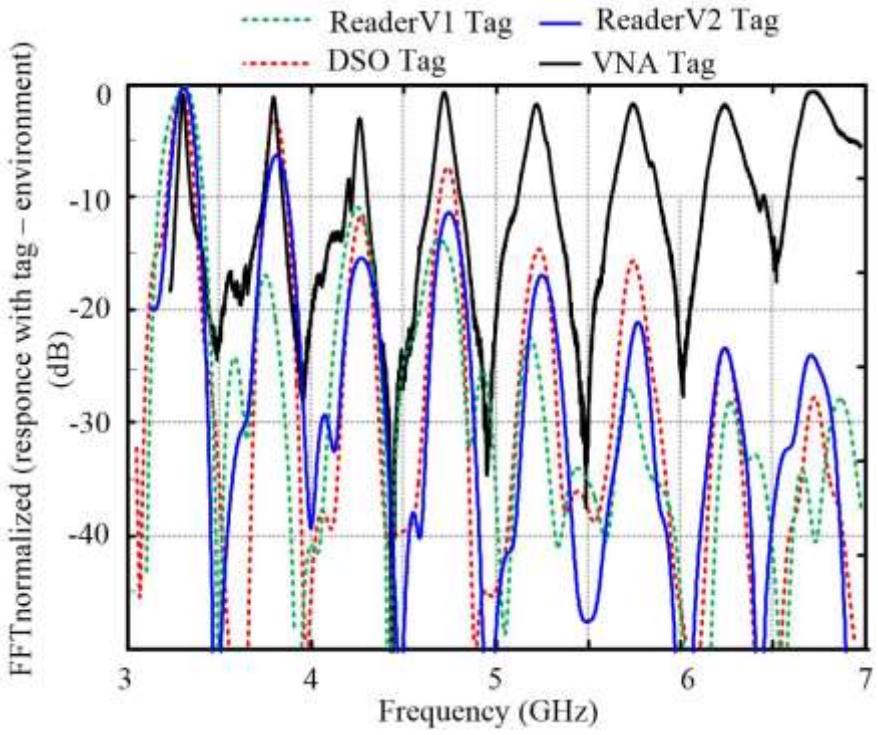


Figure 4.17. *A chipless tag acquisition with different reading systems, which are based on SFCW and IR-UWB with different performance in terms of jitter. The VNA N5222A from Keysight emulates a SFCW based reader, while the first reader version (Chapter 3) and the second version used to show jitter effects.*

The measurement with the VNA N5222A from Keysight emulates a chipless reader based on SFCW. It is a costly test equipment with performance greatly superior at all the presented

frequency based chipless reader in literature as for [KOS 12 - POP 16 - PRE 10]. The DSO 91204A measurement was performed with the Hyperlabs HL9200 pulse generator in an IR-UWB configuration. With *Reader V1* is indicated the reader version presented in the chapter 3, while with *Reader V2* is indicated the presenting optimized reader.

As expected, the measurement with the VNA presents the best performance and with the higher frequency resolution. In addition, compared to the other measurements (IR-UWB configurations), all the peaks present a comparable power response. This is due to the approach, in case of IR-UWB, the pulse generator frequency response is not flat for all the UWB band. Nevertheless, the measurement performed with the *reader V2* and the DSO are similar and fully successful. Finally the first reader version *reader V1*, which has the larger jitter of 7.34 ps, presents the worst reading performance. It was not possible to read correctly the resonance positions at high frequency, and the others present shift in frequency of few MHz. This drop of performance is mostly due to the effect of system jitter, but also for the noise generated by the inefficient application of the equivalent time algorithm, due to synchronization issues. It can add noise in the entire tag's bandwidth, and its negative effects are more important at higher frequencies where the tag response has lower amplitude.

These experiments have been performed without taking into account the UWB regulations, which as shown in chapter 2, affect more frequency based readers than IR-UWB.

9. Conclusion

An optimized UWB chipless RFID reader version has been introduced. It was designed to reduce its sampling noise, with improvement at RF hardware and software level. The design of the Xilinx embedded systems was carefully optimized not limited at the reduction of the sampling noise, but also to reduce massively the reading time. The reader is fully configurable in terms of acquisition resolution (equivalent sampling rate), frame duration, and position. The reading time is on the order of few ms depending on chosen parameters. The reader sensitivity was of about -60 dB; this figure is more limited by the ADC resolutions which can be increased using a different model. The reader components cost is estimated at 2,306 € after tax and referred to retail prices. A reduction of about 20/30 % is feasible in an

industrial production. The reader performances and characteristics have been resumed with the table 4.1.

To reduce the reader component cost a pulse generator has been designed, realized and characterized. It is presented in the next chapter, and potentially it can have a retail components cost of about 200 €, which is 5 times lower that the cost of the actual reader pulse generator. As prospective, we are actually working on a more integrated reader version, where the RF front-end, the new pulse generator, and the used components of the SP601 Xilinx evaluation board are in the same board. This should free up the estimated cost from the Xilinx evaluation board, which is of about 420 €, where the employed components have a total cost of about 50 €. The use of a higher performance substrate than FR4 at higher frequencies will also increase the reader capability. A total components retail cost of 1,000 € is feasible. Finally, the design of a low cost UWB antenna is also presented in the next chapter. This was realized to be used in prospective with the new reader version we are currently developing, as so to propose a complete low cost IR-UWB chipless RFID reader solution.

10 References

[BEN 48] BENNETT W. R., ”Spectra of quantized signals,” in *The Bell System Technical Journal*, vol. 27, no. 3, pp. 1-3, July 1948.

[DEL 98] DELIYANNIS T., YICHUANG S., FIDLER J.K., ”Continuous-Time Active Filter Design,” in *CRC Press*, 1998.

[KOS 12] KOSWATTA R.V., KARMAKAR N.C., ”A Novel Reader Architecture Based on UWB Chirp Signal Interrogation for Multiresonator-Based Chipless RFID Tag Reading,” in *IEEE Transaction on Microwave Theory and Technique*, vol. 60, no. 9, pp. 2925-2933, Sept. 2012.

[LIU 13] LIU Q., WANG Y., FATHY A. E., ”Towards Low Cost, High Speed Data Sampling Module for Multifunctional Real-Time UWB Radar,” *IEEE Transaction on Aerospace and Electronic Systems*, vol. 49, pp. 1301-1316, 2013.

[MIC 17] XILINX, “MicroBlaze Processor Reference Guide Embedded Development Kit EDK 13.2”, Online available at: https://www.xilinx.com

[MIT 09] MITZNER K., Complete PCB Design Using OrCAD Capture and PCB Editor, Newnes 2009.

[POP 16] POPPERL M., CARLOWITZ C., VOSSIEK M., et. al.,”An ultra-wideband time domain reflectometry chipless RFID system with higher order modulation schemes,” in *German Microwave Conf (GeMiC*), pp. 401-404, 2016.

[PRE 10] PRERADOVIC S., KARMAKAR N.C.,”UWB Chipless Tag RFID Reader Design,” in *IEEE International conference on RFID-Technology and Applications*, Jun. 2010.

[RAM 16] RAMOS A., PERRET E., RANCE O., et. al. "Temporal Separation Detection for Chipless Depolarizing Frequency-Coded RFID," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 7, pp. 2326-2337, July 2016.

[SMI 17] SMITH P., ”Little Known Characteristics of Phase Noise,” in Analog Devices Application Note AN-741.

[XIL 11a] XILINX, “LogiCORE IP RAM-based Shift Register v11.0,” 2011, Online available at: https://www.xilinx.com

[XIL 11b] XILINX, “LogiCORE IP FIFO Generator v8.2,” 2011, Online available at: https://www.xilinx.com

[XIL 15a] XILINX, “Spartan-6 FPGA Clocking Resources, User Guide”, 2015, Online available at: https://www.xilinx.com

[XIL 15b] XILINX, “Spartan-6 FPGA SelectIO Resources User Guide”, 2015, Online available at: https://www.xilinx.com

[XIL 17a] XILINX, ”LogiCORE IP XPS UART Lite (v1.02.a), ” 2017, Online available at: https://www.xilinx.com

[XIL 17b] XILINX, “XILINX Device Driver API,” 2017, Online available at: https://www.xilinx.com

5

UWB Pulse Generator & Antenna design

1. Introduction

In this chapter the design, realization, and characterization of an UWB pulse generator and a planar UWB antenna is described. The pulse generator was designed to have low jitter and to be low cost, where high performance discrete digital Commercial Off-the-Shelf (COTS) components were employed for its realization. The designed UWB antenna was a planar Vivaldi in the bandwidth 3 – 10 GHz. Both devices have been designed and simulated, the pulse generator with Ansys Electromagnetic suite 17.0, and the antenna with CST Studio Suite 2014. The chapter is organized as follow:

- Section 2 presents the designed pulse generator with simulation and measurement result.
- Section 3 shows the measurement of frequency-coded tags with the designed pulse generator. The pulse generator is also used as emission stage of the optimized reader prototype presented in the chapter 4 to read the same tags.
- Section 4 presents the designed UWB antenna.
- Section 5 draws the conclusion of the chapter.

2. UWB pulse generator design

The optimized reader version presented in chapter 4 uses a commercial pulse generator in the emission stage. Currently the HL9200 from Hyperlabs is obsolete and substituted by the newer version HL9201. It presents similar performance than the predecessor, with a retail cost of 1.295 $. This section presents a home designed fully tunable baseband UWB pulse generator realized with COTS components. It is intended to be low cost and with low

jitter. It is made of high speed logic gates and comparators, and it is compliant with current mode logic (CML) digital standard. The pulse emitted power and bandwidth are tunable showing high flexibility. This advantage simplifies the design of the downstream shaping network to be compliant with international UWB regulations. A differential output with a very low jitter is demonstrated.

2.1. Introduction to pulse generator UWB design

UWB technology is exploited in a variety of applications, from radar for tracking and localization, to short pulse communication [FON 04]. An UWB radar transmits a train of UWB pulses in the direction of a target, and then measures the backscattered signals. These sources of information are used to recover the target position and shape. For short pulse communication applications, time or frequency-division multiplexing algorithms are used. Both are real-time implementation [FON 04], and usually adopt diode based receivers, such as a frequency converter, to recover the data in baseband. Because of the receiver characteristics, a high reproducibility of the transmitting UWB pulse is not required. Therefore, a time-gated oscillator is generally employed as UWB pulse generator. Besides pulse position modulation (PPM), it is possible to use pulse amplitude modulation (PAM) where the pulse generator output amplitude is attenuated depending on the transmitting binary code [MOO 12].

In order to reduce the fabrication costs, most of UWB radars are based on equivalent-time algorithm that permits to achieve effective time resolution in order of few picoseconds [WAN 12]. With this approach, the reproducibility of the UWB transmitting pulse is a key parameter, and therefore the pulse generator cannot be a simple time-gated oscillator. A baseband UWB pulse generator, hereafter B-UWB-PG, needs to be employed. It is capable of generating a Gaussian pulse that can after be derived in time domain, of different orders, with a dedicated downstream circuit, depending on the project requirement. This circuit can be formed of only the antenna as a result of its time derivative property [SHA 05].

According to the application, B-UWB-PGs differ in characteristics [ANG 08]. Most are designed with step recovery diode (SRD) and bipolar transistors driven in avalanche mode to generate Gaussian baseband pulse [XIE 06]. Due to the voltage and frequency output characteristics, SRD solution is the most widespread in a variety of applications, from UWB communications to systems characterization [OHW 11- LIJ 12]. The pulse is sub-nanosecond

with high slew rate, i.e. low pulse rise and fall time. The B-UWB-PG is composed of two different circuits in series, a driver and a pulser [HEW 84]. The driver is able to generate a pulse waveform with a duration of several hundred of nanosecond. The pulser exploits the junction impedance transition of the diode to generate the UWB pulse. This solution can provide a pulse repetition frequency (PRF) in the order of few MHz. The bipolar transistor driven in avalanche mode solution [ANG 07] provides a high voltage output pulse at the expense of a limited PRF, and the requirement of a high voltage supply (around 200 V). It is ideal for long distance radar utilizations.

In [KHE 14], the reproducibility of a step recovery diode (SDR) based pulse generator output is studied through its jitter modeling. It shows how defects in the pulse reproducibility negatively affect more equivalent time sampler systems rather than real time. The random jitter of the complete device (which represents the statistical variation of its propagation delay) increases rapidly most due to the shot noise of the diode. The statistical jitter standard deviation can be in the order of tens of ps [KHE 14]. The UWB chipless RFID systems are suitable for equivalent time receivers thanks to their stationary nature. Thus, the pulse generator is expected low jitter, and also low cost [GAR 15- PER 14]. It ensures an affordable and reliable reader.

It is also possible to design a B-UWB-PG with logic gates where wideband glitches are created. Almost all of them are integrated solution [REJ 13- LEE 14] based on sharped trigger input signals, with limited flexibility in terms of pulse-width and amplitude, with single ended output.

in [SCH 05] is proposed a UWB pulse generator realized with COTS components. Its architecture is based on an inverter and one OR gate, its maximum PRF is of about 100 MHz, the pulse-width is fixed at 500 ps, and it does not have any flexibility in terms of pulse-width and output amplitude. Therefore, the design of the pulse shaping network, to be compliant with international regulations, may be cumbersome. The regulations limit the UWB power emitted according to FCC and ETSI [ETS 17- FCC 16]. Finally, because of its high pulse-width, the signal energy at higher frequency can be excessively low for applications such as UWB Chipless RFID.

To overcome these limitations, a B-UWB-PG made of high frequency discrete logic, is proposed. Indeed nowadays, commercial discrete digital devices with clock frequencies over

10 GHz, are available for applications such as RF test-equipment, and serial data transmission. The proposed solution does not require any input trigger with a sharp rising edge. This feature is a relevant advantage in practical applications, because it can be integrated with low-speed transistor-transistor logic (TTL) and complementary metal-oxide semiconductor (CMOS) technologies based system. It also presents a tunable pulse-width and amplitude feature, which may be exploited to reduce the complexity of the downstream circuit design. The circuit was intentionally designed with COTS components to be easily reproduced and customized around diverse projects requirements. This unloads for an eventual ASIC design which is generally expensive and timing consuming.

2.2. B-UWB-PG architecture

The figure 5.1 shows the schematic of the proposed device. It is mainly composed of two high performance comparators, *A* and *B*, a variable delay generator, and an *AND* gate. According to CML standard, the connections between these devices are balanced. The connection between the comparator *A* and the *IN 1* input of the *AND* gate has a tunable length by soldering 0402 0 Ω surface-mount resistors. It is possible to add three different additional transmission lengths, called *A1-A2-A3*, where *A2 = 2A1*, and *A3 = 2A2* with *A1* equal to 16 mm. The positive input of *A* and the negative input of *B* are connected with the trigger input, and the others two inputs with the positive threshold voltage *VT*.

When the trigger input voltage crosses the threshold, the two comparators switch simultaneously in opposite digital directions. If the trigger input is at *0*, i.e. lower than the threshold, the output of *A* is 0_2 and of *B* is 1_2. Therefore, the output of the *AND* gate is 0_2. When the trigger crosses *VT* during its rising edge, the output of *A* will go to 1_2 and that of *B* to 0_2. However, the inputs of the *AND* gate do not switch simultaneously. The time employed of the signals to go from the output pins of the corresponding comparator to the input pins of the *AND* gate, depends between the others; from the fixed delay blocks length *A1-A2-A3* for *IN1* if employed, and from the delay generator for *IN2*. The modification of these parameters lets the two inputs of the AND gate having the same logical value 1_2 for a tunable and short period of time. It produces a glitch at the gate output, which is the generated pulse. The *AND* gate presents a pin called *VR* that is able to modulate continuously output amplitude. Its absolute amplitude variation was experimentally found between 0.6 V with the minimum at 0.03 V for *VR* equals -1.2 V, and the maximum for *VR* equals 0.4 V.

The evaluation board of the proposed pulse generator is shown in figure 5.2. Its size is 8.5 cm × 7 cm, and it is a 4 layers board manufactured on low-cost FR4 substrate.

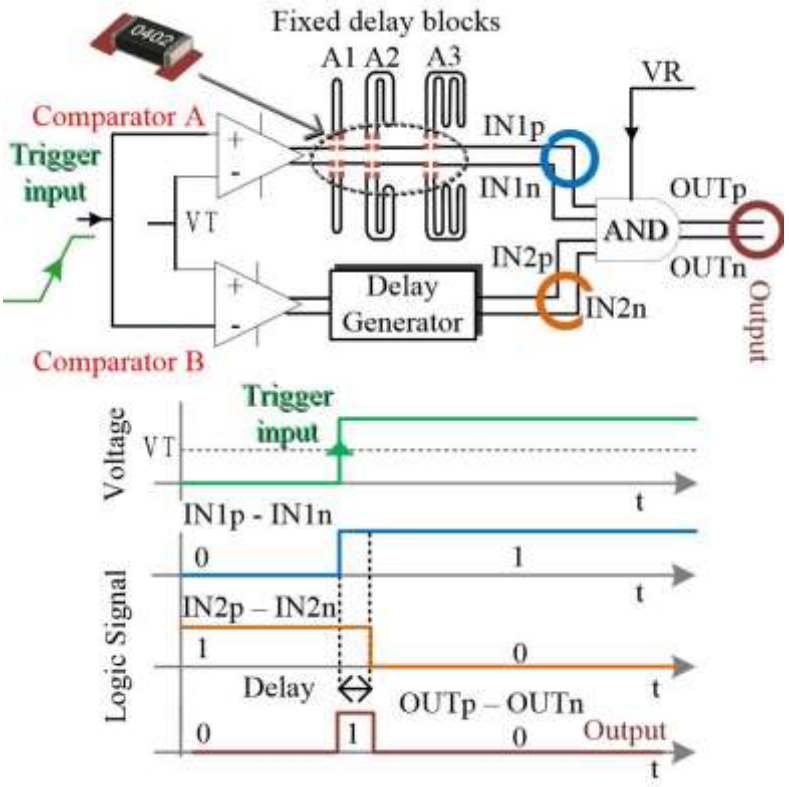


Figure 5.1. *B-UWB-PG principle schematic. After a trigger event (rising edge), the comparator A switches from 0_2 to 1_2, the comparator B from 1_2 to 0_2. Tuning the delay generator the AND gate has its two inputs with the same logical value 1 for a short period of time. It creates a glitch, i.e. a baseband UWB pulse.*

The selected comparator was the HMC675LP3E from Analog Devices, which can outputs a signal with rise and fall times of 27 ps and 18 ps respectively. It presents a deterministic jitter of 2 ps, a random jitter standard deviation of only 0.2 ps, and a balance output compatible with the CML digital standard. The delay generator is the Analog Devices HMC856LC5 with a rise and fall time respectively of 20 ps and 18 ps. It is compatible with the CML standard and presents a balance input and output. Its propagation delay is of 255 ps with an additional digitally controlled delay ranging from 0 to 93 ps, with 3 ps of resolution. The AND gate is the Analog Devices HMC722LCRC, its output rise and fall time is of 19 ps and 18 ps. It has a deterministic jitter of 2 ps and a random jitter of 0.2 ps. All the

components were chosen for their performance in terms of jitter and output rise and fall time (high slew-rate).

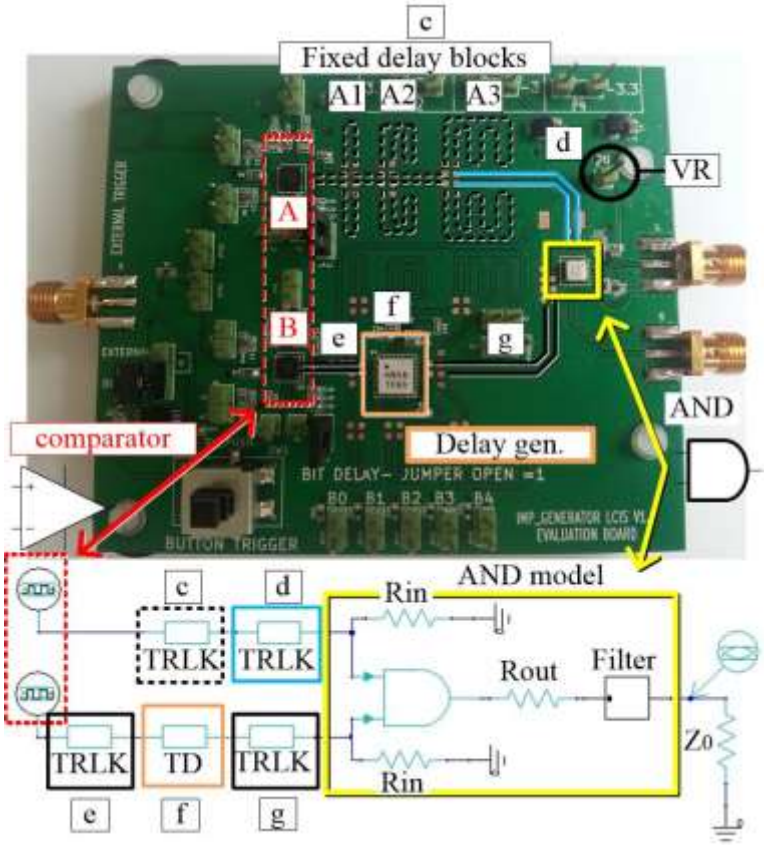


Figure 5.2. *B-UWB-PG evaluation board. This 4-layer FR4 PCB presents three different external power voltage values, 3 V,-3 V and -3.3 V. Through a jumper, the trigger could be external or entrusted on a push button. The delay of the delay generator is imposed by five jumpers. The output is balance and once DC coupled, it is capable to generate two differential output pulses. The pin called VR is used to modulate the output amplitude.*

The balanced interconnections are realized with differential parallel grounded coplanar waveguide (GCPW) transmission lines. The glitch signal, i.e. the output of the B-UWB-PG, is required to have high slew rate and pulse-width in the order of tens of picoseconds, this to ensure large -10 dB bandwidth over UWB (3.1-10.6 GHz). The retail cost after tax of the main pulse generator components is shown in table 5.1. The total cost with the delay generator is of about 381 €. The delay generator is the most expensive component, and worth 184 €. If the fine variable output pulse-width tuning characteristic is not needed, its use is not indispensable. Thus, a lower price pulse generator with a retail cost after tax of the main components of 200 € may be designed.

Pulse generator retail cost after tax	
Component	**Retail Cost after tax (2017 (Digikey))**
Comparator HMC675LP3E	35€ × 2
Delay generator (HMC856LC5)	184 €
AND gate (HMC722LCRC)	127 €
Total cost with delay generator	381 €
Total cost without delay generator	197 €

Table 5.1. *Components retail cost after tax of the presenting pulse generator.*

Playing with the blocks A1-A2-A3 for the connection between comparator *A* and *AND* gate, and also with the delay generator, it is possible to obtain a pulse with a Full Width at Half Maximum (FWHM) (pulse-width) ranging from 325 ps to 60 ps with resolution as low as 3 ps. The delay added with the blocks *A1-A2-A3* is respectively of about 100 ps, 200 ps, and 400 ps. The PRF is limited only from the pulse-width and the input bandwidth of the comparator. The latter has an input bandwidth of 10 GHz, while the maximum pulse-width is of 325 ps. In case the input trigger has a duty-cycle of 50 % then the PRF is approximately,

$$PRF = min(10\ GHz,\ \frac{1}{2PW})), \qquad [5.1]$$

where *PW* is the pulse-width. For *PW* equals to 325 ps the *PRF* is of 1.53 GHz, while for *PW* equals to 60 ps the PRF is of 8.3 GHz. The limit expressed from the equation [5.1] may be increased having a trigger signal with higher duty-cycle.

2.3. B-UWB-PG simulation model

2.3.1. Block description

In figure 5.1 is shown the simulation model of the pulse generator prototype realized using Ansys Electromagnetic suite 17.0. The output of the two high performance comparators was emulated using two eye sources. They are capable of transmitting two trains of pulses, with rise and fall time equal to the comparator specification. Moreover a source of jitter with Gaussian PDF has been added. The chosen standard deviation of 2 ps is higher than the value reported in the data sheet of the comparators. This choice can be justified thinking of real applications, where many factors such as environmental conditions, impedance mismatching, and crosstalk, may increase the effective jitter of the electronics devices [MIT 09].

The transmission lines between the comparators output and the *AND* inputs were modeled with *TRLK* blocks. They are transmission line where all the fundamental parameters are supposed not dispersive. A variable takes into consideration the different lengths of blocks *A1-A2-A3,* and was implemented with the *TRLK* called *c*. The *TRLK* of 53.04 mm, called *d,* takes into account the length of the lines which connects the comparator A, and the corresponding *AND* gate input, after the blocks *A1-A2-A3*. The connection between the output of *B* and input of the delay generator is represented with the *TRLK* block called *e,* which has a length of 12.23 mm. The *TRLK* block called *g* of 35.5 mm for the connection between the output of delay generator and the other input of *AND* gate. Another variable counts for the delay generator propagation and tunable delay, and was implemented using a *TD* block, which is an ideal transmission line defined through its impedance characteristics and its time delay.

The *AND* gate was modeled using a simple ideal threshold model written in Verilog-AMS, where AMS is for Analog and Mixed Signal Extension. Three 50 Ω resistors for input and output impedances, and finally a 5th order Gaussian low pass filter with bandwidth of 10.84 GHz. This figure was obtained exploiting the well-known relationship between filter output rise time at ideal step input, and filter bandwidth reported in chapter four equation [4.7] [DEL 98]. The output rise time was the one of the *AND* gate data sheet, multiplied for an empiric factor of 1.6 to be converted from 20-80 % to 10-90%. In figure 5.2, *Z0* represent an ideal 50 Ω load. The AND gate output jitter was added in post processing using Matlab, with a Gaussian PDF with 2 ps standard deviation from the Ansys transient simulation issue. For simplicity all the connections between the different components were single instead of balanced.

In figure 5.3 is shown the eye diagram of the simulation model output tuning the variable that models the delay generator. The color bar represents the vertical histogram results of the eye diagram in logarithmic scale. It was realized over 300 of pulse realizations with Matlab. The *TRLK* called *c* was fixed at 32 mm (*A2*) while the variable representing the delay generator was varying between the discrete values of: 279 ps (255 ps + 24 ps), 285 ps (255 ps + 30 ps), 300 ps (255 ps + 45 ps), 315 ps (255 ps + 60 ps), and 348 ps (255 ps + 93 ps). The smaller pulse-width of figure 5.3 of about 30 ps corresponds to the minimum delay imposed of 279 ps, and the bigger pulse-width of about 100 ps for the maximum delay of 348 ps. In the simulation model, the effect of the output amplitude variation using the pin *VR* was implemented, but not reported because it only varies linearly the output amplitude without

affecting the system performance. From figure 5.3 for the signals with a pulse-width under 50 ps, the amplitude also decreases.

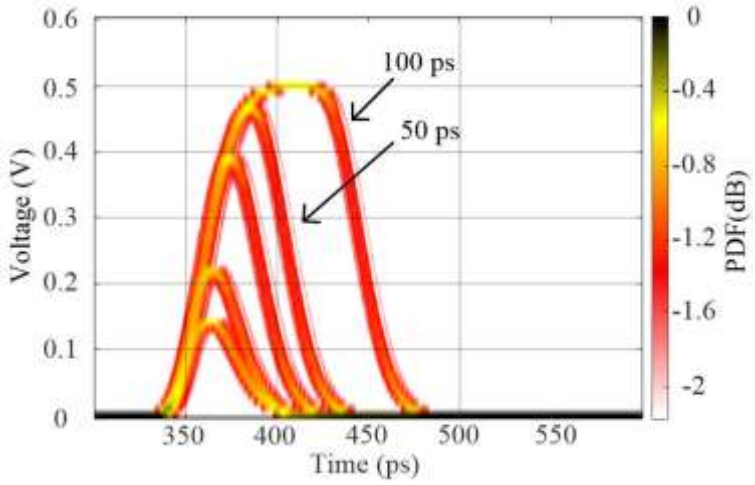


Figure 5.3. *Eye diagram of the simulation model in figure 5.2 obtained tuning the variable which models the delay generator. It was realized over 300 of pulse realizations, where the jitter of the AND gate output was added from the Ansys transient simulation results, in post processing with Matlab.*

2.3.2. Noise rejection

The use of high performance comparators in terms of low rise and fall time is indispensable in practical applications. This because the digital logic devices employed do not have hysteresis capability. Therefore, their input-output characteristic is a static non-linear function, where the dynamic effect is only due to parasitic components. The proposed prototype is designed to be integrated with onset UWB systems, where it may share the same PCB with other blocks of circuit. The proposing prototype is composed of transmission lines with a length in the order of few centimeters between the comparators output and the AND gate input. Thus it may suffer from crosstalk effects. At that scope different simulations have been performed making use of the model in Fig. 5.2.

The crosstalk effects have been emulated with two sinusoid voltage generator called Vup and Vdown. They were inserted at the output of the two eye sources that simulate the output of the two comparators. The amplitude of the Vup and Vdown were fixed at 40 mV, while the frequency was varied from few GHz to tens of GHz. The B-UWB-PG was simulated with a fixed configuration, corresponding to a pulse-width of approximately 90 ps. the simulation was carried out acting on the eye sources rise and fall time. First they were settled to 27 and

18 ps corresponding with the characteristics of the two actual comparators employed. The corresponding simulation results are shown in Fig 5.4 (a). Then the eye sources rise and fall time have been settled to 1 ns, which can correspond to a rise and fall time of TTL and CMOS devices. The corresponding simulation results are shown in Fig. 5.4 (b). In case of the lower rise and fall time (27/18 ps) (Fig. 5.4 (a)) a high rejection at crosstalk effect is demonstrated. In case of higher rise and fall time (1 ns) the B-UWB-PG output has an increased jitter due to the crosstalk for the lower frequency values of Vup and Vdown. On the contrary for higher frequency values, the B-UWB-PG output distortion is prominent. Thus, the simulation results validate the use of high performance comparators with low output rise and fall time ((27/18 ps)).

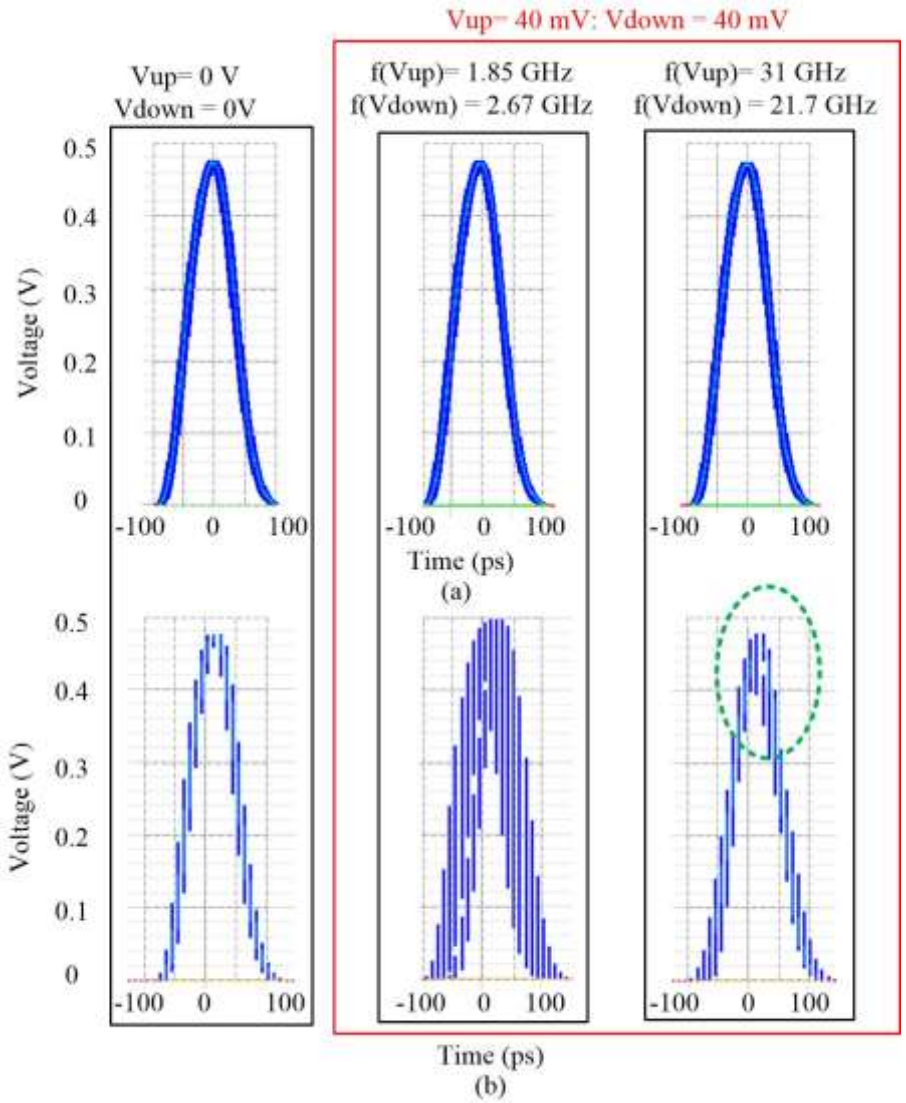


Figure 5.4. *Simulation of crosstalk effect on the proposed B-UWB-PG. (a) Simulated eye diagrams of the B-UWB-PG output in case eye sources rise and fall time of 27 ps and 18 ps respectively. They correspond to the output rise and fall time of the actual comparators used for the design of the B-UWB-PG. The B-UWB-PG was simulated with a fixed configuration, corresponding to a pulse-width of approximately 90 ps. (b) Simulated eye diagrams of the B-UWB-PG output in case of eye sources with rise and fall time of 1 ns, which can correspond to a rise and fall time of either a TTL or a CMOS device.*

2.4. Measurement results

2.4.1. B-UWB-PG output characterization

As the B-UWB-PG presents a balanced output, two pulses with inverted polarity can be generated. According to the CML digital standard, the DC component of the two output pins

differs. It is of 0 V for the negative single output and -0.4 V for the positive output, when no pulse is created. However, it is possible to force the DC component of both pins at 0 V once AC coupled to ground.

Measurement of the positive and the negative output voltages of the proposed pulse generator, with different FWHM with VR equals 0 V, are shown respectively in figure 5.5 (a), and figure 5.5 (b). The variation of pulse amplitude with pulse-width is starting from FWHM of around 90 ps, while it was of 50 ps from simulation results of figure 5.3. This can due to filtering effect at higher frequency of the realized PCB.

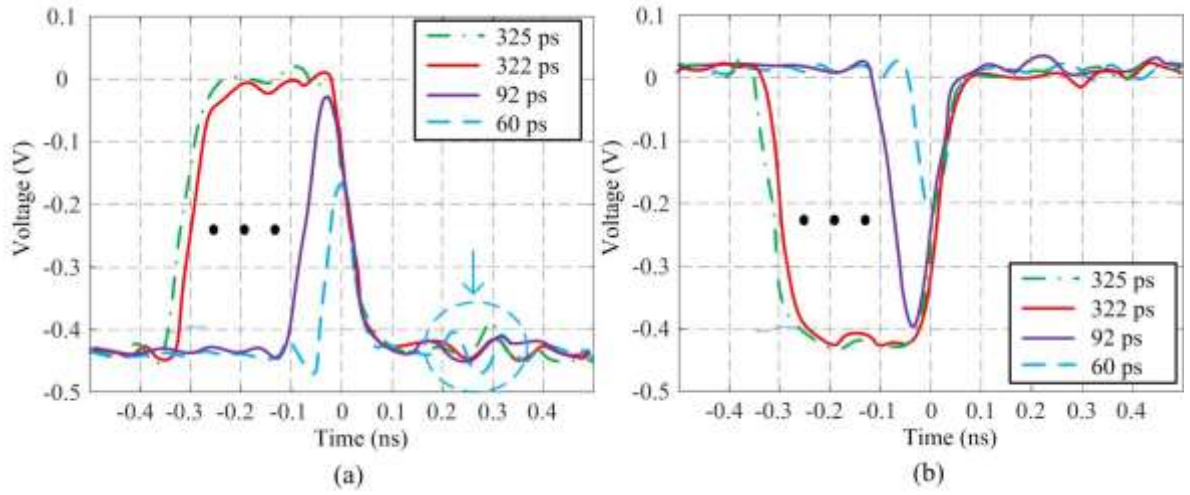


Figure 5.5. *Single output of the B-UWB-PG evaluation board measured for different delay generator configuration, and transmission line length (A1-A2-A3) with VR equals to 0 V. In (a) and (b) respectively the measured of the positive and negative balanced output of the AND gate, both referred to ground.*

The corresponding PSD over MHz of the positive output voltage (figure 5.5 (a)) is shown in figure 5.6. It was estimated with Matlab supposing a PRF of 1 MHz, which is that of the optimized reader of chapter 4. Its absolute values can be increased of a maximum of 2.5 dB varying *VR* from 0 to the maximum value of 0.4 V. As expected, the maximum response is at 0 Hz, independently from the pulse-width [GHA 07]. The -10 dB bandwidth for the 60 ps is of about 10 GHz. To modulate the position of peaks and the valleys along with the frequency range, it is essential to derivate in time the response of the pulse generator

From figure 5.5 the shape of the pulses can be approximated with a rectangular function for bigger FWHM, while Gaussian for smaller FWHM. The module of the spectrum of a rectangle of width ΔT and amplitude A is,

$$|G(f)| = |A\Delta T sinc(\pi f \Delta T)|, \quad [5.2]$$

and its -10dB bandwidth is approximately

$$f_{-10dB} = \frac{0.73}{\Delta T}. \quad [5.3]$$

From figure 5.5 (a) the bigger pulse FWHM is of 325 ps, and according to equation [5.3], it should have a -10 dB bandwidth of 2.25 GHz, instead the measured is smaller and of 2.2 GHz. The error respect to 2.25 GHz is of only 2.2%, which validate the rectangular pulse assumption. The narrower pulse shapes can be approximated with Gaussian pulses with the expression,

$$V(t) = \frac{A}{\sqrt{2\pi\sigma^2}} e^{\left(-\frac{t^2}{2\sigma^2}\right)}. \quad [5.4]$$

where *A* is the maximum of the pulse, and σ is the shape factor (standard deviation). For simplicity we suppose the curve centered in 0 s. The module of its spectrum is,

$$|G(f)| = \left| Ae^{\left(-\frac{(2\pi f\sigma)^2}{2}\right)} \right|, \quad [5.5]$$

and its -10dB bandwidth is,

$$f_{-10dB} = \frac{\sqrt{2.303}}{2\pi\sigma}. \quad [5.6]$$

For Gaussian pulse the relationship between FWHM and shape factor is,

$$FWHM = 2\sqrt{2ln2}\sigma \approx 2.3548\sigma. \quad [5.7]$$

Therefore combining equations [5.6] and [5.7] we obtain,

$$f_{-10dB} = \frac{0.5687}{FWHM}. \quad [5.8]$$

From figure 5.5 (a) the minimum FWHM is of about 60 ps. Using the equation [5.8] its -10 dB bandwidth should be of about 9.48 GHz. The measured value differs of only 5.5 % and is of about 10.2 GHz. It can be demonstrated that this error is due to the ringing effect underlined in figure 5.5 (a). For the case of FWHM equals 92 ps, from equation [5.8] the -10 dB bandwidth should be of 6.18 GHz but it is of 6 GHz. This small difference is reduced respect to the previous case due to the almost absence of pulse ringing [MIT 09].

In figure 5.7 is shown the measurement results for the negative (black dashed lines) and positive (red lines) outputs of the proposed B-UWB-PG, for two FWHM configurations, respectively of 235 ps and 126 ps varying linearly the voltage applied to the pin *VR* from 0.4 V and -1.2 V. The figure 5.7 shows a dynamic variation for each port from 0.6 V to 0.03 V.

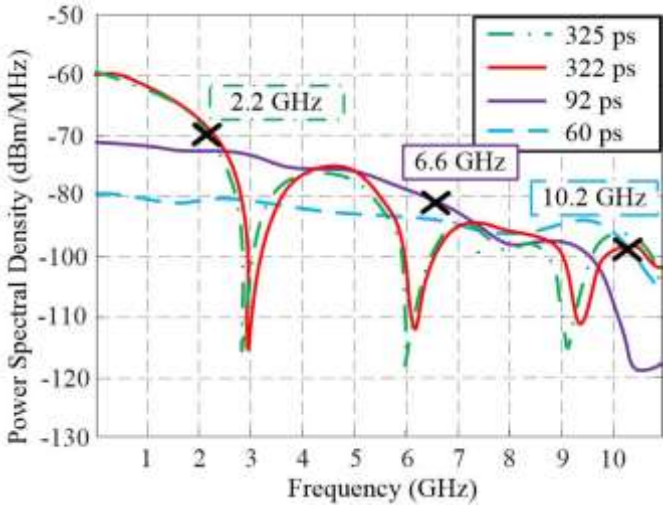


Figure 5.6. *Calculated PSD/MHz with a PRF of 1 MHz of the signals plotted in figure 5.5 (a) with a PRF of 1 MHz.*

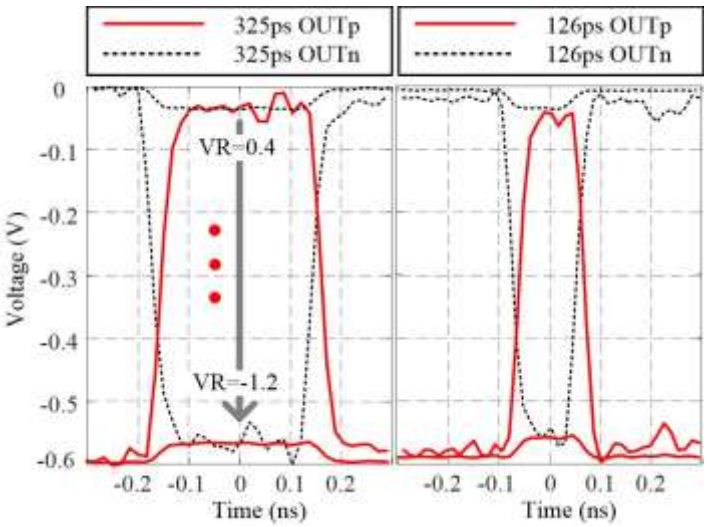


Figure 5.7. *measurement results for the negative (black dashed curves) and positive (red curves) outputs of the proposed B-UWB-PG, for two FWHM configurations, respectively of 235 ps and 126 ps varying linearly the tension applied to the pin VR from 04 V to -1.2 V.*

2.4.2. B-UWB-PG jitter characterization

The jitter of the pulse generator was measured using the bench shown in figure 5.8 (a). It is composed of the DSO Agilent DSO91204A (with 12 GHz bandwidth and 40 GSa/s sampling rate), the Agilent 1134A high performance probe, and an arbitrary function generator (AFG) AFG3102C from Tektronix.

The AFG is used to trigger the pulse generator using a periodic square signal of 1 MHz (PRF). The probe is placed at the input of the comparator A, and used as a trigger for the DSO, which is connected to the pulse generator outputs. The eye diagram for a pulse with a FWHM of around 60 ps over 1 k pulses is shown in figure 5.8 (b). The pulse-width duration presents a standard deviation of 1.6 ps and peak-to-peak of 8.33 ps. The fall and rise time (20-80%) standard deviation is of 1 ps and 0.8 ps respectively. These values are in accordance with the jitter specifications of the high performance components employed. In order to compare with a commercial solution, the jitter standard deviation of the commercial solution HL9200 from Hyperlabs, employed as transmitting stage of the readers in chapters 3 and 4, is from datasheet of 3 ps. The presenting solution shows the lower jitter results, and with a more performing RF board substrate it would further decrease.

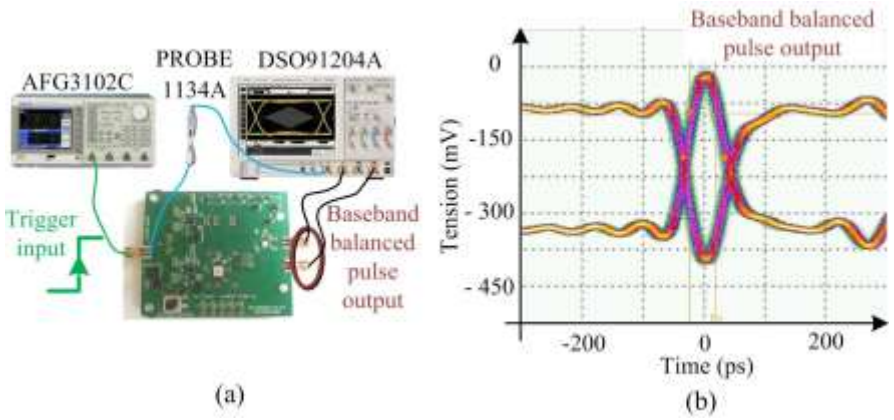


Figure 5.8. *Deterministic period jitter measurement with eye diagram using the 12 GHz Agilent DSO91204A, and the 7 GHz Agilent 1134A probe as trigger reference for the oscilloscope. (a) Test bench. (b) Measurement results.*

2.5. Output stage consideration

2.5.1. Output power enhancement

The maximum PSD/MHz of each single B-UWB-PG output, with VR equal to 0 V, is ranging from -59 dBm/MHz to -80 dBm/MHz (see figure 5.6), for a pulse-width of 325 ps and 60 ps respectively. This low level of power is due to the low duty cycle used, i.e. low PRF. Increasing the PRF will results in a higher PSD/MHz. To increase the output power, the low cost Analog Devices HMC788 gain block amplifier was used as a final stage of the proposed B-UWB-PG. It is characterized by an operative band from DC to 10 GHz, a gain of 14 dB, an input compression point of 6 dBm, and a noise figure (NF) of 7 dB. An evaluation board for the amplifier was fabricated on the same FR4 substrate of the pulse generator. The measurement test bench is shown in figure 5.9 where the amplifier is connected in cascade with one output of the B-UWB-PG. The measured output voltage is shown in figure 5.10 (a), while its estimated PSD/MHz is in figure 5.10 (b). The proposed solution shows an output amplitude ranging from 1.1 V to 2.3 V with VR yet equals to 0 V. Comparing the same results without the output amplifier, the – 10 dB level of the pulses decreases. It was caused in majority by the negative decay of the gain of the amplifier with frequency.

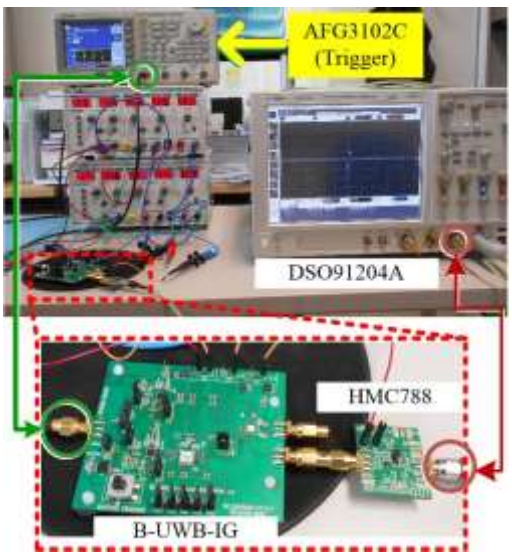


Figure 5.9. *Measurement setup of a single output of the B-UWB-PG amplified with the evaluation board for the HMC788 gain block amplifier.*

2.5.2. UWB shaping network

In order to be compliant with FCC regulation in terms of power mask, the output of the proposed B-UWB-PG needs to be shaped [FCC 16]. In the regulation, the reported value of

PSD/MHz is a measure of EIRP, and therefore the characteristics of the transmitting antenna have to be taken into account. Outside of the 3.1-10.6 GHz band, the allowed PSD is strictly limited, especially between 1 and 2 GHz. The UWB antenna itself can be used to shape the pulse [TAM 12], or the antenna in combination with a band pass filter [MEN 05].

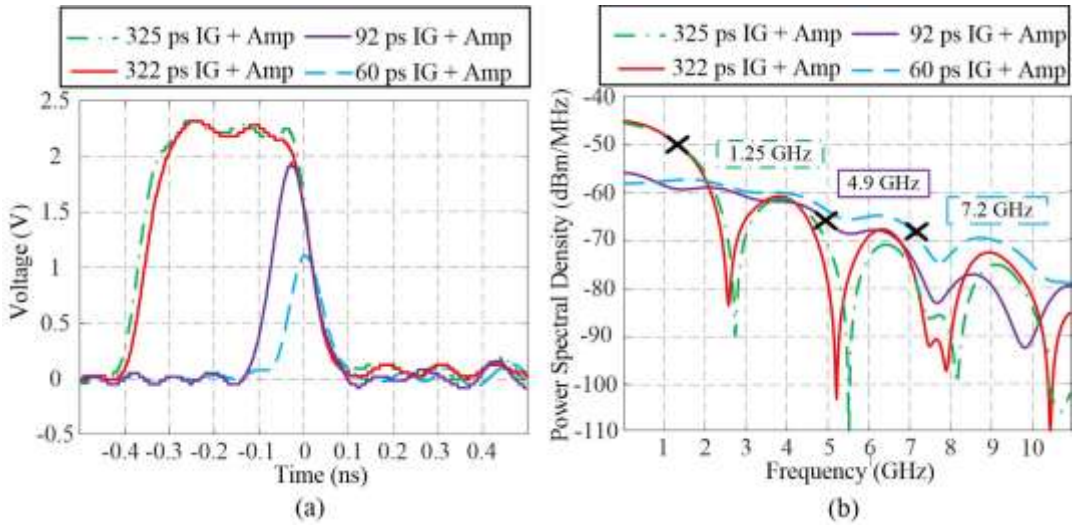


Figure 5.10. *Measurement results of the B-UWB-PG with the gain block amplifier (see figure 5.9) in time (a). (b) Calculated PSD/MHz with a PRF of 1 MHz.*

Typically a monocycle pulse, which is the result of a first derivation of a Gaussian pulse, is used at the transmitting port of commercial radars, such as the Novelda NVA-R640 kit. The corresponding maximum PSD is not located at zero frequency. By combining the balanced outputs of the proposed B-UWB-PG pulse generator, it is possible to generate a monocycle Gaussian pulse. In this way the B-UWB-PG can be used with most commercial UWB antennas while respecting regulation.

Figure 5.11 (a) shows a schematic of the combination process. The monocyle is obtained by doing the summation of two Gaussian pulses: one positive and one negative, where the latter being slightly delayed in time. The wideband combiner Mini-Circuits ZFRSC-123 was used to perform the summation. The time shift between the two pulses was done using two cables with two different overall lengths; in this case a 21 mm coaxial connector which adds a small delay to the bottom chain (see figure 5.11 (b)). In order to compensate the insertion loss of the combiner, which is of about 10 dB, the same HMC788 amplifier was employed as a final amplification stage. The results are in blue, compared with the NVA-R640 commercial

radar pulse output in black dashed in figure 5.12. The PRF was increased to 48 MHz, which corresponds to that one of the Novelda NVA-R640 kit. Both responses are similar, showing that the B-UWB-PG can be easily tuned to provide a monocycle pulse. In case of our prototype, the pin VR was at 0 V and therefore the output amplitude could be yet increased using the maximum value of 0.4 V. The higher power levels of figure 5.12, compared with figure 5.10 (b), is due to the higher PRF.

The wideband combiner Mini-Circuits ZFRSC-123 has a high insertion loss due to its large band, from DC to 12 GHz. With a lower insertion loss combiner, and using 0.4 V for *VR*, it would be possible to eliminate the final amplifier. In figure 5.12 is also shown, in red dash dot line the distinct single outputs measurement from the B-UWB-PG, called OUTP and OUTN from figure 5.11 (a), executed with VR equals to 0.4 V. They were summed in post processing with a delay of 14 ps, and finally attenuated of 3dB to emulate an ideal -3 dB insertion loss combiner. The signal in time and frequency presents almost the same trend as the case with the amplifier (blue line).

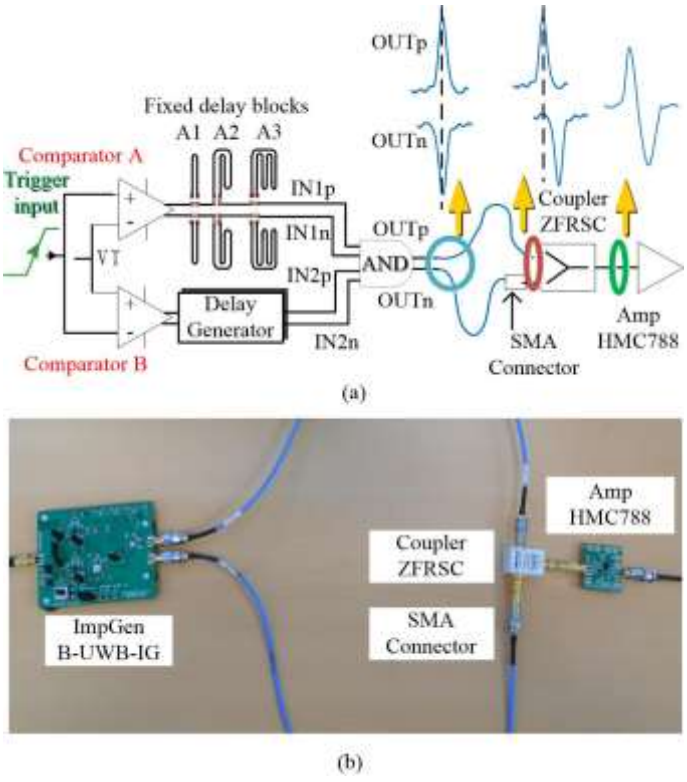


Figure 5.11. *(a) Schematic and (b) photograph of the monocycle pulse generator obtained from the combination of the balanced outputs of the proposed B-UWB-PG, using a power combiner, and a short delay line.*

As final example, the same configuration of figure 5.11 was used, where the combiner was substituted with the Mini-Circuits ZFSC-2-9G+ band pass combiner. The filtering effect of the new combiner is clearly visible in figure 5.13 (a). The estimated PSD/MHz is shown in Figure 5.13 (b), where the gain of the Satimo QH2000 was taken into account for the EIRP estimation. The PRF was of 1 MHz, and the FCC average power mask for indoor applications is also shown on the figure. As it can be observed, the final emitted pulse is fully compliant with regulation. Moreover the output power could also be further increased.

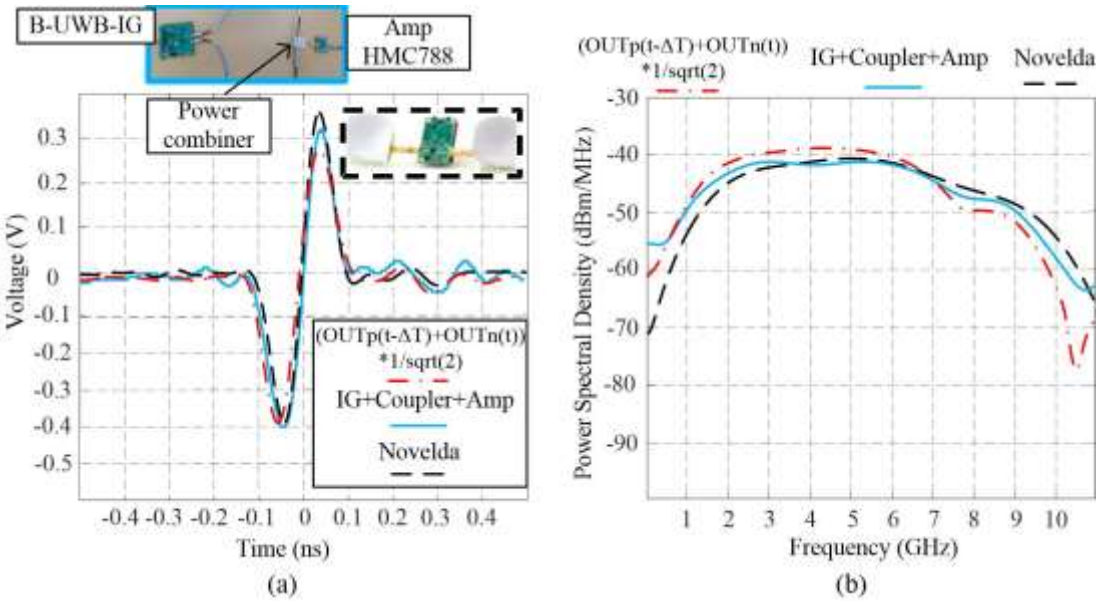


Figure 5.12. *In blue measurement of the proposed pulse generator with the wideband combiner ZFRSC-123 from Mini-Circuit and the HMC788 amplifier (see figure 5.11) with VR equal to 0 V. In red dash dot line, the distinct single output measurement from the B-UWB-PG, called OUTP and OUTN from figure 5.11 (a), and summed in post processing with a delay of 14 ps executed with VR equal to 0.4 V. Finally in black dashed the Novelda NVA-R640 development kit pulse output. (a) Signal in time domain. (b) Calculated signal in frequency domain (PSD/MHz), where the PRF was that one of the Novelda NVA-R640 and corresponding to 48 MHz.*

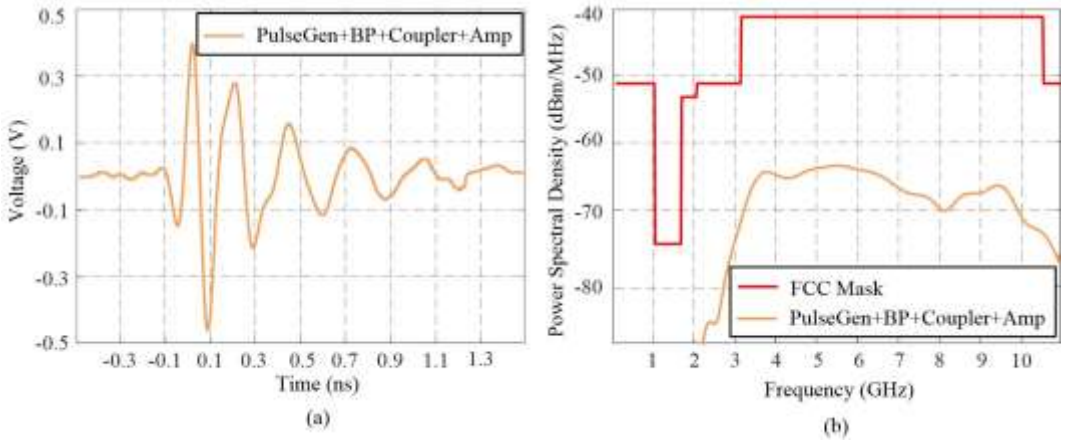


Figure 5.13. *(a) Measurement in time domain of the setup of figure 5.11 (b) with the ZFSC-2-9G+ band pass combiner. (b) Calculated PSD/MHz with a PRF of 1 MHz taking into account the gain of the Satimo QH2000 antenna, and FCC average power mask for UWB indoor applications.*

2.6. Conclusion

This section has presented a potentially low jitter fully tunable baseband pulse generator for real and equivalent-time UWB applications. COTS components and low-cost FR4 substrate has been used. The generator is based on high frequency logic gates and two comparators. It can be triggered by a low-frequency TTL-CMOS digital signal. A delay generator and variable length transmission lines permit to tune the pulse-width from 325 ps to 60 ps. A pin on the *AND* gate allow for amplitude modulation. The measured random period jitter over 1 k cycles is in the order of 2 ps. The generator outputs two pulses that can be combined to create a commonly used monocycle pulse. The proposed solution is flexible and permits to design a shaping network with COTS components to respect regulations. The use of COTS component is a big advantage compared to integrated solution, because its implementation, modification, and redesign is easier and low-cost. Also, it may be integrated in large onset UWB system. The actual design can be improved using digitally controlled RF switches instead of 0 Ω resistors to select between *A1-A2-A3*. A bigger permittivity substrate, with better performance at higher frequency, can be used to reduce the B-UWB-PG dimensions and jitter. The presenting solution has a lower jitter than the commercial HL9200 solutions, and from figure 5.12 and figure 5.13, it may easily respect the UWB regulations.

This pulse generator solution can be used as an emitted stage of the two readers presented in the chapter 3 and 4. It will decrease the reader realization cost and the system jitter. The PRF of the pulse affects the resulting PSD/MHz, and the readers of chapter 3 and

4 have a PRF of only 1 MHz. Note that, this will results in a lower PSD/MHz for UWB regulations, and therefore a further amplification stage may be added at the output of the pulse generator.

In the next section, the designed pulse generator will be used first to read chipless tag, with the high performance DSO in the reception stage, and after with the reader presented in chapter 4.

3 UWB pulse generator frequency-coded tag measurement

The designed B-UWB-PG was tested to read the REP frequency-coded tag introduced in [VEN 13], and used along with the entire manuscript to validate the different presented reader prototypes.

The B-UWB-PG was tested with two different configurations. The first exploits a single output port of the B-UWB-PG with the HMC788 gain block amplifier as final stage. It is shown in figure 5.14 and was discussed in sub-section 2.5.1. The second configuration was discussed in sub-section 2.5.2. It makes the use of the wideband combiner ZFRSC-123 from Mini-Circuits to combines the two single outputs of the B-UWB-PG to create a monocycle. The HMC788 was employed as a final amplifier to compensate the combiner insertion loss.

The B-UWB-PG was first tested with the high performance DSO, and after with the optimized reader version discussed in chapter 4.

3.1 Pulse generator measurement result

The B-UWB-PG was connected as the emission stage of an IR-UWB reader based with test equipment. The DSO Agilent DSO91204A was in reception, while the antenna was the dual access Satimo QH2000 with the tag placed at 10 cm. The bench is shown in figure 5.14. The B-UWB-PG was configured with a single output amplified with the HMC788, and with a FWHM of about 90 ps as shown in figure 5.10. The DSO was settled with an averaging of 64, and the B-UWB-PG was triggered with the AFG AFG3102C. The measurement results are shown in figure 5.15. All the measured tag frequency peaks, which correspond to the first mode resonant frequencies of the tags, are in the correct positions.

The same B-UWB-PG configuration was tested with the optimized reader version presented in chapter 4, it was used in place of the DSO. Because the reader was designed around the HL9200 that has higher output power, in the reader reception was connected the LNA Mini-Circuits TVA-82-213A+ with one attenuator of 18 dB. The external LNA decreases the ADC quantization noise (chapter 4 section 2), resulting in higher reader ADC equivalent bits number. The LNA has a typical gain of 25 dB between 0.8 and 21 GHz, adding the attenuator, the corresponding gain is reduce to 7 dB but enough to retrieve the tag ID. To avoid using this external preamplifier, it is sufficient to increase the number of ADC bits (currently they are 9 over 1.5 V_{p-p}), or to use the same driver employed in the reader version of chapter 3 to add gain at the output of the S/H amplifier. The corresponding bench is shown in figure 5.16, where the reader was settled with the maximum averaging of 512. The corresponding measurement results are shown in figure 5.17. All the tag frequency peaks are in the expected position (resonant frequencies). Less accurate are the results concerning the last peak, it was due to the use of the external preamplifier, and the pulse generator spectrum that shows attenuation at higher frequencies.

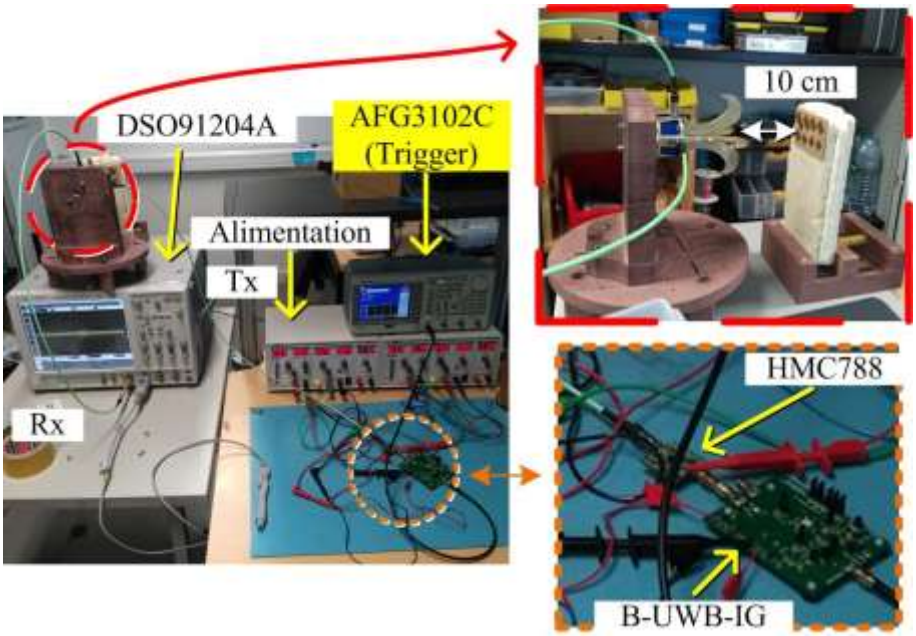


Figure 5.14. *Bench of tag measurement in practical environment with the DSO DSO91204A in reception. The function generator AFG3102C was used as trigger for the B-UWB-PG. One single output of the B-UWB-PG was used as emission stage, along with the block gain amplifier HMC788. The B-UWB-PG was settled for a FWHM of about 90 ps as shown in figure 5.10. The tag was placed at 10 cm from the dual access antenna, SatimoQH2000. The measurement is in cross-polarization and the DSO averaging was of 64.*

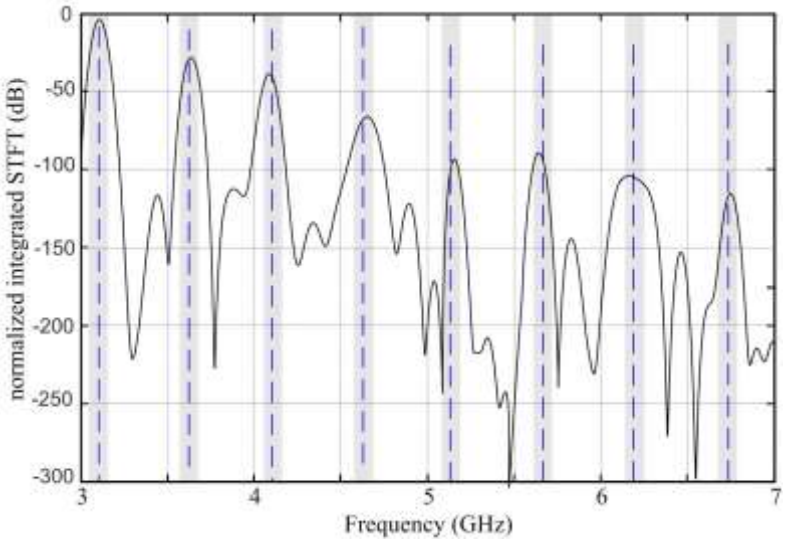


Figure 5.15. *Tag measurement result of bench on figure 5.14. All the tag frequency peaks are in the expected position (resonant frequencies).*

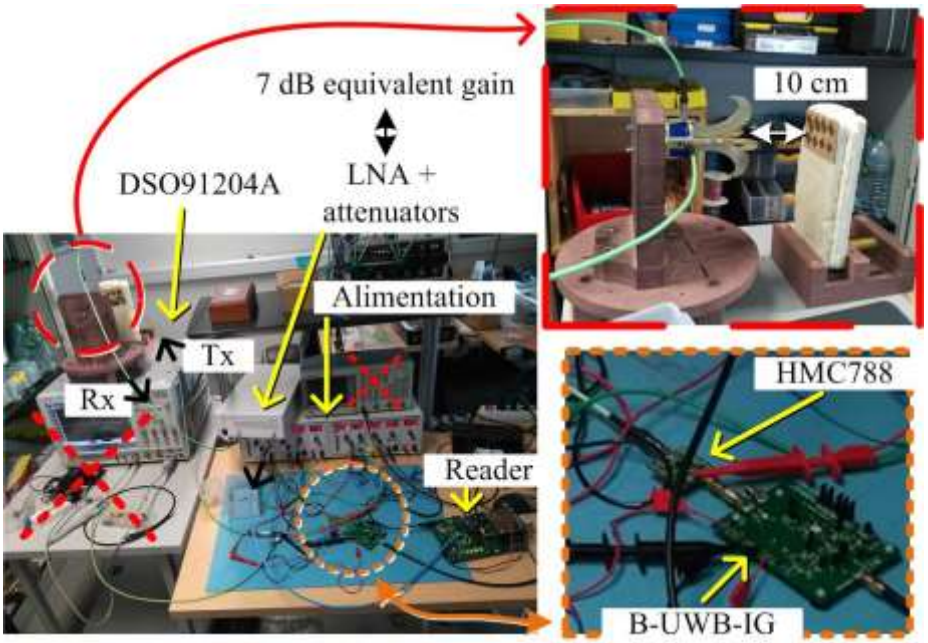


Figure 5.16. *Bench of tag measurement in practical environment with the optimized reader of chapter 4 in reception. In reception the LNA Mini-Circuits TVA-82-213A+ with one attenuator of 18 dB, were interposed between the reader RF input and one port of the antenna. One single output of the B-UWB-PG was used as emission stage, along with the block gain amplifier HMC788. The B-UWB-PG as settled for a FWHM of about 90 ps as shown in figure 5.10. The tag was placed at 10 cm from the dual access antenna, SatimoQH2000. The measurement is in cross-polarization and the reader averaging was of 512.*

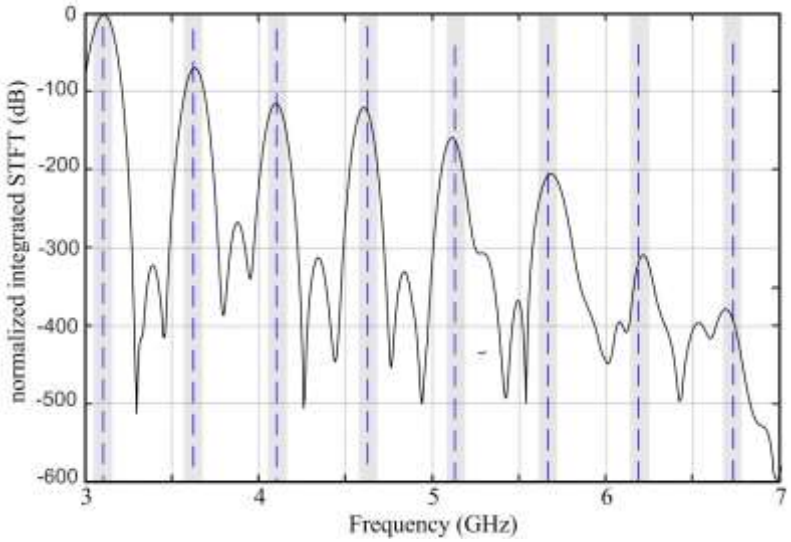


Figure 5.17. *Tag measurement result of bench on figure 5.16. All the tag frequency peaks are in the expected position (resonant frequencies). The high frequency peak apexes are less accurate. It was due to the use of an external preamplifier, and the pulse generator spectrum that shows attenuation at higher frequencies.*

The second configuration for the B-UWB-PG was based on the monocycle creation shown in figure 5.12. The same measurements with the DSO and the optimized reader of chapter 4 were performed. Respect to the bench of figure 5.14 and 5.16 the only difference was the B-UWB-PG configuration, therefore they are not shown. The measurement results are in figure 5.18. Both DSO and reader approach show correct reading results.

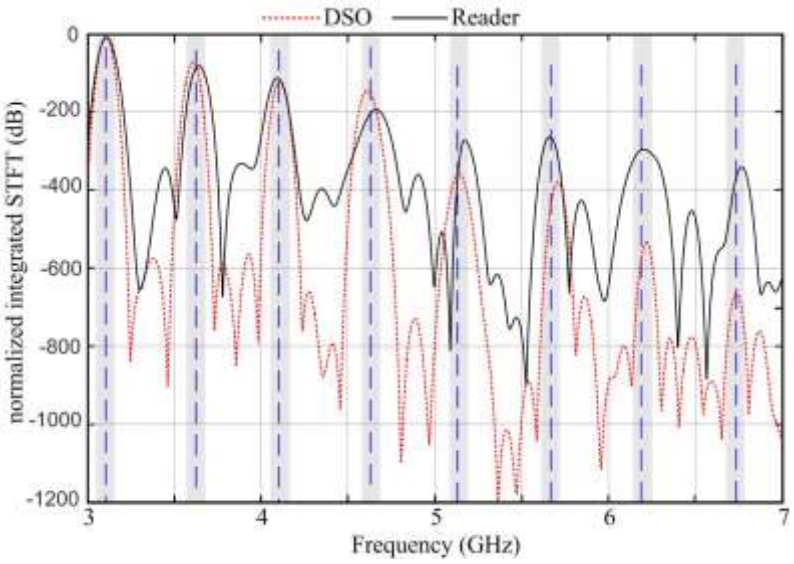


Figure 5.18. *Tag measurement result with second B-UWB-PG configuration. All the tag frequency peaks are in the expected position (resonant frequencies)*

3.2 Conclusion

This section has presented the potentiality of the designed B-UWB-PG as emission stage of an UWB chipless RFID reader based on IR-UWB approach. The measurements were performed in turn with a high performance DSO and the optimized reader of chapter 4 in reception in a practical environment. The two reading systems were able to read the tag introduced in [VEN 13], where the reader needed an external preamplifier of only 7 dB of gain to reduce the reader ADC quantization noise. Either the use of an ADC with higher resolution (bit quantity), or the use of a driver with a settled gain between the reader S/H amplifier and the analog ADC input, will free up the reader by the use of the external preamplifier.

4 UWB antenna design

The readers presented in chapter 3 and 4 use commercial ultra large-band antenna, such as the Satimo QH2000. It is an open boundary quad-ridge horns antenna, working between the bandwidth 2 – 32 GHz, with a boresight gain between 10 and 14 dBi in the UWB 3.1 – 10.6 GHz. The price of this type of antenna is of around 6 k€. For the deployment of chipless technology, the reader should be low cost. A printed antenna may represent a good candidate, where the feeding network should be simple to realize. An unbalanced antenna

access point, such as an SMA connector, is preferable because compatible with microstrip technology often used in PCB layout.

Many different antennas can be used at the scope. First a selection based on the polarization has to be done. Because the cross-polarization principle is used, the reader should be equipped with two linear polarized antennas, placed in cross-configuration attaining to decrease the coupling as much as possible. In a UWB chipless RFID system, the read range is limited and since the low power signal reflected back from the tag, and its liner behavior, the receiving antennas should have a high gain to maximize the link-budget (equation [2.7] in chapter 2). The transmitting antenna may have a more isotropic character, this because both regulations, FCC and ETSI [FCC 16- ETS 17], discriminated maximum emitted power with the EIRP. On the other side a lower gain may generate a higher antennas coupling (leakage), hence both antennas for transmission and reception are preferable having high gain.

Between all the planar printed UWB linear polarized antennas, the most employed are the monopole, dipole, Bow-Tie, Log-Periodic, and Vivaldi. The monopole and dipole antennas have a low gain that is hardly higher than 5 dBi in all the band of interest (3.1 – 10.6 GHz) [RAM 16]. The Bow-Tie is composed of two triangular metal sheets, fed with classical aperture coupling technique employing a broad band stub. It has a quasi-omnidirectional radiation pattern along the H-plane, and therefore a limited gain [WIE 09]. The Log-Periodic antenna has high bandwidth. It is a multi-resonant antenna, and therefore has a variable group delay over its bandwidth. This makes reading time-based tags difficult because the antennas tends to spread out the transmitting or receiving UWB pulse, creating ringing effects [WIE 09]. The Vivaldi antenna is a frequency independent antenna, therefore has reduced ringing effects. It has high gain and bandwidth, and is easy to be realized.

A Vivaldi antenna was fabricated on a high performance laminate Rogers R03003 0.76 mm substrate, which at 10 GHz has a relatively dielectric constant of 3, and a dissipation factor tan δ of 0.0010. For the design, CST Studio Suite 2014 was used. The antenna has a balance radiative structure on the bottom formed of an exponential tapered slot line, and an unbalanced fed structure based on microstrip. According to figure 5.19, their coupling arrangement is composed of the radial stub on top layer, coupled with the circular cavity on the bottom. In table 5.2 are shown the corresponding design dimensions, and in figure 5.19 the CST design. The exponential tapered slot line has been modified during design to reduce

the overall antenna dimension, therefore its profile does not obey with the well-known equations reported in [KAH 15].

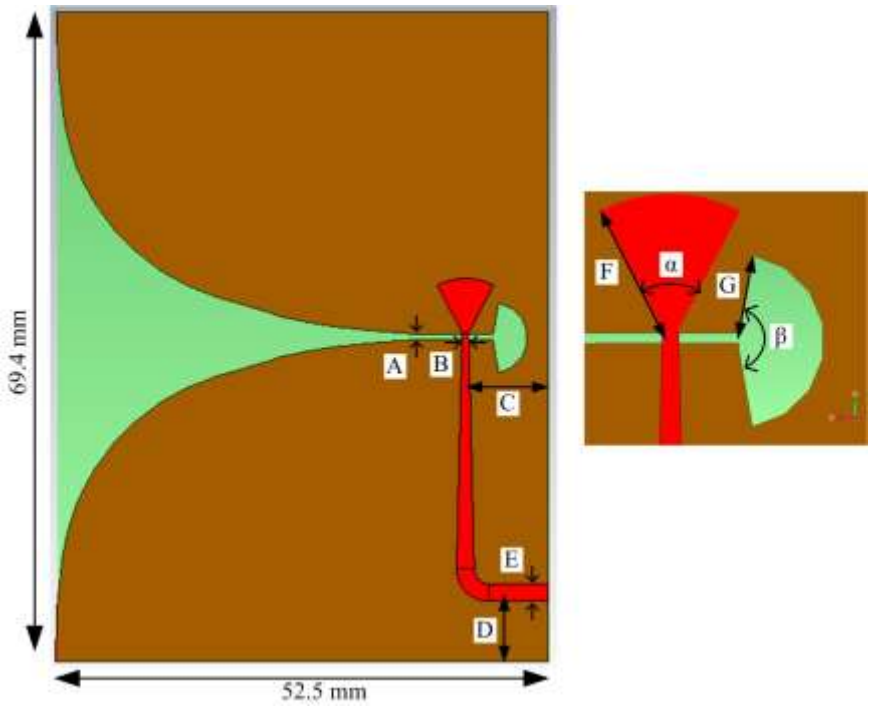


Figure 5.19. *Realized Vivaldi antenna.*

A	B	C	D	E	F	G	α	β
0.42 mm	0.70 mm	8.92 mm	7.48 mm	1.89 mm	6.52 mm	3.67 mm	0.304π rad	0.885π rad

Table 5.2. *Corresponding dimensions of figure 5.19.*

A photograph of the realized antenna, and the measurement of its reflection coefficient are shown respectively in In figure 5.20 (a) and In figure 5.20 (b). The reflection coefficient is lower than -10 dB in the entire tested band 3.1 – 10 GHz. In figure 5.21 is shown the simulated far field gain at 5.5 GHz where its maximum is of 7.33 dBi. In figure 5.21 (a) the polar chart in the E-plane is represented. It shows an aperture of 49°, and a side lobe level of -8.9 dB. In figure 5.21 (b) the polar chart in the H-plane, it shows an aperture of 92°, and a side lobe level of -7 dB.

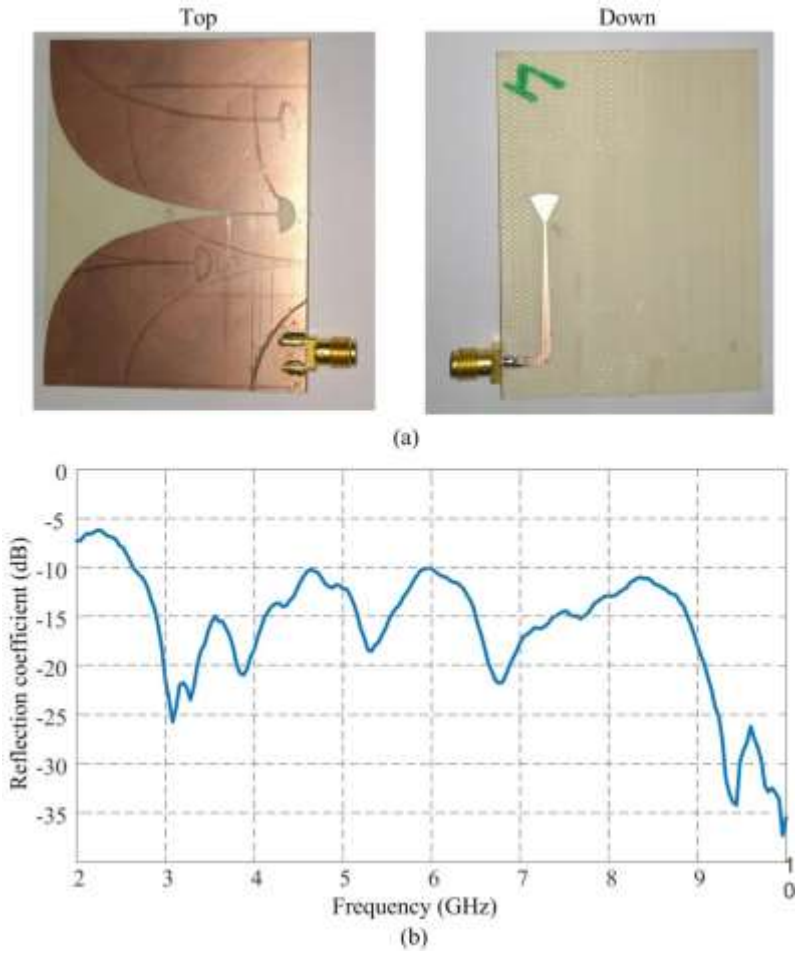


Figure 5.20. *Photograph and reflection coefficient measurement of the realized UWB Vivaldi antenna whose design is in figure 5.19.*

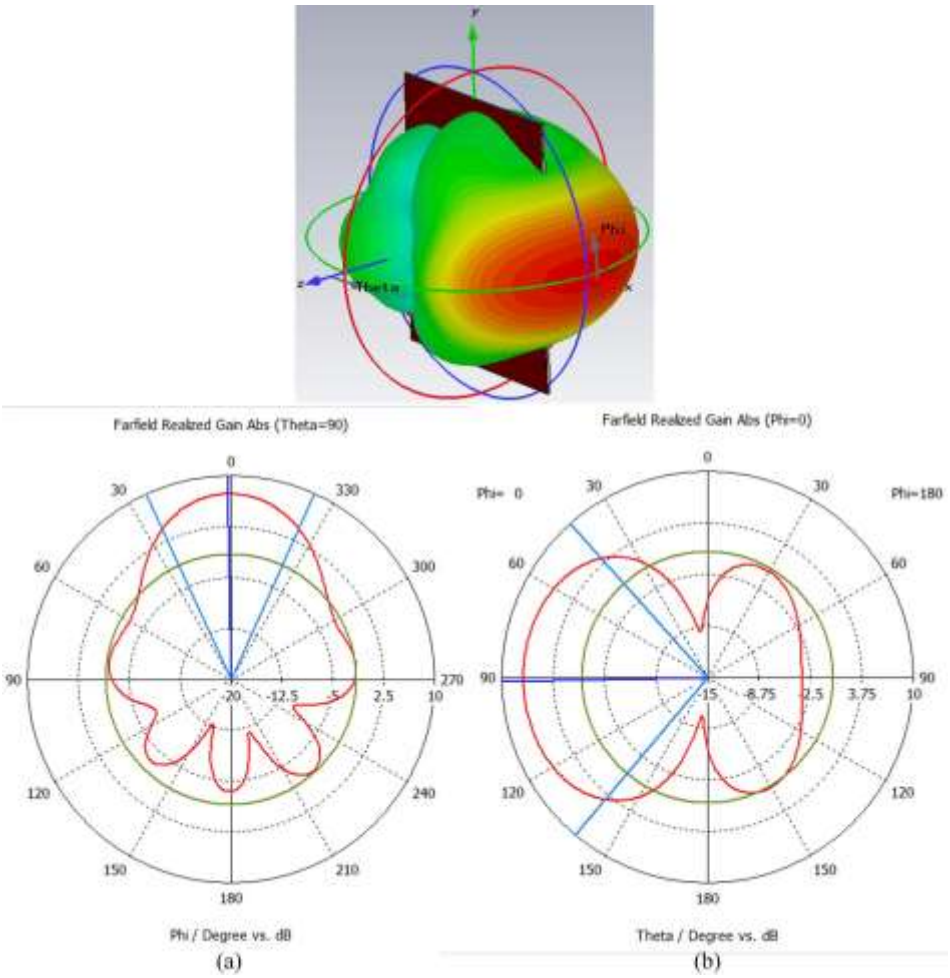


Figure 5.21. *Simulated far field gain at 5.5 GHz of the antenna in figure 5.19. (a) Polar chart of the gain in the E-plane. (b) Polar chart of the gain in the H-plane.*

5. Conclusion

The design, realization, and characterization of a low jitter UWB pulse generator was depicted in the section 5.2. It is based on COTS components, and represents a low cost solution. Its main components retail cost after tax varying from 384 € to about 197 €. The more expensive solution provides a fine tuning of the output pulse-width, which is not possible for the latter that misses the delay generator chip. A prototype of the more expensive solution was realized on FR4 and characterized. It shows a low random jitter of 2 ps of standard deviation over 1,000 cycles. To be compliant with UWB regulations, some shaping network configurations have been proposed. Its design has been facilitated

exploiting the pulse generator flexibility. It may be used as the emitter stage of the UWB chipless RFID readers designed in chapter 3 and 4, as demonstrated in section 3.

A planar Vivaldi UWB antenna have been realized and described in section 4. It shows a reflection coefficient lower than –10 dB in the entire band 3 – 10 GHz. It was designed to have an unbalanced alimentation structure as so to be used with the proposed readers.

In the next chapter, the problem of reading UWB chipless RFID tags, independently from their orientation, is faced. A technique based on polarization diversity is proposed. A reading system based on test equipment was realized as proof of concept, and after the same principle was applied to the reader presented in chapter 4.

5.5 References

[ANG 07] DE ANGELIS A., DIONIGI M., MOSCHITTA A., et al., ”A low-cost ultra-wideband indoor ranging technique,” in *IEEE Instrument and Measurement Technology Conference IMTC 2017*, pp. 1-6, 2007.

[ANG 08] DE ANGELIS A., DIONIGI M., GIGLIETTI R., et al., “Experimental low-cost short pulse generators”, in *IEEE Instrument and Measurement Technology Conference*, pp. 259-564, 2008.

[DEL 98] DELIYANNIS T., YICHUANG S., FIDLER J.K., Continuous-Time Active Filter Design, CRC Press, 1998

[ETS 17] ETSI E. 302 065 v1.2.1, Electromagnetic compatibility and Radio spectrum Matters (ERM); Short Range Devices (SRD) using Ultra Wide Band technology (UWB) for communication purposes; harmonized EN covering the essential requirements of article 3.2 of the R&TTE Directive, accessed on 2017. [Online]. Available: http://www.etsi.org/.

[FCC 16] FCC, ”Title 47, Chapter 1, Subchapter A, Part 15, Subpart F 2016,” accessed on 2017. [Online]. Available: http://www.ecfr.gov/.

[FON 04] FONTANA R. J., ”Recent system applications of short-pulse ultra-wideband (UWB) technology,” in *IEEE Transaction on Microwave Theory and Technique*, vol. 54, no 9, pp. 2087-2104, 2004.

[GAR 15] GARBATI M., SIRAGUSA R., PERRET E., et al., ”Low cost low sampling noise UWB Chipless RFID reader,” in *IEEE MTT-S International Microwave Symposium (IMS)*, pp. 1-4, 2015.

[GHA 07] GHAVAMI M., MICHAEL L. B., KOHNO R., Ultra-Wideband Signals and Systems in Communication Engineering, John Wiley & Sons, 2007.

[HEW 84] HEWLETT PACKARD, ”Pulse and waveform generation with step recovery diodes,” in Application Notes AN918. 1984.

[KHE 14] A. KHEIRDOOST, G. MORADI, E. ELKHOLY, et al., ”Modeling and Jitter Improvement of SRD-Based Ultra-Wideband Pulse Generator,” in *IEEE Transaction on Microwave Theory and Technique*, vol. 62, no. 8, pp. 1736-1747, Aug. 2014.

[LEE 14] LEE K. K., LANDE T. S., ”A Wireless-Powered IR-UWB Transmitter for Long-Range Passive RFID Tags in 90-nm CMOS,” in *IEEE Transaction on Circuits Systems II*, vol.61, no. 11, pp. 870-874, 2014.

[LIJ 12] LI Q., JIANG W., XU Y., et al., ”Analysis and design of wide-band comb generator based on SRD,” in *IEEE International Conference on Material and Manufacturing Technology* (ICMMT), pp. 1-2, 2012.

[MEN 05] MENZEL W., RAHMAN TITO M. S., ZHU L., ”Low-loss ultra-wideband (UWB) filters using suspended stripline,” in *IEEE Microwave Conference Proceedings*, 2005.

[MIT 09] MITZNER K., Complete PCB Design Using OrCAD Capture and PCB Editor, Newnes 2009.

[MOO 12] MOORFELD R., LU Y., FINGER A., ”Energy detection with optimal symbol constellation for M-PAM in UWB fading channels,” in *EEE International Conference on Ultra-Wideband* (ICUWB), vol. 54, pp. 397-401, 2012.

[OHW 11] OH S., WENTZLOFF D. D., ”A step recovery diode based UWB transmitter for low-cost impulse generation,” in *EEE International Conference on Ultra-Wideband* (ICUWB), pp. 63-67, 2011.

[PER 14] PERRET E., Radio Frequency Identification and Sensors: From RFID to Chipless RFID, London, UK: Wiley-ISTE, 2014.

[RAM 16] RAMOS A., LAZARO A., GIRBAU D., et al, RFID and Wireless Sensors Using Ultra-Wideband Technology, 1st Edition, ISTE Press, 2016.

[REJ 13] REJA M. M., HAMEED Z., MOEZ K., et al., ”Compact CMOS IR-UWB transmitter using variable-order Gaussian pulse generator,” in *Electronics Letters*, vol.49, no. 16, pp. 1038-1040, 2013.

[SCH 05] SCHWOERER J., MISCOPEIN B., UGUEN B., et al., ”A discrete fully logical and low-cost sub-nanosecond UWB pulse generator,” in *IEEE Annual Conference Wireless and Micrwave Technology*, pp. 43-46, 2005.

[SHA 05] SCHANTZ H. G., The Art and Science of Ultra-Wideband Antennas, Artech House Print on Demand, 2005.

[TAM 12] TAMMAM E., YANG L., ALLAM A., et al. ”Design of a small size UWB antenna with band-rejection characteristics,” in *IEEE Conference on Electronics, Communications and Computers*, pp. 112-117, 2012.

[KAH 15] KAHAR M., MANDAL J., MANDAL M. K., "A compact Vivaldi antenna with microstrip feed line for the 2–18 GHz ultra-wideband applications," 2015 *IEEE Applied Electromagnetics Conference (AEMC),* Guwahati, 2015, pp. 1-2.

[VEN 13] VENA A., PERRET E., TEDJINI S., "A Depolarizing Chipless RFID Tag for Robust Detection and Its FCC Compliant UWB Reading System," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 8, pp. 2982-2994, Aug. 2013.

[WAN 12] WANG Y., "UWB Pulse Radar for Huma Imaging and Doppler Detection Application", Ph.D. dissertation, Univ. Tennessee, Knoxville, Tennessee, 2012.

[WIE 09] WIESBECK W., ADAMIUK G., STURM C., "Basic Properties and Design Principles of UWB Antennas," in Proceedings of the IEEE, vol. 97, no. 2, pp. 372-385, Feb. 2009.

[XIE 06] XIE H. L., WANG X., WANG A., et al., "An ultra-low-power low-cost Gaussian impulse generator for UWB applications," in *IEEE International Conference on Solid-State and Integrated Circuit Technology Proceedings* (CSICT), pp. 1814-1820, 2006.

6

UWB Chipless RFID Reading System Independent of Tag Orientation

1. Introduction

The UWB chipless RFID tags need to be aligned with the reader antennas, in order to maximize the reading capability, when a cross-polarization approach is used. The reading is therefore tag orientation dependent. In this chapter is proposed a reading technique, based on polarization diversity from the reader part, to obtain a reading which is instead independent of the tag orientation maintaining a cross-polarization configuration. In the first part of the chapter some measurements of chipless RFID tags with state of the art test equipment are shown. After, to read tags independently from their orientation, a modified version of the optimized reader presented in chapter 4 is detailed. The chapter is organized as follows:

- Section 2 introduces the problems of tags reading whatever their orientation from a theoretical prospect.
- Section 3 presents the potentiality of a 4 ports state of the art VNA to perform balanced measurement. The proposing reading technique is introduced and balanced measurements are done with the VNA to read the tags whatever their orientation, in a practical environment.
- Section 4 demonstrates the feasibility of the proposing technique, with a reduced number of measurements (only two), to be used in practical applications.
- Section 5 shows the proposing method applied to the optimized reader of chapter 4, with the addition of some external hardware components. Measurements of tags in practical environment are shown.

- Section 6 draws the conclusion of the chapter.

2. Theory of operation

One of the major drawbacks of UWB chipless RFID systems is the polarization dependence. Most of the proposed tags in literature have to be specifically oriented with the reader, working in linear polarization, and using high directive antennas to maximize the read-range [PER 14]. The tags are isotropic and have, as well as the reader, some discrete directions of maximum radiation. Thus, the tags must be correctly oriented with the reader to maximize the reading. To attain a UWB Chipless RFID system independent from mutual orientation, a dedicated work may involve either the reader or the tag design. Chipless UWB tags with circularly-polarized antennas [SHEN 12], or tags independent of polarization [VEN 12], have been proposed but they do not have the robust detection advantages of working in cross-polarization [VEN 13].

A typical scenario of a tag reading process is shown in figure 6.1. The tag is read in a cross-polarization configuration, and therefore the E-planes of the reader transmitting and receiving antennas are orthogonal, as shown in the figure. The tag is supposed to be aligned with the reader antennas in the direction of maximum backscattering RCS. Then, the tag can be interrogated with different reader antenna orientations, defined by the angle α_T, to characterize the response of the tag. α_T is defined in figure 6.1. It is the angle of the intersect between the reader transmitting antenna E-plane, and the Cartesian coordinate system (x,y) defined in the tag plane. A variation of α_t corresponds to a rotation of the reader antennas. The tag position is defined with β, which is the angle between the x axis and the tag direction. This direction is defined by the straight line parallel to its longer size, and crossing the origin of the Cartesian coordinate system (x,y). The tag on figure 6.1 is the cross-polarized tag presented in [VEN 13], and used to characterize the different reader prototypes in this manuscript.

A model of the tag was realized in CST Studio Suite, and simulated varying α_T between 0 and 90 deg. For simplicity the tag was placed with β equals to 0 deg as shown in figure 6.2. The tag response is shown in figure 6.3, the positions of the eight tag resonant frequencies versus the angle are underlined with gray dashed lines. The STFT algorithm was employed, in post processing with Matlab, to remove the tag structural mode contribution from the simulated tag response [RAM 16]. The tag shows a symmetric response around 45 deg: the

tag maximum response is for α_t of 0 and 90 deg, and the minimum for α_t of 45 deg. The tag ID was correctly retrieved with α_t between 0 and 35 deg, which results are similar to α_t between 55 and 90 deg. For the others directions around 45 deg, the reading was difficult because the tag response amplitude is several dB reduced respect to the more favorable cases (0 and 90 deg).

The simulation performed covers an α_t variation in the first, and the third quadrants of the x,y Cartesian coordinate system (the angle range 0 – 90 deg is equivalent to the range 180 – 270 deg). The behavior of the tag for the second and fourth quadrants, which is with α_t between 90 and 180 deg (equivalent to 270 – 360 deg) gives about the same results due to the tag shape. Thus, the response of a cross-polarized tag is periodic with period of 90 deg. This has been demonstrated in literature, and will be formalized in the section 4.

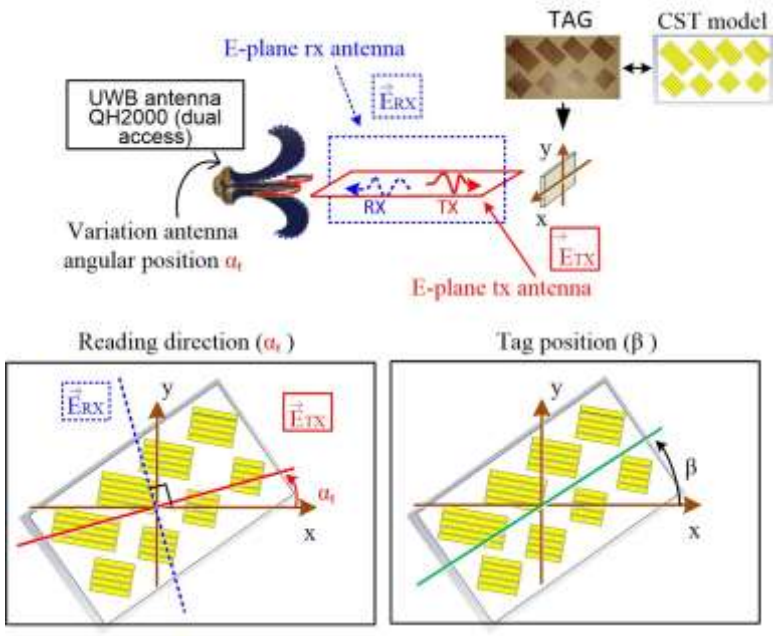


Figure 6.1. *Scenario of a tag reading in cross-polarization configuration, varying the direction of interrogation (α_T). α_T. is the angle of the intersect between the reader transmitting antenna E-plane, and the Cartesian coordinate system (x,y) defined in the tag plane. A variation of α_t corresponds to a rotation of the reader antennas. The tag position is defined with β, which is the angle between the x axis and the tag direction. This direction is defined by the straight green line parallel to its longer sizer, and crossing the origin of the Cartesian coordinate system (x,y)*

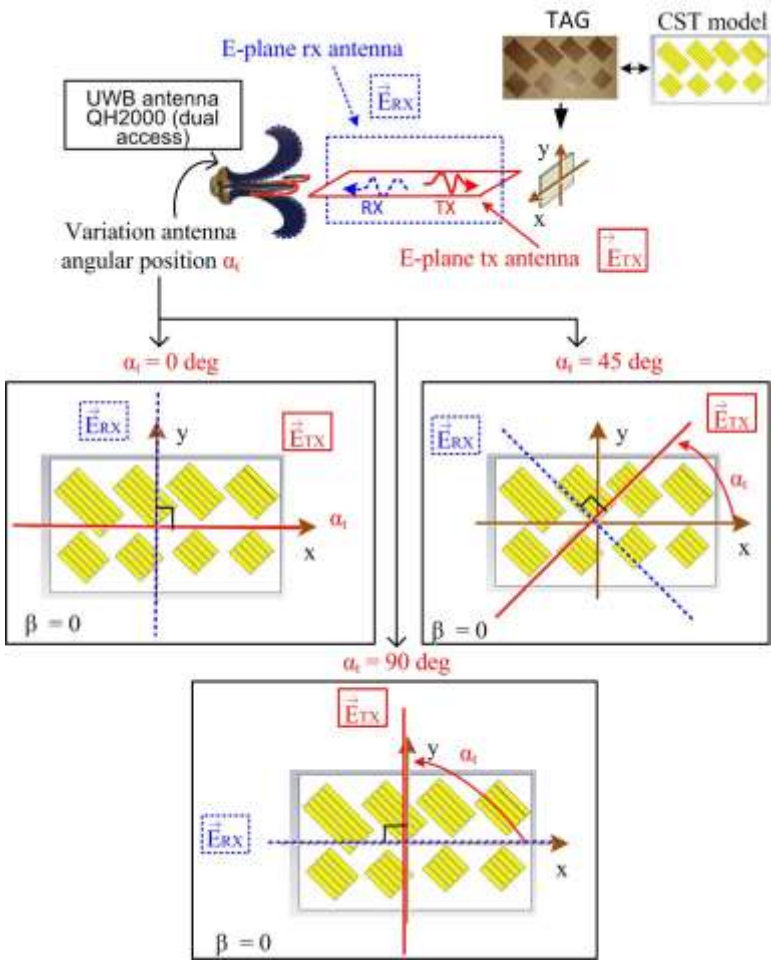


Figure 6.2. *Scenario of a reading of a tag in cross-polarization configuration, varying the direction of interrogation (α_t) with the tag position β equals 0 deg. A CST Studio Suite model of the tag was realized and simulated varying α_t between 0 and 90 deg. The tag was the cross-polarized tag presented in [VEN 13]. It is characterized by eight resonant frequencies in the bandwidth 3 - 7 GHz.*

As have been shown, typically cross-polarized tags have two preferential reading directions [VEN 12] that maximize the antenna (tag) mode cross-polarization RCS, and allow recovering the tag ID in best condition. They are orthogonal and therefore 90 deg distant, and from figure 6.2 and 6.3, they correspond to the case of α_t equals β ± *n* 90 deg, with *n* integer. Between them exists two perpendicular directions of minimum tag response as shown in figure 6.4. When β is 0 deg, they are located in α_t equals 45 and 135 deg (β ± *n* 45 deg, with *n* odd integer). The aim of this thesis is improving the state of the art of UWB chipless RFID reader technology, therefore the orientation problem has been studied in that prospect. The goal is to show a reader that is able to electrically rotate its interrogating

signal, varying α_t, while always receiving in the perpendicular direction (i.e., the reading is always in cross-polarization).

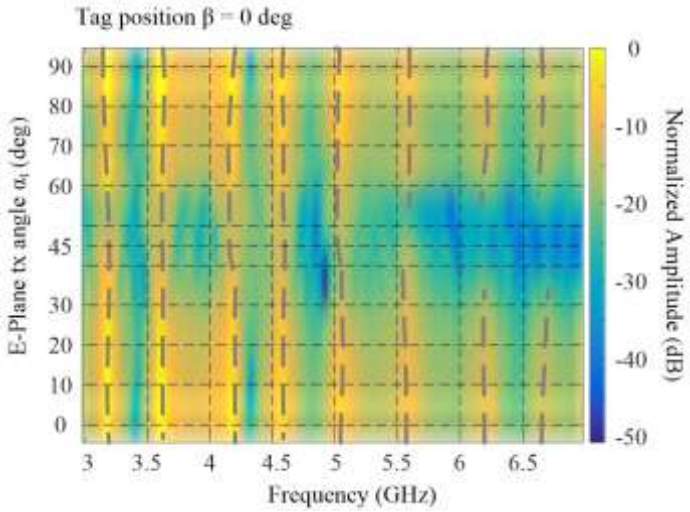


Figure 6.3. *Simulation result of the scenario shown in figure 6.1 with tag placed at β equals to 0 deg. The STFT algorithm was employed in post processing with Matlab to remove the tag structural mode contribution from the simulated tag response. The tag has a symmetrical behavior around the minimum response of α_t equals to 45 deg. The maximum is at 0 and 90 deg. In gray dashed lines the retrieved position of the eight resonant frequencies.*

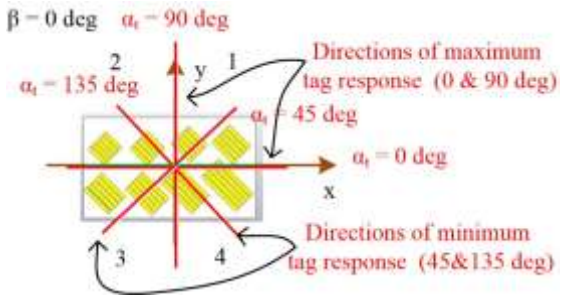


Figure 6.4. *Directions of tag maximum and minimum response for cross polarization reading.*

To read the tag independently from its orientation, one can either sweep either in the interval [0 - 90] deg or in [90 - 180] deg, due to tag response symmetry as shown in figure 6.5. This assures the reading of the tag in the best condition for at least one value of α_t, maximizing the antenna (tag) mode cross-polarization RCS. For simplicity the chapter is

focusing on the interval [0 - 90] deg. This approach has been demonstrated with the use of the 4 ports Agilent VNA N5222A, in balanced measurement configuration. The next section introduces the VNA balanced measurement principle of operation.

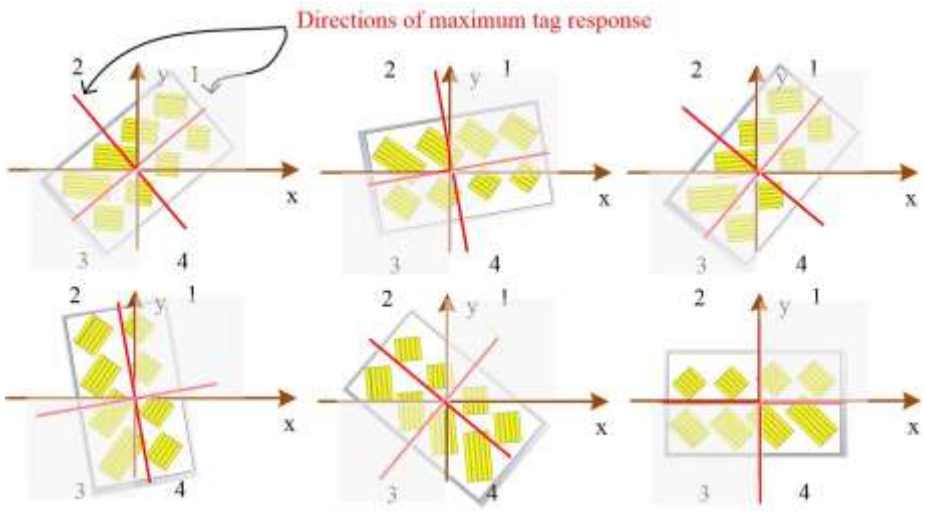


Figure 6.5. *A reading process with α_t varying in the interval [0 - 90] deg corresponds to a sweep in the first and third quadrants of the Cartesian coordinate system (x,y). Whatever the position of the tag, at least for one time, the tag is interrogated along with one of its two preferential reading directions.*

3. VNA balanced measurement

3.1. Variation of the transmitting signal direction α_t

The N5222A VNA is equipped with four physical ports, and it has the possibility to perform balanced measurements in true-mode (real balanced signals) [PNA 16]. The VNA four ports are grouped in two logic ports 1 and 2, where the first is composed of the physical ports 1 and 3, while the logic port 2 with the physical ports 2 and 4, as shown in figure 6.6. The signals at the two logic ports have a common and differential component, which may be defined respectively as in equation [6.1] and [6.2] for the logic port 1, and as in equation [6.3] and [6.4] for the logic port 2.

$$V_{LP1-Common} = \frac{V_1+V_3}{2} \quad [6.1]$$

$$V_{LP1-Diff} = \frac{V_1-V_3}{2} \quad [6.2]$$

$$V_{LP2-Common} = \frac{V_2+V_4}{2} \quad [6.3]$$

$$V_{LP2-Diff} = \frac{V_2-V_4}{2} \quad [6.4]$$

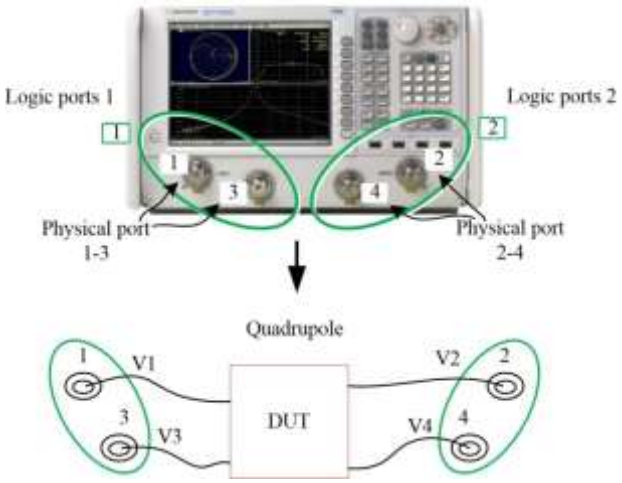


Figure 6.6. *Organization of the VNA physical 4 ports in a balanced measurement configuration. They are arranged with two logic ports, and each associated at two physical ports. The logic port 1 at the physical ports 1 and 3, whereas the logic port 2 with the physical ports 2 and 4.*

It is possible to do common to common (c-c), common to differential (d-c), differential to differential (d-d), and finally differential to common (c-d) S-parameter measurements, from logic port 2 to logic port 1 and vice-versa, where C stand for common and d for differential. A balanced signal, that has a null differential component, is composed of two signals with equal amplitude and phase (equations [6.2], [6.4]). While if the common component is null, the two signals are equal in amplitude and opposite in phase (equation [6.1],[6.3]). Besides balanced to balanced measurement it is possible to perform single to balanced and balanced to single measurement. From figure 6.6, the only difference is that one of the two logic ports is composed of only one physical port. Compared to balanced to balanced, the others have some limitations in true more as shortly explained.

The Satimo QH2000 is a dual access antenna, and therefore can be connected to one of the two logic ports once in balanced configuration. The antenna connected with the logic port 2 (physical ports 2 and 4) is shown in figure 6.7. Each antenna components, vertical and horizontal, will transmit a linear polarized EM signal along with the respective E-planes. The resulting signal towards the tag will be the vector sum between the two linear polarized signals, as shown in figure 6.7. To avoid an interrogating signal with elliptical polarization, the two exiting components of the antenna, V_4 and V_2 have to be in phase or out of phase. If the exiting signals of the logic port 2 are common signals, then the two components have the same phase. Therefore, the interrogating signal will be a linear polarized one in the first and

third quadrants of the Cartesian coordinate system (x,y) (see figure 6.7). The transmitting angle α_t will be equal to 45 deg because the two components have also the same amplitude. In case the transmitting signal is differential, their two components will be out of phase, and α_t will be equal to 135 deg. As previously said at the end of last section, the selected interval of variation of α_t to interrogate the tag was in between [0 - 90] deg. So to vary α_t in that interval, keeping a linear polarized transmitting signal, the amplitude of the two components V_4 and V_2 need to be varied, while keeping the same phase.

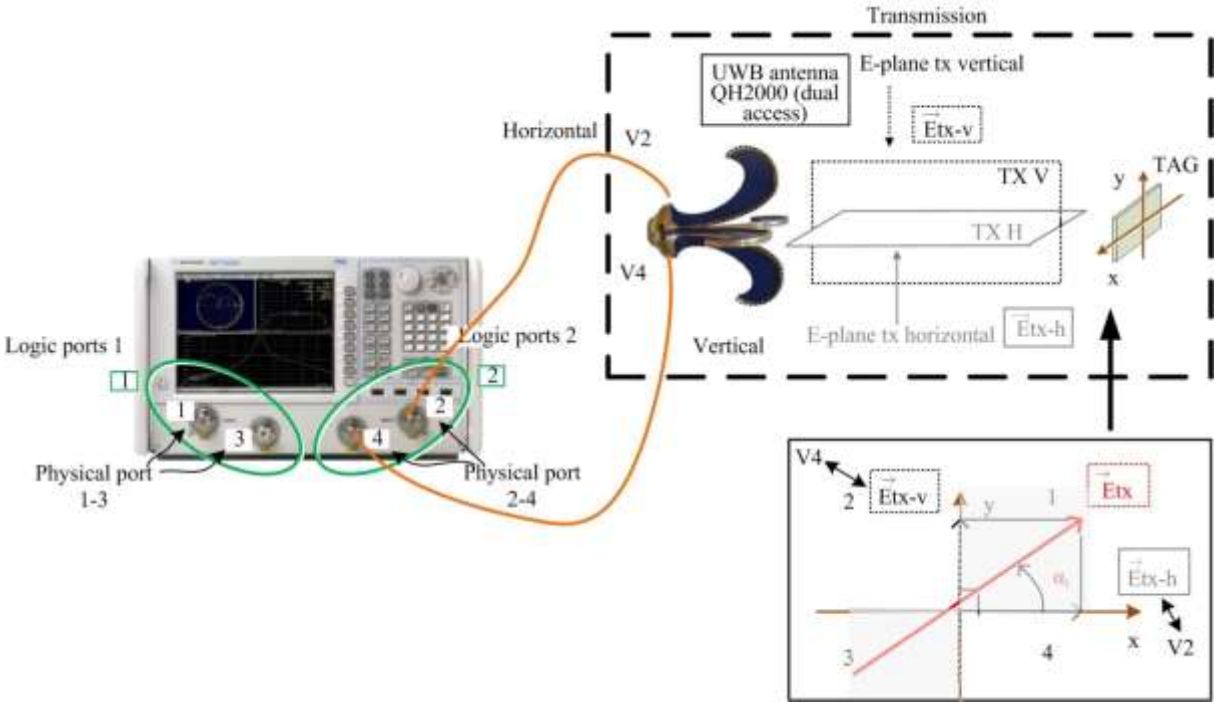


Figure 6.7. *Connection between the VNA and one dual access antenna. Using the logic port 2 of the VNA in transmission with a balanced configuration, the transmitting signal toward the tag will be the vector sum of the two linear polarized signals, in the two orthogonal E-planes of the antenna.*

The VNA allows for setting a power offset between the two signals V_4 and V_2 of a balanced port, maintaining the same phase relationship. The user can select the amount of power offset, whereas the sum of the transmitted power of the two single ports will be unvaried. Thus, it is possible to vary α_t in transmission inside the interval [0 - 90] deg. In more general application, this option is used to compensate from cables and PCB layout mismatching when measuring a chip characteristic as Common Mode Rejection Ratio (CMRR) of operational amplifier. The power offset between the two signals V_4 and V_2 is,

$$P_{offset} = 20log10(\frac{V_4}{V_2}). \quad [6.5]$$

The angle α_t depends from the amplitude of the two electric fields along the two E-planes of the antenna, $\vec{E}_{tx-v}$, and $\vec{E}_{tx-h}$. These electric field amplitudes are directly proportional to the amplitude of V_2 and V_4. Thus, α_t can be expressed with,

$$\alpha_t = \arctan(\frac{V_4}{V_2}). \quad [6.6]$$

Combining the equation [6.5] and [6.6], the relation between the power offset of the two signals V_4 and V_2, and the transmitting signal direction α_t is,

$$\alpha_t = \arctan\left(10^{\frac{P_{offset}}{20}}\right). \quad [6.7]$$

Table 6.1 shows some discrete values obtained with the aforementioned equation. As it can be observed, a power offset between +/- 15 dB is enough to cover almost all of the range [0 - 90] deg.

Relation between α_T and P_{offset}									
α_t(deg)	90	80	70	60	45	30	20	10	0
P_{offset}(dB)	∞	15	8.8	4.7	0	-4.7	-8.8	-15	-∞

Table 6.1. *Relation between α_T and P_{offset} using the equation [6.7].*

It is possible to make common to single (s-c) S-parameter measurement from logic port 2 to logic port 1, i.e. Ssc12. The transmitting balanced logic port 2 is composed of the two physical ports 2 and 4. The receiving logic port 1 is single and composed of only the physical port 1. In this manner, the transmitted balanced signal (logic port 2) has a differential component equals 0, and presents only a common component. This means that the two exiting signals of the transmitting antenna, V_2 and V_4 are in phase and equal in amplitude. Their power offset is 0 dB, and according to table 6.1, the transmitted linear-polarized signal has an angle α_t of 45 deg. Then it is possible to vary the power offset between the two components according to table 6.1 to modify α_t.

The true mode needs to be selected because otherwise the VNA will emulate only a balanced measurement. The VNA will perform only single to single measurements on the three physical ports 2, 4, and 1. Finally the VNA will arrange the results to retrieve the results

as for a real balanced measurement. Thereby, the true mode option is required for these experiments.

Another VNA option that has to be selected is called *offset as fixture.* It will not take into account, or more exactly compensate, the imposed power offset on the balanced logic ports, in post processing to retrieve the measurement result. Indeed, varying the power offset according to table 6.1 of the transmitting signal of the logic port 2, will create two signals V_2 and V_4 with same phase but different amplitude. The resulting transmitting signal toward the tag will be still linear polarized, but from equations [6.3] and [6.4], a differential component will be created besides the common one. The VNA is settled with common to single analysis, therefore it will make calculation only on the common component of the transmitting signal, expressed with equation [6.3], to give the measurement result. When the option *offset as fixture* is selected*,* the VNA will not take into account the imposed power offset variation from calculation, and the transmitting signal is considered as pure common in calculation. Indeed, independently from the selected power offset, the transmitting balanced signal has the same power.

The variation of the transmitting signal between the angle α_t equals 10 deg and 80 deg, which corresponds to a power offset variation P_{offset} from -15 dB to 15 dB (table 6.1), was validated in anechoic environment. The bench of the validation measurement process is shown in figure 6.8. One Satimo QH2000 antenna in transmission is connected to the balanced logic port 2 of the VNA, corresponding to the physical ports 2 and 4, and the other is connected to the VNA logical port 1 (physical port 1 only). This second antenna can be considered as a linear polarized probe in reception, where only one of the two “Vivaldi” antennas forming the QH2000 is connected to the VNA, and the other connected to a 50 Ω SMA load. The rotation of the probe antenna (receiving antenna) was executed with an electrical engine, and the two antennas were distant approximately 25 cm to recreate a typical UWB chipless RFID reading range.

The measurement results of the bench shown in figure 6.8 are in figure 6.9. In (a) the power offset equals to 15 dB that corresponds to an angle α_t equals to 80 deg. In (b) the power offset was 0 dB corresponding to an angle α_t equals to 45 deg, and in (c) a power offset of 15 dB corresponding to an angle α_t equals to 10 deg. These theoretical figures are validated with the corresponding measurements in figure 6.9.

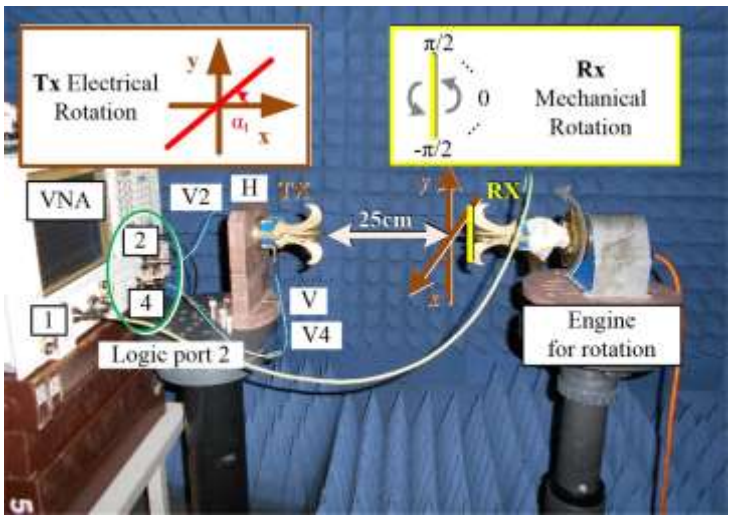


Figure 6.8. *Validation of the transmission Ssc12 balanced measurement in anechoic environment. A power offset P_{offset} is used in transmission (logic port 2) to turn the Tx linearly-polarized signal with the VNA option power offset as fixture. One Vivaldi component of the Satimo QH2000 antenna is used as a probe in reception (single port 1), and it is rotated mechanically to analyze the characteristics of the transmitted signal.*

3.2. Isolating the cross-polarized component in reception

In reception, the cross-component (related to the polarization of the transmitting signal) of the receiving signal, from the tag, needs to be measured. It corresponds at the EM field component with an angle equals to α_t plus 90 deg. The receiving antenna may be another dual access device connected to the physical ports 1 and 3. Then, it is possible to extract the tag contribution at α_t plus 90 deg (cross-polarization) from the signal measured at the two ports of the antenna. To do that, the clockwise system of reference rotation matrix can be applied at these two components to obtain the response in the wanted direction.

The measurement setup of a reading system using a 4 ports VNA Agilent N5222A, and two dual-access Satimo QH2000 wideband antennas, is shown Figure 6.10 (a). One antenna is used in transmission, and the other in reception. Ports 2 and 4 of VNA are connected to the transmitting antenna (Tx antenna), while ports 1 and 3 are connected with the receiving antenna (Rx antenna). From the figure, the transmitting and receiving antennas have the same orientation, hence, the rotation matrix has to be applied to an angle equal to α_t, and it is,

$$\begin{pmatrix} V_{cross} \\ V_{co} \end{pmatrix} = \begin{pmatrix} \cos(\alpha_t) & -\sin(\alpha_t) \\ \sin(\alpha_t) & \cos(\alpha_t) \end{pmatrix} \begin{pmatrix} V_3 \\ V_1 \end{pmatrix}. \quad [6.8]$$

V_1 and V_3 are respectively the receiving signals on the VNA physical ports 1 and 3, which are connected to the vertical and horizontal component of the receiving antenna. V_{cross} is the part of the receiving signal along with the wanted direction at α_t + 90 deg. V_{co} represents the response along with the direction defined by α_t. From equation [6.8] V_{cross} is,

$$\text{Vcross} = cos(\alpha_t)V_3 - \sin(\alpha_t)\,V_1. \quad [6.9]$$

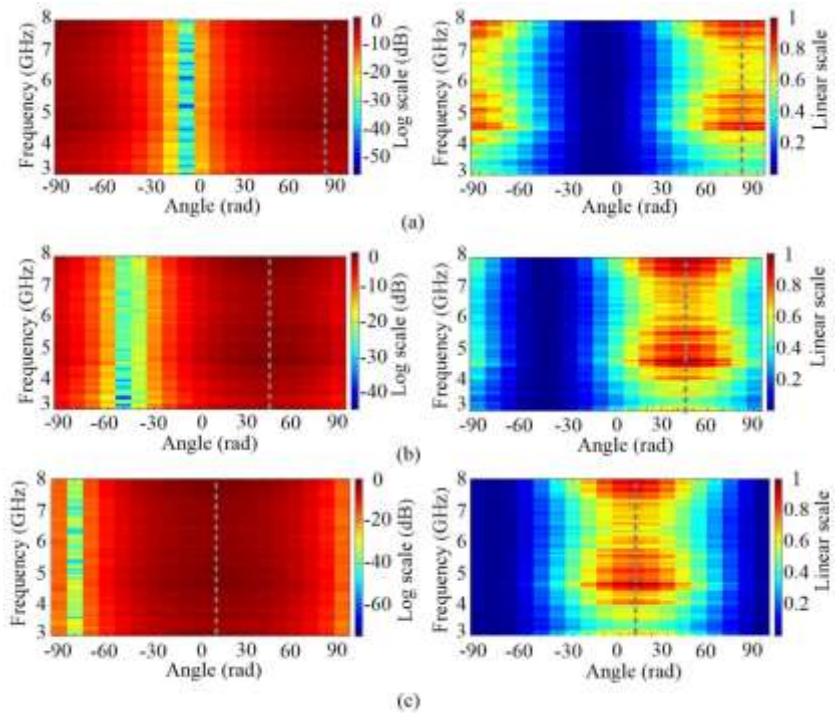


Figure 6.9. *Validation of the transmission Ssc12 balanced measurement for power offsets of (a) 15 dB, corresponding to 80 deg, (b) 0 dB, corresponding to 45 deg, and (c) -15 dB, corresponding to 10 deg. The scale is semi-logarithm on the left side 2-d plots, and linear on the right side.*

3.3. Measurements of cross-polarized tag

To measure the two components of the receiving antenna, as shown in figure 6.10 (a), the simplest way would be to set up the VNA with two common to single measurements Ssc12. The single logic port 1 is the physical port 1, for one measurement, and the physical port 3 for the other. Unfortunately this is not possible in a true mode approach. So another option provides the execution of one common to common (Scc12) and one common to differential (Sdc12) measurement. In reception, the logic port 1 is composed of the two physical ports 1 and 3, and is treated as a balanced port. The measurement in reception of the common and

differential components, of the balanced receiving signal, correspond to the two signals of equation [6.1] and [6.2]. From figure 6.10 (b), it is equivalent to a rotation of 45 deg, of the receiving Cartesian coordinate system (x,y). Finally the rotation matrix of equation [6.8] has to be modified as in equation [6.10], to take into account the rotation of 45 deg (see figure 6.10 (b)) already done, and applied to the measured signals $V_{LP1-Common}$, and $V_{LP1-Diff}$.

$$\begin{pmatrix} V_{cross} \\ V_{co} \end{pmatrix} = \begin{pmatrix} \cos(\alpha_t - 45) & -\sin(\alpha_t - 45) \\ \sin(\alpha_t - 45) & \cos(\alpha_t - 45) \end{pmatrix} \begin{pmatrix} V_{LP1-Common} \\ V_{LP1-Diff} \end{pmatrix}. \quad [6.10]$$

The V_{cross} becomes,

$$\text{Vcross} = cos(\alpha_t - 45) V_{LP1-Common} - \sin(\alpha_t - 45)\, V_{LP1-Diff}. \quad [6.11]$$

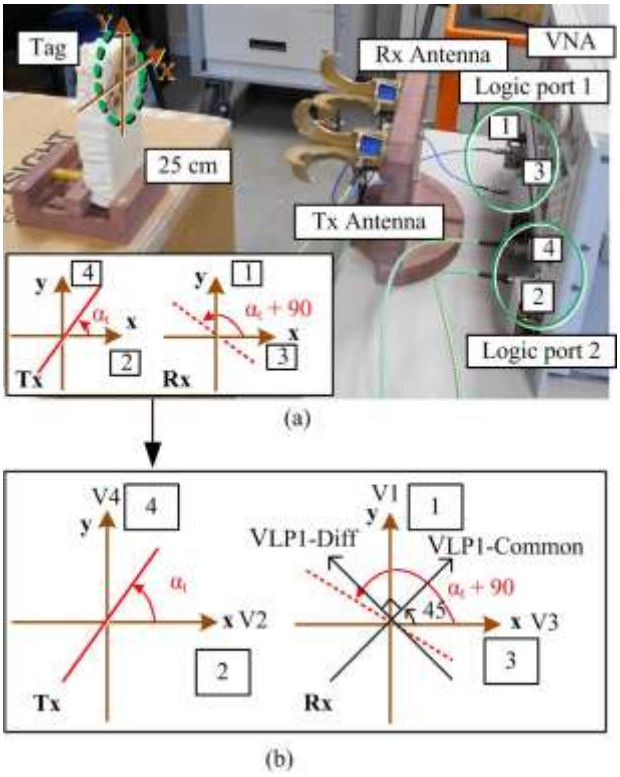


Figure 6.10. *(a) Measurement setup of a reading system using a 4 ports VNA Agilent N5222A, and two dual-access Satimo QH2000 wideband antennas. One antenna is used for transmission, and the other for reception. (b) Antennas configuration, where the receiving signal is measured on its common and differential components ($V_{LP1-Common}$, $V_{LP1-Diff}$).*

This approach was validated in practical environment, where the bench is presented in the figure 6.10 (a). The tag was placed at different orientations (β), and for each the transmitting

signal direction was modified to retrieve the tag position (α_t equals β). The power offset (P_{offset}) in transmission was selected according to table 6.1. The measurement results are shown in figure 6.11. The STFT approach was used, and the results are normalized. The tag orientation β was varied with the discrete positions: 0, 30, 45, and 90 deg. The tag was correctly decoded for each of its positions.

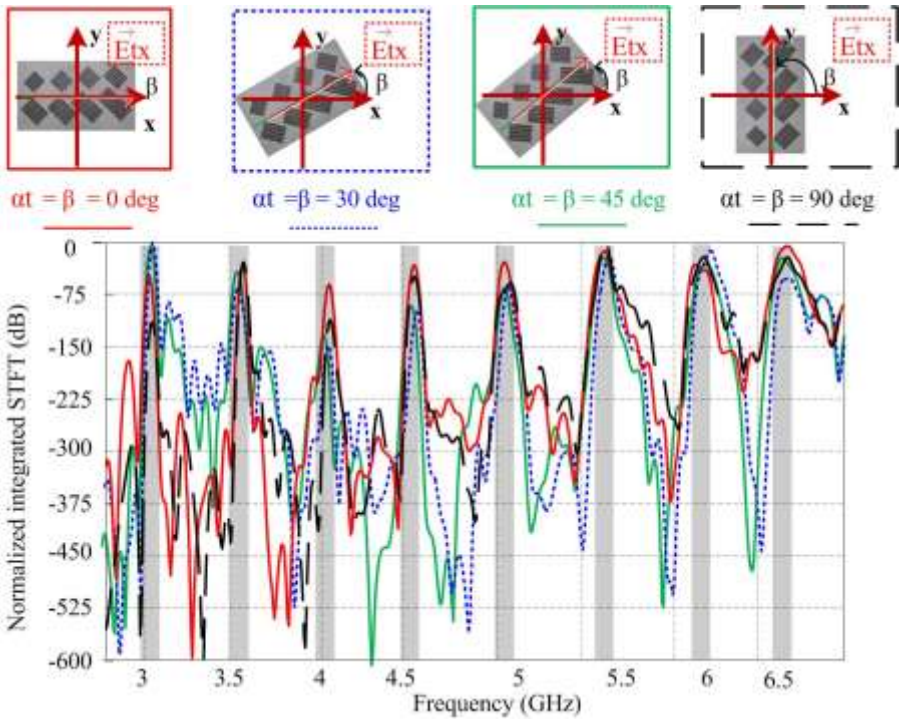


Figure 6.11. *Measurement of the cross-polarized tag presented in [VEN 13], for different orientations (β), referred to the bench of figure 6.10. The VNA was settled with two measurements (Scc12), and (Sdc12). The angle α_t is varying in transmission to retrieve the tag position β, and used the equation [6.11] to retrieve the cross-polarized tag response.*

The proposed approach expects the variation of α_T in the range [0 - 90] deg, which is controlled by the power offset (P_{offset}) between the two physical ports 2, and 4, of the transmitting logic port 2. As demonstrated in the next section, in a practical approach, the backscattered signal from the tag needs to be evaluated only for two orientations α_T (one distant of 45 deg from the other) to retrieve the tag ID, independently from its orientation. A GUI software in Matlab, presented in Appendix 8, has been realized to perform balanced measurement.

4. Tag measurements using the VNA - a simplified approach

4.1. Practical approach

The variation of antenna (tag) mode cross-polarization RCS of a tag versus the angle of observation (transmitting signal direction) has been characterized in [RAN 17], and simulated in the first section of this chapter, where the results are shown in figure 6.3. The tag mode cross-polarized RCS is a function of the difference between β and α_t , and may be expressed with equation [6.12].

$$\frac{\sigma_{\alpha_t-\beta}}{\sigma_{CROSS}} = |(1 - 2sin^2(\beta - \alpha_t))|^2 \qquad [6.12]$$

$\sigma_{\alpha_t-\beta}$ is the actual RCS in that condition of measurement, and σ_{CROSS} is the RCS in the best case, which is when α_t equals β ±*n* 90 deg, with *n* integer. The domain of the function is defined by $\beta - \alpha_T$. The transmitting angle α_t was chosen varying between 0 and 90 deg. The function is periodic of 90 deg, and plotted in figure 6.12 (a) in linear scale, and in figure 6.12 (b) in semi-logarithmic scale. The variation of the function amplitude around their maximums is of 6 dB in the range ±30 deg. Outside this range, the $\sigma_{\alpha_t-\beta}$ decreases quickly with a theoretical dynamic variation of ∞ dB when the variation is of ± 45 deg.

From the equation [6.12], represented in semi-logarithmic scale, for any two points in the function domain distant of 45 deg, at least one of the two will be inside the favorable range of ±22.5 deg around one of the maximums of the function. It corresponds to a maximum RCS variation of 3 dB respect to the maximum σ_{CROSS}, which allows to retrieve the tag ID without ambiguity. Because the tag position β is fixed, then selecting two points 45 deg distant means varying the transmitting interrogating angle α_t of 45 deg. Thus, the proposed approach presented in the last section may be used. In such as case, only two variations of α_t will be imposed to retrieve the tag response (ID) whatever its orientation. The solely constraints are: 1) the two α_t have to be 45 deg distant, 2) from the two measurement results, a simple criterion has to be applied to select which of the two contains the tag information (ID). For instance, in figure 6.13 is shown the measurements of one tag using the two angles α_t equal to 0 deg and 45 deg. The tag is placed at the discrete positions β equal to 0 deg and 45 deg. In (a) is shown the measurement results for the transmitting angle α_t equal to 0 deg. When the tag is on horizontal position (β = 0 deg), the measurement is fully successful, while when at 45 deg, the results are inconsistent with the presence of significant

secondary lobs around some of the tag resonances. This is because $\beta - \alpha_t$ is equal to 45 deg that represents one minimum of the equation [6.12] (see figure 6.12). Instead, in figure 6.13 (b) is shown the measurement results varying α_t to 45 deg, and the previous case of failure becomes a fully successful reading.

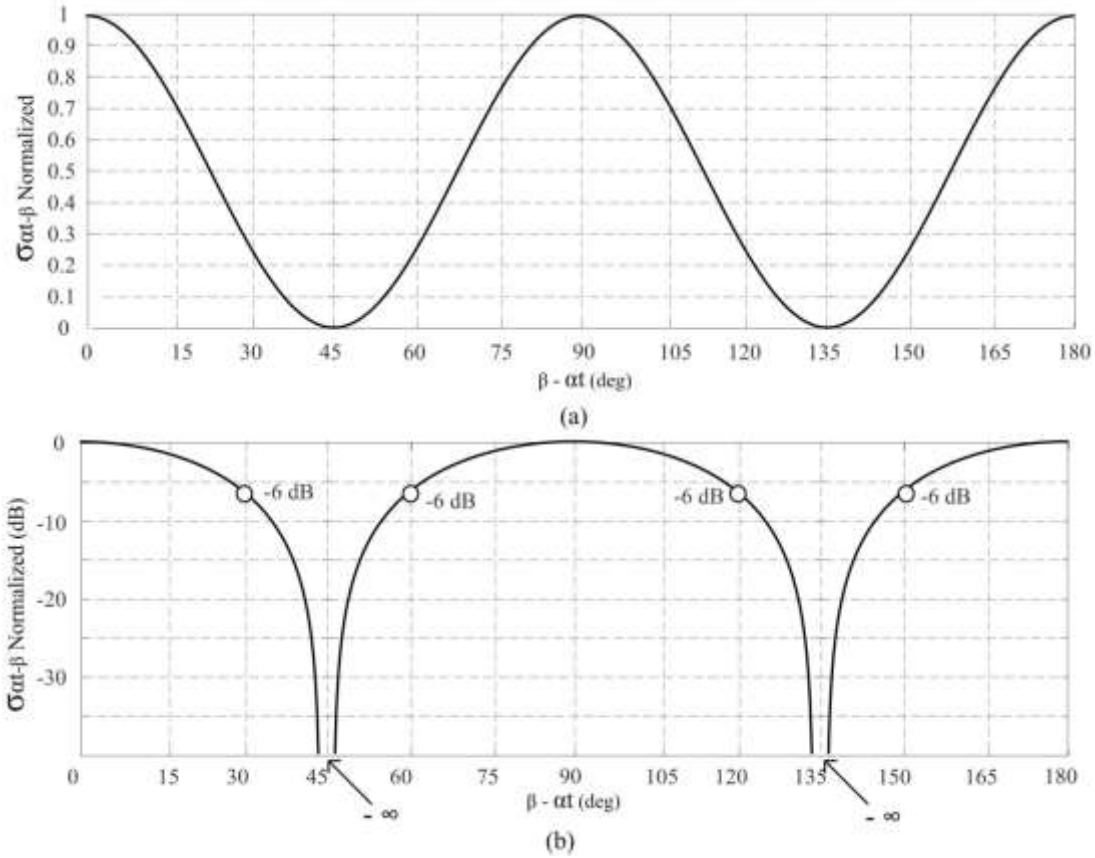


Figure 6.12. *Representation of equation [6.12] in linear (a) and semi-logarithm (b) scale. A variation of $\sigma_{\alpha_t-\beta}$ in the range ±30 deg, around one maximum of the function, assures a cross-polarized RCS dynamic variation of 6 dB.*

In figure 6.14 is shown the normalized measurement using the STFT of a cross-polarized tag, for different tag positions, with a fixed α_t equal to 0 deg. Note that for sake of clarity, i.e. to ease the comparison, all the signals have been normalized. In exchange, we lose in Fig. 6.14 the information on the RCS amplitude dependency with the orientation that we can retrieve in figure 6.12. The test bench is that of figure 6.10 (a). The tag position β was varying between 0, 15, 30, and 45 deg. The reading was successfully when $\beta - \alpha_t$ was in between 30 deg. It corresponds to the case of β equals 0, 15 and 30 deg. As expected the best result is for β equals to α_t ($\beta - \alpha_t$ = 0), which corresponds to one maximum of equation [6.12]. This result validates the assumption that the tag can be read even though not perfectly oriented

with the antenna of the reader, i.e. in a certain range around the maximums of the equation [6.12]. In this case, it was read at a distance of 30 deg from the maximum.

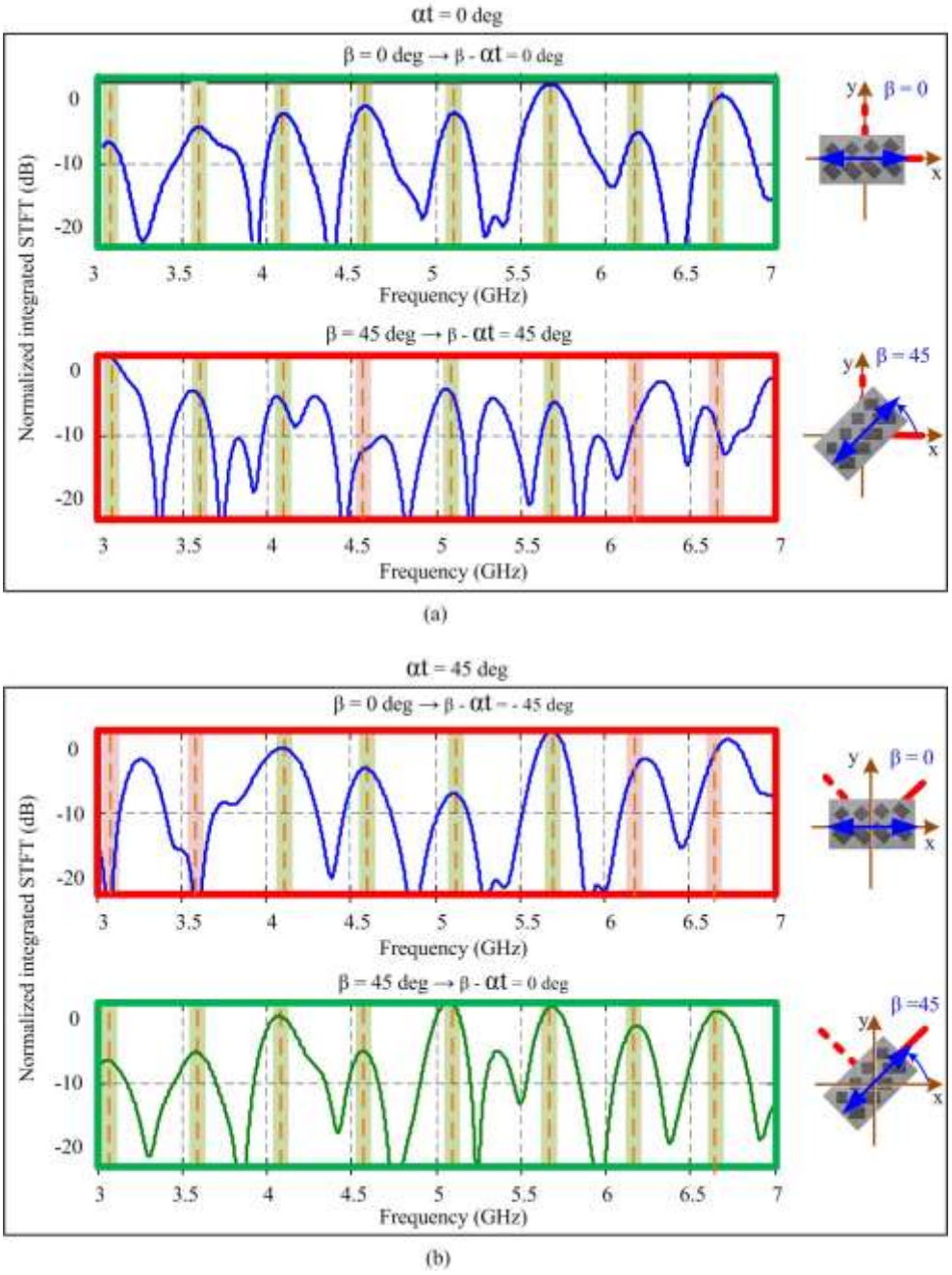


Figure 6.13. *Reading of a tag using electrical rotation principle based on two discrete transmitting angles. (a) Tag measurement results with α_t equals to 0 deg, the tag position corresponds to β = 0 deg and β =45 deg. (b) Tag measurement result varying just α_t to 45 deg.*

The two measurements are needed to read the tag independently from its orientation as demonstrated with figure 6.13 and 6.14. In the next section, this approach is applied to the optimized reader discussed in the chapter 4. A criterion of selection is given to select which of the two measurements has to be used to retrieve the tag ID.

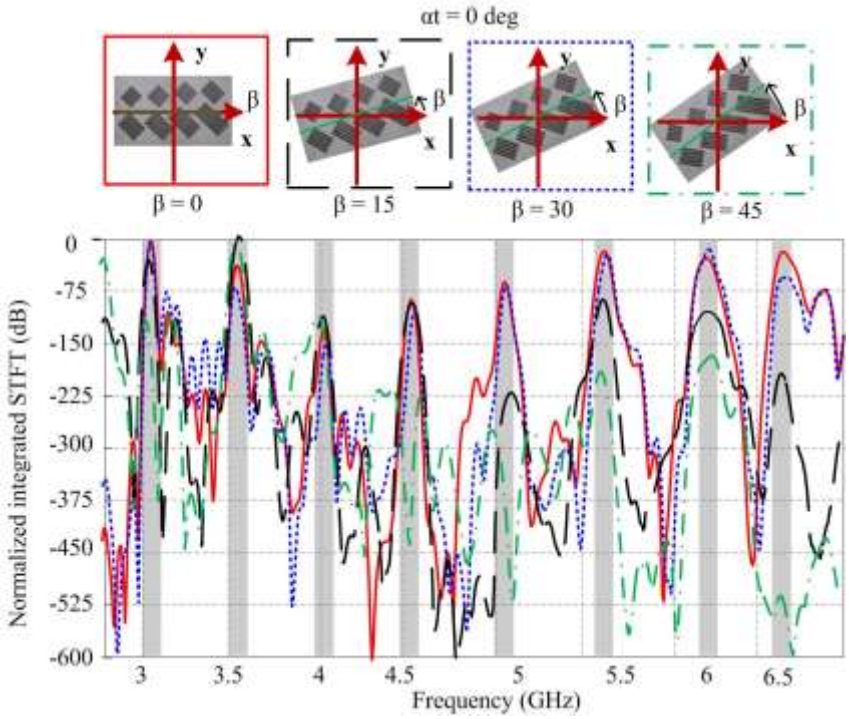


Figure 6.14. *Normalized measurement using STFT of a cross-polarized tag, for different tag positions with a fixed α_t equals to 0 deg. The bench is that on figure 6.10 (a). The tag position β was varying between 0, 15, 30, and 45 deg. The reading was successful for all the values of β, except that for 45 deg (minimum of equation [6.12]).*

5. Optimized reader approach

The chipless reader version, presented in chapter 4, may be modified to be able to turn towards the tag the linear polarized interrogating signal as for the VNA. It has to perform two measurements with α_t varying of 45 deg, according to last section result. The proposing reader is shown in figure 6.15. It is composed of the central block with the addition of other components. The transmission part is composed of the pulse generator Hyperlabs HL9200, followed by the wideband splitter ZN2PD-63+ from Mini-Circuits. One of its outputs is directly connected with the port allowing for horizontal polarization of the Satimo QH2000 antenna. The other splitter output is connected to a wideband switch, with one output closed to a 50 Ω load, and the other to the second port of the same transmitting antenna allowing for vertical

polarization. In reception another dual polarized antenna is connected to a switch, followed by the HPF Mini-Circuit VHF-3100+, and a LNA Mini-Circuits TVA-82-213A+. Both the transmission and reception chains are connected to the optimized reader of chapter 4, which is composed of the Xilinx FPGA evaluation board SP601, the designed RF-front end, and the alimentation board.

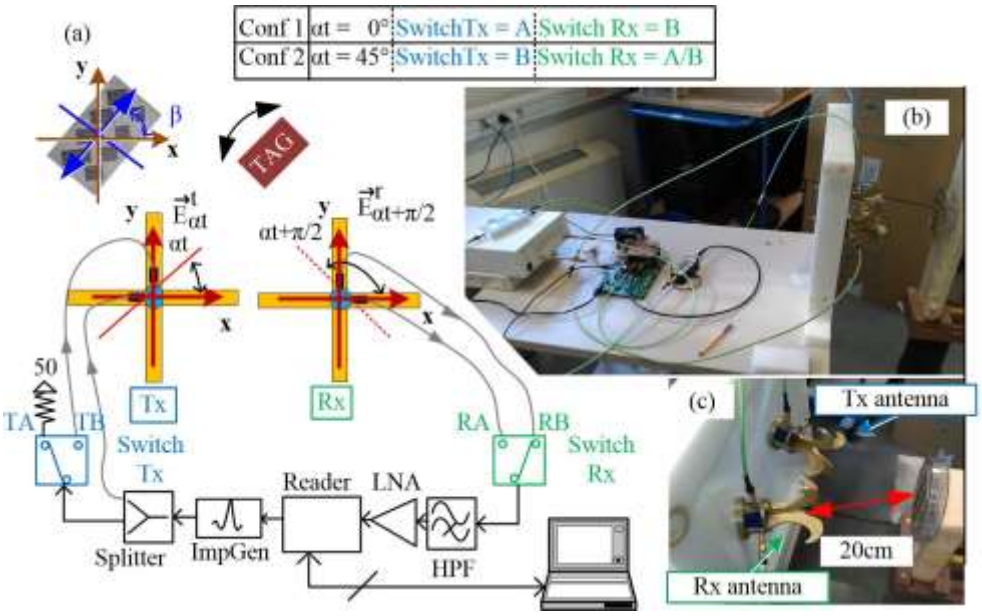


Figure 6.15. *Optimized reader of chapter 4, modified to perform measurement with α_t in two discrete positions (0 & 45 deg), to retrieve the tag ID independently from its orientation. (a) Reader architecture, (b) measurement bench in real environment, (c) zoom on antennas and tag positions.*

In transmission the reader is able to send a linear polarized signal with α_T equals 0 deg and 45 deg, respectively for the configurations called *Conf. 1* and *Conf. 2* (see figure 6.15). In reception, by changing the position of the switch between R_A and R_B, the tag response in the two orthogonal directions can be measured in turn. Finally, with post processing it is possible to isolate the cross component depending on the imposed transmitting angle α_t. For α_t equals 0 deg (*Conf. 1*), the reader needs to measure only the vertical contribution of tag response, as so the switch in reception chain is set in position R_B. For α_T equals 45 deg (*Conf. 2*) both orthogonal components need to be measured (postion R_A and thereafter R_B). After to isolate the electrical field contribution in cross direction (α_t + 90 deg), as describe by equation [6.9], it is sufficient to substrate the horizontal contribution to the vertical.

The reader has an external LNA to compensate from multiple attenuating factors. First the use of a splitter in transmission reduces the transmitted power as low as 3 dB in case of Conf. 1 (α_t = 0 deg). In case of Conf. 2 (α_t = 45 deg) the limitation are in reception, because the tag response in cross, (α_t + 90 deg) with α_t equals to 45 deg is measured in turn through its projections along with the two receiving antenna components, and therefore attenuated each of 3 dB. Thus, the effective ADC number of bits used may decrease, as shown in chapter 4 (section 2), increasing the quantization noise. The second attenuating factor is the use of two distinct dual access antennas instead of only one, as for classical reading technique. With only one antenna, the tag can be well aligned with the tag, while with two it is more difficult and less effective especially when the distance of the tag is varying. Moreover the antennas are designed to work from 2 GHz and therefore are larger than required for UWB applications (3.1 – 10.6 GHz).

Figure 6.16 shows measurements performed in practical environment with the reader in *Conf. 1* (α_t = 0 deg), where the tag position β is gradually varied from best case, β equals 0 deg, to worst case β equals 45 deg. The setup is shown in figure 6.15 (b), where the tag was placed at 20 cm from the antennas as shown in figure 6.15 (c). First an empty measurement without the tag was performed, then a second with the tag. As predicted, the reader was able to read the tag just with β ranging from 0 to 30 deg. At 45 deg, the reading was incorrect because the useful signal level was excessively low. To read the tag in this last orientation, the *Conf. 2* needs to be used (α_t = 45 deg).

Figure 6.17 shows the measurement of a tag placed at 45 deg (β) using the two configurations, respectively in blue dashed line for the *Conf. 1*, and in red straight line for the *Conf. 2*. As expected the *Conf. 2*, which match the position of the tag, shows the best reading (α_t = 45 deg). In *Conf. 1* only the first resonance is in the correct position, while for *Conf. 2* almost all the resonance positions are correctly placed. The second resonance (to a lesser extent the third resonance) is shifted of few tens of MHz also *in Conf. 2*. This measurement deviation is due to many factors which could be improved. Besides those already exposed, important contributions come from the antennas adaptation, which is above -10 dB until 4 GHz. Finally the reader prototype is composed of a numerous of distinct devices some of them on FR-4 sbustrate.

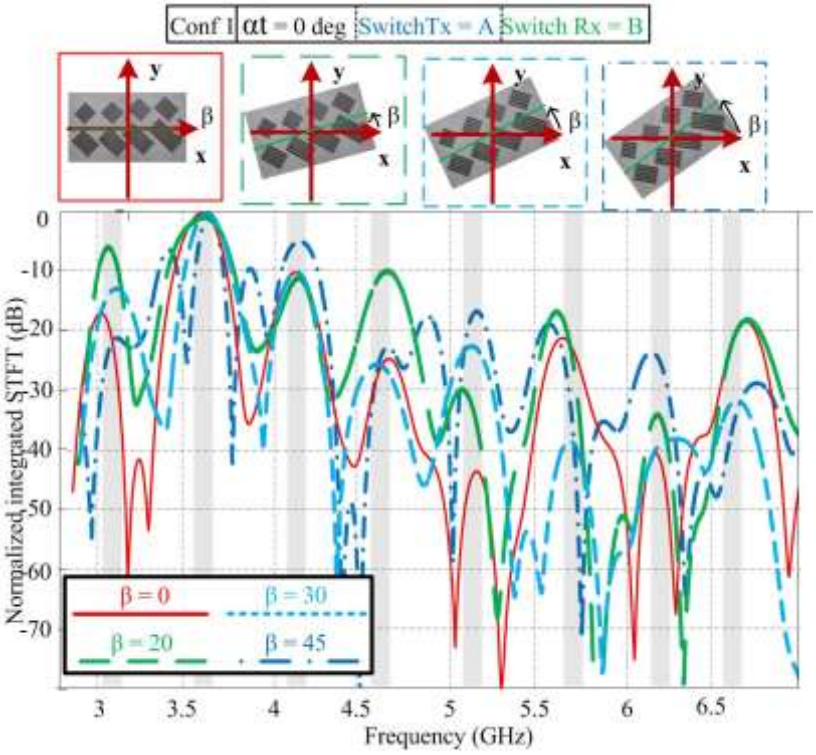


Figure 6.16. *Normalized Measurement results of bench in figure 6.15 (b) in practical environment. The tag was oriented in different directions, from β equals to 0 to 45 deg using Conf. 1 (α_t = 0 deg).*

As demonstrated in this chapter, the reading in both configurations (*Conf. 1* and *Conf. 2)* may guarantee a correct tag reading independently from the tag orientation. However, a criterion is needed to select which measured response is the correct one. From figure 6.16, in some cases it is possible to discriminate the correct reading between the two configurations only if the expected number of peaks (resonant frequencies), in the given frequency range, is already known. In a more general case, a criterion of selection is needed. One may keep the last peak position fixed as criterion, and use the others to encode the tag ID. Yet, it reduces the tag coding capacity, and it does not prevent the situation where both configurations (Conf. 1 and Conf. 2) give a correct position of the last peak. The suggested approach is to discriminate the two signals based on tag signal maximum power. In figure 6.17 is shown the response of the tag of figure 6.16 in time domain. For clarity, the signal in time has been cut at 8 ns. In the first 2 ns is present the tag structural mode, and after the antenna (tag) mode where the signal contains the coding information. The tag structural mode was removed with the application of the STFT. The power of the structural mode in *Conf. 2* (correct reading) is higher than that in *Conf. 1*. Anyway it is risky to use this power

difference as criterion because it can vary based on the item at which the tag is attached. Thus, a discrimination based on the antenna (tag) mode is more appropriate. The selected measurement, to be used to decode the tag ID, will be the more powerful one inside the tag mode frame [MAN 15]. This algorithm frees the tag designer from any additional constraints from the reader part.

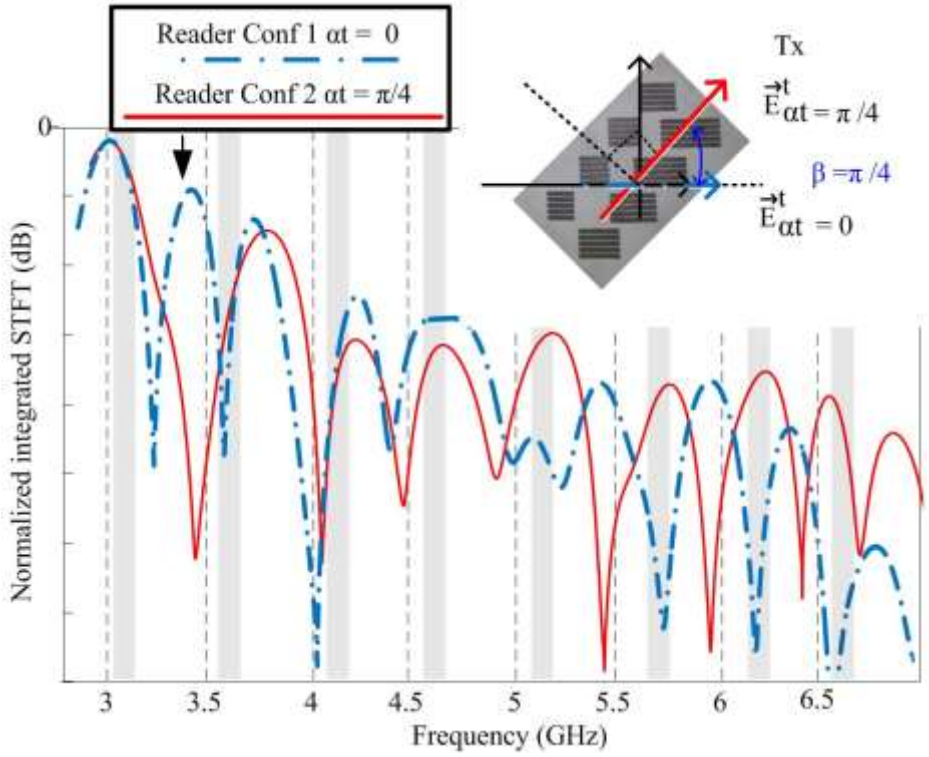


Figure 6.17. *Tag placed at β equal to 45 deg and read with both reader configurations. The measurement was executed in practical environment, and the setup is shown in figure 6.15 (b).*

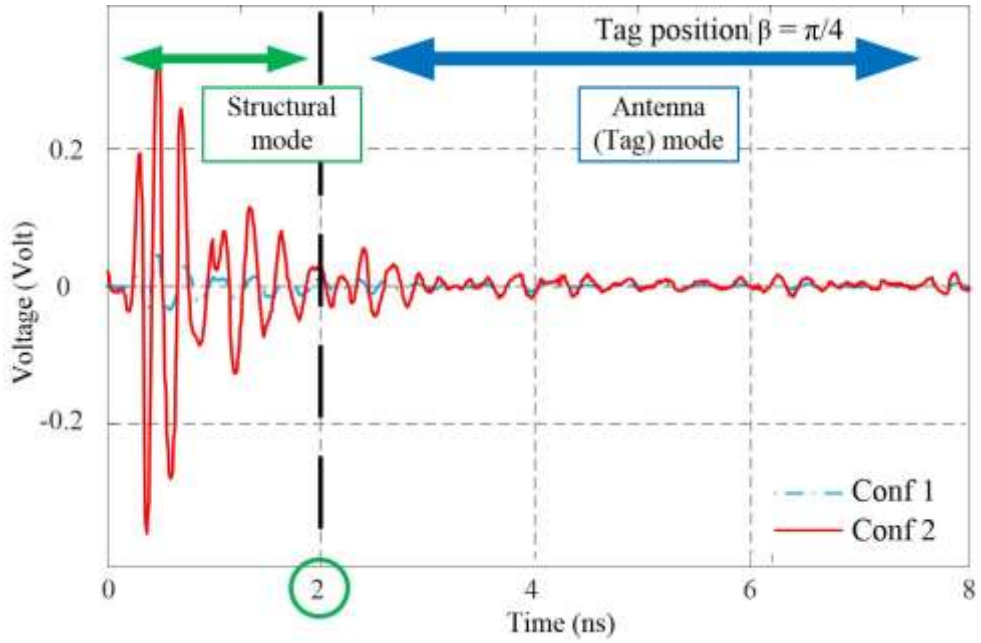


Figure 6.18. *Response in time domain of the measurement of figure 6.17. The tag was placed at β equals 45 deg, and interrogated with both reader configurations (conf. 1, conf. 2).*

6. Conclusion

This chapter has proposed a reading system for the UWB chipless RFID technology, which is independent from the orientation of the tag. It is an original approach because, conversely to the others RFID systems, it is not based on circular polarized antennas, and the reading is specific to chipless tags that are designed based on the cross-polarization principle.

The concept for electrically changing the reader antenna polarization has been presented, and validated in an anechoic environment. Measurements of a chipless tag at different polarization orientations show that the tag can be read with a fixed antenna, while keeping cross-polarization configuration. The first reader system was based on a state of the art 4 ports VNA, and its capability to perform balance measurement have been exploited. After a second reader realized based on the hardware implementation of chapter 4 was proposed. It is able to perform measurement at two discreet positions, which are enough to retrieve correctly the tag ID. A criterion for discriminate which of the two measurements performed has to be used to recover the ID was introduced. This reader does not give any constraint to the designer on the tag shape or even the encoding approach to be used. In prospective to

improve the reader performance a dedicated work on the antennas part is needed. This with the aim of reducing their dimensions in order to be better aligned with the tag. In addition, a work in component integration and the use of an ADC with a better resolution is expected.

6.7 References

[MAN 15] REZAIESARLAK R., MANTEGHI M., "Accurate Extraction of Early-/Late-Time Responses Using Short-Time Matrix Pencil Method for Transient Analysis of Scatterers," in *IEEE Transactions on Antennas and Propagation*, vol. 63, pp. 4995-5002, 2015.

[PER 14] PERRET E., Radio Frequency Identification and Sensors: From RFID to Chipless RFID, Wiley-ISTE, 2014.

[PNA 16] KEYSIGHT TECHNOLOGIES, PNA Series Network Analyzers Help, Information online available at :http://na.support.keysight.com.

[RAM 16] RAMOS A., PERRET E., RANCE O., et al., "Temporal Separation Detection for Chipless Depolarizing Frequency-Coded RFID," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 7, pp. 2326-2337, July 2016.

[RAN 17] RANCE O., PERRET E, SIRAGUSA R., et al., RCS Synthesis for Chipless RFID 1st Edition, ISTE Press – Elsevier, 2017.

[SHEN 12] SHEN Y., LAW C. L., "A Low-Cost UWB-RFID System Utilizing Compact Circularly Polarized Chipless Tags," *IEEE Antennas and Wireless Propagation Letters*, Vol. 11,pp. 1382-1385, 2012.

[VEN 12] VENA A., PERRET E., TEDJINI S., "High Capacity Chipless RFID Tag Insensitive to the Polarization," in *IEEE Transactions on Antennas and Propagation*, Vol. 60, pp. 4509-4515, Oct. 2012.

[VEN 13] VENA A., PERRET E., TEDJINI S., "A Depolarizing Chipless RFID Tag for Robust Detection and Its FCC Compliant UWB Reading System," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 61, No. 8, pp. 2982-2994, Aug. 2013.

General Conclusion and Prospective

General conclusion

A summary of the investigation of UWB chipless RFID reader technology is presented here. After an introduction of the chipless RFID technology in the chapter 1, a study of the state of the art focused on the reader part has been shown in chapter 2. In literature, all the reader solutions are based on frequency domain approach (SFCW/FMCW), and therefore may ensure accurate reading at the expense of excessive reading time, in the order of tens of seconds. A comparison with IR-UWB is also given in the chapter 2, and a link-budget taking into account the UWB regulations is proposed. The IR-UWB approach ensures higher receiving power than frequency domain reader when the UWB regulations are taken into account. However it has higher input noise bandwidth, due to the characteristics of the receiver, and then the hardware has to be optimized to reduce its sampling noise. The IR-UWB permits a reduced reading time and a real time reader may be realized. For these reasons the IR-UWB approach was selected to design all the readers presented in this manuscript.

Previous the beginning of the thesis, a first prototype of an IR-UWB chipless RFID reader was developed, and presented in the chapter 3. It was completely operative and designed as proof of concept. The reader development has been founded with the project *Gravit,* which started in December 2010 and terminated in 2012. After that some intern students have been involved in its amelioration until the beginning of the current thesis in February 2014. The majority part of the chapter 3 is focused on the presentation of the first reader version designed during this thesis. It shows a more integrated hardware solution with higher performance in term of acquisition accuracy. The retail cost after tax of the reader components was halved respect to the previous reader version, and of about 2,350 € not

considering the antennas. The introduced reader has a reduced sampling noise as a result of the exploitation of the FPGA Spartan 6 internal facilities, and an advanced hardware design.

An optimized reader version is presented in chapter 4. It was designed to reduce further the reader sampling noise to significantly improve the reading performance. In fact, persistent hardware architecture can be optimized with ameliorations in the board layout, in the FPGA design, and with the use of few low cost passive components. The reader shows a sampling clock period jitter, which is correlated with the sampling noise, of only 2.45 ps of standard deviation, and a peak to peak of 16.31 ps over 1,000 cycles. The reader input sensitivity is of -60 dBm, and the reader was optimized also in terms of flexibility and reading time. The sensitivity could be improved using a higher ADC resolution after the S/H amplifier (number of bits).

The reader flexibility is at the level of the acquisition window time. It can be customized in term of position, length, and equivalent sampling period. The reading time was varying, depending on acquisition parameters, with a minimum of 6 ms for one measurement without averaging, to 0.5 s for the maximum averaging of 512. It is a huge improvement respect to all the readers presented in literature, but also compared to the previous reader version (chapter 3). The reader was shown in the Drupa 2016 event, in Düsseldorf Germany from 16 June to 25 June, which is a global showroom for printing technologies, and accredited as the largest showroom in the word. To show the chipless RFID technology to the attendees, the reader has being used without interruptions for 10 hours a day reading printed single layer Powercoat PW230 paper substrate frequency-coded tags. The reader cost estimation was close to the previous version of around 2,306 €.

The design of a low jitter UWB pulse generator was described in the first part of chapter 5. It was realized on low cost substrate and based on COTS components. The pulse generator was simulated and its emission was characterized based on FCC mask, and also compared with commercial available solutions. Its random jitter is of only 2 ps of standard deviation, over 1,000 cycles. The pulse generator has been used to read frequency-coded tags in practical environment. It could be used as the emission stage of the optimized reader presented in chapter 4. In prospective, it will reduce the reader price from 2,306 € to something around 1503 €, for a version without output pulse width fine tuning, or 1699 € with fine tuning. The design of a UWB planar Vivaldi antenna is also proposed in the chapter 4. It has a -10dB bandwidth between 3 and 10 GHz (measured), and a maximum gain of 7.33 dBi

at 5.5 GHz (simulated). This antenna could also be employed as radiative parts of the optimized reader version (chapter 4).

Depolarizing based chipless RFID tags are a robust solution compatible with readings in a practical environment. These tags also carry on a significant quantity of information, in some cases of about 40 bits. The major inconvenient of depolarizing based chipless RFID tags is their inner dependency on orientation. Therefore the tags have to be aligned with the reader antennas to ensure correct identification. A solution of this issue was proposed in the chapter 6 with a novel reading approach. Measurements of a chipless tag at different orientations have been done, and the results shown for the first time that the tag can be read with fixed antennas, while keeping a cross-polarization reading configuration. The concept was first verified with state of the art test equipment. A 4 ports VNA, and its capability to perform balanced measurements, has been used. After, the optimized reader presented in chapter 4 was adapted to use the proposed technique. It is able to perform measurement at two discreet positions, which are enough to retrieve correctly the tag ID whatever its orientation. A criterion was introduced to discriminate which of the two performed measurements has to be used to recover the tag ID. This reading technique does not give any constraint to the tag design.

Prospective

The thesis results show that the design of a low cost (compared to laboratory equipment) UWB chipless RFID reader based on IR-UWB technology is feasible. It can be a real time device and easily compliant with UWB regulations. All the proposed prototypes have been realized with COTS components. It gives the opportunity to optimize the reader performance using new components on the market. The use of COTS components may also be exploited to add functionalities, such as the reading independent on tag orientation shown in chapter 6. Finally, the realization of an ASIC, that integrates the analog part of the reader, may open to integrated solutions in mobile devices such as the smartphone. The problem of energy consumption should be faced.

The reader components cost was estimated at 1.503 € after tax and referred to retail price, with the use of the proposed pulse generator (no pulse width fine tuning), and the UWB antennas proposed in the chapter 5. A reduction of about 20/30 % is feasible in an

industrial production. As prospective, actually we are working on an integrated version, where the RF front-end, the new pulse generator, and the used components of the SP601 Xilinx evaluation board are integrated in the same board. This will free up the estimated cost from the Xilinx evaluation board, which is of about 432 € where the used components have a total cost of about 50 €. The new reader version may have a retail components cost, after tax, of about 1,121 €. With a reduction of 30 % it could be reduced at 785 €. The use of a lower loss substrate than FR4 at higher frequencies will also increase the reader acquisition performance.

7

Appendix

- **Appendix 1. Matlab GUI acquisition software for Agilent DSO91204A**
- **Appendix 2. PC application software for first reader version in chapter 3**
- **Appendix 3. Reader chapter 3 - FPGA Reader_0 block description**
- **Appendix 4. External Flash**
- **Appendix 5. User Logic Reader chapter 4**
- **Appendix 6. Matlab GUI reader chapter 4**
- **Appendix 7. Schematic power supply board reader chapter 4**
- **Appendix 8. Matlab GUI acquisition software for VNA N5222A performing balanced measurement**
- **9. References**

Appendix 1

Matlab GUI acquisition software for Agilent DSO91204A

To facilitate the use of the high performance DSO Agilent 91204A, a GUI has been developed in Matlab environment. It was used for the debugging of all the electronics cards realized during the work of the thesis, and also to read UWB chipless tags in an IR-UWB configuration.

A screenshot of the Matlab GUI is shown in figure A.1, it is divided in four rows, each referred to a different acquisition channel of the DSO, and all sharing the same characteristics. A radio button let's select between measurement with or without trigger. A measurement without trigger means that the GUI transfers to the PC the actual signal on the memory of the DSO, for that particular channel. If the measurement with trigger is selected, the DSO will start a new acquisition, and will transfer to the PC the data referred to the selected channel. Finally, a button lets acquires at the same time the data of all the channels.

To use the Matlab environment to communicate with the DSO, the Instrument Control Toolbox needs to be installed on the PC. It contains a library of functions that can make use of the Agilent IO Libraries Suite. It is a collection of libraries and software utilities to enable the communication with the DSO. Between the others it contains The Virtual Instrument Software Architecture (VISA) libraries that are used by the developed Matlab GUI.

To established the communication with the DSO the following lines of code are used,

```
% Create the Visa object v for the DSO, using the USB interface
v=visa('agilent', 'USB0::0x0957::0x9002::MY51050102::0::INSTR');
% Remove data from the input buffer of the object v
flushinput(v)
% Allocate the object v input buffer
v.InputBufferSize=buffersize;
```

```
% Opening the communication with the DSO

fopen(v);

% Define a time out of 10 seconds

v.Timeout=10;
```

To query for data of a precise channel with trigger the next lines of code are used. If the measurement is without trigger, it is sufficient to comment the first line of this code.

```
% Single trigger section

fprintf(v,':SINGLE');

% Select the Channel Chan

fprintf(v,':WAVEFORM:SOURCE CHAN');

% Define the waveform format in byte

fprintf(v,':WAVEFORM:FORMAT BYTE');

% Query for channel vertical increment and origin

yinc=str2double(query(v,':WAVEFORM:YINC?'));

yor=str2double(query(v,':WAVEFORM:YOR?'));

% Query for channel horizontal (time) increment and origin

xinc=str2double(query(v,':WAVEFORM:XINC?'));

xor=str2double(query(v,':WAVEFORM:XOR?'));

% Query for channel measurement

fprintf(v,':WAVEFORM:DATA?')

% Save measurement in variable y

y = binblockread(v,'int8');

fread(v);
```

The lines of code to close the communication are the following,

```
% Clear object v

clrdevice(v);

% Close the communication with object v

fclose(v);

% Remove object v

delete(v);
```

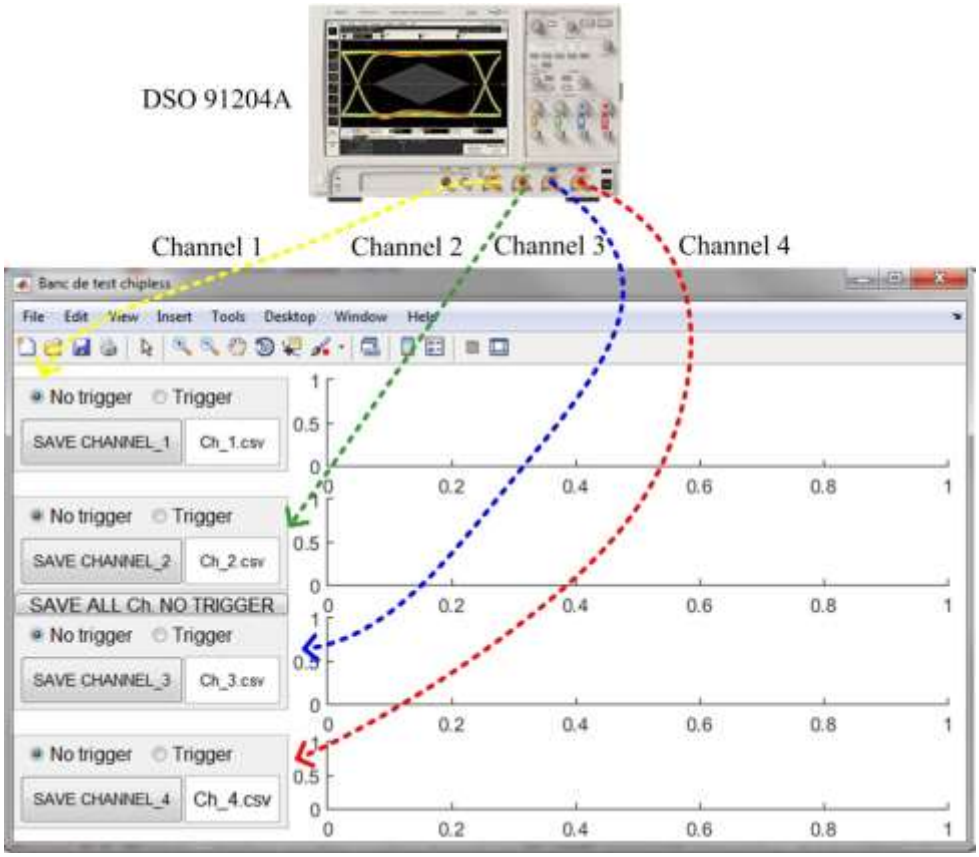


Figure A.1. Matlab GUI realized to acquire the Aglient 91204A DSO measuring data. It can save the data from all the four channels of the DSO.

Appendix 2

PC application software for first reader version in chapter 3

The first IR-UWB reader version, designed previous the beginning of the thesis, came with a dedicated application software for the PC. It was written in Matlab, and is based on different scripts that are called by the GUI shown in figure A.2. It expects the execution of a tag measurement according with the simple two measurements background subtraction procedure (tag and background measurements), without a calibrating tag. The GUI was designed to read the frequency coded tags presented in [VEN 13], which are based on coupled short-dipoles with REP and cross-polarization approach. They have been presented in chapter 1 section 3, and used along with the entire manuscript to characterize the performance of the designed readers. A photograph of the tag is also shown in figure A.2.

The GUI has two main columns, where the first controls the acquisition from the reader, and the second is in charge of post processing, and tag ID retrieving. On the top left to open the communication with the COM port of the reader, and to select the averaging factor. Once started the acquisition with the *Measure* command, the reader executes the reading process and transfers the results to the GUI, which will show it in time domain in the corresponding first window.

In the *Files* section, it is possible to memorize the acquired measurement pushing on the relative *save* button. The GUI requires two measurements in data base, the tag and background measurement to perform the post processing.

The RCS calculator section defines the timing window inside the frame of acquisition of 120 ns, where the tag decoding should be executed. The identifier section gives the possibility to correlate the response of the tag with the response of an ideal resonator, which is emulated in amplitude with a Gaussian function. Finally on the bottom, once retrieved the resonant frequencies of the measured tag, their position is compared with a data base, and the tag ID is given. According to the chapter 1 section 3, the backscattering measurement is

used only to characterize the coupling of the reader antennas (leakage). It is convenient to perform this calibration only one time in a practical application. Thereby the GUI is able to automatize the reading process in a loop execution of tag reading with the button *Read*, and selecting the checkbox *Loop*.

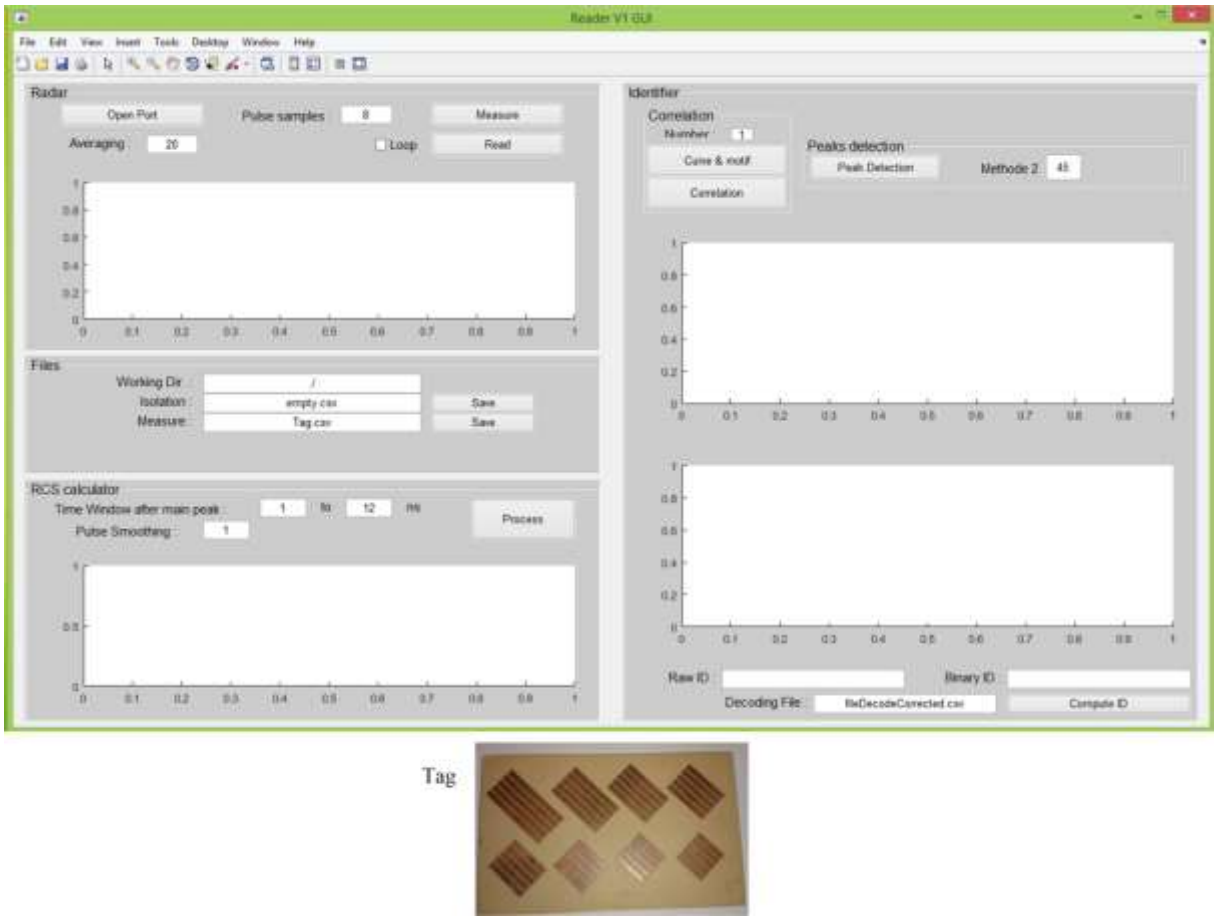


Figure A.2. *GUI realized in Matlab to read the tags shown in the figure, with the reader realized previous the beginning of the thesis. The tag was of the same family presented in [VEN 13], and used along with the entire manuscript to characterize the performance of the designed readers.*

2.1. PC - reader communication

The reader communicates with the PC using a USB port, where a UART is emulated. Inside the Xilinx SP601 FPGA evaluation board there is a CP2103GM chip from Silicon Labs, which is a USB-to-UART chip. It is connected with the FPGA from the UART side, and with the PC from the USB side. The Matlab GUI uses the Windows COM library to communicate

with the established COM connection with the reader. The GUI creates a serial port object called *s* with the following function,

```
s = serial(port,'BaudRate', 460800,'TimeOut', 80,'InputBuffer', 16384);
```

The BR is of 460.800 kb and the serial time-out is of 80 s, the latter covers the maximum time needed by the reader to complete an acquisition once received the command from the PC. For the maximum averaging of 128, it is of about 64 s.

The Matlab function in charge of communicating with the reader is called getRadarFrame(~,~). The chunk of code that queries the reader for a reading process, and retrieves the reader measured data, is the following.

```
% Get the averaging factor written in the corresponding editing box
avg = str2double(get(data.RadarAvg,'String'));
% Convert the averaging factor from double to string
str = sprintf('G%03d', avg);
% Transmit the command to the reader
fprintf(s, str);
% Receiving the information about the number of acquired points from the reader
numSamples = str2double(fgetl(s))
% Reading from the reader
Tampon = zeros(1, numSamples);
for i = 1 : numSamples
        Tampon(i) = str2double(fgetl(s))-512;
end
```

Appendix 3

Reader chapter 3 - FPGA Reader_0 block description

The block schematic of the custom Reader_0 block, implemented on the first reader prototype designed during the thesis, is shown in figure A.3. To simplify the comprehension of its operation, it is shown interfaced with the main components of the reader. It is composed of a User Block and a PLB slave interface. The former is the solely block that interacts with the reader analog board, it communicates with the FPGA microprocessor (microblaze 8.20a) through the PLB bus using the PLB slave interface.

3.1. User Logic description

The User Block contains a FIFO memory, which is directly connected with the output of the ADC, a main control unit and some blocks for synchronization purpose. The clock (called Master Clock) at 67 MHz is the temporization signal for the PLB bus and all the peripherals at which it is connected. From figure A.3 the input clock of the delay generator, in the reader RF front-end board, is the master clock, while its output is delayed depending on the *Frame_Step(10:0)* output of the control unit block. To accomplish with the equivalent time algorithm, the pulse generator is triggered by the Control Unit using as timing reference the master CLK, which is not delayed. The output of the delay generator is the sampling clock of the S/H amplifier. Thereby the trigger for the pulse generator and the sampling clock are dynamically delayed during the acquisition, depending on the *Frame_Step(10:0)* value. A copy of the sampling clock is an input for the Reader_0 custom peripheral, and is used as write clock for the FIFO memory.

The User Logic was written in VHDL using the Xilinx ISE design tool of the Xilinx ISE Design Suite 13.2. It was simulated before been integrated within the complete FPGA embedded system. The FIFO capacity is of 16 k words of 10 bits each, which represents the resolution of the ADC.

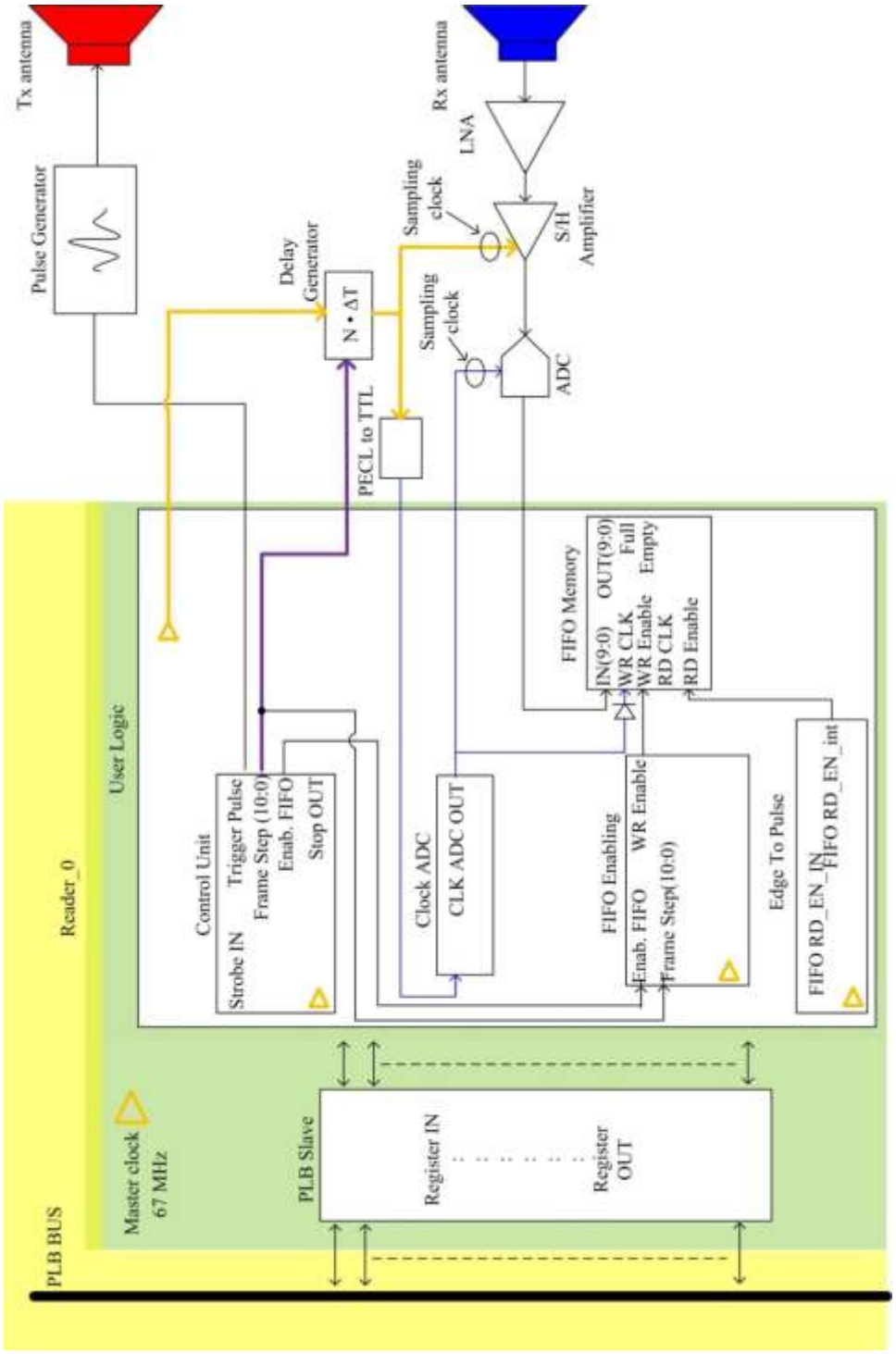


Figure A.3. *Block schematic of the Reader_0 PLB peripheral inside the FPGA of the reader presented in chapter 3. Its connections with the reader RF front-end board, and the trigger of the pulse generator, are also shown.*

The reader acquisition starts when the input strobe of the control unit block is at 1_2. After, the control unit sets up the *Frame_Step(10:0)* signal to 0_{10}, and transmits a trigger event to the pulse generator. The *FIFO_enabling* block waits for some master clock cycles before allowing the memorization of the ADC output inside the FIFO. This interval of time between triggering the pulse generator, and FIFO write enabling, settles the reader acquisition frame position which is fixed. After the FIFO remains in writing state for all the duration of the acquisition frame, this is of about 120 ns (eight master clock periods). At 120 ns corresponds eight points of the tag response sampled by the S/H amplifier, one each sampling clock period (≈15 ns). Once finished the acquisition from the FIFO, the *Control_Unit* updates the *Frame_Step(10:0)* by adding 1_{10}, and restarts with the same acquisition procedure until the *Frame_Step(10:0)* value is equal to 1499_{10} ((15 ns / 10 ps) -1). Finally, the C*ontrol_Unit* infers the *Stop_OUT* signal at 1_2 to inform the microprocessor. For each *Frame_Step(10:0)* increment, the total internal dynamic delay of the delay generator chips, is increased of 10 ps. A partial chronogram of the reader acquisition is shown in figure A.4. It is focused from the trigger event of the delay generator, to the memorization of the eight samples inside the User Logic FIFO memory for one value of *Frame_Step(10:0)*.

3.2. Microprocessor application software

The microprocessor can communicate with the Reader_0 block only through the registers of the Reader_0 PLB slave interface. The FIFO output data, the *full* and *empty* flags, and the *Stop_OUT* of the Control Unit are connected with one register of the PLB slave interface. In parallel, the *Strobe_IN* signal and the *FIFO_RD_EN_IN* are connected with another register of the same PLB slave interface. The *FIFO_RD_EN_IN* signal enables the reading process from the FIFO memory by the microprocessor.

At the end of the acquisition, the microprocessor downloads the FIFO content using the registers of the Reader_0 PLB slave interface. The microprocessor application program was written in C, and developed with Xilinx Software Development Kit. It uses the libraries with the driver for the FPGA internal blocks, and libraries of common C functions, such as the input output standard library stdio. A driver for the block Reader_0 was developed; it is based on a couple of simple functions able to access the registers of the PLB slave interface to communicate with the User Logic.

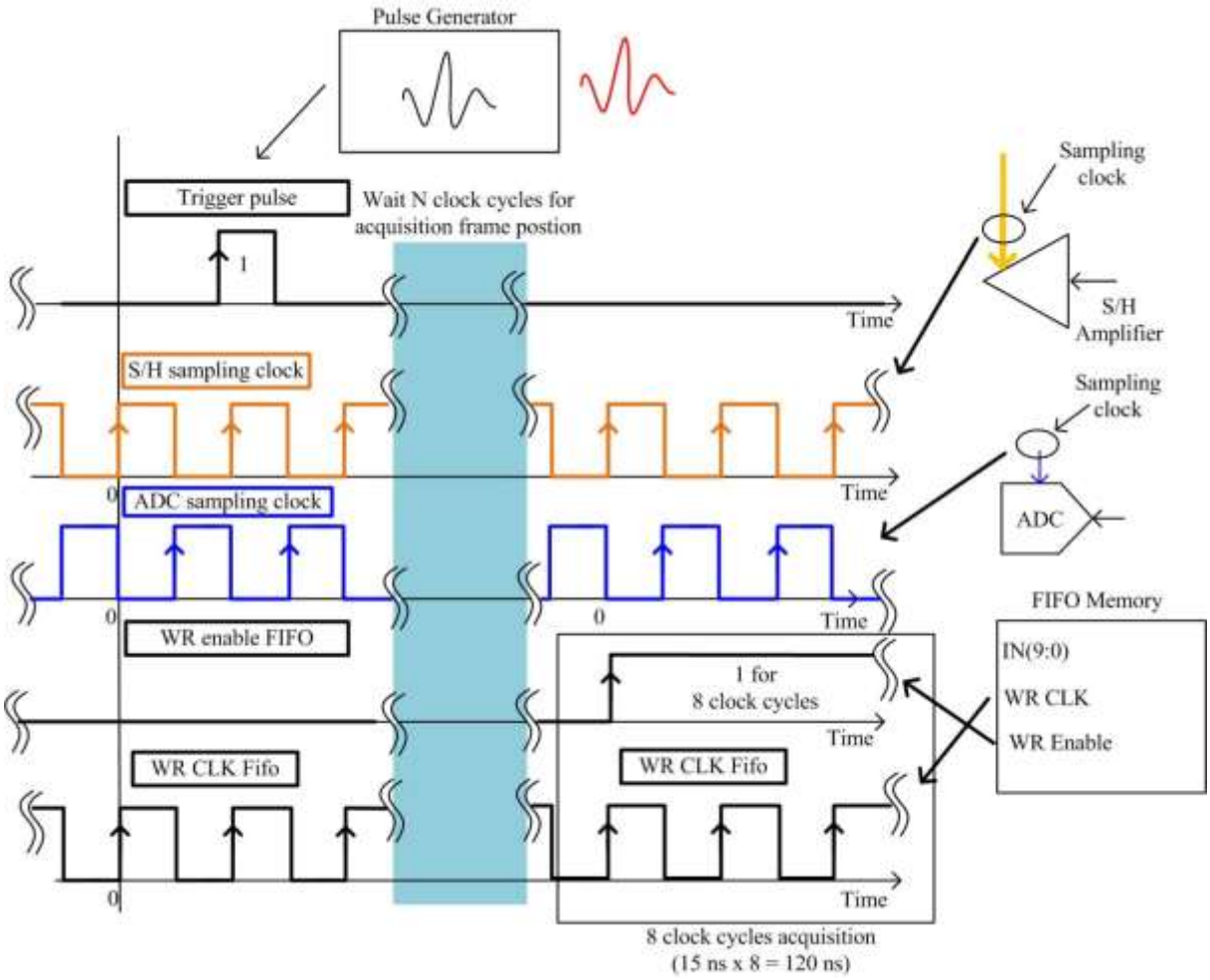


Figure A.4. *Partial chronogram of the reader acquisition. The control_unit of the User Logic triggers the pulse generator, after N clock cycles, the FIFO memory is enabled to acquire eight samples (ADC output) of the reader measuring signal.*

The driver for the Reader_0 was essential to start the acquisition from the User Logic, and also to empty out its internal FIFO at the end of the acquisition. It corresponds to retrieve the reader measured signal. The microprocessor application software starts testing internal and external peripherals, and enabling the microprocessor interrupts. Afterwards the microprocessor waits for the PC, through the UART, to have information about the required averaging factor essential to start the reading process. For an averaging of N, the User Logic executes for N times one row acquisition, and for each the microprocessor empties out the User Logic internal FIFO. All the data are transferred to one different column of a predefined matrix, inside the external DDR2 memory. Finally, the application performs the averaging of all the N columns row to row, and transfers the result to the PC with the UART.

3.3. Synchronization problems

From figure A.3 the Reader_0 block presents two clock signal, one is the master clock, and the other is the ADC and S/H amplifier sampling clock, which is represented in blue line inside the FPGA. The two clocks are progressively delayed depending on the delay of the delay block chips imposed by *Frame_Step(10:0)*. Working with two clocks with a not constant delay inside a digital architecture, such as an FPGA implementation, creates problems of synchronization and is metastability prone. In case of the reader custom peripheral Reader_0, the synchronization was affecting the FIFO memory operation. The acquisition of some points was shifted of one clock cycle going out of the predefined acquisition frame. This can be understood considering that the FIFO *WR_enable* signal is referred to master clock, and the FIFO *WR_CLK* to the sampling clock. Thus, the FIFO *WR_enable* may not respect the setup time relatively to the FIFO *WR_CLK,* when going to 1_2.

The block *FIFO_Enabling* has the signal *Frame_Step(10:0)* as input, therefore this block knows the dynamic delay imposed inside the external delay generator chips. Inside of this block a VHDL code was used either to anticipate or to postpone the rising edge of the FIFO *WR_enable* signal (0_2 to 1_2), with a resolution of half clock period. This procedure was executed for the values of *Frame_Step(10:0)* where a FIFO setup or hold time violation were noted. Unfortunately this solution may create some errors because the real delay between the master clock and the sampling clock cannot be characterized. Indeed the delay of a signal inside the FPGA may vary during the time, depending on the temperature of the chip. This imply that, the related clock events for the S/H amplifier, the ADC, and that of the FIFO *WR_CLK* should be in optimal positions to not affect the acquisition quality for eventual FPGA temperature gradients. This problem was faced in the second version of the reader presented in the chapter 4.

Appendix 4

External Flash

In figure A.5 is shown the block schematic of the FPGA embedded system of the reader presented in chapter 4. It has the W25Q64BV from Winbond as external Flash memory. Its capacity is of 64 Mb organized in 32,768 programmable pages of 256 bytes each. It has a Serial Peripheral Interface (SPI), which in this case is used to communicate with the FPGA. A dedicated FPGA internal controller communicates with the memory.

The FPGA Spartan 6 is a volatile device, as so it needs to be configured when it is powered up. The Spartan 6 hardware architecture is defined through its CMOS configuration laches (CCLs) memory, and different configuration modes are available. In the reader presented in chapter 3, all the FPGA configuration process, from CCLs to the download of the microprocessor application software inside the external DDR2 memory, was executed using the JTAG. Each time a user wanted to work with the reader, he had to use the Impact software from the Xilinx ISE Design Suite to program the FPGA (CCLs plus DDR2). This process is tedious because the downloading can take different seconds. The Flash memory is a not-volatile memory, and therefore can maintain the bitstream in its internal memory cells even though the power is off. The reader of chapter 4 was configured with the Master Serial/ SPI configuration mode x4 [XIL 17] using the Flash.

The FPGA bitstream, besides the hardware description data to be stored inside the FPGA CCLs memory, contains the microprocessor application software to be stored inside the FPGA BRAM. This is shown in figure A.6 (a), where the FPGA is not powered. At the FPGA power on, the device can be self-programmed, populating its CCLs memory and BRAM, using the selected Master Serial/ SPI configuration mode x4, as shown in figure A.6 (b). In case of the all the designed readers, the application software could not be fit inside the internal BRAM, and must reside in the external DDR2.

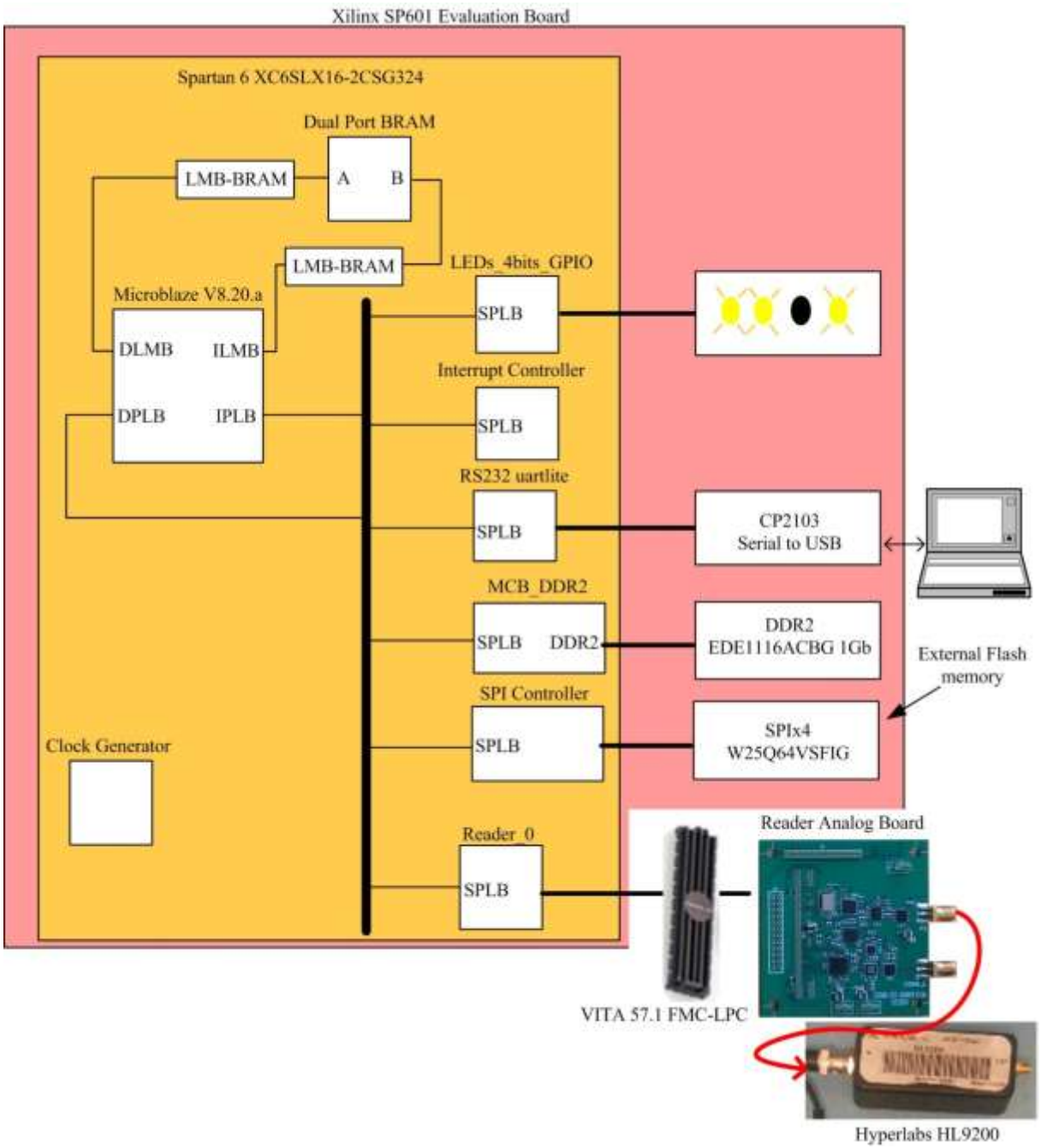


Figure A.5. *Block schematic of the FPGA embedded system: with the main peripherals of the digital board SP601 used to implement the reader in the chapter 3. The custom block Reader_0 is the solely that may communicate with the analog board and trigger the pulse generator.*

The Spartan 6 SPI interface for FPGA configuration purpose is only able to transfer data from the external Flash to the internal FPGA CCLs and BRAM. To download the application software from the Flash to the DDR2, a dedicated microprocessor software application is

needed. Thus, two microprocessor software applications were developed in C, using the Xilinx Software Development Kit. One was the bootloader that was used exclusively to transfer the other application software from the Flash to the DDR2. This application software is small in size, and must reside inside the BRAM of the FPGA, as so it was merged with the data for the CCLs forming one bitstream file. The main microprocessor application software for reading tags was splitted into two files, one for its vector section and the other one for the rest section. After they were downloaded in the Flash at non-contiguous memory addresses compared with the bitstream, this is shown in figure A.7 (a).

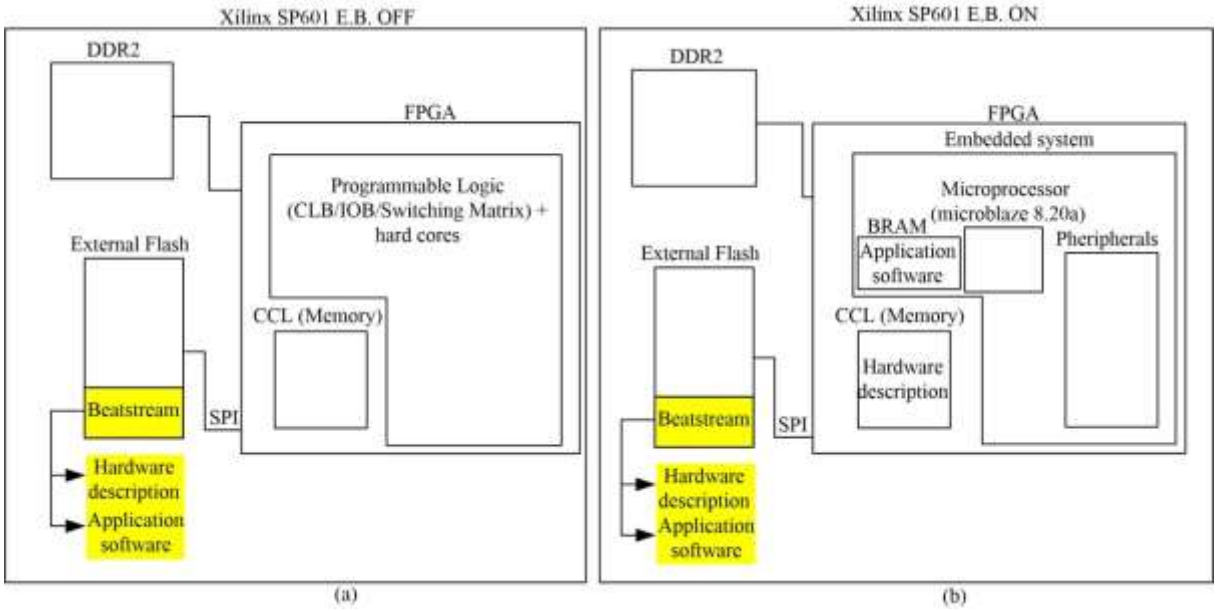


Figure A.6. *(a) Xilinx SP601 evaluation Board not powered up, with the bitstream, containing the hardware description and the microprocessor application software, on the external Flash memory. (b) At power up, the CCLs memory copies the part of the bitstream with hardware description, and the remaining part which is the microprocessor application software, is copied to the FPGA internal BRAM.*

The bootloader was written using the SPI protocol described in the Motorola M68HC11 data sheet [NXP 17], where the two Flash starting memory addresses, used for the microprocessor applications software files, were noted at the bootloader application. From figure A.7 (a), when the reader is off (no power), the microprocessor application software (vector section plus reset section), and the bitstream (Hardware description plus the bootloader) resides only in the Flash memory. At FPGA power up, first the FPGA CCLs gates are populated with the part of the bitstream that take care of the hardware description. After the rest of the bitstream, which contains the bootloader, is copied inside the FPGA

BRAM. This is show in figure A.7 (b). Finally the bootloader starts to copy the microprocessor application software (vector section plus reset section) from the Flash to the external DDR2, as shown in figure A.7 (c).

The Impact software tool from Xilinx ISE Design Suite was used to load the flash. It needs first to create a Programmable Read Only Memory (PROM) file, and after it may use the JTAG, which can access directly the FPGA SPI interface, to write inside the Flash. The PROM file was created according to the standard Intel MCS-86 Hexadecimal Object (MCS).

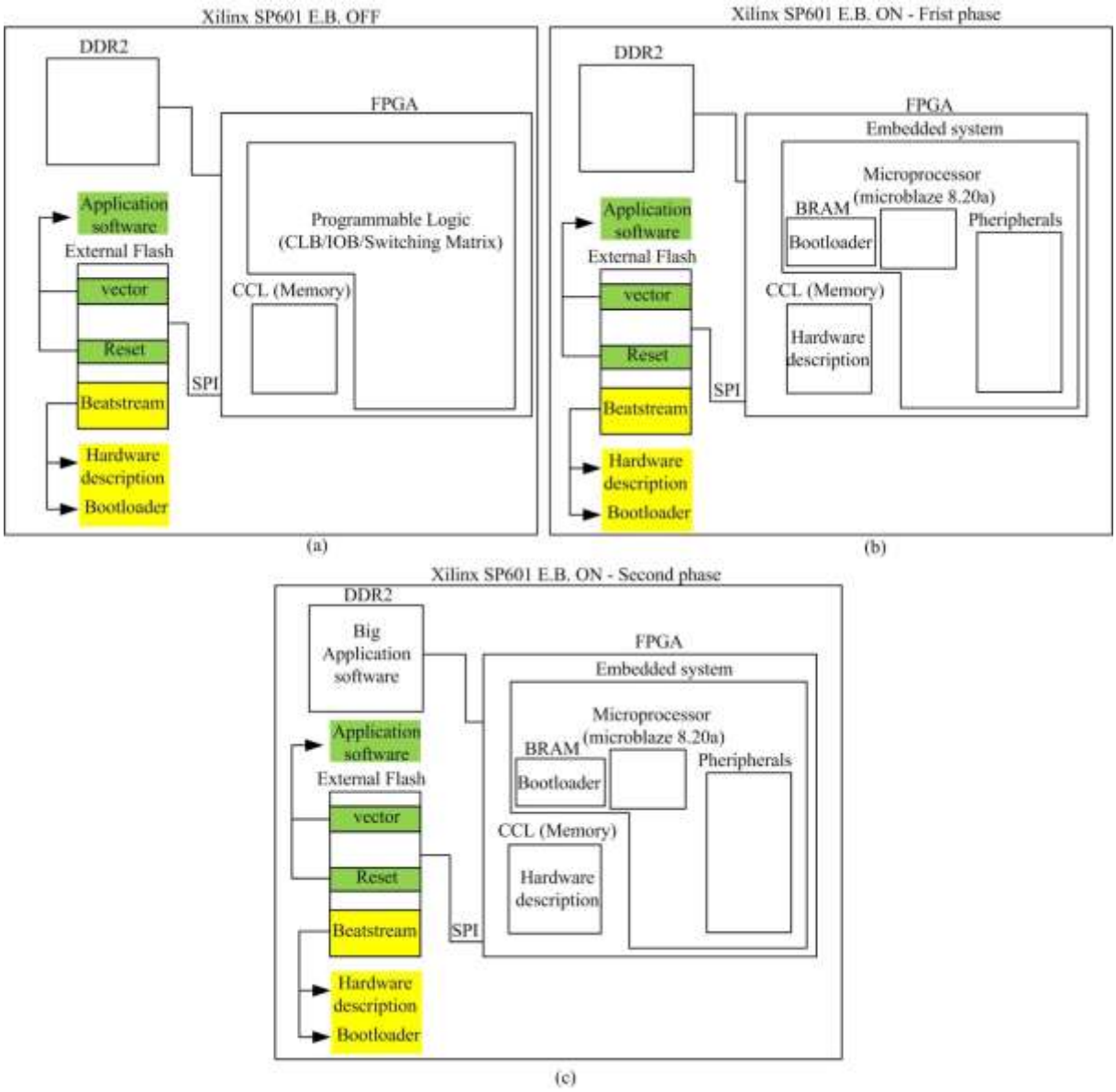


Figure A.7. *(a) Xilinx SP601 evaluation Board not powerd up, with the bitstream and the microprocessor application software on the external Flash memory. (b) First self-programming phase at power up, the CCLs memory copies the part of the bitstream with hardware description, and the rest (bootloader) is copied to the FPGA internal BRAM. (c) Second phase of the FPGA self-programming. The bootloader copies the main microprocessor program from the Flash to the external DDR2.*

Appendix 5

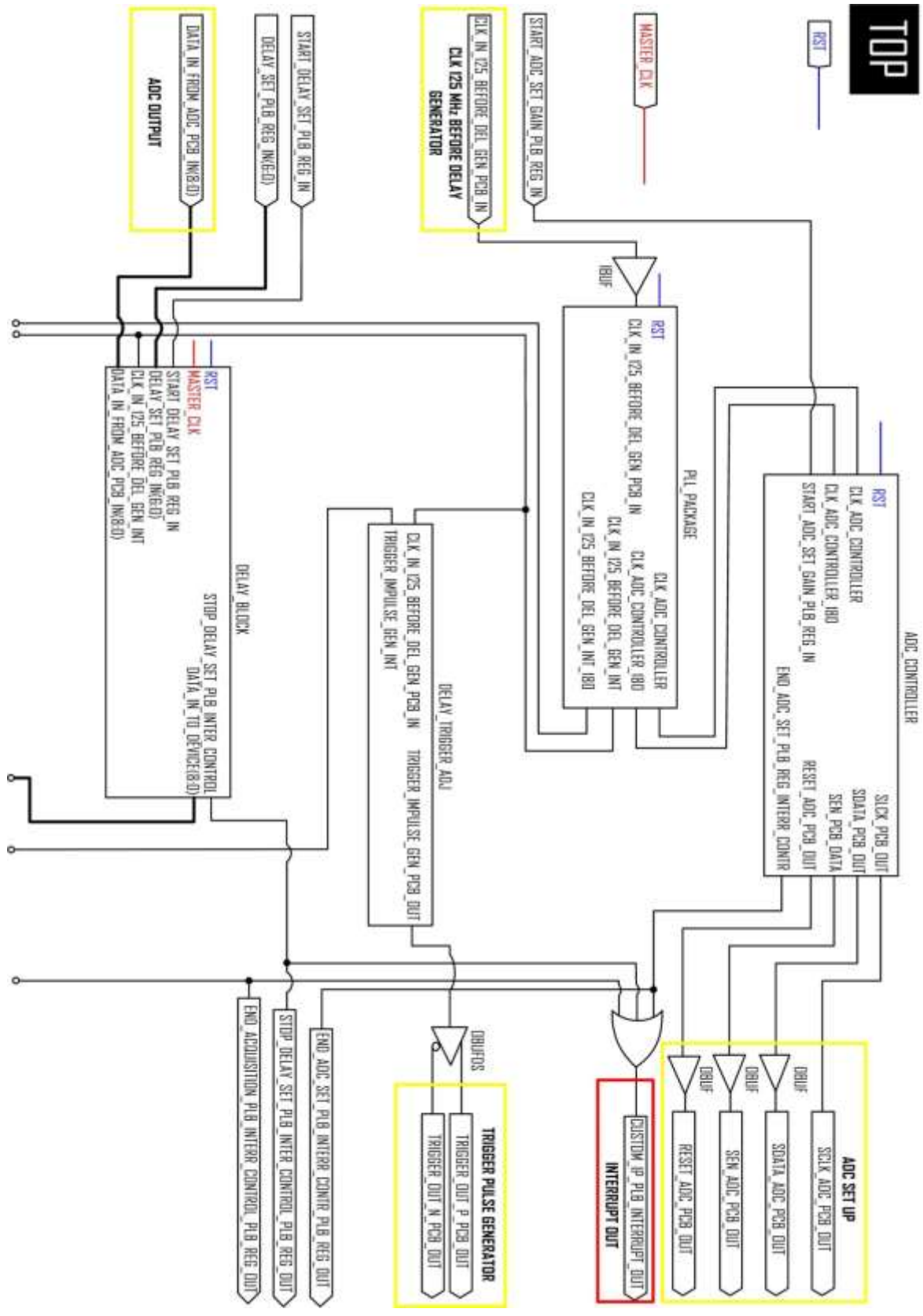
User Logic Reader chapter 4

The Reader_0 User Block is composed of three main control units called *ADC_CONTROLLER*, *DELAY_BLOCK*, and *ACQUISITION_CU_MG,* which are shown in figure A.8. Each of these three main control units can be activated independently from the input PLB slave interface registers. Once completed their operation, they can inform the microprocessor (microblaze v8.20a) with an interrupt request, using the signal *CUSTOM_IP_PLB_INTERRUPT_OUT*, and also using the output PLB slave interface registers.

The *ADC_CONTROLLER* is in charge of setting the external ADC gain in the RF front-end board. The ADC output signals, called *DATA_IN_FROM_ADC_PCB_IN(8:0)*, is memorized inside the smaller FIFO memory called *FIFO_FAST_SAMPLE_PACKAGE,* when required. Its capacity is of only 32 words of 9 bits (ADC bit capacity). The block *DELAY_BLOCK* delays the ADC output signals to be effectively memorized in the small memory, without violating FIFO setup and hold time. Finally, the *ACQUISITION_CU_MG* is in charge of the acquisition exploiting all the others blocks. In the next three sub-sections each control unit operation are described, starting from the *ADC_CONTROLLER.*

5.1. ADC_CONTROLLER

The reader ADC (ADS58B19) has a low speed serial communication interface, which is able to customize the converter operational characteristics. The ADC_CONTROLLER block inside User Block communicates with the ADC, through this serial interface, to set up the ADC internal gain to 3.5 dB. The PLL_PACKAGE exploits the Spartan 6 clock resources [XIL 15a], and embeds a PLL, which input is the 125 MHz clock generated inside the RF front-end, before be delayed by the delay generator (*CLK_IN_125_BEFORE_DEL_GEN_PCB_IN*). The PLL is used to clean up its input signal, to generate two out of phase clocks of 125 MHz, to provide the low frequency clock for the serial communication with the external ADC (about 5 MHz), and finally for synchronization purposes.


TOP
RST
MASTER_CLK
START_ADC_SET_GAIN_PLB_REG_IN
CLK_IN_125_BEFORE_DEL_GEN_PCB_IN
CLK 125 MHz BEFORE DELAY GENERATOR
DELAY_SET_PLB_REG_IN[6:0]
START_DELAY_SET_PLB_REG_IN
DATA_IN FROM_ADC_PCB_IN[8:0]
ADC OUTPUT
IBUF
PLL_PACKAGE
CLK_ADC_CONTROLLER
CLK_ADC_CONTROLLER_IBO
CLK_IN_125_BEFORE_DEL_GEN_INT
CLK_IN_125_BEFORE_DEL_GEN_INT_IBO
ADC_CONTROLLER
CLK_ADC_CONTROLLER
START_ADC_SET_GAIN_PLB_REG_IN
END_ADC_SET_PLB_REG_INTERR_CONTR
SCLK_PCB_OUT
SDATA_PCB_OUT
SEN_PCB_DATA
RESET_ADC_PCB_OUT
DELAY_BLOCK
STOP_DELAY_SET_PLB_INTER_CONTROL
DATA_IN_TO_DEVICE[8:0]
DELAY_TRIGGER_ADJ
TRIGGER_IMPULSE_GEN_INT
TRIGGER_IMPULSE_GEN_PCB_OUT
OBUFDS
OBUF
ADC SET UP
SCLK_ADC_PCB_OUT
SDATA_ADC_PCB_OUT
SEN_ADC_PCB_OUT
RESET_ADC_PCB_OUT
TRIGGER PULSE GENERATOR
TRIGGER_OUT_P_PCB_OUT
TRIGGER_OUT_N_PCB_OUT
CUSTOM_IP_PLB_INTERRUPT_OUT
INTERRUPT OUT
END_ADC_SET_PLB_INTERR_CONTR_PLB_REG_OUT
STOP_DELAY_SET_PLB_INTER_CONTROL_PLB_REG_OUT
END_ACQUISITION_PLB_INTERR_CONTROL_PLB_REG_OUT

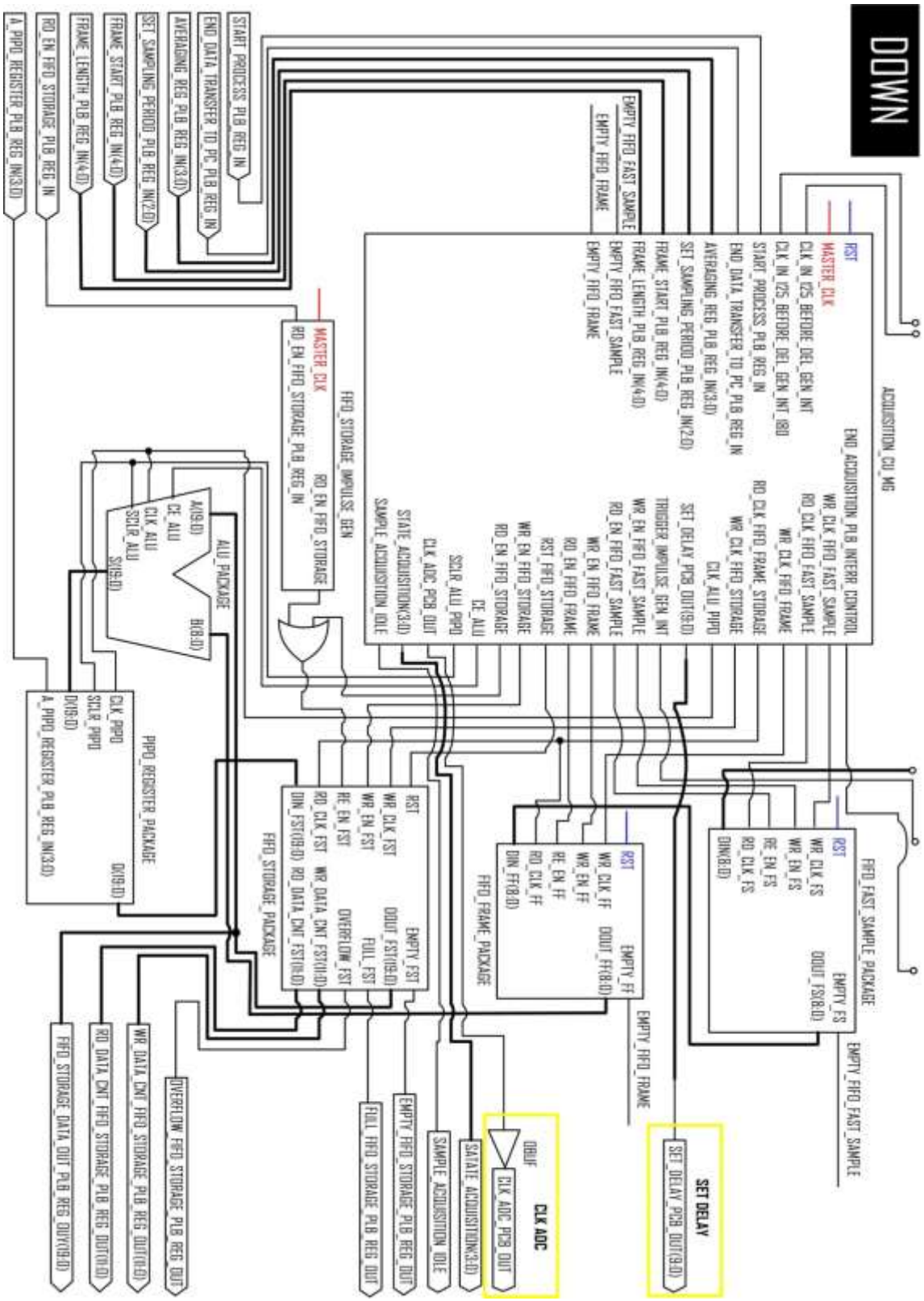

DOWN
ACQUISITION_CU_MG
RST
MASTER_CLK
CLK_IN_I2S_BEFORE_DEL_GEN_INT
CLK_IN_I2S_BEFORE_DEL_GEN_INT_180
START_PROCESS_PLB_REG_IN
END_DATA_TRANSFER_TO_PC_PLB_REG_IN
AVERAGING_REG_PLB_REG_IN(3:0)
SET_SAMPLING_PERIOD_PLB_REG_IN(2:0)
FRAME_START_PLB_REG_IN(4:0)
FRAME_LENGTH_PLB_REG_IN(4:0)
EMPTY_FIFO_FAST_SAMPLE
EMPTY_FIFO_FRAME
END_ACQUISITION_PLB_INTERR_CONTROL
WR_CLK_FIFO_FAST_SAMPLE
RD_CLK_FIFO_FAST_SAMPLE
WR_CLK_FIFO_FRAME
RD_CLK_FIFO_FRAME_STORAGE
WR_CLK_FIFO_STORAGE
CLK_ALU_PIPD
SET_DELAY_PCB_OUT(9:0)
TRIGGER_IMPULSE_GEN_INT
WR_EN_FIFO_FAST_SAMPLE
RD_EN_FIFO_FAST_SAMPLE
WR_EN_FIFO_FRAME
RD_EN_FIFO_FRAME
RST_FIFO_STORAGE
WR_EN_FIFO_STORAGE
RD_EN_FIFO_STORAGE
CE_ALU
SCLR_ALU_PIPD
CLK_ADC_PCB_OUT
STATE_ACQUISITION(3:0)
SAMPLE_ACQUISITION_IDLE
FIFO_FAST_SAMPLE_PACKAGE
RST
WR_CLK_FS
WR_EN_FS
RE_EN_FS
RD_CLK_FS
DIN(8:0)
EMPTY_FS
DOUT_FS(8:0)
EMPTY_FIFO_FAST_SAMPLE
SET DELAY
SET_DELAY_PCB_OUT(9:0)
FIFO_FRAME_PACKAGE
RST
WR_CLK_FF
WR_EN_FF
RE_EN_FF
RD_CLK_FF
DIN_FF(8:0)
EMPTY_FF
DOUT_FF(8:0)
EMPTY_FIFO_FRAME
CLK ADC
OBUF
CLK_ADC_PCB_OUT
SAMPLE_ACQUISITION_IDLE
STATE_ACQUISITION(3:0)
EMPTY_FIFO_STORAGE_PLB_REG_OUT
FULL_FIFO_STORAGE_PLB_REG_OUT
FIFO_STORAGE_PACKAGE
RST
WR_CLK_FST
WR_EN_FST
RE_EN_FST
RD_CLK_FST
DIN_FST(18:0)
EMPTY_FST
DOUT_FST(18:0)
FULL_FST
OVERFLOW_FST
WR_DATA_CNT_FST(11:0)
RD_DATA_CNT_FST(11:0)
OVERFLOW_FIFO_STORAGE_PLB_REG_OUT
WR_DATA_CNT_FIFO_STORAGE_PLB_REG_OUT(11:0)
RD_DATA_CNT_FIFO_STORAGE_PLB_REG_OUT(11:0)
FIFO_STORAGE_DATA_OUT_PLB_REG_OUT(19:0)
FIFO_STORAGE_IMPULSE_GEN
MASTER_CLK
RD_EN_FIFO_STORAGE_PLB_REG_IN
RD_EN_FIFO_STORAGE
ALU_PACKAGE
A(19:0)
CE_ALU
CLK_ALU
SCLR_ALU
S(19:0)
B(18:0)
PIPD_REGISTER_PACKAGE
CLK_PIPD
SCLR_PIPD
DI(18:0)
DO(19:0)
A_PIPD_REGISTER_PLB_REG_IN(3:0)
START_PROCESS_PLB_REG_IN
END_DATA_TRANSFER_TO_PC_PLB_REG_IN
AVERAGING_REG_PLB_REG_IN(3:0)
SET_SAMPLING_PERIOD_PLB_REG_IN(2:0)
FRAME_START_PLB_REG_IN(4:0)
FRAME_LENGTH_PLB_REG_IN(4:0)
RD_EN_FIFO_STORAGE_PLB_REG_IN
A_PIPD_REGISTER_PLB_REG_IN(3:0)

Figure A.8. *Block schematic of the top User Logic block of Reader_0. It set up the ADC internal gain to 3.5 dB using a low speed (5 MHz) serial peripheral. It delays the ADC output signals before reaching the FIFO_FAST_SAMPLE_PACKAGE memory, and finally performs the real acquisition ruled by the ACQUISITION_CU_MG block.*

5.2. DELAY_BLOCK

In order to respect the *FIFO_FAST_SAMPLE_PACKAGE* memory setup and hold time, the data output of the ADC (*DATA_IN_FROM_ADC(8:0)*) are properly delayed with the *DELAY_BLOCK* block in writing operation. Internally at the block is implemented an *IODELAY2* capable of a variable delay generator with step of about 40 ps [XIL 15b]. The input signal *DELAY_SET_PLB_REG_IN(6:0)* is used to settle the correct delay quantity, and the signal *STOP_DEL_SET_INTER_CONTROL* to inform when the delay is properly resolved.

To obtain the correct value of the delay with *DELAY_SET_PLB_REG_IN(6:0),* was sufficient to test the reader with known signals and check the reading results. Thus, the calibration process was executed only one time during reader debagging.

5.3. ACQUISITION_CU_MG

The control unit of the sequential equivalent time algorithm during the reader acquisition process is the *ACQUISITION_CU_MG*. The simplified execution of the *ACQUISITION_CU_MG* block may be synthetize with the flow chart of figure A.9. It is put in relation with the equivalent time algorithm shown also in figure 3.3 of chapter 3, and executes the following operations:

1. It reset all the memories and start the acquisition

2. It sets the delay of the delay generator external chip with the signal *SET_DELAY_PCB_OUT(9:0)*. After it triggers the pulse generator using the block *DELAY_TRIGGER_ADJ*, and finally acquire few points of the ADC output, which are memorized in *FIFO_FAST_SAMPLE_PACKAGE*.

3. It transfers the content of the *FIFO_FAST_SAMPLE_PACKAGE* to the bigger *FIFO_FRAME_PACKAGE*.

4. It updates the delay generator external chip (current delay plus ΔT), and restarts from point 2 if the delay is different from the S/H amplifier sampling period of 8 ns -

ΔT. Differently, the sequential equivalent time algorithm is accomplished, and the reader measured signal is in the memory *FIFO_FRAME_PACKAGE*. After it performs the fast hardware averaging algorithm explained in chapter 4 sub-section 4.1.3. If the number of executed acquisitions is equal to the reader averaging factor, it informs the microprocessor with an interrupt, otherwise it starts a new acquisition from 1.

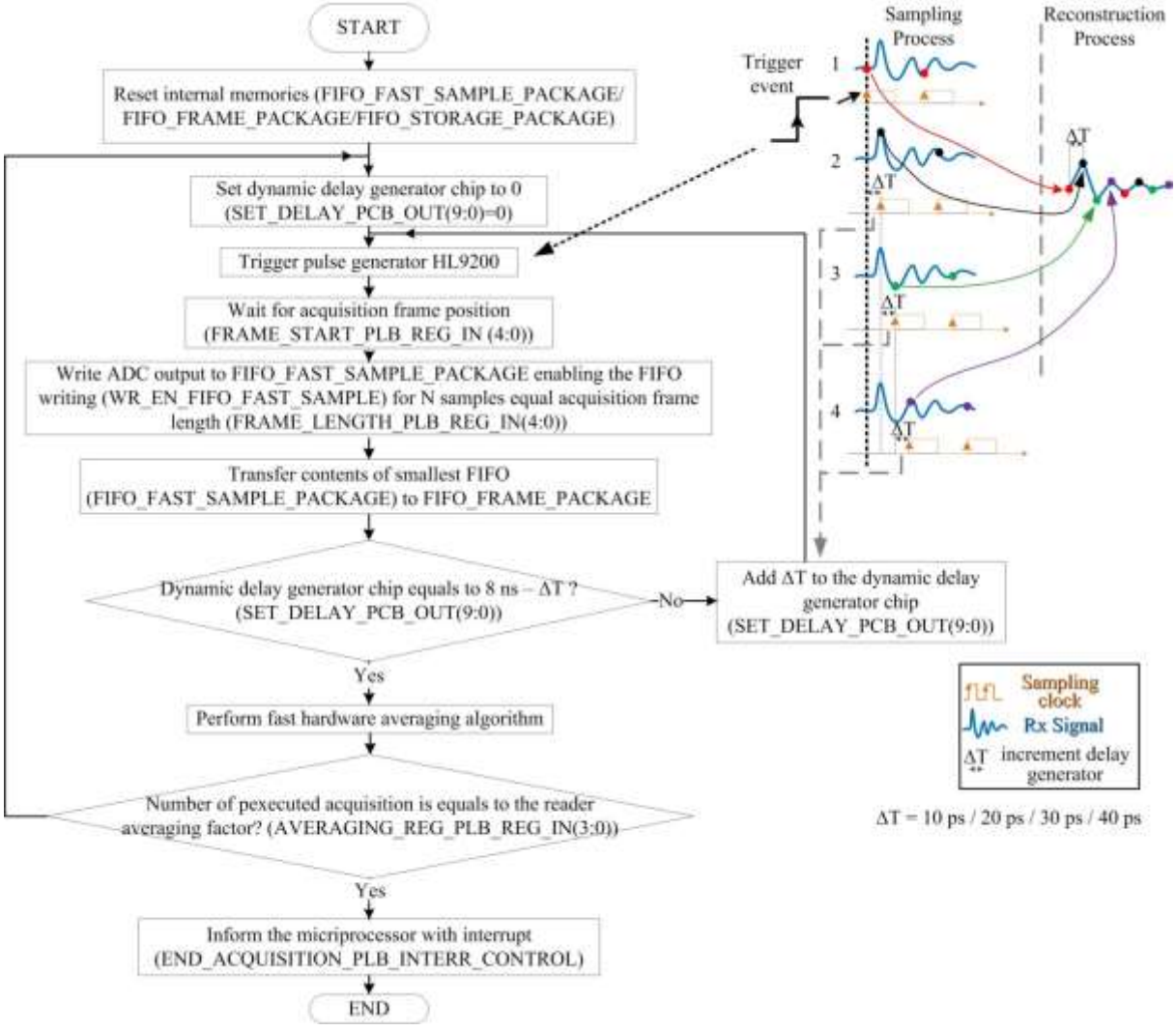


Figure A.9. *Simplified flow-chart of the ACQUISITION_CU_MG control unit. It is put in relation with the equivalent time algorithm shown also in figure 3.3 of chapter 3.*

The *ACQUISITION_CU_MG* block schematic is shown in figure A.10, it is composed of a control unit *INTERNAL_CU* that takes care of all the others blocks, each performing one independent operation.

The *SET_DELAY_GENERATOR* is in charge of varying the dynamic delay of the delay generator chip on the RF front-end board. The *SAMPLING_ACQUISITION* block controls the acquisition of the ADC output to the smaller *FIFO_FAST_SAMPLE_PACKAGE* memory. The block TRASFER_TO_FIFO_FRAME transfers the content of the *FIFO_FAST_SAMPLE_PACKAGE* to the bigger *FIFO_FRAME_PACKAGE.* Finally, the *PERFORM_AVERAGING* block executes the fast hardware averaging algorithm explained in chapter 4. It is accomplished with the memories *FIFO_FRAME_PACKAGE* and *FIFO_STORAGE_PACKAGE,* the *ALU_PACKAGE*, and finally with the *PIPO_REGISTER_PACKAGE*.

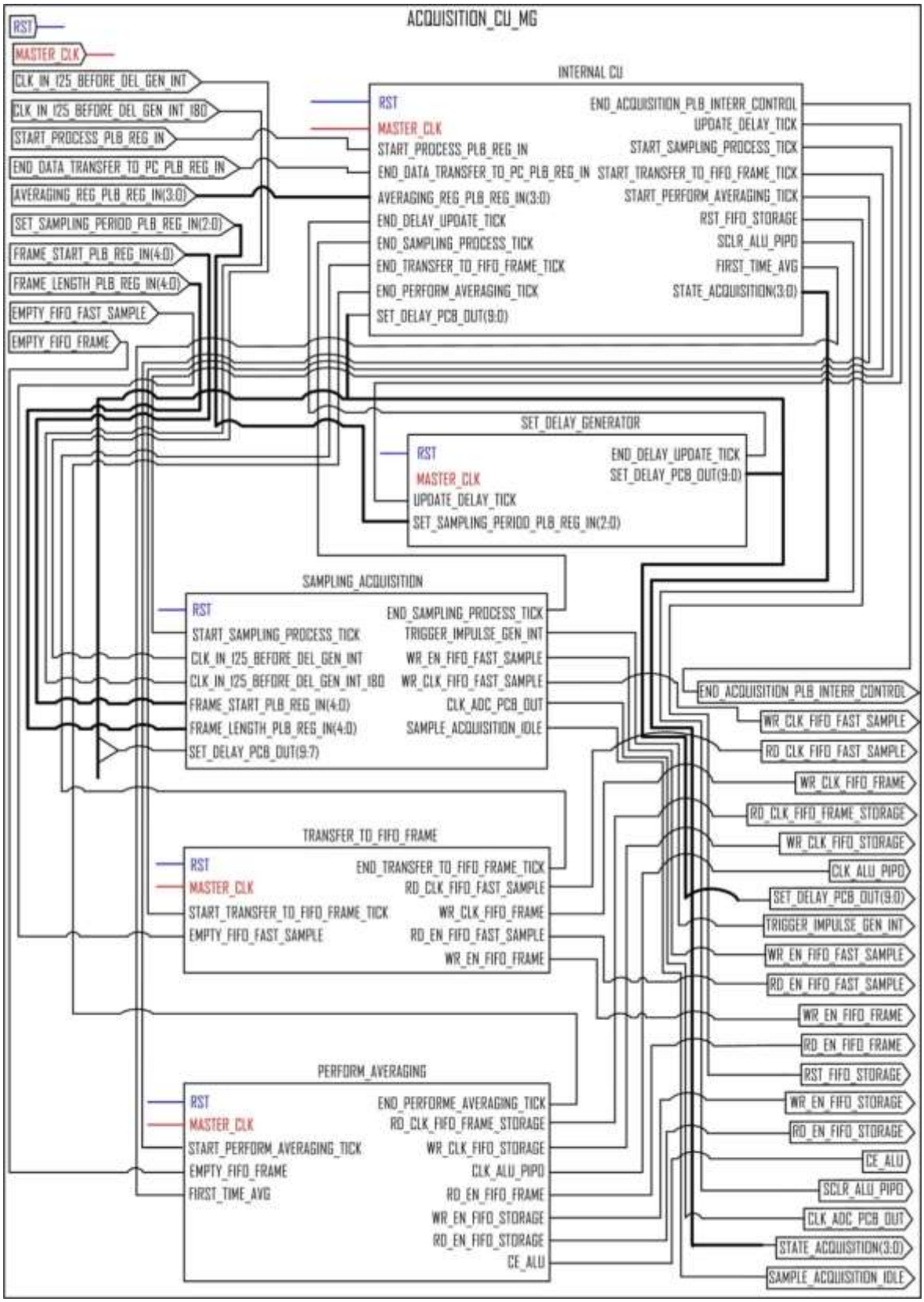

ACQUISITION_CU_MG
RST
MASTER_CLK
CLK_IN_125_BEFORE_DEL_GEN_INT
CLK_IN_125_BEFORE_DEL_GEN_INT_180
START_PROCESS_PLB_REG_IN
END_DATA_TRANSFER_TO_PC_PLB_REG_IN
AVERAGING_REG_PLB_REG_IN(3:0)
SET_SAMPLING_PERIOD_PLB_REG_IN(2:0)
FRAME_START_PLB_REG_IN(4:0)
FRAME_LENGTH_PLB_REG_IN(4:0)
EMPTY_FIFO_FAST_SAMPLE
EMPTY_FIFO_FRAME
INTERNAL CU
RST
MASTER_CLK
START_PROCESS_PLB_REG_IN
END_DATA_TRANSFER_TO_PC_PLB_REG_IN
AVERAGING_REG_PLB_REG_IN(3:0)
END_DELAY_UPDATE_TICK
END_SAMPLING_PROCESS_TICK
END_TRANSFER_TO_FIFO_FRAME_TICK
END_PERFORM_AVERAGING_TICK
SET_DELAY_PCB_OUT(9:0)
END_ACQUISITION_PLB_INTERR_CONTROL
UPDATE_DELAY_TICK
START_SAMPLING_PROCESS_TICK
START_TRANSFER_TO_FIFO_FRAME_TICK
START_PERFORM_AVERAGING_TICK
RST_FIFO_STORAGE
SCLR_ALU_PIPD
FIRST_TIME_AVG
STATE_ACQUISITION(3:0)
SET_DELAY_GENERATOR
RST
MASTER_CLK
UPDATE_DELAY_TICK
SET_SAMPLING_PERIOD_PLB_REG_IN(2:0)
END_DELAY_UPDATE_TICK
SET_DELAY_PCB_OUT(9:0)
SAMPLING_ACQUISITION
RST
START_SAMPLING_PROCESS_TICK
CLK_IN_125_BEFORE_DEL_GEN_INT
CLK_IN_125_BEFORE_DEL_GEN_INT_180
FRAME_START_PLB_REG_IN(4:0)
FRAME_LENGTH_PLB_REG_IN(4:0)
SET_DELAY_PCB_OUT(9:7)
END_SAMPLING_PROCESS_TICK
TRIGGER_IMPULSE_GEN_INT
WR_EN_FIFO_FAST_SAMPLE
WR_CLK_FIFO_FAST_SAMPLE
CLK_ADC_PCB_OUT
SAMPLE_ACQUISITION_IDLE
TRANSFER_TO_FIFO_FRAME
RST
MASTER_CLK
START_TRANSFER_TO_FIFO_FRAME_TICK
EMPTY_FIFO_FAST_SAMPLE
END_TRANSFER_TO_FIFO_FRAME_TICK
RD_CLK_FIFO_FAST_SAMPLE
WR_CLK_FIFO_FRAME
RD_EN_FIFO_FAST_SAMPLE
WR_EN_FIFO_FRAME
PERFORM_AVERAGING
RST
MASTER_CLK
START_PERFORM_AVERAGING_TICK
EMPTY_FIFO_FRAME
FIRST_TIME_AVG
END_PERFORME_AVERAGING_TICK
RD_CLK_FIFO_FRAME_STORAGE
WR_CLK_FIFO_STORAGE
CLK_ALU_PIPD
RD_EN_FIFO_FRAME
WR_EN_FIFO_STORAGE
RD_EN_FIFO_STORAGE
CE_ALU
END_ACQUISITION_PLB_INTERR_CONTROL
WR_CLK_FIFO_FAST_SAMPLE
RD_CLK_FIFO_FAST_SAMPLE
WR_CLK_FIFO_FRAME
RD_CLK_FIFO_FRAME_STORAGE
WR_CLK_FIFO_STORAGE
CLK_ALU_PIPD
SET_DELAY_PCB_OUT(9:0)
TRIGGER_IMPULSE_GEN_INT
WR_EN_FIFO_FAST_SAMPLE
RD_EN_FIFO_FAST_SAMPLE
WR_EN_FIFO_FRAME
RD_EN_FIFO_FRAME
RST_FIFO_STORAGE
WR_EN_FIFO_STORAGE
RD_EN_FIFO_STORAGE
CE_ALU
SCLR_ALU_PIPD
CLK_ADC_PCB_OUT
STATE_ACQUISITION(3:0)
SAMPLE_ACQUISITION_IDLE

Figure A.10. *The ACQUISITION_CU_MG block schematic. It is composed of a control unit INTERNAL_CU that takes care of all the others blocks, each performing one independent operation during the reader measurement process.*

Appendix 6

Matlab GUI reader chapter 4

The Matlab GUI for the reader proposed in chapter 4 is shown in figure A.11. It presents the same tag post-processing treatment of the GUI for the reader in chapter 3, with the addition of the STFT shown with spectrogram utility. In [RAM 16] the STFT for REP based UWB frequency-coded chipless RFID tags is studied. According to [RAM 16] the spectrogram was integrated in time domain between *start point integration* and *stop point integration.* The STFT window was rectangular and its duration settled with *DURATION SUB-WINDOW.* As a result of the reader performance and post processing STFT implementation, the background measurement may sometimes be omitted, and therefore two pop-up menu of the matlab GUI lets to select for it.

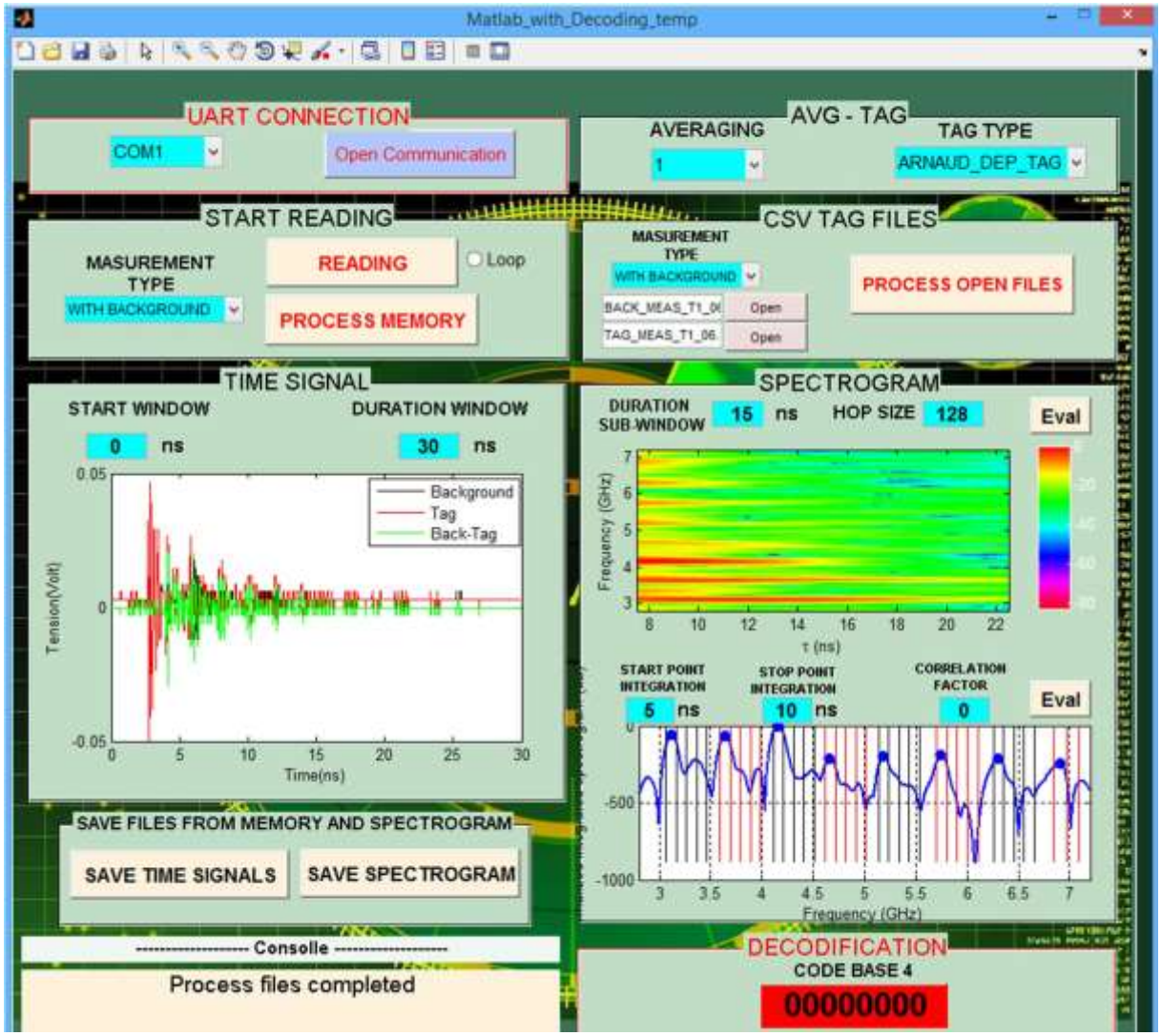


Figure A.11. *Reader Matlab GUI of chapter 4. With respect to the GUI for the reader version developed before the starting of the thesis, it introduces the STFT analysis.*

Appendix 7

Schematic power supply board reader chapter 4

In figure A.12 is shown the schematic of the power supply board realized for the reader presented in chapter 4. It generates the required voltage values for the RF front-end from the two 12 V pins available on the Xilinx FPGA evaluation board SP601.

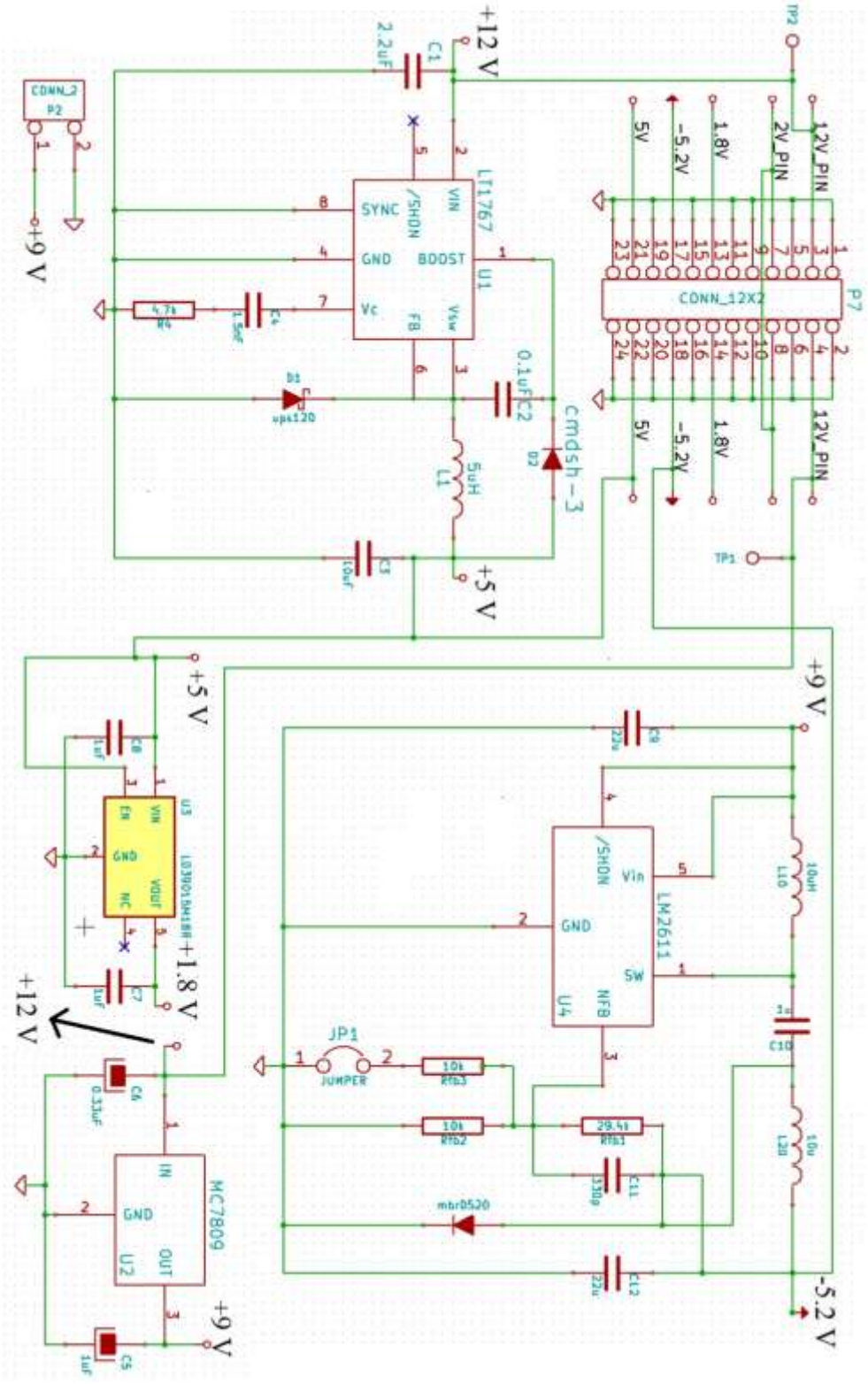


Figure A.12. *Power supply board schematic of the reader on chapter 4.*

Appendix 8

Matlab GUI acquisition software for VNA N5222A performing balanced measurement

To simplify the use of the VNA N5222A, when performing balanced measurement, a user friendly GUI in Matlab has been realized. It is interactive and changes items visibility based on the current connection state. A console is used to inform the user about the measurement evolution. The GUI at the software initialization is shown in figure A.13 (a). It expects the selection of one or both balanced measurements Scd21 and Scc21, in true-mode or not. After the software is in communication with the VNA, the GUI changes its appearance as shown in figure A.13 (b).

The power and/or the phase between the signals of the two physical ports 2 and 4 of logic port 2 may be varied. The power variation range is retained between ±15 dB to avoid possible VNA error message. The option *offset as fixture* is also selectable. Varying the power offset in true-mode corresponds to a variation *of* α_t between the range [10 - 80] deg as shown in chapter 6 table 6.1. Finally the GUI allows for an internal averaging of the measured results beside that one of the VNA. It consists on performing several queries of measurement process at the VNA.

To use the Matlab environment to communicate with the VNA, the Intrument Control Toolbox needs to be installed on the PC. It contains a library of functions that can exploit the Agilent IO Libraries Suite, which is a collection of libraries and utility software to enable the communication with the instrument. Between the others it contains the VISA libraries that were used by the developed Matlab GUI.

To established the communication with the VNA the following lines of code are used,

```
% Create the Visa object obj1 for the VNA, using the USB interface
obj1 = visa('AGILENT', 'USB0::0x0957::0x0118::MY51421171::0::INSTR');
% Set input buffer size for largest possible read of 32001 points in float32 (32001*4*2)
```

```
set(obj1,'InputBufferSize', 260000);
% Opening the communication with the VNA
fopen(obj1);
% Active continuously trigger system
fwrite(obj1, 'INIT:CONT ON');
% Single precision floating points (32 bit)
fwrite(obj1, 'FORM REAL, 32');
% Byte orders (LSB first – little-endian)
fwrite(obj1, 'FORM:BORD SWAP');
%Delete all measurements on VNA (clean the VNA)
fprintf(obj1, 'CALC:PAR:DEL:ALL');
```

To set up a differential measurement the following code is used. It refers the case of Scc21, for Sdc21 a similar code can be used.

```
%Define one measurement
fwrite(obj1,'CALC:PAR:DEF:EXT "MYSCC12","S11"');
%Select the measurement just created
fwrite(obj1,'CALC:PAR:SEL "MYSCC12"');
% Set balanced parameters ON
fwrite(obj1,'CALC:FSIM:BAL:PAR:STAT ON');
% Set balanced transformation to BBAL (balance to balance )
fwrite(obj1,'CALC:FSIM:BAL:DEV BBAL');
% Allow for variable phase offset between physical ports of the same logic port
fwrite(obj1,'CALC:FSIM:BAL:FIXT:OFFS:PHAS OFF')
% Allow for variable power offset between physical ports of the same logic port
fwrite(obj1,'CALC:FSIM:BAL:FIXT:OFFS:POW OFF');
% Define balanced measurement to SCC12
fwrite(obj1,'CALC:FSIM:BAL:PAR:BBAL:DEF SCC12');
% Display trace
fwrite(obj1,'DISP:WIND1:TRAC1:FEED "MYSCC12"');
if(TRUEMODE)
        % Enable true mode measurement
        fwrite(obj1,'CALC:FSIM:BAL:STIM:MODE TM');
else
        fwrite(obj1,'CALC:FSIM:BAL:STIM:MODE SE'); % Single-Ended stimulus
 end;
```

To vary the power offset or the phase offset on the balance port 2:

```
fprintf(obj1,'CALC:FSIM:BAL:BPOR2:OFFS:PHAS %g',phase_i);

fprintf(obj1,'CALC:FSIM:BAL:BPOR2:OFFS:POW %g',power_t);
```

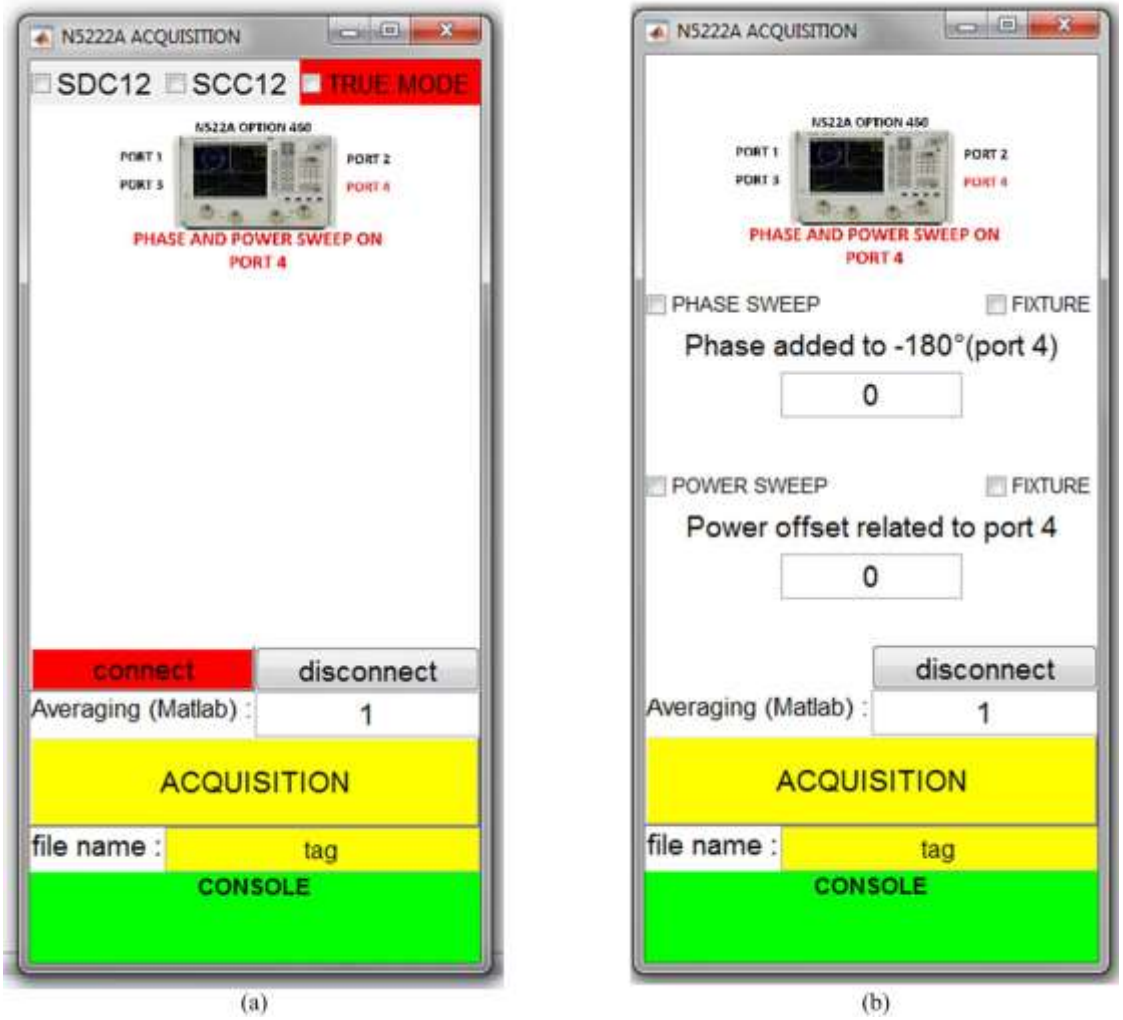


Figure A.13. *Matlab GUI realized to acquire the Agilent N5222A VNA measuring data in balanced mode.(a) GUI that appears at software initialization before selecting the wanted measurements (Sdc12-Scc12) and before be connected with the VNA. (b) GUI after the selection of measurement and connection. It is interactive and change items visibility based on the current connection state. A console is used to inform the user about the measurement evolution.*

9. References

[NXP 17] NXP, “M68HC11 Reference Manual”, Online available at: https://www.nxp.com.

[RAM 16] RAMOS A., PERRET E., RANCE O., et al., ”Temporal Separation Detection for Chipless Depolarizing Frequency-Coded RFID,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 7, pp. 2326-2337, July 2016.

[VEN 13] VENA A., PERRET E., TEDJINI S., "A Depolarizing Chipless RFID Tag for Robust Detection and Its FCC Compliant UWB Reading System," *IEEE Transactions on Microwave Theory and Techniques*, Vol. 61, No. 8, pp. 2982-2994, Aug. 2013.

[XIL 15a] XILINX, “Spartan-6 FPGA Clocking Resources, User Guide,” 2015, Online available at: https://www.xilinx.com.

[XIL 15b] XILINX, “Spartan-6 FPGA SelectIO Resources User Guide,” 2015, Online available at: https://www.xilinx.com.

[XIL 17] XILINX, “Spartan-6 FPGA Configuration,” 2017, online available at: www.xilinx.com.

List of publications

International journals with reviewing committee:

1. **M. Garbati**, R. Siragusa, E. Perret, and C. Halopé, "Impact of an IR-UWB Reading Approach on Chipless RFID Tag", *IEEE Microwave and Wireless Components Letters*, Vol 27, Issue 7, pp 678 - 680, June 2017.

2. **M. Garbati**, E. Perret, R. Siragusa, and C. Halopé, "Ultra-Low-Jitter Fully Tunable Baseband Pulse Generator for UWB Applications", *IEEE Transaction on Microwave Theory and Technique*, Vol PP, Issue 99, pp 1-11, July 2017.

3. **M. Garbati**, E. Perret, R. Siragusa, and C. Halopé, "UWB Chipless RFID – the Reader Technology from SFCW to IR-UWB", *IEEE Microwave Magazine*, Accepted August 2017.

4. **M. Garbati**, E. Perret, R. Siragusa, and C. Halopé, "Towards Chipless RFID Reading Systems Independent of Tag Orientation", *IEEE Microwave and Wireless Components Letters*, Vol 27, Issue 11, September 2017.

International conferences with selection committee:

1. **M. Garbati**, R. Siragusa, E. Perret, A. Vena, C. Halopé, "High performance chipless RFID reader based on IR-UWB technology," *2015 9th European Conference on Antennas and Propagation (EuCAP)*, Lisbon, 2015, pp. 1-5.

2. **M. Garbati**, R. Siragusa, E. Perret, C. Halopé, "Low cost low sampling noise UWB Chipless RFID reader," 2015 *IEEE MTT-S International Microwave Symposium*, Phoenix, AZ, 2015, pp. 1-4.

3. **M. Garbati**, A. Ramos, R. Siragusa, E. Perret, C. Halopé, "Chipless RFID reading system independent of polarization," 2016 *IEEE MTT-S International Microwave Symposium (IMS)*, San Francisco, CA, 2016, pp. 1-3

National conferences with selection committee:

1. **M. Garbati**, R. Siragusa, E. Perret, A. Vena, C. Halopé, "Lecteur RFID Chipless large bande", *XIXèmes Journées Nationales Microondes*, 3-5 Juin 2015.

2. **M. Garbati**, A. Ramos, R. Siragusa, E. Perret, C. Halopé, " Système de lecture de tags RFID sans puces indépendant de la polarisation", *XXèmes Journées Nationales Microondes*, 16-19 Mai 2017.