Investigation of aging and cracking mechanisms in advanced ceramic materials for microelectronics

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Investigation of aging and cracking mechanisms in advanced ceramic materials for microelectronics

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Acronyms

AEC Automotive Electronic Council
BEoL Back End of Line
CMP Chemical-mechanical polishing
CPI Chip-Package Interactions
CSM Continuous Stiffness Measurement
CTE Coefficient of Thermal Expansion
FEoL Front End of Line
FIB Focused Ion Beam
HAST High Accelerated Steam Test
HTOL High Temperature Operating Life
HTSL High Temperature Storage Life
JEDEC Joint Electron Device Engineering Council
MEoL Middle End of Line
OSG Organo Silicate Glass
PECVD Plasma Enhanced Chemical Vapor Deposition
PMD Pre Metal Dielectric
PSG PhosphoSilicate Glass
RC Resistance-Capacitance
SEM Scanning Electron Microscopy
TC Temperature Cycling
TEM Transmission Electron Microscopy
THS Temperature-Humidity Storage
USG Undoped Silicate Glass

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General introduction

The increasing complexity of microelectronic devices illustrates the race to miniaturize the components and to optimize their performances, driving the microelectronic industry. Indeed, products have more and more functionalities thanks to always innovative processes and materials. In addition, the long-term reliability of electronic components has become a crucial commercial argument, especially for markets with a strong commitment to quality, such as automotive, medical or space.

Systematic product qualification is defined during its development to guaranty its reliability and ensures the minimum failure rate. In addition to the wide range of electrical failures, mechanical-induced failures are also sometimes observed. Indeed, with new integration schemes of package and extensive integration of new porous insulating materials with low mechanical properties, failure hazard increases dramatically.

At such scale (few hundreds of nanometers), the characterization of mechanical properties and the understanding of fracture mechanisms are a great challenge. Thin film effect, sample preparation, defect monitoring are just a few examples of the problems faced by the microelectronic industry in this field of research. This is even more complex when dealing with the mid and long-term reliability. In this context, this manuscript is set with the main objective of addressing these mechanical reliability issues focused on the chip. One can question if these issues come from a modification of the embedded materials due to aging effect and/or due to a time-dependent and/or cumulative process (fatigue mechanism, corrosion...).

These questions will guide our investigation throughout this manuscript. Before going deeper into the description of our objectives and strategy, a quick introduction to the very basic concepts of the microelectronics is given in the following part.

A packaged integrated circuit can be divided into two parts: the *Front End* and the *Back End*. The first is the active part, which is called the *chip* or the *die*. The latter is related to the package likely comprising the *molding compound* and the *printed-circuit board* (figure 1).

Chips are processed from wafers of semiconductor material, typically silicon, which presents electrical properties of either conductor or insulator material depending on the energy provided to the material. Nowadays, these single-crystal silicon wafers have usually a diameter of 200 or 300 mm. Then, the wafers are sawed into chips, assembled to the *printed-circuit board* and encapsulated to form a packaged integrated circuit.

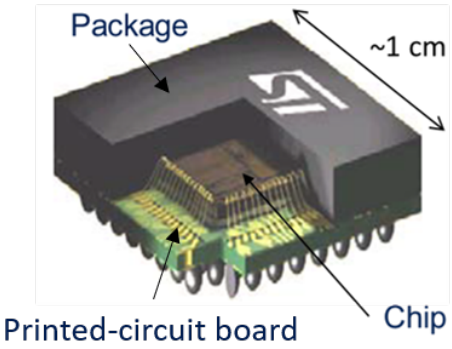

Figure 1: *Example of an integrated circuit in its package with partial opening of the molding compound revealing the chip, which is connected with gold wires to the printed-circuit board*

The *Front End* consists in a combination of three main parts:

- the *Front End of Line* (FEoL), housing the electrical active (transistors) or passive (resistors) components. A particular dimension of the transistor, the gate length, determines the technology node of the integrated circuit. Nowadays, commonly produced devices range from 130 nm downto 10 nm for the most advanced technologies.

- the *Middle End of Line* (MEoL), connecting the FEoL to the BEoL through tungsten contacts separated by the *pre-metal dielectric* (PMD)

- the *Back End of Line* (BEoL), where the active components are interconnected, through metal wires on several levels, according to the final function of the integrated circuit. The metal levels are referred as M_x for metal and V_x for via, where x stands for the interconnect layer number in ascending order from the FEoL to the BEoL. Depending on the device, this number may vary between 1 and 10.

A chip structure includes *insulating layers* (dielectric materials with a low dielectric constant to avoid parasitic RC[1] coupling between metal levels), *barriers* (such as silicon nitride and silicon carbo-nitride to prevent copper diffusion in the oxide layers), *metal levels* (copper is the material used for the most recent technologies because of its low electrical resistivity), two *passivation layers* (a PSG[2] layer to protect the BEoL structure from chemical contamination and a capping silicon nitride for preventing the BEoL structure from mechanical aggression) and *bonding sites* for the chip-package connections (aluminum contacts) (figure 2).

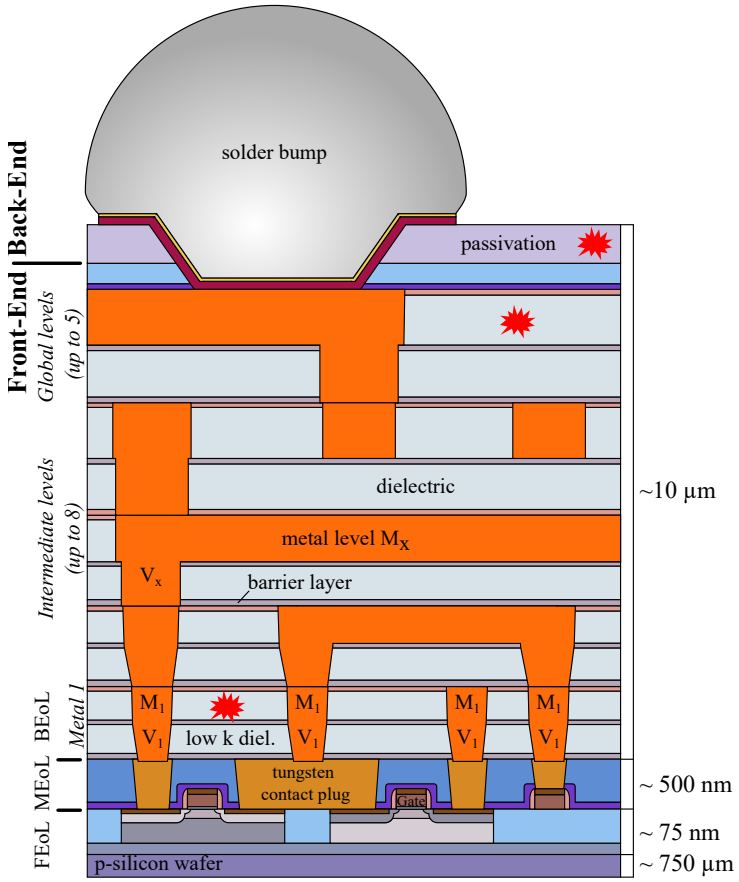

Figure 2: *Schematic illustration of a chip cross-section (the red marks stand for the localization of the dielectric layers studied in this manuscript)*[3]*. Note that the figure is not scaled to better show the thinnest layers.*

Material integration challenges in the BEoL The increase in traveling speed of a signal in a microelectronic circuit is proportional to the inverse of the circuit response time τ also called the RC delay ($\tau = RC$). Thus, τ is the product of the resistance R, which slows the flow of electrons in the metallic interconnect line and the capacitance C, which slows the current through charging delays.

[1] RC = resistance/capacitance

[2] PSG stands for PhosphoSilicate Glass.

[3] © Cepheiden / CC BY-SA 4.0 (via Wikimedia Commons), modified.

In order to improve the device performances, the need for new materials arises. On one hand, copper was introduced for the metal line manufacturing, in replacement of aluminum, to reduce the resistance. On the other hand, new insulating materials with low dielectric constant k were brought in to reduce the capacitance.

Metals From 2004, copper metal lines substitute aluminum to reduce the interconnection resistance. Indeed, its lower resistivity ($\rho = 1.67\ \mu\Omega.cm$ for the copper instead of $\rho = 2.65\ \mu\Omega.cm$ for the aluminum) and good resistance to electromigration make copper a good candidate for the interconnection processing. However, integrating copper requires a new fabrication process: the so-called double damascene process, illustrated in figure 3 in a very simplified way[4]: *(1) dielectric deposition:* the dielectric layer is deposited and will serve as a future insulator for the metal lines; *(2) photolithography:* the surface is coated with photo-resist and lithographically patterned; *(3) line etch:* the layer is etched to create the future metal lines; *(4) copper deposition:* the copper is now deposited and fills the previously etched lines; *(5) CMP:* a chemical-mechanical polishing is performed to flatten the surface for the next metal level processing; *(6) encapsulation:* a silicon nitride barrier is finally deposited.

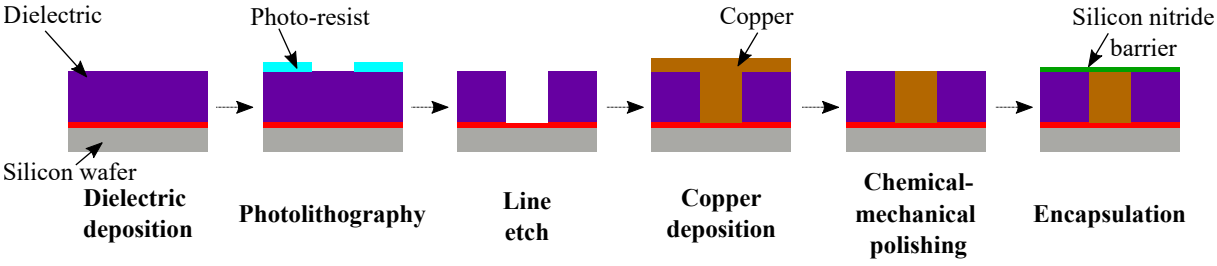

Figure 3: *Simplified schematic of the damascene architecture*

Insulating materials In order to decrease the propagation time of information in the interconnections, low permittivity dielectrics were developed to replace the standard silicon oxide (SiO_2). These low permittivity dielectric materials are commonly called the *low k* dielectrics and are deposited at the first metal levels (*i.e.* where the copper density is the highest). Among low permittivity films, we can cite hydrogen-doped silicon oxides, organic polymers, carbon-doped silicon oxides (*low k* SiOC:H) and porous and carbon-doped silicon oxides (*ultra-low k* SiOC:H).

These materials were developed for the improvement of their electrical properties (decreasing k value), usually at the expense of their mechanical properties. Indeed, these materials show mechanical properties (reduced modulus, hardness and fracture resistance) almost divided by 10 as compared to classical silicate glasses [10]. Thus, their integration to the BEoL and its integrity become critical.

[4]Many other barrier layers are deposited, for example to limit the copper diffusion, to stop the CMP process and so one. They are not detailed here, only a simplified illustration of the double-damascene is given. See [17] for further details.

Typical failure modes in the BEoL During the different process steps, product qualification and service life, a device can experience a variety of mechanical and thermal stresses. The potential failures observed in a BEoL can be at the dielectric layers as well as at the metal lines: among others, *stress voiding* and *hillocks* for the metal interconnections, or *cracking* and *delamination* for the dielectric layers.

Cracking and delamination of the dielectric films become an increasingly important issue when integrating *low k* dielectric materials to the BEoL stack. Even if they are more critical due to their poor mechanical properties, the *low k* films are not the only ones subjected to cracking as cracks were observed also in other dielectric layers. Figure 4 illustrates a crack present (a) in the SiN_xH_y passivation layer near the bump side and one that propagates (b) throughout the BEoL stack.

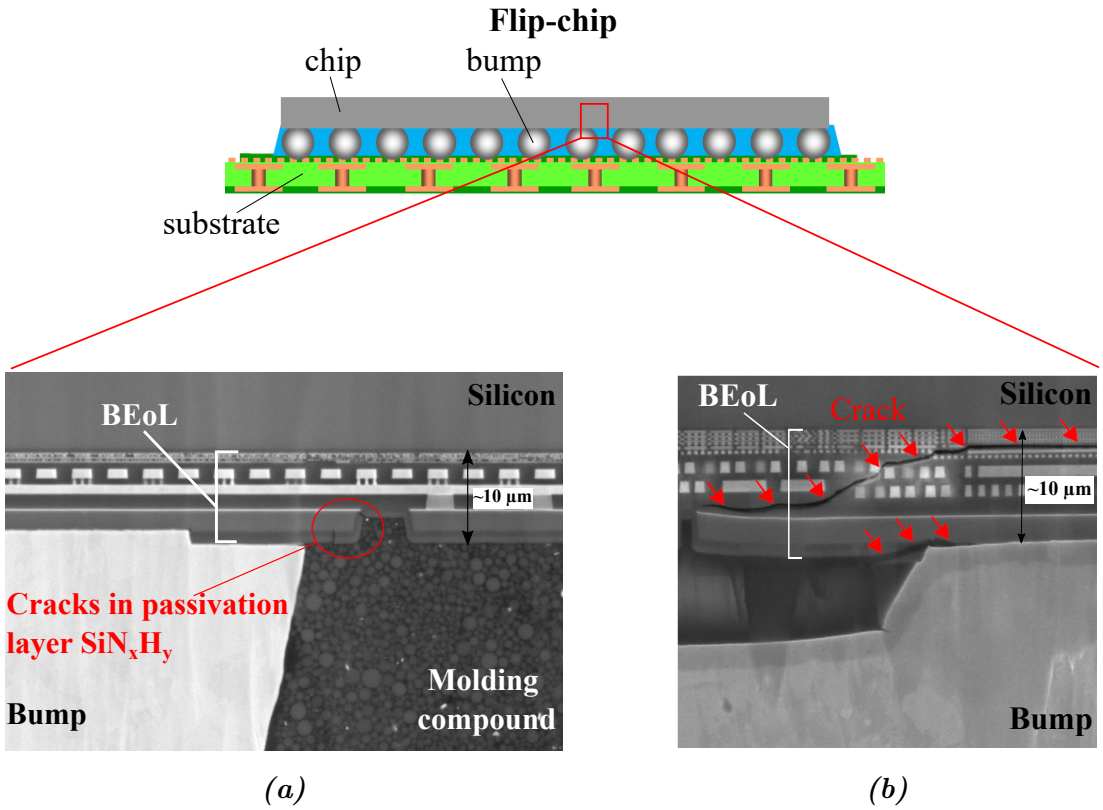

Figure 4: *SEM cross-sections of cracks: (a) at the SiN_xH_y passivation level and (b) in all the BEoL stack. Note that the FEoL component is not visible here due to the large scale.*

These failures can compromise the good functioning of the integrated circuit. Therefore, it is essential to identify their root-causes. The sources of stresses are diverse:

– at the chip level: the process flow, due to the different material deposition temperatures and their different Coefficients of Thermal Expansion (CTE), thermo-mechanical stresses arise in the structure. The material deposition parameters may also impact the intrinsic stresses. Both sources contribute to the residual stresses.

– at the package level: depending on the package assembly option, mechanical loading may be applied to the BEoL. Package assembly induces also different deposition temperatures and materials, which lead to similar thermo-mechanical stresses.

In this context, *Chip-Package Interactions* (CPI) are known for their criticality. They refer to the evidence of thermo-mechanical stresses within the chip, because of interactions with the package. Figure 5 illustrates how stresses can be transferred through bump connections towards the BEoL interconnections in case of a flip-chip assembly, embedded in many materials of different natures (metals versus ceramics), after thermal loading.

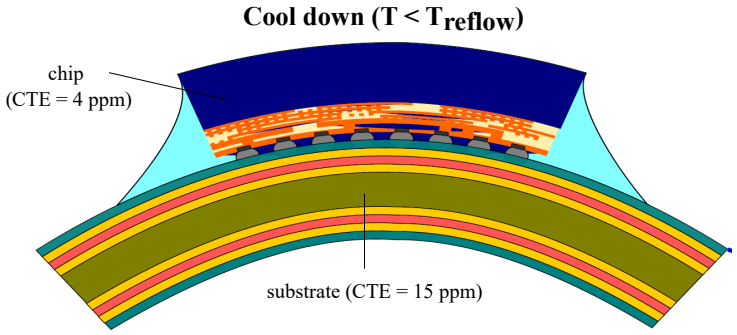

Figure 5: *Schematic illustration of the chip-package interaction caused by CTE mismatch between the chip and the substrate for a flip-chip assembly (not scaled) [125]*

Thesis motivations and strategy With the constant increasing integration density, new materials and architectures are continuously being developed to create innovative products. The mechanical reliability of these new components has become one of the key points to be mastered. Beyond the tests already in place, either on the assembly line or during product qualification, the question is raised of the mechanical behavior of the product throughout its operating life, and its related reliability.

In this work, a specific focus is done at the BEoL level[5] in order to reduce the failure hazard at these levels. Indeed, as introduced earlier, the porous *low k* dielectric materials, embedded in BEoL, are known to be critical. However, few is known about their mechanical behavior after aging and/or with regard to the environment. The main difficulties rely on the considered scales (typically < 0.5 μm) and their brittle behavior, causing many issues for implementing samples and *in situ* observations.

The approach adopted in this thesis is in line with the perspective of understanding the interactions between the environment (temperature and humidity) and the mechanical reliability of dielectric films. The strategy is twofold: first, evaluate the potential evolution

[5]This work is in collaboration with the Crolles site of STMicroelectronics, one of the world's leading industrial players in the field of microelectronics. This is a 200/300 mm Front-End manufacturing site, therefore, one where the main interests lie in the FEoL/BEoL layers.

of the mechanical properties of materials after environmental aging, second, investigate the contribution of the environment in the crack mechanisms. Such a dual approach should allow the investigation of potential root-causes of failures observed in the BEoL in long-term reliability.

Hence, the manuscript begins with **chapter I**, which shows how the microelectronic industry ensures their product reliability through accelerated aging tests and related standards. Then, the basics of fracture mechanics in brittle materials are reminded, and to study the influence of environment, the stress-corrosion cracking mechanism is introduced.

Chapter II introduces the panel of studied dielectric films. It covers the standard families of materials used in the most advanced technology nodes. Then, the chapter follows with the different characterization methods used in this thesis, and specifically developed for it.

In **chapter III**, we investigate the mechanical properties of the dielectric materials after temperature cycling and humid environment storage. The variations of the main mechanical parameters (reduced modulus, hardness and fracture resistance) are measured during the aging steps. Therefore, specific methods such as nanoindentation or wafer-curvature measurement are used to determine the local mechanical properties of the thin films and residual stress.

In **chapter IV**, the influence of the environment on the cracking mechanisms of the *ultra-low k* SiOC:H is more specifically studied. A dedicated characterization tool is thus designed. Specific sample preparation and experimental protocol are also developed to able an *in situ* small-scale cracking characterization. Besides, a finite element simulation is provided to bring added insights into the experimental results.

In the last **chapter V**, the experimental results found in the two previous experimental chapters are placed in an industrial context. They are discussed regarding our initial problematic on the product reliability in microelectronics. The amplitude of properties variation and crack mechanisms are compared to those encountered during standard qualification step. In that frame, finite element modeling is also used to feed the discussion.

Finally, the main achievements of this work are gathered, and we propose recommendations for future studies.

CHAPTER I

General considerations on reliability and on fracture of ceramics

Interconnections are structures comprising many different materials with complex geometries. Failures such as cohesive, interfacial or mixed (both cohesive and adhesive) cracks could happen during the assembly process as well as during the product service-life. To ensure product long-term reliability and validate product design, accelerated environmental aging tests are performed with varying conditions of temperature, humidity level and pressure. Any mechanical failure occurring during these tests needs to be analyzed, so to identify the origin of the failure and to propose solutions to prevent it.

The first part of this chapter is dedicated to the general description of a typical qualification flow. A particular attention is paid on two accelerated aging tests, which address the mechanical and environmental failure modes: the temperature cycling and the temperature-humidity storage.

Fracture mechanics is an excellent tool for describing and determining structure integrity. It will be used in this work to characterize the fracture properties of dielectric materials. The main notions of fracture mechanics in brittle bulk materials are first reminded. Then, the particularities linked to film-on-substrate systems are presented. Finally, as the environmental influence on the fracture properties of *ultra-low k* dielectric materials is one of the key problems of this PhD, stress-corrosion cracking is also introduced for ceramics.

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I.1 Reliability in microelectronics

The reliability determines the time period during which a product will maintain its initial function for which it was designed. To assess reliability, standardized accelerated tests are typically used to identify potential failure mechanisms in semiconductor devices and to estimate the rate of their occurrence.

The historical approach to investigate the relationship between a maximum failure rate during accelerated tests and a product failure rate during service is to choose an apparent thermal activation energy E_a for a given product. The activation energy is defined as the minimum amount of energy required to initiate a particular process. Its value indicates the relative tendency of a failure mechanism to be accelerated through thermal heating.

To ensure the device qualification, a set of aging tests, which are driven by standards, are performed depending on the product and its application [1]. In this manuscript, the automotive context is highlighted, where the reliability is the focus of much attention.

Today, the reliability assessment for key automotive products is mainly based on the following typical philosophy:

1. Determination of the failure mode (electrical, mechanical...)
2. Determination of the adequate acceleration model for the considered degradation process
3. Determination of the accelerated test duration according to the degree of robustness agreed with the involved customers (safety coefficient *versus* estimated end-of-life) to be in line with the service-life conditions of the products

Obviously, numerous tests are focused on electrical failure modes. These modes are out-of-scope of this PhD, which deals about mechanical reliability only, and thus are not described here.

The main tests with a mechanical scope are presented below:

– High Temperature Storage Life (HTSL) is a test used to determine how products wear can be accelerated by temperature (and current/voltage if High Temperature Operating Life (HTOL) test is performed). This test is performed at 125°C. Bond intermetallic material aging as well as die cracks are examples of addressed failure mechanisms with HTSL.

– Temperature Cycling (TC) is used to highlight the CTE mismatch between the materials, which compose the product. Indeed, TC is performed to estimate the ability of products to withstand thermally-induced mechanical stresses. The delta temperature depends on the final application. The automotive application targets for instance a temperature cycling from -55°C to 150°C. Metal shorts, passivation layer integrity, die cracks as well as solder bump detachment are some of addressed failure mechanisms susceptible to be initiated by TC.

– Temperature-Humidity Storage (THS) is performed to evaluate the moisture resistance of the products, especially of non-hermetic packages, in humid environment. Metal corrosion and hermeticity loss are some of addressed failure mechanisms with THS.

– Highly Accelerated Steam Test (HAST) is a test, more severe than THS, which combines temperature, humidity and pressure effects. The targeted failure mechanisms are the same than THS, but involved under stronger moisture conditions.

Below are detailed more specifically two accelerated aging tests used in this PhD, the TC and THS, as they are known to be critical for the mechanical and environmental failure modes.

I.1.1 Temperature cycling

Temperature cycling is a common accelerated stress test used for microelectronic products to reproduce the temperature variations during their normal use. Self-heating of products during on/off cycles or cyclic environmental changes can cause these thermal variations. In both cases, these repeated temperature variations induce thermal cyclic loads, which can lead to product failure.

To evaluate test duration, the Coffin-Manson acceleration model is used as a standard to calculate the acceleration factor A_f (equation (I.1)) corresponding to the ratio of the product life at accelerated test and usual operating conditions.

$$A_f = \left(\frac{\Delta T_t}{\Delta T_u} \right)^m \tag{I.1}$$

where ΔT_t and ΔT_u are respectively the temperature change during aging and product life and m is the Coffin-Manson exponent, its value depends on the targeted failure mechanism.

Knowing the acceleration factor, the test duration is calculated with:

$$n_t = \frac{n_u}{A_f} \tag{I.2}$$

where n_t and n_u are respectively the temperature cycle number in aging test and in use environments.

Standards provide a framework for calculating the accelerated test specifications. The agreement then assumed that microelectronic devices experience an average thermal cycle temperature change of 76°C and about 54750 on/off cycles over 15 years of normal use. As perform reliability tests over such a long period would be not relevant, accelerated temperature cycling from -55°C to 150°C is done. To calculate the acceleration factor, m is set at 4 corresponding to cracks in hard metal alloys which is the supposed failure mechanism [1]. With this value and using equations (I.1) and (I.2), the total number of temperature cycles to perform in the accelerated test environment is 1034. This number

of cycles is used in most of qualification procedures at STMicroelectronics in agreement with the AEC standard [1].

In practice, the temperature amplitude is obtained with two thermal chambers: one set at -55°C and the other at 150°C. An automatic elevator mechanism transfers the specimens from one chamber to the other to perform a cycle every 15 minutes.

I.1.2 Temperature-Humidity Storage

Similarly, temperature-humidity storage is used to simulate how products are affected by humidity (*i.e.* corrosion, sealing of barrier...). Indeed, increasing humidity level can induce product or material failure occurring in shorter times as compared to dry environments. Humid testing is usually performed at elevated temperature to speed up aging, as the acceleration factor depends on both humidity level and temperature.

For temperature-humidity storage, the acceleration factor is calculated with the Hallberg-Peck equation:

$$A_f = \left(\frac{RH_t}{RH_u}\right)^p \frac{E_a}{k_B}\left(\frac{1}{T_u} - \frac{1}{T_t}\right) \tag{I.3}$$

where $RH_{t,u}$ are the relative humidity levels, $T_{t,u}$ the average temperatures, E_a the activation energy for the considered failure mechanism and k_B the Boltzmann's constant. The subscripts u and t are the same as for temperature cycling: u for use environment and t for test environment.

In operating conditions, over 15 years of use, the average relative humidity level is assumed to be 74% RH and the average temperature is 32°C [1]. In accelerated test environment, the humidity level is set at 85% RH and the temperature at 85°C. Moreover, the supposed failure mechanism is the bond pad corrosion. For such failure mechanism, p is equal to 3 and E_a to 0.8 eV given with equation (I.3) an exposure time of 960 hours [1]. Such duration is accepted in most of qualification procedures at STMicroelectronics in agreement with the JEDEC and AEC standards.

After being aged, the products are electrically tested to assess their good functioning. In addition to the qualification tests, systematic failure analysis is also provided to determine the failure root-causes. Imaging (*e.g.* SEM, TEM, X-Ray) and deprocessing (*e.g.* chemical, FIB, mechanical) methods are used to identify the crack characteristics. However, in order to understand and forecast these failures, a theoretical background is also needed. The field of fracture mechanics is introduced in the next paragraph.

I.2 Fracture mechanics of ceramics

Fracture toughness of thin film is a topic of great interest in microelectronics, where film-on-substrate systems are usually subjected to thermo-mechanical stresses. The crack nucleation and propagation is thus an important issue. This section aims to provide to the reader a global overview of the fracture mechanics, as in this manuscript, the cracking of thin films is discussed.

Ceramics are typically brittle over a wide range of temperatures [52, 56, 117]. Thus, around ambient temperature, they fracture after exceeding their elastic strength without (or with negligible) plastic deformation. Usually, their behavior is often considered as linear elastic until failure.

I.2.1 Linear elastic fracture mechanics

This section presents basics of the linear elastic fracture theory, commonly used to describe crack propagation in brittle bulk materials. This theory is valid for elastic materials with a limited damaged/plastic zone at crack tip as compared to crack length and sample dimensions.

Three cracking modes exist and cover all the fracture cases observed (figure I.1). Mode I corresponds to the opening mode, *i.e.* the crack extension is perpendicular to the crack front. Mode II is the sliding mode corresponding to a crack extension in the crack front plan, in a perpendicular direction. Mode III is called the tearing mode and corresponds to a crack extension in the crack front plan and following the crack front direction.

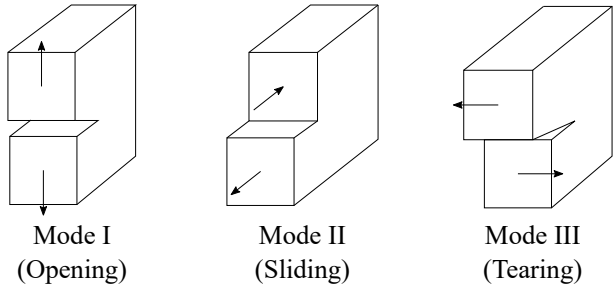

Figure I.1: *Crack extension modes according to the loading direction into mode I, mode II and mode III*

Note that the fracture mechanics theory assumes the presence of a pre-defect into the structure studied. The crack nucleation process is beyond the scope of this theory. The analysis focuses then on the propagation of this defect.

I.2.1.1 Global approach: concept of energy release rate G

The Griffith theory is commonly used to describe pre-cracked brittle solids [47]. This approach is purely energetic and is a balance between two states: the initial state of a pre-cracked loaded structure and the same structure after the growth of this crack. The

principle is that if the strain energy released for the crack extension is greater or equal to the surface energy required to the creation of the new fractured surfaces, then the crack propagation occurs. The energy criterion is obtained from the energy balance between the two states:

$$\delta U_{pot} + \delta U_{kin} + G_c \delta_s = 0 \tag{I.4}$$

where δU_{pot} is the potential energy, δU_{kin} is the kinetic energy variation, $G_c\delta_s$ is the energy required to initiate a crack of area δ_s. G_c is the critical energy release rate of the material.

Thus, a crack extension occurs if:

$$G = \frac{-\delta U_{pot}}{\delta S} \geq G_c \tag{I.5}$$

The left term of equation (I.5) corresponds to the energy provided for the crack propagation, *i.e.* the energy release rate G. The right term is the energy needed to produce new surfaces during the crack propagation and corresponds to the critical energy release rate G_c.

Thus, if $G < G_c$, else the crack does not propagate without increasing the applied load. In the other side, if $G \geq G_c$, else the crack propagates in an unstable manner.

We note that G_c corresponds to a dissipation of energy per surface unit localized in the damaged zone around the crack tip. It is an intrinsic material property independent of the structure geometry.

I.2.1.2 Local approach: concept of stress intensity factor $\mathbf{K}_I$

Irwin proposed the second commonly used approach to describe fracture in brittle material [63]. His work analyzed the stress field around the crack tip of a linear elastic material, considering a small crack in an infinite specimen (figure I.2).

The stress field ahead of the crack tip is described by the following function:

$$\sigma_{i,j}(r,\theta) = \frac{K_\alpha}{\sqrt{2\pi r}} f_{i,j}(\theta) \tag{I.6}$$

where θ is the angle from the x-direction, r is the distance from the crack tip, K_α is the stress intensity factor, α is the opening mode and $f_{i,j}$ are dimensionless functions of θ (the subscripts i and j correspond to the space components x,y and z).

Equation (I.7) expresses the stress intensity factor at the crack tip:

$$K_\alpha = \sigma_\infty \sqrt{\pi a} \tag{I.7}$$

where σ_∞ is the applied stress.

The criterion for unstable crack propagation is the critical stress intensity factor K_c referred as the fracture toughness of a material. K_c depends on the opening mode (I, II or III), so labeled K_{Ic}, K_{IIc} or K_{IIIc}. The stress intensity factor depends on the applied stress to the specimen and on the crack geometry.

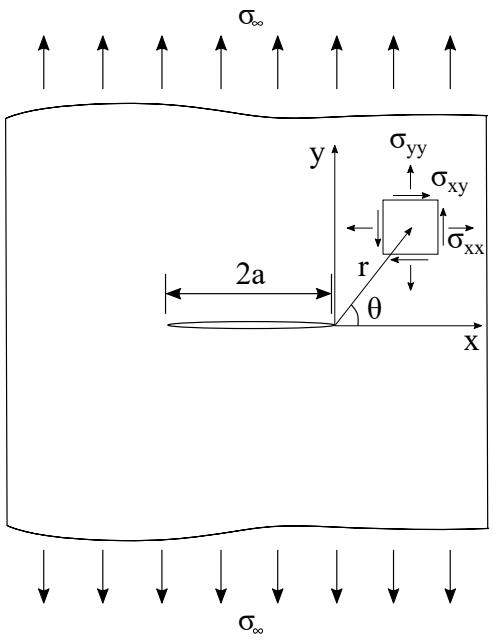

Figure I.2: *Crack specimen under mode I loading and stress fields in an arbitrary element ahead of a crack tip*

The loading parameters G and K can be converted into each other with[1]:

$$G = \frac{K_I^2}{E} \tag{I.8}$$

I.2.1.3 Critical flaw size

With the case described in figure I.2 (*i.e.* finite crack into an infinite specimen loaded in mode I), a critical flaw size is defined combining equations (I.7) and (I.8):

$$a_c = \frac{EG_c}{\pi\sigma_\infty^2} = \frac{1}{\pi}\left(\frac{K_{Ic}}{\sigma_\infty}\right)^2 \tag{I.9}$$

where a_c is the critical flaw size, E the specimen Young's modulus, σ_∞ the applied stress.

This means that if a defect created in the material is smaller than a_c, there is no crack propagation for an applied stress σ_∞. On the contrary, for defects longer than a_c, propagation is induced at σ_∞.

I.2.2 Crack nucleation

As seen before, the theory of linear fracture mechanics considers only the crack propagation from a pre-existing defect. However, sometimes, structures don't have pre-cracks and the nucleation of a new crack in a material starts from geometric and/or material singularities.

[1] In plane strain conditions, $G = \frac{K_I^2(1-\nu^2)}{E}$

We saw previously two approaches to describe crack propagation from pre-existing defects. First, if the applied stress σ is larger than the critical value σ_c, then a crack propagates for a given crack size. On the other side, a crack propagates if the energy release rate G is greater than the critical value G_c.

However, Leguillon showed that the two previous independent criteria are necessary but not sufficient conditions for the crack nucleation. He proposed a stress-energy coupled criterion [81], which states that both conditions (stress-based and energy-based) are necessary for crack nucleation. In other words, the stress level in the material has to be enough to initiate a crack and enough energy has to be accumulated to allow the crack opening.

Figure I.3 illustrates the coupled-criterion for crack initiation [28].

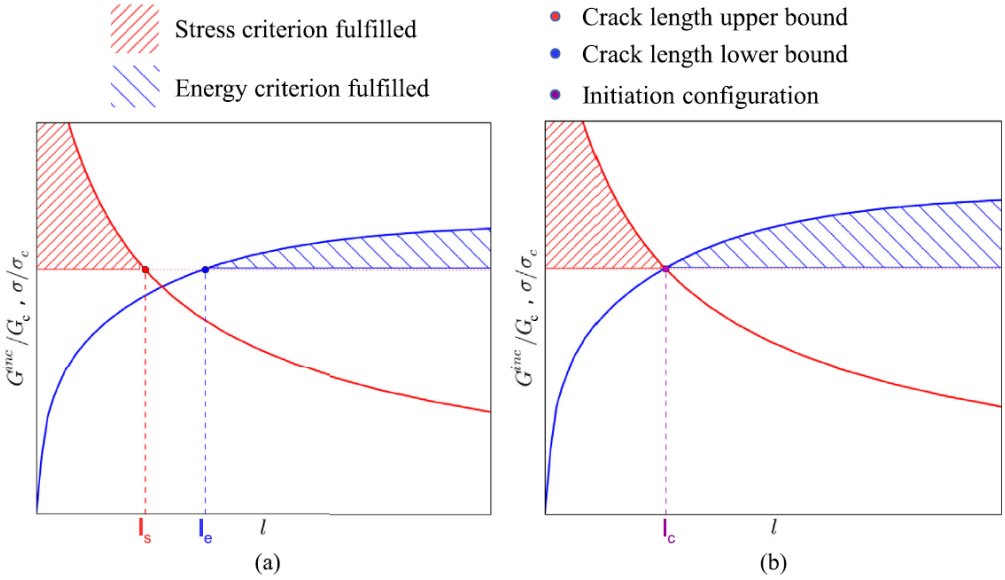

Figure I.3: *σ/σ_c and G_{inc}/G_c ratios as a function of the crack length l (a) before the initiation loading and (b) at the initiation loading (from [28]). G_{inc} is the incremental energy release rate corresponding to the energy release rate G when l tends to 0.*

First, for a decreasing stress, the distance l, on which the stress condition is valid, increases. Thus, the stress criterion determines an upper bond for all the admissible crack lengths at initiation l_s. Second, if the energy criterion is fulfilled for a crack length l_e at a given loading, then it is also fulfilled for all crack lengths greater than l_e. Thus the energy criterion determines a lower bond for all the admissible crack lengths. Figure I.3.b corresponds to the initiation loading where the lower and upper bonds coincide ($l_s = l_e = l_c$).

I.2.3 Case of thin films

Thin film deposition on substrates leads to residual stresses due to thermal property mismatch and material deposition parameters [27]. These residual stresses can cause the crack propagation through the film thickness or at the interface between the film and its substrate.

Fracture of thin films depends on the mechanical properties of the film, those of the substrate and those of the interface between the film and the substrate. Figure I.4 shows few examples of fracture cases that can occur in thin films.

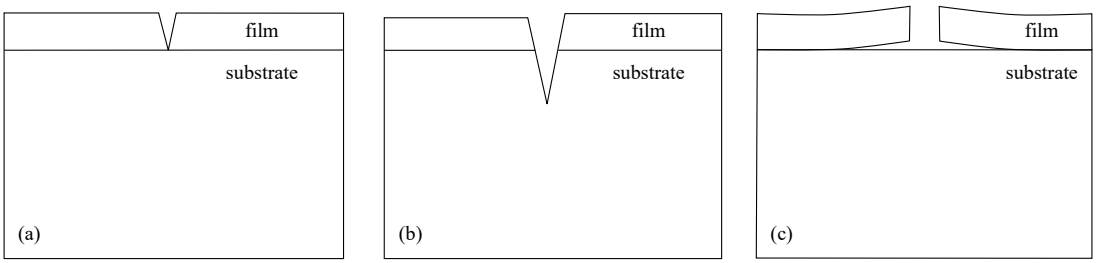

Figure I.4: *Different scenarios of cracks for thin films deposited on a substrate: (a) film channel cracking (b) film and substrate cracking (c) film channel cracking and interfacial cracking along the film/substrate interface*

The released energy around a crack that propagates cohesively through a film deposited on a substrate is given by:

$$G = \frac{Z\sigma_\infty^2 h_f}{E_f} \tag{I.10}$$

where Z is a dimensionless factor depending on the elastic mismatch between the film and the substrate and on the crack geometry, σ_∞ is the applied stress, h_f the film thickness and E_f the film modulus.

The crack propagates if the released energy is greater than the critical energy release rate G_c of the film. Thus, rewriting equation (I.10), a critical film thickness exists under which the film cannot be cracked. This critical thickness is defined by:

$$h_{fc} = \frac{G_c E_f}{Z\sigma_\infty^2} \tag{I.11}$$

For a given applied stress σ_∞, a crack does not propagate if the film has a thickness of less than h_{fc}. In contrast, a crack propagation is possible in a film of thickness larger than h_{fc}.

Experimental methods

For thin films, the measurement of the film fracture toughness faces difficulties because of the small scale (thickness typically below one micron). Dedicated equipment, sample

processing and surface roughness induce complex characterization at this scale. In addition, the films usually have different elastic, plastic and fracture properties as compared to their substrates. This increases the complexity of the fracture toughness determination of the film itself.

These difficulties lead to the development of many techniques owing their pro and cons to address the **interfacial fracture** (nanoindentation normal to the surface [139], nanoindentation on the cross-section [87], scratch techniques [76] and mechanical delamination tests [74]...) and **cohesive fracture** within the film (nanoindentation normal to the surface, cantilever beam deflection technique [92], freestanding film method [65, 100], micro-tensile fracture tests [68], and four-point bending [66]...) of a thin film. For the sake of clarity, all these different methods are not detailed here. However, some of them (nanoindentation, double-torsion and four-point bending), being used in this work, are described more precisely in the next chapter.

I.2.4 Environment-assisted slow crack growth

Dielectric thin films used in the interconnections are silicate-based ceramics. In this kind of materials, cracks can grow slowly at a stress intensity factor lower than the critical value K_{Ic}. This phenomenon is referred to as **slow crack growth**, as well as **stress-corrosion cracking**. It corresponds to the delayed fracture of a material from the application of stress due to the environment. It could be problematic, as components can fail long after they have been manufactured.

Stress-corrosion cracking corresponds to a combined effect of the stress field ahead of the crack and the environment surrounding the crack tip. This mechanism was observed in glasses since 1889 by Grenet [46]. Later, Orowan highlighted the role played by water on the crack propagation. His results showed that the critical fracture stress of glass can be three times lower in air than in vacuum. This suggests that corrosive molecules present in the environment are adsorbed at the crack tip, causing a decrease in surface energy of the glass, which becomes weaker [116] (figure I.5).

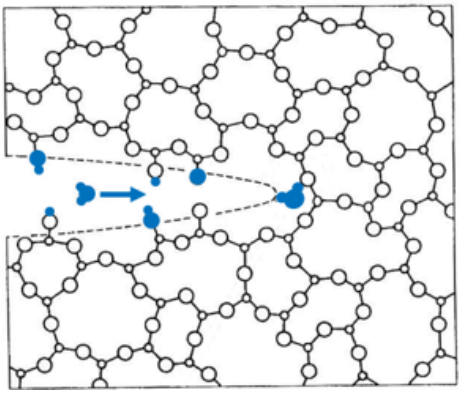

Figure I.5: *Schematic illustration of interaction between environment corrosive molecules and material molecules at the crack tip*

I.2.4.1 v-K_I curve

To characterize stress corrosion cracking in ceramics, the crack growth rate v (logarithm scale) is plotted as a function of stress intensity factor K_I. In figure I.6, a $v - K_I$ curve is schematized for the cracking of a ceramic in a humid environment.

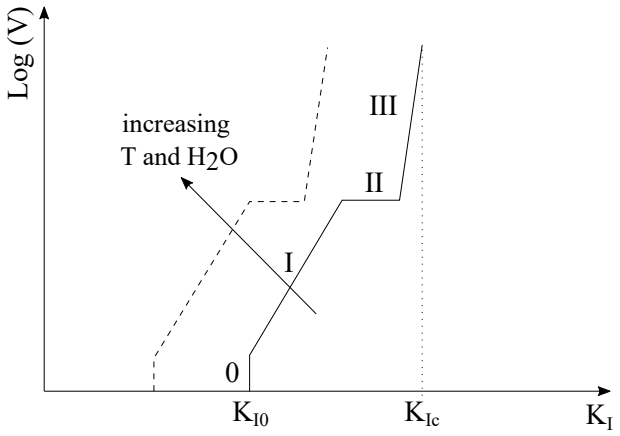

Figure I.6: *Schematic evolution of crack growth rate as a function of stress intensity factor*

Four zones can be distinguished:

- In **region 0**, cracks do not propagate. K_{I0} corresponds to the cracking threshold. Wan *et al.* showed first the existence of the stress intensity threshold K_{I0} studying slow crack growth in mica crystal samples [140].
- In **region I**, the crack growth rate is limited by the reaction rate between corrosive molecules present in the environment and atomic bonds at the crack tip [106]. The crack growth rate v increases along with the stress intensity factor K_I following the analytic formula [52]:

$$v = A \left(\frac{K_I}{K_{cst}} \right)^n exp \left(\frac{-Q_{app}}{RT} \right) \tag{I.12}$$

  where A is a constant, K_{cst} is a normalization constant, n is the sub-critical growth exponent and Q_{app} is the apparent activation energy of the sub-critical cracking kinetic.
- In **region II**, the crack growth rate is almost independent from the stress intensity factor K_I and is no longer limited by the reaction rate between the corrosive molecules and the material at the crack tip. The diffusion rate of the molecules to the crack tip drives the mechanism in region II [141].
- In **region III**, the crack growth rate becomes relatively independent from the environment. In contrast, the stress intensity factor drives the crack growth rate. In this region, the slope of the $v - K_I$ curve becomes steep, which is a sign of fast fracture. The crack propagation is linked to bond breaking, caused by the stress field at the crack tip with a limited influence of corrosion.

Characterization of K_{Ic}, usually obtained at high crack growth rate tests, is of importance. Figure I.6 suggests that the critical stress intensity factor can overestimate the actual crack resistance of the material, which may lead to a premature rupture of the ceramic component. In a practical case, the determination of K_{I0} is essential to set the lower limit of crack propagation. In addition, Wiederhorn showed that increasing the water content of the surrounding environment and the temperature decreases the threshold K_{I0}. The kinetic is also accelerated, meaning that for a similar stress intensity factor, the crack growth rate is increased (figure I.7) [141].

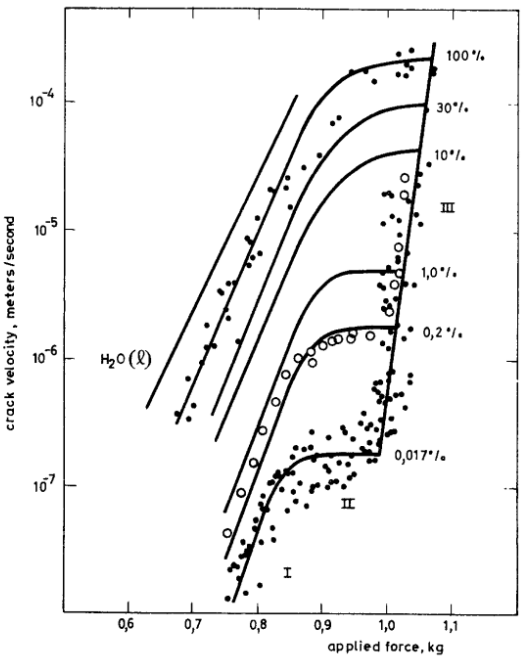

Figure I.7: *Dependence of crack velocity on applied force for different humidity levels for bulk soda-lime glass specimens (from [141])*

I.2.4.2 Slow crack growth in silicate glasses

Although slow crack growth in silicate glasses were observed for a long time [46], its characterization dates back to the 1960s [14]. Since then, slow crack growth in diverse ceramics have been widely studied [18, 78, 96, 112, 136, 142, 144].

The water content is not the only influential parameter, the temperature as well as other polar molecules can also modify the stress-corrosion cracking of ceramic materials [143]. In the following sections, only the influence of water will be discussed.

A physico-chemical interpretation of the slow crack growth in ceramics was proposed by Charles and Hillig [14]. They explained the phenomenon through a corrosion mechanism, which happens following three steps: (1) transport of the water molecule to the crack tip, (2) material dissolution and creation of the corrosion products, (3) transport of the corrosion products out of the crack tip. The crack propagation is controlled by the slower mechanism for the slower crack growth rates (*i.e.* material dissolution). However,

this model did not take account the possibility of a crack propagation in the absence of water molecules (*i.e.* in vacuum, where a dissolution mechanism cannot happen).

Later, Michalske and Freiman proposed a physico-chemical process to explain the slow crack growth in silicate glasses: the mechanism is attributed to ionic bond breaking [106]. In this case, the fracture is possible at a local critical stress reached in vacuum. In aqueous environments, the mechanical load needed to break these kind of bonds is decreased, as the mechanism is enhanced by the water molecules.

In more details, a Si-O-Si bond is dissociated to form two new silanol bonds (Si-O-H) according to the reaction: $Si - O - Si + H_2O \rightarrow 2SiOH$ [29, 33]. Locally, the Si-O-Si bond is broken, enhanced by both the mechanical loading and the chemical reaction. The principle, which makes consensus among ceramists today, is schematized in figure I.8.

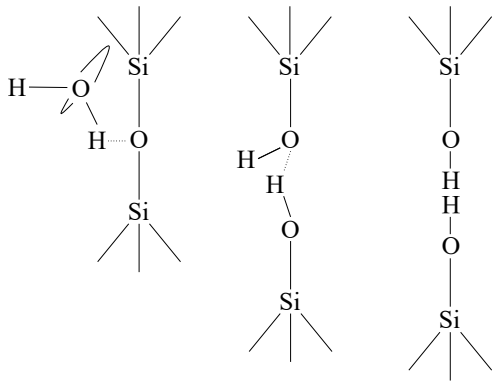

Figure I.8: *Schematic of the steps of the reaction between SiO_2-based ceramics and water happened at the crack tip*

Later, Zhu *et al.* demonstrated experimentally how water molecules reduce the breaking energy of chemical bonds of silicate glass, which agrees with the model proposed by Michalske and Freiman [106, 149].

In the field of microelectronic, SiO_2-based dielectric layers undergo stress-corrosion cracking, already studied by several authors.

McElhaney and Ma (and previously Ma in [95]) demonstrated the advantages of a sample comprising a metallic interlayer to generate cohesive channel cracks in a thin brittle SiO_2 film without breaking the substrate [101]. The authors observed evidence of sub-critical crack growth in a 4 µm-thick PECVD silicate glass deposited on Si wafer with a metallic interlayer loaded in four-point bending configuration. Figure I.9 shows the crack velocity as a function of strain energy release rate for their SiO_2 samples tested under ambient and dry environments.

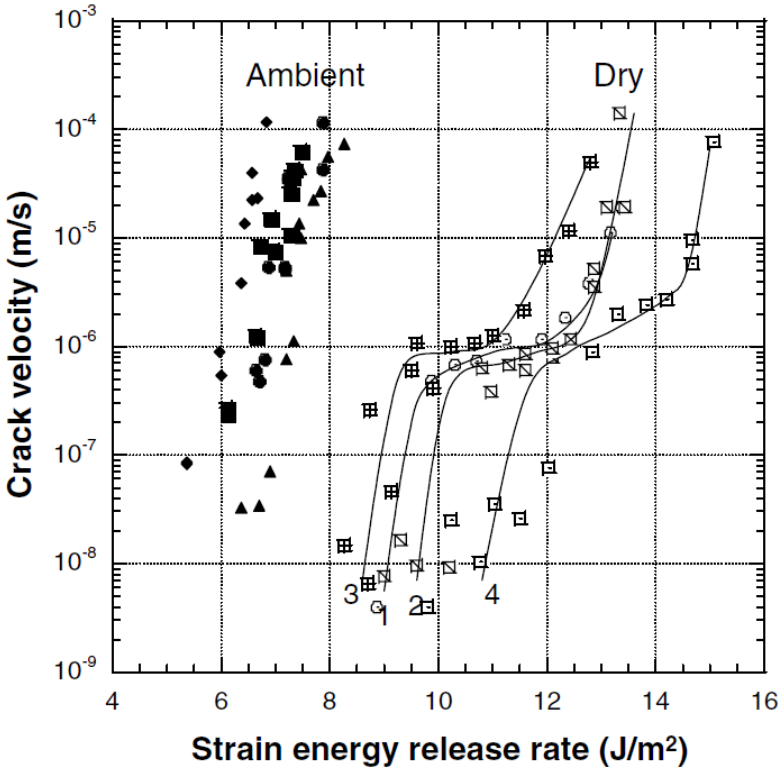

Figure I.9: *Crack velocity as a function of strain energy release rate under ambient (25˚C and 40 to 60% RH) and dry N2 environments. The 4 µm-thick SiO_2 (Undoped Silicate Glass) films deposited onto 2 µm of metal layer and a silicon substrate show increased crack resistance when tested in reduced humidity levels. The data from the dry environment also exhibit the characteristic S-shape of the three principal regions of moisture-assisted cracking (from [101]).*

In her PhD manuscript, Brillet tried similar experiments (*i.e.* channel cracking tests) on SiO_2 films of thicknesses ranging from 2 to 4 µm with a copper interlayer between the silicon substrate and the film. However, her experiments were unsuccessful as the silicon substrate fractured before any sign of crack propagation in the upper film. In contrast, Brillet showed that both more than 1 µm-thick PECVD and spin-on SiOC:H were subjected to sub-critical crack growth through four-point bending tests in ambient environment [10]. Figure I.10 presents the crack velocity measured in SiOC:H films with different thicknesses deposited on silicon substrates as a function of the stress intensity factor.

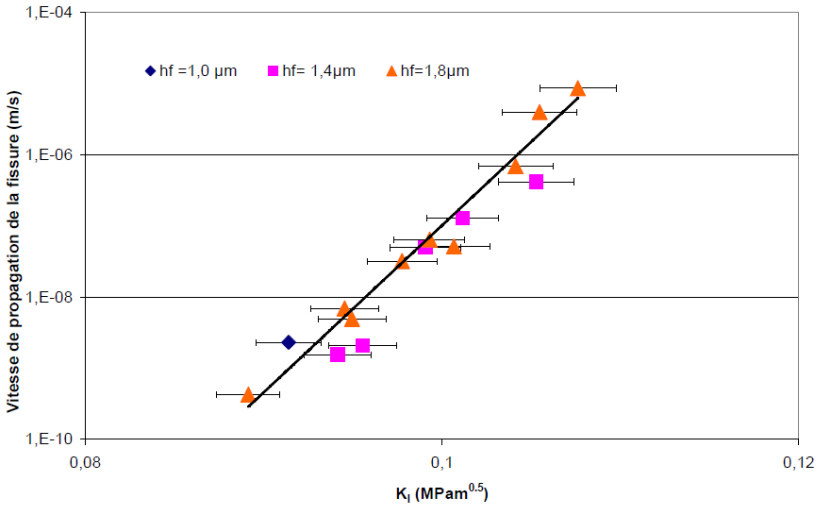

Figure I.10: *Crack velocity as a function of stress intensity factor for SiOC:H/Si configurations tested in ambient environment(from [10]). hf stands for film thickness.*

Concerning *low k* dielectrics, the possibility of generating arrays of stable channel cracks in OSG films of thickness of 2 µm deposited on silicon wafers was demonstrated [54] (see figure I.11), as well as of propagating an interfacial stable crack between an OSG layer and a SiN or SiCN barrier [23, 85, 90]. This demonstrates the sensitivity of this kind of materials and interfaces to sub-critical crack propagation.

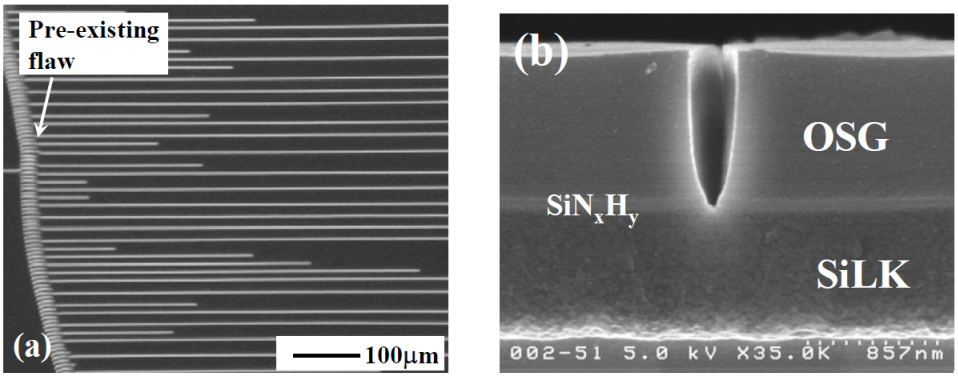

Figure I.11: *Channel cracks in OSG films (a) for a 2 µm-thick OSG deposited on a silicon substrate and (b) for a 1 µm-thick OSG deposited on a 60 nm-thick SiN_xH_y barrier and a 834 nm-thick low k SiOC:H film and then on a silicon substrate (from [54])*

I.2.4.3 Slow crack growth in silicon nitrides

So far, there are few studies on environmentally-assisted cracking in SiN_xH_x films. In this field, Birringer *et al.* showed the influence of the environment on interfacial crack growth between SiN_xH_y films and copper [8]. More recently, Vellinga *et al.* observed faster crack propagation in SiN_x barriers deposited on polyethylene nephthalate substrates in higher relative humidity environments using resistance measurements and *in situ* optical microscopy [138]. They concluded that SiN_x barriers undergo crack growth enhanced by

the environment. In order to determine the sub-critical growth exponent n, Guan *et al.* performed dynamic and static bending tests on a SiN_x layer deposited on polyethylene nephthalate substrate [48]. Their results suggested that SiN_x thin film is sensitive to environmentally-assisted sub-critical crack growth in contrast to bulk Si_3N_4, which is essentially insensitive to this mechanism. However, these studies do not directly measure the crack growth rates as a function of driving force of channel cracks propagating in the SiN_x layer. To discuss this problematic, Kim *et al.* conducted an *in situ* optical microscopy channel crack experiment in PECVD SiN_x layers deposited on PET substrates under different environmental conditions [71]. Their results showed that 250 nm-thick SiN_x can be subjected to environmentally-assisted crack growth with a channel crack growth rate about 10 times higher in humid air than under a dry nitrogen atmosphere. Moreover, a higher channel crack density was observed in humid air, meaning that crack propagation and nucleation compete and are both accelerated by water presence in the surrounding environment.

PECVD deposited SiN_x films differ from the bulk Si_3N_4 in their chemical structure and present oxygen (probably incorporated during the deposition process or by diffusion of oxygen and/or water vapor through the pores upon exposure to the atmosphere) and hydrogen mainly linked to Si and N atoms. Kim *et al.* explained the mechanism of sub-critical crack growth of SiN_x films similarly to what happen in glass samples [71]. In details, water molecules could enhance the rate of Si-N bond breaking, so the crack growth rate, at a crack tip. They proposed a stress-assisted hydrolysis reaction similar to the surface dissolution of Si_3N_4: $Si_3N_4 + 6H_2O \rightarrow 3SiO_2 + 4NH_3$. However, it is know that no crack growth in Si_3N_4 can occur due to its covalent bonding features. If crack propagation is observed in PECVD silicon nitride materials, it seems to be more due to the presence of some hydrogen and oxygen molecules incorporated during the deposition process.

I.3 Conclusion

In this chapter, typical reliability tests used in the microelectronic industry were presented to provide a general understanding of the industrial requirements and solutions provided to reduce the long-term risk of product failure. These tests will be used in chapter III to study the influence of the environment (*i.e.* temperature and humidity level) on the dielectric materials integrity. A particular attention will be paid to films in production at STMicroelectronics. Indeed, these films are generally thinner than model samples, and a dedicated characterization is needed.

Then, basic introduction to fracture mechanics was provided to introduce notions used latter in chapter IV to analyze fracture testing results. A particular attention was paid to the stress-corrosion cracking mechanism already observed in dielectric materials, similar to the ones studied in this manuscript. However, most of the studies are performed on

thick model layers (*i.e.* thicknesses of more than one micron) deposited on substrates, while submicronic films are targeted in this PhD.

The next chapter will be dedicated to the presentation of the materials investigated in this work and the methods used in that frame.

CHAPTER II

Materials and experimental methods

Failures may occur in the BEoL stack due to chip-package interactions, and are particularly known for their criticality. This results in the appearance of cracks in the dielectric materials constituting the stack. Beyond the tests already performed either on the assembly line or during product qualification, questions remain open regarding the mechanical behavior of the product, its long-term reliability and the effects of the environment. Especially, porous materials with low dielectric constant (*low k*), used on the most advanced technology nodes, are little described under this regime. Thus, in this manuscript, we propose to investigate more precisely four dielectric materials including two types of advanced *low k* and two others with a more classic nature. This would provide an overall picture of BEoL dielectric thin films used in microelectronic industry. The target is to evaluate the potential variations of mechanical properties due to environmental aging and the effect of the environment on the crack mechanisms.

This chapter first presents the studied dielectric materials. Then, experimental characterization methods involved in this PhD are described: nanoindentation for the determination of micro-mechanical parameters (reduced modulus, hardness, local fracture resistance) and wafer-curvature measurement for the evaluation of film residual stresses. Finally, complementary small-scale fracture tests are presented with different bending set-ups: double-torsion and four-point bending configurations.

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II.1 Investigated materials

As already shown in the general introduction, most of the mechanical failures occur in the brittle dielectric materials rather than in metals. Interconnected metal lines are insulated from one to another through a matrix of dielectric materials. The embedded materials, characterized by their dielectric constant (figure II.1), depend on the technology node and can be divided in two categories: the dense and the porous materials. The former is the oldest one and is based on silicon oxide with various doping components. The latter, with a much lower dielectric constant, is used in the most advanced nodes. Hence, two porous dielectric materials, a typical silicate glass used as reference, and a passivation silicon nitride known as a stable material in environment, were selected. All of them are massively used in the microelectronic industry and will provide an overview of the behavior of this category of materials.

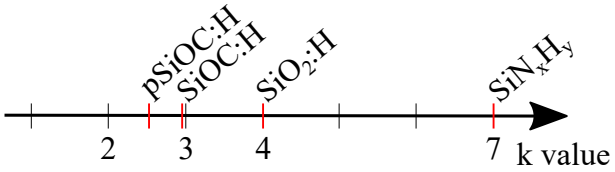


Figure II.1: *Dielectric constant values for the studied dielectric materials. The dielectric constant refers to the relative permittivity of the material, which is the ratio of the capacitance of a capacitor using that material as a dielectric, compared with a similar capacitor that has vacuum as its dielectric.*

In summary, four thin ceramic films, used as dielectric layers in the interconnect part of the chip, were studied:

- a silicon nitride
- a silicate glass
- a carbon-doped silicon oxide (referred to as *low-k*)
- a porous and carbon-doped silicon oxide (referred to as *ultra low-k*)

The silicon nitride is used as a passivation layer to protect the interconnections from any external aggression (environmental as well as mechanical). This layer is the last deposited at the very top of the BEoL stack. The silicon oxide is found at the global levels at the top of interconnections. The two last materials, found at the bottom of the stack (M1 to M5 - see figure 2), are the so-called *low-k* dielectrics, developed in the past decades to reduce the dielectric constant of the interconnection insulation.

All films correspond to industrial real layers deposited onto 300 mm diameter wafers under clean-room environmental conditions at STMicroelectronics Crolles site. They are deposited by Plasma-Enhanced Chemical Vapor (PECVD) deposition onto silicon substrates[1]. This technique consists in depositing a film on a substrate through surface

[1]Thanks to the Process Development Dielectric team at STMicroelectronic Crolles site

chemical reaction, by creating the elements to be deposited in a gaseous form, then causing the nucleation of the film on the surface of a substrate. The gas phase includes the precursors carrying the chemical elements to be deposited, additives, and a carrier gas. In order to reduce the deposition temperature, the CVD technique is enhanced by plasma, which provides energy to the chemical reaction (PECVD). This technique is used to deposit dielectric films at a temperature of 400°C and below.

II.1.1 Silicon wafer substrate

Substrates were (100) single-crystal silicon wafers with a diameter of 300 mm and a thickness of 775 µm (figure II.2). As silicon is anisotropic, its mechanical properties depend on the considered crystallographic plane. In this study, default mechanical properties of the substrate are taken from literature for single-crystal silicon considering the same crystallographic orientation [99].

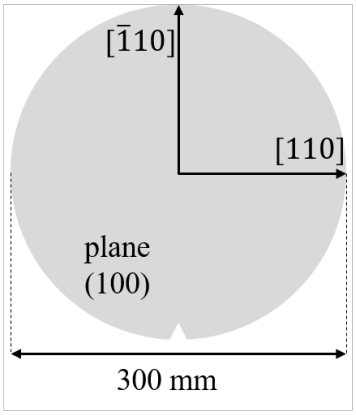


Figure II.2: *(100) silicon wafer*

II.1.2 Silicon nitride

Amorphous silicon nitride (SiN_xH_y) was deposited at a temperature of 380 °C from silane (SiH_4), ammonia (NH_3), and nitrogen (N_2) precursors. SiN_xH_y contains about 36 at.% of silicon, 48 at.% of nitrogen and 16 at.% of hydrogen bonded both to the Si and N atoms [17]. Its dielectric constant, noted k, is about 7 (figure II.1).

II.1.3 Silicate glass

Silicate glass (SiO_2:H), known as the standard Undoped Silicate Glass (USG), was deposited from silane (SiH_4) and nitrous oxide (N_2O) precursors at 400 °C. SiO_2:H contains a small amount of hydrogen (< 5 at.% [17]) forming Si-OH bonds. The SiO_2:H has a dielectric constant about 4.

II.1.4 Carbon-doped silicon oxide (low k)

Carbon-doped silicon oxide (SiOC:H) was deposited from trimethylsilane (labeled 3MS, $(CH_3)_3SiH$) and oxygen at 350 °C. SiOC:H has a dielectric constant about 3. This low value of k is obtained by incorporating methyl groups (replacing Si-O-Si bonds by Si-CH_3 bonds), which induces structural nanoporosity. SiOC:H has a porosity fraction about 6-8% and a density about 1.4 g/cm^3.

II.1.5 Porous and carbon-doped silicon oxide (ultra-low k)

Porous and carbon-doped silicon oxide (pSiOC:H) was obtained from co-deposition at 300 °C of a silica-based matrix together with an organic polymer playing the role of sacrificial porogen. Precursors were methyldiethoxysilane ($C_5H_{13}O_2Si$, named mDEOS) and bicycloheptadiene ($C_{14}H_{18}$, named BCHD). After deposition, the film was irradiated by UV-assisted thermal curing at 380 °C to remove the porogen and create the pores. Its dielectric constant is less than 3. pSiOC:H has a density about 1.2 g/cm^3.

Three sub-layers form the p-SiOC:H: the initiation, the core, and the capping (figure II.3). The initiation layer is a silicate glass deposited on the silicon substrate. The core is then deposited and has an open porosity with a fraction of 17%. On top of it, there is the capping with a porosity fraction of 13%. The decrease in porosity is obtained by decreasing the proportion of porogen amount over the silica-based matrix. The pores have an average size of 0.6 nm. For a 220 nm thick p-SiOC:H, the initiation, core and capping layers have thicknesses respectively of 50, 90 and 80 nm.

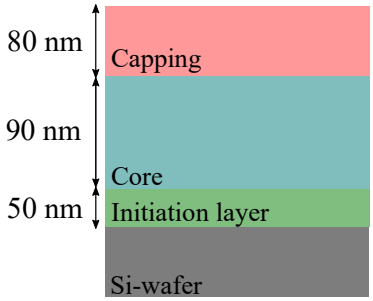


Figure II.3: *Schematic description of the 220 nm-thick ultra-low k porous and carbon-doped silicon oxide*

II.2 Characterization of mechanical properties

To evaluate the effect of environmental aging on dielectric materials, some mechanical key parameters need to be measured. Nanoindentation tests were performed to determine the reduced modulus, hardness and fracture resistance of the dielectric films at the local scale. In addition, the residual stresses of each film was also characterized thanks to the wafer-curvature measurement.

II.2.1 Nanoindentation

II.2.1.1 General presentation

Nanoindentation is a widely used method for testing small-scaled materials. Indeed, this method is particularly suitable for evaluating local mechanical properties, which is especially attractive for thin films deposited on a substrate. Nanoindentation originates from the classical hardness test, whose the principle is to measure the print size left by a geometry-known tip after penetration. Several types of hardness are defined depending on the tip geometry (figure II.4)[97].

The difference between hardness test and nanoindentation is related to the penetration depth. The latter is limited to two hundreds of nanometers for the nanoindentation, whereas the micro and macro-indentation hardness tests go deeper into the tested material. Another difference relies on the resulting hardness computation. The area used for the hardness calculation corresponds to the print size measured on the contact surface for the standard hardness testing, while for instrumented nanoindentation, the area is the projected tip area calculated through calibration tests (detailed later).

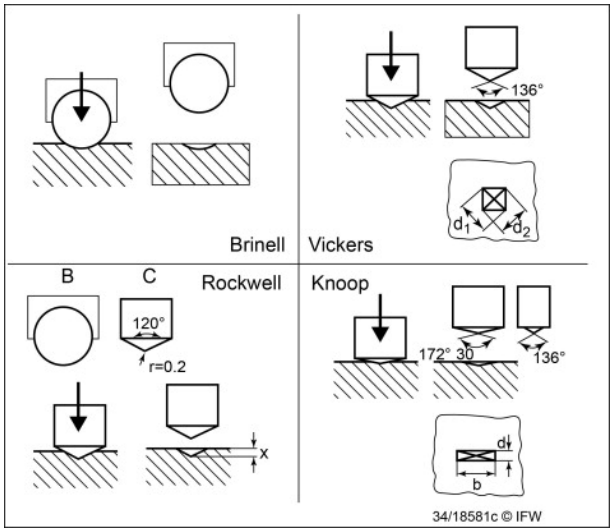


Figure II.4: *Classical hardness tests (from [97])*

Modifying tip geometry and applied load, nanoindentation can give access to several mechanical properties: elastic modulus and hardness [113], toughness [80], as well as adhesion strength of films [72, 98, 119, 147].

II.2.1.2 Indenter geometry

Several tip geometries can be used for nanoindentation testing. The choice of the geometry depends on the tested material and the targeted property. Two pyramidal indenters used to test our dielectric films are schematized in figure II.5: the Berkovich indenter for the measurement of reduced modulus and hardness on the one hand, and the cube-corner indenter to determine the fracture resistance on the other hand.

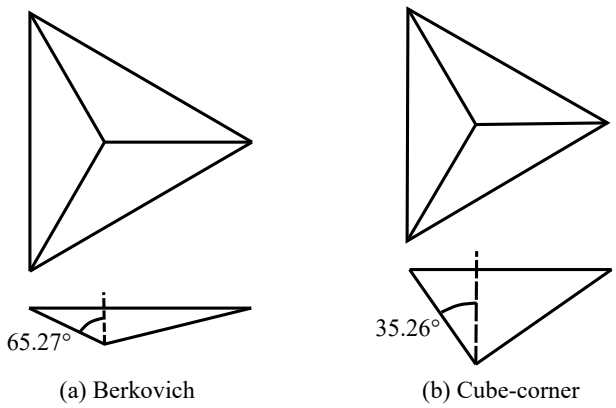


Figure II.5: *Indenter tip geometries: (a) Berkovich and (b) cube-corner*

Both are three-sided pyramids made of diamond, which elastic properties are taken into account through the reduced modulus. The two tips differ in their face angle: 65.27° for the Berkovich and 35.26° for the cube-corner (figure II.5).

The Berkovich is a common tip used to determine elastic modulus and hardness of materials [36], while the cube-corner is found to favor crack initiation at very small applied loads. Thus, this tip has gained popularity for the evaluation of an apparent fracture toughness in small volumes, for thin films in particular [62, 110]. Indeed, the sharp end of the cube-corner tip generates cracks more easily from the corners of indentation imprints; a higher strain is reached for an equivalent indentation depth. This approach is more detailed in §II.2.1.4.

II.2.1.3 Elastic modulus and hardness (Berkovich test)

Oliver-Pharr model

The calculation of reduced modulus and hardness parameters is based on a loading-unloading indentation cycle. During an instrumented indentation test, the applied load P and tip penetration h are recorded continuously (figure II.6).

The most common analysis of indentation tests adopts the Oliver-Pharr's procedure [113, 114]. Its popularity comes from its simple implementation, the precise analysis of the load-displacement curve and the precise definition of the contact between the indenter and the material. We present the contact geometry in figure II.7 using a conical indenter as a reference case, as commonly done in instrumented indentation.

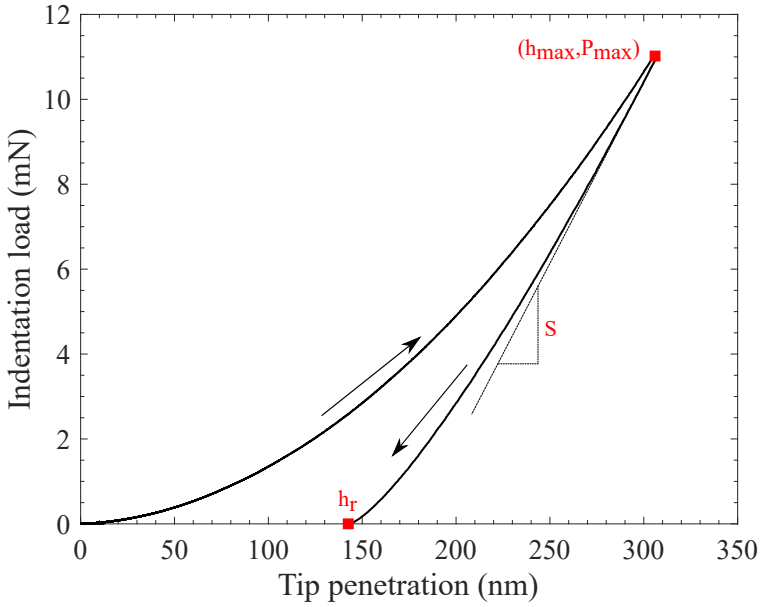


Figure II.6: *Typical nanoindentation load-displacement curve: loading/unloading cycle. P_{max} is the maximal applied load, h_{max} is the maximal penetration reached by the indenter, h_r is the depth of the residual print after unloading and S is the contact stiffness at the beginning of the unloading.*

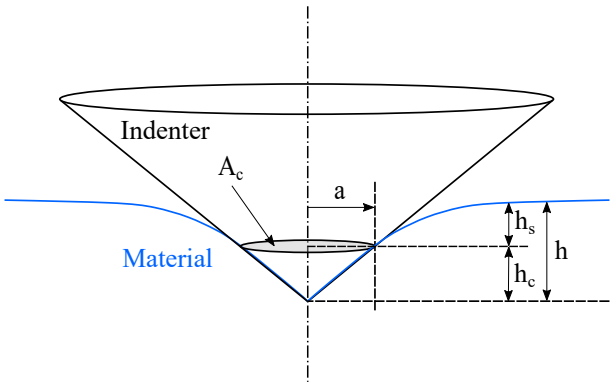


Figure II.7: *Schematic representation of the contact for a conical indenter as defined in [114]. h is the tip penetration, h_s is the vertical displacement of the surface, h_c is the true contact depth, A_c is the contact area calculated according to h_c and r_c is the contact radius.*

The true contact depth during indentation is calculated with:

$$h_c = h - h_s \tag{II.1}$$

Oliver and Pharr proposed the following expression for h_s, which is the elastic penetration (sinking-in), assuming the Berkovich tip as an equivalent conical indenter, while h is directly monitored during the test:

$$h_s = \epsilon \frac{P}{S} \tag{II.2}$$

where ϵ is a constant depending on the indenter geometry ($\epsilon = 0.72$ for a conical indenter).

The unloading curve is described by equation (II.3).

$$P = C(h - h_r)^m \tag{II.3}$$

where C and m are fitting coefficients and h_r is the final depth, as defined in figure II.6.

Thus, the contact stiffness S at the beginning of unloading is obtained by deriving equation (II.3) with respect to h:

$$S = \frac{dP}{dh} = mC(h_{max} - h_r)^{m-1} \tag{II.4}$$

The contact stiffness during nanoindentation is linked to the Young's modulus E of the sample by Oliver and Pharr from previous Sneddon's work [133]:

$$S = 2\ a\frac{E}{1-\nu^2} \tag{II.5}$$

where a is the contact radius and ν is the Poisson's ratio of the sample.

At $P = P_{max}$:

$$a = \frac{\sqrt{A_c}}{\pi} \tag{II.6}$$

where A_c is the projected contact area as defined in figure II.7.

Combining equations (II.5) and (II.6), the reduced modulus E_r is defined as:

$$E_r = \frac{S\sqrt{\pi}}{2\beta\sqrt{A_c}} \tag{II.7}$$

where β is a correction factor ($\beta = 1.034$ for a Berkovich tip). E_r is related to the Young's modulus and Poisson's ratio of the indenter and the tested material by equation (II.8) for an elastic, isotropic and homogeneous half-space.

$$\frac{1}{E_r} = \frac{1-\nu^2}{E} + \frac{1-\nu_i^2}{E_i} \tag{II.8}$$

where the subscript i stands for the indenter.

Finally, the hardness H is calculated with equation (II.9).

$$H = \frac{P_{max}}{A_c} \tag{II.9}$$

The following section is dedicated to the tip calibration in order to estimate A_c, needed for both hardness and elastic modulus calculation.

Berkovich tip calibration: determination of $\mathbf{A}_c$

To calculate the reduced modulus and hardness, the geometry of the tip has first to be determined. A proper calibration is therefore performed to compute its projected contact area. This calculation has been done carefully due to its strong impact on the result accuracy. Indeed, we do not have directly access to the projected contact area during

an indentation test, but only to the tip penetration into the material. Moreover, the materials can show sink-in or pile-up behaviors, which may modify the true contact area (figure II.8).

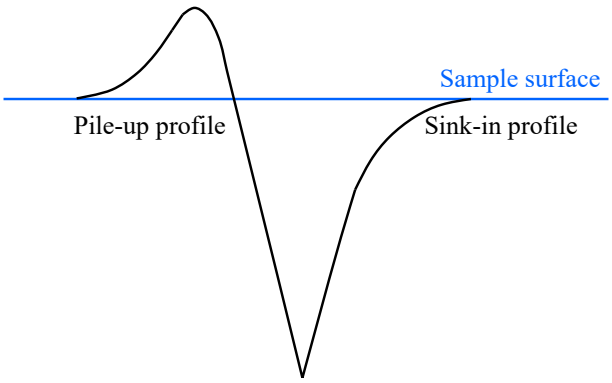


Figure II.8: *Pile-up and sink-in schematic profiles. The type of profile depends on the tested material.*

For all tip geometries, an area function $A_c = f(h_c)$ is defined. For a perfect Berkovich tip, the area function is given by:

$$A_c = 24.56h_c^2 \tag{II.10}$$

However, this equation cannot be used to describe the tip because of the non-perfect geometry of the tip. This defect comes from manufacturing (rounded tip with a radius of curvature ranging from 30 to 50 nm for a new tip) and is worsen with use, increasing the tip radius.

To illustrate the wear of a Berkovich tip, profiles of two indents, made with the same tip, were scanned by atomic force microscopy in figure II.9. Indentations were made in a gold layer (thickness of 500 nm), material chosen for its high ductility, deposited on a silicon wafer. The blue and the red profiles correspond respectively to a new tip and to the same tip after approximately 800 indentations into materials such as dielectric layers, silicon and fused silica. Piling up is noted as expected for a highly ductile material. Profiles highlight well the wear of the tip during indentation and thus, the need of systematic shape calibration.

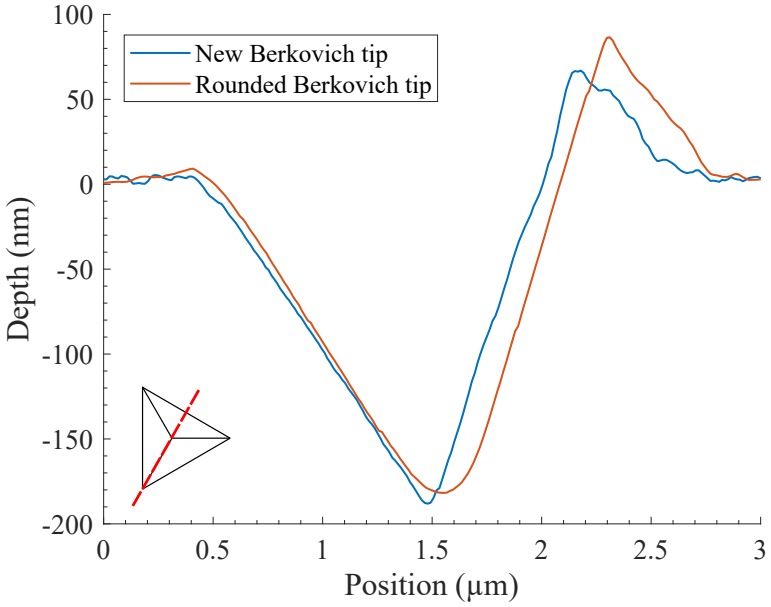


Figure II.9: *AFM profiles of Berkovich indents in Au. Two states are presented: new tip and tip after 800 indentations (dielectric materials, silicon and fused silica). The insert indicates the scan line with regard to the indent shape.*

The calibration was done by performing a series of indents in a material with well-known properties. Fused silica, which is homogeneous, isotropic, and smooth, is often used for calibration with a Young's modulus of 72 GPa and a hardness of 9.6 GPa. The calibration step consists in determining the contact area as a polynomial function of the contact depth to retrieve E_r and H values for the standard material (equation (II.11)) [114].

$$A_c = \sum_{n=0}^{n} C_n h_c^{1/2^{n-1}} \tag{II.11}$$

The coefficients C_n are fitted in order to get a constant modulus over the depth range. For a perfect Berkovich tip, the coefficient C_0 is equal to 24.56 and the others are equal to zero, which brings us back to equation (II.10).

It is worth mentioning that the thinner the measured layer is, the more accurate the calibration has to be, especially for the shallow depths. Indeed, indenting thin films requires a low penetration of the tip, and so the calibration is performed only for the very end of the tip.

Continuous Stiffness Measurement

For testing film-on-substrate systems, the Continuous Stiffness Measurement (CSM) technique is often used. It allows the continuous measurement of the contact stiffness S during the loading by superimposing a small-amplitude oscillation to the monotonous loading force signal for a given frequency (here, f = 200 Hz) [3, 114]. This protocol provides data,

such as reduced modulus and hardness, as a function of penetration depth in a single experiment. In addition, the contact point with the sample surface is clearly determined by the significant increase in the harmonic contact stiffness after contact. All the Berkovich indents were performed using the CSM mode.

Correction of substrate effect for thin film testing

Researchers have often applied Oliver-Pharr model to analyze different kinds of samples, including thin films on substrates. However, for thin film testing, the deconvolution of the film and substrate contributions to the indentation response need to be performed, and this may induce artifacts in the determination of the film properties. In a first approach, it is recommended that the maximum penetration depth should not exceed 10% of the film thickness to make the substrate effect negligible [35]. This accepted rule was first established for hardness, and then was widely extended to elastic modulus determination. However, this could lead to difficulties in measuring thin films commonly used in microelectronic industry generally with a thickness of less than one micron. Indeed, the sample surface roughness and the area function of the indenter tip at very small depths, which may not be reliable, contribute to increase the experimental errors. In addition, the 10% rule does not strictly apply for nanoindentation measurements of elastic modulus of thin films deposited on a substrate since there is always some elastic displacement of the substrate during an indentation test [35].

Reduced modulus Other models, empirical or analytical, were also developed in the literature to correct the substrate influence on the determination of the elastic modulus [26, 43, 86, 104]. In our study, the Hay-Crawford model was chosen to evaluate the dielectric film properties [53]. Indeed, it was found to be effective in correcting both soft films on hard substrates and hard films on soft substrates. This characteristic can be useful in microelectronic industry regarding the large panel of materials used. In the case of soft films on hard substrates (*i.e.* the majority of our dielectric films deposited on silicon wafers), the Hay-Crawford model was tested and found to accurately determine the film modulus [53, 137]. Moreover, Li *et al.* also validated by finite element simulation the Hay-Crawford model when the film is much more compliant than the substrate [88].

The Hay-Crawford model is a development of the Song-Pharr model (which in turn, draws from the Gao model) in the sense that it introduces the influence of the hard film by a modification of the film-on-substrate system representation [43, 127, 145]. In more details, the Hay-Crawford model corresponds to an arrangement of springs, presented in figure II.10, representing the film and the substrate with a fitting parameter F determined by finite element simulation.

According to this model, the film-on-substrate system shear modulus, μ, is defined as:

$$\frac{1}{\mu} = (1 - I_0)\frac{1}{\mu_s + F I_0 \mu_f} + I_0 \frac{1}{\mu_f} \tag{II.12}$$

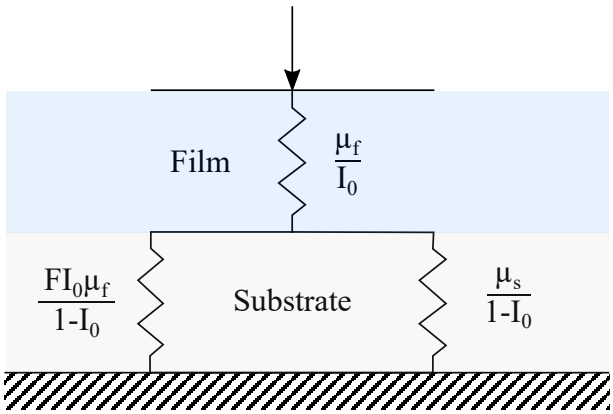


Figure II.10: *Schematic of the Hay and Crawford model [53]. The film acts in series and in parallel with the substrate to consider both film-substrate configurations (i.e. $E_f < E_s$ and $E_f > E_s$)*

In this expression, the constant F is equal to 0.0626 (valid until a penetration depth of 40% for a soft film on a hard substrate and of 25% for a hard film on a soft substrate), $\mu_{f,s}$ is the shear modulus of the film (subscript f) or the substrate (subscript s) and I_0, defined in equation II.13, is the Gao weight function with x being the ratio of the film thickness over the contact radius r_c [43].

$$I_0(x) = \frac{2}{\pi} arctan\left(\frac{1}{x}\right) + \frac{1}{2\pi(1-\nu_f)}\left[(1-2\nu_f)\frac{ln(1+x^2)}{x} - \frac{x}{1+x^2}\right] \tag{II.13}$$

Finally, the elastic modulus of the film can be deduced, knowing the film-on-substrate system shear modulus, μ, in equation (II.12), the substrate properties and the film Poisson's ratio, ν_f:

$$E_f = 2\mu_f(1+\nu_f) \tag{II.14}$$

As recommended by the authors, the model is limited to indentation depths lower than 20% of the film thickness, as we used the Oliver-Pharr model to determine the contact area.

Hardness The previously presented model is available for correcting the reduced modulus. For the hardness, the plastic deformation zone beneath the indenter is much smaller than the elastic deformation zone. Therefore, hardness is expected less sensitive to substrate influence than reduced modulus, so no specific correction is provided as it does not show much variation with penetration depth (as illustrated in the next chapter).

II.2.1.4 Fracture resistance (Cube-corner test)

Several methods exist to evaluate crack resistance of ceramic at small-scale like thin films involving flexural tests, micro-bending, dual beam cantilever, free-standing films, lab on chip methods or nanoindentation (see chapter I). The latter has gained increasing attention for the estimation of local fracture resistance properties of brittle materials and particularly for thin film study due to the easiness of sample preparation and testing. Indeed, during nanoindentation, cracks arise because of local stress build-up (usually during the unloading, but also possibly during the loading phase) and initiate from the indenter corners acting as stress concentrators. In addition, no specific sample preparation is required to generate cracks at the micro-scale which is not the case for the other mentioned methods. Moreover, with a cube-corner tip, smaller applied load is required to generate cracks as compared to the Berkovich tip (sharper tip shape). That's why cube-corner nanoindentation was the preferred option to monitor the cohesive fracture of our dielectric thin films. However, it could be noted that the analysis of indentation cracking tests is delicate as crack propagation is driven by local tensile stresses, whereas the test is in compression.

Here, we used a cube-corner tip mounted on the transducer to initiate cracks in our thin films. The tip was loaded to penetrate the material. Then the load was held at the maximal value for 5 seconds to compensate for any time effect. Finally, the tip was removed from the sample and the cracks can be imaged.

Indentation-induced cracks observed in ceramics

Sharp nanoindentation usually generates four major crack morphologies in a brittle material: radial, lateral, median and "half-penny" cracks as presented after indentation in figure II.11.

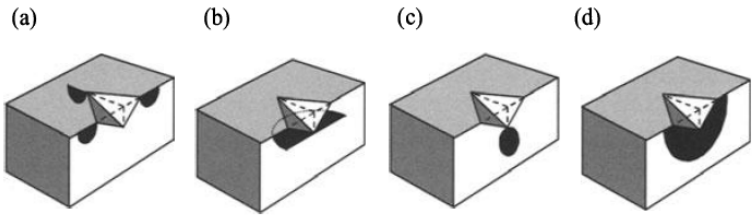


Figure II.11: *Illustration of different crack systems induced by nanoindentation: (a) radial cracks, (b) lateral cracks, (c) median cracks and (d) half-penny cracks (from [37])*

During loading, the indenter sets up a contact stress field. The widening of the plastic zone created beneath the indenter induces a tensile component, which provides the driving force for the fracture initiation. Then, removing the tip from the sample creates additional stresses due to the mismatch between the elastically deformed surrounding material and the plastic zone. So that, the cracks propagate from the bottom of the indent to the sample surface.

When the applied load is limited, short radial cracks are observed and are labeled *Palmqvist* cracks. This kind of cracks (*i.e.* radial or Palmqvist) emanates from the corner of the plastic contact impression and remains close to the surface (figure II.11 (a)). This leads to the formation of three semi-circularly shaped cracks with a maximum depth in the same order as the indentation depth for the cube-corner case.

Estimation of the apparent fracture resistance parameter K_{app}

Different equations exist to calculate the material apparent fracture toughness based on the size of the indent, the crack morphology and dimensions. We note that K_{app} corresponds to a crack stop criterion and not to a crack initiation criterion. Figure II.12 illustrates the geometrical parameters of interest.

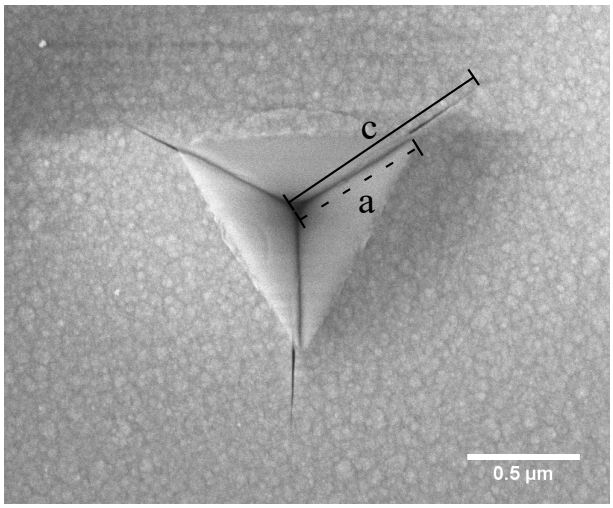


Figure II.12: *Crack parameters for a cube-corner indentation.* ***c*** *is the total crack length and* ***a*** *is the indent size. The illustration corresponds to a cube-corner indent into a 0.6 µm thick silicon nitride film.*

Lawn *et al.* had first developed a method to estimate the apparent fracture resistance from Palmqvist previous observations and using the Marsh's elastic-plastic model for Vickers indentations, then generalized to other axisymmetric indenters [80]. The authors proposed the following equation assuming the crack length c is greater or at least twice the indent print size a (*i.e.* the median-radial crack system is activated).

$$K_{app}^{Lawn} = \beta_1 \frac{P}{c^{3/2}} \left(\frac{E_f}{H_f}\right)^{1/2} \tag{II.15}$$

where β_1 is an empirical constant depending on the indenter geometry (β_1 is equal to 0.016 for a Vickers and Berkovich indentation and range from 0.032 to 0.040 for a cube-corner indentation [2, 51, 120, 121]).

Many fracture studies of glasses and ceramics used this method, which requires only the crack length and the maximal indentation load, knowing the elastic modulus and the hardness of the material [22, 25, 93, 131]. The last two properties are measured by Berkovich nanoindentation tests (§ II.2.1.3).

Later, Laugier *et al.* proposed a modified equation for the Palmqvist morphology (*i.e.* $c < 2a$)(equation (II.16)) [77].

$$K_{app}^{Laugier} = \beta_2 \left(\frac{a}{l}\right)^{1/2} \frac{P}{c^{3/2}} \left(\frac{E_f}{H_f}\right)^{2/3} \tag{II.16}$$

where β_2 is equal to 0.015 and $l = c - a$.

Despite the generalized use of nanoindentation for testing the fracture toughness of thin films on substrates, the use of nanoindentation testing for such purpose was also severely criticized by some authors [109, 124]. Indeed, the fracture toughness is a critical stress intensity factor for fast crack propagation and standard fracture tests consider only one pre-crack that propagates in an accelerating catastrophic manner through the entire sample. In contrast, nanoindentation fracture test measures an arrest criterion of a three-dimensional crack network emanating in a complex residual stress field and many equations that need to be calibrated are used for the fracture resistance parameter determination [55]. Thus, we must keep in mind that the parameter measured by nanoindentation is not a critical stress intensity factor in its proper definition.

Thin film configuration

Both models, used to calculate the apparent fracture resistance by cube-corner nanoindentation and presented above, were developed for bulk materials:

- the material is considered as isotropic
- the applied load has to be high enough to generate well-developed cracks
- the tested surface is supposed unstressed

In case of thin films on substrates, at least two obvious consequences of this material arrangement play a role on indentation fracture: the substrate constrains the development of the indentation cracks and the film is submitted to a preexisting stress.

Crack containment The first requirement in order to characterize thin film fracture properties is to contain the crack into the film to avoid substrate cracking or delamination at the film-substrate interface. Figure II.13 depicts the two cases: a cube-corner indent print *(a)* without and *(b)* with delamination.

Brillet proposes two recommendations to prevent any delamination [11]. First, in order to confine the plastic zone within the film thickness t_f, indentation depth has to be at least smaller than the film thickness. This is illustrated by equation (II.17) with the contact area between the cube-corner indenter and the sample surface expressed as $2.6h_c^2$, assuming similar Berkovich and cube-corner hardness. Second, the author recommends having a crack length at least smaller than 1.8 times the film thickness (limiting the crack depth to $0.9t_f$ and assuming the crack as semi-circular with a crack length equal to 2 times the crack depth).

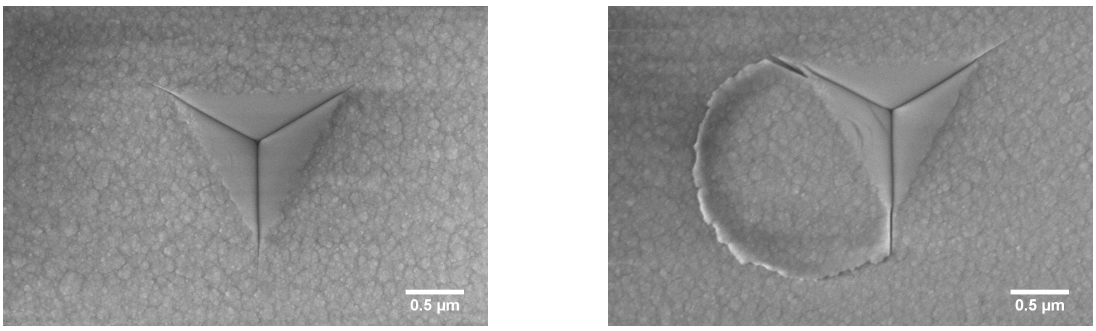


Figure II.13: *Cube-corner indentations for a 0.6 µm thick SiO_2 deposited on a silicon substrate: case (a) is the indent without delamination and case (b) shows a large chip corresponding to delamination between the film and the substrate.*

$$H_f \geq \frac{P_{max}}{2.6t_f^2} \tag{II.17}$$

When a crack is confined to a film, two limit cases can be considered: the thick film which behaves similarly to a bulk layer, and the thin film [69]. Both are illustrated in figure II.14. In insert (a), the radial crack system is observed while for (b), the crack develops from a radial shape to a channel crack constrained by the substrate.

In our study, the indentation load is set sufficiently low to ensure a radial crack mode II.14a. Thus, the film apparent fracture resistance is calculated with equations (II.15) and (II.16) depending on the crack morphology. The model used to calculate the fracture parameter for a channel cracking mode is described elsewhere in the literature and will not be detailed in this manuscript [69].

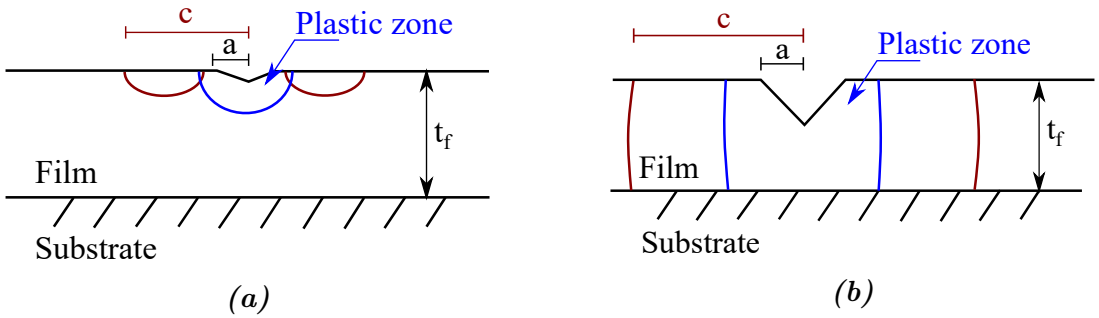


Figure II.14: *Schematic cross-section of an indent generating cracks: (a) partial penetration radial fracture emanating from indent and (b) indent-induced and substrate-constrained channel cracking (adapted from [69])*

Film residual stresses To consider the preexisting stress contribution to the stress intensity at the crack tip, Lawn proposed a formulation of the residual stress intensity factor for the median-radial crack system [79].

$$K_{res}^{Lawn} = \psi \sigma_{res} c^{1/2} \tag{II.18}$$

where ψ is a parameter dependent on the crack shape equal to 1.21 for the radial morphology and σ_{res} is the residual film stress.

With the same purpose, Brillet developed the equation (II.19) considering the shape of the crack as semi-circular, and so more suitable for Palmqvist crack shape.

$$K_{res}^{Brillet} = \sigma_{res}\sqrt{\frac{\pi}{2.04}t_f}\left(\frac{l}{t_f}\right)^{\frac{1}{2}}\left(-\frac{l}{t_f}\right)^{\frac{1}{2}-s}\left(+\frac{\lambda l}{t_f}\right) \tag{II.19}$$

In equation (II.19), t_f if the film thickness, l is the crack length, λ is a fitting parameter and s is the stress singularity exponent [6, 11]. Both parameters depend on the materials of the film and the substrate. For a SiO_2-on-Si system, λ is equal to 0.04 and s to 0.40. For a PECVD SiOC:H-on-Si system, λ is equal to 0.08 and s to 0.30 [11].

The two stress intensity terms (residual stress and indentation stress contribution) are finally summed using the principle of superimposition to estimate the fracture resistance parameter of the film determined by nanoindentation K_{NI}.

$$K_{NI} = K_{app} + K_{res} \tag{II.20}$$

II.2.1.5 Nanoindentation apparatus: Bruker-Hysitron TI 980 TriboIndenter

The TriboIndenter TI980 from Bruker is used to carried out the indentation tests in ambient laboratory environment (21°C and 40% of relative humidity). Specific developments are dedicated to more extreme conditions (*i.e.* at high temperature), but these are out of our automotive realistic conditions and *ex situ* measurements after aging are preferred [20]. The nanoindenter is composed of:

- a stage which can carry 300 mm wafers. The stage allows the (x,y) displacement of the sample.
- an optical camera system mounting with a 20x objective lens. Magnified images from 20x to 220x of the sample can be done for focus and positioning.
- standard and high-load transducers. The standard transducer has a load range from 100 nN to 10 mN. Due to its very low load capacity, the standard transducer is used for testing our thin films. The high load transducer has a higher load limit and tests can be performed up to 10 N. It is usually implemented when the standard one is limited in load, particularly for crack initiation in stiff materials. The tips are mounted on the transducer via a piezoelectric scanner which generates the vertical displacement.

The TI 980 TriboIndenter can be used in both quasi-static indentation and continuous stiffness mode. The tests are always carried out under a load-control mode.

Protocol

To measure the reduced modulus and the hardness of our samples, the following protocol is used:

- the contact area and the machine compliance are calibrated from CSM indentations into a reference fused silica
- a matrix of 49 CSM indents is performed with the Berkovich indenter into the tested material
- the reduced modulus and hardness are plotted as a function of indentation depth normalized by film thickness
- the Hay-Crawford correction is applied to the measured reduced modulus to account for the substrate effect
- the hardness value is directly computed from the measured data as the substrate influence is expected to be much less marked than for the elastic modulus

II.2.1.6 Complementary chemical analysis

Micro-mechanical modifications in thin film properties can be due to chemical changes during aging. That's why, the mechanical parameters determined by nanoindentation are used in conjunction with Fourier Transform Infrared Spectroscopy analysis (FTIR).

FTIR (QS3300 from Nanometrics) is used in normal incidence transmittance mode for the film spectra acquisitions to analyze any structural changes with aging. Spectra are recorded in the range of 400-4000 cm^{-1} at 6 cm^{-1} spectral resolution. Each spectrum is converted in absorbance baseline, then the baseline is corrected. Finally, the spectrum is normalized with respect to the layer thickness.

II.2.2 Wafer-curvature measurement

Thin films can develop large residual stresses during and after their deposition. A large stress can induce physical or electrical (piezoresistive effect) failures. However, it may also induce a curvature of the wafer (especially with 300 mm size) leading to handling issues during the process flow. This property is thus one of the mechanical key parameters of thin films. It is characterized indirectly by wafer-curvature measurements.

II.2.2.1 Origin of stresses in a thin film deposited on a substrate

Stress occurring during film deposition is often referred to as intrinsic stress [27].

Intrinsic stresses appear during the deposition process and can be distinguished from the thermal stress as they are already present at the deposition temperature [27, 134]. They are attributed to film properties evolution during the deposition process and depends

on the deposition method and conditions. For example, in the case of chemical vapor deposited films, intrinsic stresses appear if the precursors reaction is incomplete. The mechanisms underlying the intrinsic stresses in a film depends on the material as well as on the deposition conditions as the temperature, rate or pressure.

Thermal stresses arise when the film deposited on the substrate is subjected to thermal variations and because of the CTE mismatch between the film and the substrate. As the deposition temperature usually differs from the ambient temperature, the film is stressed at ambient environment. The thermal stresses are evaluated from equation (II.21) assuming constant thermo-mechanical properties over the range of temperature considered.

$$\sigma_f = \frac{E_f}{1-\nu_f}(\alpha_s - \alpha_f)(T - T_0) \tag{II.21}$$

where α stands for the CTE, T the current temperature and T_0 the film deposition temperature. The subscripts s and f are respectively given for the substrate and the film properties.

The residual stresses are then the sum of the intrinsic stresses and the thermal stresses.

Figure II.15 illustrates the apparition of stresses into the film and the curvature of the wafer. The convention of negative values for compressive stresses is adopted.

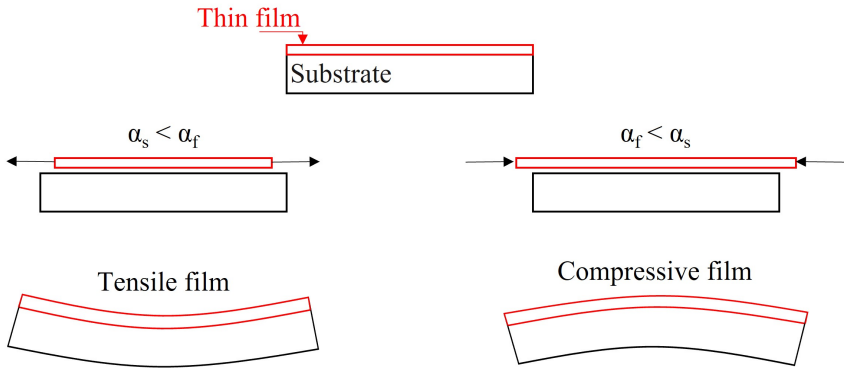


Figure II.15: *Thermal stresses into films deposited in substrates for a cooling*

II.2.2.2 Film residual stresses determination

Film stresses are calculated from the wafer deformation which is characterized by curvature measurement. The bow of the wafer is measured by chromatic confocal microscopy with a FRT MICROPROF and calculated with equation (II.22). The tests were performed at CEA-LETI.

$$B = \frac{z_{FS} - z_{RS}}{2} \tag{II.22}$$

where B is the bow of the wafer, z_{FS} is the distance between the confocal sensor and the wafer surface for the front side, and z_{RS} is the same distance measured when the wafer is upside down (figure II.16).

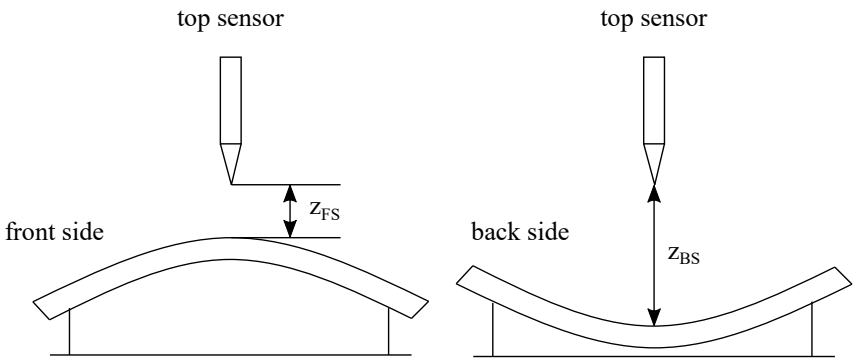


Figure II.16: *FRT MICROPROF bow measurement principle*

During the measurement, the wafer is placed on three supports and so, it is curved due to its own weight. This effect is compensated by measuring both the front and reverse sides.

From the bow measurement and geometrical considerations, the radius of curvature R is calculated with equation (II.23).

$$R = -\left(\frac{D^2}{8B} + \frac{B}{2}\right) \tag{II.23}$$

where D is the wafer diameter.

Stoney model

The model proposed by Stoney is widely used to calculate the stresses into thin films deposited on substrates [135]. Several hypotheses are associated to this model:

- the film thickness is much smaller than the substrate thickness
- the layer is homogeneously deposited onto the substrate
- the materials are assumed to be elastic and isotropic
- the deformation of the wafer is spherical

The residual stress of the film is calculated with the equation (II.24).

$$\sigma_f^{res} = \frac{E_s}{1-\nu_s}\frac{t_s^2}{6t_f}\left(\frac{1}{R_{post}} - \frac{1}{R_{pre}}\right) \tag{II.24}$$

where R_{pre} and R_{post} are respectively the curvature radii measured before and after film deposition, $t_{f,s}$ the film and substrate thicknesses, E_s the substrate elastic modulus and ν_s the substrate Poisson's ratio.

This method is widely used in microelectronic industry as the film stress can be evaluated without knowing the film mechanical properties.

II.3 Investigation of fracture mechanisms

As already mentioned, one of the most common failure related to chip-package interactions is a crack path growing through the *low-k* films at the first metal levels. Indeed, their integration is a major challenge for the industry which has to find the proper balance between their poor mechanical properties and the advanced package requirements. A good understanding of the fracture mechanisms of these *low-k* materials and of the effects of the environment is thus mandatory to optimize their integration. This is why we proposed to study more specifically the fracture mechanisms and environmental influence of the porous *ultra-low k* film.

Several requirements need to be fulfill by both experimental methods: **(1) repeatability:** experiments must be repeatable **(2) monitoring:** crack initiation and propagation must be measurable **(3) control:** crack propagation must be manageable easily to choose the regime of failure **(4) environmental effects:** system must be compatible with other equipments (*e.g.* can be placed under an optical microscope or inside a SEM chamber) to evaluate environmental effects.

These four specifications are delicate to fulfill simultaneously, especially at the sub-micron scale. The development and validation of a dedicated tool for micro-mechanical tests, with an appropriate procedure of sample preparation, were one of the key challenges of this PhD work. The double-torsion and four-point bending show their capacity to control the crack propagation in a sub-micron system. Most of our attention will then be dedicated to these two techniques.

II.3.1 Four-point bending

Bending tests are commonly used for studying the mechanical behavior of brittle materials. Its popularity comes from its relative simplicity: the load is applied by pins and the specimen, with a simple geometry, does not need to be fixed. In addition, 4PB has gained more attention than 3PB because of the constant bending moment between the two inner pins. Thus, in a 4PB configuration, the stress applied to the specimen on the tensile face is unidirectional and constant between the two inner pins (figure II.17 and table II.1).

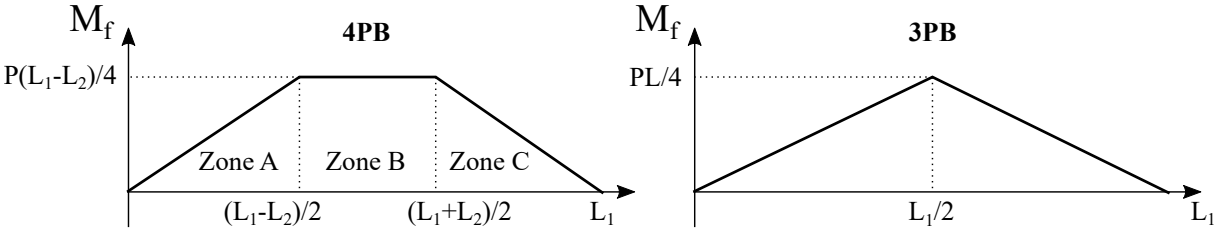


Figure II.17: *Schematic illustration of the bending moment in the 4PB case versus in the 3PB case, L_1 is the distance between the outer spans and L_2 is the distance between the inner spans.*

Table II.1: *Equations for the calculation of shear force and bending moment for 4PB test*

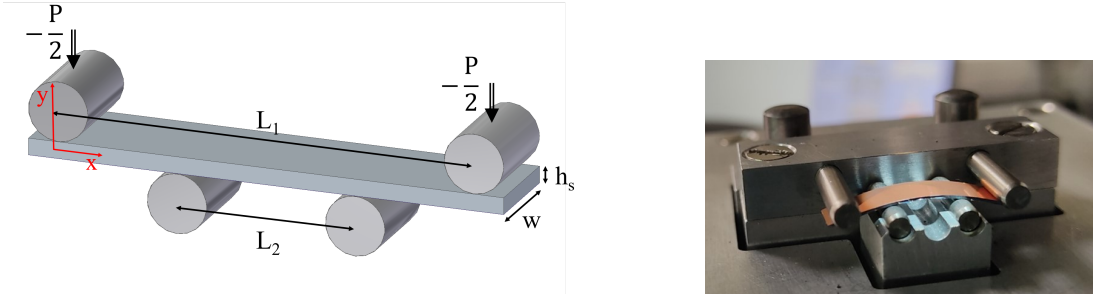
	Zone A	Zone B	Zone C
T(x)	P/2	0	-P/2
M_f(x)	-Px/2	-P(L_1-L_2)/4	-P(L_1-x)/2

Among many applications, 4PB is widely used to test thin films deposited on substrates, and thus is well-documented in the literature for:

- the estimation of film fracture behavior [10, 54, 101],
- the characterization of interfacial adhesion [24, 59, 94],
- the investigation of microelectronic structure robustness (interconnections [10], seal-rings [126]).

II.3.1.1 Description of the test

We present in figure II.18 a schematic of the 4PB configuration applied to a single-material specimen.



(a) ***(b)***

Figure II.18: *(a) four-point bending model:* $\boldsymbol{L_1}$ *and* $\boldsymbol{L_2}$ *are the distances between the pins,* $\boldsymbol{W}$ *is the specimen width and* $\boldsymbol{P}$ *is the applied load and (b) real configuration with the prototype testing machine developed in this work*

Now, considering the assumption of the Euler-Bernoulli beam theory, the deformation along x-direction can be derived (equation (II.25)). It is proportional to the distance y between the neutral axis and the calculation point.

$$\epsilon_{xx}(y) = \frac{-yM_f(x)}{I}\frac{(1-\nu^2)}{E} \tag{II.25}$$

where I is the area moment of inertia of the cross-section given by:

$$I = \frac{wh_s^3}{12} \tag{II.26}$$

Now, we focus on zone B where the bending moment is constant. Another assumption is made to calculate the stress in the plate: the tensile and compressive behaviors are

symmetric so that the neutral axis is located at half the section. The stress applied to the specimen into zone B is calculated by the following equation:

$$\sigma_{xx}(y) = -\frac{yM_f(x)}{I} \tag{II.27}$$

Combining equations (II.26) and (II.27) at y=± $h_s/2$ and between the two inner pins, the maximal stress is given by:

$$\sigma^s_{xx} = \pm\frac{3P(L_1 - L_2)}{2wh_s^2} \tag{II.28}$$

II.3.1.2 Stresses in thin film induced by 4PB

Considering the problem as fully elastic, the total stresses in thin films on substrates subjected to 4PB are calculated as the algebraic sum of the stresses induced by the deposition process (II.24) and the stresses induced by the substrate deformation (equation (II.28)).

The stress σ^s_{xx} supported by the substrate during the 4PB test is calculated with equation (II.27). Moreover, we assumed the film to be perfectly adherent to the substrate, so that the longitudinal strains of the film and the substrate can be considered as similar at y=$h_s/2$.

$$\epsilon^f_{xx} = \epsilon^s_{xx} \tag{II.29}$$

The longitudinal strain in the film is calculated by:

$$\epsilon^s_{xx} = \sigma^s_{xx}\frac{1-\nu_s^2}{E_s} \tag{II.30}$$

Using the condition of plane strain, the stress σ^f_{xx} applied to the film during the 4PB test is:

$$\sigma^f_{xx} = \frac{E_f(1-\nu_s^2)}{E_s(1-\nu_f^2)}\sigma^s_{xx} \tag{II.31}$$

Combining equations (II.24) and (II.31), the total stress in the film is defined as:

$$\sigma_f = \sigma_{res} + \sigma^f_{xx} = \sigma_{res} + \frac{E_f(1-\nu_s^2)}{E_s(1-\nu_f^2)}\frac{h_s M_f}{2I} \tag{II.32}$$

II.3.1.3 Sample description and preparation

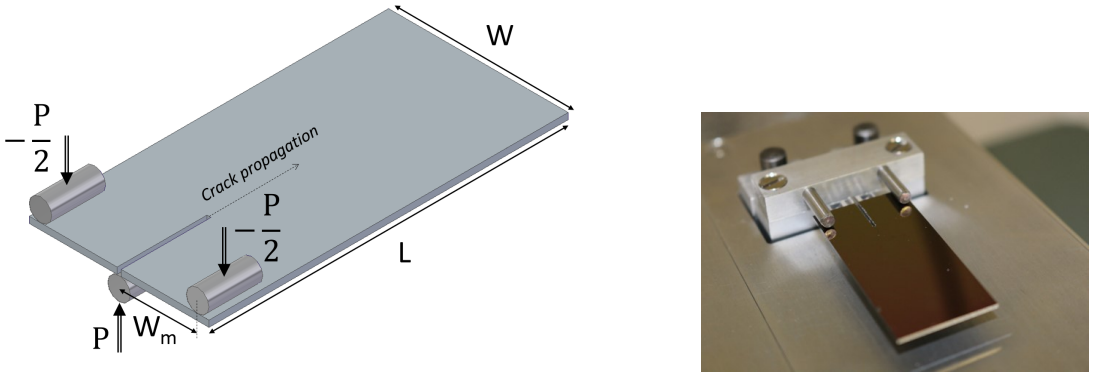
Small rectangular samples, having a width of 4 mm and a length of 20 mm, are collected from wafers to perform 4PB tests. They were mechanically sawed or cleaved depending on the level of stress targeted into the silicon. Indeed, as shown in the previous section, the maximal stress reached into the film is directly linked to the stress level in the silicon. In addition, silicon is highly brittle and sensitive to notch effect (*i.e.* pre-existing defects). The cleavage has been found as the best method to give the highest fracture strength to the silicon substrate.

II.3.2 Double-torsion

Since its first introduction in the late 1960's, the double-torsion test has gained an increasing attention for characterizing fracture behavior of a wide range of ceramics (zirconia [70], silicon nitride [45, 102], glasses [7] and silicon [16]). The advantage of this technique relies on the stability of the crack propagation. Indeed, the double-torsion allows for the propagation of relatively long cracks in a controlled manner even for highly brittle materials. With the double-torsion test, estimation of fracture toughness [128, 16], generation of crack velocity versus stress intensity curve [70, 19] and also cyclic fatigue studies [132] under different environmental conditions can be conducted. Another claimed benefit was the independence of the stress intensity factor K_I from the crack length which allows testing materials even if the crack cannot be observed. This capability was also discussed by some authors showing a non-constant value for K_I along with the crack propagation, but the variation remains low [19, 41, 129]. This point is detailed later.

II.3.2.1 Description of the test

The double-torsion configuration consists in loading a rectangular plate on one edge to induce torsional deformation into the two symmetrical plate's halves. The loading can be performed in a four-point or three point bending configuration. The double-torsion specimen, parameters and loading are detailed in figure II.19. In this work, the plate is loaded in a 3PB configuration with a lower pin centered into the notch. The upper face is under tension.



(a) *(b)*

Figure II.19: *(a) double-torsion loading configuration and specimen geometry:* $\boldsymbol{P}$ *is the load,* $\boldsymbol{W}$ *the sample width,* $\boldsymbol{W}_m$ *the moment arm and* $\boldsymbol{L}$ *the sample length and (b) real configuration*

With in the double-torsion configuration, two modes can be evaluated: one to determine the critical fracture toughness K_{IC}, and one to plot the v-K_I curve to highlight the influence of the environment on cracking (see chapter I).

II.3.2.2 Double-torsion for determining K_{IC}

To estimate K_{IC}, after an initial crack initiation step, the sample is unloaded and then reloaded with a displacement rate at 500 µm/min until the specimen breaks (figure II.20). The rate is selected sufficiently high to limit any slow crack growth caused by air humidity during the test. From this test, the critical load value $P_{critical}$ is obtained.

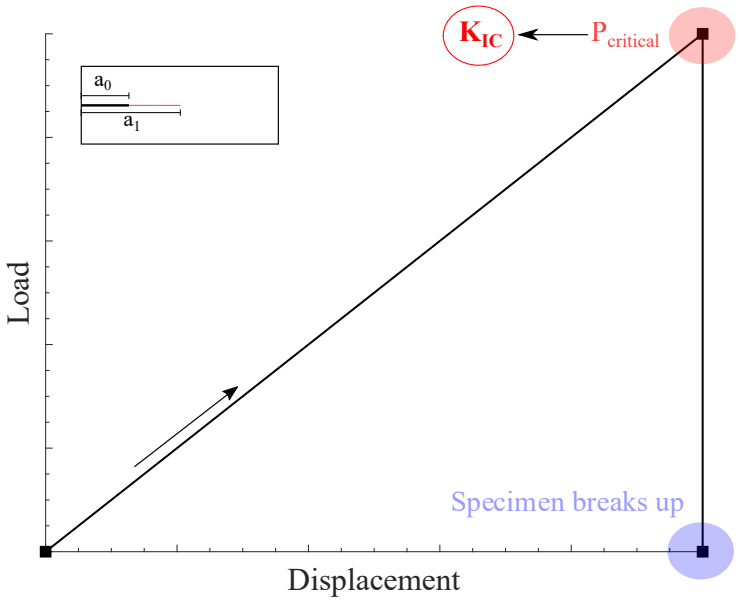


Figure II.20: *Schematic load-displacement curve during a K_{IC} test*

The stress intensity factor at the crack tip is calculated by analytic equation (II.33).

$$K_{I(analytical)} = \frac{PW_m}{t^2}\left(\frac{3(1+\nu)}{W\psi(t,W)}\right)^{1/2} \tag{II.33}$$

The parameters are defined in figure II.19. The thickness correction factor $\psi(t,W)$, depending on the sample width W and thickness t, is given by (II.34):

$$\psi(t,W) = 1 - 1.2604\left(\frac{t}{W}\right) + 2.4\left(\frac{t}{W}\right)exp\left(\frac{-W\pi}{2t}\right) \tag{II.34}$$

Equation (II.33) leads to the fracture toughness for a plane stress condition and for a K_I value independent of crack length. Chevalier *et al.* reported a slight but significant dependence of the analytic value of K_I on the crack length for zirconia samples [19]. They attributed this dependence to the unbroken ligament at the compressive side of the sample (see figure II.21) and proposed a correction given in equation (II.35).

$$K_I = K_{I(analytical)}\left(\frac{a_1}{a_0}\right)^{\gamma} \tag{II.35}$$

where the exponent γ depends on both the tested material and the specimen geometry and is determined experimentally [19] (a_0 is the notch length and a_1 the length of the pre-crack).

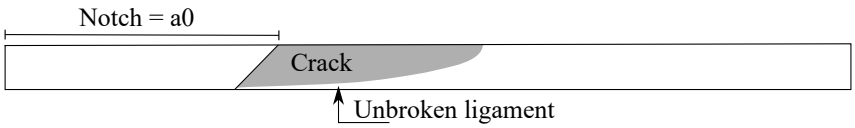


Figure II.21: *Schematic representation of the crack cross-section with the inclined notch end, the crack front and the unbroken ligament (reproduced from [19])*

II.3.2.3 Double-torsion for determining v-K_I curve

Double-torsion relaxation test was also used to investigate slow crack growth. The specimen is loaded at a rate of 20 µm/min until the crack extends and then, the displacement is held constant (figure II.22). During this time period, the crack length and the load are recorded. The load decreases progressively as the crack grows. As we performed *in situ* testing under a light microscope, the crack length is directly measured.

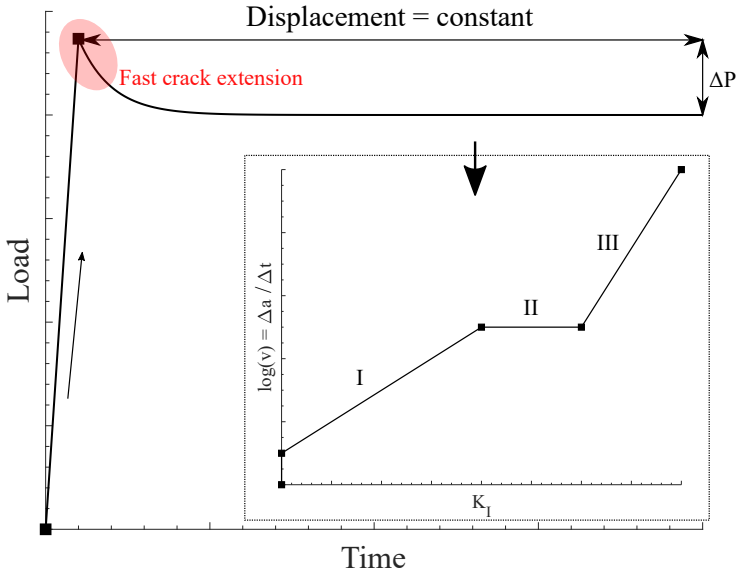


Figure II.22: *Schematic load-time curve during a relaxation test and the schematic v-K curve in insert*

K_I is calculated from the load values, with equations (II.33) and (II.35). Then, from the monitoring of crack length *versus* time, the crack growth rate is estimated as *da/dt*. Thus, the crack growth rate and the stress intensity factor are obtained and the *v-K* curve is plotted for the specimen (figure II.22).

The relaxation test is not the only method to get the *v-K* curve from a double-torsion test. However, the constant-load [122] and constant-displacement [32] rate tests provide only one point on the *v-K* diagram per test while the relaxation test gives access to the entire curve in a single test.

II.3.2.4 Sample description and preparation

The double-torsion specimen is a rectangular plate, namely 40 mm by 20 mm. The plates are mechanically sawed from the wafer. A notch is then made by circular sawing. The notch is about 10 mm long, and is centered with respect to the width of the sample. Due to the circular shape of the saw, the end of the notch is inclined as shown in figure II.23.

To initiate a crack, the specimen is loaded at a rate of 20 μm/min. Then, when an event is noted on the load-displacement curve, the sample is quickly unloaded at 500 μm/min. The rapid decrease in load (*i.e.* the event) is due to the crack extension from the notch. At this point, the notch length and the initial crack length can be measured by light microscopy on the tensile face and respectively correspond to the parameters a_0 and a_1.

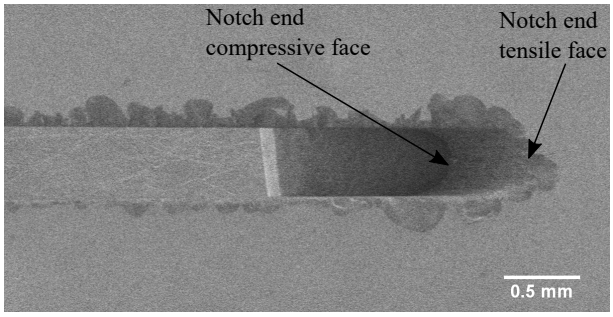


Figure II.23: *SEM top view of the inclined notch end*

II.3.3 Bending micro-machine description

Due to the small scale issue and the need to observe *in situ* the crack propagation, a laboratory-made device was developed by MATEIS electronic team, specifically for this work. A detailed opened view of the machine is given in figure II.24. The micro-machine is composed of: the electronic part and the motor (1) which has its rotation transmitted to a worm screw by a belt (2). Then, the horizontal displacement of the low part of the inclined plane due to the worm screw is transmitted to a vertical displacement of the upper pins (4) with a groove (3). While applying the vertical displacement on the sample (5), the load is monitored by the load cell (6) positioned just below the sample and lower pins. The load range can vary from 0 N to 100 N with a precision of 0.01 N. The lower pins are removable to perform four-point or three-point bending (as in the double-torsion configuration) depending on the experimental need.

The micro-machine is very compact, so that it can be used for *in situ* testing under a light microscope or into the chamber of a scanning electron microscope. Moreover, it allows the direct imaging of the tensile face of samples either in bending or double-torsion tests, which is required for monitoring the crack growth in our films.

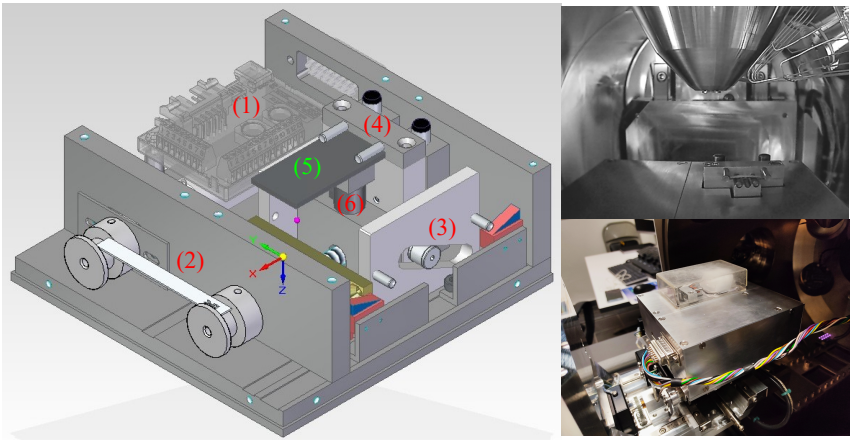


Figure II.24: *Detailed view of the components composing the bending micromachine: (1) electronic part (2) belt (3) groove (4) upper pins (5) specimen (6) load cell; and real configurations into SEM chamber*

II.4 Direct observation methods

Throughout this chapter, the observation of cracks is a requirement for both nanoindentation-induced cracks (*ex situ* in this work) when calculating the fracture resistance parameters and for bending-induced cracks (*in situ* and *ex situ* in this work) when monitoring the crack growth. Two methods were used: the Atomic Force Microscopy (AFM) and the Scanning Electron Microscopy (SEM), coupled, or not, with a Focused Ion Beam (FIB) column.

II.4.1 Atomic force microscopy

Atomic Force Microscopy is a scanning probe microscopy with a maximal vertical resolution below the nanometer. This method measures topography of surfaces using a probe referred as the cantilever. A piezoelectric transducer moves this cantilever over the sample surface to scan it. When the tip approaches the surface, the interaction forces between the tip and the sample deflect the cantilever towards the surface and inversely when the tip is far from the surface (and so when there is less/no interaction forces). All sample-probe interactions induce cantilever deflections detected by a laser beam focused on it. Different imaging modes are available: contact (with a constant force or height), non-contact (vibrating probe) and tapping (vibrating probe) modes. Advantages of the AFM beyond its high precision are its capacity to image the considered zone directly on 300 mm wafers.

In this study, we used the tapping mode to image the cube-corner indents and to measure the film surface roughness. In this mode, the cantilever oscillates at a frequency close to its resonance and the oscillation amplitude changes with surface topography which are monitored and used as control signal. The advantage of this mode is that the tip is only periodically in contact with the sample and so, sliding forces are avoided contrary

to the full-contact mode. Acquisition was done in ambient environment with a Bruker Dimension FastScan AFM with a rate of 0.5 Hz and a horizontal resolution of 10 nm.

II.4.2 Scanning electron microscopy and focused ion beam

Scanning electron microscopy principle is to scan a focused electron beam over a surface to create an image. Electrons of the beam interact with the sample, and this interaction produces various signals that are used to obtain, for instance, surface topography and composition information.

SEM was used in our study for two purposes:

- **imaging the cube-corner indents.** The SEM is associated with a FIB to mil the sample. The cross-sections are then imaged with the SEM to observe the crack morphology. When working with the dual-beam mode of the microscope, the gallium ion source (FIB) is used to mill the materials very precisely (*sputtering*). The SEM-FIB equipment used at STMicroelectronics was a ThermoFisher Helios 5 DualBeam. On this equipment, 300 mm wafers can be imaged[2].
- **perfoming *in situ* 4PB testing.** To observe the damage behavior of thin films, *in situ* tests are performed in 4PB configuration. Tests were carried out at the laboratory MATEIS with a ThermoFisher Quattro ESEM. The environmental conditions will be detailed in chapter IV[3].

Both SEM microscopes are used in secondary electron emission imaging mode to inspect the topography of sample surface. The SEM images are performed in high vacuum and the operating voltage is set at low values (between 2 and 5 kV) to limit the interaction between the electron beam and the insulating material.

[2]Thanks to the Physical Characterization team at ST Crolles site

[3]Courtesy of V. Trillaud at MATEIS laboratory

CHAPTER III

Influence of hydrothermal aging on mechanical properties of dielectric films

Hydrothermal accelerated aging tests are performed on products to ensure product reliability. In our study, a particular attention is paid to the mechanical behavior of dielectric thin films and their potential evolution under environmental conditions.

Thus, the aim of this chapter is to characterize dielectric thin films at different aging states to study potential variations and understand the associated phenomena.

First, we present the adopted experimental protocol, based on the standard aging tests detailed in chapter I. Then, the initial mechanical properties are measured after film deposition, and their evolution after temperature cycling and temperature-humidity storage is studied. For each test, the involved mechanisms of aging are identified, and discussed regarding literature studies and the chemical nature of the films.

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III.1 Experimental protocol

Hydrothermal accelerated tests are used to assess the reliability over time of microelectronic products (see chapter I). For automotive applications, the Automotive Electronic Council standardizes these tests. This standard defines different environmental conditions (temperature, humidity level and time) according to the product service-life environment, the failure mechanism and the operating temperature requirements to ensure product reliability [1].

In this study, two standard aging tests were implemented: Temperature Cycling (TC) and Temperature-Humidity Storage (THS). The evolution of mechanical properties of dielectric thin films with temperature and humidity was monitored. Standard conditions presented in chapter I were used.

III.1.1 Definition of T_0 and T_{0b} reference states

The dielectric films have different characteristics, so they are not deposited at the same interconnect level. The studied silicon nitride (SiN_xH_y) is a passivation layer and is the last deposited. The undoped silicate glass (SiO_2:H) is a material found in the global metal levels. The two carbon-doped silicon oxides (SiOC:H and pSiOC:H) are deposited where the copper density is the highest (*i.e.* first metal levels) as they have a low dielectric constant. These two *low-k* films are deposited at the first metal levels, and therefore have to withstand temperature elevations corresponding to the deposition of other layers (see the general introduction).

For the 28 nm technology node, we estimate the average number of dielectric layers to about ten. Therefore, ten cycles from 21°C to 400°C at ambient humidity level (about 40% RH at 21°C) were carried out on the SiOC:H samples before starting the aging tests to simulate processing conditions. We performed this thermal treatment with an environmental chamber heated at 400°C. The specimens were stored 15 minutes inside and 15 minutes outside the chamber. These additional cycles are less relevant for both SiN_xH_y and SiO_2:H as they are on the last levels of the interconnect part.

The reference *as-deposited* state is labeled T_0, while the reference *after thermal treatment* state is labeled T_{0b} in the following sections.

III.1.2 Experimental protocol

To measure the evolution of mechanical properties with environmental aging, the films were characterized at different steps (figure III.1). First, the properties were evaluated just after material deposition (T_0). Besides, for both SiOC:H and pSiOC:H, the properties were also measured after process thermal treatment (T_{0b}). Then, the samples were exposed to temperature cycling with a measurement at 500 and 1000 cycles (TC_{500} and TC_{1000}). Finally, the specimens were stored in a humid environment and the properties

were evaluated after 250, 500 and 1000 hours (THS_{250}, THS_{500} and THS_{1000}).

All characterizations were performed *ex situ* in ambient environment (21°C and 40% RH). The aging tests/characterizations sequence has to be performed as quickly as possible to limit the variations due to the wafer storage post aging. All wafers were thus stored in lab environment for a maximum of one half-day between the aging tests and the nanoindentation measurements.

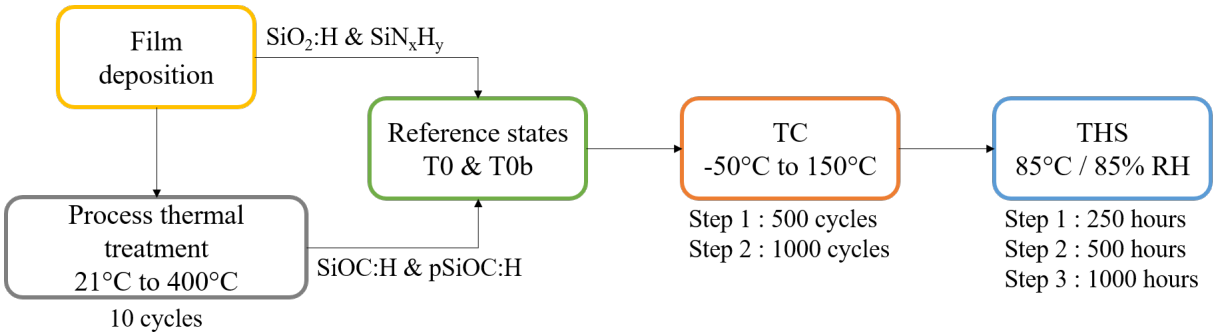


Figure III.1: *Aging protocol applied to specimens: the TC and THS conditions are defined by the AEC standard (see chapter I) [1]*

III.2 Mechanical properties at T_0

Wafer-curvature measurement was used to estimate the averaged film residual stress. The reduced modulus, hardness and fracture resistance were measured by nanoindentation. The reader could refer to chapter II for the detailed experimental methods.

As the measurement of mechanical properties by nanoindentation at very small thicknesses is challenging, a preliminary study was performed on two similar SiO_2:H (USG) deposited on silicon wafers with different thicknesses (616 nm and 1620 nm) for calibration. Then, nanoindentation measurements were carried out on the four dielectric thin films previously presented and the results for each film are discussed in the following sections. Each layer thickness t_f was controlled by ellipsometry after deposition and was reported in table III.1. The thicknesses are those deposited in actual products. The silicon wafer substrates have thicknesses of 775 µm.

Table III.1: *Films thicknesses controlled by ellipsometry after deposition*

Materials	**SiN_xH_y**	**SiO_2:H**	**SiOC:H**	**pSiOC:H**
t_f (nm)	595 ± 5	616 ± 9	569 ± 10	219 ± 3

III.2.1 Preliminary considerations

III.2.1.1 Roughness *versus* minimal indentation depth

One challenge in testing thin films in nanoindentation is the influence of surface roughness, which can affect the determination of the true contact area between the indenter and the tested material. Thus, sample surface for nanoindentation should be very smooth and the indentation depth should largely exceed the sample roughness. The ISO standard referenced a study investigating the effect of roughness on hardness measurements of metals and gave a criterion of $h > 20R_{ms}$ [64]. This criterion is not unique. For example, Miller *et al.* proposed the criterion $h > 5R_{ms}$ for cement paste [107].

The RMS roughness was measured thanks to Atomic Force Microscopy by scanning an area of 5x5 µm^2 which is larger than the Berkovich imprint size. The RMS roughness results are 2.1, 3.2, 0.5 and 0.4 nm respectively for SiN_xH_y, SiO_2:H, SiOC:H and pSiOC:H. Regarding each film thickness, the condition $h > 20R_{ms}$ corresponds to respectively 7, 10, 2 and 4% of the film thickness, which will be considered as the minimal depth for the properties extraction.

III.2.1.2 Hay-Crawford correction for reduced modulus determination

To take into account the substrate influence and to determine the film reduced modulus, the Hay-Crawford model described in chapter II was used to correct the measured reduced modulus, considering a substrate modulus of 170 GPa [53].

To confirm the validity of the Hay-Crawford correction in our case, nanoindentation tests were carried out on two SiO_2:H films of two thicknesses: 616 nm and 1620 nm[1]. Both films have similar deposition precursors and close compressive residual stresses of -189 MPa and -193 MPa respectively for the 1620 nm and 616 nm-thick films. Figure III.2 presents the reduced modulus as a function of the normalized indentation depth to the film thickness for both films.

[1]This exercice could not be done with the *low k* films (more critical due to their lower expected reduced modulus) because they have gradient properties. Moreover, films of thickness greater than 1 µm were not available.

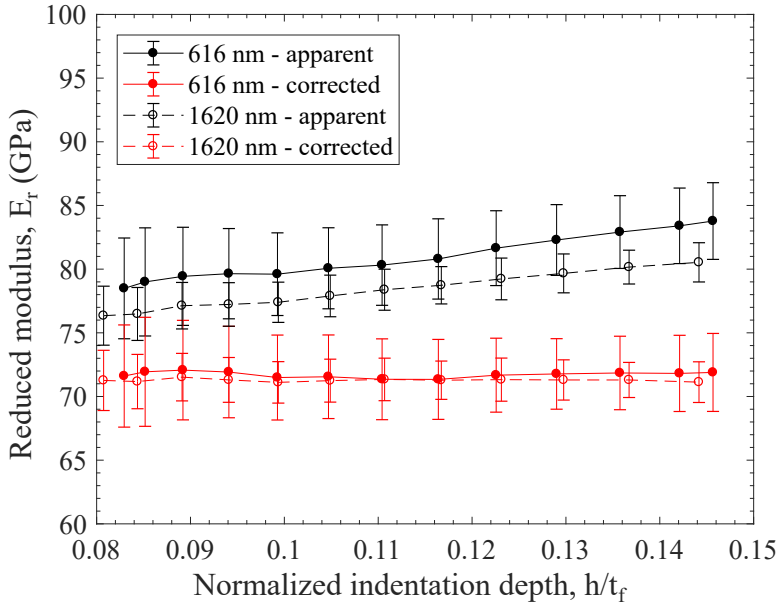


Figure III.2: *Reduced modulus as a function of normalized indentation depth for two undoped silicate glasses deposited on Si wafers: t_f = 616 nm and t_f = 1620 nm. The film reduced modulus (red curve) is obtained after applying the Hay-Crawford correction [53]*

The Hay-Crawford model does accurately compensate for the substrate influence with a constant corrected reduced modulus for the two films until at least 15% of the film thickness. Therefore, the effectiveness of the Hay-Crawford model for correcting nanoindentation data for our applications is confirmed on films of standard materials and with a relatively large thickness. This model will be used for all studied dielectrics except SiN_xH_y, as its reduced modulus is expected to be close to that of silicon.

Note: It is common practice in nanoindentation to extract the reduced modulus at a depth of 10% of the film thickness to obtain a substrate-independent film reduced modulus. However, here we note that the values measured at $h/t_f = 0.1$ are already 12% and 9% higher than the corrected ones for the 616 nm and 1620 nm-thick layers, respectively.

III.2.2 Film residual stress

Table III.2 summarizes the residual stresses measured after film deposition. We note that SiN_xH_y and SiO_2:H are under compressive stresses, while both SiOC:H and pSiOC:H are under tensile stresses at ambient temperature. This agrees with the CTE of these materials[2]. Indeed, the CTE of SiN_xH_y and SiO_2:H are measured respectively at 2.8 and 1.8 ppm/°C, which is lower than the silicon CTE equals to 3, so the films show compressive residual stresses. Concerning SiOC:H and pSiOC:H, the CTE are measured respectively at 11 and 13 ppm/°C. Thus, they show tensile residual stresses. In addition, the relative experimental scatter for pSiOC:H is substantially higher than for the three

[2]ST internal characterization

other configurations. The small thickness and stiffness of the film may explain that effect, as it induces smaller curvature of the wafer, therefore less accuracy in the measurement.

Table III.2: *Film residual stresses measured by wafer-curvature measurements after deposition*

σ_{res} (MPa)	SiN_xH_y	SiO_2:H	SiOC:H	pSiOC:H
T_0	-379 ± 8	-193 ± 8	49 ± 8	52 ± 23

III.2.3 Reduced modulus

In figure III.3, the measured reduced modulus according to the normalized indentation depth by the film thickness is plotted for each dielectric film deposited on a Si wafer substrate. Only the depths between 8 and 20% of each film thickness are considered. Indeed, due to tip defects, film surface roughness, and tip calibration errors in this range, data below 8% are excluded (approximately 50 nm for the thicker films and 20 nm for pSiOC:H). Also, except for the two SiOC:H films, data above 20% of the film thickness are not available due to load cell limitation, so to homogenize the results, data above 20% are not plotted for all materials.

As expected, the reduced modulus of SiN_xH_y is close to the silicon one (E = 170 GPa), so its reduced modulus is constant along with the indentation depth, without correction (figure III.3a). This is not the case for SiO_2:H (figure III.3b) and both SiOC:H films (figures III.3c and III.3d), where the measured reduced modulus increases monotonically upon the tip penetration. In addition, we note that for both SiOC:H and pSiOC:H, despite the application of the Hay-Crawford correction, the reduced modulus still increases even if the trend is less pronounced than without correction.

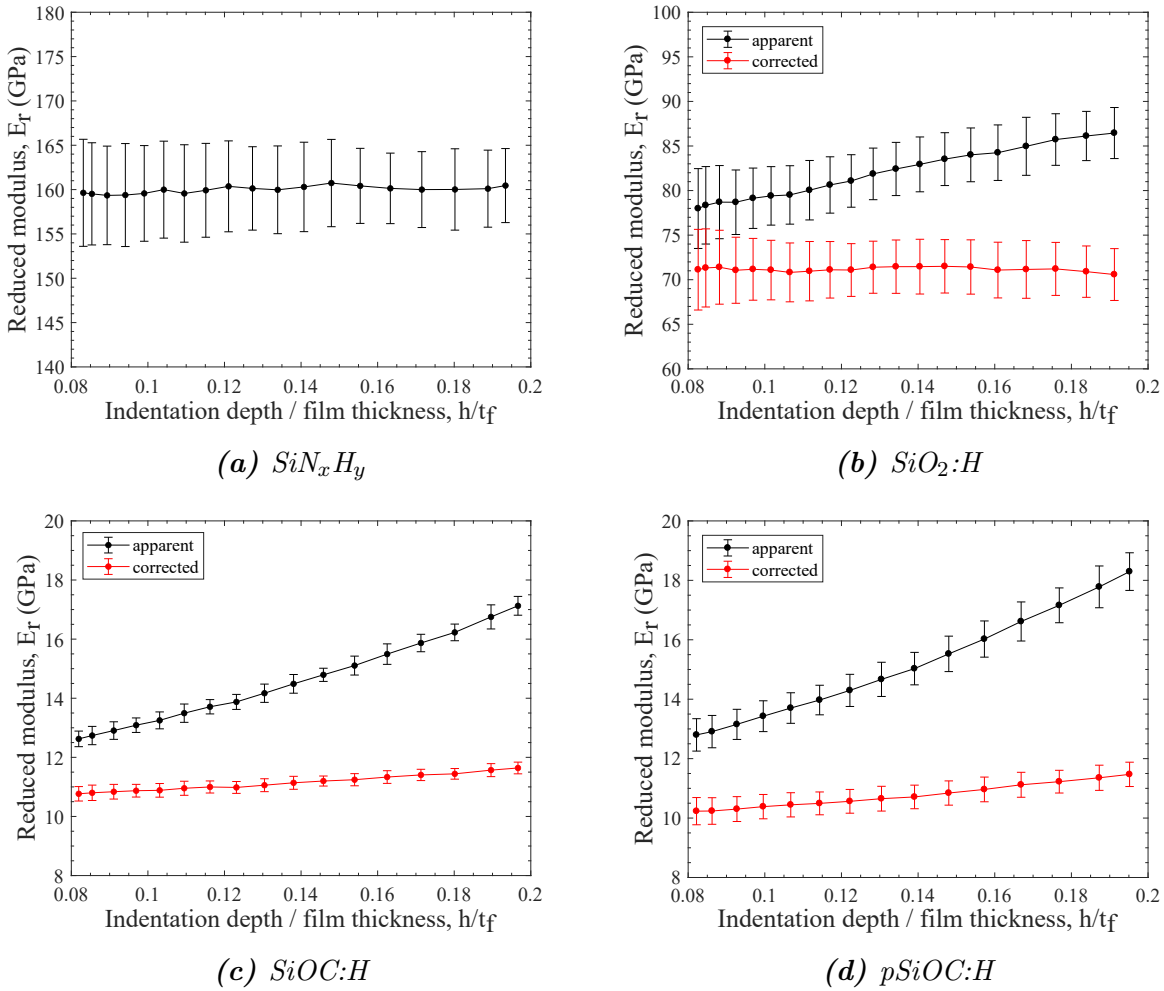


Figure III.3: *Reduced modulus at T_0 as a function of normalized indentation depth h/t_f for (a) the 595 nm-thick SiN_xH_y (no correction applied) (b) the 616 nm-thick SiO_2:H (c) the 569 nm-thick SiOC:H and (d) the 219 nm-thick pSiOC:H*

An explanation can come from the porosity of these materials. Indeed, an overestimation of the elastic modulus measured by nanoindentation compared to other methods has already been reported in the literature for materials of same nature [31]. Du *et al.* compared the mechanical response of porous *ultra-low k* films under nanoindentation with two configurations: the film directly deposited on a silicon substrate and a bi-layer comprising a silicon substrate, the *ultra-low k* SiOC:H layer and an upper film of TEOS SiO_2, both deposited on Si substrate. To analyze the nanoindentation curves of the bi-layer configuration, authors used the Ogden hyperfoam model in their numerical study to describe the mechanical response of the porous SiOC:H mid-layer. Their results showed that during nanoindentation, a densification phenomenon increased the apparent film reduced modulus (table III.3). These results agree with the conclusion made by Bailey *et al.*, who showed that during nanoindentation of an *ultra-low k* porous SiOC:H, the obtained modulus is twice larger than the same film measured by Brillouin light scattering method [5].

Table III.3: *Literature results of Young's modulus of two ultra-low k films of thicknesses of 400 nm [31]. The* ***Min value*** *is the minimum value of the nanoindentation curve. The* ***Hay-Crawford*** *is the minimum value of the corrected curve with the Hay-Crawford model. The* ***Bi-layer*** *is the bi-layer result (500 nm-thick TEOS - 400 nm-thick ultra-low k - 500 µm-silicon substrate) obtained through nanoindentation and numerical simulation with the Ogden hyperfoam model.*

Young's modulus (GPa)	Min value	Hay-Crawford	Bi-layer
OMCTS[3]ULK	10	7.1	5.2
pSiOC:H ULK	9	5.9	2.6

The aim of our study being to compare the same film at different aging states, the results after Hay-Crawford correction are used. To compute a single value of reduced modulus for each film, the corrected data are averaged between 9 and 11% of the corresponding film thickness (table III.4). The standard deviation is calculated on 7x7 matrices of indents.

Table III.4 also provides literature values for reduced modulus. Overall, the reduced moduli measured in our study are in the same order of magnitude for similar PECVD films. Unfortunately, for the SiOC:H and pSiOC:H, the effect of the porosity cannot be discussed because porosity rate is not indicated.

Table III.4: *Film reduced modulus results measured by nanoindentation at T_0, averaged data between 9% and 11% of film thickness after Hay-Crawford correction application and literature values for similar PECVD dielectric materials*

E_r (GPa)	SiN_xH_y	SiO_2:H	SiOC:H	pSiOC:H
T_0	160 ± 5	71 ± 3	10.9 ± 0.2	10.3 ± 0.4
Lit. T_0	107-198 [17, 58, 12]	69-75 [17, 38]	6.2-12.2 [17, 10, 108]	

First, the properties of PECVD SiN_xH_y films show a large variability regarding their physical properties with the deposition conditions. Concerning the mechanical properties, Huang *et al.* reported that the Young's modulus and hardness of PECVD SiN_xH_y films increase with an increasing deposition temperature and RF power, and a decreasing chamber pressure [58]. Moreover, PECVD SiN_xH_y films are amorphous, so they contain a certain amount of hydrogen incorporated as Si-H and N-H bonds, which may decrease the mechanical properties from the crystalline Si_3N_4.

For PECVD SiO_2:H, the variation in mechanical properties also depends on the deposition conditions, especially on the precursor flow. Indeed, elastic moduli ranging from 67 to 76 GPa are internally reported at STMicroelectronics for SiO_2:H deposited with the same precursors with varying flow and RF power.

[3]OMCTS (octamethylcyclotetrasiloxane) is a precursor used to deposit *ultra-low k* films.

The cases of SiOC:H and pSiOC:H are more complex as the mechanical properties of such materials depend on the deposition conditions, but also on the material porosity fraction. Moreover, we saw in chapter II that pSiOC:H is not a homogeneous material as it is composed of three sub-layers with different properties. We note only a small difference between the reduced modulus of the SiOC:H and the pSiOC:H, while the properties of the pSiOC:H were expected smaller due to the higher porosity rate (8% for SiOC:H *versus* 17% for the pSiOC:H core layer and 13% for its capping). An additional measurement was therefore done on a pSiOC:H with a thickness of 742 nm. Figure III.4 details the sub-layers forming this new film compared to those of the 219 nm-thick pSiOC:H.

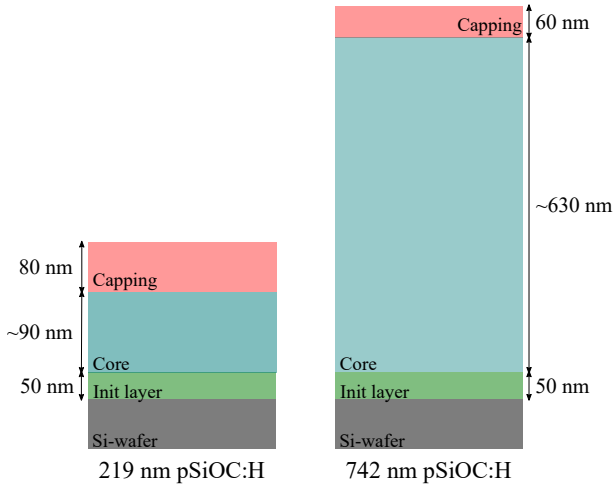


Figure III.4: *Detailed sub-layers forming the 219 nm and 742 nm-thick pSiOC:H films and corresponding indentation depth. The indentation depth is of 25 nm for the 219 nm-thick layer and of 80 nm for the 742 nm-thick layer.*

The reduced modulus for the 742 nm-thick pSiOC:H is measured at 7.4 ± 0.2 GPa *versus* 10.3 ± 0.4 GPa for the 219 nm-thick film. This difference could be attributed to the sub-layer structure of the two samples (*i.e.* the predominance of the core for the 742 nm-thick pSiOC:H). Indeed, STMicroelectronics internal characterizations of capping and core single-layers of thicknesses of 300 nm deposited on silicon substrates show that the reduced modulus of the capping is about 10.0 GPa and that of the core is about 8.5 GPa. Additionally, the very small thickness of the 219 nm-thick layer increases the experimental uncertainties in the determination of the true film reduced modulus.

III.2.4 Hardness

Figure III.5 presents the hardness evolution as a function of normalized indentation depth for all dielectric films. We note the hardness slightly increases until 15% of the film thickness for the dense materials, then stabilizes until at least 30% of the film thickness (figures III.5a and III.5b). Concerning the porous materials, the hardness shows an increase along with the indentation depth, but is still limited (figures III.5c and III.5d). This slight increase is, similarly to the reduced modulus, attributed to substrate effect

and densification of the film beneath the indenter. However, the substrate effect is less marked for the hardness than for the reduced modulus. This is explained by the size of the zone deformed plastically beneath the indenter, which is smaller than the zone deformed elastically [38].

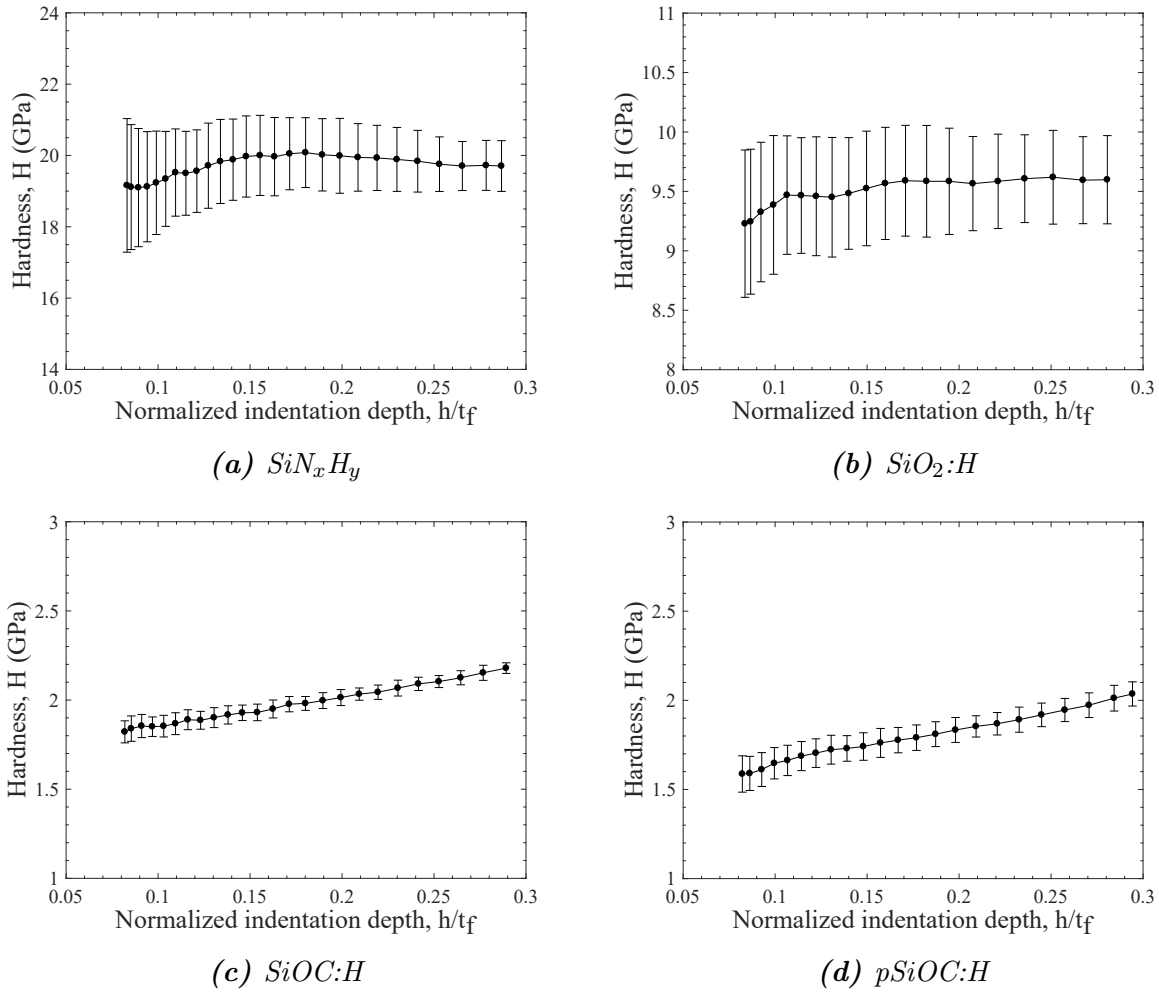


Figure III.5: *Hardness at T_0 as a function of normalized indentation depth h/t_f for (a) the 595 nm-thick SiN_xH_y (b) the 616 nm-thick SiO_2:H (c) the 569 nm-thick SiOC:H and (d) the 219 nm-thick pSiOC:H*

Thus, to minimize any substrate influence, the results are extracted directly from the measured hardness at 15% of the film thickness. Table III.5 summarizes the hardness results together with literature values for similar films. As for the reduced modulus, the hardness results are in the same order of magnitude as similar PECVD dielectric films. We can notice the high hardness value of SiN_xH_y, fitting well with its role of mechanical protection.

The hardness of the 742 nm-thick pSiOC:H (presented in figure III.4) was also measured through nanoindentation. The value is measured at 1.2 ± 0.1 GPa, which is slightly lower than the hardness of the 219 nm-thick layer, but the difference between the two films is less marked than for the reduced modulus.

Table III.5: *Film hardness results measured by nanoindentation at T_0, data extracted at 15% of film thickness and literature values for similar PECVD dielectric materials*

H (GPa)	**SiN_xH_y**	**SiO_2:H**	**SiOC:H**	**pSiOC:H**
T_0	20 ± 1	9.4 ± 0.4	1.9 ± 0.1	1.7 ± 0.1
Lit. T_0	11.9-23.8 [17, 58, 60]	7.6-9.5 [17, 38]	0.9-2.1 [10, 17, 108]	

III.2.5 Fracture resistance

In this section, fracture resistance of pSiOC:H, SiN_xH_y and SiO_2 films is investigated. To do so, cube-corner nanoindentation was performed for each film. The validity of such method and the related models is then discussed regarding the layer thickness and the observed crack morphology.

As a reminder, the fracture parameter estimated by nanoindentation K_{NI} is the sum of two terms: the apparent fracture toughness K_{app} and the film residual stress contribution K_{res}. K_{NI} estimation requires inputs such as the elastic modulus and hardness of the film, the indentation-induced crack length c, the indent print size a and the film residual stress σ_{res}. The reader may refer to chapter II for the method description.

For all materials, the upper limit of applied load is defined by rewriting equation (II.17), which ensures the containment of the zone deformed plastically within the film thickness [10]:

$$P_{max} \leq 2.6Ht_f^2 \tag{III.1}$$

with H the film hardness obtained through Berkovich nanoindentation and t_f the film thickness.

As seen in chapter II, the applied load is also limited to avoid the adhesive cracking at the interface film/substrate as we focused on the cohesive fracture resistance.

III.2.5.1 pSiOC:H

The fracture resistance estimation of pSiOC:H is of importance regarding the low properties of such material and the cracks observed in the BEoL during qualification procedure. Thus, the study focuses specifically on this material rather on the SiOC:H. However, as the 219 nm-thick layer is very thin, the limit between adhesive and cohesive failure is too close in terms of applied loads to control the formation of radial cracks without observing delamination at the film-substrate interface. Thus, to study the fracture properties of such material, the sample with a thicker layer (*i.e.* thickness of 742 nm) of similar composition presented in figure III.4 is used.

The applied load to initiate cracks is only a few hundred micro-newtons. Equation (III.1) reveals a load limit at 1 mN. However, the maximal load was limited to 0.4 mN to avoid delamination of the film from the substrate.

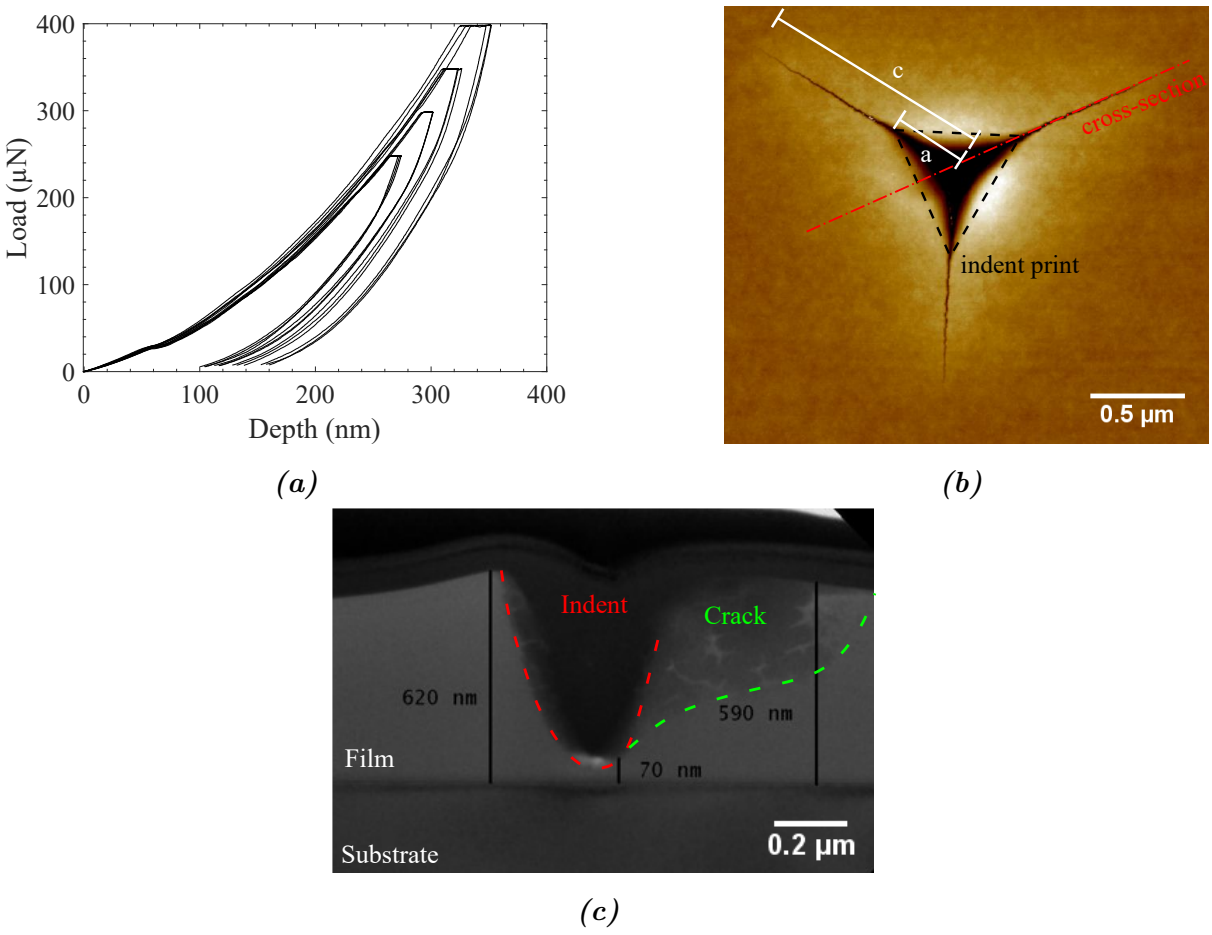


Figure III.6: *Cube-corner indentation of the 742 nm pSiOC:H at T_0: (a) load-displacement curves, (b) AFM top view, (c) STEM cross-section (HV = 200 kV). Note that the indent appears deeper on the STEM cross-section than the maximal penetration depth measured on the load-displacement curves. This artifact is attributed to the FIB/SEM lamella preparation.*

To confirm the containment of the cracks within the film, the indent cross-section and its surrounding cracks were imaged by Scanning Transmission Electron Microscopy (STEM). The cohesive cracking of the 742 nm pSiOC:H at 0.4 mN is confirmed (see figure III.6).

Figure III.7 presents the averaged crack length of three indents per load raised to power 3/2 *versus* the applied load.

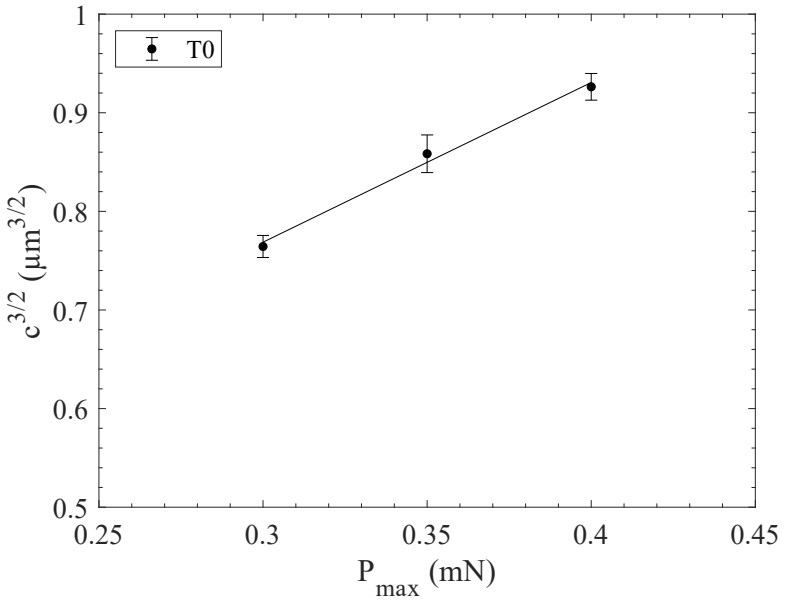


Figure III.7: *Average crack length raised to power 3/2 as a function of maximal applied load during cube-corner nanoindentation for the 742 nm-thick pSiOC:H at* T_0

To calculate the apparent fracture toughness, the cracks have to be measured. Indeed, if the condition c/a $\geq$ 2 is fulfilled (see figure III.6b), K_{app} is calculated with the Lawn equation (II.15). If not, the Laugier expression is used (equation (II.16)). This is linked to the crack morphology, when median-radial cracks are well-developed at high applied loads, the Lawn model is adequate, whereas the Laugier model is dedicated to Palmqvist cracks at lower applied loads.

Usually, the indent print size a is directly measured on the top view. However, as it can be seen in figure III.6, the edges of the residual indent are not clearly defined, so the parameter a cannot be accurately determined. Thus, we calculate it starting from the projected contact area of the perfect cube-corner indentation:

$$A = 2.6h_c^2 \tag{III.2}$$

From geometrical considerations, the indent print edges L_n are defined by:

$$L_n = \sqrt{\frac{4A}{\sqrt{3}}} \tag{III.3}$$

Then, a can be calculated using equation (III.4).

$$a = \frac{2}{3} sin\frac{\pi}{3} L_n \tag{III.4}$$

The ratio c/a is equal to 2.3 for a minimal applied load of 0.25 mN, so the Lawn model is used to calculate K_{app}. The morphology of the crack is also confirmed with the STEM cross-section, with a well-developed median crack in figure III.6c.

The reduced modulus, hardness and residual stress of the 742 nm-thick pSiOC:H are respectively measured at 7.4 ± 0.2 GPa, 1.2 ± 0.1 GPa and 59 ± 6 MPa. Table III.6 summarizes the calculated fracture resistance parameters.

Table III.6: *Fracture resistance parameters calculated for the 742 nm-thick pSiOC:H at* T_0

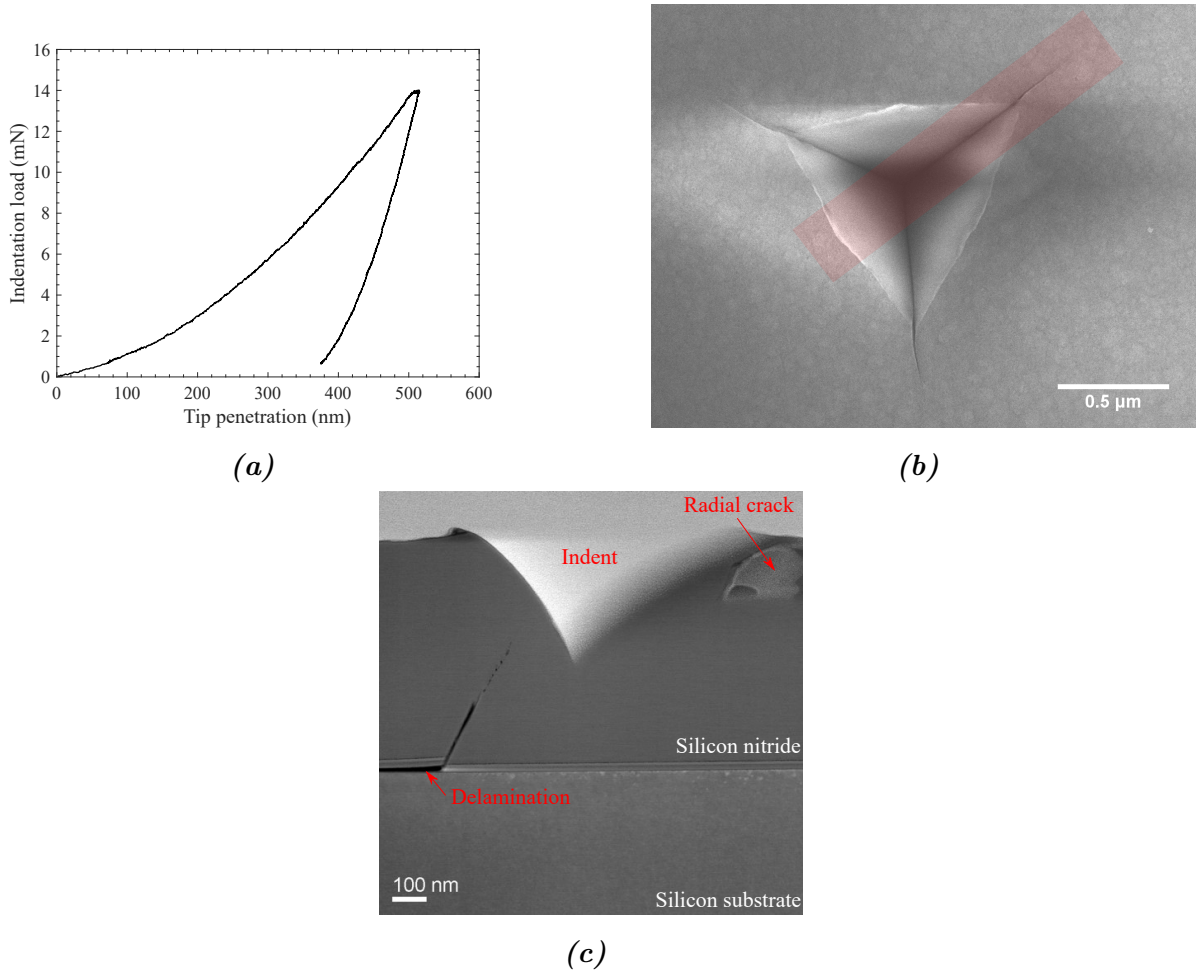
pSiOC:H	K_{app} **(MPa**$\sqrt{m}$**)**	K_{res} **(MPa**$\sqrt{m}$**)**	K_{NI} **(MPa**$\sqrt{m}$**)**
T_0	0.037 ± 0.003	0.066 ± 0.007	0.10 ± 0.02

In the literature, the fracture resistance measured by nanoindentation of similar porous SiOC:H is found between 0.078 and 0.086 MPa$\sqrt{m}$ [10, 111]. The value calculated in this study is slightly higher and the difference can come from a potential substrate influence. Indeed, Brillet showed that the K_{NI}, calculated for similar thicker films with similar residual stress, varied with the film thicknesses. She obtained a fracture resistance of 0.065 MPa$\sqrt{m}$ for a 1.8 µm-thick PECVD SiOC:H and of 0.086 MPa$\sqrt{m}$ for the same material deposited with a thickness of 1.0 µm, whereas the same residual stresses were measured for the two films [10].

III.2.5.2 SiN_xH_y

The maximal applied load is limited to 14 mN for the SiN_xH_y film (equation (III.1) gives an upper load limit of 18 mN). Figure III.8 gives the typical load-displacement curve, the SEM top view and the STEM indent cross-section. The elastic recovery is less marked during the unloading than for the pSiOC:H, which is illustrated by three well-defined indent edges. The indent print size is therefore directly measured on the SEM top view of the indent.

Three radial cracks emanating from the indent corners are observed. However, we also see a delamination that occurred between the silicon nitride and its substrate (STEM cross-section). To calculate K_{app} defined in equation (II.15), the absence of delamination between the film and the substrate is required. Indeed, when delamination occurs, a fraction of the mechanical driving force can be consumed in creating the new delaminated surfaces. It is then difficult to separate the energy corresponding only to the cohesive cracking of the film. Thus, regarding the delamination of the film and the fact that radial cracks are not yet well-developed in the film, K_{app} is not estimated for this layer.



(a) *(b)* *(c)*

Figure III.8: *Cube-corner indentation of the 616 nm silicon nitride film: (a) load-displacement curve, (b) SEM top view (HV = 2 kV), (c) STEM cross-section (HV = 200 kV)*

III.2.5.3 SiO_2:H

Similar investigation was done for the 616 nm-thick SiO_2:H film. Cube-corner indentation was performed with an applied load of 9 mN calculated with equation (III.1). However, as for the silicon nitride, we could not found an applied load range inducing only cohesive cracks in the film without delamination. Therefore, no calculation of the apparent fracture toughness could be done.

Consequently, the influence of accelerated aging tests on the fracture resistance determined by nanoindentation can be evaluated only for the 742 nm-thick pSiOC:H film.

III.3 Effect of process thermal treatment on SiOC:H properties

During the interconnection processing, SiOC:H layers, being located at the bottom of the stack, are exposed to numerous thermal cycles. That is why ten temperature cycles from 21°C to 400°C, reproducing this thermal treatment, were performed before the accelerated aging tests for these films (section III.1). Also, to monitor the fracture resistance of the pSiOC:H, the additional sample presented in figure III.4 was also studied.

III.3.1 Results

III.3.1.1 Film residual stress

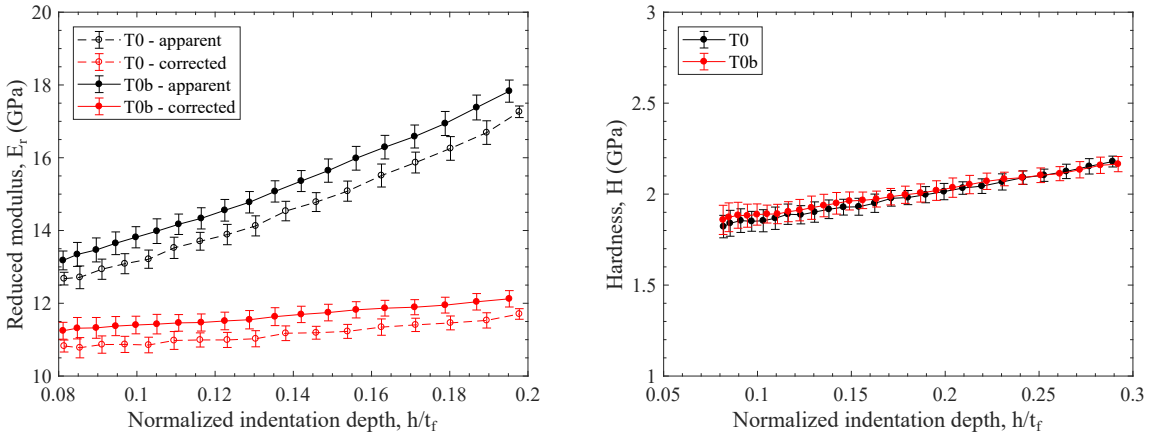
Film residual stress was measured after process thermal treatment for each SiOC:H film and the results are reported in table III.7 with respect to T_0. All SiOC:H films see their residual tensile stress built up. We also note that the increase is significantly smaller for the 742 nm-thick pSiOC:H, which seems less affected by the thermal cycling.

Table III.7: *Evolution of residual stresses with respect to T_0 after process thermal treatment (T_{0b}) for SiOC:H and pSiOC:H films.*

σ_{res} (MPa)	SiOC:H	pSiOC:H	pSiOC:H
t_f *(nm)*	*569*	*219*	*742*
T_0	49 ± 8	52 ± 23	59 ± 6
T_{0b}	86 ± 8	104 ± 23	72 ± 6
var/T_0	+76%	+100%	+22%

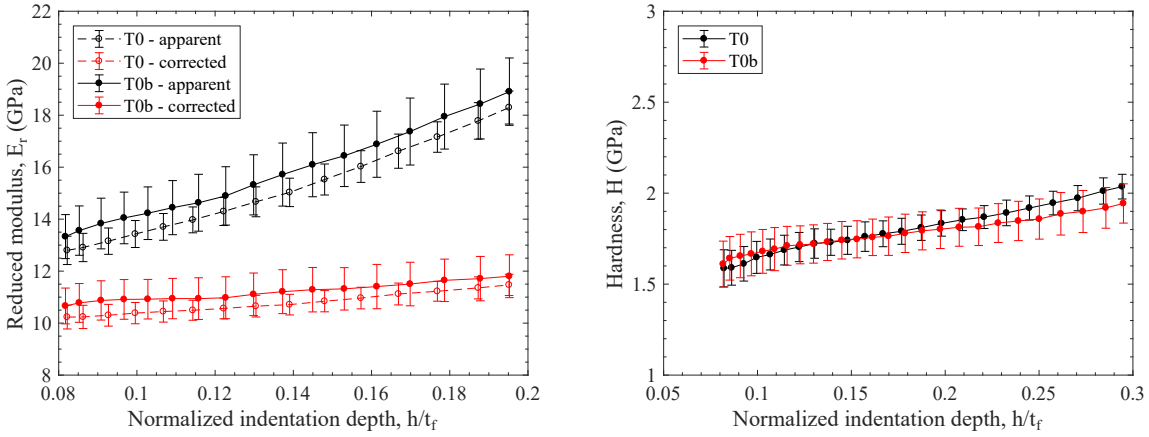
III.3.1.2 Reduced modulus and hardness

The next figures present the reduced modulus and hardness for all SiOC:H films at T_0 and T_{0b} before and after applying the Hay-Crawford correction for the reduced modulus. We observe a slight increase in reduced modulus from T_0 to T_{0b} for both the 569 nm-thick SiOC:H and 219 nm-thick pSiOC:H films, but is still limited. However, the hardness seems less affected by the thermal cycling. In contrast, we do not observe significant variation for the 742 nm-thick pSiOC:H for both properties.



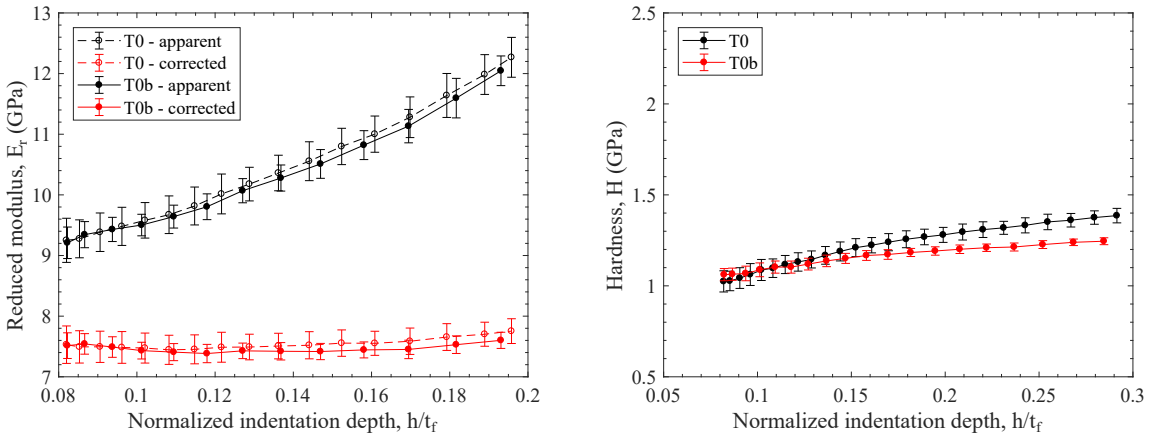
(a) ***(b)***

Figure III.9: *Reduced modulus (a) and hardness (b) as a function of normalized indentation depth h/t_f for the 569 nm-thick SiOC:H after deposition (T_0) and after process thermal treatment (T_{0b})*



(a) ***(b)***

Figure III.10: *Reduced modulus (a) and hardness (b) as a function of normalized indentation depth h/t_f for the 219 nm-thick pSiOC:H after deposition (T_0) and after process thermal treatment (T_{0b})*



(a) *(b)*

Figure III.11: *Reduced modulus (a) and hardness (b) as a function of normalized indentation depth h/t_f for the 742 nm-thick pSiOC:H after deposition (T_0) and after process thermal treatment (T_{0b})*

Tables III.8 and III.9 show the results at T_0, at T_{0b} and the evolution between T_0 and T_{0b}.

Table III.8: *Evolution of reduced modulus with respect to T_0 after process thermal treatment (T_{0b}) for SiOC:H and pSiOC:H films*

E_r (MPa)	**SiOC:H**	**pSiOC:H**	**pSiOC:H**
t_f *(nm)*	*569*	*219*	*742*
T_0	10.9 ± 0.2	10.3 ± 0.4	7.4 ± 0.2
T_{0b}	11.4 ± 0.2	10.9 ± 0.8	7.4 ± 0.1
var/T_0	+5%	+6%	0%

Table III.9: *Evolution of hardness with respect to T_0 after process thermal treatment (T_{0b}) for SiOC:H and pSiOC:H films*

H (MPa)	**SiOC:H**	**pSiOC:H**	**pSiOC:H**
t_f *(nm)*	*569*	*219*	*742*
T_0	1.9 ± 0.1	1.7 ± 0.1	1.2 ± 0.1
T_{0b}	2.0 ± 0.1	1.7 ± 0.1	1.2 ± 0.1
var/T_0	+2%	0%	0%

III.3.1.3 Fracture resistance

Cube-corner indention was performed on the 742 nm-thick pSiOC:H at T_{0b}. Figure III.12 shows the average crack length raised to the power 3/2 as a function of applied load and table III.10 summarizes the results. Only data for 0.35 and 0.40 mN are available, respecting the conditions of $c/a \geq 2$ and the absence of delamination.

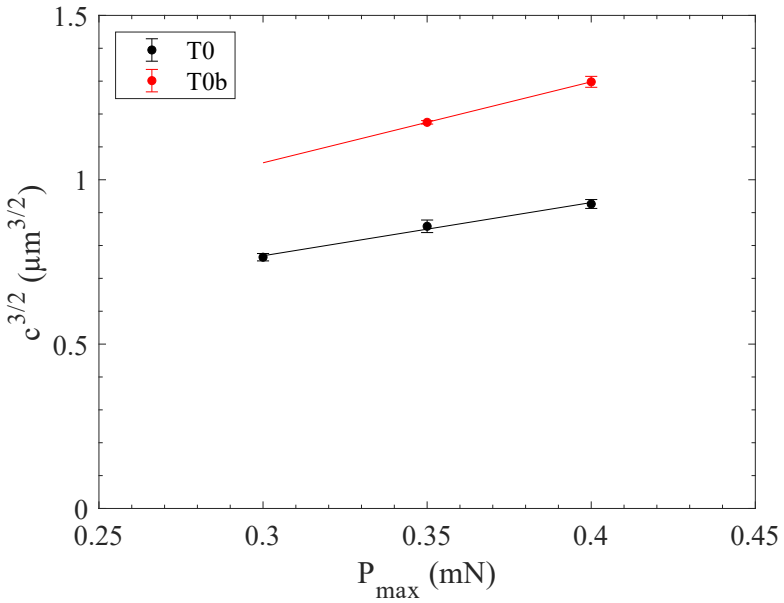


Figure III.12: *Average crack length raised to the power 3/2 as a function of the maximal applied load during cube-corner nanoindentation of the 742 nm-thick pSiOC:H for both as deposited (T_0) and after process thermal treatment (T_{0b})*

For these applied loads, measured crack lengths are significantly higher than at T_0, and thus a lower K_{app} is calculated. As the film sees its residual tensile stress increased (table III.7), the residual stress contribution is higher than at T_0 (*i.e.* K_{res} is proportional to σ_{res} in equation (II.18), leading to a significant increase in K_{res} as compared to T_0. The final fracture parameter K_{NI} is increased after process thermal treatment (T_{0b}), with a value about 17% higher than at T_0.

Table III.10: *Evolution of fracture resistance parameters with respect to T_0 after process thermal treatment (T_{0b}) for the 742 nm-thick pSiOC:H*

pSiOC:H	K_{app} **MPa**$\sqrt{m}$	K_{res} **MPa**$\sqrt{m}$	K_{NI} **MPa**$\sqrt{m}$
T_0	0.037 ± 0.003	0.066 ± 0.007	0.10 ± 0.02
T_{0b}	0.028 ± 0.002	0.093 ± 0.008	0.12 ± 0.02
var/T_0	-24%	+41%	+17%

III.3.2 Discussion

The residual stress of the films seems to be the most sensitive parameter to the process-like thermal cycling. The residual tensile stresses for the three SiOC:H films significantly increase. In addition, we also observe a slight increase in reduced modulus for both the 569 nm-thick SiOC:H and the 219 nm-thick pSiOC:H at T_{0b}.

When a PECVD oxide is annealed at high temperature (*i.e.* at least at the deposition temperature), Zhang *et al.* explained the increase in residual tensile stress by a desorption of impurities [148]. This desorption leads to a structural rearrangement of the film, which becomes denser, and therefore to an associated shrinkage inducing an increase in residual tensile stress.

Fourier Transform Infrared Spectroscopy (FTIR) was therefore used to identify the chemical structure of the 569 nm-thick SiOC:H and 219 nm-thick pSiOC:H films and understand the evolution, especially of the residual stress, from T_0 to T_{0b}. As a reminder, the process thermal treatment corresponds to 10 cycles from 21°C to 400°C. Figures III.13 and III.14 present the FTIR spectra respectively for SiOC:H and pSiOC:H films in the range 400-4000 cm^{-1}.

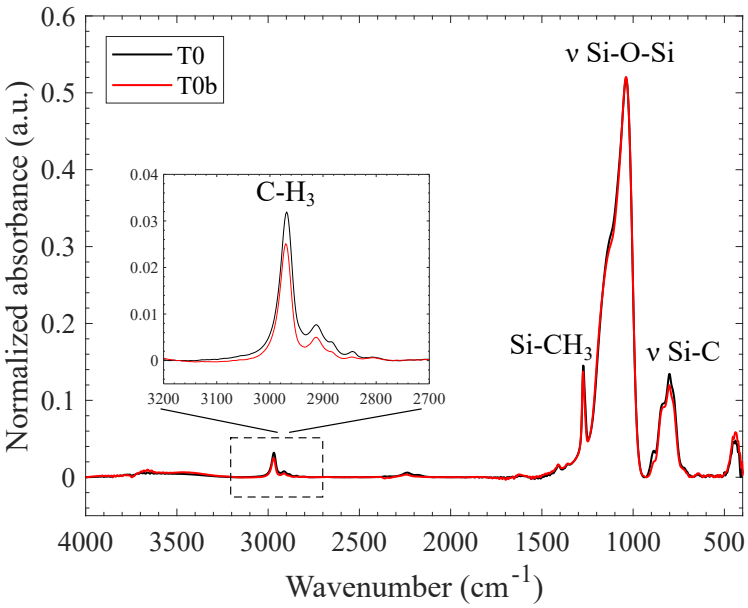


Figure III.13: *FTIR spectrum for the 569 nm-thick SiOC:H film as-deposited (T_0) and after process thermal treatment (T_{0b})*

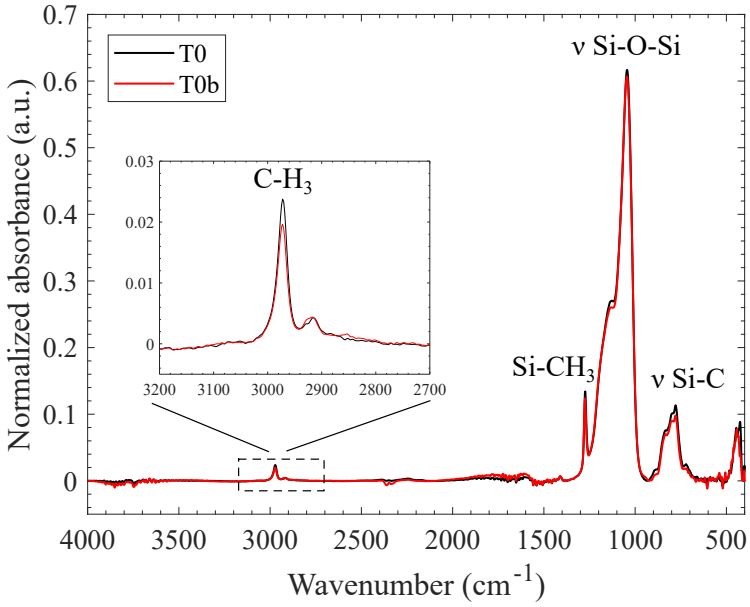


Figure III.14: *FTIR spectrum for the 219 nm-thick pSiOC:H film as-deposited (T_0) and after process thermal treatment (T_{0b})*

Both films have a similar structure composed of typical Si-O-Si bonds observed in the range 400-1400 cm^{-1}. In addition, an absorption band is found near 1270 cm^{-1} and corresponds to methyl groups linked to Si atoms. Over the range of 2800-3800 cm^{-1}, a predominant band at 2970 cm^{-1} is also detected and corresponds to CH_3 vibrations. The CH_3 contribution decreases after the process thermal treatment in both cases. The band height has decreased by 25% for the SiOC:H and by 17% for the pSiOC:H from T_0 to T_{0b} whereas the bands corresponding to Si-O-Si contributions remain similar.

As already mentioned in chapter II, introducing methyl groups in the Si network increases the steric hindrance, and so the free volume. Thus, we suppose a structural rearrangement of the films during the process thermal treatment, which could explain the decrease in CH_3 contribution, and therefore the higher residual tensile stress and the increase in reduced modulus of the SiOC:H films. However, the fact that the hardness does not vary as the reduced modulus might be intriguing, and confirms that the mechanism is still limited.

Regarding the fracture parameters of the 742 nm-thick pSiOC:H, the large increase in residual tensile stress after process thermal cycling can explain the longer cracks measured (increase in parameter c), so the decrease in K_{app}. Indeed, residual tensile stresses exist in the film, favor crack propagation and decrease K_{app}. In contrast, residual compressive stresses restrain crack propagation around indents. The final K_{NI} value, calculated as the sum of K_{app} (determined from the measurement of the crack lengths) and K_{res} (determined from the mean residual stresses), is also increased showing that the averaged residual stress of the film drives K_{res} and so K_{NI}.

The variation of residual stresses in the films is important and confirmed (the residual stress is an independent parameter). However, K_{NI} is driven by the residual stress level

in the film. In addition, K_{res}, which is a correction to consider the pre-stressed state of the film, is more influential in the calculation of the final value K_{NI} than the apparent fracture resistance K_{app}. The significance of such measurement, which is not intrinsic to the material, can be questioned and compared with Brillet's results, showing that K_{NI} depends on the film thickness, even if the residual stress of each film was similar [10]. Given this limitation, the fact that K_{NI} increases slightly with the process-like thermal treatments would be in agreement with a densification and thus increased crack resistance.

III.4 Effect of temperature cycling

As mentioned in chapter I, the temperature cycling from -50°C to 150°C is an accelerated aging test used in microelectronic industry to evaluate product long-term reliability [1]. In this section, we study the influence of this aging test on mechanical properties for all dielectric materials up to 1000 cycles. For that purpose, we characterized the film residual stress, reduced modulus and hardness after 500 and 1000 cycles for each specimen.

III.4.1 Results

III.4.1.1 Film residual stress

Table III.11 summarizes the residual stress results at TC_{500} (*i.e.* 500 thermal cycles) and TC_{1000} (*i.e.* 1000 thermal cycles) together with the evolution with respect to the reference states (*i.e.* T_0 for SiN_xH_y and SiO_2:H and T_{0b} for SiOC:H and pSiOC:H). To remind, SiN_xH_y and SiO_2:H were not submitted to the process thermal treatment because they are deposited at the top of the interconnect stack. For the SiN_xH_y and SiO_2:H, there is no measurement available at TC_{500} as the equipment was down during this period.

Table III.11: *Evolution of residual stresses with respect to reference states T_0 and T_{0b} after thermal cycling (TC_{500} and TC_{1000}) for all studied dielectrics*

σ_{res} (MPa)	SiN_xH_y	SiO_2:H	SiOC:H	pSiOC:H	pSiOC:H
t_f *(nm)*	*616*	*596*	*569*	*219*	*742*
T_0	-379 ± 8	-193 ± 8	49 ± 8	52 ± 23	59 ± 6
T_{0b}	-	-	86 ± 8	104 ± 23	72 ± 6
TC_{500}	x	x	108 ± 8	101 ± 23	75 ± 6
var/T_0 (or T_{0b})	x	x	+26%	-3%	+4%
TC_{1000}	-330 ± 8	-173 ± 8	134 ± 8	34 ± 23	29 ± 6
var/T_0 (or T_{0b})	-13%	-10%	+56%	-67%	-60%

At TC_{1000}, the residual stresses of both SiN_xH_y and SiO_2:H are less compressive than at the reference state (-10%). However, this evolution is low compared to those observed for the SiOC:H films. For the 569 nm-thick SiOC:H, a large increase in residual tensile

stress is measured at TC_{500} and then at TC_{1000} (+56%). For the two pSiOC:H films, the residual tensile stress remains quite stable from T_{0b} to TC_{500}, and then drastically drop (-60%).

III.4.1.2 Reduced modulus and hardness

Reduced modulus and hardness were measured at TC_{500} and TC_{1000}. Figure III.15 shows the evolution of the relative variation with respect to the reference states for the two parameters after temperature cycling for all films.

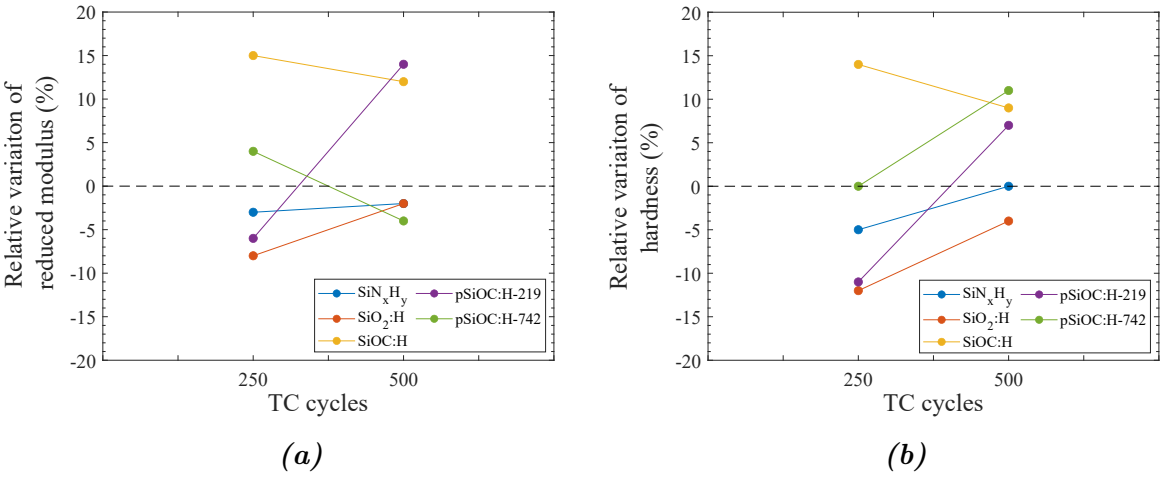


Figure III.15: *Relative variation of (a) reduced modulus and (b) hardness with respect to the reference states (T_0 and T_{0b}) during temperature cycling for all dielectric films*

The reduced modulus and hardness variations are less than 5% for SiN_xH_y, so this material can be considered as stable with temperature cycling. SiO_2:H shows more variations for the two properties. However, the decrease in both reduced modulus and hardness observed at TC_{500} can be questioned, as at TC_{1000} we find almost the T_0 values. SiOC:H is more sensitive to temperature cycling with respect to T_{0b}. Its reduced modulus and hardness increase at TC_{500} and the parameters seem almost stabilized at TC_{1000}. A different trend is observed for the 219 nm-thick pSiOC:H. The reduced modulus is slightly decreased at TC_{500}, while TC_{1000} has a greater impact. Hardness variations are less marked at TC_{1000} even if a slight increase with respect to T_{0b} is measured. However, less variation is observable for the reduced modulus and hardness of the 742 nm-thick pSiOC:H, even if its residual stress show the same trend. The results are respectively summarized in tables III.12 and III.13 and compared to the reference states.

Table III.12: *Evolution of reduced modulus with respect to reference states T_0 and T_{0b} after thermal cycling (TC_{500} and TC_{1000}) for all studied dielectrics*

E_r (MPa)	**SiN_xH_y**	**SiO_2:H**	**SiOC:H**	**pSiOC:H**	**pSiOC:H**
t_f *(nm)*	*616*	*596*	*569*	*219*	*742*
T_0	160 ± 5	71 ± 3	10.9 ± 0.2	10.3 ± 0.4	7.4 ± 0.2
T_{0b}	-	-	11.4 ± 0.2	10.9 ± 0.8	7.4 ± 0.1
TC_{500}	155 ± 5	66 ± 3	13.1 ± 0.6	10.2 ± 0.8	7.7 ± 0.2
var/T_0 (or T_{0b})	-3%	-8%	+15%	-6%	+4%
TC_{1000}	156 ± 6	70 ± 3	12.8 ± 0.4	12.4 ± 0.5	7.1 ± 0.1
var/T_0 (T_{0b})	-2%	-2%	+12%	+14%	-4%

Table III.13: *Evolution of hardness with respect to reference states T_0 and T_{0b} after thermal cycling (TC_{500} and TC_{1000}) for all studied dielectrics*

H (MPa)	**SiN_xH_y**	**SiO_2:H**	**SiOC:H**	**pSiOC:H**	**pSiOC:H**
t_f *(nm)*	*616*	*596*	*569*	*219*	*742*
T_0	20 ± 1	9.4 ± 0.4	1.9 ± 0.1	1.7 ± 0.1	1.2 ± 0.1
T_{0b}	-	-	2.0 ± 0.1	1.7 ± 0.1	1.2 ± 0.1
TC_{500}	19 ± 1	8.3 ± 0.4	2.2 ± 0.1	1.5 ± 0.2	1.2 ± 0.1
var/T_0 (or T_{0b})	-5%	-12%	+14%	-11%	0%
TC_{1000}	20 ± 1	9.0 ± 0.4	2.1 ± 0.1	1.8 ± 0.1	1.3 ± 0.1
var/T_0 (or T_{0b})	0%	-4%	+9%	+7%	+11%

III.4.1.3 Fracture resistance

The fracture resistance evolution with temperature cycling was also investigated for the 742 nm-thick pSiOC:H using cube-corner indentation. The $c^{3/2}$ *versus* P_{max} plot is shown in figure III.16 for the cycled states in comparison with T_{0b}.

The crack lengths measured after temperature cycling are globally smaller at TC states as compared to T_{0b}. From T_{0b} to TC_{1000}, K_{app} shows a non-monotonous evolution. Indeed, the value has increased of 21% at TC_{500}, whereas the value is almost similar to T_{0b} again at TC_{1000}. This trend is consistent with the variation of crack length *c*. However, K_{res} shows a different evolution which can be correlated with the variation of the residual stress (table III.11).

The final value of K_{NI} is mainly driven by K_{res} again, with a constant value from T_{0b} to TC_{500} and a final decrease at TC_{1000}.

Table III.14: *Evolution of fracture resistance parameters with respect to T_{0b} after temperature cycling (TC_{500} and TC_{1000}) for the 742 nm-thick pSiOC:H*

pSiOC:H	K_{app} **MPa**$\sqrt{m}$	K_{res} **MPa**$\sqrt{m}$	K_{NI} **MPa**$\sqrt{m}$
T_{0b}	0.028 ± 0.001	0.093 ± 0.002	0.12 ± 0.02
TC_{500}	0.034 ± 0.002	0.089 ± 0.008	0.12 ± 0.02
var/T_{0b}	+21%	-4%	-
T1000	0.027 ± 0.002	0.035 ± 0.007	0.06 ± 0.02
var/T_{0b}	-4%	-62%	-50%

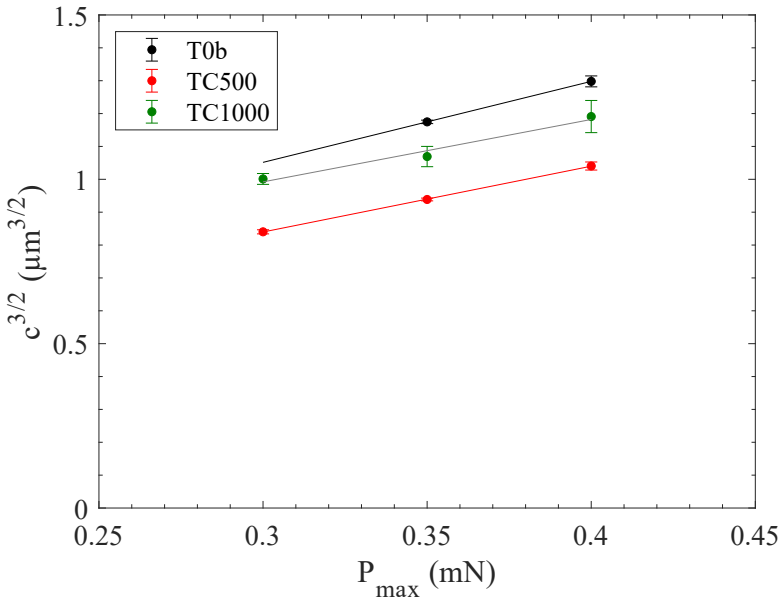


Figure III.16: *Average crack length raised to power 3/2 as a function of maximal applied load during cube-corner nanoindentation of the 742 nm pSiOC:H after process thermal treatment (T_{0b}) and temperature cycling (TC_{500} and TC_{1000})*

III.4.2 Discussion

The residual stress (and, in turns, the fracture resistance parameter) of the films seems to be the most sensitive parameter to thermal cycling. The compressive residual stress slightly decreases (-10%) for both SiN_xH_y and SiO_2:H after temperature cycling. On the contrary, the tensile residual stress significantly increases (two times larger) for the 569 nm-thick SiOC:H film. The two pSiOC:H behave differently than the SiOC:H. Indeed, their residual stresses remain almost constant at TC_{500} as compared to T_{0b}, whereas the values drop at TC_{1000}.

The stability of the properties (residual stress, reduced modulus and hardness) for both SiN_xH_y and SiO_2:H agrees with the literature where several studies observed irreversible

modifications for similar films at much higher temperature, at least close to the deposition one (*i.e.*, 400°C). In such cases, the residual stress evolution is irreversible and attributed to hydrogen desorption, resulting in film densification [17, 60]. We can conclude that the mechanical properties of the SiN_xH_y and SiO_2:H films are stable with temperature cycling.

Concerning the 569 nm-thick SiOC:H and the 219 nm-thick pSiOC:H, the evolution is not direct. Indeed, the reduced modulus is increased for both films, but not for the 742 nm-thick pSiOC:H layer. The residual stress parameter is more sensitive and consequently the fracture resistance as well. However, the trends are not monotonous. To better understand the mechanisms, FTIR analyses were performed on the 569 nm-thick SiOC:H (figure III.17) and 219 nm-thick pSiOC:H (figures III.18) films to compare TC_{1000} from T_{0b}.

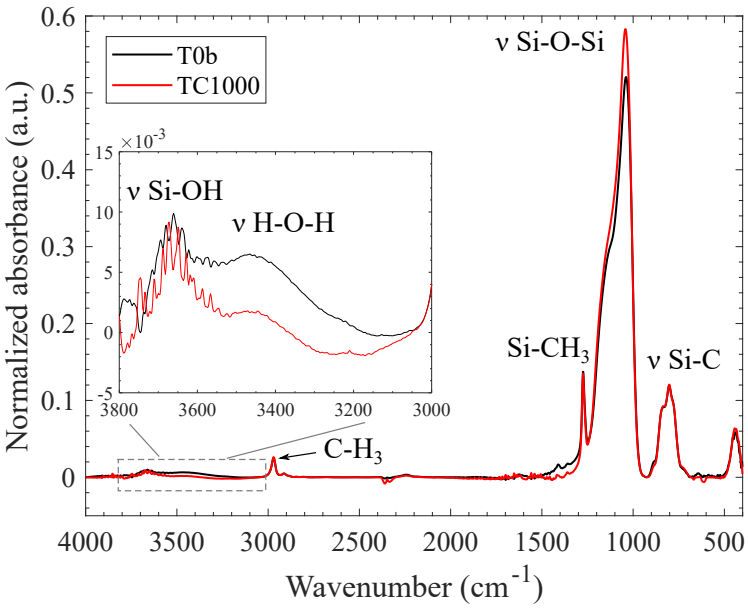


Figure III.17: *FTIR spectrum for the 569 nm-thick SiOC:H after process thermal treatment (T_{0b}) and after 1000 temperature cycles (TC_{1000})*

Two changes are observable between 400 cm^{-1} and 4000 cm^{-1} for the SiOC:H comparing T_{0b} and TC_{1000}. First, the water contribution ν H-O-H is reduced with temperature cycling (weakly bonded H_20). We could note that the band ν Si-OH height (strongly bonded H_2O) at 3661 cm^{-1} is less affected by temperature cycling. A higher temperature is required to break these bonds [49]. In addition, we note an increase in Si-O-Si band height at 1040 cm^{-1} after cycling (+12%). The FTIR spectrum show a slightly reorganized chemical structure with less H-O-H and more Si-O-Si bonds. We suppose a densification mechanism of the film, which is illustrated by an increased residual tensile stress as well as reduced modulus and hardness.

For the 219 nm-thick pSiOC:H, no change in water-related bonds can be observed on FTIR spectra, as their contribution is insufficient; only a slight increase in Si-O-Si stretching band can be detected (+4%) with a less marked shoulder at 1130 cm^{-1}, which supposes a slight Si network rearrangement [123].

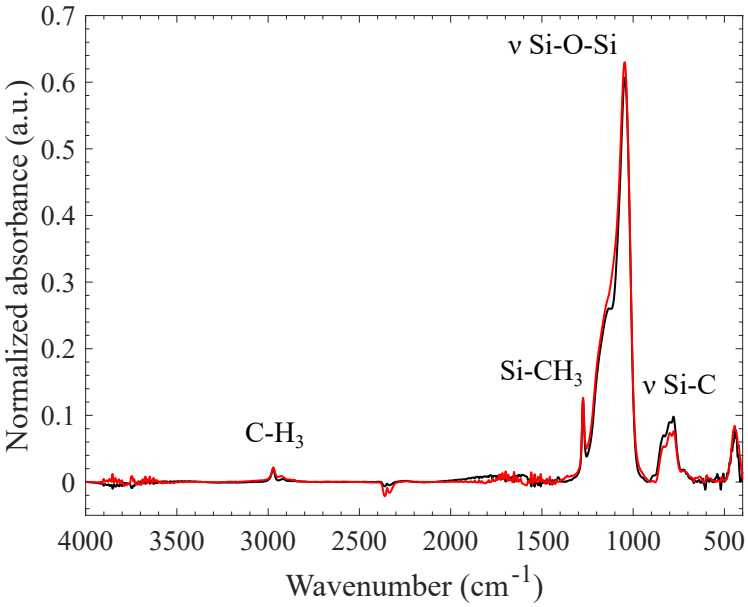


Figure III.18: *FTIR spectrum for the 219 nm-thick pSiOC:H after process thermal treatment (T_{0b}) and after 1000 temperature cycles (TC_{1000})*

Comparing the 219 nm and 742 nm-thick pSiOC:H films, the evolution of their residual stresses with thermal cycling shows similar tendencies: an almost identical value between T_{0b} and TC_{500}, whereas the value is decreased at TC_{1000}. However, their reduced modulus and hardness values do not show the same sensitivity to temperature cycling. Two root-causes can be assumed: first, the structural modification does not occur through the entire film thickness and is mainly near the film surface. As global properties are measured through nanoindentation, the thinnest film appears to be the most sensitive to temperature cycling. The infrared rays penetrating the entire film thickness, the FTIR cannot illustrate this. Second, for the 219 nm-thick SiOC:H, the nanoindentation characterization can be less accurate at these very small penetration depths because of a less accurate tip calibration, a surface roughness degradation with aging as well as a potential surface contamination caused by the environmental chamber.

We conclude that all variations noted during the temperature cycling are limited when compared to the intrinsic differences between the dielectrics, as illustrated by the reduced modulus and hardness (<15% for all studied dielectrics). There is no dramatic collapse and the mechanical properties remain on the same order of magnitude. Anyway, the possible impact of these variations is discussed in more details in chapter V. On the other side, the fracture parameters of the pSiOC:H are more affected. This is mainly related to the residual stress, which seems to be a more sensitive parameter to control the impact

of temperature cycling on such materials deposited on Si wafer substrates.

III.5 Effect of temperature-humidity storage

Water absorption may occur during the process steps or during the product lifetime if a diffusion path from the exterior exists in the interconnect part. Note that this state would therefore be induced by another problem elsewhere in the product (*e.g.* crack at the die edge). Materials are not and should not be in this condition during normal operation. This section aims to evaluate if humidity can affect the dielectric mechanical properties. As we target long-term modifications, the samples were stored in a temperature-humidity storage chamber over 1000 hours after the temperature cycling. Residual stress, reduced modulus, hardness and fracture resistance were measured at 250, 500 and 1000 hours, hereafter labeled THS_{250}, THS_{500} and THS_{1000}. The environmental conditions were set to 85°C and 85% RH.

III.5.1 Results

III.5.1.1 Film residual stress

The variations of film residual stress with humid aging are reported in table III.15 with respect to the last aged state TC_{1000}.

Table III.15: *Evolution of residual stresses with respect to reference states T_0 and T_{0b} and to the last cycled state (TC_{1000}) after temperature-humidity storage (THS_{250}, THS_{500} and THS_{1000}) for all studied dielectrics*

σ_{res} (MPa)	SiN_xH_y	SiO_2:H	SiOC:H	pSiOC:H	pSiOC:H
t_f (nm)	*616*	*596*	*569*	*219*	*742*
TC_{1000}	-330 ± 8	-173 ± 8	134 ± 8	34 ± 23	29 ± 6
THS_{250}	-331 ± 8	-221 ± 8	73 ± 8	56 ± 23	60 ± 6
var/TC_{1000}	< 1%	+28%	-46%	+65%	+107%
THS_{500}	-333 ± 8	-216 ± 8	75 ± 8	64 ± 23	65 ± 6
var/TC_{1000}	< 1%	+25%	-44%	+88%	+124%
THS_{1000}	-324 ± 8	-230 ± 8	85 ± 8	83 ± 23	65 ± 6
var/TC_{1000}	-2%	+33%	-37%	+144%	+124%

SiN_xH_y residual stress remains quite stable during THS with a variation within 2% from TC_{1000}. This film is the most stable under thermal and hydrothermal cycling. SiO_2:H is slightly more compressive after THS. The larger variation happens at THS_{250}, where the residual compressive stress increases by 28%, while the difference between all THS states is within 4%. The residual stress of the 569 nm-thick SiOC:H film largely decreases with THS from TC_{1000} showing a significant effect of humid aging on this material. An opposite

trend is observed for the two pSiOC:H, for which the residual stresses significantly increase during THS with respect to the low values measured at TC_{1000}. We note the evolution is the same for the two pSiOC:H films whatever the thickness.

III.5.1.2 Reduced modulus and hardness

We monitor the film reduced modulus and hardness at 250, 500 and 1000 hours of humid aging. Figure III.19 presents the relative variation of the reduced modulus and the hardness with respect to the reference states for both temperature cycling and temperature-humidity storage. Table III.16 summarizes the results for reduced modulus and table III.17 for the hardness. In the tables, the variations are provided with respect to TC_{1000} which is the last cycled state before THS.

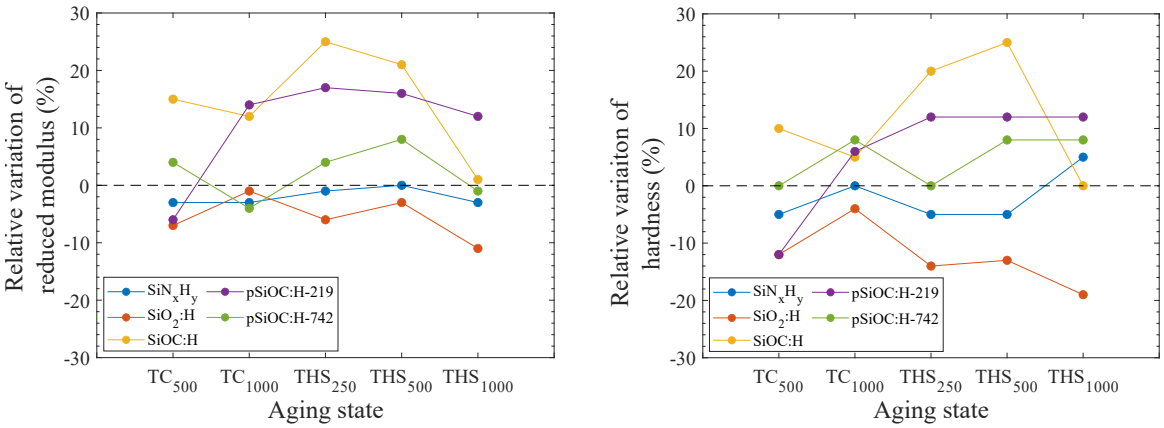


Figure III.19: *Relative variation of (a) reduced modulus and (b) hardness with respect to the reference states (T_0 and T_{0b}) during humid storage (in complement to temperature cycling) for all dielectric films*

For SiN_xH_y, both reduced modulus and hardness remain almost constant during temperature-humidity storage. Only a slight increase in hardness at THS_{1000} is noted, but it is considered as insignificant regarding the other properties and aging states. The silicon nitride films seem very stable and not affected by thermal or water aging problems.

For SiO_2:H, we note a slight, but significant decrease in both reduced modulus (-10%) and hardness (-15%) during temperature-humidity storage with respect to TC_{1000}.

The SiOC:H properties are slightly increased at THS_{250} and THS_{500} as compared to TC_{1000}. Then, a larger decrease is observed at THS_{1000}.

Concerning the 219 nm-thick pSiOC:H, its properties remain remarkably stable during THS, varying of less than 6 % from TC_{1000}. The 742 nm-thick pSiOC:H is also relatively stable during THS.

Table III.16: *Evolution of reduced modulus with respect to the last cycled state TC_{1000} after temperature-humidity storage for all studied dielectrics*

E_r (MPa)	**SiN_xH_y**	**SiO_2:H**	**SiOC:H**	**pSiOC:H**	**pSiOC:H**
t_f (nm)	*616*	*596*	*569*	*219*	*742*
TC_{1000}	156 ± 6	70 ± 3	12.8 ± 0.4	12.4 ± 0.5	7.1 ± 0.1
THS_{250}	158 ± 6	67 ± 5	14.3 ± 0.9	12.7 ± 1.0	7.7 ± 0.3
var/TC_{1000}	< 1%	-4%	+12%	+2%	+8%
THS_{500}	160 ± 5	69 ± 4	13.8 ± 1.5	12.6 ± 1.2	8.0 ± 0.2
var/TC_{1000}	+2%	< 1%	+8%	+1%	+13%
THS_{1000}	155 ± 4	63 ± 3	11.5 ± 0.4	12.2 ± 0.5	7.3 ± 0.1
var/TC_{1000}	< 1%	-10%	-10%	-1%	+3%

Table III.17: *Evolution of hardness with respect to the last cycled state TC_{1000} after temperature-humidity storage for all studied dielectrics*

H (MPa)	**SiN_xH_y**	**SiO_2:H**	**SiOC:H**	**pSiOC:H**	**pSiOC:H**
t_f (nm)	*616*	*596*	*569*	*219*	*742*
TC_{1000}	20 ± 1	9.0 ± 0.4	2.1 ± 0.1	1.8 ± 0.1	1.3± 0.1
THS_{250}	19 ± 1	8.1 ± 0.6	2.4 ± 0.2	1.9 ± 0.1	1.2 ± 0.1
var/TC_{1000}	-5%	-10%	+14%	+5%	-4%
THS_{500}	19 ± 1	8.2 ± 0.6	2.5 ± 0.1	1.9 ± 0.2	1.3 ± 0.1
var/TC_{1000}	-5%	-9%	+15%	+5%	0%
THS_{1000}	21 ± 1	7.6 ± 0.3	2.0 ± 0.1	1.9 ± 0.1	1.3 ± 0.1
var/TC_{1000}	+7%	-15%	-8%	+5%	0%

III.5.1.3 Fracture resistance

The evolution of the fracture resistance with THS of the 742 nm-thick pSiOC:H is also investigated through cube-corner indentation. Figure III.20 gives the $c^{3/2}$ *versus* P_{max} curve for the THS states together with T_{0b} and TC_{1000} for comparison.

The crack lengths measured after THS are shorter as compared to TC_{1000} results. Consequently, K_{app} is increased from TC_{1000} to THS_{250}. K_{res} follows the same trend as the residual stress evolution with the larger variation from TC_{1000} to THS_{250}. Finally, K_{NI} increases with THS.

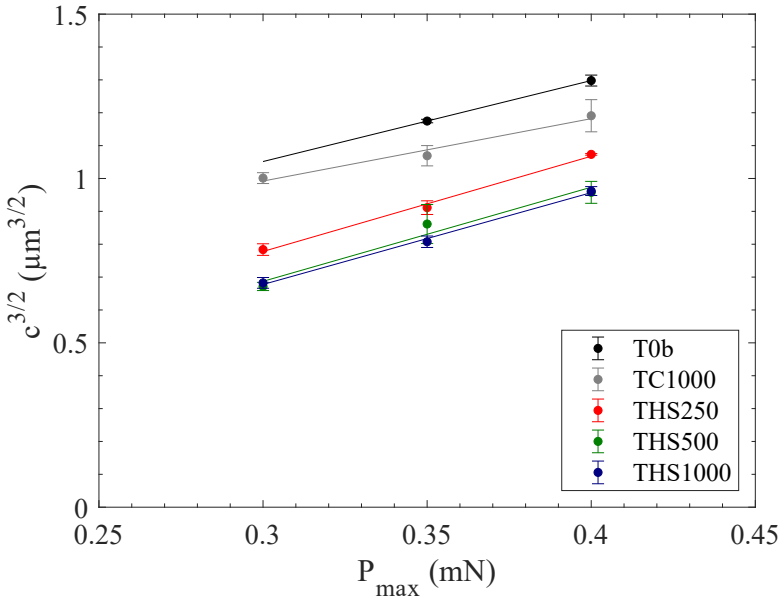


Figure III.20: *Average crack length raised to power 3/2 as a function of maximal applied load during cube-corner nanoindentation for the 742 nm pSiOC:H for the reference state (T_{0b}), at the end of the temperature cycling (TC_{1000}) and during temperature-humidity storage (THS_{250}, THS_{500} and THS_{1000})*

Table III.18: *Evolution of fracture resistance parameters with respect to the last cycled state TC_{1000} after temperature-humidity storage for the 742 nm-thick pSiOC:H*

pSiOC:H	K_{app} **MPa**$\sqrt{m}$	K_{res} **MPa**$\sqrt{m}$	K_{NI} **MPa**$\sqrt{m}$
TC_{1000}	0.027 ± 0.002	0.035 ± 0.007	0.06 ± 0.02
THS_{250}	0.034 ± 0.003	0.068 ± 0.007	0.10 ± 0.02
var/TC_{1000}	+26%	+94%	+65%
THS_{500}	0.036 ± 0.003	0.073 ± 0.007	0.11 ± 0.02
var/TC_{1000}	+33%	+109%	+76%
THS_{1000}	0.037 ± 0.002	0.072 ± 0.008	0.11 ± 0.02
var/TC_{1000}	+37%	+106%	+76%

III.5.2 Discussion

SiN_xH_y

The residual stress of SiN_xH_y shows almost no variation during THS (less than 2% with respect to TC_{1000}) and the same observation is confirmed for the reduced modulus and the hardness. The SiN_xH_y passivation film is an efficient stable barrier against humidity.

SiO_2:H

In contrast, SiO_2:H becomes more compressive during THS and its reduced modulus and

hardness decrease along with THS time.

When exposing a SiO_2 film to humidity, it may absorb water present in the surrounding environment, forming new Si-OH bonds by breaking Si-O-Si bonds. This bond breaking leads to a more compressive residual stress [9]. Indeed, the new incorporated OH groups would occupy a larger volume than the one of a single oxygen linked to two silicon atoms. Thus, the film dilatation may explain the variation of residual stress. In addition, the introduction of OH groups to the Si network may cause the formation of structural porosity (figure III.21). The variation of the film porosity rate would be responsible of lower mechanical properties. For example, measurements on longitudinal sound velocities, which can be related to the specimen Young's modulus, in silica with different water content were reported by Fraser and Le Parc *et al.* [40, 118]. They show that the longitudinal sound velocities decrease upon an increase in OH content, traducing a decrease in reduced modulus.

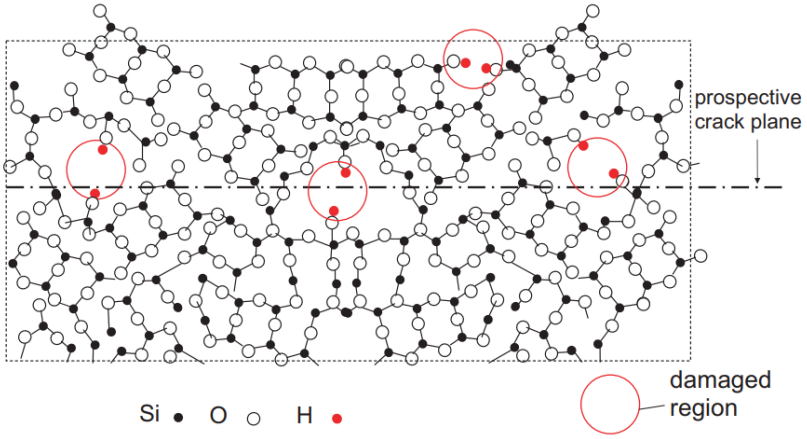


Figure III.21: *Volume element of silica showing damage by bond breaking due to the water/silica reaction, third dimension ignored (from [33])*

However, the variations of reduced modulus and hardness remain limited for the highly compressive SiO_2:H studied here. Indeed, for a material of same nature, different deposition conditions can be used and generates films with different residual stresses. In an additional series of tests, we compared two SiO_2:H with different residual stresses: the SiO_2-STR previously studied and a SiO_2-STD, another undoped silicate glass of same thickness used at STMicroelectronics. The SiO_2-STD has a residual stress of -60 MPa at T_0. This sample was directly exposed to 1000 hours of THS (without previous thermal cycling). We observe larger variations in residual stress, reduced modulus and hardness for the SiO_2-STD as compared to the SiO_2-STR (table III.19). Its residual compressive stress has increased of more than twice its initial value and both the reduced modulus and hardness have decreased of respectively 21% and 36%. The difference between the two films relies in the precursor flows which lead to a less compressive film (-193 MPa to -60 MPa).

The mass was also measured and FTIR anaysis was performed on the SiO_2-STD. The

Table III.19: *Evolution of residual stress, reduced modulus and hardness at* THS_{1000} *with respect to* T_0 *for two undoped* SiO_2*:H films with different as-deposited residual stresses. Note that for the* SiO_2*-STD, no previous temperature cycling was performed.*

Material	Aging state	Stress (MPa)	E_r (GPa)	H (GPa)
SiO_2-STR	T_0	-193 ± 8	71 ± 3	9.4 ± 0.4
	THS_{1000}	-230 ± 8	63 ± 3	7.6 ± 0.3
	var/T_0	-19%	-11%	-19%
SiO_2-STD	T_0	-60 ± 1	66 ± 2	8.3 ± 0.3
	THS_{1000}	-173 ± 1	52 ± 2	5.3 ± 0.2
	var/T_0	-188%	-21%	-36%

results show that the film mass uptake is about 6% after THS. In addition, the FTIR spectra presented in figure III.22 shows that the water-related bonds (Si-OH and H-O-H) band heights significantly increase after THS as well as Si-O-Si contributions.

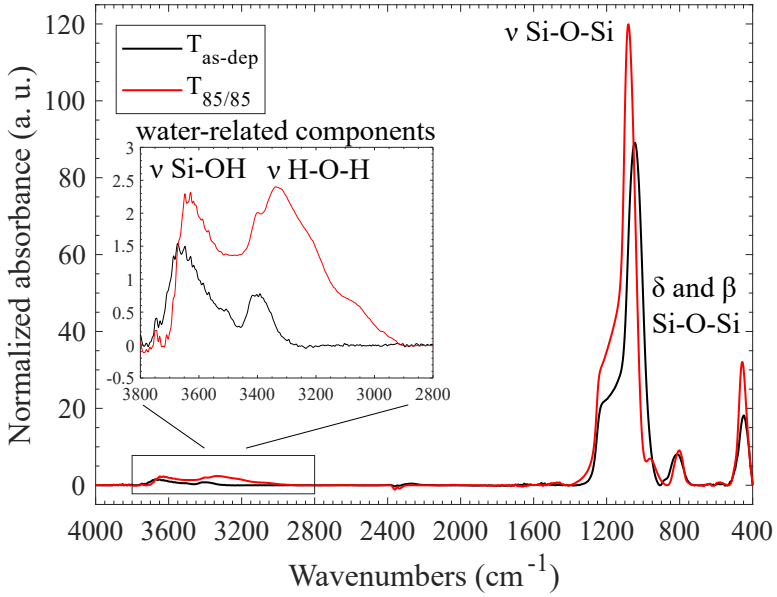


Figure III.22: *FTIR spectra for* SiO_2*-STD as deposited and after 1000 hours under 85°C and 85% RH aging*

Two simultaneous reactions can explain both increases in Si-OH and Si-O-Si contributions. Equation (III.5) describes the absoprtion of water into the Si network by breaking the Si-O-Si bonds to form new Si-OH and is well described for plain glass [33]. Equation (III.6) describes the recombination of Si dangling bonds present in PECVD SiO_2 materials to form ionic bonds Si-O-Si as attested by the FTIR results (figure III.22). However, as the mechanical properties (both reduced modulus and hardness) have decreased after THS, the mechanism described by equation (III.5) seems to be predominant.

$$Si - O - Si + H_20 \rightarrow 2SiOH \tag{III.5}$$

$$2Si^{\cdot} + H_2O \rightarrow Si - O - Si + H_2 \tag{III.6}$$

SiOC:H

Concerning the SiOC:H film, its tensile residual stress first decreases at THS_{250} as compared to TC_{1000}, and then increases more slowly at THS_{500} and THS_{1000}. Its reduced modulus and hardness follow the opposite trend with a value increased at THS_{250}, and then decreased at THS_{500} and THS_{1000}.

Guo *et al.* show an increase in reduced modulus (+ 8%) and hardness (+ 17%) after annealing at 400 °C previously humidified SiOC:H films [49]. The variations of the properties are attributed to a desorption of two water components: the α-bonded and β-bonded water. The difference is that the β-bonded water is tightly hydrogen-bonded to two neighboring hydroxyl groups, while the α-bonded water is loosely bonded to each other and to surface hydroxyl groups. In our case, the properties are decreasing with an increased THS time, which agrees with Guo *et al.* results. However, the significant increase in both reduced modulus and hardness from TC_{1000} to THS_{250} remains difficult to explain.

pSiOC:H

In contrast, the pSiOC:H properties are remarkably stable regarding the reduced modulus and hardness. This is not the case for the residual stress, and consequently for the fracture resistance parameter K_{NI}.

To simplify the analysis, a parallel study with different parameters (mass evolution, residual stress measurement and nanoindentation (E_r and H)) on a simpler sample was performed. The sample is a 350 nm-thick core layer with neither capping nor initiation layer, see chapter II. This sample was used to reduce the variability linked to the film thickness and sub-layers heterogeneity. Results show a mass uptake of 8.6% of the film mass after 1000 hours of THS under the same aging conditions (85°C and 85% RH). Neither previous process thermal treatment nor thermal cycling was performed before THS. The measurements show that neither the residual stress (10%) nor the mechanical properties (5%) are significantly affected. However, when post-annealing the film at only

125°C, almost all the previously gained mass was lost (80%). This supposes that only free and weakly-bonded H_2O were present after THS [49].

The bulk chemical structure of the porous pSiOC:H can be described with the schematic presented in figure III.23. In such structure, methyl groups (introduced by the porogen and still present at the surfaces of the material after deposition), few silanols bonds, and porosity can be found. Moreover, the core pSiOC:H is known as being hydrophobic due to the presence of methyl groups at the film and pore surfaces. Thus, it is likely that the absorbed moisture is present mainly as water entrapped in pores, with limiting bonding to the Si-O-Si network.

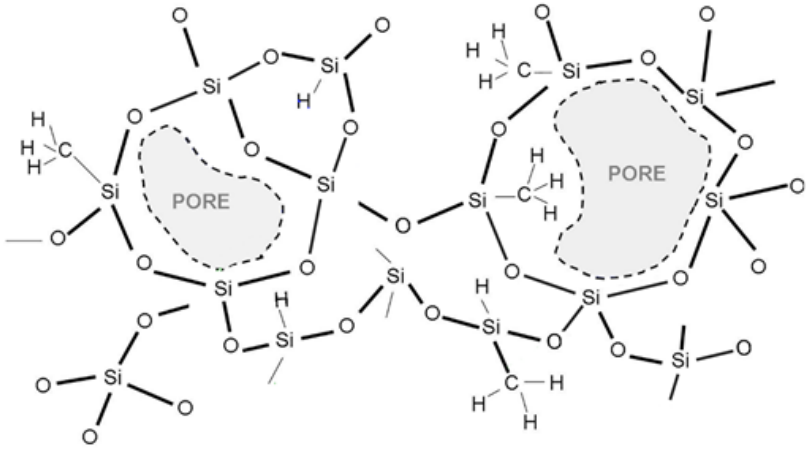


Figure III.23: *Core structure of a porous and carbon-doped silicon oxide. Reproduced from [44]*

Basically, the total absorbed mass of water into 100% of the pores can be roughly estimated with:

$$M_{H_2O} = V_{pores} * \rho_{vol,H_2O} \tag{III.7}$$

where V_{pores} is the volume occupied by the pores (porosity fraction of 17%) and ρ_{vol,H_2O} is the water density.

The calculation gives a mass uptake of 13% of the film mass, which is in the same order of magnitude than the 8.6% actually measured after THS. The difference can be attributed to the assumption simplicity: a saturation of all pores. However, it is likely that some pores may not be accessible and not totally saturated. The potential effect of remaining polar OH groups on water absorption is also not considered.

Hence, the water absorption through the pores of the SiOC:H film is consistent with the almost constant mechanical properties and residual stress (i.e no change in film porosity and volume) as well as with the capacity to desorb at 125°C for the core layer of the pSiOC:H.

The same investigation has to be done with the capping and initiation layer to be able to decorrelate the mechanisms observed for the porous SiOC:H films.

III.6 Conclusion

In this chapter, five dielectric thin films deposited on silicon substrates were exposed to two standard environmental aging tests: a silicon nitride (SiN_xH_y), an undoped silicate glass (SiO_2:H), a carbon-doped silicon oxide (labeled *low-k* SiOC:H) and two porous and carbon-doped silicon oxides (labeled *ultra low-k* pSiOC:H).

Firstly, the mechanical properties were measured for each film after deposition. The reduced moduli were corrected with the Hay-Crawford model to minimize the substrate influence and the hardness was determined at a penetration depth corresponding to 15% of the film thickness. The properties were found in agreement with the literature for similar PECVD-deposited dielectric thin films.

Before the aging tests, all SiOC:H films were exposed to ten cycles from 25°C to 400°C. This thermal treatment was carried out to reproduce the temperature elevations experienced by these materials during the interconnection fabrication.

Then, all the films were exposed to temperature cycling (TC: -50°C to 150°C up to 1000 cycles) and temperature-humidity storage (THS: 85°C and 85% RH up to 1000 hours), aligned with the automotive reliability standards.

Film residual stress, reduced modulus, hardness and fracture toughness were monitored by wafer-curvature and nanoindentation measurements over long test time in order to evaluate the variability of such properties with temperature and humidity.

The main conclusions are:

- The SiN_xH_y, used as passivation layer in the interconnections, appears as an efficient barrier against environmental degradation. Indeed, its properties were found to be stable with temperature cycling and humidity ingress.

- The SiO_2:H showed more variations, especially after temperature-humidity storage where its affinity with humidity was traduced by a decrease in reduced modulus and hardness. In addition, another similar SiO_2 film with a lower residual compressive stress was found to be significantly more sensitive to humidity ingress. The predominant mechanisms highlighted was the formation of OH bonds by breaking Si-O-Si bonds as observed with plain glass samples.

The *low k* and *ultra-low k* dielectric films showed more sensitivity to the aging tests compared to the previous ones, even if the variations remains limited ($< 15\%$):

- The SiOC:H was found to be sensitive to all aging tests performed. This sensitivity seems mainly linked to water absorption and desorption mechanisms.

- The pSiOC:H was also found to be sensitive to all aging tests performed. Studying the core sub-layer of the pSiOC:H, we suppose that the absorbed moisture during the temperature-humidity storage was mainly into the pores regarding the results. We assumed the sacrificial porogen precursor playing a role in the hydrophobic

behavior of the porous SiOC:H film. Indeed, in this film, the degradation of the Si-O-Si network appears limited, while a significant amount of water is absorbed during temperature-humidity storage. The condensation of water into the pores seems promoted for the core sub-layer.

Concerning the fracture resistance of the pSiOC:H film through cube-corner nanoindentation, we showed that the K_{NI} value strongly depends on the correction K_{res}, and thus on the residual stress of the film. Figure III.24 presents the influence of the parameters used in the calculation of K_{NI} regardless to the different aging states. The figure clearly shows that the residual stress is the predominant influential parameter in the determination of the fracture resistance by nanoindentation for the porous SiOC:H.

Globally, we found that the residual stress is the most sensitive mechanical parameter, whereas the conventional mechanical parameters always show slighter variations. Moreover, complementary analyses, FTIR and mass measurements, were found very useful to deeper analyze the involved mechanisms.

All properties constitute an essential database for the finite element simulation of the interconnections and prediction of product reliability, presented in chapter V.

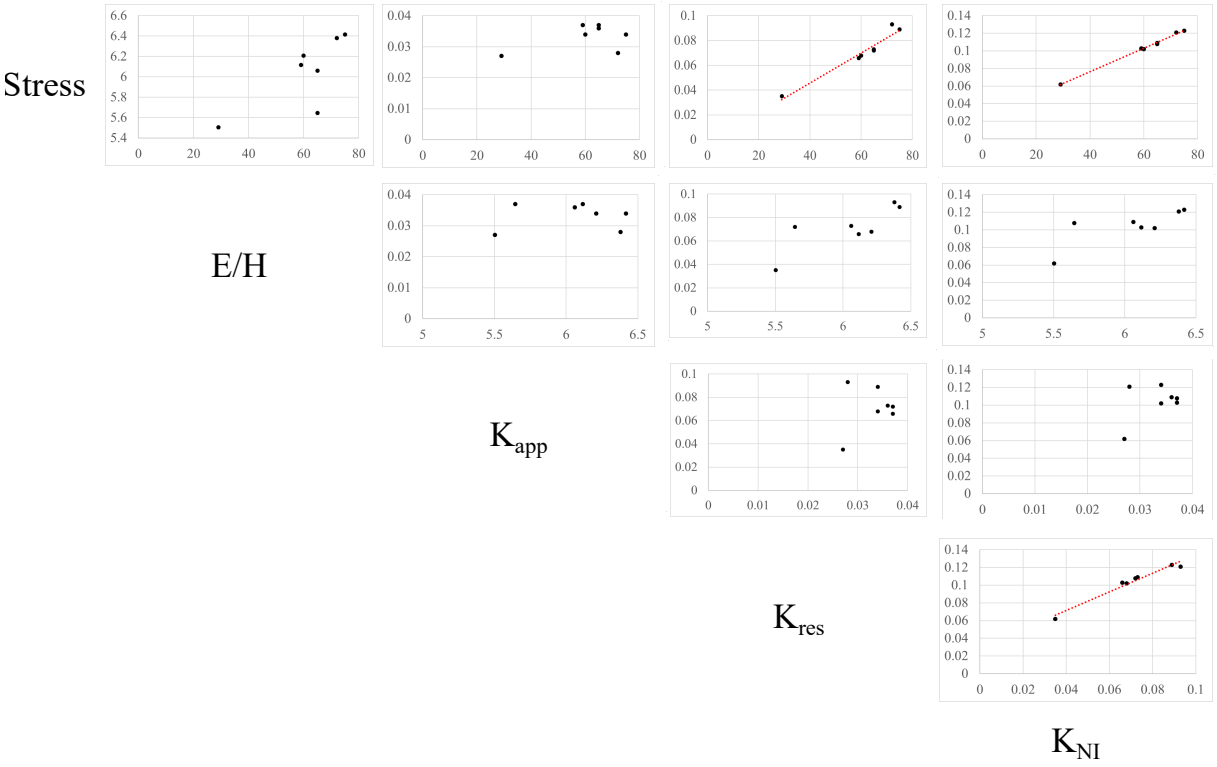


Figure III.24: *Parameter's influence on the calculation of fracture resistance by nanoindentation regardless to aging states*

CHAPTER IV

Characterization of cracking mechanisms in porous SiOC:H

This chapter deals with the cracking mechanisms characterization of the 742 nm-thick porous SiOC:H film.

Studying such material behavior for the *ultra-low k* materials is of particular interest as microelectronic products show interaction issues between the chip and its package. A common mechanical failure observed in service is a crack propagation in this porous SiOC:H layer. Thus, a particular attention is paid to understand cracking mechanisms in such material and highlight any influence of the environment (in particular the humidity level).

The first study in this chapter identifies the properties of the silicon wafer, which supports the porous SiOC:H film, by double-torsion tests coupled with optical imaging for the crack observation. The sample is directly extracted from a wafer by mechanical sawing.

Then, the following section is dedicated to the characterization of the 742 nm-thick porous SiOC:H film through channel cracking experiments carried out in a four-point bending configuration. The influence of humidity level on the observed cracking mechanisms is discussed.

Finally, numerical simulation of the channel cracking test, using a stress-energy coupled criterion, is performed to predict fracture parameters from the results obtained experimentally. This coupled experimental/numerical approach could enable, with further developments, the prediction of cracking in a more realistic and complex structure.

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IV.1 Fracture behavior of silicon wafer substrate by double-torsion testing

In microelectronics, dielectrics are commonly deposited on silicon wafer substrates. Silicon is highly brittle with a low fracture toughness, which depends on the crystallographic orientation. In this study, we investigated the crack resistance of silicon thanks to the double-torsion testing. Samples were extracted from a (100)-oriented wafer by mechanical sawing. Two thicknesses were evaluated: 775 µm and 200 µm. Indeed, most of the products are manufactured with a thinned substrate. The aim is check the feasibility of double-torsion test on an ultra-thin wafer of thickness of 200 µm. Note also that two silicon samples per thickness were measured. The sample preparation and loading procedure are detailed in chapter II. In addition, to facilitate the crack initiation, two close Vickers indentations were aligned to the notch to induce short pre-cracks. Then, a crack was initiated from the notch end and propagated through both indents by slowly loading the specimen.

In situ light microscopy double-torsion experiments were conducted on the micro-machine developed and presented in chapter II under ambient environment. First, tests were carried out to determine the silicon fracture toughness, followed by a study on the potential environmental-assisted slow crack growth for this material.

IV.1.1 Silicon fracture toughness

IV.1.1.1 Load-displacement curves

In situ double-torsion testing was used to estimate silicon fracture toughness under a light microscope (figure IV.1). After crack initiation, the samples were loaded at a high displacement rate until fracture. Figure IV.2 shows the force-displacement curves obtained for two 200 and 775 µm-thick wafers. A displacement rate was applied from 500 µm/min (for the 775 µm-thick wafer) towards 50 µm/min (for the 200 µm-thick wafer) and the loading was stopped (at a fixed displacement) to re-focus on the sample surface. This manipulation, done for the 200 µm-thick samples, generates events on the loading curve corresponding to machine relaxation. In figure IV.2, we observe that the force drops after maximum loading, associated to an unstable crack propagation, leading to the sample complete fracture. We also note that the maximal force is drastically (and logically) reduced for the 200 µm-thick sample. In addition, the slope of the loading curve is steeper for the 775 µm-thick sample as it is more rigid.

IV.1.1.2 Interpretation

The critical loads are measured at 4.4 and 4.9 N for the 775 µm-thick and 0.28 and 0.29 N for the 200 µm-thick samples. K_{IC} is calculated with equation (II.35) at respectively 0.88 ± 0.01 MPa$\sqrt{m}$ and 0.89 ± 0.09 MPa$\sqrt{m}$. These values are consistent and agree

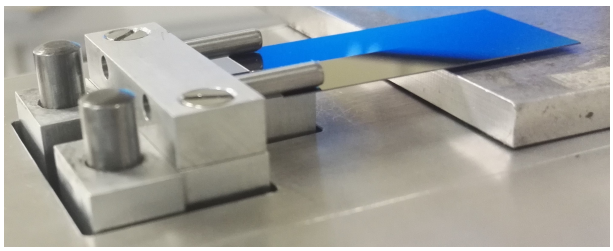


Figure IV.1: *Double-torsion configuration for the 200 µm-thick silicon sample. A centered crack is observable on the tensile face.*

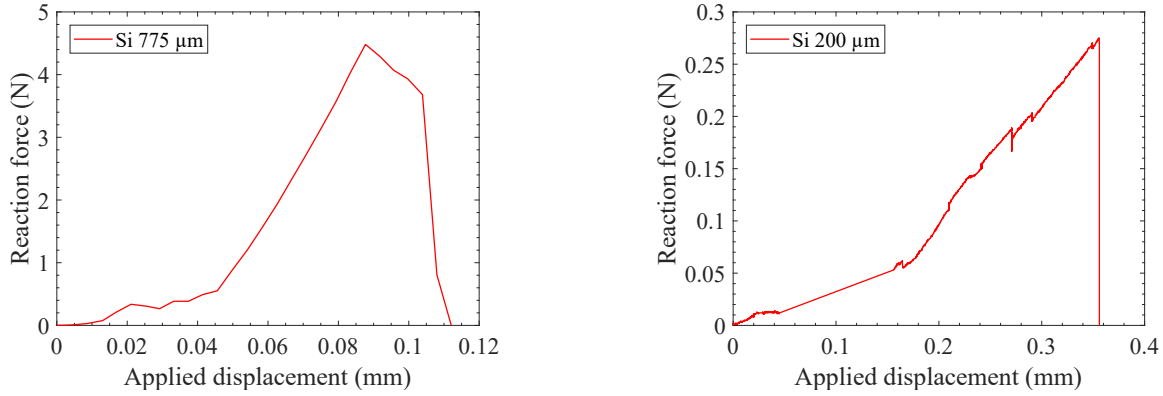


Figure IV.2: *Force-displacement curves of silicon wafer specimens loaded in double-torsion configuration for two thicknesses: (a) 775 µm and (b) 200 µm*

with literature where fracture toughness is reported from 0.65 to 1.23 MPa$\sqrt{\text{m}}$ for (100)-oriented silicon wafers [21, 99].

IV.1.2 Sub-critical fracture tests

Relaxation tests were then carried out to study the sensitivity of the crack growth to ambient environment for the silicon wafer substrates. In this case, the samples were slowly loaded (displacement rate of 20 µm/min) until crack extension, then the displacement was blocked. During the holding time, we monitored the load and crack length through *in situ* light microscopy observation.

Both 775 µm and 200 µm-thick samples show first a fast crack extension at critical load, then no more crack growth is measurable for at least 24 hours during relaxation. The crack extension during the fast fracture is measured at 0.3 mm and at 1.0 mm respectively for the thick and thin wafers.

Considering that crack extension happened during less than 0.1 second, corresponding to the response time of the human eye, the upper crack growth rate bound is about 10^{-3} m/s and 10^{-2} m/s respectively for the thick and thin silicon samples at $K_I \geq 98\%\ K_{IC}$. The lower crack growth rate bound is defined only by the incertitude of the crack length, estimated at 5 µm, as no crack growth was observed. It is about 10^{-11} m/s for both

samples when $K_I < 98\% K_{IC}$. In other words, the crack rate is lower than 10^{-11} m/s as long as $K_I < 98\% K_{IC}$, then immediately reaches over 10^{-3} m/s. This suggests that a water-enhanced slow crack growth does not exist in silicon wafers. These results agree well with literature [16, 39].

IV.2 Fracture behavior of porous SiOC:H thin film by double-torsion

In this section, double-torsion experiments were conducted with the porous SiOC:H thin film deposited on a silicon substrate. Each specimen (*i.e.* substrate thicknesses of 775 µm and 200 µm) was loaded at a displacement rate of 20 µm/min until crack extension, then the displacement was blocked. The load and crack length were then monitored with time.

After a sudden crack extension at maximum load, neither further crack extension nor load relaxation is measured during relaxation. After unloading the sample, a FIB-SEM cross-section of the crack was milled perpendicular to the crack direction. Figure IV.3 shows that the crack propagates in both the pSiOC:H film and the silicon substrate. We conclude that the silicon substrate governs the cracking dynamics due to its larger thickness (ratio about 1/1000), higher stiffness (ratio about 5/100) and low fracture resistance as compared to the SiOC:H film. The crack propagates first in the silicon, then induces the film fracture. The intrinsic fracture behavior of the pSiOC:H itself cannot be characterized through double-torsion tests.

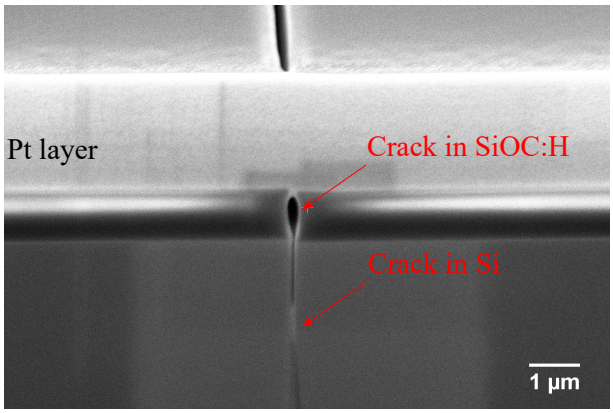


Figure IV.3: *FIB-SEM cross section of the crack initiated through double-torsion within the 742 nm-thick porous SiOC:H deposited on silicon wafer (HV = 5 kV). The Pt layer was deposited to protect the film during the FIB step.*

IV.3 Fracture behavior of porous SiOC:H thin film by four-point bending

Due to the impossibility of inducing crack propagation in the film only with the double-torsion technique, another test was developed to investigate the cracking mechanism in the 742 nm-thick porous SiOC:H film with the following specifications:

- sample and loading configurations which generate cracks only in the porous SiOC:H without fracturing the silicon substrate
- *in situ* test with observation of the tensile face, to observe and monitor the crack growth
- test with controlled, measurable and reproducible crack monitoring

To fulfill the above mentioned specifications, *in situ* SEM four-point bending experiments were performed with a channel cracking sample configuration using the same micromachine as for the double-torsion tests.

IV.3.1 Sample description

To prevent channel cracks from entering the silicon substrate, a 2 µm-thick copper interlayer was deposited on a 400 µm-thick silicon substrate prior to the porous oxide. Indeed, preliminary tests without this layer were unsuccessful with a fracture of the Si substrate before any sign of micro-crack propagation in the film. Introducing the metallic interlayer was already confirmed to be a successful method for generating channel cracks into thin and brittle films deposited on silicon substrates. The metallic interlayer plays as a crack barrier preventing propagation into the substrate [95, 101]. For deposition concerns and similarly to actual products, a thin silicon nitride barrier with a thickness of 60 nm was deposited between the copper and the porous SiOC:H. The silicon substrate was thinned down to a thickness of 400 µm to reduce the critical load during four-point bending tests as the load cell is limited to 100 N. Figure IV.4a schematically illustrates the channel cracking configuration obtained thanks to the Four-Point Bending (FPB) technique.

The specimens, with lateral dimensions of 20x4 mm^2, were taken from wafers by cleavage to limit damages created by mechanical sawing. With this cutting method, the silicon substrate of thickness of 400 µm can sustain tensile stresses by far higher than 1 GPa. The specimens were manually cleaved, so their widths can vary from 3 to 4 mm.

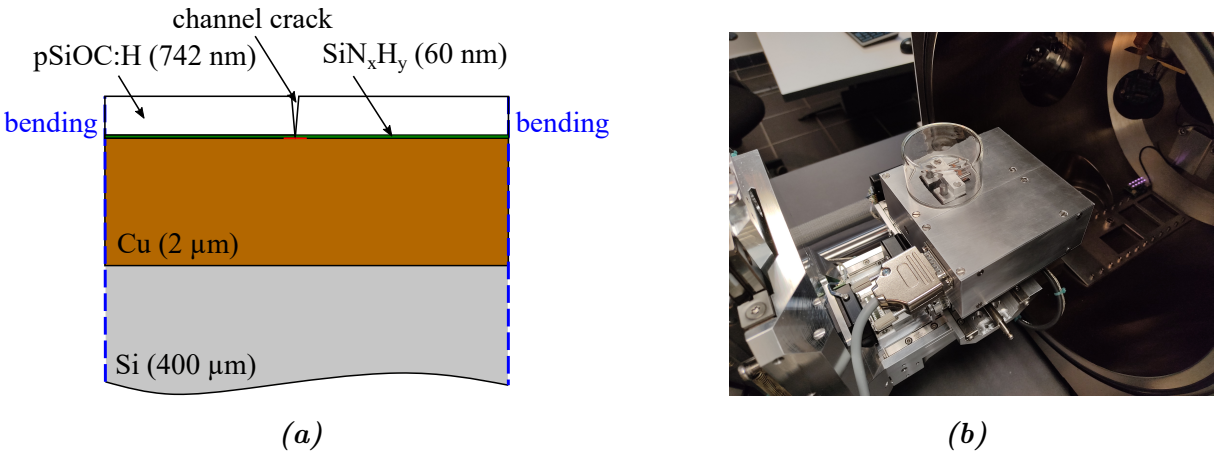


Figure IV.4: *Channel cracking configuration: (a) schematic illustration of a channel crack in a sample comprising 742 nm of pSiOC:H, 60 nm of SiN_xH_y, 2 µm of copper and 400 µm of silicon and (b) actual micromachine mounted on the sample holder of the SEM*

IV.3.2 Fracture characterization

IV.3.2.1 Incremental loading tests

To characterize the cracking mechanism in the porous SiOC:H film, incremental loading tests were carried out. First, the sample was loaded at P_{crit} corresponding to the nucleation of the first cracks in the film. Then, the load was decreased at $P_{img} << P_{crit}$ to image the cracks through SEM. P_{img} was set at 20 N (about 75 MPa in the film), which was considered as sufficiently low to limit any slow crack growth during the imaging time. Then, the sample was loaded by steps of 3 N corresponding to tensile stress steps of 80 MPa in the substrate and 3 MPa in pSiOC:H (equations (II.27) and (II.32)). All the loading increments were performed outside the SEM chamber to prevent random breakage of silicon substrate, which may damage the SEM. The protocol is summarized in figure IV.5.

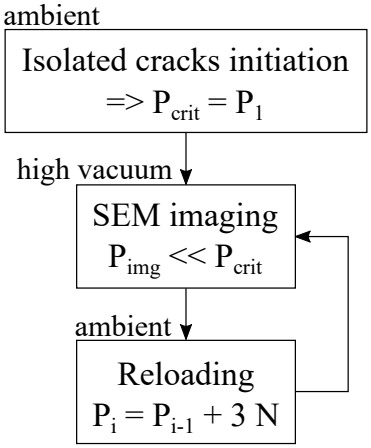


Figure IV.5: *Incremental loading test protocol*

IV.3.2.2 Image analysis

To describe the cracking mechanism in the porous SiOC:H, statistical parameters on the cracks forming within the film were defined: surface crack density, total crack length and averaged crack spacing. These parameters were used to describe the crack network development under different applied stresses and environmental conditions. The surface crack density is defined as the number of cracks per unit area. The length parameter is the total crack length per unit area. The spacing is the average spacing between two cracks, determined through a linear intercept method. In details, lines were drawn, perpendicular to the cracking direction (cracks being all parallel, *i.e.* all perpendicular to the main tensile stress, see figure IV.6), and the intercepts between a line and a crack were numbered. Then, the average spacing was calculated with equation IV.1 assuming no cracks ending at the image edges.

$$S = \frac{L_{line} N_{line}}{N_{intercept} + 1} \tag{IV.1}$$

where L_{line} is the line length, N_{line} the number of lines, $N_{intercept}$ the number of intercepts between a line and a crack. In this study, N_{line} is equal to 30 and L_{line} is equal to 170 µm.

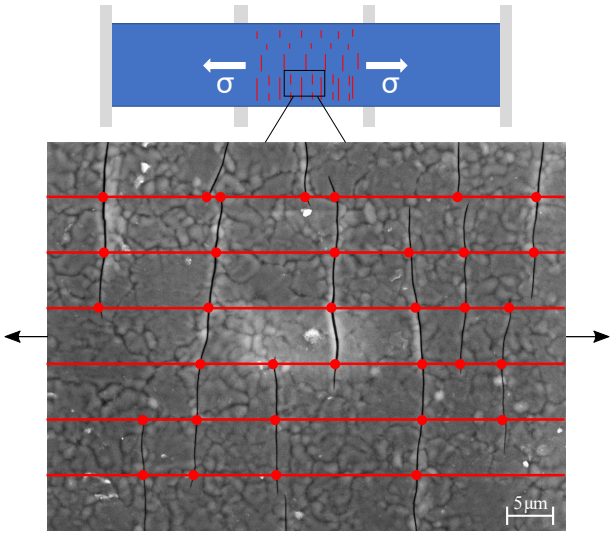


Figure IV.6: *Illustration of the linear intercept method used to estimate the average crack spacing. The red circles show intercepts between lines and cracks.*

IV.3.2.3 Results

Load-displacement curve Figure IV.7 shows the force-displacement curve obtained during an incremental loading test with four specific increments: the first loading, the increment corresponding to the onset of cracking, an intermediate increment and the final one corresponding to sample complete fracture. Neither force drop nor stiffness decrease is observed during the loading, indicating that the film cracking did not affect the sample stiffness. This also supports the fact that the substrate is not cracked until the last increment.

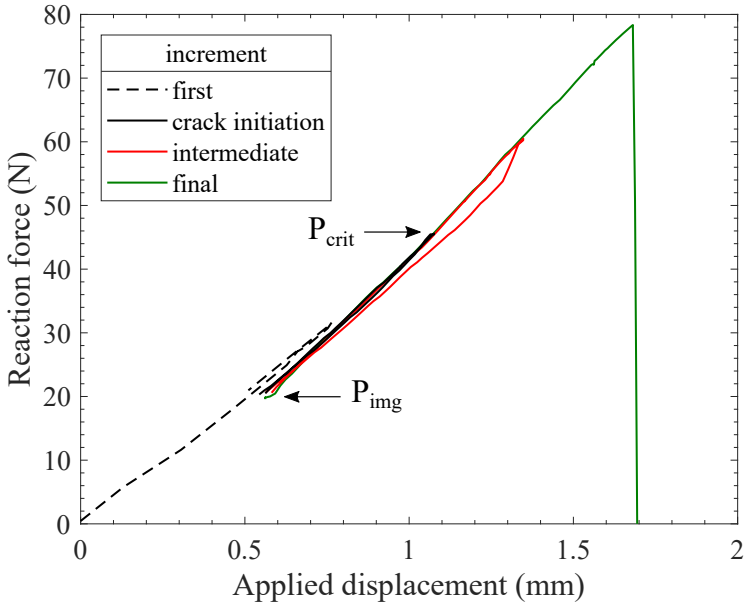


Figure IV.7: *Force-displacement loading-unloading curve during an incremental loading test for four increments: initial, onset of cracking, intermediate and final*

Localization of the cracks As mentioned above, neither force drop nor stiffness decrease is noted on the force-displacement curve, suggesting that the substrate does not crack. To confirm the localization of the cracks in the specimen, a FIB-SEM cross-section of one crack observed during the incremental loading was milled perpendicular to the crack propagation direction (figure IV.8). As seen in the cross-section view, the channel crack cuts across both the silicon oxide and nitride barrier layers and stops at the interface between the silicon nitride and the copper. An interfacial crack is also propagated along the interface between the silicon nitride and the copper near the channel crack.

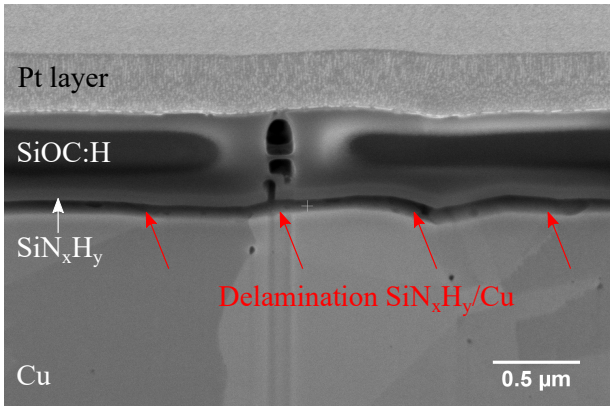
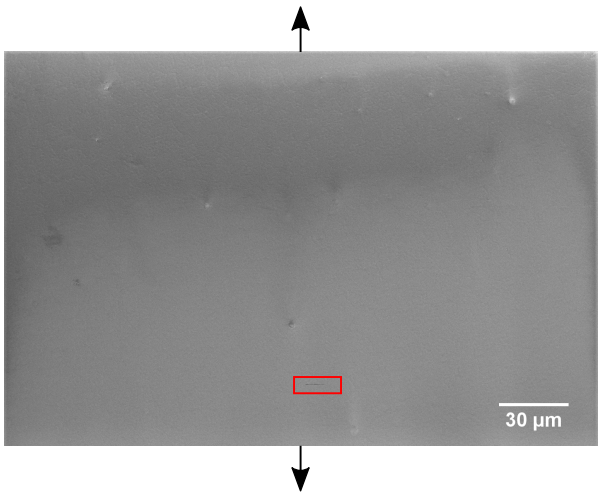


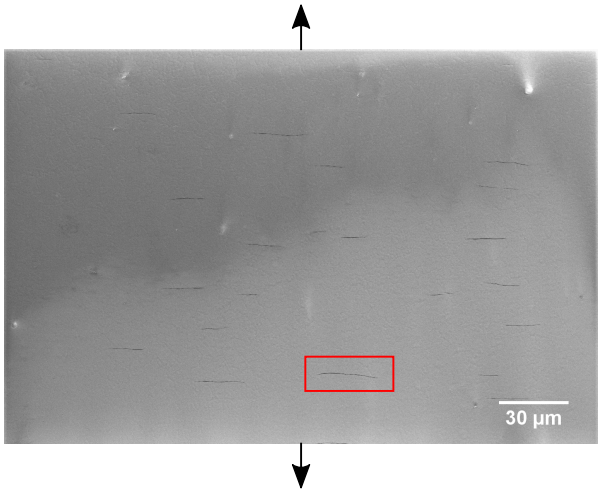
Figure IV.8: *FIB-SEM cross-sectional view of a channel crack cutting across the pSiOC:H and SiN_xH_y films and stopping at the SiN_xH_y/Cu interface. An interfacial crack is also present at the SiN_xH_y/Cu interface.*

Crack network description The SEM observations of the tensile loaded surface (top surface) during the incremental loading tests show the formation and development of channel cracks within the pSiOC:H and SiN_xH_y films. The cracks are randomly distributed, at least at first observation, over the entire zone of the sample between the two 4PB inner spans where the tensile stress is constant. Figure IV.9 shows the porous SiOC:H surface at different levels of total film stress[1]. We observe a progressive cracking mechanism with first the nucleation of some cracks followed by the crack network development towards saturation. The crack direction is normal to the tensile stress in the film. The film residual stress was evaluated before cutting the samples by wafer-curvature measurement and is found at 60 MPa. This value correlates with the 59 MPa determined for the 742 nm-thick pSiOC:H film deposited on the silicon substrate in chapter III, showing that the presence of the copper interlayer does not affect the residual stress of the pSiOC:H film.

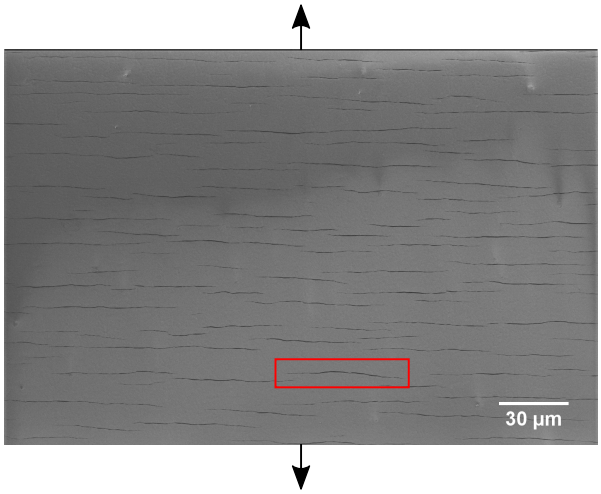
[1]The total film stress is calculated with equation (II.32) as the sum of the film residual stress and the stress transferred from the substrate to the film through the interface during the FPB test, see chapter II. In the following, total film stress (σ_f) always refers to the sum of the residual (σ_{res}) and applied (σ_{FPB}) film stresses.



(a) $\sigma_f = 112$ MPa



(b) $\sigma_f = 130$ MPa



(c) $\sigma_f = 152$ MPa

Figure IV.9: *SEM top views of an array of channel cracks growing in the 742 nm-thick porous SiOC:H deposited on a SiN_xH_y/Cu/Si stack for different total film stresses in the film. The black arrows indicate the tensile stress direction. The red open rectangles show the evolution of one crack.*

Crack density The first presented parameter is the crack density plotted as a function of total film stress for two samples. Three different zones per sample were considered (size of 250 by 170 µm), indicating the good reproducibility of the phenomenon (figure IV.10).

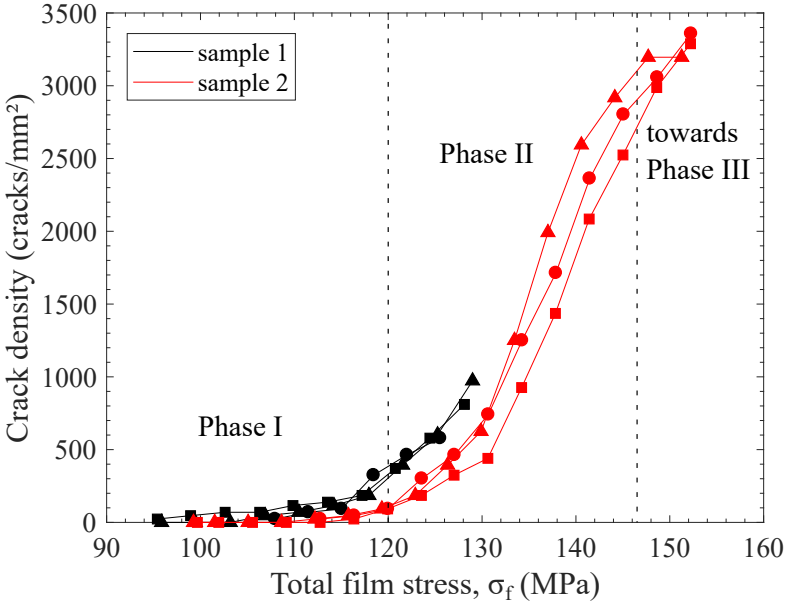


Figure IV.10: *Crack surface density as a function of total film stress (the circle, triangle and square marks correspond to three different zones observed per sample)*

The cracking process reveals three damaging phases:

– Phase I: onset of cracking

  At the beginning of the test, some cracks initiate, randomly distributed on the sample surface (figure IV.9a). We assumed that the crack initiation is governed by the statistical distribution of small defects such as surface flaws. When increasing the stress, new cracks initiate and slightly interact with each other. However, during this phase, no propagation of existing cracks is observed. We estimate the critical film stress σ_c, corresponding to the apparition of the first array of cracks, at 109 $\pm$ 8 MPa.

– Phase II: mid-point cracking

  When reaching a certain level of total film stress, the cracking mechanism is accelerated. This is observed by a steeper slope of the density curve in figure IV.10. This accelerated nucleation is observed together with a significant propagation of the pre-existing cracks (figure IV.9b).

– Phase III: towards saturation

  At the end of phase II, for one zone (red triangle marks on figure IV.10), we observe the beginning of the crack saturation (phase III). However, for the other regions, the density is still increasing. We suppose the saturation phase was close to the end

of our experiment for sample 2, but it prematurely broke before reaching this step. The sample 1 broke long before phase III showing the dispersion of the substrate fracture strength.

Crack length The total crack length per unit area is plotted as a function of total film stress for the same samples in figure IV.11. Similar crack development with phases I and II is observed, but phase III is not detected here. The interest in having the total crack length, besides the surface crack density, relies on the possibility to quantify the crack growth, so to decorrelate crack nucleation from crack propagation. Indeed, if the cracks grow, the total crack length increases for a given crack density. On the contrary, if the cracks do not propagate, the total crack length is constant for a given density and only increases if the density is increased. That is what we schematically see in figure IV.11: very low crack length per unit area up to 125 MPa, then an increase, which shows that new cracks nucleate and the pre-existing cracks propagate.

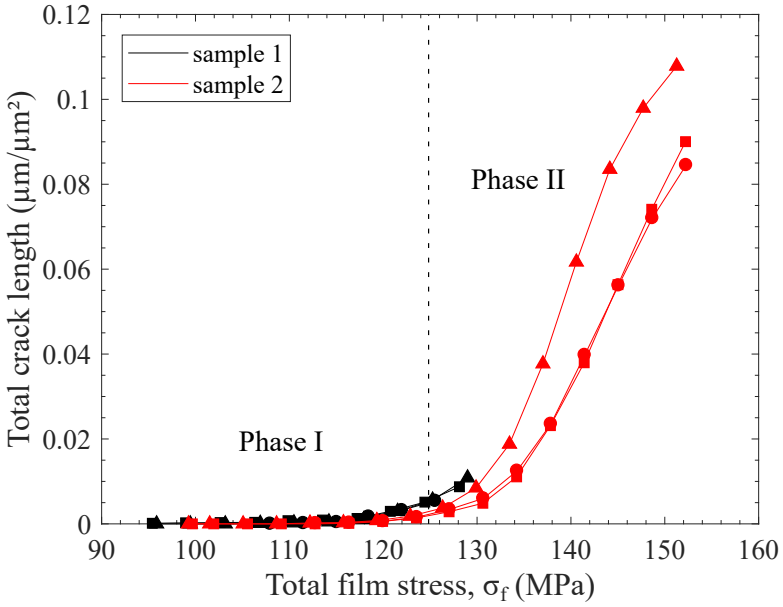


Figure IV.11: *Total crack length per unit area as a function of total film stress (the circle, triangle and square marks correspond to three different zones observed per sample)*

However, for different crack densities, attributing an increased length parameter to new cracks initiation or to existing cracks propagation could be difficult. Another way to characterize the crack propagation is the use of the statistical distribution of the individual crack lengths. Figure IV.12 below shows the statistical distribution of the crack lengths as a function of total film stress for sample 2. The distribution is represented with box-plots. The three first increments are not represented by box-plots as their populations are too small.

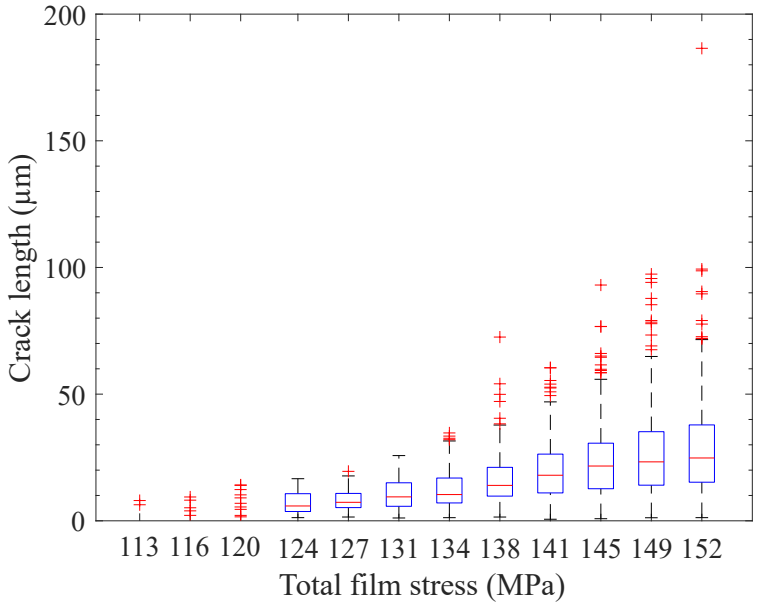


Figure IV.12: *Statistical distribution[2] of crack length as a function of total film stress for sample 2*

The maximal measured length is substantially increased with film stress, varying from less than 10 µm for the initial increment to almost 190 µm for the last. The variations are less important for the median values but still significant: until 134 MPa, the median lengths increase with film stress is rather limited. In this range, only small populations of cracks are observed. From 134 MPa to 145 MPa, the median lengths significantly increase at each increment from 10.4 µm to 21.6 µm. After 145 MPa, the median lengths still increase up to a median value of 24.8 µm. We note the increasing amount of outliers for the last states corresponding to long cracks measured once.

To partially conclude, the total crack length per unit area can compare crack lengths at identical densities to state on the crack propagation. However, to compare two states with different densities, the individual crack length distribution help to decorrelate the crack nucleation from the crack propagation.

Crack spacing The last defined parameter is the crack spacing, plotted versus the total film stress in figure IV.13. Looking at the crack spacing evolution, this parameter decreases continuously with an increased film stress. During phase I, there are a few cracks in each zone, so the calculated crack spacing depends largely on the image size. From 125 MPa, the decrease is smoother, and the spacing tends to an asymptotic value. In our experiments, the minimal average crack spacing is measured at 11 $\pm$ 1 µm at $\sigma_f = 152$ MPa.

[2]The box-plot is a statistic method to represent groups of numerical data. The red line is the median, the bottom and top of the blue box are the 25^{th} and 75^{th} percentiles, the whiskers go from the end of the interquartile range to the furthest observation within the whisker length (= 1.5 times the interquartile range) and the red crosses are the values out of the whiskers.

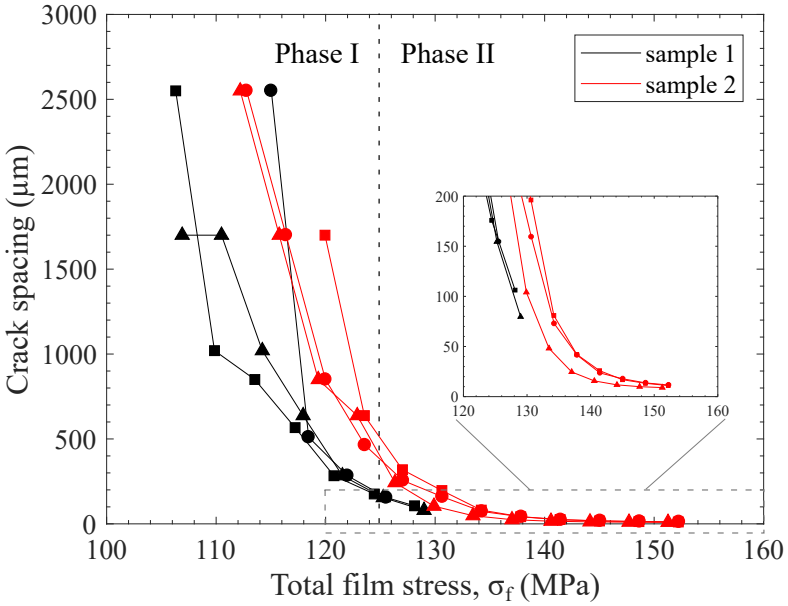


Figure IV.13: *Average crack spacing as a function of total film stress (the circle, triangle and square marks correspond to three different zones observed per sample)*

IV.3.2.4 Discussion

In the previous section, the cracking mechanism was described for the 742 nm porous SiOC:H film deposited on the following stack: SiN_xH_y 60 nm / Cu 2 µm / Si 400 µm. The crack network evolution was described in three stages: onset of cracking, mid-point cracking, and saturation. This sequence was already observed in thin films deposited on substrates during fracture tests [15, 84]. However, questions may be raised about the particular cracking mechanism observed (short crack network) and the influence of the Cu interlayer on it. Moreover, the cross-sectional view showed that an interfacial crack propagates at the SiN_xH_y/Cu interface near the channel crack. We thus discuss the influence of this beneath interfacial failure on the cohesive cracking of the film here below.

Influence of the copper interlayer on the pSiOC:H total film stress

In chapter II, the total film stress calculated with equation (II.32) corresponds to the sum of the residual stress and the stress applied to the film during FPB. We previously saw that SiOC:H film residual stress was unaffected by the presence of the copper interlayer. However, the previous equation, used to calculate σ_f, was defined for a film directly deposited on a substrate. To state on the influence of the copper interlayer on the stress field in the film during the FPB, the test was modeled using finite elements with Ansys software. The analysis was carried out in 2D and plane strain condition. All the materials were considered isotropic. To simplify the analysis, only the half-sample was represented due to symmetry conditions. The applied boundary conditions were:

– blocked vertical and longitudinal displacements of the lower roller

– vertical displacement of the upper roller to load the sample

– at x=0, applied symmetric condition along all the sample thickness

The model is schematized in figure IV.14. The pSiOC:H film was meshed with 3 elements through the thickness, the copper interlayer with 2 elements through the thickness (quadratic element) and the silicon had a progressive meshing with a refinement near the copper layer and near the FPB spans contact zone (figure IV.15).

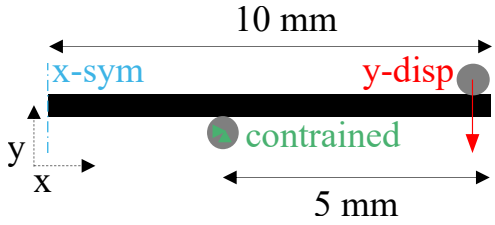


Figure IV.14: *Schematic of the finite element model*

To take into account the plasticity of the copper interlayer, we considered a simple bi-linear strain-stress law with an elastic modulus of 135 GPa, a yield strength of 200 MPa and a plastic hardening coefficient of 20 GPa (figure IV.16a) [125]. Figure IV.16b shows the total stress in pSiOC:H as a function of the silicon substrate maximum tensile stress (just at the Cu layer interface). The black line in figure IV.16b is the maximum tensile stress in the pSiOC:H layer analytically calculated with equation (II.32) and the red line results from the finite element analysis considering an elasto-plastic Cu under-layer. The mismatch between the analytic and simulated stresses is about 0.8%. We conclude that is the silicon substrate which drives the stress seen by the film during the FPB and confirms the validity of equation (II.32) even in presence of a ductile copper interlayer.

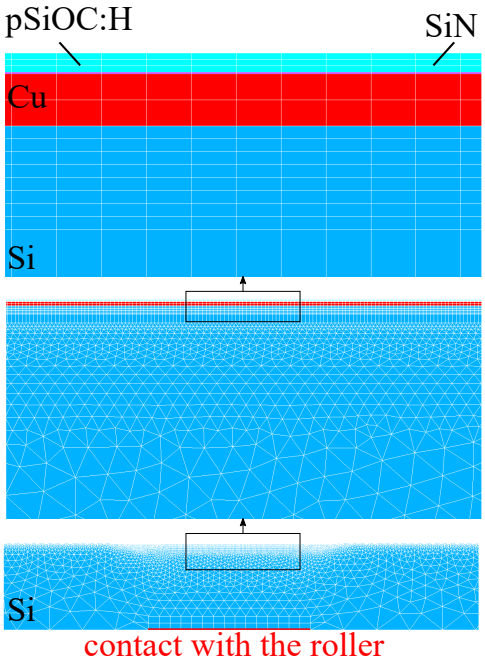
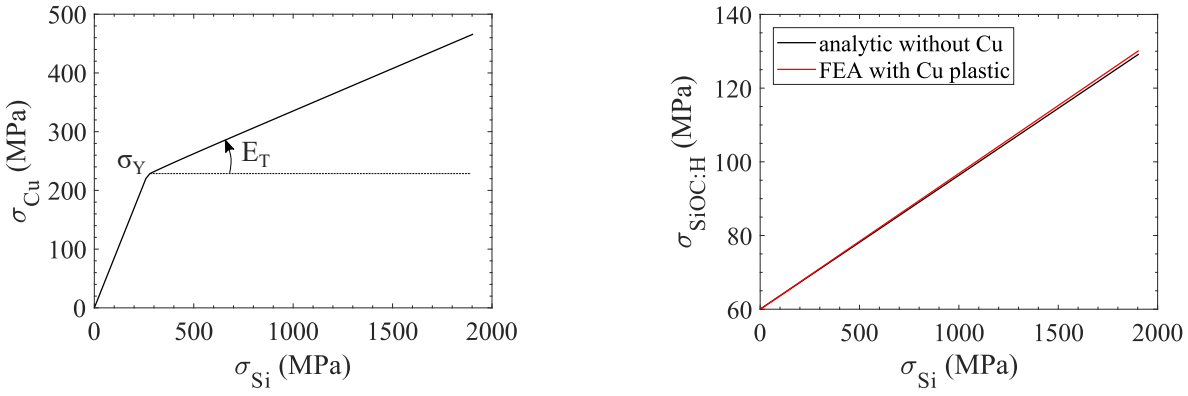


Figure IV.15: *Progressive meshing of the silicon substrate to overcome the scale difference between the thin films and the thick substrate: black open rectangles show the details of the upper surface of the sample, finally revealing the three layers of Cu, SiN_xH_y and pSiOC:H deposited on the silicon wafer*



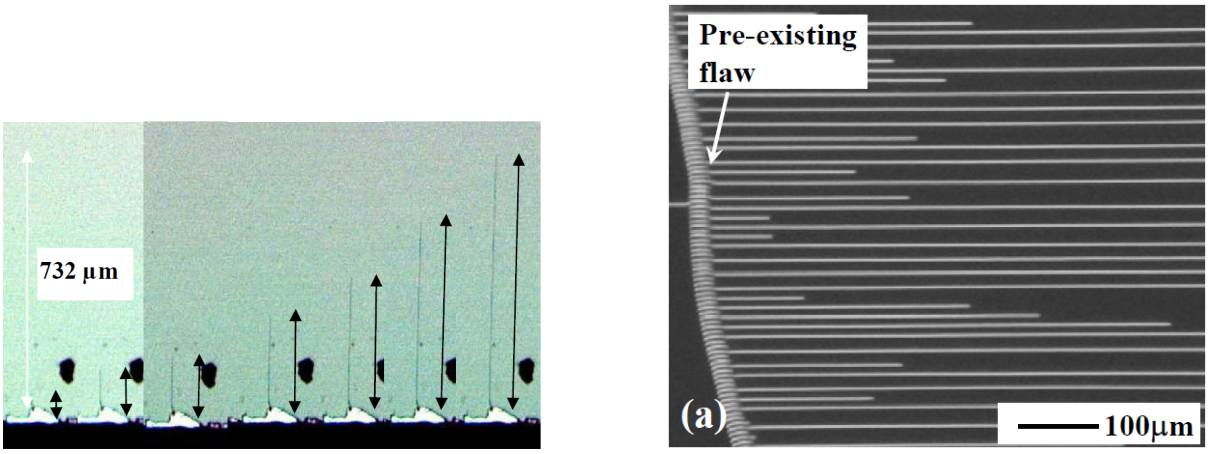
(a) ***(b)***

Figure IV.16: *Influence of copper sub-layer on SiOC:H film stress: (a) elasto-plastic bi-linear law with σ_Y = 200 MPa and E_τ = 20 GPa (b) analytic results without Cu versus numerical results with plastic Cu*

Influence of the copper interlayer on the channel crack morphology

The observed damage mechanism in the 742 nm-thick porous SiOC:H deposited on a stack comprising a 60 nm-thick SiN_xH_y and a 2 µm-thick Cu on a 400 µm-thick Si wafer was an array of short cracks forming and extending in both SiOC:H and SiN_xH_y (figure IV.8).

On SiOC:H films under four-point bending loading, but of thicknesses of 1.8, 1.6 and 1 µm, Brillet observed continuous channel cracks running along the entire width of the sample and forming in SiOC:H directly deposited on the silicon substrate [10]. He *et al.* made the same observation for a 2 µm-thick OSG[3] film deposited on a silicon substrate, also loaded in four-point bending configuration [54]. In both studies, the cracks initiated from artificially created flaws (figure IV.17).



(a) *(b)*

Figure IV.17: *Channel cracks in low k films deposited on silicon substrates: (a) 1.8 µm-thick SiOC:H film (from[10]) and (b) 2.025 µm-thick OSG film (from[54])*

However, Brillet showed that a higher stress in the substrate had to be reached to crack a thinner film. Moreover, He *et al.* studied another multilayer: they deposited a 1 µm-thick OSG onto a film stack comprising a 60 nm-thick SiN_xH_y and an 843 nm carbon-doped silicon oxide deposited on a silicon substrate. Thus, we note that other materials can be efficient as interlayers than metals. In that configuration, the authors observed again an array of continuous channel cracks cutting across the SiOC:H and SiN_xH_y layers, stopping at the SiN_xH_y/SiOC:H interface. This conclusion justifies the use of the copper interlayer to be able to crack the 742 nm-thick pSiOC:H, which is thinner than the films of similar natures observed in the previously cited studies.

Thus, a question is raised: *how would the copper interlayer presence affect the upper channel crack morphology?* Two parameters are discussed to address this question: the thickness of the porous SiOC:H (< 1 µm) and the presence of a 2 µm-thick ductile copper layer below the oxide film.

[3]The OrganoSilicate Glass is a kind of *low k* carbon-doped oxide.

In [101], McElhaney and Ma investigated a channel cracking mechanism forming within a 4 µm-thick SiO_2 layer deposited on 2 µm-thick Al-Cu interlayer on a Si wafer loaded in four-point bending (figure IV.18). In this case, they observed an array of continuous channel cracks. We note that the SiO_2 had a larger thickness than the beneath metallic interlayer.

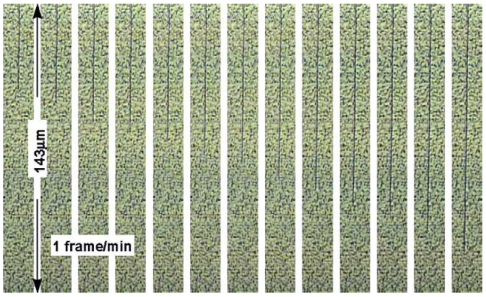
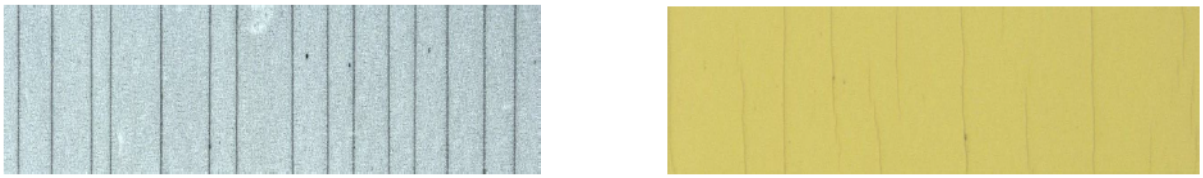


Figure IV.18: *Channel cracks in a 4 µm-thick SiO_2 film deposited on 2 µm of Cu deposited on silicon wafer (from [101])*

In [15], Ben Cheikh studied the influence of a ductile silver interlayer between two titanium oxide films. Two stacks, deposited on soft Poly Ethylene Terephthalate (PET) substrates, with different thicknesses were considered: 30/10/30 nm and 30/80/30 nm to evaluate the influence of the silver interlayer thickness on the cracking mechanism (figure IV.19). The results showed that, for the first configuration, some short cracks initiated within the three layers stack, while for the latter, long continuous cracks were observed after tensile testing. We note that the three layers fractured in their experiment (*i.e.* both oxide and silver layers). Even if the material, layer configuration and crack location are different, the study by Ben Cheikh showed the influence of a ductile interlayer on the cracking of a ductile-brittle stack.



(a) ***(b)***

Figure IV.19: *Channel cracks in a tri-layer TiOx-Ag-TiOx deposited on a soft PET substrate: (a) thicknesses of 30-10-30 nm : continuous cracks corresponding to brittle cracking (b) thicknesses of 30-80-30 nm: short cracks corresponding to ductile fragmentation (from [15])*

The difference between the experiments carried out by McElhaney *et* Ma and the present study is the thickness and stiffness of the oxide film compared to those of the metallic interlayer. We suppose that the deformation applied to pSiOC:H is similar to that within the copper layer, which is predominant regarding its thickness and stiffness.

Thus, even if the copper layer does not fracture, the transferred deformation from the substrate to the film through the copper influence the fracture mechanism. A stiffness ratio is defined considering an effective stiffness (elastic modulus times thickness) of the upper film and of the metallic interlayer, similar to the one defined by Le Druillennec for a film-on-substrate system [30]:

$$R = \frac{E_m t_m}{E_f t_f} \tag{IV.2}$$

where E_m and t_m are respectively the elastic modulus and thickness of the copper interlayer.

Le Druillennec showed that the thickness of the film can be responsible of the transition from a continuous cracking to a short crack mechanism in metallic thin films. This behavior can be monitored thanks to the parameter R. If R is near 1, the thin film and metallic interlayer show a similar effective stiffness, which results in a continuous cracking mechanism. If R is high, the metallic interlayer show a higher effective stiffness, which is traduced by a short cracking mechanism.

Using equation (IV.2), we calculate the ratio for the configuration used in [101] to 1, while in our study, the ratio is equal to 52. Qualitatively, we have a soft and thinner film deposited on the metallic interlayer. We assumed that if the metallic interlayer effective stiffness is greater than the thin film effective stiffness, the predominant deformation is that of the metallic interlayer, which is a ductile layer. Moreover, a thicker film stores more energy than a thin film, which is so more prone to continuous cracking.

We suppose that a limit ratio can be defined to justify the existence of both the short and continuous cracking for similar multilayers with different thicknesses. However, experiments varying the thicknesses of both film and metallic interlayer must be conducted to estimate this limit. As a first approach, considering a ratio of 1 to observe a continuous cracking, the corresponding copper interlayer thickness needed to observe continuous cracks forming with the same 742 nm-thick pSiOC:H film is calculated at 38 nm. A copper layer of such thickness can be deposited but a question remains about the effectiveness of a such thin interlayer to constrain the crack within the oxide film.

To conclude, the copper interlayer is supposed to play a role in the cracking mechanism of the above thin film. Indeed, the pSiOC:H film shows a cracking mechanism characteristic of the ductile fracture, probably induced by its stiff and thick metallic beneath layer. To observe a continuous cracking in the same configuration, the film thickness must be increased and/or the copper interlayer thickness must be reduced.

Influence of the interfacial delamination on the pSiOC:H cracking mechanism

Figure IV.20 depicts the array of channel cracks, observed with a light microscope. The contrast at the edge of some cracks shows that the film partially delaminates from the substrate for approximately 20% of the cracks at $\sigma_f = 152$ MPa (see figure IV.8 for the localization of the delamination). Thus, a mixed-mode cracking is observed with concomitant cohesive fracture and interfacial delamination for some cracks (figure IV.21). The former pertains to the brittleness of pSiOC:H subjected to tension, while the latter illustrates the loss of adhesion between SiN_xH_y and Cu. Two questions are thus raised: *under what conditions interfacial debonding would accompany the growth of a channel crack? How would the interfacial delamination affect the fracture in thin film structures?*

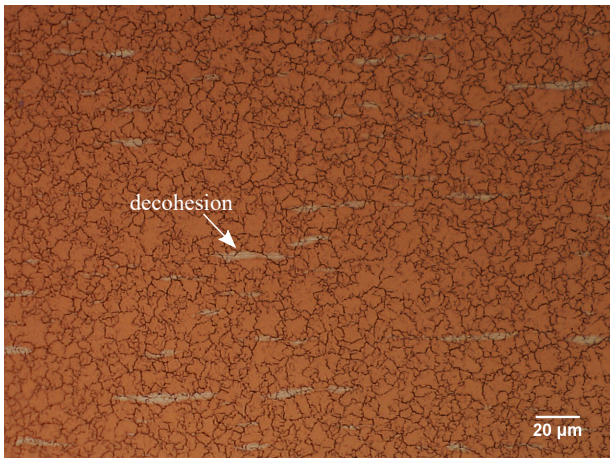


Figure IV.20: *Optical top view of an array of channel cracks in pSiOC:H ($\sigma_f = 152$ MPa). The black substructure is the copper layer microstructure, and the contrasted areas (appearing in light grey) are interfacial cracks at the SiN_xH_y/Cu interface.*

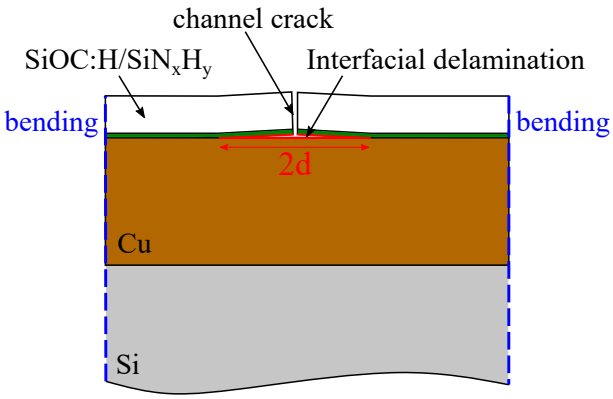


Figure IV.21: *Schematic illustration of a channeling crack cutting across the porous SiOC:H and SiN_xH_y with a concomitant interfacial debonding between the SiN_xH_y and the Cu layers. The parameter d is the half-width of the interfacial crack.*

The energy release rate of an interfacial crack of width d is calculated in equation (IV.3). We assume the channel cracks are in steady-state.

$$G_d = Z_d \frac{\sigma_f^2 h_f}{E_f} \tag{IV.3}$$

where Z_d is a dimensionless function depending on the delamination width, the film thickness and the Dundurs' parameters [6, 103]. To determine Z_d, the 2D plane-strain problem illustrated in figure IV.21 has to be solved. The measured interfacial crack widths, d, range from t_f to 2.6 t_f on the sample 2 loaded at $\sigma_f = 152$ MPa.

Thus, an interfacial crack can propagate if:

$$G_d > G_{ic} \tag{IV.4}$$

where G_{ic} is the SiN_xH_y/Cu interface critical energy release rate.

Now, the influence of a surrounded interfacial crack on the driving force of a channel crack is discussed. When considering a mixed-mode channel cracking mechanism in thin films on substrates, the energy release rate is rewritten as [103]:

$$G_{tot} = G_{ss} + \frac{2}{t_f} \int_0^d G_d(x) dx \tag{IV.5}$$

where G_{ss} stands for the energy release rate of the channel crack, t_f is the film thickness, d is the delamination width, and $G_d(x)$ is the energy release rate of the interfacial crack of total thickness d (along x axis).

The delamination, if occurring, relaxes the stress at the crack tip, so the driving force necessary for channel cracking is higher than without delamination. Moreover, additional energy can also be necessary to fracture the interface. Thus, if the energy release rate is higher than the critical energy release rates of the channel cracking and the interfacial crack, a mixed-mode cracking is observed with concomitant cohesive fracture and interfacial delamination. If not, only cohesive fracture is observed. This is illustrated by [103]:

$$G_{tot} \geq G_c + G_{ic} \tag{IV.6}$$

where G_c is the critical energy release rate of the film and G_{ic} is that of the interface.

The effective energy release rate for a channel cracking accompanied by a stable delamination can be considerably higher than the energy release rate of a purely cohesive channel crack.

However, in some cases, the stress concentration at the crack tip can causes the delamination initiation without additional loading. However, without cohesive crack, the delamination cannot be initiated as the stress level in the film is not sufficient.

Determination of the energy release rate for a steady-state channel crack

A steady-state channel crack is usually defined as when the crack length exceeds the film thickness and propagates stably (*i.e.* no critical crack extension). In this case, the energy release rate is calculated as the energy change that occurs when converting an intact slice of material ahead of the crack into a cracked slice of material in the crack wake. As only 20% of the cracks show a surrounding delamination, the interfacial cracking is not considered in the following. According to Hutchinson and Suo, the energy release rate for a channel crack can be determined under plane strain condition with [61]:

$$G_{ss} = Z\frac{\sigma_f^2 h_f}{\overline{E}_f} \tag{IV.7}$$

To calculate Z for a plastic substrate (such as in figure IV.4a including the copper interlayer), Hu *et* Evans developed an approximate formula using a shear lag model (equation (IV.8)) [57].

$$Z \approx \frac{\sigma_f}{\sqrt{3}\sigma_Y + Z_{el}} \tag{IV.8}$$

where σ_Y is the yield stress of the copper layer and Z_{el} the elastic component of the dimensionless parameter Z.

With $Z_{el} = 1.25$ (from the tables in [6] considering $E_f = 7.4$ GPa and $E_{Cu} = 135$ GPa), G_{ss} at the onset of cracking (*i.e.* at $\sigma_f = 109$ MPa) is equal to $\mathbf{1.7 \pm 0.3\ J/m^2}$. Assuming the steady-state for the channel cracks forming within pSiOC:H and no shear loading in mode II or mode III (*i.e.* imposed symmetric loading and equi-biaxial residual stress), the channel crack propagates in mode I. The energy release rate can thus be expressed as a function of the stress intensity factor K_I (equation (IV.9)).

$$G_{ss} = \frac{K_I^2(1-\nu_f^2)}{E_f} \tag{IV.9}$$

From equation (IV.9), K_I at the onset of cracking is estimated at $\mathbf{0.11 \pm 0.01\ MPa\sqrt{m}}$. This value agrees with K_{NI} calculated at 0.10 ± 0.02 MPa$\sqrt{\text{m}}$ through nanoindentation testing after film deposition.

In this section, the delamination was assumed to be negligible to calculate the energy release rate as only 20% of the cracks show a surrounding delamination. However, we note that regarding the cracked surfaces, at $\sigma_f = 152$ MPa, the cohesively fractured surface is about 3117 µm^2. On the other side, the delaminated surface is about 1943 µm^2 considering a width of 2.5 µm and 20% of the channel cracks having a concomitant delamination. Further investigations are needed to take into account the delamination, especially to determine the fracture parameters of the interface SiN_xH_y/Cu.

IV.3.3 Influence of the environment

IV.3.3.1 Constant loading tests

To study the influence of the environment (and in particular of the humidity) on the cracking mechanism in pSiOC:H, we carried out constant loading tests. First, samples were loaded at P_{crit} to initiate some isolated cracks. Then, the displacement was blocked to observe *in situ* the evolution of the crack network with time. The displacement was kept constant for 20 min and between each time step, the micromachine was placed into the SEM chamber for the imaging. As discussed in chapter I, the water molecules enhance the nucleation and propagation of cracks by reducing the stresses needed to break the atomic bonds. To highlight this mechanism, the samples were tested under three environments: ambient (21°C and RH estimated between 35 and 60% but not controlled), high vacuum in the SEM chamber and humidity saturation, all at room temperature. The last condition was obtained using a small chamber placed around the FPB fixture into which 1 g of hydrophilic cotton humidified with 20 ml of hot water (100 °C at the beginning of the test) was placed. This small set-up allowed the environment saturation in humidity in a few minutes with condensed water on the chamber walls. For all experiments, the initiation was performed in ambient environment.

IV.3.3.2 Imaging

To describe the crack network and its evolution during the constant loading tests, the samples were imaged at different time steps. During the last experiments, we observed a noticeable effect of the electron beam on the pSiOC:H surface. To clarify this effect, two zones were compared, one was previously irradiated by SEM and the other was not irradiated and chosen sufficiently far away from the first one. As already mentioned in chapter II, the porous SiOC:H is sensitive to electron beam, thus a low voltage was used to image the crack array (HV = 2 kV). The total crack length per unit area *versus* crack surface density for the two zones is plotted in figure IV.22.

A higher total length is measured for the new zones at an equivalent crack density. That means the electron beam affects the crack propagation, while the nucleation mechanism seems only slightly influenced. As a precaution, a new zone will be imaged at each step during the following constant loading tests[4].

Even if the same crack cannot be monitored in this case, we saw, with the previous step-loading experiments, the great reproducibility of the crack network parameters between each zone. Thus, the channel crack network development under constant loading under different environmental conditions can be studied properly.

[4]A light microscope was also tried but the underneath copper microstructure associated with the inherited film surface topography induced a high contrasted image, where the cracks were not easily detected.

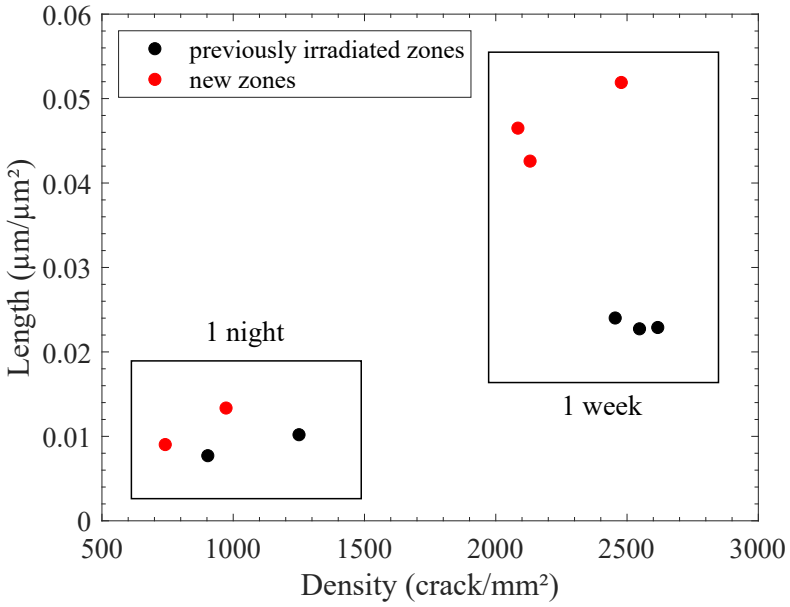


Figure IV.22: *Total crack length per unit area as a function of surface crack density for two cases: previously irradiated zones and new zones non affected by the electron beam. Two holding time are plotted: 1 night and 1 week for the same sample.*

IV.3.3.3 Results

In this section, the crack network was monitored during the constant loading tests under three environments: ambient, humidity saturation and high vacuum.

Load-displacement curve The load-displacement curve obtained during a constant loading test is given in figure IV.23a. Similarly to the incremental loading curve, there are no force drops corresponding to crack initiation and extension, as the film is too thin compared with its thick and stiff silicon substrate. The slight load variation (about 2 N over 6 h) during the holding time is attributed to the set-up relaxation (figure IV.23b). Also, the repeated decreases and increases in load are caused by the loading and unloading of the micromachine into the SEM chamber (figure IV.24). Indeed, evacuating the SEM chamber slightly plays on the measured load.

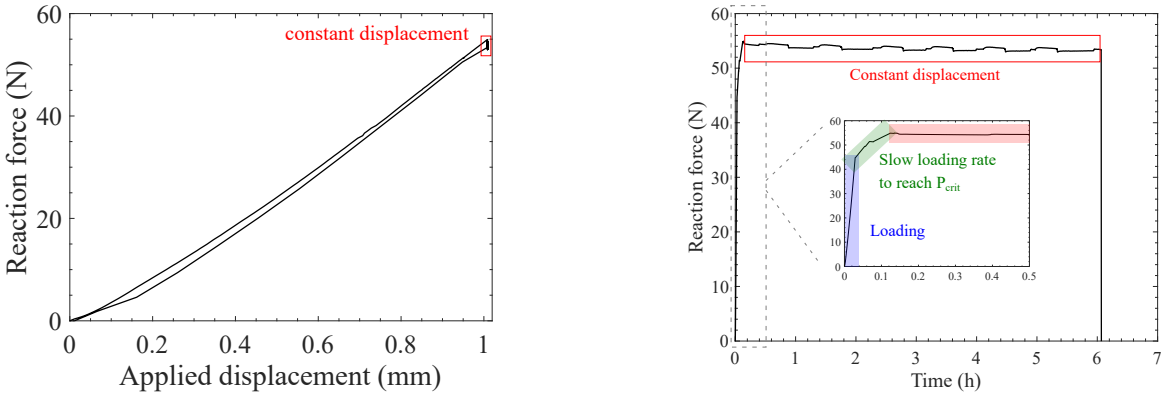


Figure IV.23: *Force-displacement (loading-unloading) (a) and force-time (b) curves during constant loading (red rectangles show the constant displacement steps)*

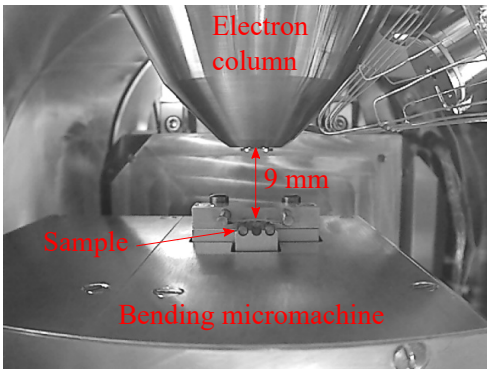


Figure IV.24: *In situ SEM bending micromachine configuration*

Ambient environment Figure IV.25 presents the increase in surface density during the constant loading compared to the previous results obtained with the incremental loading test as a function of total film stress. The time effect is clear: after holding the displacement for one week, a density about 2400 cracks/mm^2 is measured at $\sigma_f = 110$ MPa. This corresponds to the crack density observed at 140 MPa during the incremental loading test. Thus, new cracks nucleate during constant loading tests under ambient environment.

Figure IV.26 depicts the statistical distribution of crack lengths for the different holding times. As there are not enough data before 40 min, all data points are plotted. Between the onset of cracking and 40 min, no long crack propagation is observed. However, during longer holding times (*i.e.* one night and one week), the crack length distributions show evidence of crack propagation for the majority, even if very small cracks are still measurable. Moreover, a larger maximal crack size is measured after one week regarding the outlier data of the box-plots. Thus, the experiment confirms the crack propagation under constant loading at ambient environment. We also note the increase in dispersion of the crack lengths with increasing time. The crack propagation explains the increase in length, while the crack nucleation explains the lower boundary of crack length.

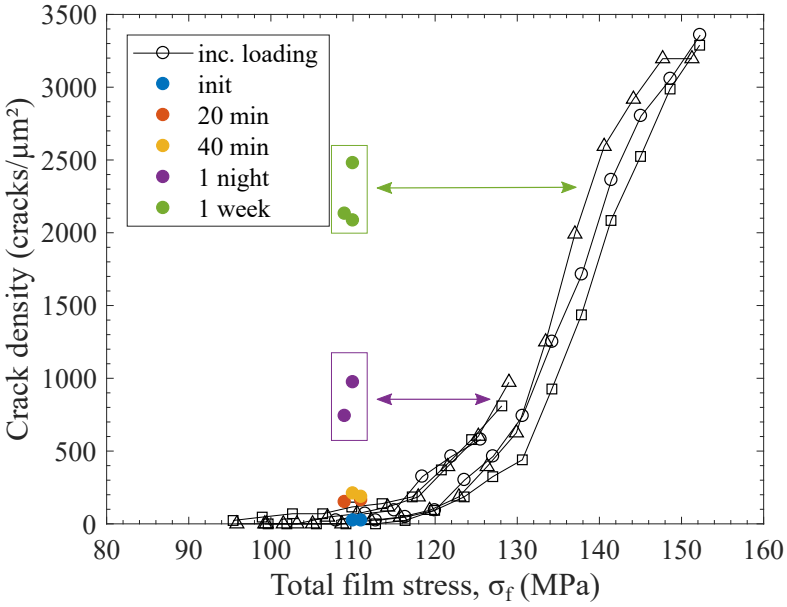


Figure IV.25: *Surface crack density as a function of total film stress: comparison between incremental loading results (open marks) versus constant loading results (full marks) under ambient environment*

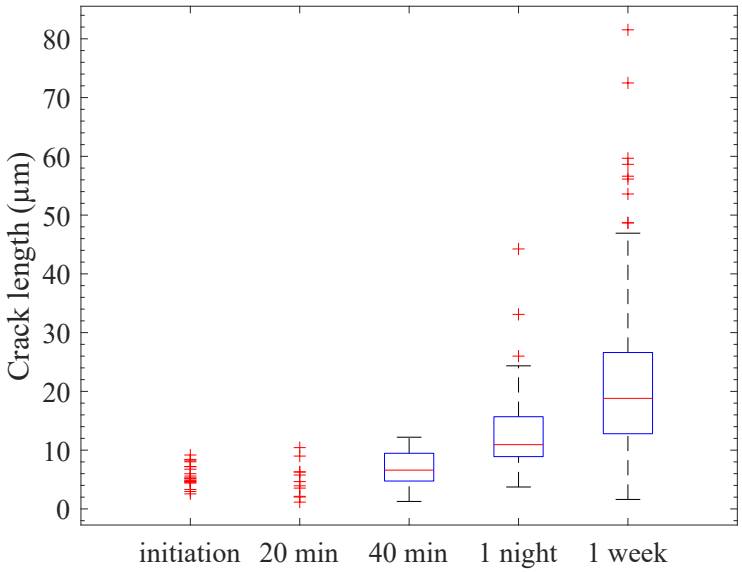


Figure IV.26: *Statistical distribution of crack length as a function of holding time during constant loading test at $\sigma_f = 110$ MPa in ambient environment*

To summarize, crack nucleation and propagation phenomena are both enhanced by ambient environment at $\sigma_f = 110$ MPa.

Modified environments We carried out the same experiments under different environments to highlight their influence on the cracking mechanism of pSiOC:H. Figure IV.27 shows the total crack length per unit area *versus* crack density for three en-

vironments: high vacuum, ambient and humidity-saturated for holding times of 20 and 40 min. The crack nucleation mechanism is accelerated under humidity-saturated environment, whereas the tests performed under high vacuum reveal neither crack nucleation nor propagation during the constant loading test. In addition, the humidity-saturated environment highly accelerates the crack nucleation especially during the first 20 min, the next 20 min step showing a smaller effect on both crack density and length.

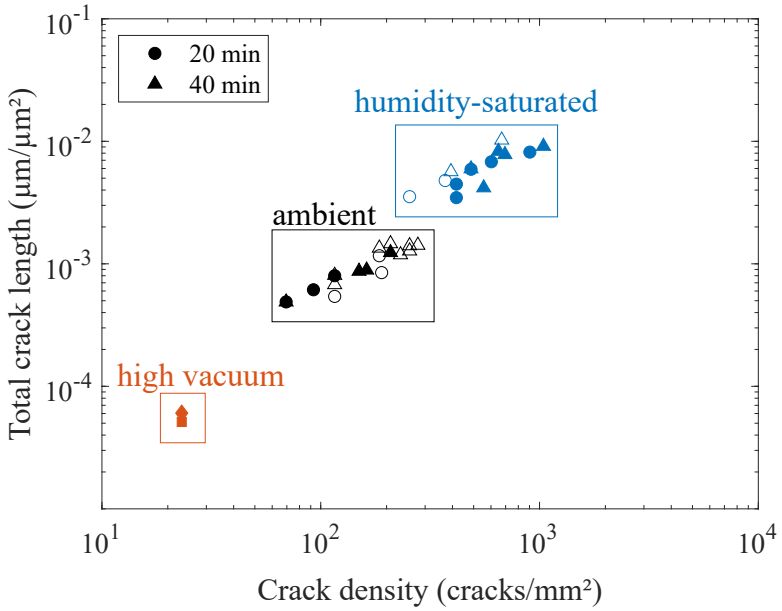


Figure IV.27: *Total crack length per unit area as a function of crack density under different environments: high vacuum, ambient and humidity-saturated. The filled and empty markers stand for sample 1 and sample 2.*

The crack length distribution is given in figure IV.28 for the tests under humidity-saturated environment, so to decorrelate propagation from nucleation mechanisms. The distributions show for both sample evidence of crack propagation as the increase in median value is significant after 20 min. Moreover, comparing the difference between the initiation median length and the value after 20 min in figures IV.26 and IV.28, moisture also clearly affects propagation of cracks.

We show that the crack nucleation and propagation are affected by the environment with no crack propagation under high vacuum and accelerated mechanisms under humidity saturation as compared to ambient environment.

IV.3.3.4 Discussion

Reproducibility of the humidity-saturated environment tests The environment saturated with humidity was obtained with a small chamber including hydrophilic cotton humidified with hot water. Both temperature and humidity were not controlled during the experiment. However, visually, condensed water varied on the edges of the chamber for some steps. The same experiments were reproduced with two other samples (red and

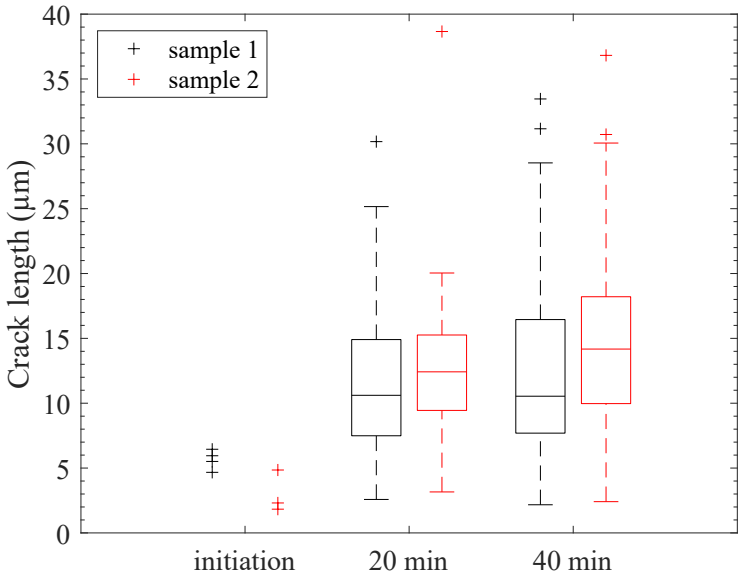


Figure IV.28: *Statistical distribution of crack length as a function of holding time during constant loading test at σ_f = 110 MPa under humidity-saturated environment*

green markers, figure IV.29). For sample 3, it is observed that after 40 min, the surface crack density has increased together with the total crack length per unit area. However, the results are closer to the ambient group. With additional time, results are more in line with those of the two first humidity-saturated samples. A similar observation is made for sample 4 with a surface crack density and total crack length per unit area close to the ambient group after 20 min, while at 40 min a large increase in both parameters (total crack length and surface crack density) is observed. A qualitative correlation was observed between the strong behavior modification of the crack mechanisms (*i.e.* blue points, 60 min for sample 3, and 40 min for sample 4) and the higher water condensation on the chamber blanks. That means the cracking mechanism in pSiOC:H is very sensitive to the environmental conditions (both temperature and humidity). It would be interesting to measure them precisely with a small temperature-humidity probe. Another solution could be using different saline salts to control the humidity level.

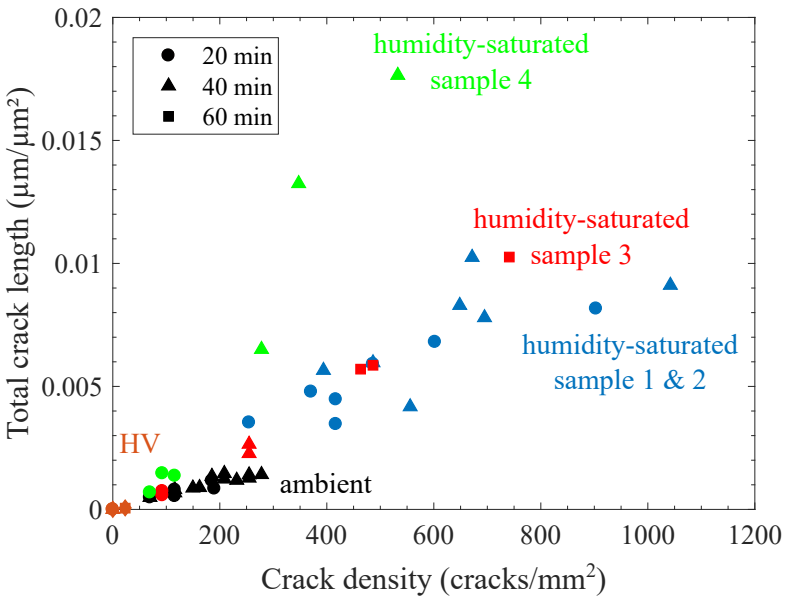


Figure IV.29: *Total crack length per unit area as a function of surface crack density under different environments: high vacuum, ambient and humidity-saturated. Reproducibility of the experiments under humidity-saturated environment.*

Mehl–Avrami–Johnson law for nucleation/growth process description In this paragraph, the experimental data are fitted with the Mehl–Avrami–Johnson (MAJ) equation [67]. Indeed, the use of the MAJ law (equation (IV.10)) derives from the fact that crack network modifications with both stress and time follows a nucleation and growth process, traduced by a sigmoidal curve. The crack length is the parameter considered here since it represents both mechanisms.

$$f = 1 - exp[-(bt)^n] \tag{IV.10}$$

In equation(IV.10), f is the transformation fraction (here, the total crack length divided by the total crack length at saturation) and t is the time. Both n and b are constants and can be derived from the ln(ln(1/(1-f))) *versus* ln(t) curve. The parameter n is related to the nucleation and growth conditions and is discussed below.

First, the total crack length according to total film stress is fitted to estimate the saturation total length value as the curve showed a sigmoidal shape. However, the fitted parameters n and b cannot be interpreted as it is not a time-dependent mechanism. We use the experimental data represented by red triangles in figure IV.11 because they are the closest to the saturation state, traduced by a slight inflection at the end of the curve. Figure IV.30 gives the corresponding total crack length per unit area as a function of the total stress in the film with the fit obtained with the sigmoid equation. The resulting total crack length per unit area at saturation is estimated at 0.108 µm/µm^2.

Knowing the total crack length per unit area at saturation, the same approach can

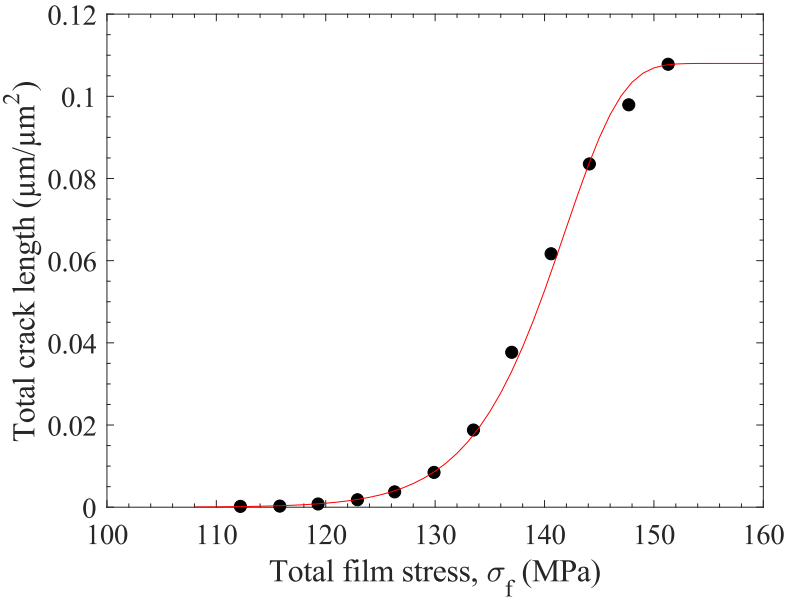


Figure IV.30: *Total crack length per unit area versus total film stress σ_f for sample 2 of figure IV.11. The red solid line represents the fitting of the experimental results by a sigmoidal curve to found the saturation value at 0.108 $\mu m/\mu m^2$.*

be applied with the constant loading test results at ambient environment. The same procedure is used to calculate n and b considering a saturation total crack length of 0.108 μm/μm^2 (see figure IV.31). The fit gives $n = 0.7$ and $b =$ 5e-5. We note the stability of the linear fit varying the total crack length at saturation. Indeed, varying the total crack length at saturation from 0.09 to 0.12 results in n values ranging from 0.7 to 0.8.

Figure IV.32 gives the total crack length per unit area as a function of the time in the film with the fit obtained with the MAJ equation. We estimate the time to reach the total crack length at saturation at 2500 hours.

In the MAJ theory, the n parameter is related to nucleation and growth conditions according to time. We calculated a n value of 0.7. According to the MAJ theory, a small value of n traduces a high nucleation rate as compared to the crack growth rate and/or a crack growth in 1D. This agrees with the experimental observations as fast crack nucleation was observed accompanied by slow crack propagation.

This analysis can be further applied on tests performed in humidity-saturated environments with more reliable temperature and humidity conditions, where both crack nucleation and propagation were found to be accelerated. This was unfortunately not possible during the PhD.

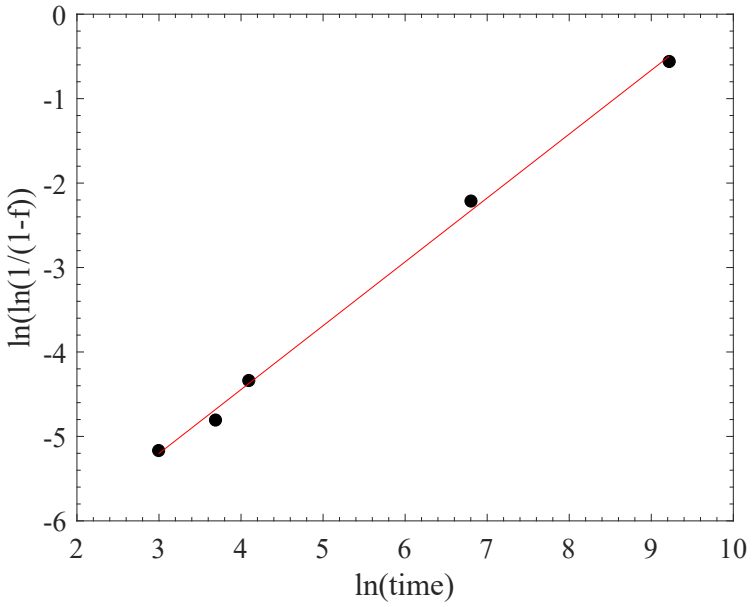


Figure IV.31: *Plot of ln(ln(1/(1-f))) versus ln(time) for the determination of n (slope) and ln b (ordinate origin) in the MAJ equation for the constant loading test. The red solid line represents the linear fitting of the experimental results with* $R^2 = 0.998$.

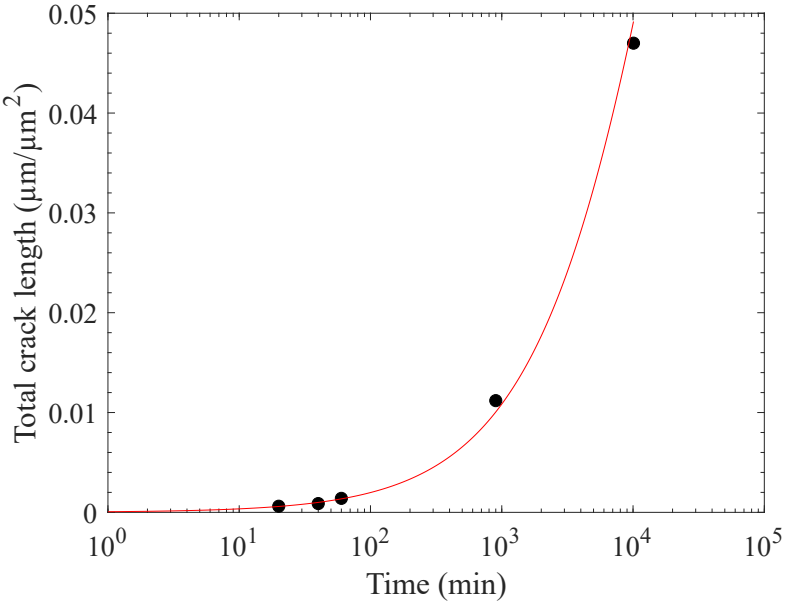


Figure IV.32: *Total crack length per unit area versus time t for constant loading test results in ambient environment. The red solid line represents the fitting of the experimental results by the Mehl–Avrami–Johnson equation with* $n = 0.7$.

Crack growth rate estimation The results presented above have showed the growth of small cracks in a 742 nm-thick pSiOC:H deposited on a stack comprising a 2 µm-thick copper interlayer under constant loading. First, we have shown that slow and stable crack extension can occur under constant loading in presence of water with an increase in the median crack lengths. This kind of crack propagation has already been observed in many other materials where it is usually attributed to environmental factors for ceramics such as glasses. The reader may refer to chapter I for more information on stress-corrosion mechanism in ceramics. Second, we have also shown an accelerated crack nucleation and propagation under humidity-saturated environment, whereas under high vacuum no evidence of crack propagation at least for a loading during 100 min was observed. Because the electron beam influences the crack propagation, new zones are imaged at each step, so the crack growth rate cannot be directly monitored for a single crack. However, a first estimation of this parameter can be calculated from the median length values with equation (IV.11).

$$v_{median} = \frac{\Delta l_{median}}{\Delta t} \tag{IV.11}$$

As a first approach, we calculate the crack growth rate from the median lengths to compare the crack growth under ambient and humidity-saturated environments for 20 min. Table IV.1 summarizes the results and shows that for a time of 20 min, the crack growth rate is higher under humidity saturation with an averaged rate from $\mathbf{10^{-11}}$ **m/s** under ambient to $\mathbf{10^{-9}}$ **m/s** under humidity-saturated environments.

Table IV.1: *Crack growth rates under ambient and humidity-saturated environments calculated from median values of crack length (equation* (IV.11)*)*

Environment	Crack growth rate (m/s)
Ambient	4×10^{-11}
Humidity-saturated sample 1	4×10^{-09}
Humidity-saturated sample 2	8×10^{-09}

The crack growth rate was also estimated from the surface crack density and total crack length per unit area defined in section IV.3.2.2:

$$v_{param} = \frac{\Delta length / \Delta density}{\Delta t} \tag{IV.12}$$

The calculated crack growth rates with equation (IV.12) are given in table IV.2. A similar trend is observed as for the rate calculated from the median results. The crack growth rate is higher under humidity saturation with a value at $\mathbf{10^{-9}}$ **m/s** instead of $\mathbf{10^{-10}}$ **m/s** calculated under ambient environment.

We note that with our two methods, the crack growth rates calculated at ambient environmental conditions show a difference of one order of magnitude. This shows the

Table IV.2: *Crack growth rates under ambient and humidity-saturated environments calculated from the surface crack density and total crack length per unit area (equation* (IV.12)*)*

Environment	Crack growth rate (m/s)
Ambient	7×10^{-10}
Humidity-saturated sample 1	3×10^{-09}
Humidity-saturated sample 2	8×10^{-09}

difficulty to calculate a reliable crack growth rate when having multiple cracks and when it is not possible to follow only one crack.

In [10], Brillet compared porous SiOC:H layers of three different thicknesses: 1.8, 1.4 and 1.0 µm. The samples comprised SiOC:H layers directly deposited on silicon substrates. The author reported a dependence of the crack growth rate on the layer thickness, with a larger stress intensity factor required to reach the same crack growth rate in the thinner film. She reported a value of crack growth rate between 10^{-9} and 10^{-4} m/s at a stress intensity factor about 0.1 MPa$\sqrt{\text{m}}$. We note that the crack growth rates reported in tables IV.1 and IV.2 are smaller than the range measured by Brillet. However, our porous SiOC:H film has a lower thickness than the ones investigated in her study and is not exactly similar in terms of chemical composition and porosity fraction. The cracking mechanism, which is different because of the copper interlayer in our case, can also explain the difference. Indeed, in this study, a short crack array is created, whereas Brillet obtained continuous cracks forming in the SiOC:H. Moreover, we observed two simultaneous mechanisms (both crack propagation and nucleation) confirming the particularity of our tested multilayer specimen.

IV.3.4 Numerical analysis

The aim of this section is to propose a method to simulate the crack network initiation and development in the pSiOC:H film. It could be used in a near future to study the mechanical integrity of more complex systems, where the experimental study could be challenging. The coupled-criterion was used to simulate the incremental loading experiment. First, we present how the coupled-criterion is implemented in a Representative Volume Element (RVE) to predict the initial cracking and the further subdivisions. Then, the numerical results are compared with the experiments. Finally, the influence of the Cu interlayer and the delamination between the SiN_xH_y and Cu films on the cracking of the pSiOC:H is deepened. The simulations were developed by Aurélien Doitrand at MATEIS laboratory.

IV.3.4.1 Coupled-criterion to model the damaging mechanism in thin films

Multicracking mechanism is described using the coupled-criterion, first introduced by Leguillon *et al.* [81]. It is based on the simultaneous fulfillment of an energy and a stress

criteria. In other words, the stress level in the material has to be enough to initiate (or propagate) a crack and enough energy has to be released to allow the crack opening (see chapter II). Below, we focus on the application of the coupled-criterion on thin films deposited on substrates.

During the four-point bending experiments, cracking occurred in the porous SiOC:H and SiN_xH_y films. Also, the cohesive cracking was possibly followed by an interfacial cracking at the silicon nitride / copper interface. This point will be discussed further.

A 2D model using a RVE was developed so the complete sample is obtained by a periodic distribution of this RVE. This method allows the simulation of crack arrays without consuming too much CPU time, as the multicracking mechanism can give rise to a large number of cracks. The 2D model represents a section of the sample. Two states of the RVE are considered, the uncracked and cracked states (figure IV.33).

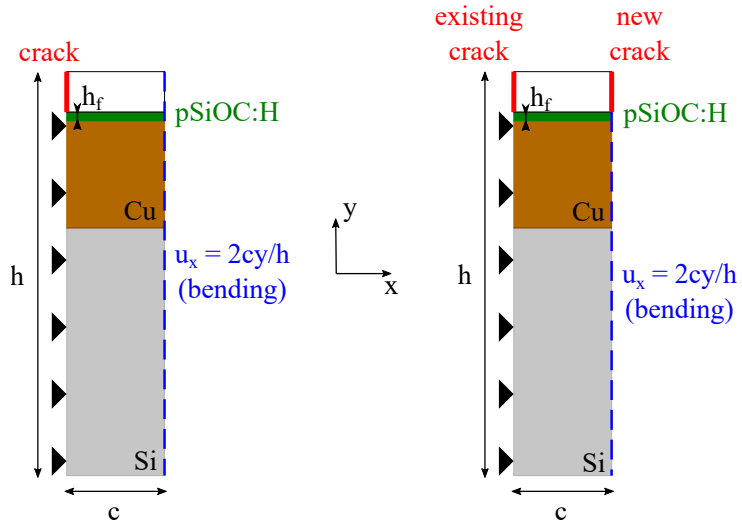


Figure IV.33: *Representative volume elements for the analysis of the first crack occurrence (left) and for the subsequent subdivisions (right). The red line shows the location of the cracks, the blue dashed line is the prescribed displacement, and the black triangles are for the symmetry.*

Crack initiation The first step of the simulation was focused on the initiation of the first crack in the RVE (figure IV.33). As the RVE was periodically repeated, a periodic array of cracks with spacing *2c* was assumed at the onset of cracking. The left frames were used to analyze the occurrence of the first cracks. A symmetry was applied for the copper and silicon substrate. On the right boundary of the RVE was prescribed a horizontal unit strain for the bending equal to $u_x = 2cy/h$ (where h stands for the total specimen thickness $>>$ h_f). The spacing c value at initiation corresponds to the smallest value for which a constant initiation stress is observed. Indeed, if the cracks are sufficiently spaced, the same stress is found in the film at the initiation of the periodic array of cracks (mean distance between cracks: 2c). When the cracks become too close, it requires a larger imposed loading to initiate an additional crack.

Crack network subdivision The next step of the simulation was to create a new crack in between two existing cracks. This induces a new periodic array of cracks with spacing c (figure IV.33). The right side of the RVE (red line "new crack") was used to simulate the subsequent subdivisions. In this case, the initiation spacing, c_0, was computed with the corresponding stress in the film $\sigma_f(c_0)$. Similarly, the multiplication spacings, c, were computed with the corresponding stress in the film. At each step, the number of cracks doubles.

Coupled-criterion for the prediction of film cracking The stress criterion is defined by the statement that the tensile stress must exceed the tensile strength along all the crack path:

$$\sigma_f \geq \sigma_c \tag{IV.13}$$

where σ_f is the total tensile stress supported by the film during the test far away from already pre-existing cracks and σ_c is the film tensile strength.

The energy criterion is obtained from an energy balance between the two states: uncracked and cracked states (equation IV.14).

$$\delta U_{pot} + \delta U_{kin} + G_c \delta S = 0 \tag{IV.14}$$

where δU_{pot} is the potential energy variation, δU_{kin} is the kinetic energy variation, $G_c\delta S$ is the energy required to initiate a crack of area δS. As the model is developed in 2D, δS is reduced to t_f, the thickness of the cracked film. G_c is the critical energy release rate of the material.

Rewriting equation IV.14 for a 2D model assuming there is no kinetic energy before crack initiation (quasi-static conditions), the energy criterion is defined as:

$$G_{inc} = \frac{-\delta U_{pot}}{t_f} \geq G_c \tag{IV.15}$$

where G_{inc} is the incremental energy release rate.

Leguillon *et al.* applied the coupled-criterion to sub-micron films to predict multi-cracking mechanisms [82, 83] and showed the efficiency of this technique to describe multi-cracking in thin films. In addition, they showed that the energy criterion governs the cracking mechanisms for very thin films, whereas the stress criterion governs the cracking mechanism for thicker films. They also conclude on the challenge to predict numerically and accurately the multi-cracking mechanisms because of large scattering in the experiments due to a random distribution of flaws and the many influential parameters (relative thickness of the layers, material properties, loading...). Nevertheless, the numerical prediction meets satisfactorily the orders of magnitude of crack densities as a function of increasing applied loads. This is encouraging for further applications of the coupled-criterion numerical analysis on other thin film-on-substrate systems.

IV.3.4.2 Multi-cracking modeling results

As for the experimental characterization of the array of cracks developed in the porous SiOC:H film, crack density, length and spacing per unit area parameters can be defined. The density was defined as $D = 1/(2cw)$, the length parameter as $1/(2c)$ and the crack spacing was equal to $2c$ for the first crack network, then it is c for crack network subdivision. The simulation represents an array of continuous cracks of length equal to the sample width w.

In figure IV.34 are plotted the density, length and spacing as a function of tensile stress in the film with σ_c at 80 MPa, G_c at 1.4 J/m^2 and K_{IC} at 0.1 MPa$\sqrt{m}$ considering all materials have elastic properties and no debonding of the films from the copper interlayer. The plots are given for various crack initial spacings (colored curves). As seen, the final spacing at saturation is found around 1 - 1.6 µm (figure IV.34c) which is much smaller than the minimal spacing value observed experimentally (*i.e.* 11 µm). The typical experimental crack size for the last step of the incremental loading was around 20 - 100 µm and the density was estimated at 3.5×10^{-3} cracks/µm^2. In the model, one crack has a length of 4 mm (*i.e.* the specimen width) and the density at saturation is estimated around 0.125 - 0.250×10^{-3} cracks/µm^2 (figure IV.34a). Thus, the results are consistent if one simulated crack corresponds to 14 - 28 experimental cracks regarding the crack densities. This gives a mean crack length from 143 to 286 µm. Comparing to the experimental results, the mean crack length is overestimated.

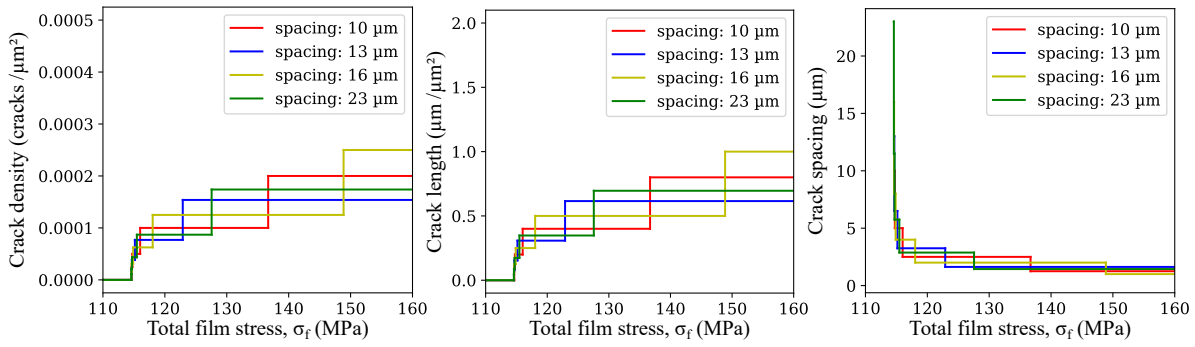


Figure IV.34: *Numerical results: (a) crack density, (b) length and (c) spacing parameters as a function of film tensile stress for different crack initial spacing*

To increase the accuracy of the model, some improvements were considered by taking into account copper layer plastic deformation, interfacial cracking along silicon nitride and copper layers interface and adjusting G_c and σ_c.

IV.3.4.3 Considering copper plasticity

As shown in the experimental part, at the level of stresses required to crack the porous SiOC:H layer, the copper has probably already been plasticized. To improve the numerical

model, instead of purely elastic properties, a bi-linear elasto-plastic behavior is used to describe the mechanical behavior of the copper interlayer with parameters $E_\tau = 20$ GPa and $\sigma_Y = 345$ MPa.

There is no change in the stress-based criterion, which remains the same as defined in equation IV.13.

However, the energy-based criterion has to be rewritten considering the energy variation caused by the plastic deformation of the copper interlayer $\delta U_{plastic}$:

$$G_{inc} = \frac{-\delta U_{pot} - \delta U_{plastic}}{h_f} \geq G_c \tag{IV.16}$$

Figure IV.35 gives the variations of film stress σ_f and incremental energy release rate G_{inc} as a function of crack spacing for both elastic and plastic cases. The red curves give results for the crack initiation phase (one crack in the RVE) and the blue curve for the crack multiplication phase (initiation of the second crack in the RVE).

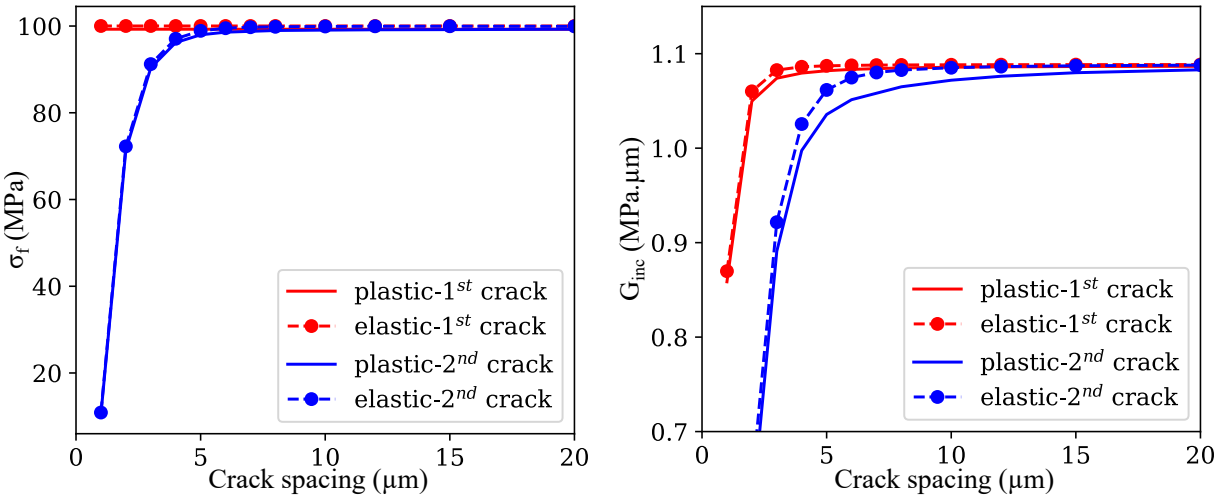


Figure IV.35: *σ_f and G_{inc} as a function of crack spacing considering that the Cu layer is fully elastic, or elasto-plastic*

For both the crack initiation and multiplication phases, the film stress values σ_f *versus* crack spacing are almost identical showing that copper plasticity does not influence the stress level in the pSiOC:H layer.

The incremental energy release rate G_{inc} for the first crack initiation is similar for both elastic and plastic Cu properties. In case of second crack initiation, we see a mismatch of the elastic and plastic curves for crack spacing ranging from 5 to 15 µm, and then the curves converge to the same G_{inc} value. At a crack spacing of 5 µm, G_{inc} varies from 1.07 to 1.04 MPa.m corresponding to a difference of 3%, which is limited.

IV.3.4.4 Considering SiN_xH_y/Cu interface debonding

In this section, the plasticity of the copper interlayer and an interfacial crack along the interface SiN_xH_y/Cu are considered. An interfacial crack of width of 2.5 µm, as observed

experimentally, is added once the channel crack is initiated. We note that during bending, the interfacial crack initiates due to stress concentration at the tip of the channel crack, thus the channel crack initiates first, then the delamination occurs. Figure IV.36 shows the variations of film stress σ_f and incremental energy release rate G_{inc} *versus* the crack spacing for both the elastic and plastic cases considering an interfacial cracking. Similarly to the precedent case, the first crack initiation and crack multiplication phases are presented.

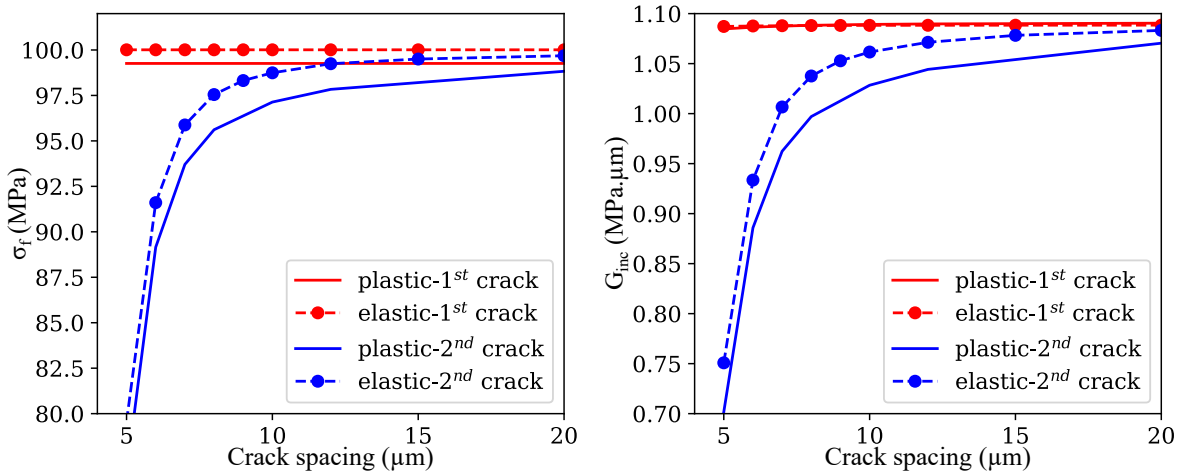


Figure IV.36: *σ_f and G_{inc} as a function of crack spacing for both elastic and plastic cases with debonding*

The account of interfacial cracking together with the plasticity of the copper interlayer plays a slight role on the stress level in the pSiOC:H layer.

For the first crack initiation, the pSiOC:H film stress considering elastic Cu properties is similar considering the interfacial cracking or not. However, considering plastic properties and interfacial cracking slightly reduces the stress in the pSiOC:H film (-1 MPa). For the multiplication phase, a decrease in the film stress is noted when taking into account both the plastic Cu properties and the interfacial cracking as compared to the elastic case.

Taking into account both plastic properties and interfacial cracking do not modify the incremental energy release rate for the first crack initiation as a function of crack spacing. However, a larger loading to crack network saturation is necessary considering both plastic Cu properties and interfacial cracking.

IV.3.4.5 Correlation with experimental results

Figure IV.37 presents the evolution of the total crack length *versus* total film stress. The total crack length was used instead of crack density as the experimentally observed crack network and modeled crack network were different (*i.e.* short cracks *versus* continuous cracks). Thus, direct correlation between the two densities is not possible. Experimental and numerical values (taking into account both copper plasticity and interface debonding)

are compared. The numerical analysis was carried out fixing σ_c at 109 MPa (as observed experimentally) and varying K_{Ic} for various initiation crack spacings. In this case, both Cu plasticity and interfacial cracking was considered.

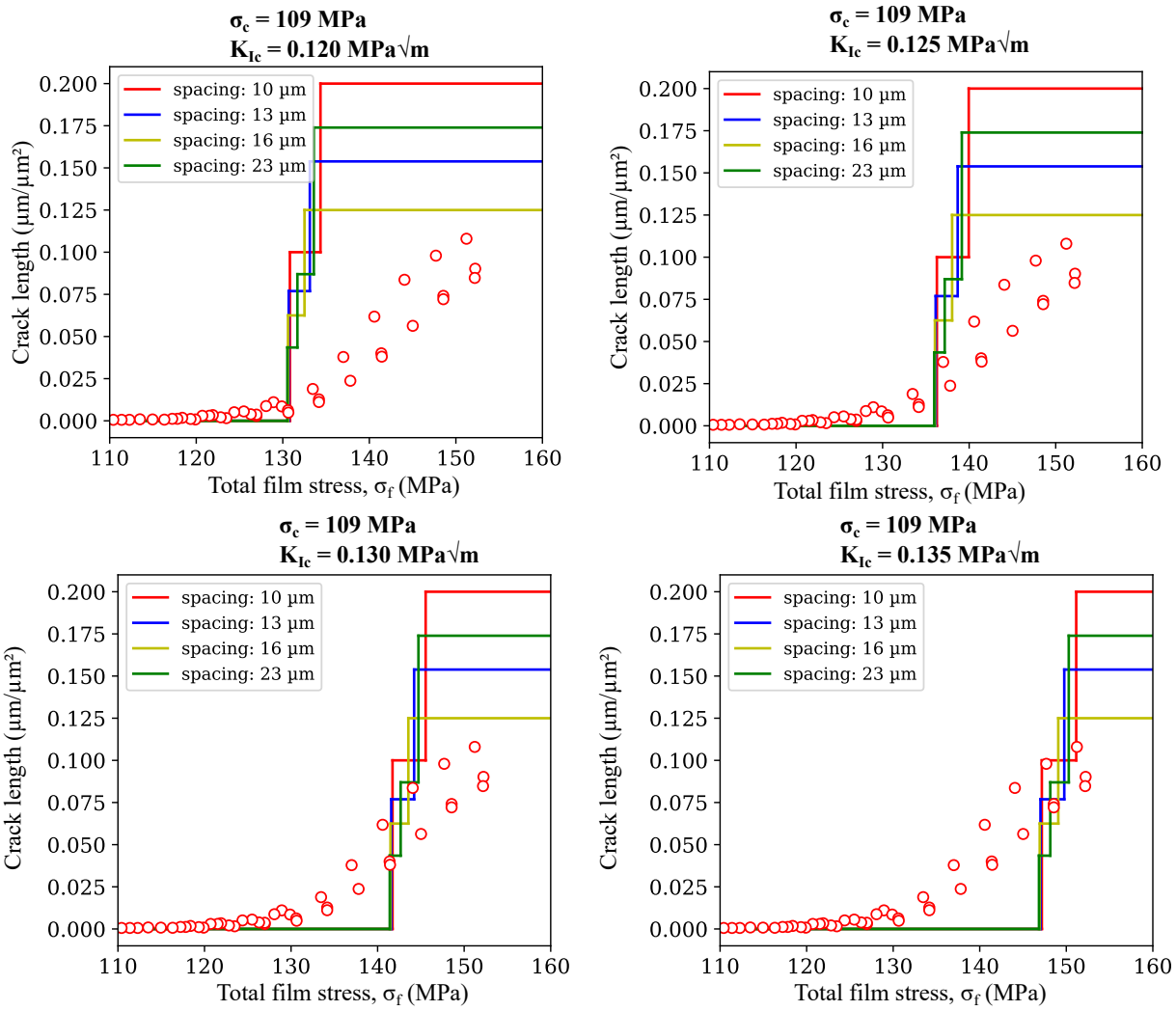


Figure IV.37: *Crack length versus total film stress: comparison between experimental and numerical results*

First, we note that the numerically predicted total crack length variation is in the same order of magnitude than the experimentally measured lengths even if the variation is steeper for the numerical results.

The maximal total crack length, with the spacing at the onset of the first crack of 16 µm, is predicted at 0.125 µm/µm^2, which is slightly higher than the saturation value obtained with the Mehl-Avrami-Johnson law at 0.108 µm/µm^2. Again, considering the different crack shapes and the complexity of the multi-cracking mechanism, the estimated value is satisfactory as compared to the experiments. Thus, we confirmed the efficiency of the coupled-criterion to predict multi-cracking in thin brittle films.

The prediction is very sensitive to variation of the toughness suggesting that the energy condition governs the cracking.

We note that this 2D model does not account for the crack growth. Indeed, the crack

lengths are equal to the sample width, so no short crack can be modeled. To try to explain crack morphology, a 3D model, which model the interaction between cracks, the copper layer plasticity and the interfacial crack along the SiN_xH_x/Cu interface, can be developed. However, this was out of the scope of this PhD and the reader may refer to the work of Le Druillenec, who proposed a 3D numerical analysis of the multi-cracking mechanism showing the existence of the two crack shapes (short and continuous) [30].

IV.4 Conclusion

In this chapter, a channel cracking experiment was developed to study the cracking mechanism of the porous SiOC:H layer and state on the sensibility of this material to stress-corrosion cracking.

Firstly, the behavior of the silicon substrate itself was studied through double-torsion testing. The results show the non-sensitivity of the silicon wafer cracking mechanism to environment and the fracture toughness was found to be equal to 0.88 MPa$\sqrt{\text{m}}$ for both a 775 µm and a 200 µm-thick silicon (100)-oriented wafers, in good consistence with literature values.

Then, the channel cracking experiments were conducted with two purposes: first, describe the damaging mechanism in the thin porous SiOC:H, and then state on the effect of environment on the crack growth. Preliminary, the double-torsion technique was found not relevant to crack only the thin upper film, so the four-point bending was chosen for the study.

To address the first objective, incremental loading tests were carried out *in situ* an electron scanning microscope. The results show that a short crack network formed in the porous SiOC:H and in the thin silicon nitride under-layer, accompanied by a partial interfacial cracking mechanism along the SiN_xH_y/Cu interface. The particular channel crack morphology is attributed to the presence of the 2 µm-thick copper interlayer below the cracked film and the low thickness of this latter. The array of short cracks was then described with three parameters: the density, the total length and the averaged spacing. The two first stages of the cracking test were observed when increasing the applied stress: the onset of cracking and the mid-point cracking. Unfortunately, the saturation phase was not clearly detected as the sample (silicon substrate) breaks before. From these tests, the critical stress for the onset of cracking is found to be equal to 109 MPa. The corresponding energy release rate considering a steady-state channel crack is calculated at 1.7 J/m^2 corresponding to a fracture toughness estimated at 0.11 MPa$\sqrt{\text{m}}$.

Then, the influence of the environment on the cracking mechanism is discussed. Constant loading tests at $\sigma_f = 110$ MPa were carried out under ambient, high vacuum and humidity-saturated environments. The results show a crack nucleation and propagation mechanism during the holding time with an accelerated mechanism under a humidity-saturated environment and a stable damage state for the tests performed under high

vacuum. Hence, a stress-corrosion cracking mechanism is confirmed for the pSiOC:H material. A perspective of this work is to perform the same kind of tests with different saline salts to better control the humidity level. Finally, the Mehl-Avrami-Johnson law was used to fit the total crack length *versus* time. The results show great correlation with a n factor of 0.7, indicating that crack nucleation rate is higher than the crack propagation rate, which agrees with the experimental observations.

A particular attention is payed in the last section to the numerical simulation of such experiment. Indeed, studying the fracture mechanism of a very thin film deposited on a highly brittle substrate could be very challenging experimentally. Thus, be able to numerically predict such behavior could be very helpful to avoid failure in more complex structures and to better understand the involved mechanisms. The experiment was simulated with the coupled criterion (stress and energy) to predict the onset of a periodic array of cracks and the multiplication phase. The predictions are satisfactory as we are in the same order of magnitude than the experimental results in terms of total crack length at saturation and predicted film fracture toughness.

CHAPTER V

Application to microelectronics

Throughout this manuscript, we highlighted the sensitivity of dielectric materials to environmental effects (*i.e.* temperature and humidity). We carried out two studies: (1) an experimental characterization campaign of their local mechanical properties under temperature cycling and temperature-humidity storage conditions; (2) an *in situ* small-scale fracture characterization of the most critical dielectric film, the *ultra-low k* porous SiOC:H, under different humidity conditions.

A discussion is now proposed to put these results into perspective regarding the industrial context of microelectronics. It is legitimate to ask whether the variations caused by aging observed in chapter III are critical to the reliability of the product. Similarly, we wonder to what extent could the results obtained in chapter IV on a simplified sample be transferable to a finished product.

Thus, this chapter first presents a numerical analysis to evaluate the effect of the dielectric properties variations on the Back End of Line (BEoL) stress fields. A multiscale finite element method is thus used to model the die and its package. Then, material (embedded in the BEoL integrated circuit) parameter's variability is discussed as well as other sources of variation in the integrated circuit, such as package material and geometry parameters.

Finally, the failure modes in different environmental conditions identified previously are compared with some of the most common failures observed during product qualification procedure. The similarities and differences in cracking mechanisms are highlighted and discussed.

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V.1 Introduction

The *low k* and *ultra-low k* SiOC:H materials were integrated in the newest nodes, so to improve the chip performance, reducing the RC delay thanks to their low dielectric constant. However, the durability of these materials is questioned because of their higher porosity fractions and lower mechanical resistances.

In this chapter, we propose a discussion to put into perspective the results of the previous chapters. Several items are hence discussed: (1) *How should we consider the variations in the mechanical properties after aging for the reliability of a product?* (2) *How can we interpret the failure mode and the critical threshold value obtained with the four-point bending tests regarding actual products, logically more complex?* (3) *How can the environmental effects observed in chapter V affect the product reliability?*

To answer these questions, first, a 3D numerical analysis was used to study the stresses in the chip. A particular attention was paid to the first levels of interconnections where these materials are integrated. The contribution of the potential influential factors was also discussed. A typical thermal loading step was reproduced numerically on a standard BGA[1] package. The stress fields obtained at T_0 and after temperature cycling (at TC1000, with modified properties) are compared. Finally, a discussion is proposed regarding the crack mechanisms observed in chapter IV. The failures occurring during the standard qualification procedures are compared with those found in this chapter. Their own characteristics are discussed, aiming to shed further the light on the results.

V.2 Effects of material aging on product reliability

This section aims to evaluate numerically the influence of environmental aging on the mechanical behavior of the chip. For this purpose, a finite element model was built and material properties were varied to detect any change in the local stress field in the interconnect part due to aging. Thus, the numerical results would help to evaluate the effects of the dielectric aging on the overall reliability.

V.2.1 Numerical model and parametric study

The chip-package interactions refer to the apparition of thermomechanical stresses within the die in presence of its package. These stresses mainly result from the difference in CTE between the different materials, which compose the integrated circuits. Thus, having a complete picture of stresses in the different materials requires to consider both the interconnect part and the package. However, because of the very detrimental scale ratio (*i.e.* **mm** for the package *versus* **nm** for the interconnections), a large amount of elements would be needed if a classical finite element method was used. To overcome this issue,

[1]Ball Grid Array

a multiscale modeling method was adopted, and detailed in [34, 105], and briefly summarized below. The finite element model was developed by the Mechanical and Thermal Modeling team at STMicroelectronics on Ansys software v19.

Numerical model

The multiscale modeling principle is based on the successive execution of two models: a macro-model (packaging) and a micro-model (interconnect part) (figure V.1). The main steps consist in:

1. Computing the macro-model to obtain the displacement field of the package. The applied loading is thermal, consisting in a temperature ramp from 150°C down to -50°C corresponding to the temperature range of one cycle, as defined in the automotive standard [1].

2. Defining the micro-model future location, *i.e.* where the package displacement or stress is maximum.

3. Applying the previously calculated displacement field as boundary conditions of the micro-model. The local stress field can be now computed for the interconnect layers at the lowest temperature (*i.e.* -50°C). We note that the stress-free state is assumed at the assembly temperature, thus at 230°C[2].

This approach provides a link between the two considered scales. Further details and method description can be found in [34, 42].

[2]This temperature corresponds to the liquidus temperature of the solder material.

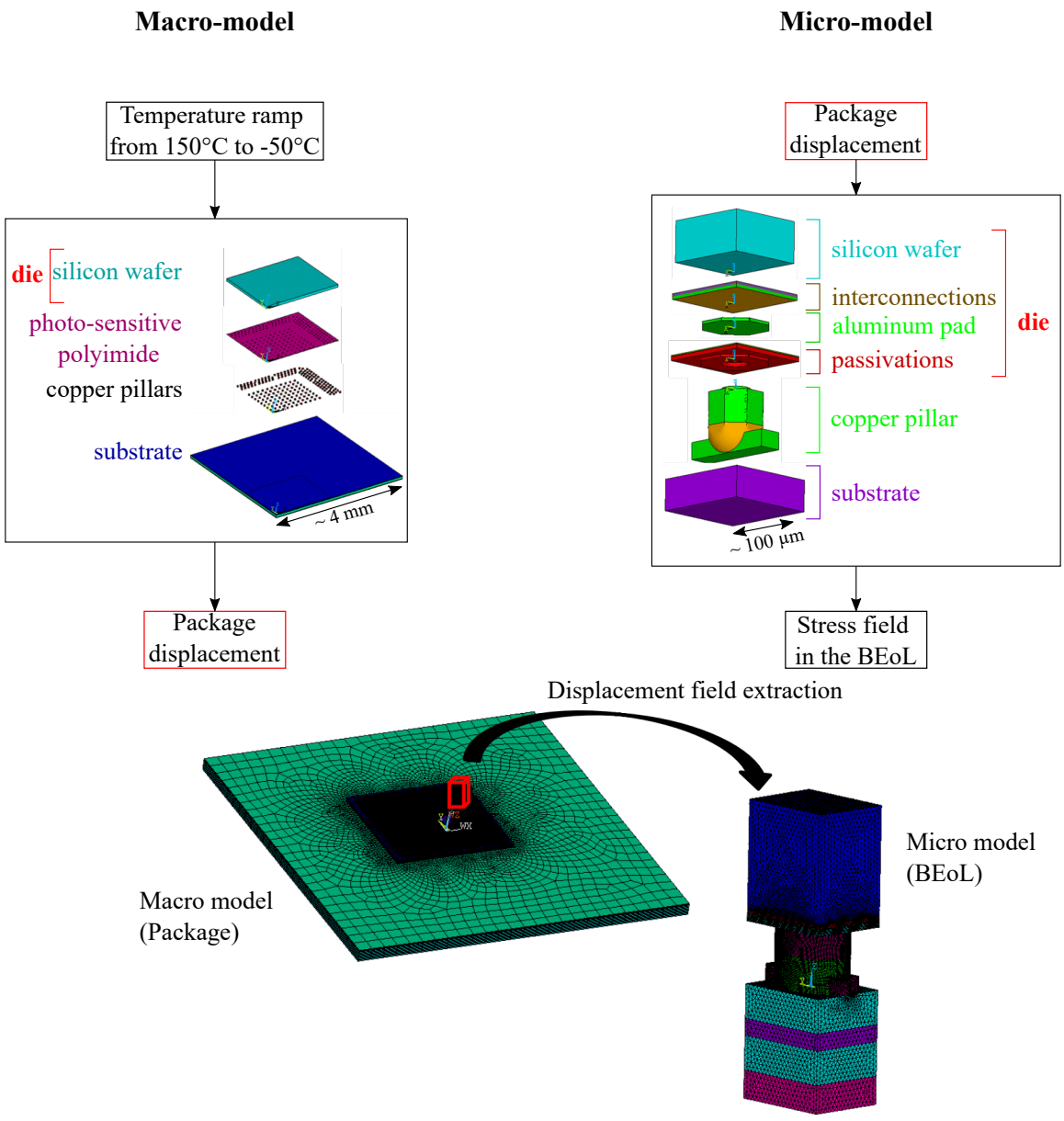

Figure V.1: *Multiscale modeling approach*

The macro-model represents a BGA package, which is arbitrarily chosen as an illustration. Indeed, various packages exist in microelectronics (BGA, QFP[3], Imager Packaging...). Only a quarter model (symmetry of the BGA package) is computed.

The package is connected to the die with the flip-chip technique (figure V.2). In our case, copper pillar bumps of diameter of 60 µm, made of 35 µm in height of copper and 10 µm in height of tin-silver alloy solder, connect the die to the printed-circuit board. Underfill is then injected by capillarity between the die and the PCB. This component allows to reduce and spread the stress at the BEoL level. At last, the die is encapsulated with a molding compound to prevent it against mechanical stresses and chemical attacks.

[3]Quad Flat Package

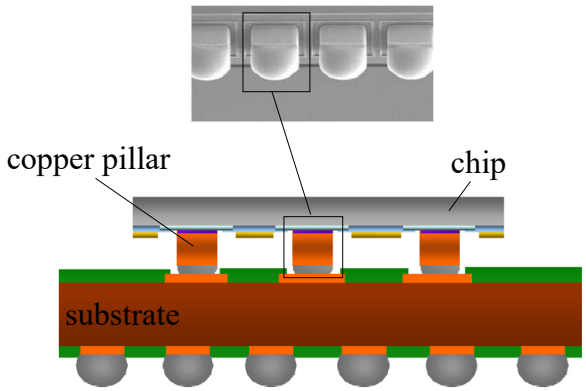

Figure V.2: *Schematic cross-section of an integrated circuit assembled by flip-chip with copper pillars (NB: molding compound is not represented here) (from [75])*

At the macroscale, the chip is modeled only as a silicon bulk, whereas at the microscale, the BEoL layers are detailed. However, even with a micro-model, the BEoL remains complex and needs to be simplified numerically. This is done through a homogenization technique, which consists in homogenizing the layer properties to avoid the meshing of all the geometrical details. Our model comprises 7 metal levels. The *low k* and *ultra-low k* SiOC:H materials[4] are found in the first metal levels (either one or the other), whereas the last metal levels are composed of more classical dielectrics, such as USG. At the top is found the passivation layers (SiN_xH_y and PSG). The substrate has a typical size of 8 mm by 8 mm, while the die has dimensions of 6 mm by 5 mm. All materials are considered as linear elastic.

Table V.2 summarizes all the layer thicknesses. Figure V.3 presents the detailed layers which compose a BGA package as well as the considered BEoL layers.

Table V.1: *Material properties used for the macro-model. Two values of E and CTE are given for temperature-dependent materials: they correspond respectively to the parameter considered below and above T_g.*

Macro-model	**E (GPa)**	ν	**CTE (ppm/°C)**	**T_g (°C)**
Resin laminate (core)	25 - 14	0.19	11 - 4	255
Copper (copper pillar)	121	0.30	16.3	-
DFSM[5](soldermask)	40	0.37	45 - 127	135
Epoxy-glass fibers (underfill)	11 - 0.08	0.35	31 - 95	107
Epoxy at T0 (MC)	24.2 - 1.6	0.37	8.5 - 37.8	105
Epoxy at TC1000 (MC)	25.0 - 2.7	0.37	8.5 - 37.8	120
Silicon (die)	131	0.28	2.6	-

[4]In actual product, the use of *low k* and *ultra-low k* materials depends on the RC requirements and also affects the thickness of the first level. This thickness modification is not reproduced here to simplify the analysis.

[5]Dry-film photoimageable

Layer	Thickness (µm)
Macro-model	
Core	200
Prepreg	18 (x2)
Solder mask	10 (x2)
Copper pillar	45
Polyimide	4.5
Die	300
BEoL (Micro-model)	
Passivation	1.10
Mz	0.88
Vz	0.88
Mx	0.10
Vx	0.08
M1	0.10
PMD[6]	0.28

Table V.2: *Thicknesses of the modeled layers*

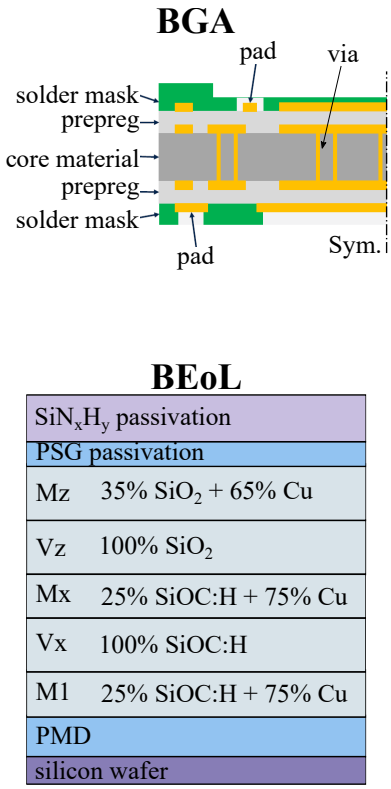

Figure V.3: *Detailed layers of BGA package and the BEoL considered*

Parametric study

The aim of this numerical study is to detect any influence of dielectric properties variation during temperature cycling on the stress field at the first metal level. This section lists the variations of the BEoL properties evaluated. The impact of molding compound properties and copper pillar height is also evaluated as comparative.

Most of macro-model materials properties are given by the manufacturers or issued from the literature (table V.1). The molding compound (MC) properties were measured through DMA and TMA[7] at the Material Characterization Lab at STMicroeletronics Agrate at T0 and also at TC1000.

Another considered variation is the height of the copper pillar. In this study, its height varies about +/- 10%. This value corresponds to the observed process variability of this parameter. Other various sources of variability (geometrical, recipes, tolerance...) exist and may contribute to modify the stress fields, but they are not considered here.

The dielectric materials reduced modulus, hardness and residual stress are measured by nanoindentation and wafer-curvature measurement in chapter III or result from previous STMicroelectronics internal characterizations. We recall the results of chapter III after 1000 thermal cycles in table V.3.

[6]Pre-Metal Dielectric

[7]Dynamical Mechanical Analysis and Thermo-Mechanical Analysis

Table V.3: *Temperature cyling influence on the mechanical properties of the dielectric materials (see chapter III)*

	Aging state	**E (GPa)**	σ_{res} **(MPa)**	CTE (ppm/°C)
SiN_xH_x	T0 / TC1000	146 / 142	-379 / -330	2.3
SiO_2:H	T0 / TC1000	65 / 64	-193 / -173	2.7
SiOC:H	T0b / TC1000	10.4 / 11.6	86 / 134	7.6
pSiOC:H	T0b / TC1000	9.9 / 11.3	104 / 34	10.8

Table V.4 presents the scenario for the parameter sensitivity analysis. The height of the Copper Pillar (CP) is set at the extreme values (+/-10%). For the molding compound as well as each dielectric layers, the properties are taken at T0 and at TC1000 for the analysis.

Table V.4: *Scenario for the sensitivity analysis*

Scenario	**CP**	**MC**	**SiN_xH_x**	**SiO_2:H**	**SiOC:H**	**pSiOC:H**
S1	-10%	T0	T0	T0	T0b	T0b
S2	-10%	TC1000	TC1000	TC1000	TC1000	TC1000
S3	+10%	T0	T0	T0	T0b	T0b

V.2.2 Results and discussion

At the macro-scale, results are analyzed at the lowest temperature (*i.e.* -50°C), where the stress level is expected to be the highest. Figure V.4 presents the deformation of the package. Its deformed shape is convex, with a maximal out-of-plane displacement about 70 µm at the substrate corners. It should be noted that fatigue effects due to multiple thermal ramp applications are not considered here.

Since we simulated the copper pillar layout with the macro-model, the stress of each copper pillar location can be evaluated. Below focus is done at the outermost copper pillar corresponding to the most stressed one. The vertical stress field at the copper pillar contact (i.e. copper/aluminum interface) is obtained via the micro-model and plotted in figure V.4. It is observed that the maximum stress occurs along the copper pillar footprint, clearly identifiable. The stress values at the SiOC:H level are thus computed along this path and maximum values are picked.

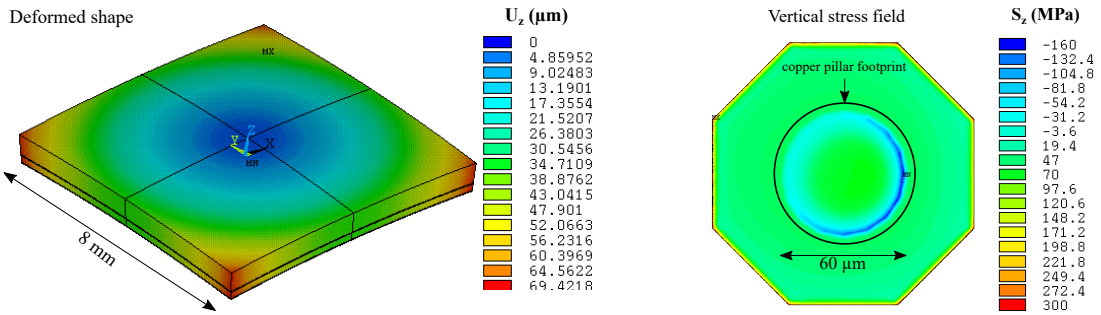

Figure V.4: *Numerical results at T = -50°C: (a) Macro-model: vertical displacement contours of the deformed package (b) Micro-model: stress fields within the aluminum pad at the copper pillar contact for the outermost copper pillar (i.e. where the stress is maximum)*

At the micro-scale, the stresses in the *low k* or *ultra-low k* layers are now discussed. As the *low k* and *ultra-low k* materials exhibit brittle failure behaviors, they are more likely to fracture under tension. Thus, the maximum first principal stress σ_I is reported (mainly out-of-plane), in order to assess such failure behavior in the BEoL (table V.5). Stress values are close to 100 MPa and the highest values are found for the *ultra-low k* configuration. The differences in the first principal stresses in both the *ultra-low k* and *low k* SiOC:H layers remain within 1% when varying both the material properties and the copper pillar height. Between S1 and S2, the materials properties were aged and this results in a slight increase in the stress level for both the SiOC:H and pSiOC:H layers. On the contrary, the increase of 10% of the copper pillar height slightly reduces both the stress levels of the SiOC:H and pSiOC:H layers.

Table V.5: *Numerical results of the maximal first principal stresses σ_I in the first metal level dielectric layers (SiOC:H and pSiOC:H) according to the scenario of table V.4*

σ_I (MPa)	SiOC:H	pSiOC:H
S1	95.8	113.4
S2	96.5	113.9
S3	95.5	113.0

The variations induced by aging have a limited impact on the stress field at the BEoL level. The main contributions come from the intrinsic CTE mismatch between the different components of the package. Hence, the aging effects on the BEoL dielectrics do not seem to play an important role on the long-term reliability.

In [146], Yang *et al.* reported a first principal stress from 40 to 90 MPa depending on the metal level considered for the integration of the *low k* material. In addition, Chang *et al.* reported, in their numerical parametric study, a first principal stress for the *low k* layer from 84 to 152 MPa when varying geometrical and material parameters [13]. Our

results are consistent with these studies regarding the assumptions of the models and considered material properties.

At this step, it is worth mentioning that the mechanical properties of the BEoL materials are neither monitored online nor subjected to specifications. Microelectronic industry focuses its attention on other parameters such as the refractive index or the thickness. The consequences are twofold: (1) it is difficult to compare the variations due to the aging with those due to the process variability (2) it is then implicitly expected that slight variations of the mechanical properties do not alter the overall reliability of the products. Regarding the residual stress, on certain risky products, this parameter is more closely monitored due to possible handling problem. However, the specification remains quite large with acceptable variations ranging from ± 50% to 100%.

These statements confirm our numerical analysis that the slight modifications of dielectric properties after aging do not act as major contributor on the overall reliability.

Modification of the properties due to inter-metallic compound growth or stress voiding should also be evaluated. Such very wide scope study is not addressed in this manuscript, but these effects should be considered with care in the future. Finally, and as discussed in the next section, the propagation of pre-defects may also explain critical failures.

V.3 *Ultra-low k* SiOC:H fracture behavior

V.3.1 Failure mode and threshold value

The calculated stresses for the *ultra-low k* porous SiOC:H are close to the critical stress of the first crack initiation of 109 MPa determined through the channel cracking experiments described in chapter IV. Dramatic and quite systematic failure should thus occur for this kind of configuration. That is not the case in the actual products, especially if we consider that the previous packaging step (*i.e.* reflow step when the die is assembled to the substrate) is considered usually as more critical for the BEoL stack as the underfill is not yet incorporated.

On one hand, the numerical values should be considered as comparative indicators, as there are several assumptions made on the inputs of the numerical analysis, a homogenization technique for the material properties, and a simplified elastic behavior for the bumps. Only a comparative study is relevant as the same method is kept between the different cases of study (*i.e.* sensitivity analysis). The quantitative results should be treated with caution.

On the other hand, the direct use of the experimental value in a complex structure may be questionable. In the literature, it was shown that the failure hazard of an interconnect structure depends on various parameters such as the loading, the arrangement and number of metal levels [10, 91, 89]. Furthermore, the question of the threshold value is intrinsically linked to the loading mode.

In our four-point bending tests, the pSiOC:H film cracks in pure tension. Thus, the cracking mode I is the most critical one. However, in a much more complex structure as interconnections, thus under a more complex loading, a mixed-mode loading does exist. This loading is induced by the assembly but also by residual stresses existing in the surrounding environment.

Another point to consider is the encapsulation of the pSiOC:H layer in the real product. Indeed, the *ultra-low k* SiOC:H is encapsulated with a silicon barrier. We suppose the encapsulation able to influence the cracking mechanism of the pSiOC:H by a possible local modification of its properties due to the process. In addition, Orain *et al.* showed that crack nucleation in *low k* layers can be enhanced by small stress-induced voids in copper and crack propagation by large voids showing the influence of the surrounding materials on the fracture of the *low k* materials [115].

In chapter IV, we observed a pattern of short mode I channel cracks with lengths from 5 to 10 µm at initiation. In parallel, in products, the most common characteristic of failures is a crack propagating in the *ultra-low k* SiOC:H layer, at the interface or parallel to it, with a length of several dozen of µm [10, 125]. The crack behavior is strongly affected by the presence of ductile materials, interfaces, residual stresses and stress state. Examples are given in figure V.5. It is thus not surprising to observe different failure modes on simpler samples, compared to those tested in this work. Hence, the results of the chapter IV have to be considered as a first step in the understanding of the cracking within a complex BEoL stack. A direct extrapolation of these results should be considered with care.

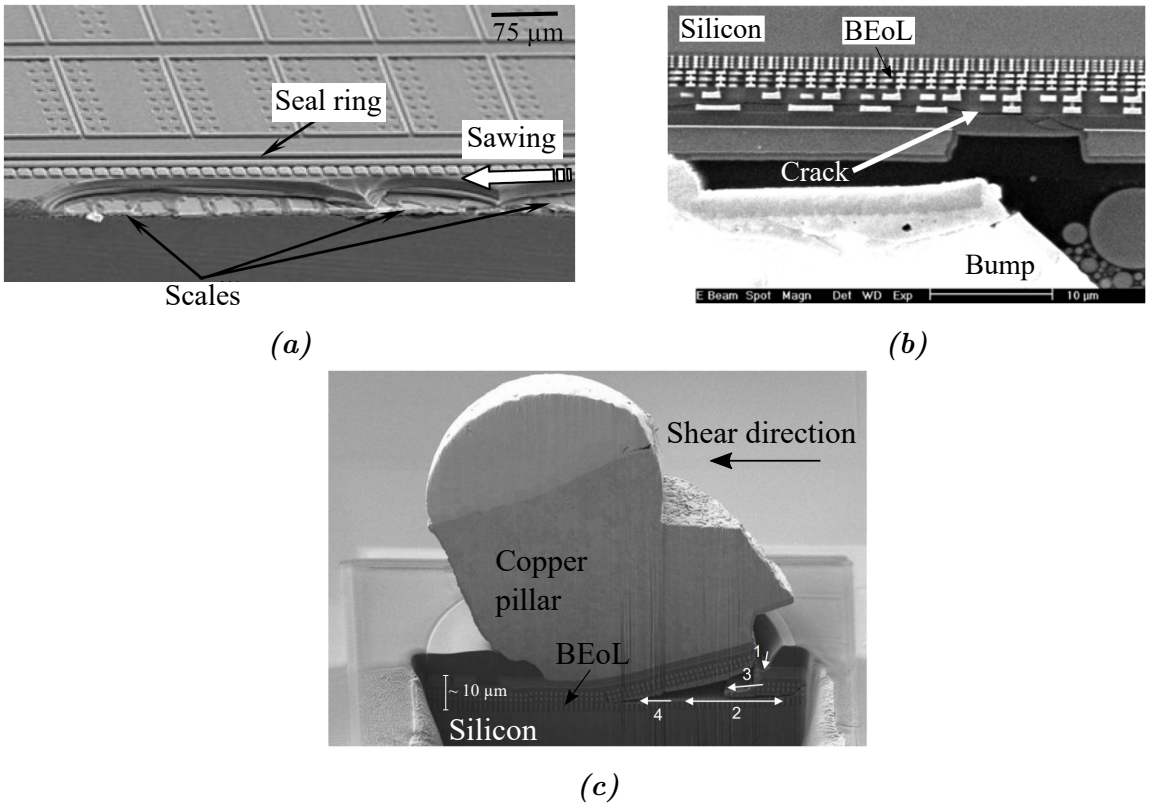

Figure V.5: *Failures in BEoL structures: (a) Large delamination scales induced by the sawing step during chip process, (b) Crack propagating across a BEoL structure under the bump [4], and (c) Brittle failure mechanism in low-k during bump shear qualification (1. Al pad cracking 2. Horizontal crack initiation in Y-level 3. First crack bifurcations towards the second 4. Intersection, merging and propagation of the two cracks in one) [130]*

V.3.2 Environmental effects

In addition to the failure mode itself, we clearly highlighted the detrimental effect of the environment on the sub-critical cracking mechanism in the pSiOC:H film in chapter IV, in particular the humidity effect. For both interfacial and cohesive cracking, influence of environmental conditions for classic dielectrics was discussed in literature, which shows considerable effects on the structure strength at critical loading (Kim *et al.* and Guyer *et al.* for the impact of CMP chemistry on the cohesive fracture of an *ultra-low k* dielectric through DCB testing [73, 50], Raid for the impact of humidity on the transition from interfacial to cohesive fracture in an *ultra-low k* film through four-point bending [125] as well as Lin *et al.* showing an adhesion energy decreasing from 7 J/m^2 downto 3 J/m^2 after water exposure of OSG[8]/SiN$_x$ stacks [90]). However, the sub-critical cracking of these materials and samples was less studied.

From an electrical point of view, the humidity degrades the RC characteristics of a material. It is now factually shown that the humidity also affects the crack kinetics. In

[8]OSG refers to OrganoSilicateGlass which is a kind of *low k* dielectric film.

order to protect the die from chemical degradation and crack propagation, a dedicated structure surrounded the die, the so-called seal ring structure, is embedded systematically in products. This structure is also used to stop potential crack propagation from the die edge. This is all the more important, as we know that the sawing step[9] creates defects in the BEoL. Hence, even without modification of the stress fields due to the aging, crack may propagate, enhanced by the humidity.

V.4 Conclusion

In order to put into perspective the properties variations in *low-k* and *ultra-low k* materials, observed in chapter III due to environmental aging, a numerical analysis was carried out. The parametric study showed that the dielectric properties variations had a limited impact on the BEoL stress fields, and therefore, on the reliability.

However, the critical threshold stress value experimentally determined in chapter IV seems low with respect to the stress fields obtained with the modeling. A direct comparison of the two sources is however risky due to assumptions of the adopted numerical model (elastic homogenized properties, simplified interconnect stack...). Moreover, local effects and different loading are expected to affect the failure mode as well as the effective resistance of the *ultra-low k* pSiOC:H integrated layer. These differences are in some ways expected and understandable regarding the more simple sample used to study the film fracture in chapter IV. However, this experiment allowed us to clearly show that the humidity influences the cracking mechanisms of the porous SiOC:H.

The studies made throughout this PhD have to be considered as a first step in the understanding of possible root-causes of products mechanical failure hazard. Nevertheless, our results show that deep experimental and computation analyses, besides the actual reliability tests performed on products, are required to deal with the material failure and product life expectancy, which are complex problems.

[9]The sawing step is performed during the packaging of the chips and consists in sawing the wafers into single dies.

General conclusions

With the trend towards an increasing integration density, new materials and architectures are constantly being developed to commercialize innovative products. Today, the mechanical reliability of these components, which embedded various natures of materials, has become a crucial concern of the microelectronic industry.

In this manuscript, a specific focus was done on the dielectric materials which composes the interconnect levels. Indeed, due to their poor mechanical properties and brittle behavior, most of the failures are the result of cracks in these materials. The challenge was placed in the considered scales (< 0.5 µm), causing many issues for implementing samples and testing mechanical properties.

The influence of the environment (temperature and humidity) on the dielectric materials integrity was studied. Two approaches were adopted: first, the sensitivity of a panel of dielectric materials to hydrothermal aging was evaluated, then, the influence of humidity level on the cracking mechanism kinetics of a *low k* porous SiOC:H film was studied.

Summary of results

Aging In the first part of this work, the accent was put on the aging mechanisms of PECVD-deposited dielectric films. Experimental characterizations through curvature measurement and nanoindentation at different aging states were carried out.

The samples were first submitted to process thermal treatment (10 cycles from 21 to 400°C), then to temperature cycling (1000 cycles from -50 to 150°C), and finally to temperature-humidity storage (85°C and 85% RH for 1000 hours) to cover the usual accelerated aging tests used in microelectronic industry. These tests are standardized in terms of temperature/humidity conditions and time.

It turns out that the passivation silicon nitride can be considered as an efficient barrier for protecting the interconnection stack from the environment thanks to its good mechan-

ical stability over the aging. Then, the undoped silicate glass were found to be stable during temperature cycling, while water components were absorbed during temperature-humidity storage. The highlighted mechanisms were absorption of water through Si network by forming silanols (Si-OH) as well as through Si dangling bonds by forming new Si-O-Si bonds. This resulted in a more compressive residual stress and decreased reduced modulus and hardness. We also found that a denser film showing a more compressive residual stress was less sensitive to water absorption than a less compressive and less dense film. Concerning the *low k* SiOC:H, this material was sensitive to both temperature cycling and temperature-humidity storage. The mechanisms are mainly related to hydrogen species absorption and desorption through silanol and/or methyl groups, traduced by slight variations of reduced modulus and hardness, while the residual stress was found to be more sensitive. The *ultra-low k* SiOC:H show sensitivity with temperature cycling and temperature-humidity storage with a variation of properties (especially the residual stress). With a simpler sample than the actual porous SiOC:H (*i.e.* only the core sub-layer), we show that most of the absorbed water during temperature-humidity storage may be into the pores with limited bonding to the Si network. Indeed, the limited mechanical properties degradation and the large amount of water absorbed promotes this assumption. For all films, the residual stress was found to be the most sensitive parameter to environmental aging.

About the fracture resistance determined by cube-corner nanoindentation, SiN_xH_y and SiO_2:H could not be evaluated due to the irrelevant fracture morphology obtained. Only the pSiOC:H has been studied. We found that the determined parameter was highly dependent on the residual stress of the film. Due to this strong dependence of calculated toughness on the residual stresses and the limitations of indentation-based fracture resistance evaluation, the values of toughness obtained must be taken as estimations rather than absolute values.

Cracking In the second part of this work, the cracking mechanism of the *ultra-low k* porous SiOC:H was studied. In this part, we validated a sample, cutting method, loading configuration, and a micro-machine, developed in-house, for *in situ* testing. The challenge mainly relied on two points: testing a sub-micron film to be as close as possible to industrial standards and founding a configuration to allow the fracture characterization with the material deposited on a silicon substrate. Indeed, modifying the film thickness requires to change the deposition and curing parameters which can affect the material structure. Moreover, silicon is the most common substrate used in microelectronic applications, and it is difficult to process these materials with a different substrate.

First, we confirmed the brittle behavior of the bare silicon substrate through *in situ* double-torsion testing and its non-sensitivity to stress-corrosion cracking.

Then, the cracking mechanism of the porous SiOC:H was described with three parameters: crack density, total crack length per unit area and crack spacing, showing a three

stage crack network development: onset of cracking, mid-point cracking and saturation. The crack shape is particular, *i.e.* a network of short cracks, whereas fast and continuous cracks are usually observed in brittle thin films. This particularity was attributed to the presence of the ductile and predominant (in terms of stiffness and thickness) copper inter-layer.

In order to determine the sensitivity of the porous SiOC:H to stress-corrosion cracking, relaxation tests were performed under ambient, high vacuum and humidity-saturated environments. We showed that both crack nucleation and crack propagation mechanisms occur under constant loading. Moreover, both mechanisms are highly accelerated with humidity, while under high vacuum neither additional crack nucleation nor further crack propagation were observed. Then, the Mehl-Avrami-Johnson law is used to fit the total crack length *versus* time curve. With this analysis, we show that crack nucleation rate is higher than crack propagation rate during constant loading test under ambient environments. Finally, the tests were modeled through finite element simulation with the coupled-criterion for fracture. The results are encouraging as the predictions are close to the experiments.

Application The last part of this work was dedicated to the contextualization of the results. Therefore, finite element numerical study was used to evaluate the impact of the properties variations observed in this work on the BEoL stress field. We conclude that the variations have a limited impact on the BEoL, and therefore, on the product reliability. Regarding the failure mode and the critical threshold value obtained in the experimental part, being said that more complex interactions and mechanisms in real product than in our sample are expected. These differences are expected and understandable.

Perspectives

The mechanical characterization of dielectric films regarding different environmental conditions has been proposed in this work. Many questions about these material integrity in long-term reliability were answered, and numerical applications were proposed. However, the thermo-mechanical behavior of the dielectric materials, especially the *ultra-low* k layer, as well as that of the product is not completely characterized and understood. We listed a few recommendations for further studies:

– In this work, we found that the aging mechanisms in dielectric materials do not seem to play a main role on the long-term reliability of products. We recommend further studies to investigate the aging mechanisms of other materials embedded in microelectronic components as metals and package materials. Fatigue mechanisms with mechanical cycling loads induced by temperature cycling may induce plasticity and/or hardening in metals. Moreover, package materials, mostly polymers, may be more sensitive to aging.

– The fracture tests performed in this work were done on basic samples to develop the method and to better understand the fundamentals of the crack mechanisms. Thus, it may be interesting to investigate more realistic samples (*i.e.* closer to microelectronic standard): (1) sample with simple copper patterning and *ultra low k* film to study the influence of the structure (*i.e.* stress concentration effects) (2) sample with an additional thin barrier layer on the top to reproduce the encapsulation effects on the loading mode of the *ultra low k* layer.

– The cracking experiments conducted in this work show promising results to study the stress-corrosion cracking of the *ultra-low k* material. However, in our experiments, it was difficult to monitor the crack growth rate due to electrons/sample interactions. We also propose the replacement of the copper inter-layer by another material, such as *low k* films, as literature studies show the efficiency of other barrier materials than metals. This in order to be able to observe the cracks under a light microscope (*i.e.* without copper microstructure) and avoid the ductile behavior beneath the studied film. The information of the crack growth rate according to the environment may be quite interesting in the frame of numerical investigations. It may be used to feed simulations of crack propagation under a given loading.

– In order to increase the reproducibility of the fracture experiments, we recommend to use saline solutions to better control the environment and to vary the couple (T, RH).

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Résumé

Dans un contexte très concurrentiel et riche d'innovations, l'industrie de la microélectronique propose des produits de plus en plus compacts présentant toujours plus de fonctionnalités. Pour augmenter leur performance, de nouveaux matériaux sont donc introduits tels que les diélectriques à faible permittivité, appelés diélectriques *low k*. Ces matériaux sont très performants d'un point de vue isolation. Cependant, leur résistance mécanique se voit divisée par dix par rapport à un oxide diélectrique standard, ce qui en fait la source de certaines défaillances de type fissuration. En effet, les composants sont soumis à de nombreuses variations de température et d'humidité pendant leur fonctionnement pouvant engendrer leur défaillance. L'intégrité mécanique des produits lors de leur utilisation est un facteur de différenciation déterminant vis-à-vis du marché et des compétiteurs. Dans cette optique, des tests de fiabilité sont systématiquement mis en place pour valider la tenue des produits dans le temps et le cas échant, la clarification des possible défaillances afin d'assurer un produit fiable aux clients.

Dans le cadre de cette thèse, nous nous proposons d'étudier plus précisément les mécanismes de défaillance mécanique liés aux matériaux diélectriques composant la structure d'interconnexions des puces électroniques. L'étude portera sur deux volets principaux : la modification intrinsèque des propriétés mécaniques des matériaux diélectriques liée à un phénomène de vieillissement ainsi que les phénomènes de fissuration des céramiques. Nous nous attacherons à étudier des films diélectriques au plus proche de la réalité, pour la majorité déjà en production sur le site de Crolles de STMicroelectronics.

Le manuscrit présente tout d'abord une mise en contexte bibliographique, dans le chapitre I, avec d'une part la présentation des tests de fiabilité, dont notamment le cyclage thermique et le stockage humide, utilisés dans ce travail. D'autre part, la mécanique de la rupture est introduite afin de définir les notions principales utilisées et de présenter la fissuration par corrosion sous contraintes dans les matériaux céramiques. Les matériaux et méthodes de caractérisations sont présentés plus en détails au chapitre II. Deux volets principaux seront étudiés par la suite. Le premier porte sur la caractérisation des propriétés mécaniques de ces diélectriques et de l'étude de leurs variations après vieillissement environnemental. Pour cela, la méthode de nanoindentation ainsi que la mesure de courbure de plaquettes sont utilisées pour caractériser les échantillons. L'ensemble des résultats est reporté dans le chapitre III. Le second volet de cette thèse consiste à quantifier le phénomène de fissuration par corrosion sous contrainte de l'oxyde de silicium poreux, connu pour sa faible tenue mécanique. Un protocole et un équipement dédiés aux tests mécaniques à l'échelle submicronique sont développés pour pouvoir suivre la croissance de fissures sous environnement contrôlé. Cette étude fait l'objet du chapitre IV. Les résultats expérimentaux de ces deux études sont finalement mis en perspective dans un contexte industriel, dans le chapitre V, à l'aide de simulations numériques.

Le chapitre I présente les tests de fiabilité établis pour le suivi des produits de la microélectronique. Ces tests sont définis par des normes notamment l'AEC (Automotive

Electronic Council) et la JEDEC (Joint Electron Device Engineering Council). La mise en place de ces tests systématiques est fondée sur :

1- La définition du mode de défaillance visé
2- La définition d'un modèle d'accélération adéquat
3- La définition des conditions de vieillissement accéléré selon le degré de fiabilité visé

Les principaux tests visant une défaillance mécanique sont présentés. Parmi eux, le cyclage thermique et le stockage sous humidité sont détaillés et seront utilisés pour vieillir les matériaux diélectriques. Les conditions standards, utilisées dans notre étude, sont -55°C à 150°C jusqu'à 1000 cycles pour le cyclage thermique et 85°C et 85% d'humidité relative pour le stockage thermique. Une compréhension de l'origine des défaillances mécaniques est nécessaire pour assurer la fiabilité des produits. Dans cet optique, la mécanique de la rupture est utilisée et également présentée au chapitre I. De plus, la notion de sensibilité des céramiques silicatées à la fissuration par corrosion sous contrainte est détaillée. Les mécanismes de sensibilité de la fissuration à la température et au taux d'humidité sont explicités. Des travaux existants sur les films diélectriques sont présentés et notamment l'utilisation d'échantillons plus épais que la réalité est soulignée (généralement supérieure au micron). Une attention particulière sera donc portée sur l'utilisation d'un film d'épaisseur inférieure au micron pour cette étude.

Le chapitre II s'attache à présenter les matériaux et méthodes de caractérisation utilisées tout au long de ce travail. Un panel de films diélectriques utilisés dans un empilement standard d'interconnexions a été étudié comprenant : (1) un film de nitrure passivation d'épaisseur 600 nm, qui est la couche de protection supérieure de l'empilement, (2) un film standard d'oxide de silicium utilisé dans les niveaux supérieurs également d'épaisseur 600 nm (3) un film d'oxide de silicium dopé au carbone (*low k)* d'épaisseur 560 nm et (4) un oxide de silicium poreux dopé au carbone (*ultra-low k*) d'épaisseur 220 nm. Ces deux derniers sont utilisés pour l'isolation des premiers niveaux d'interconnexions. En effet, dans ces premiers niveaux, la densité de cuivre est plus importante et l'utilisation de matériaux à faible permittivité permet une meilleure isolation électrique des interconnexions métalliques. Tous les films sont déposés par PECVD sur des plaquettes en silicium de 300 mm de diamètre. Pour le suivi des propriétés mécaniques des films, deux méthodes sont utilisées : (1) la mesure de courbure de plaquettes pour évaluer leur contrainte résiduelle et (2) la nanoindentation avec une pointe Berkovich pour leur module réduit et leur dureté et une pointe Cube Corner pour leur résistance à la fissuration. Ces méthodes sont choisies afin de pouvoir évaluer les propriétés des films directement déposés sur les plaquettes en silicium. Pour étudier la sensibilité du film poreux d'oxide de silicium dopé au carbone à la fissuration, la flexion quatre points est utilisée. Cette méthode a déjà fait ses preuves dans la littérature pour l'initiation et la propagation de fissures canalisées dans un film déposé sur un substrat. Des essais de double-torsion sont menés au préalable pour évaluer la sensibilité du substrat en silicium seul à la fissuration par corrosion sous contrainte. Cette méthode a pour avantage sa capacité à générer des fissures stables dans des matériaux fragiles.

La première partie du travail expérimental de cette thèse expose donc dans le chapitre III la caractérisation mécanique des films diélectriques soumis à différentes conditions de vieillissement accéléré, alignées avec les standards de l'automobile. En premier lieu, dix cycles de 21 à 400°C sont effectués sur les deux diélectriques dopés au carbone (*low k* et *ultra-low k*),

permettant de simuler le budget thermique subis par ces deux matériaux lors de la fabrication des interconnexions. En effet, étant déposés durant les premières étapes, ils subissent des cycles en température correspondant aux dépôts des autres couches diélectriques supérieures. Par la suite, l'ensemble des échantillons sont soumis à un cyclage thermique de -55°C à 150°C pendant 1000 cycles puis à un stockage humide à 85°C et 85% d'humidité relative pendant 1000 heures. Les propriétés mécaniques suivies sont la contrainte résiduelle des films, le module réduit et la dureté pour tous les films ainsi que la résistance à la fissuration. Il est à noter que pour cette dernière, seul l'oxide de silicium poreux dopé au carbone (*ultra-low k*) (avec un film d'épaisseur 740 nm) a permis d'obtenir des fissures cohésives sans décollement du film par rapport au substrat en silicium. Les autres matériaux ne sont donc pas évalués sur ce paramètre. Toutes les propriétés sont mesurées après le dépôt du film, au cours du cyclage thermique (une mesure à 500 et 1000 cycles) et au cours du stockage humide (une mesure à 250, 500 et 1000 heures). Les résultats de cette étude ont montré que :

- Le film de nitrure de silicium est mécaniquement stable quelles que soient les conditions de température et d'humidité étudiées. Il assure bien sa fonction de barrière de protection contre l'environnement.
- Le film d'oxide de silicium étudié montre des variations limitées pendant les vieillissements. On note tout de même une affinité du film avec l'eau qui se traduit par une diminution de son module réduit et de sa dureté (11% et 19%) ainsi qu'une augmentation de sa contrainte en compression (19%). En revanche, ce film étant initialement très compressif (-193 MPa), à des contraintes plus modérées (-60 MPa), un film similaire d'oxide de silicium est plus sensible à la reprise d'eau avec des propriétés mécaniques diminuant d'en moyenne 30% et une contrainte résiduelle en compression ayant quasiment doublée (passant de -60 MPa à -188 MPa après stockage humide). La reprise d'eau est supposée via deux mécanismes simultanés :

$$(1)\ \text{Si-O-Si} + H_2O \rightarrow 2\text{SiOH}$$

$$(2)\ 2\text{Si} + H_2O \rightarrow \text{Si-O-Si} + H_2$$

- La première correspondant à la reprise d'eau sous forme de groupes OH générés après rupture de liaisons Si-O-Si, mécanisme largement décrit pour les matériaux verres. La deuxième est responsable de l'augmentation des contributions Si-O-Si observées en FTIR après stockage sous humidité, nouvelles liaisons générées par la reprise d'eau par liaisons Si pendantes, présentes initialement dans le film d'oxide déposé par PECVD. Néanmoins, les propriétés mécaniques ayant diminué, le mécanisme (1) est supposé dominant.
- Le film d'oxide de silicium dopé au carbone (*low k*) est nettement plus sensible au vieillissement environnemental. En effet, ses propriétés mécaniques, et surtout sa contrainte résiduelle, montre de fortes variations (augmentation de 56% de sa contrainte résiduelle en tension après cyclage thermique et diminution de 40% après stockage humide). Après analyse FTIR, ces variations sont supposées fortement liées à des mécanismes d'absorption/désorption d'eau.
- Le dernier film étudié, l'oxide de silicium poreux dopé au carbone (*ultra-low k*), est également plus sensible aux effets d'environnement, et surtout au stockage humide. En étudiant un échantillon-modèle plus simple, il a été supposé que la reprise d'eau se fait essentiellement à travers le réseau de pores sans liaisons fortes avec la structure du

matériau. Cette hypothèse corrèle avec des propriétés mécaniques qui varient peu mais une reprise en masse du film significative après stockage sous humidité. La résistance à la fissuration de la couche à 740 nm a montré des variations significatives pendant les vieillissements. Cependant, ce paramètre étant extrêmement sensible à la variation de la contrainte résiduelle du film, c'est celle-ci qui est primordiale.

Le chapitre IV traite des résultats obtenus lors des essais de fissuration du film poreux d'oxide de silicium dopé au carbone. Pour effectuer les essais de fissuration (flexion quatre points et double-torsion), une micromachine dédiée a été fabriquée selon les critères suivants :

- Les essais de fissuration de films submicroniques doivent être répétables.
- L'initiation et l'avancée des fissures doivent pouvoir être suivies et mesurables.
- L'avancée des fissures doit être contrôlée afin de pouvoir être dans un régime de fissuration sous critique pour le mécanisme de corrosion sous contrainte.

Les essais doivent pouvoir se faire sous environnement contrôlé afin d'étudier le mécanisme de corrosion sous contrainte. Les différents tests ont par la suite montré l'adéquation des caractéristiques de la machine avec nos objectifs.

Dans un premier temps, il a été montré que les substrats en silicium d'épaisseur 775 µm et 200 µm, sur lesquels sont fabriqués les puces électroniques, ne sont pas sensibles au mécanisme de corrosion sous contrainte grâce à des essais de double-torsion. Des tests similaires ont été pratiqués sur la configuration avec film mais le substrat étant très rigide et très fragile, la fissuration de ce dernier s'est trouvée être le mécanisme dominant de l'essai. C'est pourquoi, des essais de flexion quatre points ont été pratiqués par la suite. La configuration d'échantillons choisie utilise une inter-couche métallique en cuivre d'épaisseur 2 µm, celle-ci servant de barrière pour contenir la fissure dans le film supérieur sans endommager le substrat. Le substrat en silicium a été aminci de 775 µm à 400 µm pour favoriser la fissuration dans le film. Les premiers tests ont été pratiqués à chargement incrémental afin de générer un réseau de fissures dans le film et d'étudier son évolution avec l'augmentation de la contrainte. Il en est ressorti que dans ce type de configuration (film mince + inter-couche métallique), un réseau de fissures courtes est généré. Des paramètres de suivi du réseau de fissures ont été définis : la densité de fissure, la longueur totale de fissure par unité d'aire ainsi que l'espacement moyen entre deux fissures. Une évolution de type : nucléation aléatoire – fissuration intermédiaire – saturation a été observée. La présence de l'inter-couche en cuivre est supposée responsable de la morphologie de la fissure. En effet, sans présence d'inter-couche métallique ou en présence d'une inter-couche d'épaisseur plus petite que le film fragile supérieur, le mécanisme observé dans la littérature est une fissuration longue et continue du film. En plus, il a été montré qu'environ 20% des fissures sont accompagnées de décollement entre la couche fragile supérieur et le film de cuivre. A partir de la fissuration confinée dans le film d'oxide de silicium poreaux dopé au carbone, il est possible d'approximer le taux d'énergie critique du film G estimé à 1.7 ± 0.3 J/m², correspondant à une ténacité K_{IC} égale à 0.11 ± 0.01 MPa$\sqrt{m}$. Cette valeur corrèle avec le paramètre de fissuration obtenu par nanoindentation, lui étant estimé à 0.10 ± 0.02 MPa$\sqrt{m}$. Ensuite, des tests à chargement constant ont été pratiqués à différents taux d'humidité afin d'étudier l'influence de celui-ci sur la fissuration de l'oxide de silicium poreux. Il a été montré que la nucléation et la propagation des fissures sont fortement accélérés par la présence d'eau, confirmant une sensibilité forte de ce matériau à l'environnement. Au

contraire, des essais sous vide *in situ* MEB confirment que sans la présence de l'eau, le mécanisme ne s'active pas (pas de nucléation ni de propagation de fissures).

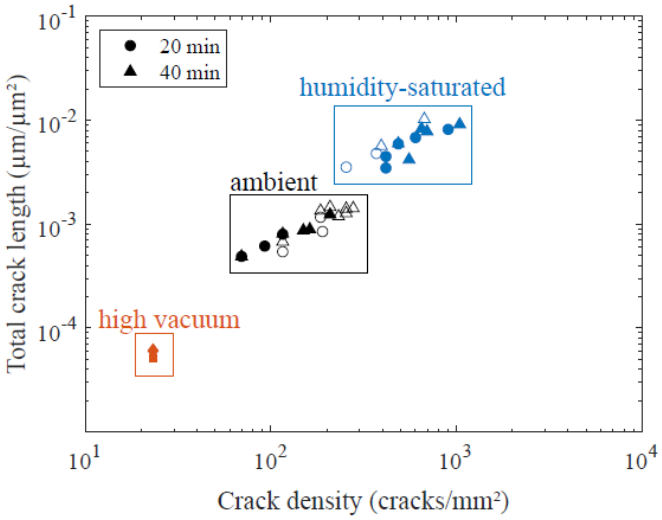

Figure 1 - Influence de l'environnement sur les paramètres longueur totale de fissure versus densité de fissure pour un film d'oxide de silicium poreux dopé au carbone

Le mécanisme observé étant de type nucléation-croissance, nous avons proposé de corréler une loi de Mehl-Avrami-Johnson (MAJ) aux résultats expérimentaux en utilisant la longueur totale de fissure. Cela a permis de montrer que le processus de nucléation est prédominant à celui de propagation des fissures avec un paramètre de loi *n* égal à 0.7 pour les essais à environnement ambiant.

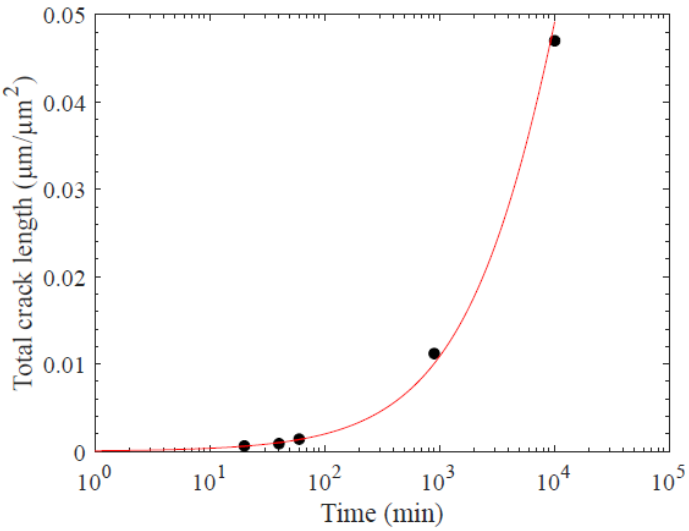

Figure 2 - Longueur totale de fissure par unité d'aire versus temps et corrélation avec la loi de Mehl-Avrami-Johnson

Enfin, une étude numérique a été effectuée basée sur un critère couplé, combinant une analyse en énergie et en contrainte. Cette étude est une première approche à la simulation numérique de ces phénomènes de fissuration de film mince ouvrant la porte à des études sur échantillons plus complexes où l'étude expérimentale peut s'avérer beaucoup plus difficile. En effet, les résultats ont montré une bonne corrélation entre la simulation

numérique et l'expérience avec un bornage de K_{IC} de 0.12 à 0.14 MPa√m pour une contrainte critique de 109 MPa.
Le dernier chapitre de ce manuscrit regroupe les résultats obtenus dans les deux études précédentes et permet d'en discuter la pertinence vis-à-vis des défaillances observées dans un produit fini. Pour cela, la simulation numérique est utilisée. Une approche multi-échelle a permis de modéliser les champs de contraintes observés dans l'empilement d'interconnexions lors d'une étape d'assemble boitier standard. L'étude porte alors sur l'impact de la variation des propriétés mécaniques des matériaux diélectriques (mesurées au chapitre III) sur le champ de contrainte. Les résultats ont montré une faible variation de 1% de la contrainte observée dans l'oxide silicium poreux dopé au carbone. Nous pouvons conclure que les variations des propriétés mécaniques (contrainte résiduelle, module réduit et dureté) observées pendant les vieillissements accélérés ne semblent pas à l'origine des défaillances de type fissuration observées dans les puces. En revanche, les valeurs numériques de contraintes sont proches de celles obtenus expérimentalement dans le chapitre IV lors de la fissuration du film, supposant un risque systématique de défaillance élevé non réaliste (en configuration standard). Dès lors, les valeurs obtenues par simulation numérique sont à considérer comme un ordre de grandeur considérant les simplifications du modèle associé. En plus, nous pouvons noter que la fissuration d'une structure d'interconnexions est un mécanisme bien plus complexe que celui adressé sur des films monocouches comme dans cette thèse. Néanmoins, un mécanisme de corrosion sous contrainte du film, qui expliquerait une défaillance à long terme, n'est pas à proscrire vue la sensibilité de celui-ci à la présence d'eau. Cette présente étude est donc à considérer comme une première approche et ouvre la porte à des essais sur échantillons plus complexes, et donc plus proche de la réalité.

Pour conclure, dans cette thèse, l'influence de l'environnement sur l'endommagement de films diélectriques utilisés dans l'empilement d'interconnexions d'une puce électronique a été étudié. Il a été montré que le vieillissement de ces matériaux sous cyclage thermique et stockage humide ne semble pas être responsable des défaillances observées dans le produit fini. Cependant, nous avons montré la sensibilité significative de la fissuration des films *'ultra-low k'* à la présence d'eau avec un mécanisme de nucléation et de propagation de fissure accéléré. En perspectives, nous proposons de poursuivre le travail expérimental engagé ici sur des échantillons plus complexes comprenant des motifs de cuivre par exemple mais aussi avec des temps plus longs. De même, un meilleur contrôle du taux d'humidité (via l'utilisation de solutions salines par exemple) est conseillé pour améliorer la reproductibilité. De plus, il serait intéressant d'élargir l'étude de vieillissement à d'autres matériaux tels que les polymères constituant les boitiers, directement exposées à l'environnement extérieur et très sensibles aux cycles thermo-hydriques, ou les métaux.

FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : RUBECK
(Avec précision du nom de jeune fille, le cas échéant)

DATE de SOUTENANCE : 08/07/2022

Prénoms : Sarah Elisabeth

TITRE : Investigation of aging and cracking mechanisms in advanced ceramic materials for microelectronics

NATURE : Doctorat

Numéro d'ordre : 2022LYSEI065

Ecole doctorale : Ecole Doctorale Matériaux de Lyon

Spécialité : Matériaux

RESUME :
Dans l'industrie de la microélectronique, l'intégrité mécanique des produits lors de leur utilisation est un facteur de différenciation déterminant vis-à-vis du marché et des compétiteurs. En effet, les composants sont soumis à de nombreuses variations de température et d'humidité pendant leur fonctionnement pouvant engendrer une dégradation de leurs matériaux et in fine, leur défaillance. Dans le cadre de cette thèse, nous nous proposons d'étudier plus précisément ces mécanismes. Plus particulièrement, les matériaux diélectriques, notamment l'oxyde de silicium poreux connu pour être le foyer de nombreuses défaillances mécaniques, seront étudiés. Ce travail est constitué de deux volets principaux. Le premier porte sur la caractérisation des propriétés mécaniques d'un panel représentatif de matériaux diélectriques et de l'étude de leurs variations après vieillissement environnemental. Pour cela, la méthode de nanoindentation ainsi que la mesure de courbure de plaquette sont utilisées pour caractériser les échantillons. Le second volet consiste à quantifier le phénomène de corrosion sous contrainte de l'oxyde de silicium poreux, connu pour sa faible tenue mécanique. Un protocole et équipement dédiés à l'échelle submicronique sont développés pour pouvoir suivre la croissance de fissures sous environnement contrôlé. Ces deux études ont permis de montrer d'une part, que le vieillissement hydrothermal induit une variation limitée des propriétés mécaniques des matériaux diélectriques. D'autre part, nous montrons que le mécanisme de fissuration de l'oxyde de silicium poreux est accéléré par la présence d'eau. Pour chacune de ces études, des simulations numériques sont proposées pour mettre en perspective et approfondir les résultats. Finalement, une meilleure connaissance sur les phénomènes de vieillissement des matériaux diélectriques utilisés dans la microélectronique est apportée. Notamment, les effets d'environnement sur les processus de fissurations de l'oxyde de silicium poreux ont pu être quantifiés grâce à un nouveau protocole, ouvrant ainsi la voie à de possibles évaluations sur des empilements plus complexes.

MOTS-CLÉS :
Microélectronique / Interconnexions / Matériaux diélectriques / Céramiques / Films minces / Vieillissement environnemental / Nanoindentation / Fissuration sous critique / Multi-fissuration / Simulation mécanique

Laboratoire (s) de recherche : MATEIS

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